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# High-Speed MOS ICs for a Signal Processor Input Interface of an Optical Synchronous QPSK Receiver and Related Clock Distribution Issues

Zur Erlangung des akademischen Grades

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Dedicated to

# MY LATE PARENTS

*for giving me their unconditional support*

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Zusammenfassung der Dissertation:

# Hochgeschwindigkeits MOS ICs für eine Signalprozessor-Eingangsschnittstelle eines optischen synchronen QPSK Empfängers und entsprechende Taktverteilungsprobleme

**Vijitha Rohana Herath**

Das exponentielle Wachstum des Internetverkehrs macht es notwendig, die Übertragungskapazität der optischen Hauptverbindungen zu vergrößern. Zurzeit arbeitetet der größte Teil der Hauptinternetverbindungen mit Datenraten bis zu 10 Gbit/s (OC-192/STM-64). Die Erhöhung der Kapazität der vorhandenen Übertragungssysteme durch neuartige Modulationstechniken ist eine Lösung. Die Quadraturphasenumtastung (QPSK) mit Polarisationsmultiplex vierfacht die Kanalkapazität gegenüber dem Intensitätsmodulationsschema. Die synchrone QPSK Übertragung mit Return-to-Zero (RZ)-Codierung und Polarisationsmultiplex erscheint als die vielversprechendste Weise, die vorhandenen Faser-Verbindungen auszubauen. Diese Modulationstechnik kann vorhandene 10 Gbit/s-Verbindungen zu 40 Gbits/s steigern. Das von der EG-Kommission geförderte synQPSK-Projekt zielte darauf, die gewerblich nicht verfügbaren Komponenten des synchronen QPSK Übertragungssystems zu entwickeln. Das phasenrauschtolerante Takt und Datenrückgewinnungsmodul ist ein solcher Bestandteil, der entwickelt wird. Dieses Modul schließt A/D-Wandler und eine digitale Signalverarbeitungseinheit (DSPU) ein. Die nominelle Datenrate eines A/D-Wandler-Ausgangkanals ist 10 Gbit/s. Das A/D umgewandelte empfangene Signal wird dann in die DSPU verarbeitet. Die DSPU ist in CMOS Technologie entworfen, um die Kosten der Herstellung und den Stromverbrauch zu reduzieren. Das Standardzellenmodul der DSPU kann nicht mit 10 GHz Taktfrequenz funktionieren. Deshalb ist es notwendig, eine individuell angepasste Eingangsschnittstelle für den CMOS DSPU zu entwickeln. Die Schnittstelle reduziert die Eingangsdatenrate auf ein Niveau das die Standardzellen DSPU verarbeiten kann. Diese Doktorarbeit präsentiert das Design der Eingangsschnittstelle der synchronen QPSK Empfänger DSPU (mit und ohne Polarisationsmultiplex). Die Schnittstelle wurde in 130 nm CMOS Technologie entworfen. Es schließt einen 1:8 DEMUX Stufe und einen quellengekoppelte FET Logik zu CMOS Logikkonverter Stufe ein. Die Doktorarbeit bespricht die Designprobleme von verschiedenen Schaltungsblöcken der Schnittstelle sowie den Schaltungsentwurf. Die Simulations- und Testergebnisse sowohl der Schnittstelle, des alleinstehenden Frequenzteiler-Chips, als auch des 1:2 DEMUX Chips werden besprochen. Die Simulationsergebnisse von Ultra-Hochgeschwindigkeitsmodulen werden auch präsentiert. Außerdem präsentiert diese Doktorarbeit eine Methode um den Erwartungswert der Taktungenauigkeit von einem ausgeglichenen H-Baum-Takt-Verteilungsnetz in Anwesenheit von zufälligen Prozess-Schwankungen und ungleichförmiger Substrat-Temperatur zu schätzen.

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Abstract:

**High-Speed MOS ICs for a Signal Processor Input Interface of an Optical Synchronous QPSK Receiver and Related Clock Distribution Issues**

**Vijitha Rohana Herath**

The exponential growth of the internet traffic makes it necessary to increase the transmission capacity of the backbone optical transmission system. At present most of the internet backbone operates at data rates up to 10 Gbit/s (OC-192/STM-64). Upgrading the capacity of the existing transmission systems using novel modulation techniques is one solution. The Quadrature PSK (QPSK) with polarization multiplex quadruple channel capacity over the intensity modulation scheme. The synchronous QPSK transmission with return to zero (RZ) coding and polarization division multiplexing emerge as the most promising way of upgrading the existing fiber links. This modulation technique can upgrade existing 10 Gbit/s links to 40 Gbit/s. The European commission funded synQPSK project aimed at developing the commercially unavailable components of the synchronous QPSK transmission system. The phase noise tolerant clock and data recovery module is one such component that is being developed. This module includes A/D converters and a digital signal processing (DSP) unit. The nominal data rate of an A/D converter output channel is 10 Gbit/s. The A/D converted received signal is then processed in the DSP unit. The DSP unit is designed using CMOS technology in order to reduce the cost of fabrication and the power consumption. The standard cell module of the DSPU can not operate at 10 GHz clock frequency. Therefore it is necessary to develop a full custom input interface for the CMOS DSPU. The interface reduces the input data rate to a level the standard cell DSPU can process. This dissertation presents the design of the input interface of the synchronous QPSK receiver DSPU (with and without polarization multiplex). The interface was designed using 130 nm bulk CMOS technology. It includes a 1:8 DEMUX stage and a source coupled FET logic to CMOS logic converter stage. The dissertation discusses the design issues of various circuit blocks of the interface as well as the layout. The simulation and test results of both interface, stand alone static frequency divider chip, and 1:2 DEMUX chip are discussed. The results of the simulation of ultra high speed circuit modules are also presented. Furthermore this dissertation presents a method of estimating the expected value of the skew of a balanced H-tree clock distribution network in the presence of random process variations and nonuniform substrate temperature. The proposed algorithm can estimate the expected value of the clock skew when the substrate temperature is non uniform with higher degree of accuracy. The simulation and calculation results are compared to verify the claim.

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Paderborn, Germany — Vijitha Rohana Herath
March 10, 2009

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# List of Important Symbols

| | | |
|---|---|---|
| $c$ | Velocity of the light | m/s |
| $C_{gs}$ | Gate-source capacitance of the MOS transistor | F |
| $C_{gd}$ | Gate-drain capacitance of the MOS transistor | F |
| $C_{ox}$ | Capacitance per unit area of the gate oxide | $F/m^2$ |
| $f$ | Frequency | Hz |
| $f_T$ | Transit frequency of the MOS transistor | Hz |
| $g_m$ | Transconductance of the MOS transistor | S |
| $I_D$ | Drain current of the MOS transistor | A |
| $S_{ii}$ | Scattering parameters | - |
| $Z_0$ | Characteristic impedance | Ω |
| $V_{TH}$ | Threshold voltage of the MOS transistor | V |
| $V_{DS}$ | Drain-source voltage of the MOS transistor | V |
| $V_{GS}$ | Gate-source voltage of the MOS transistor | V |
| $\chi$ | Clock skew | s |
| $\varepsilon_r$ | Relative permittivity | - |
| $\gamma$ | Chromatic dispersion index factor | - |
| $\lambda$ | Wavelength | m |
| $\varphi_s$ | Signal phase angle | rad |
| $\varphi_{LO}$ | Local oscillator signal phase angle | rad |
| $\varphi_{IF}$ | Intermediate frequency signal phase angle | rad |
| $\omega$ | Angular frequency | rad/s |
| $\omega_s$ | Signal angular frequency | rad/s |
| $\omega_{LO}$ | Local oscillator signal angular frequency | rad/s |
| $\omega_{IF}$ | Intermediate frequency signal angular frequency | rad/s |
| $\mu_n$ | Mobility of electrons | $m^2/V.s$ |

# Chapter 1

# Introduction

## 1.1 Background

The history of telecommunication dates back to the beginning of the human civilization. The methods of telecommunication have gradually been improved, from smoke signals to telegraphs and to first coaxial cables by 1940s. These developments were a result of human need for reliable long distance communication. But, certain fundamental limitations restricted electrical and microwave systems performances. Electrical systems were limited by their small repeater spacing due to attenuation while the microwave communication speed was limited by the carrier frequency [1].

Optical carrier understood to have distinct advantages such as extremely low loss, high data carrying capacity, and immunity from electromagnetic interferences. But, due to the unavailability of coherent light sources and suitable transmission medium, Optical communication did not come into fruition until later. The development of lasers in 1960s and the development of optical fibers in early 70s laid the foundation for the commercial optical fiber communication. The first commercial optical communication system was commissioned in late 70s, which operated at wavelengths around 850 nm. GaAs semiconductor lasers, and multimode graded index fibers were used in this system. Early optical fiber communication (OC) systems were dispersion limited due to poor dispersion performance of multimode fibers. Present OC systems use dispersion limited single mode fibers. In the single mode fiber light is confined to smaller core (< 10 μm and cladding about 125 μm) which has high refractive index. Single mode fibers allow longer and higher performance links. Present day optical systems operate in low dispersion 1310 nm (S band) window or low attenuation 1550 nm (C band) window with single mode fiber.

| Wavelength (nm) | Loss (dB/km) |
|---|---|
| 850 | 2.0 |
| 1310 | 0.5 |
| 1550 | 0.2 |

**Table 1.1:** Wave lengths of optical carriers their propagation losses in single mode fiber

Standard Single Mode Fiber (SSMF) has zero chromatic dispersion at 1310 nm wavelength. This can be shifted to 1550 nm window through dispersion shifted fibers, which is also the gain window of the Erbium Doped Fiber Amplifiers (EDFA). As can be seen from the Table 1.1 fiber loss at 1550 nm is only 10% of that at 850 nm and half of that at 1310 nm.

Similar to the integrated circuit transistor density improvement, OC system underwent several generations of capacity improvement. The first generation systems operated at a bit rate of 45 Mbits/s with repeater spacing of up to 10 km. The second generation optical systems operated at 1310 nm and used InGaAsP semiconductor lasers. These systems were operating at a bit rate up to 1.7 Gbit/s with repeater spacing up to 50 km. The third generation fiber optic systems operated at 1550 nm and operated commercially at 2.5 Gbit/s with repeater spacing in excess of 100 km. The fourth generation OC systems utilized optical amplification (trough EDFAs) to reduce the need for repeaters and wavelength division multiplexing (WDM) to increase the fiber capacity. Those two developments saw the doubling of system capacity every six months beginning early 90s until 2001 where bit rate of 10 Tb/s was achieved.

The Figure 1.1 depicts a basic WDM optical fiber communication system. Data bits are used to modulate the light carriers at many wavelengths. Then these multiple optical carrier signals are multiplexed on a single optical fiber. The demultiplexer at the receiver split these carriers and route them to the corresponding channels. Optical Amplifiers (OAs) are used to restore attenuated signals for reliable detection. Long haul optical fiber links may span several thousand kilometers and contains tens of OAs placed at regular intervals.

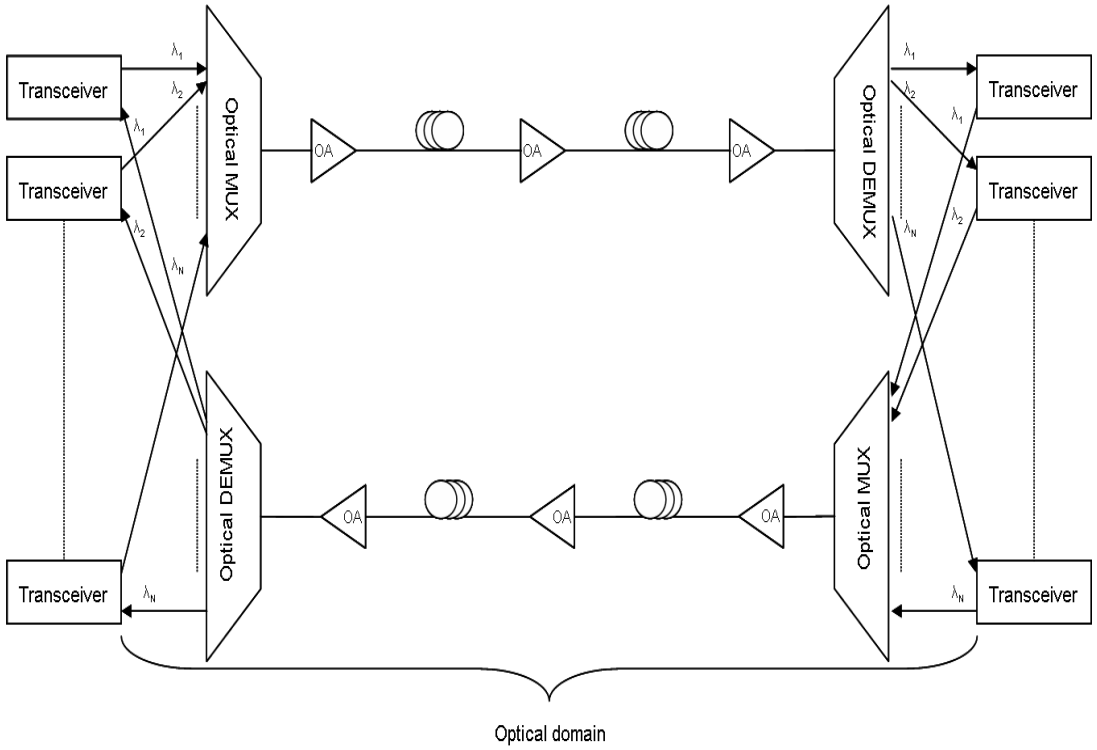



**Figure 1.1:** Basic WDM optical fiber communication system

Synchronous Optical Networking (SONET) is a standard as defined by GR-253-CORE from Telcordia (formally Bellcore). This is a standard for communicating digital information over optical fiber. The Synchronous Digital Hierarchy (SDH) standard developed by International Telecommunication Union (ITU) is SONETs international counterpart. Both SONET and SDH are widely used today, SONET in North America and SDH rest of the world. The basic

SONET signal operates at 51.84 Mbits/s and is designated synchronous transport signal one (STS-1). STS-1 is an electrical signal rate that corresponds to the optical carrier line rate of OC-1; STM-0 is the corresponding SDH line rate. Table 1.2 give defined SONET/SDH levels and corresponding bit rates for optical communication systems. At present most of the internet backbone operates at data rates up to 10 Gbit/s (OC-192/STM-64). Time division multiplexed (TDM) based commercial 40 Gbit/s (OC-768/SDH-256) systems started to deploy for internet backbone upgrades from 2006.

| SONET (North America) | SDH (Europe) | Bit-rate (Mb/s) |
|---|---|---|
| OC-01 | STM-0 | 51.84 |
| OC-03 | STM-1 | 155.52 |
| OC-12 | STM-4 | 622.08 |
| OC-48 | STM-16 | 2488.32 |
| OC-192 | STM-64 | 9953.28 |
| OC-768 | STM-256 | 39813.12 |
| OC-3072 | STM-1024 | 159252.48 |

**Table 1.2:** Optical carrier rates for corresponding SONET/SDH levels

The driving force behind the exponential growth of the telecommunication traffic in the last decade and half is internet applications. During late 1990s and early 2000, optical fiber communication industry was closely associated with the exponentially growing internet related industry (dot-com era). Due to the predictions at that time it was expected that 40 Gbit/s systems would be deployed in early part of this decade. However the global economic slowdown and the following bust of dot-com bubble lead to a slowing demand for increased optical bandwidth and consequently the investments to the OC R&D dried down. But with the global economy picking up again and emerging markets in Asia growing rapidly internet traffic continues to grow exponentially. As the Figure 1.2 shows, within the study horizon the Internet has plenty of spare capacity in the optical domain [2]. But as the graph shows demand line may cross the optical capacity around 2013. Therefore the necessity has arisen to further increase the capacity of optical fiber communication systems.

Intensity Modulation with Direct Detection (IM/DD) has been the method of choice for most commercial optical communication systems due to its low cost and simplicity. IM/DD mainly suffers from poor spectral efficiency (typically $< 0.4$ bit/s/Hz) and high photons per bit number (38 for single polarization). Spectral efficiency is specified in terms of the specified data rate in Gbit/s in 100 GHz band limitation. At high data rates IM/DD is also limited by the polarization mode dispersion (PMD) and low tolerance to the chromatic dispersion (CD). Therefore it is necessary to look for newer modulation methods and detection techniques which has higher spectral efficiency, high sensitivity (photos/bit), higher tolerance to the polarization mode dispersion, and higher tolerance to chromatic dispersion; in order to increase the link capacity to cater to the ever increasing bandwidth demand.

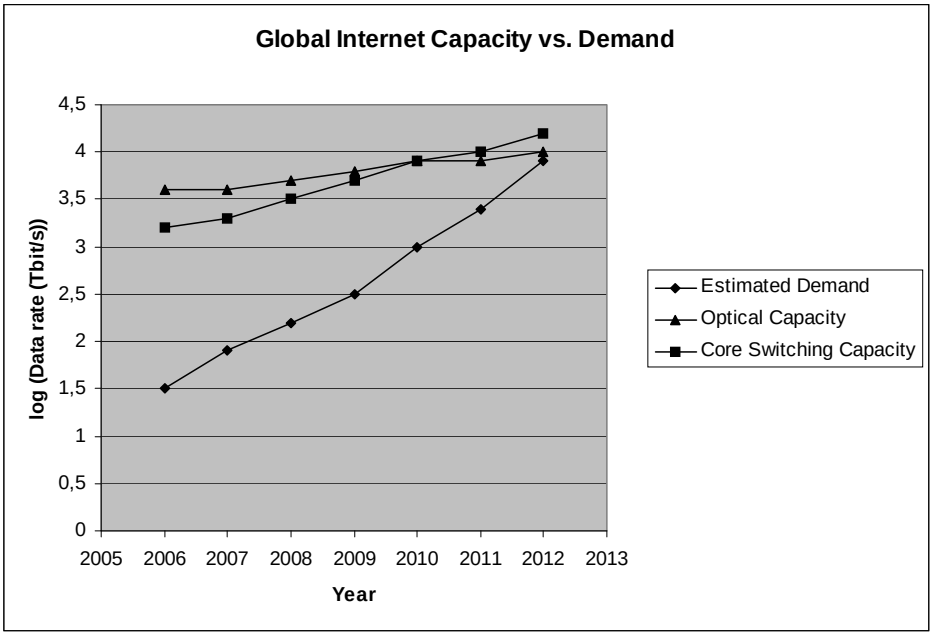



**Figure 1.2:** Global Internet capacity vs. demand 2006-2012

## 1.2 Motivation

Optical Phase Shift Keying (PSK) transmission modulates the phase of optical carrier by transmitted digital data. Optical PSK transmission has higher receiver sensitivity than the On Off Keying (OOK), which is predominantly used in the current commercial optical communication systems. PSK is useful when increasing transmission length while keeping amplifier spacing fixed as Amplified Spontaneous Emission (ASE) is the dominant noise source. Coherent optical detection demands focus because of its higher sensitivity and frequency selectivity. Furthermore coherent receivers allow to perform any required equalization of chromatic and polarization mode dispersion in the electronic domain. Quadrature PSK (QPSK) with polarization multiplex quadruple channel capacity over state of the art intensity modulated systems. This can of course increase the efficiency of the existing fiber plants. Synchronous QPSK transmission combined with return to zero (RZ) coding and polarization division multiplexing will be the face of future long haul and metropolitan area optical networks. When compared to the intensity modulation the line rate is 4 times lower, needed photons per bit number is less than half as high, the tolerance to the chromatic and polarization mode dispersion is several times better, and the tolerance against fiber non linearities is also excellent.

Because electrical signals are proportional to optical fields, photonic processing can transfer 1:1 to the electrical domain. Therefore in this case “optical signal processing is performed electronically”. All linear optical distortions (polarization transformations, polarization mode dispersion, and chromatic dispersion) can be equalized electronically without losses. Synchronous QPSK holds distinct advantages over all other modulation formats, in particular

duobinary, RZ-DPSK, and DQPSK. Maximum Optical Signal to Noise (OSNR) performance is guaranteed by synchronous demodulation. The QPSK synchronous demodulation outperforms the asynchronous or interferometric one by > 2 dB, even if DFB lasers are used. A Phase Locked Loop (PLL) based carrier recovery for synchronous QPSK transmission would fail in combination with Distributed Feedback (DFB) laser because laser line width times loop delay is too large. But the requirement of a PLL can be avoided if the novel feedforward carrier recovery scheme is used [3, 4]. This method relaxes sum line width requirement to 0.001 times symbol rate, which is with in the range of standard DFB laser. However most of the components necessary to realize the synchronous QPSK transmission system are not commercially available. For example synchronous QPSK carrier and data recovery requires high speed A/D conversion and then high speed digital signal processing (DSP). The electronic modules for this purpose are not available and have to be designed. The objective of the European commission funded project "Key components for synchronous optical quadrature phase shift keying transmission" is to realize all key components which are not commercially available for synchronous RZ-QPSK transmission with polarization division multiplex [5]. The signal processing component development includes design of 10.7 Gsymbols/s A/D converter in SiGe technology as well as a compatible carrier recovery, demultiplexing, and electronic polarization control in CMOS technology.

## 1.3 Use of CMOS Technology in High-Speed Optical Communication Systems

Aggressive scaling of MOSFET in past 35 years has brought gate length to 45 nm and is predicted to reach 13 nm by 2013. With each scaling (e.g.: 180 nm $\rightarrow$ 130 nm $\rightarrow$ 90 nm $\rightarrow$ 65 nm $\rightarrow$ 45 nm) the transistor density of integrated circuits (ICs) doubled according to the Moore's law. At the same time the intrinsic speed of a MOSFET increased several fold. The mainstream VLSI technologies such as CMOS and BiCMOS continue to take over the territories thus far claimed by GaAs and InP devices. In addition to nMOS and pMOS transistors for example in 130 nm technology provides

1. a deep n-well, which can be used to reduce substrate noise coupling.
2. a MOS Varactor, which can serve in Voltage Controlled Oscillators (VCOs).
3. six to eight layers of metal, which can form many useful structures such as inductors, capacitors, and transmission lines.

Transistor transit frequency ( $f_T$ ) is an important parameter which should be considered for successful implementation of high speed optical communication ICs. It has been shown that in the 130 nm technology $f_T$ of nMOS device falls to about 60 GHz at slow high-temperature corner, making it possible to use in 10 Gbit/s optical communication ICs [6].

The maximum speed of a differential ring oscillator is a more realistic benchmark for optical communication. It has been shown that three-stage differential ring with resistive load (RC ring oscillator) oscillate at about 18 GHz [6].

Another important parameter is the performance of a divide by two frequency divider. It has been shown that with 130 nm CMOS technology stand alone static frequency divider can operate up to 27 GHz with high source currents [7, 8].

10 Gbit/s physical layer ICs can be found primarily in long-haul applications. But, high power consumption, high cost, and lower level of integration limit their application. The CMOS technology with its low power consumption, negligible static power consumption in digital logic, high level of integration thus avoiding chip-to-chip interfacing has emerged as a viable alternative to SiGe, GaAS, and InP technologies.

Despite scaling down and performance improvement MOSFET has low drive capability ($g_m$) and face large environmental parasities due to the semi-conductive substrate. Furthermore high voltage headroom is necessary to make sure high performance due to non-scaling of the threshold voltage. High $1/f$ noise in CMOS technology lead to high jitter compared to SiGe technology which is a disadvantage in OC systems. Finally, high nonlinearity of the CMOS devices compared to bipolar devices is a distinct disadvantage specially when designing flash A/D converters.

This dissertation discusses designing of 10 Gbit/s interface between a high speed SiGe flash A/D converter and a slow standard cell DSP unit using 130 nm CMOS technology. The interface and the DSP unit are integrated into a single chip to form a mixed-signal chip.

## 1.4 Organisation of Dissertation

This dissertation is organized into five chapters including the introduction. Their focus is as follows:

Chapter two looks into synchronous QPSK transmission in detail. It discusses the basics of synchronous QPSK, its transmission setup, and explains carrier and data recovery algorithm. Furthermore basic introduction to the CMOS circuits that have been developed is given.

Chapter three gives comprehensive design details of the full custom DEMUX interface between the high speed A/D converter output and slow DSP input. This includes design and testing of basic static frequency divider and 1:2 DEMUX modules, design and testing of 10 Gbit/s 5x2 channel 1:8 DEMUX, and design and testing of 10 Gbit/s 5x4 channel 1:8 DEMUX. All the challenges faced in various stages of the design are also discussed. Designs were done in 130 nm CMOS technology.

Chapter four introduces a novel algorithm which calculates expected value of skew of a balanced H-tree clock distribution network in the presence of process uncertainties and non-uniform temperature distribution in the die. Simulation results are also included.

The fifth chapter summarizes the results obtained in this work and proposes a scope for future research.

# Chapter 2

# Optical Synchronous QPSK Transmission Systems

## 2.1 Introduction

Quadrature phase shift keying (QPSK) based multilevel modulation formats guarantee superior performance and dispersion tolerance in newly built and/or upgraded fiber links [3, 4]. Coherent optical polarization diversity receivers allow electronic polarization control, polarization mode dispersion (PMD) compensation, and chromatic dispersion (CD) compensation. This chapter discusses a synchronous QPSK transmission system with polarization multiplex which utilizes phase noise tolerant feedforward carrier and data recovery concept thus avoiding optical phase locked loop (OPLL). A penalty-free electronic polarization controller is also incorporated in the receiver. The chapter is organized as follows:

First, a brief introduction to digital modulation formats and detection techniques is given. Then, the QPSK modulator function is discussed. This is followed by a description of the synchronous QPSK receiver architecture. This section will introduce a feedforward carrier and data recovery scheme and the electronic polarization control scheme. The synchronous QPSK transmission setup with and without polarization multiplex as per European synQPSK project is also introduced. Finally, an introduction is given to CMOS systems in the synchronous QPSK receiver which were designed under synQPSK project. This will be discussed in detail in the next chapter.

## 2.2 Digital Modulation Formats and Detection Techniques for Optical Communication

For a designer of digital optical communication links their exists several modulation formats to choose from. The electrical field associated with the optical signal can be written as [9, 10]

$$E_s(t) = \hat{e}A_s(t)e^{-j(\omega_0 t+\varphi_s(t))}, \qquad \textbf{2.1}$$

where $A_s$ is the amplitude of the optical signal, $\varphi_s$ is the optical phase, $\omega_0$ is the center frequency, and $\hat{e}$ is the polarization vector of the laser source. The parameters $\hat{e}$, $A_s$ and $\varphi_s$ can be modulated by an electrical binary baseband signal

$$a(t) = \sum_{i=-\infty}^{\infty} d_i(t - iT) \qquad \textbf{2.2}$$

$$d_i(t) = c_i s(t),$$

where $s(t)$ is the signal pulse and $c_i$ is the $i^{th}$ transmitted symbol. In the trivial binary coding $c = b$, where $b \in \{0;1\}$.

Depending on which parameter of the laser source modulated, the modulation can be categorized as, Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), Phase Shift Keying (PSK), and Polarization Shift Keying (PolSK) [9, 10].

Amplitude shift keying (ASK) is the cheapest, simplest, and most commonly used digital modulation scheme. An optical ASK signal can be generated by switching on and off laser diode. In the case of ASK format the amplitude $A_s$ is modulated while keeping $\varphi_s$ constant. For binary digital modulation, $A_s$ takes one of the two fixed values during each bit period depending on whether "1" or "0" is being transmitted. In most practical situations $A_s$ is set to zero during the transmission of "0" bits. In this case ASK is called On-Off-Keying (OOK) [9, 11, 12]. OOK is identical with the modulation scheme Intensity Modulation/Direct Detection (IM/DD) which is non-coherent. Figure 2.1 shows the constellation diagram of OOK.

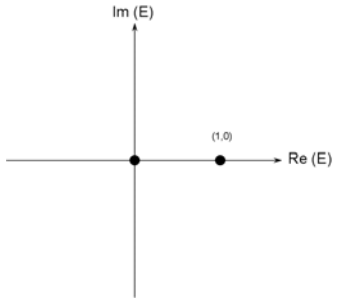



**Figure 2.1:** Constellation Diagram of OOK

In the case of the FSK modulation, information is coded on the optical carrier by shifting the carrier frequency ($\omega$) itself. For a binary digital signal, $\omega$ takes two values $\omega_0 + \Delta\omega$ and $\omega_0 - \Delta\omega$, depending on whether a "1" or "0" bit is transmitted. The shift $\Delta f$ is called the

frequency deviation and is equal to $\Delta\omega/2\pi$. The optical field for FSK format can be written as

$$E_s(t) = A_s e^{-j(\omega_0 t + (\varphi_s \pm \Delta\omega t))}. \quad \textbf{2.3}$$

So FSK can also be viewed as a modulation scheme where the carrier phase increase or decrease linearly over the bit duration. The implementation of FSK requires modulators capable of shifting the frequency of the incident optical signal. Electro-optic materials such as $LiNbO_3$ normally produce a phase shift proportional to the applied voltage. With a triangular voltage pulse (sawtooth-line) applied to a $LiNbO_3$ modulator it is possible to generate FSK signals [9, 10].

In PSK, the phase $\varphi_s$ of the optical signal is modulated while keeping amplitude $A_s$ of the carrier constant. For binary PSK, the phase $\varphi_s$ takes two values, commonly chosen to be $0$ and $\pi$. Figure 2.2 shows time domain signals of ASK, PSK, and FSK modulated optical carrier. PSK is the most sensitive of the three elementary binary modulation schemes. Pure PSK needs coherent detection, as all the information would be lost if the optical signal were detected directly without mixing it with the output of a local oscillator.

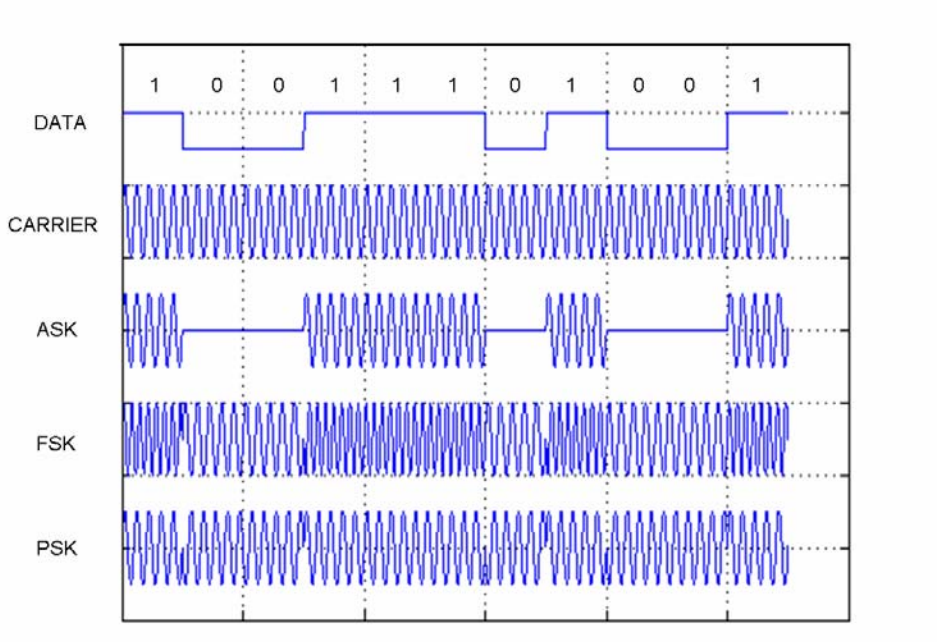



**Figure 2.2:** Time domain signal of various digital modulation formats

The lack of an absolute phase reference in direct detection receivers can be overcome by using the phase of the preceding bit as a reference. This results in differential phase shift keyed (DPSK) formats which carry the information in the optical phase change between bits. In binary DPSK the transmitted bit $c_i$ is generated according to [13]

$$c_i = c_{i-1} \oplus d_i, \quad \textbf{2.4}$$

where $d_i$ is the $i^{th}$ binary input bit to the encoder, and $c_{i-1}$ is the one bit delayed version of $c_i$. The symbol $\oplus$ denotes modulo-2 addition. The encoded symbol is transmitted in a bipolar format with either 0 or $\pi$ phase shift. As it can be seen, differential encoding needs a reference bit to initialize the encoding process. The reference can be set to either logic "1" or "0". For the input data sequence 1 0 1 1 0 0 1 0, corresponding phase shifts are $\pi$ $\pi$ 0 $\pi$ $\pi$ $\pi$ 0 0 where $c_0$ is set to "0".

According to modulo-2 addition rules

$$d_i = c_i \oplus c_{i-1}. \qquad \textbf{2.5}$$

If $c_i$ and $d_i$ are bipolar, the above equation is equivalent to

$$d_i = c_i . c_{i-1}. \qquad \textbf{2.6}$$

Therefore the received symbol can be decoded by using an interferometer having one bit delay deference between its two arms.

DPSK needs 3dB less optical signal-to-noise ratio (OSNR) than OOK in order to achieve the same bit error ratio (BER) when balanced detection is utilized. This can be understood by comparing the constellation diagrams of OOK and DPSK modulation (Figure 2.3). For the same average optical power, the symbol spacing in DPSK is increased by a factor of $\sqrt{2}$ [11].

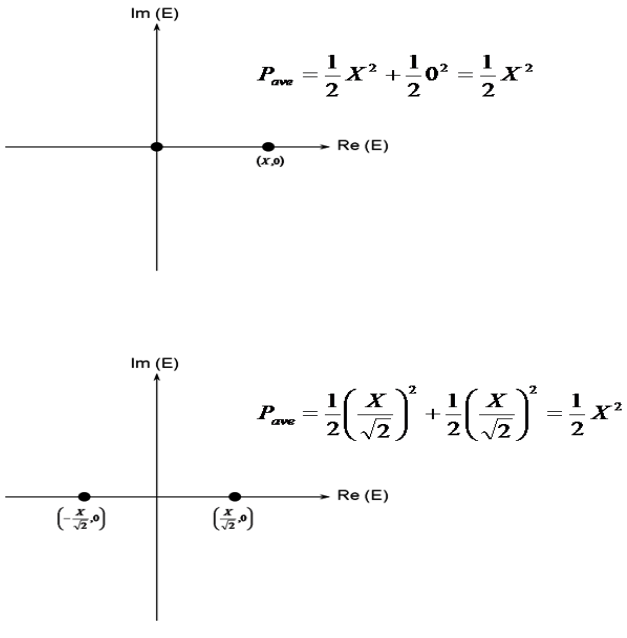



**Figure 2.3:** Comparison of symbol spacing in OOK (top) and DPSK (bottom)

## 2.2.1. Optical Transmission System Performance Parameters

The performance of an optical transmission system can be compared to that of other optical transmission systems in terms of receiver sensitivity, chromatic dispersion, and spectral efficiency.

The receiver sensitivity is usually defined as the minimum average received optical power for which the bit error ratio (BER) of the optical receiver is $10^{-9}$. The receiver sensitivity is generally given in photons/bit. The BER is a function of signal to noise ratio (SNR). The amplified spontaneous emission (ASE), introduced by the optical amplifier, is the dominant noise source in optical receivers. Shot noise and thermal noise also contribute to the SNR and as result to the BER. The received signal eye diagram gives a measure of BER such that a wide open eye diagram means a low BER and vise versa [13, 14, 15].

Chromatic dispersion (CD) is one of the basic characteristic of optical fibers. The refractive index of the optical fiber material depends on the wavelength of the travelling light. In an optical fiber transmission system, when optical carrier is modulated the resultant signal occupies certain spectral bandwidth. While travelling along the fiber, because different parts of the spectrum travel at different speeds due to chromatic dispersion, the signal pulse broadens. This effect is a problem at high bit rates because of the intersymbol interference (ISI) and the resultant distortion of the received signal. The limit on the length of the fiber where reliable transmission is possible imposed by ISI due to the chromatic dispersion depends on the chromatic dispersion index factor $\gamma$ given as [16, 17]

$$\gamma = \frac{R^2 LD \lambda^2}{\pi c}, \qquad \textbf{2.7}$$

where $R$ is the data rate of the system, and $L$ is the transmission length, and $D$ is the chromatic dispersion coefficient. $\lambda$ and $c$ are wavelength and the velocity of light in a vacuum. Standard single mode fiber (SSMF) has a dispersion coefficient from 16 to 19 ps/nm.km at the low loss window of 1550 nm.

The throughput of the dense wavelength division multiplexing (DWDM) systems can be increased by either using wider optical bandwidth, increasing the spectral efficiency (SE) or a combination of both. Utilizing higher bandwidth requires additional optical components like amplifiers. So the better option would be to increase the spectral efficiency. This can be achieved by using advanced modulation formats with higher spectral efficiency. The spectral efficiency limit SE in a DWDM system is defined as [18]

$$SE = \frac{C}{\Delta f}, \qquad \textbf{2.8}$$

where $\Delta f$ is the channel spacing and $C$ is the capacity per channel. Advanced modulation formats such as QPSK have higher spectral efficiency. As, will be discussed later in this chapter, QPSK with polarization multiplex quadruples channel capacity over binary PSK (BPSK).

## 2.2.2. Receiver Concepts in Optical Fiber Communication

This section discusses some prominent receiver concepts for ASK and PSK modulated optical signals.

The most commonly used optical receiver is a direct detection receiver, which is a non-coherent type receiver. A direct detection receiver consists of an optical pre-amp, optical bandpass filter, a photodetector to convert the optical signal to an electrical signal followed by an electrical amplifier and a lowpass filter as shown in Figure 2.4 [13, 19]. This setup is used as an ASK receiver. When the modulation format is DPSK the receiver in Figure 2.4 should be modified such that there is a Mach-Zehnder delay interferometer (MZDI), between optical bandpass filter and photodetection, with single bit delay between two arms. Instead of a single photodiode there are two differential photodiodes as shown in the Figure 2.5 which detect optical signals of the 3dB coupler output arms [11, 13, 20, 21].

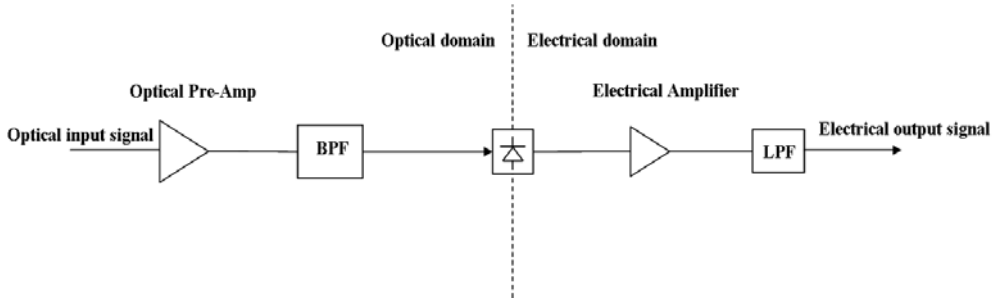



**Figure 2.4:** Optical direct detection receiver block diagram

The transfer matrix of the output coupler is $\frac{1}{\sqrt{2}}\begin{bmatrix} 1 & -j \\ -j & 1 \end{bmatrix}$. If the input optical field to the MZDI is $E(t)$, the output photocurrent $I(t)$ of the balanced photodetector is proportional to $\mathrm{Re}\left(E^*(t)E(t-T)\right)$ [13].

Direct detection has so far been the choice of selection for optical receivers due to its low cost and simplicity. But, the direct detection receiver suffers from low sensitivity and the received electrical signal can not be equalized against chromatic dispersion or polarization mode dispersion. The coherent optical receiver could overcome above problems. Figure 2.6 shows the general setup of a coherent optical receiver [9, 10, 12, 13, 22, 23].

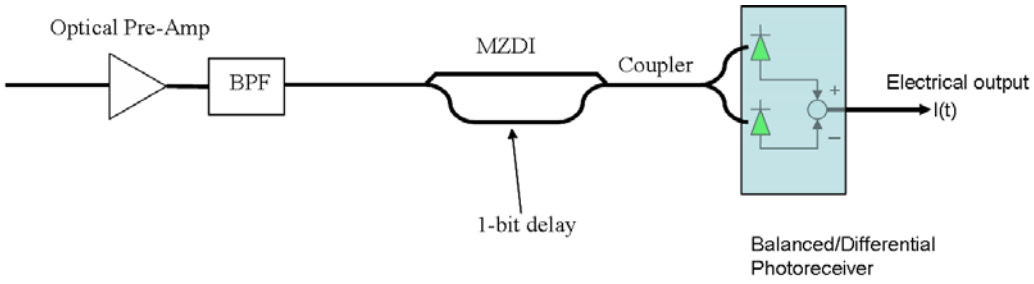



**Figure 2.5:** DPSK direct detection receiver

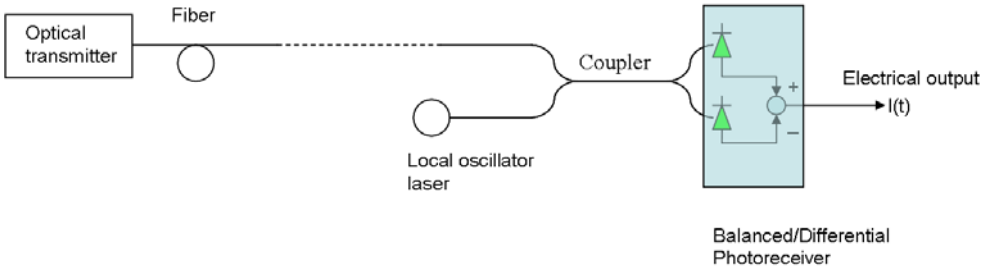



**Figure 2.6:** General setup of a coherent optical receiver

The unmodulated signal of the local oscillator (LO) laser is added to the received signal before photodetection. The polarization and the optical frequency of the LO laser and the received signal must be identical or almost identical. The signal and the LO laser must be longitudinally single-moded. The LO must be tunable in its frequency in order to match that of signal. If the signal field $\underline{E}_S(t) = \underline{E}_{S,0} e^{j\omega_S t}$ and the local oscillator field $\underline{E}_{LO}(t) = j\underline{E}_{LO,0} e^{j\omega_{LO} t}$ and the coupler transfer matrix is $\frac{1}{\sqrt{2}}\begin{bmatrix} 1 & -j \\ -j & 1 \end{bmatrix}$ the output signal $I(t)$ when polarizations are identical can be given as

$$I(t) = 2R\sqrt{P_S P_{LO}}\cos(\omega_{IF} t + \varphi_{IF}), \qquad \textbf{2.9}$$

where $R$ is photodiode responsivity, intermediate angular frequency $\omega_{IF} = \omega_S - \omega_{LO}$, $\varphi_{IF} = \arg\left(\underline{E}_{LO,0}{}^{+} \cdot \underline{E}_{S,0}\right)$, $P_S = 1/2\left|\underline{E}_s\right|^2$, and $P_{LO} = 1/2\left|\underline{E}_{LO}\right|^2$ [13]. The local oscillator is strong $\left(\left|\underline{E}_{LO}\right| >> \left|\underline{E}_S\right|\right)$ and unmodulated $\left(\underline{E}_{LO} = const.\right)$.

In a homodyne receiver $\omega_{IF} = 0$ holds. The maximum photocurrent difference is achieved for $\varphi_{IF} \in \{0, \pi\}$. This requires an optical phase locked loop (OPLL) that acts as a local

oscillator. Realizing an OPLL in practice is extremely difficult due to stringent laser linewidth$\times$loop delay requirements. When $\omega_{IF} \neq 0$, the receiver is called a heterodyne receiver. In this case it is useful choose $\pi/\omega_{IF}$ to be an integer multiple of the symbol duration $T$.

The homodyne receiver allows the processing to be done at the baseband frequency, which is a huge advantage at high bit rates. The advantage of the heterodyne receiver is that the carrier recovery is a feedforward process where an OPLL with stringent laser linewidth requirements is not necessary [3, 4, 10, 13, 17].

In order to retain advantages of both homodyne and heterodyne systems an intradyne receiver can be used. In an intradyne receiver the intermediate frequency ($IF$) is non-zero but a lot smaller than the bandwidth of the baseband signal ($IF$ is lot smaller than the symbol clock frequency) [4, 22, 23]. A non-zero $IF$ can also represented as a time-varying phase shift $\varphi_{IF}(t)$ between signal and local oscillator lasers.

There are two ways of demodulating the received electrical signal (after photoditection), namely synchronous demodulation and asynchronous demodulation. In order for the synchronous demodulation to occur the carrier should be available at the receiver. In a homodyne receiver the local oscillator generates the carrier. In a heterodyne or in an intradyne receiver the local oscillator moves the received signal to a lower frequency band. An electrical carrier signal must be generated from this signal in order to perform demodulation. However, the laser linewidth and system requirements of the synchronous demodulators are complex. The asynchronous demodulation, which does not need to generate a carrier for demodulation, is easy to implement and cheap. The DPSK heterodyne receiver is an example of an asynchronous demodulator (Figure 2.7) [11, 13, 24, 25].

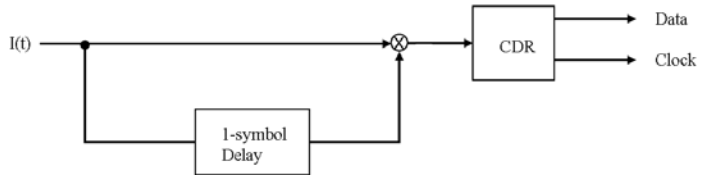



**Figure 2.7:** Asynchronous DPSK heterodyne receiver

Table 2.1 compares the sensitivity of different modulation techniques and receiver concepts [11, 13, 26]. It can be seen that the synchronous QPSK receiver concept maintains a high sensitivity (18 photons/bit) while maintaining twice as much spectral efficiency as any other modulation format. Furthermore it is possible to equalize chromatic dispersion and polarization mode dispersion in the electronic domain. The rest of this chapter discusses the implementation of synchronous QPSK in a polarization multiplex transmission system.

| | Asynchronous Demodulation | | Synchronous Demodulation | |
|---|---|---|---|---|
| | ASK | DPSK | PSK | QPSK |
| Direct detection with optical Pre-Amp, 2(1) polarizations | 40.7(38) | 21.9(20) | | |
| Heterodyne/phase diversity detection with or without optical Pre-Amp | 38 | 20 | 18 | 18 |
| Homodyne detection with(without) optical Pre-Amp | | | 18(9) | 18(18) |

**Table 2.1:** Mean required number of photons/bit for BER of $10^{-9}$ for various modulation and detection techniques

## 2.3 An Introduction to the Optical Synchronous QPSK (synQPSK) Transmission System

This section discusses the components and their functionality of a synchronous QPSK with polarization multiplex transmission system. The discussion begins with the QPSK transmitter which includes the differential encoder and the QPSK modulator. Then the receiver side of the system which includes opto-electronic 90° hybrid, A/D converters, carrier & data recovery, and electronic polarization control units is discussed. The feedforward carrier-and-data recovery algorithm and electronic polarization control algorithm are also discussed. Furthermore an introduction to the architecture of CMOS digital signal processing units is given. Finally the architecture DSPU input interface is also briefly introduced.

### 2.3.1. QPSK Transmitter

The constellation diagram of the QPSK modulation scheme is given in the Figure 2.8. It has four possible phase angles $\pm\pi/4$, and $\pm 3\pi/4$. A data quadrant number $n_d$ is generated which represents two bipolar data bits $d_1, d_2$ (Table 2.2) [3, 27]. The data quadrant number is differentially encoded to form an encoded quadrant number $n_c$ with

$$n_c(i) = (n_d(i) + n_c(i-1)) \bmod 4. \qquad \textbf{2.10}$$

This number defines the quadrant of the transmitted complex signal $\underline{c} = \mathrm{Re}\,\underline{c} + j\,\mathrm{Im}\,\underline{c} = \pm 1 \pm j$ .

Figure 2.9 shows the QPSK transmitter setup [27- 43]. The unipolar electrical signals $d_{u1}(t)$ and $d_{u2}(t)$ represent differentially encoded bit streams $b_1(t)$ and $b_2(t)$, respectively. The Mach-Zehnder modulators (MZM) are biased in such a way that the unipolar electrical drive signals $d_{u1}(t)$ and $d_{u2}(t)$ ( 0 for bit "0", and $V_\pi$ for bit "1") , $d_1(t)$ and $d_2(t)$ become -1 for bit "0" and +1 for bit "1". $V_\pi$ is the voltage that causes a phase difference of $\pi$ in the arms of the MZM.

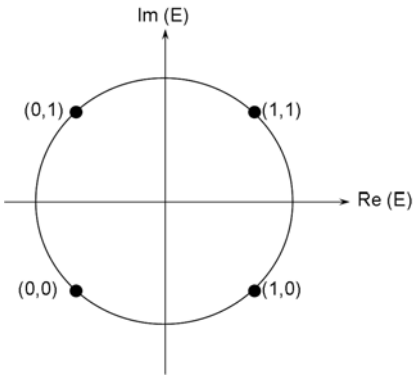



**Figure 2.8:** Constellation diagram of QPSK modulation scheme

| $d_1, \mathrm{Re}\,\underline{c}, o_1$ | $d_2, \mathrm{Im}\,\underline{c}, o_2$ | $n_d, n_c, n_o$ |
|---|---|---|
| 1 | 1 | 0 |
| -1 | 1 | 1 |
| -1 | -1 | 2 |
| 1 | -1 | 3 |

**Table 2.2:** Mapping between bipolar bits and quadrant number

Light from a continuous wave (CW) laser $\underline{E}_{CW}(t) = \sqrt{4P_s}\,e^{j[\omega_s t + \varphi_s]}$ is split by a Y-junction into upper and lower parts $\underline{E}_u(t)$ and $\underline{E}_l(t)$. $2P_s$ is the power of the CW laser. $\omega_s/2\pi$ is the frequency of the optical carrier. $\underline{E}_u(t)$ in the upper arm is modulated in the MZM by binary electrical signal $d_{u1}(t)$ and $\underline{E}_l(t)$ in the lower arm is modulated in the MZM by binary electrical signal $d_{u2}(t)$. In the lower path there is a delay equivalent to $\pi/2$ phase shift. Therefore the modulated signals in the upper and lower arms can be written as

$$\underline{E}_u^{\mathrm{mod}}(t) = d_1(t)\sqrt{2P_s}\,e^{j(\omega_s t+\varphi_s)},$$
$$\underline{E}_l^{\mathrm{mod}}(t) = jd_2(t)\sqrt{2P_s}\,e^{j(\omega_s t+\varphi_s)}. \qquad \textbf{2.11}$$

At the output Y-junction $\underline{E}_u^{\mathrm{mod}}(t)$ and $\underline{E}_l^{\mathrm{mod}}(t)$ are combined to give the output signal $\underline{E}_s(t)$

$$\underline{E}_s(t) = \left[d_1(t) + jd_2(t)\right]\sqrt{P_s}\,e^{j(\omega_s t+\varphi_s)} = \underline{c}(t)\sqrt{P_s}\,e^{j(\omega_s t+\varphi_s)} \qquad \textbf{2.12}$$
$$\underline{c}(kT) = \pm 1 \pm j \;,\; k = 0,\pm 1,\pm 2,\ldots.$$

$\underline{E}_s(t)$ is the QPSK signal, $T$ is the symbol duration, and $P_s$ is the transmitted signal power.

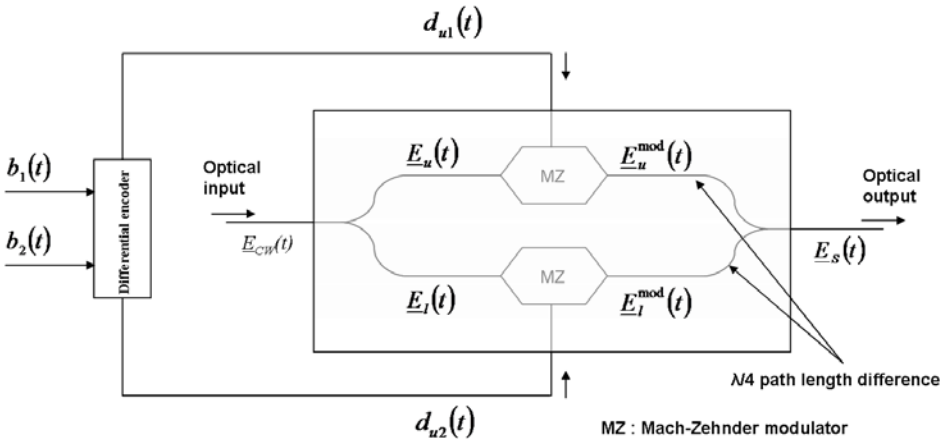



**Figure 2.9:** QPSK transmitter setup

## 2.3.2. Coherent QPSK Receiver

Figure 2.10 shows optical 90° hybrid followed by differential/balanced photodiode pair [3, 27, 43]. It consists of four 1:1 directional couplers with the transfer matrix $\frac{1}{\sqrt{2}}\begin{pmatrix} 1 & -j \\ -j & 1 \end{pmatrix}$ and a phase shifter. The balanced photodiode pair which follows the optical 90° hybrid convert the optical signal to an electrical signal.

The local oscillator (LO) laser signal is $\underline{E}_{LO}(t) = \sqrt{2P_{LO}}\,e^{j[\omega_{LO}t+\varphi_{LO}]}$ with the power $P_{LO}$ and the optical frequency $\omega_{LO}/2\pi$. The received signal is $\underline{E}_R(t) = \underline{c}(t)\sqrt{P_R}\,e^{j(\omega_s t+\varphi_s)}$ where $P_R < P_s$ because of the attenuation. If it is assumed that the effect of the phase noise and the

nonlinear effects are negligible $\omega_s$ and $\varphi_s$ remain unchanged. The LO signal and the received signal are split by two dirctional couplers at the input of the 90° hybrid. The resulting signals are

$$\underline{E}_{R,1}(t) = -\underline{E}_{R,2}(t) = \underline{c}(t)\sqrt{P_R/2}e^{j(\omega_S t+\varphi_S)},$$
$$\underline{E}_{LO,1}(t) = j\underline{E}_{LO,2}(t) = \sqrt{P_{LO}}e^{j(\omega_{LO}t+\varphi_{LO})}. \qquad \textbf{2.13}$$

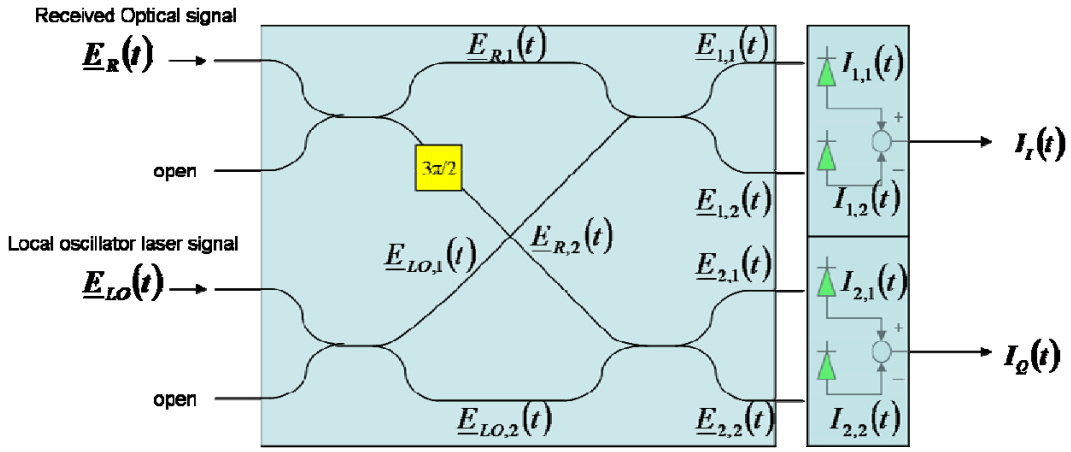



**Figure 2.10:** Optical 90° hybrid followed by differential/balanced photodiode pair

These signals are pairwise combined in another two cross couplers and then fed into two differential photodiode pair. The input signals to the photodiodes are given by

$$\underline{E}_{d,1}(t) = (1/\sqrt{2})(\underline{E}_{R,d}(t) - j\underline{E}_{LO,d}(t)),$$
$$\underline{E}_{d,2}(t) = (1/\sqrt{2})(-j\underline{E}_{R,d}(t) + \underline{E}_{LO,d}(t)),$$
$$d \in \{1,2\}. \qquad \textbf{2.14}$$

Assuming photodiode responsivity $R$ the output currents of the balanced photodiode pairs can be given as

$$I_{d,1}(t) = \frac{R}{2}\left|\underline{E}_{d,1}\right|^2 = \frac{R}{4}\left(\left|\underline{E}_{R,d}\right|^2 + 2\,\mathrm{Re}\left\{j\underline{E}^+_{LO,d}\,\underline{E}_{R,d}\right\} + \left|\underline{E}_{LO,d}\right|^2\right)$$
$$I_{d,2}(t) = \frac{R}{2}\left|\underline{E}_{d,2}\right|^2 = \frac{R}{4}\left(\left|\underline{E}_{R,d}\right|^2 - 2\,\mathrm{Re}\left\{j\underline{E}^+_{LO,d}\,\underline{E}_{R,d}\right\} + \left|\underline{E}_{LO,d}\right|^2\right)$$
$$d \in \{1,2\}, \qquad \textbf{2.15}$$

$$
\begin{aligned}
I_I(t) &= I_{1,1}(t) - I_{1,2}(t) = R\,\mathrm{Re}\left\{ j\underline{E}^{+}_{LO,1}\underline{E}_{R,1} \right\} \\
&= -\frac{R}{2}\,\mathrm{Im}\left\{ \underline{E}^{+}_{LO}\underline{E}_{R} \right\} \\
I_Q(t) &= I_{2,1}(t) - I_{2,2}(t) = R\,\mathrm{Re}\left\{ j\underline{E}^{+}_{LO,2}\underline{E}_{R,2} \right\} \\
&= \frac{R}{2}\,\mathrm{Re}\left\{ \underline{E}^{+}_{LO}\underline{E}_{R} \right\}.
\end{aligned}
\qquad \textbf{2.16}
$$

When $\omega_{IF} = \omega_S - \omega_{LO}$ and $\varphi_{IF} = \varphi_S - \varphi_{LO}$ the received signal in complex form can be given as

$$
\underline{X}(t) = \frac{\sqrt{2}}{R\sqrt{P_R P_{LO}}}\left( I_Q(t) - jI_I(t) \right) = \underline{c}(t)e^{j(\omega_{IF}t+\varphi_{IF})}. \qquad \textbf{2.17}
$$

$\underline{X}$ contains the transmitted data according to the constellation diagram Figure 2.8. The constellation diagram of the received $\underline{c}(t)$ would look like in the Figure 2.11 due to noise added in the transmission [29-31].

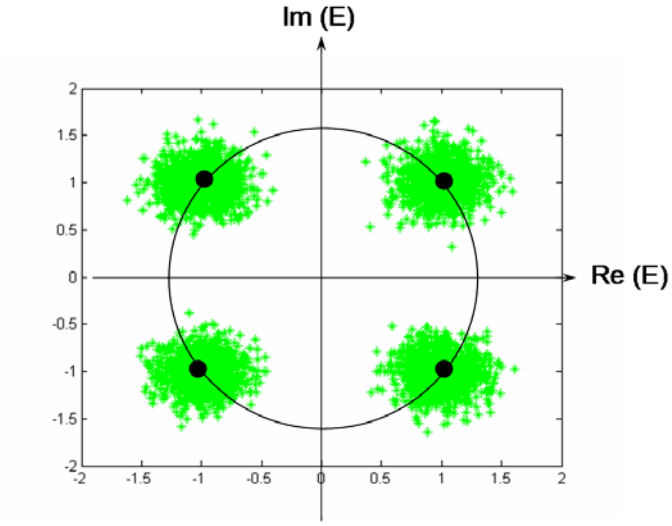



**Figure 2.11:** QPSK constellation diagram at the receiver (black dots are transmission side constellation diagram)

Due to the intermediate frequency $\omega_{IF}/2\pi$ the constellation diagram is rotating. Therefore an IF carrier recovery is necessary before the transmitted data can be recovered.

## 2.3.3. Carrier and Data Recovery Algorithm

Figure 2.12 shows the block diagram of the synchronous QPSK transmission system with carrier and data recovery units [3, 27, 36, 38, 39]. The $\mathrm{Re}\,\underline{X}$ (I) and $\mathrm{Im}\,\underline{X}$ (Q) components are sampled and digitized by 5 bit SiGe A/D converters custom made for the project. Then the resulting signals (10 Gbit/s) are transmitted to the CMOS version A DSPU. Inside the DSPU the signals are 1:M demultiplexed to a low symbol rate where complex digital functions in standard cell CMOS logic can be implemented.

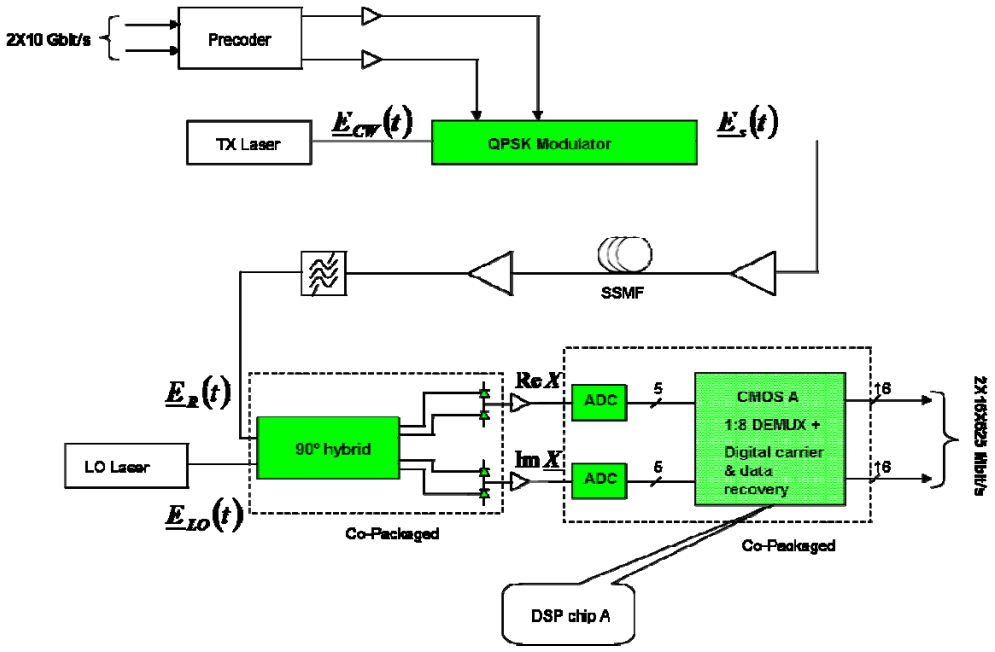



**Figure 2.12:** Synchronous QPSK transmission system block diagram

The M data streams are processed in M modules [3, 27]. These modules should intercommunicate during the processing. The $i^{th}$ complex sample $\underline{X}(i)$ of the digitized IF signal $\underline{X}$ enters the $k^{th}$ module (Figure 2.13), where $k = i \bmod M$. The other input signals to the $k^{th}$ signal processing module are provided by adjacent signal processing modules.

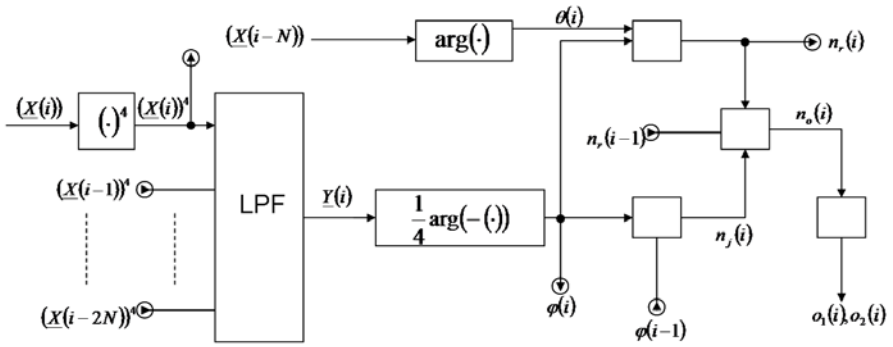


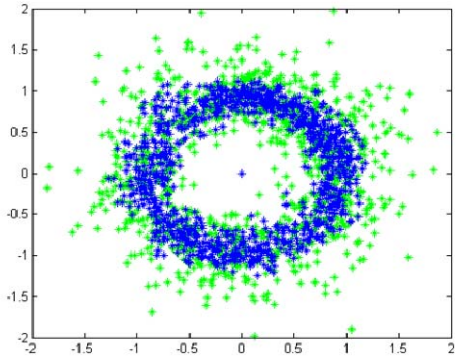

**Figure 2.13:** Block diagram of the $k^{th}$ signal processing unit after demultiplexer. The circled arrows represent signals which communicate with other modules

First $\underline{X}(i)$ is raised to the 4th power. This operation eliminate the modulation (because $\underline{c}^4 = -4$). The resulting frequency-quadrupled carrier $\underline{X}^4 \propto -e^{j4\varphi}$ must be filtered for signal-to-noise (SNR) improvement. Because IF is at or near zero low pass filtering (LPF) of $\underline{X}^4$ is necessary for noise suppression. The phase angles of the quantities $(\underline{X}(i-mM))^4$ with $m$ = 0,1,2,..., which are available in the $k$th module, may differ a lot. Therefore it may not be appropriate to base the LP filtering only on them. A good filter may take the weighted sum,

$$Y(i) = \sum_{m=0}^{2N} w_m (\underline{X}(i-m))^4 \qquad \textbf{2.18}$$

of $2N+1$ most recent samples of the frequency quadrupled carrier where $\sum_{m=0}^{2N} w_m = 1$, most of which come from adjacent modules. The filter is designed symmetric, where the centre sample is the sample to be decoded and the weight distribution is symmetric. Then the group delay of the filter equals $N$ symbols. The optimum weight distribution which gives best output should be selected after through investigation which is beyond the scope of this thesis. The input and output phasor diagrams of a LPF with $N$=2 and the weight distribution as given is shown in the Figure 2.14 which clearly shows the reduction of noise.

The summation requires more hardware than the equivalent recursive algorithm, $\underline{Y}(i) = \underline{Y}(i-1) + \underline{X}(i) - \underline{X}(i-2N)$. However, the recursive relation would need to be clocked at the symbol rate, which is practically impossible.



| $m$ | 0 | 1 | 2 | 3 | 4 |
|---|---|---|---|---|---|
| $w_m$ | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 |

**Figure 2.14:** Input and output phasor diagrams of the LPF with given weight distribution

The LPF also alters the phase angle. $\underline{Y} \propto -e^{j4\varphi}$ holds, where $4\varphi(i)$ would ideally be equal to $4\varphi'(i-N)$. As the next step, the frequency of $\underline{Y}$ is divided by a factor of 4 in order to recover the carrier phase. The best choice is a 2-D lookup table which calculates $\varphi(i) = (1/4)\arg(-\underline{Y}(i))$. The phase angle $\theta(i) = \arg \underline{X}(i-N)$ is also obtained using a similar lookup table, with a delay equal to that of the LPF. For demodulation, an integer $n_r(i)$ which fulfils $n_r(i)\pi/2 \le \theta(i) - \varphi(i) < (n_r(i)+1)\pi/2$ is determined. It may be called a received quadrant number because $\underline{c}(i-N) = (1+j)e^{jn_r(i)\frac{\pi}{2}}$ holds for $|\varphi(i) - \varphi'(i-N)| < \pi/4$. Consider the following argument, $\underline{c}^4 = (\pm 1 \pm j)^4 = -4$, $1/4\arg(-4) = -\pi/4 = \varphi(i)$. Therefore even though $\arg(\underline{c})$ can take values $\pi/4, 3\pi/4, 5\pi/4, 7\pi/4$, $\varphi(i)$ only take the value $-\pi/4$. Therefore there is a four-fold ambiguity in the calculation of $\varphi(i)$, and $n_r(i)$ does not contain all the information. Selecting $\varphi(i)$ as close as possible to $\varphi(i-1)$ could solve the problem but it is practically impossible because the correct quadrant number can not be selected within one symbol duration. The way out of this problem is as follows. Let $|\varphi(i)| \le \pi/4$ be always chosen. The $k^{th}$ module must detect whether $\varphi$ has jumped by an integer multiple of $\pi/2$. $n_j(i)$ is the quadrant jump number which fulfills $|\varphi(i) - \varphi(i-1) - n_j\,\pi/2| < \pi/4$. Angle functions are periodic. Therefore all the operations are valid modulo-4.

Figure 2.15 shows quadrant phase jumps at $i = i_0$ , $i = i_0 + 3$ and their detection. A $n_j(i_0), n_j(i_0+3) \neq 0$ indicates that all $n_r(p)$ with $p \ge i_0$ and $p \ge i_o + 3$ carry unwanted offsets $-n_j(i_0)$ and $-n_j(i_0+3)$. It is not possible to correct all $n_r(p)$ accordingly because this could have done at symbol rate. As discussed earlier data quadrant number $(n_c)$ is differentially encoded. The output quadrant number can be calculated by

$$n_o(i) = (n_r(i) - n_r(i-1) + n_j(i)) \bmod 4 = n_d(i-N). \qquad \textbf{2.19}$$

$n_o(i)$ yields the output data bits $o_1(i)$ and $o_2(i)$ (Table 2.2). These are equal to delayed data bits $d_1(i-N)$, $d_2(i-N)$. Figure 2.16 shows the successful correction of the phase jumps.

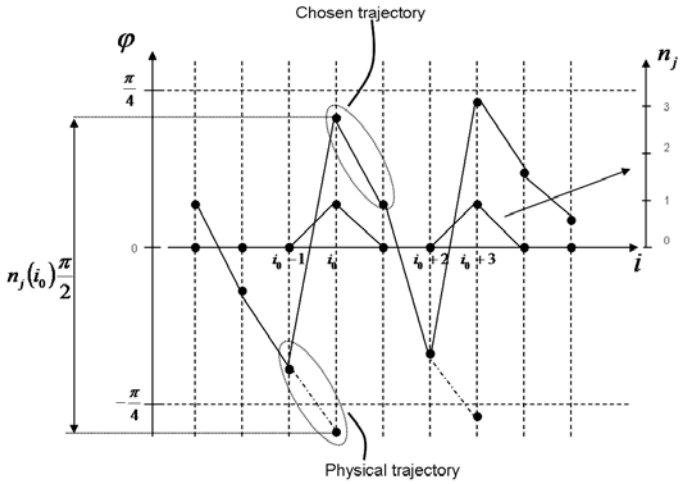



**Figure 2.15:** Quadrant phase jumps and its detection

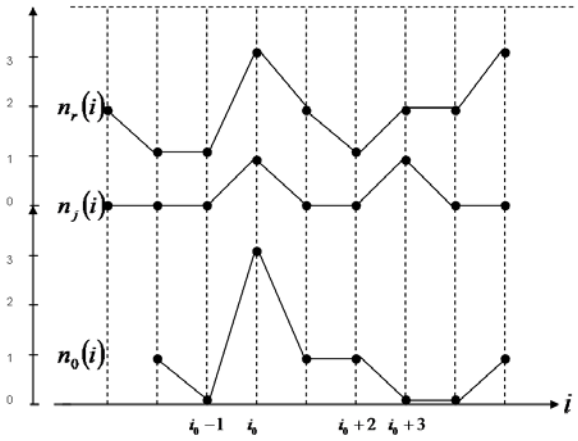



**Figure 2.16:** Successful correction of the quadrant phase jumps

## 2.3.4. Electronic Polarization Control

Figure 2.17 shows synchronous QPSK with polarization multiplex transmission system [3, 27, 40, 43]. The transmitter laser signal is split, QPSK modulated in two QPSK modulators and recombined with two $(p=1,2)$ orthogonal polarizations in a polarization beam splitter (PBS). The transmitted field $\mathbf{E}_{TX}$ is proportional to the vector $\mathbf{c}=\left[\underline{c}_1 \quad \underline{c}_2\right]^T$. The received field

$$\mathbf{E}_{RX} = \mathbf{J}\mathbf{E}_{TX}, \qquad \textbf{2.20}$$

where **J** is the fiber Jones matrix [3, 27]. The receiver consist of a 45°-polarized local oscillator (LO) laser. The received and LO lasers are each split into orthogonal polarizations, and the fields $\underline{E}_{RX,p}, \underline{E}_{LO,p}$ of each polarization p are detected in optoelectronic 90° hybrids. The in-phase and quadrature signals form together a received IF signal vector

$$\mathbf{R} = \left[\underline{R}_1 \quad \underline{R}_2\right]^T = \mathbf{J}\cdot\mathbf{c}\cdot e^{j\varphi''}, \qquad \textbf{2.21}$$

where $\varphi''$ is the phase difference between the signal and the LO lasers.

The received samples are multiplied by a complex Jones matrix **M** to form polarization separated IF vector sample

$$\mathbf{X}(i) = \left[\underline{X}_1(i) \quad \underline{X}_2(i)\right]^T = \mathbf{M}\mathbf{R}(i). \qquad \textbf{2.22}$$

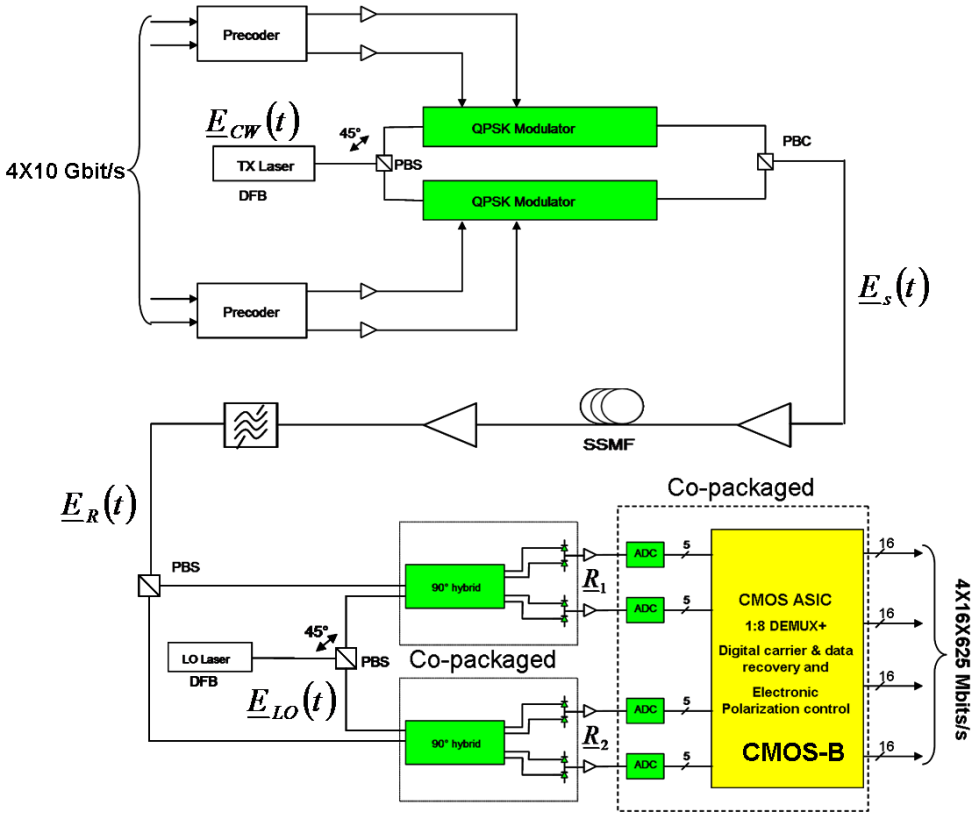



**Figure 2.17:** Polarization multiplex synchronous QPSK transmission system

Ideally **MJ** is proportional to **I** and it holds $\mathbf{X} = \mathbf{c}\cdot e^{j\varphi'}$. Angle $\varphi' - \varphi''$ is the phase shift introduced by the matrix product **MJ**. The main issue here is how to estimate coefficients of

the polarization control matrix **M** and update them to track the changes of **J.** If a perfect estimate $\langle \mathbf{Q} \rangle$ of the matrix product **MJ** is available, polarization can be controlled electronically and penalty-free by applying the iterative formula $\mathbf{M} := \langle \mathbf{Q} \rangle^{-1} \mathbf{M}$ (zero-forcing algorithm). For $\langle \mathbf{Q} \rangle \to \mathbf{I}$, where **I** is the unity matrix, the inverse can be approximated by

$$\langle \mathbf{Q} \rangle^{-1} = \left( \mathbf{I} - \left( \mathbf{I} - \langle \mathbf{Q} \rangle \right) \right)^{-1} \approx \mathbf{I} + \left( \mathbf{I} - \langle \mathbf{Q} \rangle \right). \qquad \textbf{2.23}$$

$$\mathbf{M} := \left( \mathbf{I} + \left( \mathbf{I} - \langle \mathbf{Q} \rangle \right) \right) \mathbf{M}. \qquad \textbf{2.24}$$

An unknown matrix **N** can be estimated by correlating an input vector **A** having independent zero-mean elements with an output vector **NA** (Figure 2.18).

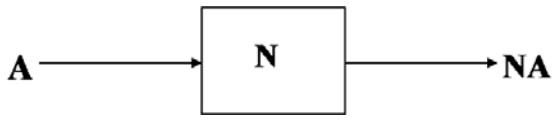



**Figure 2.18:** Estimation model of the matrix **Q**

$$\langle \mathbf{N} \rangle = \left\langle (\mathbf{NA}) \mathbf{A}^{+} \right\rangle. \qquad \textbf{2.25}$$

The matrix **Q** is obtained as follows. The polarization-separated IF vector is multiplied by $e^{-j\varphi}$ to get rid of phase noise. The result contains phase jumps and is differentially coded. Therefore it must be correlated not with the recovered data itself but with the received data vector $\mathbf{r} = [\underline{r}_1 \quad \underline{r}_2]^T$. Therefore **Q**(i) is given by

$$\mathbf{Q}(i) = (1/2) \cdot \mathbf{X}(i - N) \cdot e^{-j\varphi(i)} \cdot \mathbf{r}(i)^{+}. \qquad \textbf{2.26}$$

The factor 1/2 assures that $|\det(\mathbf{MJ})| \to 1$. Better than waiting for a perfect estimate $\langle \mathbf{Q} \rangle$ is it to choose a low control gain $g$<<1 and to update **M** immediately as $\mathbf{M} := (\mathbf{1} + g(\mathbf{1} - \mathbf{Q}))\mathbf{M}$.

To allow real-time operation, the $\mathbf{Q}(i)$ may be accumulated before an updating step of **M** is undertaken. Since the symbol duration is so short it should be sufficient in most applications to base the updating of **M** on matrices **Q** obtained in only one of M signal processing modules, which also reduces silicon area. Figure 2.19 [3, 27] shows the functional block diagram of the polarization control unit which is a part of the CMOS-B DSPU. Imbalance of the 90° hybrid and similar effects can be corrected if **M** is replaced by a complex 2x4 matrix with the 4 real-valued input signals $\mathrm{Re}\,\underline{R}_1, \mathrm{Im}\,\underline{R}_1, \mathrm{Re}\,\underline{R}_2, \mathrm{Im}\,\underline{R}_2$.

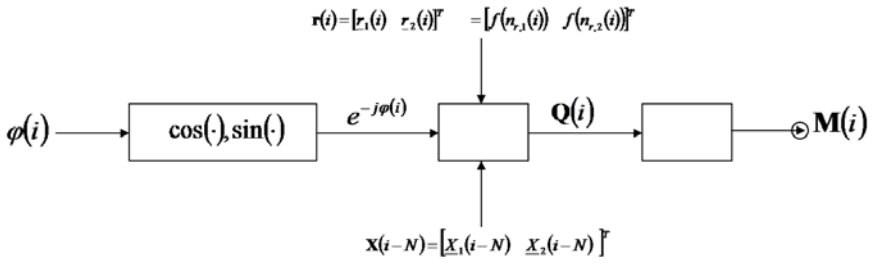



**Figure 2.19:** Polarization control matrix update block diagram

## 2.4 CMOS DSP Unit Architecture

Figure 2.20 shows the internal architecture of the CMOS chip A and Figure 2.21 shows the internal architecture of the CMOS chip B. The input stage of each DSPU is full custom 10 Gbit/s 1:8 DEMUX which interface high speed ADC output and low speed standard cell logic. The CMOS-A die has 10 parallel 1:8 DEMUX blocks correspond to 5-bit inphase and quadrature signal components. The CMOS-B die has 20 parallel 1:8 DEMUX blocks due to two orthogonal polarization components. The input of the interface is source-coupled FET logic (SCFL) while the output is CMOS logic. Therefore a SCFL-CMOS logic converter is also included in the interface. All the DEMUXes are clocked using a single input clock signal and a series of clock divider and buffer circuits. In the next chapter the designs of these interfaces will be discussed in detail.

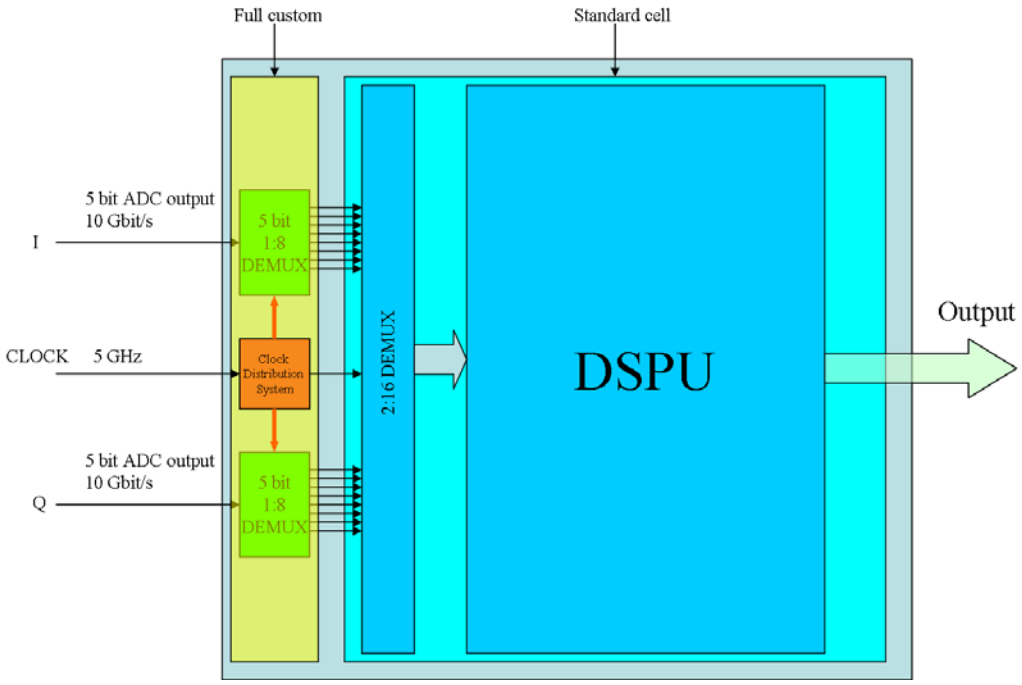



**Figure 2.20:** Architecture of the CMOS chip A

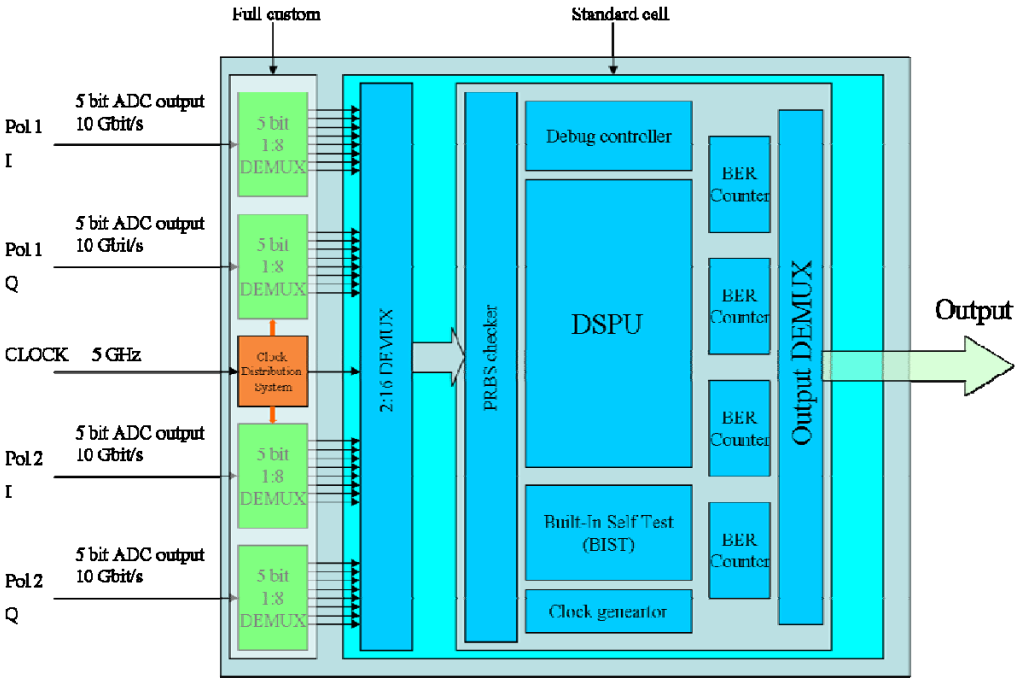



**Figure 2.21:** Architecture of the CMOS chip B

# Chapter 3

# Design of the Full Custom Input Interface for synQPSK DSP Chip

## 3.1 Introduction

The chapter two discussed the concept of optical synchronous QPSK (synQPSK) transmission and function of the various building blocks in the optical synQPSK transmission system. In the synQPSK receiver side, once the received signal is converted from optical to the electrical domain through the balanced photodiode pair, the resulting signal is fed to a 5 bit A/D converter [5]. This A/D converter nominally operates at 10 Gsymbols/s and is designed using a SiGe technology. The 10 Gsymbols/s A/D converter output data is then fed to the DSP unit which processes the data according to the algorithm discussed in chapter two. The DSP chip is designed using a 130 nm bulk CMOS technology. The signal processing unit of the chip (i.e.: the unit that executes the algorithm) uses CMOS logic with signal swing between 0 and +1.2 V. CMOS logic systems can not switch at the output data rate of the A/D converter (i.e. 10 Gbit/s). Therefore it is necessary to reduce the input data rate of DSP chip to about 1.25 Gbit/s, which is within the capabilities of the CMOS logic circuits. This is achieved using an array of full-custom designed 10 Gbit/s 1:8 demultiplexers. The input of the DEMUXes uses source coupled FET logic (SCFL) with signal swing between 1.4 V and 1.8 V. The output of the DEMUXes uses CMOS logic.

This chapter discusses the design of the input interface for the CMOS DSP chip version A and the CMOS DSP chip version B. First, a brief introduction to the 130 nm CMOS process is given. Then the design of transmission lines on chip and on prototyping ceramic board is discussed. This includes deciding cross section dimensions of various types of transmission lines in order to obtain 50Ω characteristic impedance and minimum transmission loss. After that the design of two basic building blocks of the 1:8 DEMUX, a 1:2 DEMUX and a static frequency divider, is discussed. The discussion includes circuit schematics, block diagrams, layout design, simulation results, and the test results. Then the design of the input DEMUX interface for the DSP CMOS chip version A is discussed. This interface includes a 10 channel 10 Gbit/s 1:8 DEMUX array. Special attention has been given to the design of the clock distribution network. Furthermore the layout design issues of the large scale ICs (like CMOS chip A and CMOS chip B) are discussed. The discussion also includes circuit schematics, block diagrams, layout, simulation results, and test results. Finally, the design of the input DEMUX interface for the DSP CMOS chip version B is discussed. This interface includes a 20 channel 10 Gbit/s 1:8 DEMUX array. As most design details of the CMOS chip version A is similar to the CMOS chip version B, only the new or the upgraded features are discussed here. Simulation and test results are also presented.

## 3.2 Overview of the 130 nm CMOS Process

CMOS technology dominates the digital device market because CMOS logic ideally has no static power dissipation and the CMOS technology requires very few devices. This is in contrast to the bipolar or GaAs technologies. Furthermore the dimensions of CMOS devices scale down more easily and have lower fabrication cost than the other technologies. Another attractive feature of the CMOS technology is the possibility of placing both analog and digital circuits in the same die. The analog blocks may use SCFL and the digital blocks may use CMOS logic. Integration of analog and digital blocks into the same die improves the chip performance. This is achieved by avoiding imperfect external interconnects and reducing the cost of packaging. Initially MOSFETs were quite slower and noisier than the bipolar transistors, finding limited applications. However the device scaling capability of CMOS technology continues to improve the speed of the MOSFETs. The intrinsic speed of MOS transistors has increased several orders of magnitude in the last four decades allowing the design of multi-gigahertz analog circuits using CMOS technology.

The ideal scaling theory of active devices in CMOS technology follows the following three rules [45, 46]: (1) all lateral and vertical dimensions will be reduced by a factor α(>1); (2) the threshold voltage and the supply voltage will be reduced by a factor α ; (3) all the doping levels will be increased by a factor α (Figure 3.1). Since the dimensions and voltages scale together, all electric fields in the transistor remain constant, hence the name ´´constant electric field`` scaling theory. With the scaling down of the devices and corresponding scaling of threshold voltage results in a considerable amount of leakage power dissipation due to exponential increase in the sub-threshold leakage current conductance.

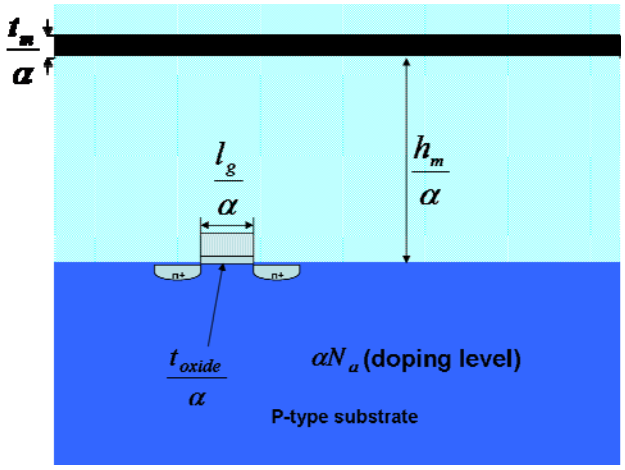



**Figure 3.1:** Scaling of the CMOS technology

The 130 nm triple well bulk deep submicron CMOS technology is used in the designs discussed in this chapter [45]. The cross section of the process is shown in the Figure 3.2. Six layer Cu metallization and the $SiO_2$ dielectric ($\varepsilon_r \approx 4.2$) for the high wiring density and the deep n-well (NISO) for substrate isolation are available. The top metal layer thickness is

0.9 µm, the bottom metal layer thickness is 0.22 µm, and the in-between metal layers have a thickness of 0.35 µm. The top metal is usually used for power distribution owing to its thickness. A thin epitaxial layer ($\approx$10 µm) is on the top of the substrate to reduce the junction capacitance. As the cross section shows the process has epitaxial substrate with the low bulk resistivity.

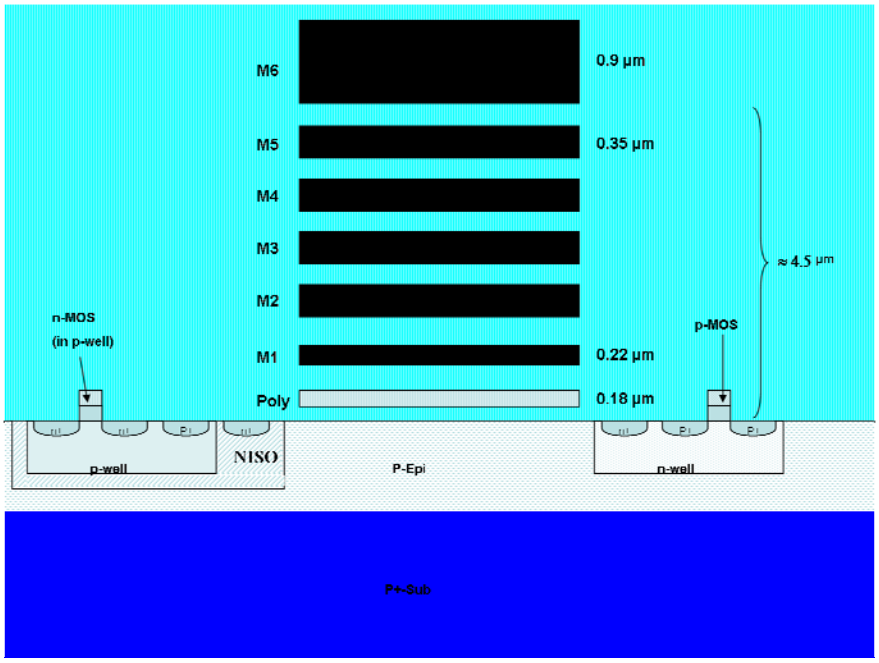



**Figure 3.2:** Process cross section of the 130 nm CMOS process

The reduced dimensions of this CMOS process compared to the 180 nm or 250 nm process allow high integration density and improved intrinsic performance of the active devices. Availability of six metal layers allows forming various useful structures (i.e.: capacitors, inductors, transmission lines, etc). The shrinking of vertical dimensions leads to higher resistivity which leads to higher losses. Shrinking sizes also introduce high parasitic capacitances. This effect pose a challenge when designing passive components and analog devices.

Figure 3.3 shows the simulated n-type MOSFET characteristics of drain current, $I_D$, versus drain-to-source voltage, $V_{DS}$, for different values of gate-to-source voltage, $V_{GS}$.

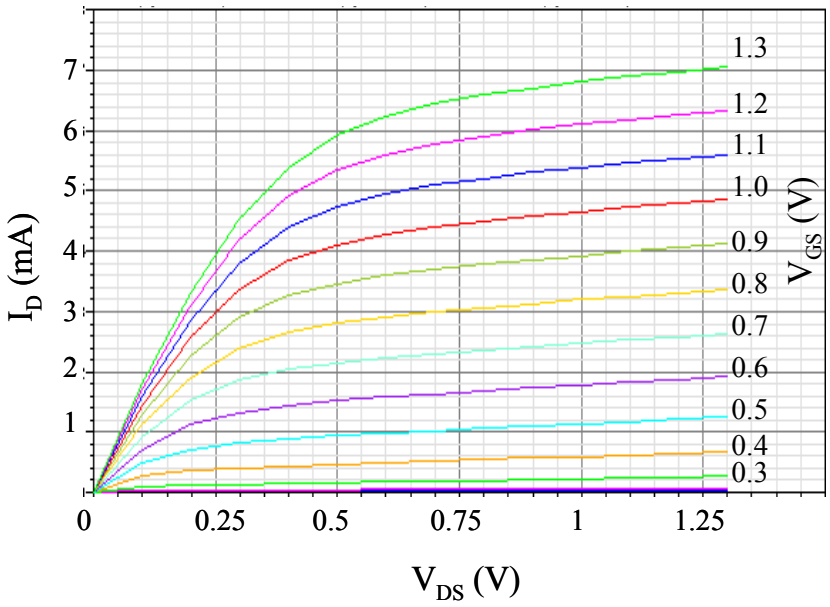



**Figure 3.3:** Simulated DC characteristics of the n-type MOSFET of 10µm width and 130 nm length fabricated in HCMOS_9GP process

A 130 nm CMOS technology is used for all the designs with High Speed and Low Leakage (HSLL) options in the mixed signal environment. The transistors have a $f_T$ of approximately 90 GHz. The threshold voltage $V_{TH}$ is about 0.3 V [45]. The circuit simulator is Spectre® and the layout editor is Virtuoso-XL®. The complete design is done in the Cadence circuit design environment.

## 3.3 The Design of On Chip and on Ceramic Board Transmission Lines

With the operating frequency in the range of tens of gigahertz, a careful design of the transmission lines is a must. The shrinking feature sizes helps to increase the operating frequency. The main design criteria for the transmission lines are maintaining the characteristic impedance at a pre-defined value which is equal to the terminal impedances (preferably 50 Ω) of the system, and maintaining line loss at a minimum level. The aim of the transmission line design is deciding the line dimensions so as to achieve above mentioned goals. The modern CMOS process with its complex architecture allows various types of transmission lines to be formed. The double layer ceramic board structure also allows different types of transmission lines to be formed.

The S-parameter (scattering parameter) model for the small signals of the two port network shown in the Figure 3.4 can be expressed as [47]

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \qquad \textbf{3.1}$$

where $S_{11}$ is the input reflection coefficient and $S_{21}$ is the forward transmission coefficient with output properly terminated. All transmission lines can be modeled as a two port (or multi-port) network. In such case the aim of the transmission line design is to minimize reflection ($S_{11}$) and maximize forward transmission ($S_{21}$) while the transmission line is terminated by a 50Ω resistor. The theory of reciprocity implies $S_{12} = S_{21}$.

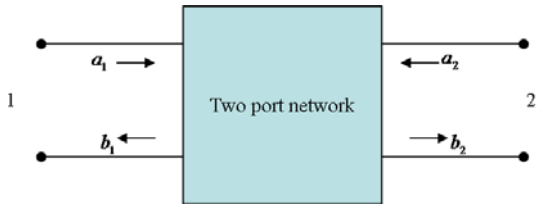



**Figure 3.4:** Incident and reflected waves of a two port network

For a lossy transmission line the characteristic impedance ($Z_0$) can be expressed as [47]

$$Z_0 = \sqrt{\frac{R_0 + j\omega L_0}{G_0 + j\omega C_0}}, \qquad \textbf{3.2}$$

where $R_0$, $G_0$, $L_0$, and $C_0$ denotes the resistance, conductance, inductance, and capacitance per unit length respectively. The complex propagation constant is $\alpha + j\beta$ where $\alpha$ is the attenuation constant and $\beta$ is the phase constant [47]. The attenuation is $A_0 = 20 \cdot \log_{10} e^{-\alpha l}$, where $l$ is the length of the transmission line. At high frequencies $R_0 << \omega L_0$, and $G_0 << \omega C_0$ holds. The loss in the transmission which is a combined result of conductor loss, dielectric loss, and Si substrate loss needs complex analysis with EM considerations.

### 3.3.1. Microstrip Line (MS-line)

A MS-line in CMOS chip is implemented using Metal-6 and Metal-1 where Metal-1 is used as the ground plane ( Figure 3.5 (left)) . As Metal-1 is the bottom metal layer, the ground plane insulate the E-field of the signal line from the lossy substrate. Because M-1 and M-6 are the furthest apart metal layers, the ground plane and the signal line are as far apart as possible. This gives the signal line maximum width for a given characteristic impedance and as a result transmission loss is minimized. The EM field lines in the microstrip line are not entirely contained in the dielectric. Therefore the propagation mode in the microstrip is not

entirely transverse EM mode (TEM mode) but quasi-TEM. Using the ADS® optimization tool it is obtained that the width of the signal line ($w$) should be 6.4 µm where $h$=3.43 µm, dielectric $\varepsilon_r = 4.2$, and line length 200 µm. The corresponding $S_{11}$ curve is shown in the. Figure 3.6.

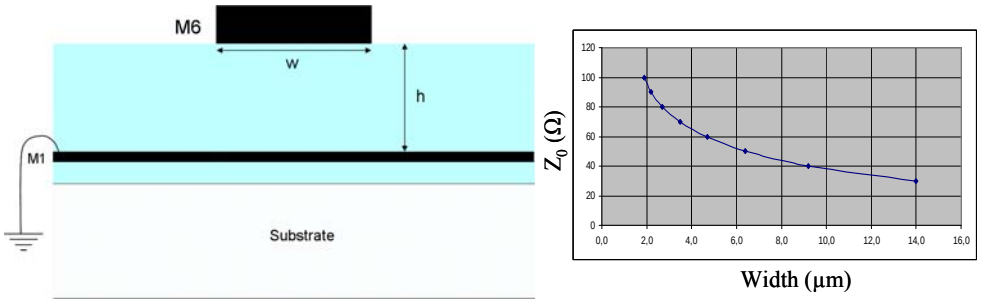



**Figure 3.5:** Microstrip line geometry (left) and its characteristic impedance as a function of conductor width (right)

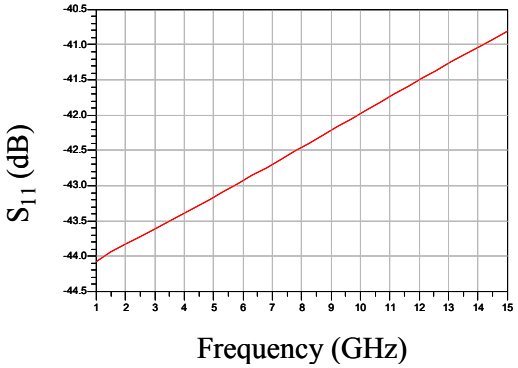



**Figure 3.6:** $S_{11}$ curve of the on chip microstrip line

## 3.3.2. Co-planar Waveguide with Ground Plane (CPWG)

A co-planar waveguide with ground plane (CPWG) is used extensively in the prototyping (ceramic) board design. CPWG has ground planes by the side of the signal line and underneath (Figure 3.7(left)). As $s << h$, $Z_0$ depends predominantly on the width of the transmission line and spacing between signal line and ground planes by the side of the signal line. If $w$ increases $L_0$ also increases and if $s$ increases $C_0$ decreases. Hence, $Z_0$ increases

with the *s* and decrease with the *w*. A normal co-planar waveguide suffers higher loss than a microstrip line at high frequencies due to stronger EM coupling to the lossy dielectric. But with the ground plane underneath that problem can be avoided. Using the ADS® optimization tool it has been estimated that *w*=100 µm and *s*=50 µm makes $Z_0$ very close to 50 Ω. For this calculation substrate ($Al_2O_3$) $\varepsilon_r = 9.9$, *h*=381 µm, and the length of the line is 15000 µm. Figure 3.8 (right) shows the $S_{11}$ curve for the above conditions.

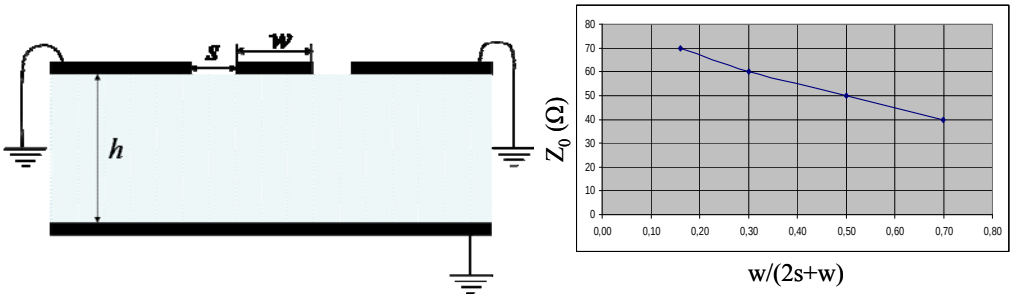



**Figure 3.7:** Geometry of CPWG (left) and its characteristic impedance as a function of aspect ratio (right)

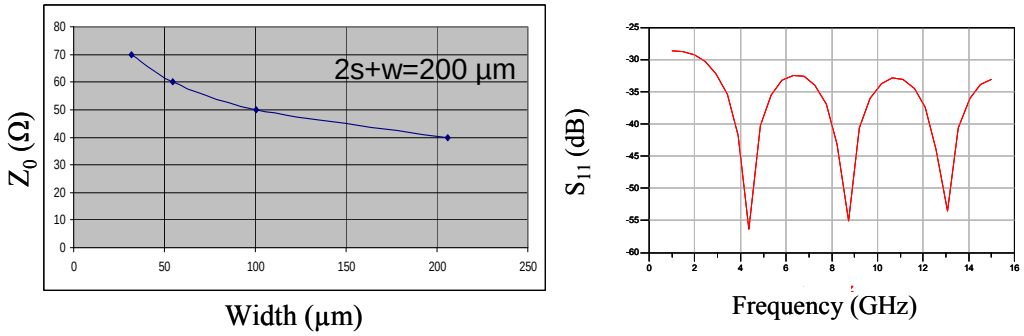



**Figure 3.8:** Characteristic impedance of CPWG as a function of width when 2s+w=200 µm (left) and $S_{11}$ curve of the CPWG in the ceramic board when w=100 µm (right)

## 3.3.3. Edge-Coupled Co-planar Waveguide with Ground Plane(ECCPWG)

ECCPWG is used when the space available to route the transmission lines is tight so that CPWG can not be implemented [48]. This type of transmission lines are used when differential pairs are available at the input and at the output. Because of the differential signals the center of two signal lines can be considered as virtual ground (symmetry property). In CCPWG there are two signal lines side by side and by the sides of the signal

conductor pair there are ground planes. In addition there is a ground plane underneath the signal conductors. It has been estimated that $w$=80 µm, $s/2$=12.5 µm, and $g$= 32.5 µm makes $Z_0$ of a single-ended line very close to 50 Ω. For this calculation substrate ($Al_2O_3$) $\varepsilon_r = 9.9$, $h$=381 µm, and the length of the line is 14000 µm. In this simulation a finite width ground conductors were used. Figure 3.9 (right) shows the $S_{11}$ curve for the above conditions.

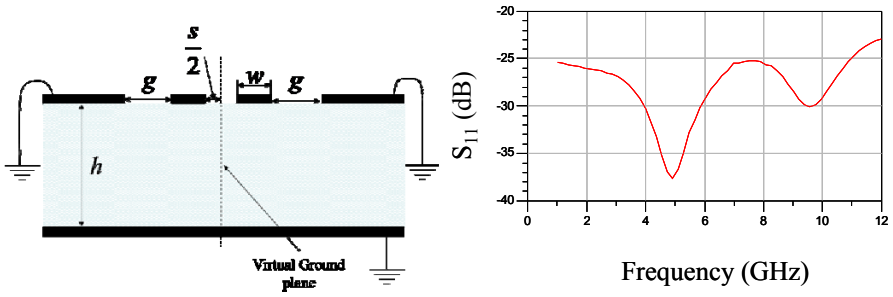



**Figure 3.9:** Geometry of ECCPWG (left) and $S_{11}$ curve of the ECCPWG in the ceramic board (right)

## 3.4 Full Custom Design of Static Frequency Divider and 1:2 DEMUX ICs

In order to verify the performance and limitations of the 130 nm CMOS technology and to establish the proper design flow it is necessary to develop and fabricate basic modules of the 1:8 DEMUX. Therefore, a standalone 1:2 DEMUX module and a static frequency divider module was designed, fabricated, and tested before the final versions of the CMOS DSP chip versions A and B were sent in for fabrication.

Normally, the highest operation frequencies for digital logic design are achieved by using differential Current Steering Logic (CSL), such as bipolar Emitter Coupled Logic (ECL) or Source Coupled FET Logic (SCFL) [49-58]. This logic family has the advantage of the excellent immunity to common mode noise and higher state change speed. The fast state change of SCFL benefits from its relatively small logic swing. However, the large overdrive voltage necessary for high frequency operation requires a large signal swing to ensure the correct switching operation of the transistor. This also restricts the speed. An other problem in CMOS technology is the voltage headroom in the logic circuit design. With the scaling down of the size of CMOS transistors, supply voltage scales down proportionally. The low supply voltage makes the voltage allotment to the stacked SCFL topology critical because the threshold voltage does not scale down at the same rate as supply voltage. One remedy for this problem is to apply higher than rated voltage to stacked SCFL circuit while maintaining the voltage across each transistor smaller than the rated voltage.

SCFL is also characterized by high functional equivalence and reduced sensitivity to threshold voltage variations. The current mode logic approach ensures an almost constant current consumption from power supplies, thereby reducing power supply noise. The major drawbacks of SCFL are low density and high power consumption.

All the following systems use Source Coupled FET Logic (SCFL). To reduce the chip area and to minimize effects of process variations, resistive loads are replaced by active loads wherever it is possible. MOS transistors with a reference voltage applied to the gate act as current sources. Both systems operate with 1.8 V supply voltage and 400 $mV_{p-p}$ single ended voltage swing. Both circuits are designed with 50 Ω input and output buffers to enable proper high speed testing.

### 3.4.1. Static Frequency Divider Test Chip

The performance of a static frequency divider is a standard benchmark used to qualify and compare high-speed technologies. The static frequency divider test chip consists of 50 Ω input and output buffers, and the static frequency divider module. The input buffers are composed of MOS source followers with a 50 Ω pull-up resistor to +1.8 V to serve as a line termination. The static frequency divider module contains two D-latches connected in Master- Slave (MS) configuration with the inverted output fed back to the data input (Figure 3.10). The two identical latches are driven by complementary clock signals [7, 61-66].

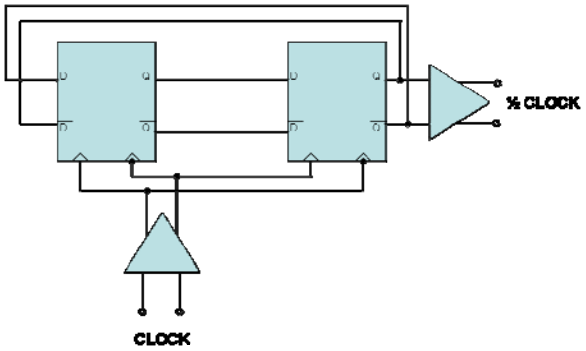



**Figure 3.10:** Static frequency divider block diagram

The maximum operating frequency ($f_{max}$) of the static frequency divider is limited by the signal propagating delay through the circuit: $f_{\max} \le 1/2t_{pd}$ ; $t_{pd} = R_L \cdot C_L$ where $t_{pd}$ is the signal propagation delay in a single delay flip flop (DFF). $R_L$ and $C_L$ are the load resistance and total capacitance at the output node respectively. $C_L = C_{FET} + C_R + C_{para,}$ where $C_{FET}$ represents total parasitic capacitance associated with the transistor and is directly proportional to its size. $C_R$ is proportional to the size of the resistor. $C_{para}$ represents other parasitic capacitances, such as those of the connecting lines. The dominant capacitance in bulk CMOS technology is the gate capacitance.

Figure 3.11 shows the circuit schematic for the D-latch. The SCL D-latch consists of two differential pairs, current switches with a current source and two pairs of NMOS and PMOS transistors, as active loads, and two source followers. The first differential pair does the sampling and the second differential pair which connected to output does the latching operation. When CLOCK (Clk) is high, the sampling pair is on and the latching pair is off.

When Clk is low, the sampling pair turns off while the latching pair turns on, storing the instantaneous state at of the output in the loop around latching pair. A single current source is used for both the sampling and the latching pair. The sampling and latching pairs have identical transistors in this design. To optimize the latch two conditions should be satisfied: (i) the latch itself must operate correctly (ii) its output signal amplitude must ensure the correct operation of the successor logic circuit. It has been demonstrated for simple circuits that it is possible to have independent current sources for sampling and latching pair [61]. Validity of those methods in complex circuit environments is yet to be shown.

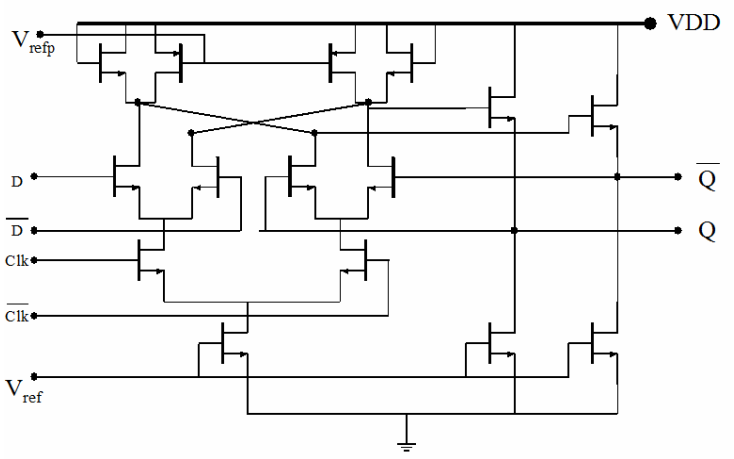



**Figure 3.11:** Circuit diagram of SCL D-latch

A MOS transistor with the voltage reference applied to the gate acts as a current source. The voltage references (Vref=0.9 V, Vrefp=1.1 V) are generated using an unequally sized PMOS - NMOS pair functioning as forward biased diodes (Figure 3.12). The current drawn by the voltage reference is negligible.

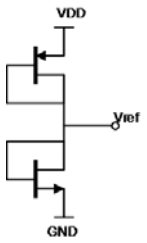
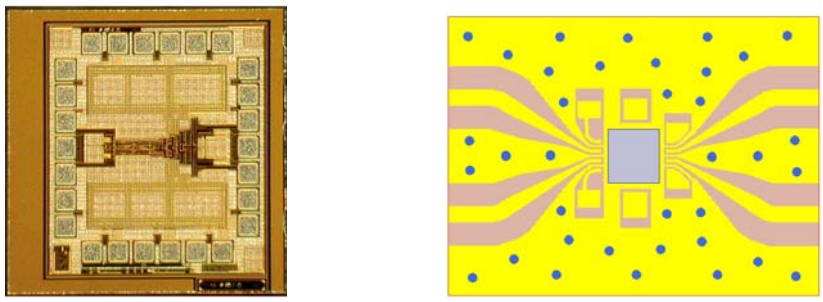



**Figure 3.12:** Schematic of the voltage reference

Figure 3.13 (left) shows the die photograph of the static frequency divider test chip. It includes a 50 Ω input buffer, static frequency divider core module and a 50 Ω output buffer. The size of the divider core is 130 μm×40 μm with a total die size of 1 mm×1 mm after dicing. Figure 3.13 (right) shows the layout of the $Al_2O_3$ ceramic board for the static

frequency divider test chip with a size of 8 mm×6 mm. 50 Ω coplanar transmission lines are used to route the high speed data and clock signals. The chip fit in a cutout of the substrate, positioned directly on the copper PCB. As a result the chip is approximately on level with the ceramic substrate, therefore enabling short bond wire loops to the substrate. 1.2 mm semi-rigid coaxial cables with SMA connectors were used to connect the high speed data and clock signals.

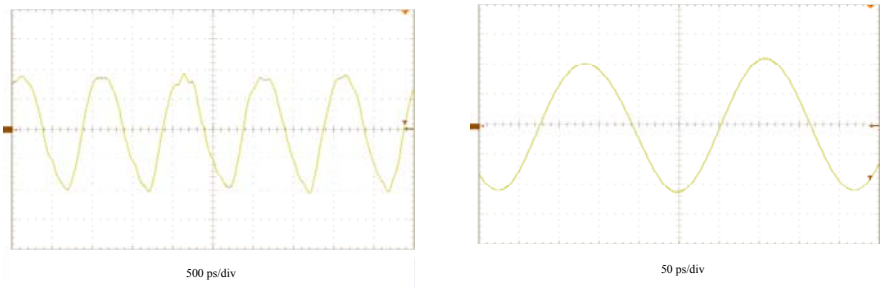


(a) (b)

**Figure 3.13:** Photograph of the static frequency divider chip (left), and layout of the ceramic substrate for the static frequency divider chip (right)

Power consumption of the simulated divider core circuit is 9 mW. Figure 3.14 shows the output waveforms when the input signal frequency is 4 GHz and 9 GHz respectively in the testing. Figure 3.15 shows the frequency domain representation of the 4.5 GHz output signal.

From the Figure 3.15 it can be seen that the second harmonic suppression is approximately 20 dB. The Figure 3.16 shows the sensitivity curve comparison of simulation without parasitics, simulation with parasitics, and the real test. The performance degradation from simulation to the real test is about 30 %.




(a) (b)

**Figure 3.14:** Output waveforms of the static frequency divider when the input signal frequency is 4 GHz (left), and 9 GHz (right).

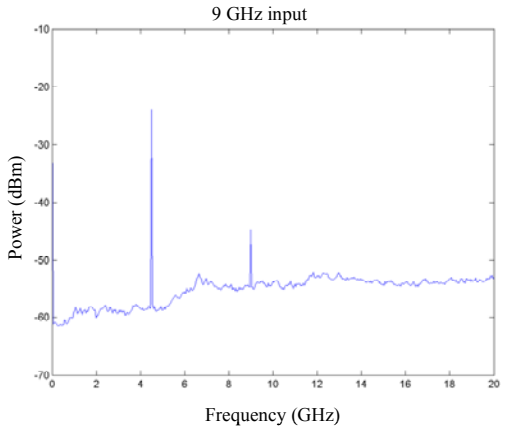



**Figure 3.15:** Frequency domain representation of the 4.5 GHz output signal

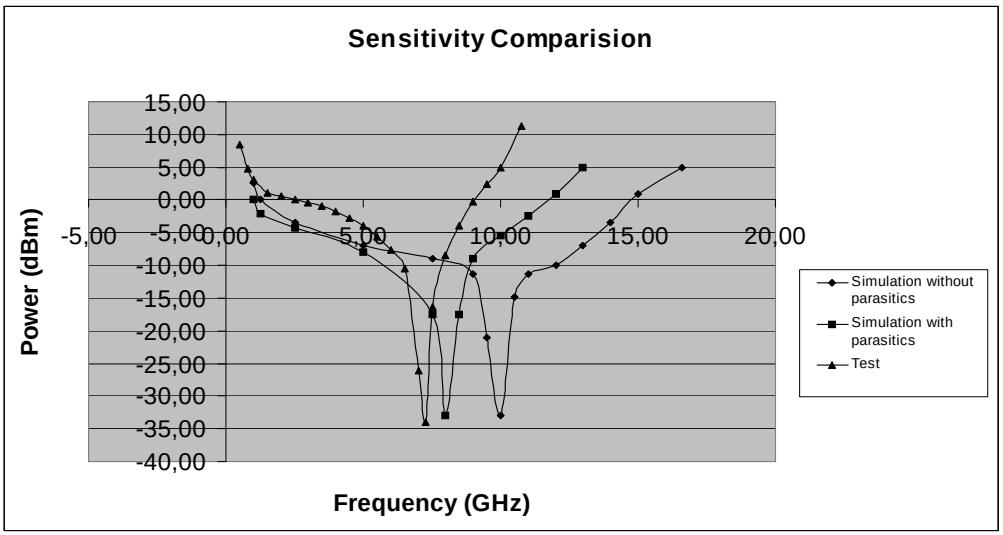



**Figure 3.16:** Sensitivity curve comparison for static frequency divider test chip

## 3.4.2. 1:2 DEMUX Test Chip

Figure 3.17 shows the block diagram of the 1:2 DEMUX test chip consisting 50 Ω data and clock input buffers, the 1:2 DEMUX core and 50 Ω data output buffers.

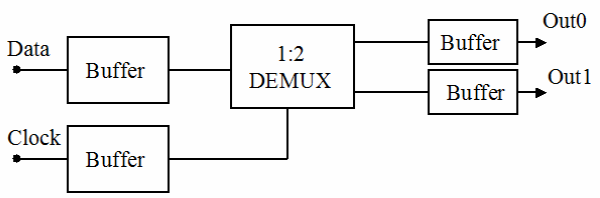



**Figure 3.17:** 1:2 DEMUX test chip block diagram

The 1:2 DEMUX consists of D-latches connected in Master-Slave (MS) and Master-Slave-Slave (MSS) configuration (Figure 3.18) [52-60]. The MS D-Flip-Flop (DFF) is triggered with the falling edge of the clock signal and the MSS-DFF with the rising edge. The MSS-DFF has one additional latch to enable the correct synchronization of the demultiplexed output channels.

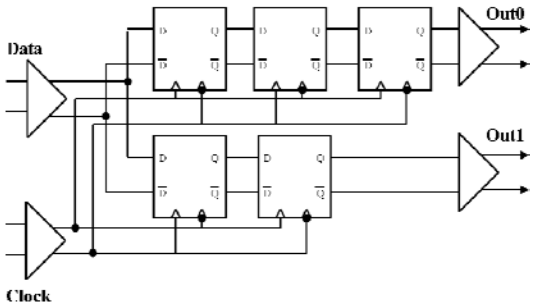



**Figure 3.18:** 1:2 DEMUX core block diagram

The photograph of the 1:2 DEMUX chip die is shown in Figure 3.19 (left). The integrated circuit includes the 50 Ω input and output buffers in addition to the DEMUX core module. The chips are diced to a size of 1 mm×1 mm while the actual 1:2 DEMUX core comprises an area of 150 µm×90 µm. The same thin film aluminium oxide ($Al_2O_3$) ceramic technology was chosen for packaging the DEMUX test chip as for the static frequency divider chip. Figure 3.19 (right) shows the layout of the ceramic board for the 1:2 DEMUX with a size of 8.1 mm×8.1 mm.
The total power consumption of the circuit is about 240 mW. But the power consumption of the core DEMUX (simulated) is only 26 mW, since most of the power is consumed in the 50 Ω input and output buffers. Simulated output eye diagrams of the 1:2 DEMUX at 10 Gbit/s input data rates with and without parasitic capacitances are shown in the Figure 3.20. The parasitic capacitances are automatically extracted from the layout of the circuit. Including the parasitic capacitances, open eye diagrams have been obtained up to a data rate of 12.8 Gbit/s in the simulations. The parasitic capacitances reduce the maximum operating frequency by about 20% compared to the ideal simulation.

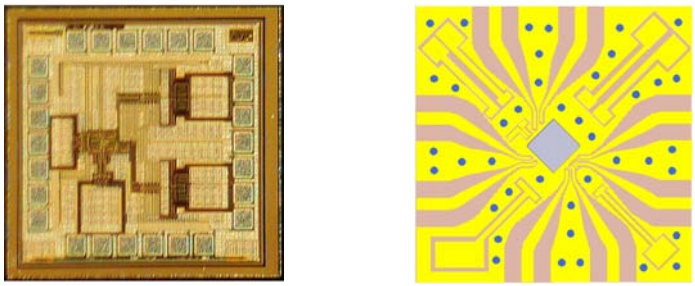


**Figure 3.19:** Photograph of the 1:2 DEMUX chip (left), and Layout of the ceramic substrate for the 1:2 DEMUX chip (right)

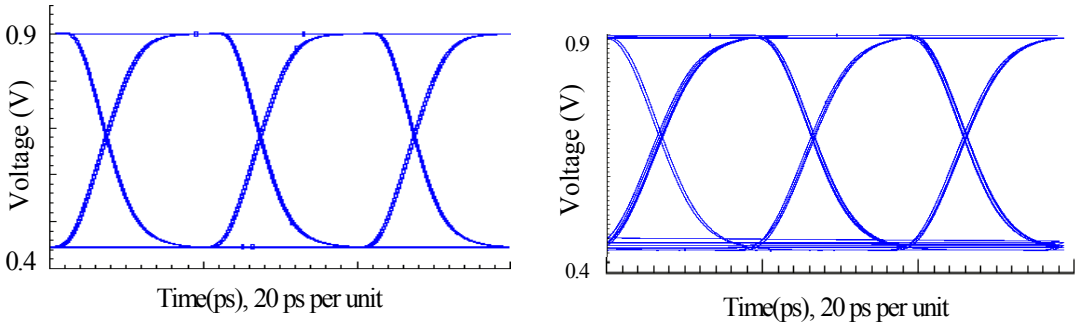



**Figure 3.20:** Simulated output eye diagram at 0.4 $V_{p-p}$ input voltage and 10 Gbit/s data rate without (left) and with parasitic (right) capacitances

Figure 3.21 shows the input and output eye diagrams, as seen in an oscilloscope, in the testing of the 1:2 DEMUX test chip with 3.75 Gbit/s input data signal.

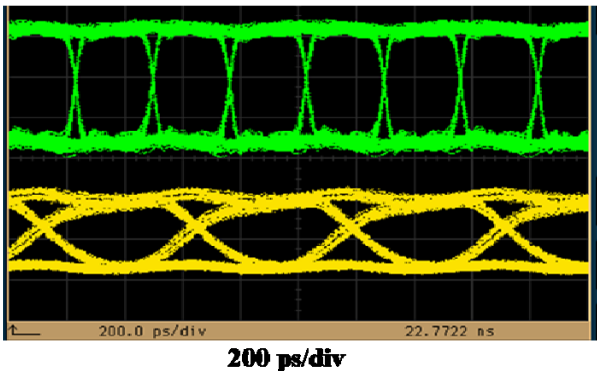



**Figure 3.21:** Input and output eye diagrams of the 1:2 DEMUX with 3.75 Gbit/s input

Both the static frequency divider test chip and the 1:2 DEMUX test chip performance were worse than expected. For example both chips were designed to operate at 10 Gbit/s but the test results showed a poorer performance than that. The possible reasons for such an out come would be:

(1) Imperfect transmission lines in the ceramic board: An ideal 50 Ω CPW transmission line has ground plane of infinite width but in practice it is much smaller (about 1mm).

(2) Reference voltage offset: It is assumed that the reference voltages Vref and Vrefp are 0.9 V and 1.1 V, respectively. But they may differ from these values in real operation. As a result, the source current of the FET may differ from the designed value. Furthermore, as a result of it active loads may operate in the nonlinear region. It is not possible to change the reference voltage without changing the supply voltage of the whole circuit. In later designs there are separate power supplies for the reference voltage generator and the rest of the circuit.

(3) Nonlinear behaviour of the active loads: Active loads may move to the nonlinear region due to change of the reference voltage. As a result signal distortions occur. In later circuits only passive loads (resistors) are used.

## 3.5 Full Custom Design of 5bit (5×2 channel) 10 Gbit/s 1:8 DEMUX

The synQPSK project focuses on designing analog-to-digital converters (ADC) to transform the incoming QPSK signal into the digital domain, and a subsequent processing circuit for carrier recovery and electronic polarization control [3, 4, 27, 32-43]. The ADCs were designed in a SiGe technology to allow a symbol rate of > 10 GS/s of the incoming QPSK signal. On the other hand, to facilitate the signal processing functions for the carrier recovery and polarization control a standard CMOS technology is preferable. CMOS technology utilizes a smaller chip area and has a potentially lower power consumption compared to bipolar technologies.

At the input of the CMOS chip there should be demultiplexers (DEMUX) to reduce the incoming data rate to a value where all successive electronic processing is possible with standard-cell logics. The version A of the CMOS chip includes a 5 bit (5×2 channels), 10 Gbit/s 1:8 DEMUX in a full-custom design and the signal processing unit in a standard-cell design. The DEMUX connects high speed (10 Gbit/s) ADC output data to the low speed (1.25 Gbit/s) digital signal processing unit (DSPU). The aim is to design a DEMUX that satisfies above requirements while using minimum possible area and consuming minimum possible power.

When compared to the CMOS logic, SCFL operates at higher speed but it utilizes considerably larger chip area and power. Therefore, for low speed operation CMOS logic is a

better option than SCFL. The last stage of the DEMUX operates at a low enough speed (2.5 Gbit/s) so that CMOS logic is used to design this stage. The use of CMOS logic also eases the burden on the clock distribution system. Combination of SCFL and CMOS logic on the same DEMUX chip gives rise to the need of having an interface between the two logic systems. One disadvantage of having SCFL and CMOS logic on a single chip is that the switching noise of the CMOS circuitry may interfere with the function of the SCFL blocks. Therefore it is necessary to isolate the two systems from each other as much as possible. The layout should be designed in such a way that there is no overlap between SCFL and CMOS logic signal lines. The power supplies to the SCFL and CMOS logic are also independent of each other.

For an 1:N DEMUX with N > 2, there are three types of structures available [59, 60]: series, parallel and tree. A series type 1:N DEMUX needs at least N D-flip-flops (DFF) to store N-bit long data words of the sub channels and every DFF must operate at the highest bit rate. This type of structure needs more chip area and more DC power. In principle, the parallel type has a simpler structure, but the highest reachable speed of the circuit will be lower, because many gates are connected to the shunting node, increasing the time constant at that node. In the tree type DEMUX only the input stage has to operate at the highest speed and the consecutive stages operate at lower speeds thus reducing size and power consumption. Therefore, the main choice for high speed DEMUXs is the tree type structure.

The DEMUX consists of static frequency divider modules, 1:2 DEMUX modules, clock control circuits, and various buffers. The input of the DEMUX has 10 differential input data channels (5 each for the inphase and quadrature component) each designed to operate at 10 Gbit/s. The nominal clock input frequency is 5 GHz, due to the half rate design of the DEMUX. All inputs are terminated with 50 Ω to obtain optimum transmission line matching to the ADC output. The 1:8 DEMUX consists of three 1:2 DEMUX stages. The first stage is designed to operate up to 10 Gbit/s input data rate, the second stage up to 5 Gbit/s, and the third stage up to 2.5 Gbit/s, respectively.

### 3.5.1. Design of Buffers, Latches, and Logic Interface

All the buffers used in this circuit (SCFL part) are simple differential amplifiers. The reason for using a differential pair is its excellent immunity to common mode noise and coupling noise [46]. Moreover, the differential pair is easy to bias and has higher linearity. Therefore differential operation has become the dominant choice in today's high performance analog and mixed signal circuits. Figure 3.22 (right) shows the frequency response of the differential pair shown in Figure 3.22 (left). The transistor gate width is 10μ, the resistor value is 480 Ω, and the source current is 1 mA. The resistors used are *n*-well type, which are smaller in size and thus have less parasitic capacitances. The small signal gain of the differential pair is 3.2 dB and the 3 dB bandwidth is 18.5 GHz.

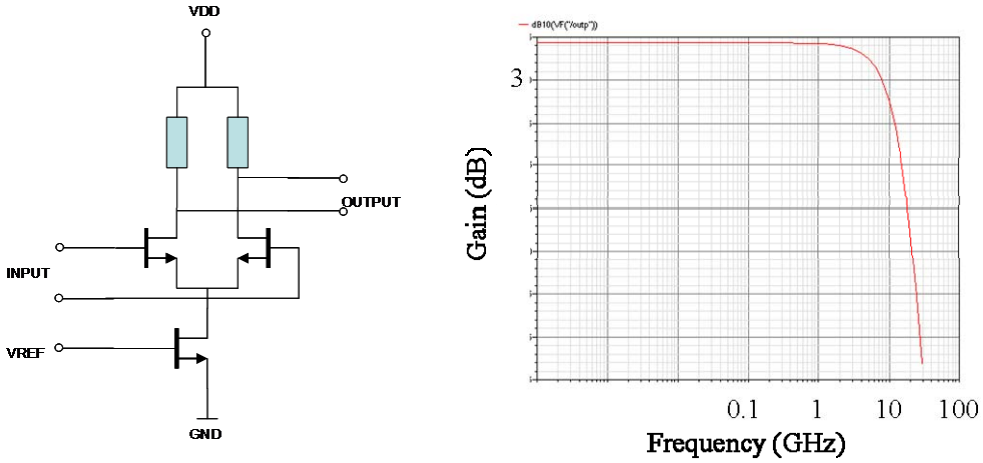



**Figure 3.22:** Differential pair schematic (left), and its frequency response (right)

A MOS transistor with the reference voltage applied to the gate acts as a current source. The voltage references (Vref=0.5 V) is generated using an unequally sized stacked PMOS-PMOS-NMOS transistor group functioning as forward biased diodes (Figure 3.23). The current drawn by the voltage reference is negligible.

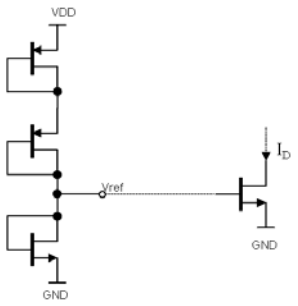



**Figure 3.23:** Voltage reference generation circuit

Figure 3.24 (top) shows the circuit schematic of the SCFL D-latch used in the design [52, 54, 55]. The D-latch consists of two differential pairs, current switches with a current source and a pair of resistive loads. The inputs to the data (D) and clock (CLK) require different dc offsets in order for the circuit to function correctly; thus, level shifting networks using source followers are required at the input. The logic high and the logic low levels at the output ($V_Q$) are

$$V_{Q,H} = V_{DD},$$
$$V_{Q,L} = V_{DD} - RI_D. \quad \textbf{3.3}$$

The minimum voltage swing required on the inputs to switch the current from one branch to the other is equal to $|V_{TH}|\sqrt{W_3/W_2}$ [67] where $V_{TH}$ is the threshold voltage, $W_2$ is the clocking transistor width, and $W_3$ is the current source width.. The noise margin of the D-latch (the difference between the logic swing and the minimum voltage swing required on the clock inputs to switch the current from one branch to the other) is given by [67]

$$\text{Noise margin} = RI_D - |V_{TH}|\sqrt{\frac{W_3}{W_2}}. \quad \textbf{3.4}$$

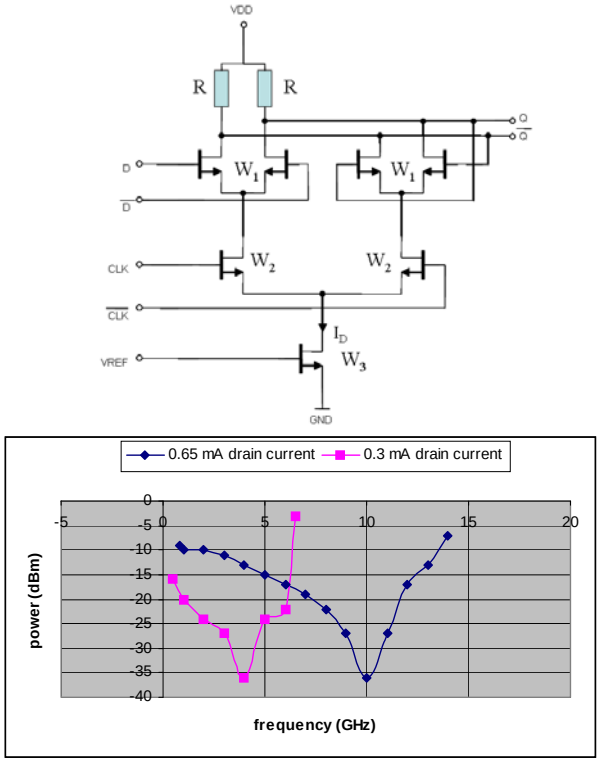



**Figure 3.24:** SCFL D-latch schematic diagram (top) and the corresponding static frequency divider performance (bottom) for different drain currents

With the increase of the clocking transistor width the noise margin also increases. Although a better noise margin is desirable, it should be mentioned that the larger clocking transistors means increased input capacitance and decreased speed. Depending on the design requirements, noise margin and speed need to be traded off.

The main design targets of a D-latch are the maximum operating frequency $f_{max}$ and the frequency range of operation. The frequency range of operation is defined as the difference between the $f_{max}$ and the minimum operating frequency $f_{min}$. The design variables are the transistor size and the source current. In order achieve high $f_{max}$ the source current of a transistor should be large (the transconductance $g_m$ increase with the source current). If the

source current is large then the transistor size should also be large. A large device limits $f_{max}$ due to the increased parasitic capacitance. By definition a static frequency divider constructed using a pair of D-latches has $f_{min}$ equal to zero. But, because of the limited slew rate of the sinusoidal input clock signal, $f_{min}$ is higher than zero. In order to achieve high $f_{max}$ and broad operating range transistor size and source current was optimized using extensive simulations. For each desired frequency range of operation the transistors had to be sized appropriately to reach the needed $f_{max}$ but still enabling broadband operation. This required a compromise between transistor size and utilized source current for each operating range, leading to different design variables for each 1:2 DEMUX cell in the overall 1:8 DEMUX. Figure 3.24 (bottom) shows the static frequency divider performances corresponding to the D-latches used in the 1st and 2nd DEMUX stages. It can be observed that the frequency divider correspond to the 1st DEMUX stage centered around 10 GHz and the frequency divider correspond to the 2nd DEMUX stage centered around 4 GHz.

Figure 3.25 shows CMOS logic D-latch [66]. The D-latch consists of two CMOS inverters and two transmission gates. When CLK is high the D-latch samples the input signal (TG1 closed, TG2 open). When CLK is low the D-latch holds the last sample (TG1 open, TG2 closed). This configuration has better noise performance than the level sensitive latch with one switch. The ratio between the sizes of p-MOS and n-MOS transistors in the inverters is 2 in order to have the logic transition at $V_{DD}/2$.

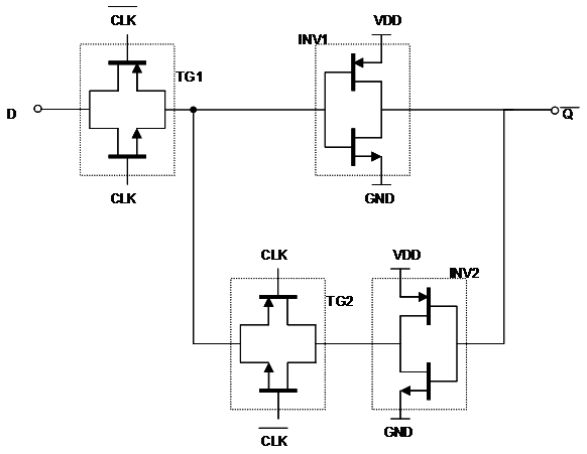



**Figure 3.25:** CMOS logic D-latch schematic

The interface between SCFL and CMOS logic consists of an input buffer (differential) and a level shifter (source follower) operating at 1.8 V supply voltage, intermediate buffer (differential) and level shifter (source follower) operating at 1.2 V, and CMOS inverter pair operating at 1.2 V supply (Figure 3.26). First and second buffers shift the signal level such that it can drive the following CMOS inverter [68, 69]. The SCFL level does not convert to CMOS levels with a single inverter stage. The inverter stage acts as a proper amplifier to convert the signal into real CMOS levels.

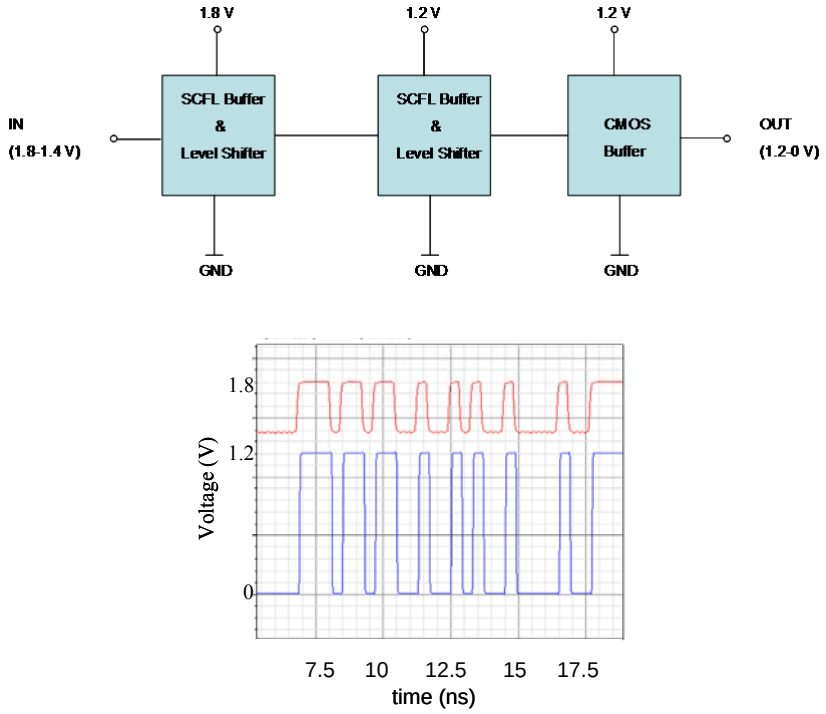



**Figure 3.26:** SCFL to CMOS interface architecture (top) and input & output waveforms at 2.5 Gbit/s data rate (bottom)

## 3.5.2. Design of 1:8 DEMUX

Figure 3.27 shows the functional block diagram of a single channel 1:8 DEMUX [59, 60]. The input, intermediate and output buffers are included in the functional blocks. This block is contained 10 times in the circuit except for the clock distribution circuitry. Because of the tree type structure used in the DEMUX the output channels are not in order. From the top the output channel numbers are 1, 5, 3, 7, 2, 6, 4, 8. This fact has to be taken into account when the DEMUX output is connected to the processing circuit. The last DEMUX stage uses CMOS logic in order to save power and space. The input operates with 1.8 V supply voltage and all the input signals should have a recommended 400 mV single-ended voltage swing. The output operates with 1.2 V supply voltage and 1.2 V voltage swing.

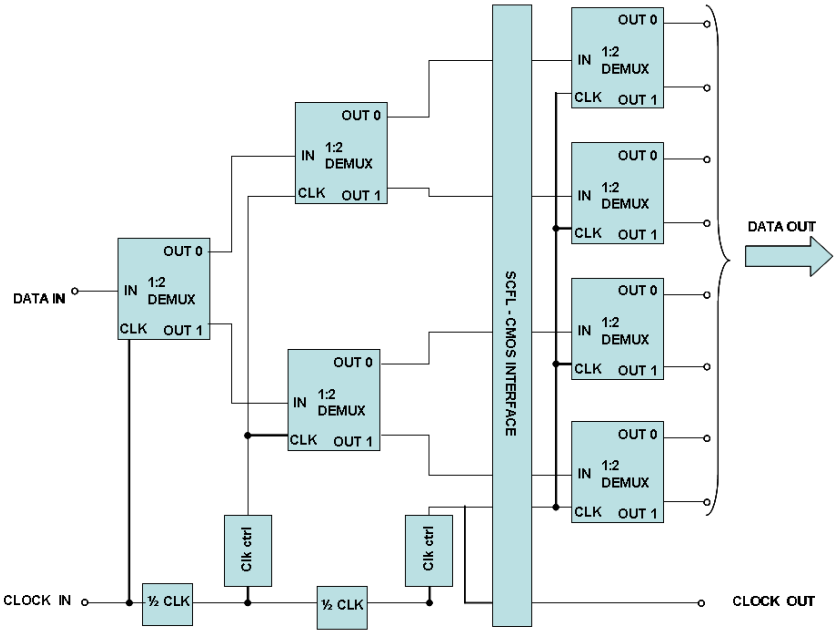



**Figure 3.27:** 1:8 DEMUX block diagram

### 3.5.3. Clock Distribution System Design

Clock distribution is a critical issue in large-area circuits. Even though the tree-type architecture provides excellent high speed performance, it involves the difficulty of the appropriate phase relationship between the different frequencies clocking the data of every stage [70]. The main requirement of the clock distribution system is to ensure the synchronicity of each 1:2 DEMUX on the same level together with the following DEMUX stages at the reduced clock and data rate. Furthermore, the clock distribution has to be able to drive every latch in each DEMUX block without degrading the quality of the clock signal. The first requirement is achieved by maintaining the length of the clock lines to all DEMUX in a same level constant and the number of buffer stages constant. Meander lines are used to maintain constant line delays whenever necessary. In order to maintain a proper clock signal so that correct switching occurs, no single buffer drives more than five subsequent buffers (fan out). Inter-stage synchronization is achieved by using clock controllers (Figure 3.28 (right)) after each clock divider stage.

The clock controller consists of a phase shifter (Figure 3.29 (left)) followed by an EXOR bit rotator (Figure 3.29 (right)). The phase shifter uses either the inphase or the 90° delayed output signal of the clock divider, depending on the control signal. The EXOR circuit can select between the inphase or the inverted clock signal. Therefore it is possible to obtain 0°, 90°, 180°, and 270° phase shifted versions of the input clock signal. DC control signals (ground/open) are applied at the control inputs [54].

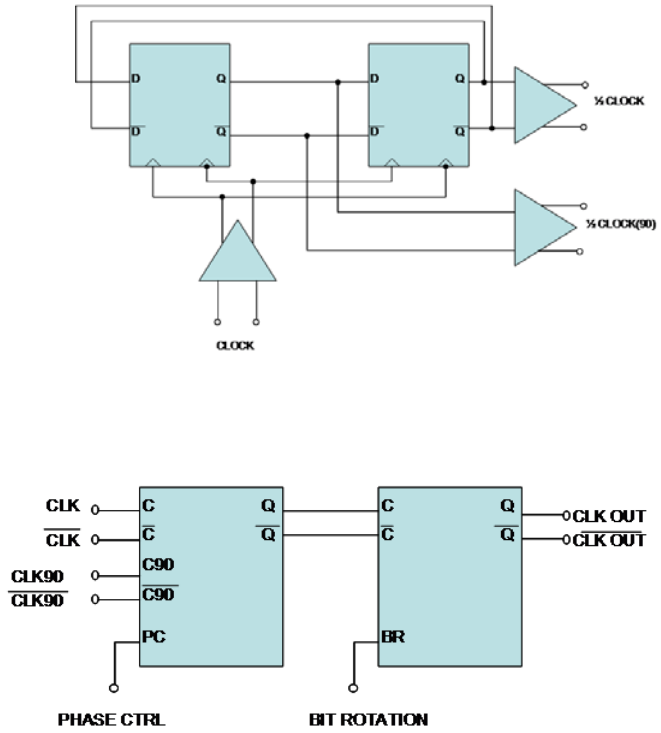



**Figure 3.28:** Clock divider (top), and Clock controller (bottom) block diagrams

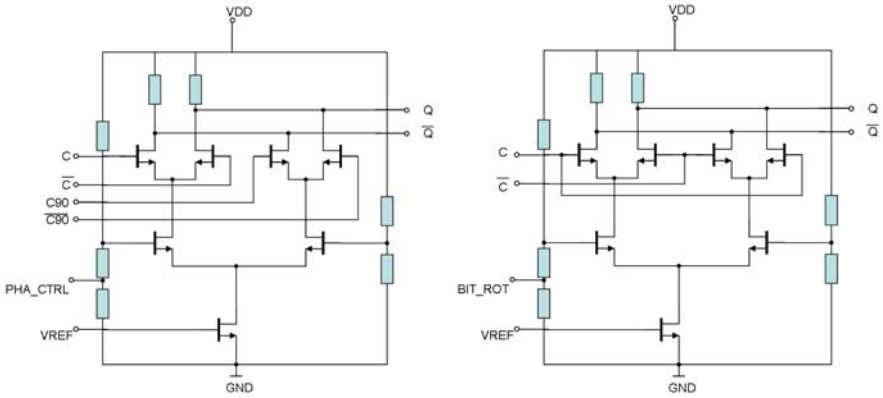



**Figure 3.29:** Phase shifter and (left), and bit rotator (EXOR) (right) schematic diagrams

The final clock distribution system has a tree architecture as shown in the Figure 3.30. The circles in the tree (except in the clock input and clock output) represent 1:2 DEMUXs. There

is a SCFL – CMOS logic interface between the second and third DEMUX stages. Clock controllers in a given stage operate identically with same control signals. The last stage of the clock distribution tree uses CMOS logic. Therefore the size of the last DEMUX stage is considerably smaller than the comparable SCFL implementation. This also relaxes the loading on the clock distribution. The next chapter discuss situations whereby most carefully designed clock distribution systems inherit clock skew.

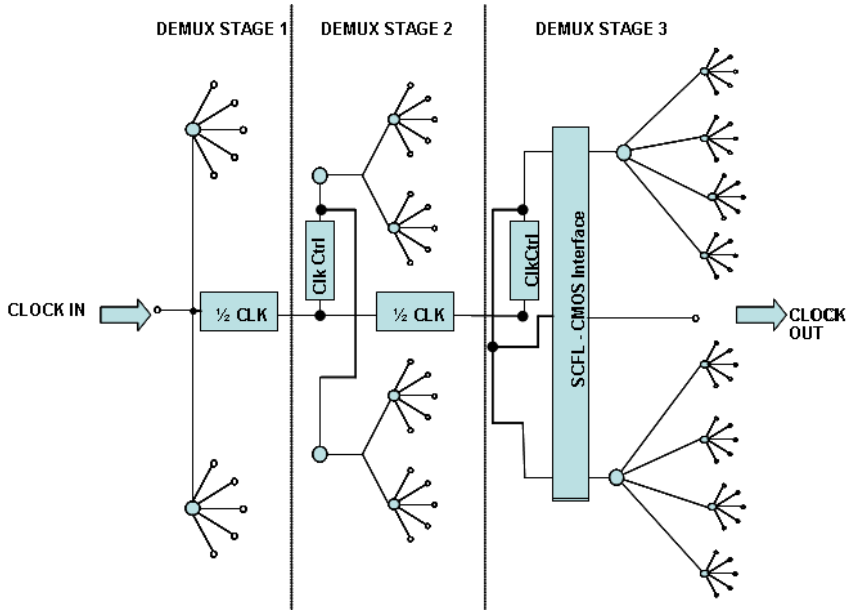



**Figure 3.30**: Clock distribution tree

## 3.5.4. Layout Design

Figure 3.31 shows the layout of the 1:8 DEMUX. As mentioned earlier, a 120 nm bulk CMOS technology from ST Microsystems (France) is used for fabrication. This technology has six copper metal layers ($\varepsilon_r$ = 4.2). Layer 1 or the bottom layer is used for signal interconnects. Layer 5 is used for ground and the layer 6 is used for power supplies. The total device count of the DEMUX chip is 6137 including 5145 transistors. The chip area is 3 mm x 2.4 mm. It is possible to design the layout of the DEMUX in a more compact form, but due to practical issues regarding the 2×5 differential 10 Gbit/s data inputs from the ADCs to the DEMUX this layout topology was selected. The clock distribution system is symmetric with respect to the horizontal center line of the chip core. Input data and clock lines are 50 Ω microstrip transmission lines. Output lines operate with CMOS logic. The IR drop or the voltage drop across the conducting metal of the power and ground lines in the chip is a critical design issue. I is the current through the supply and the ground metal conductors and R is the path resistance of the metal conductors of the supply and the ground lines. The IR drop limits the actual voltage across the devices and as a result performance degradation occurs. The

supply ($V_{DD}$) metal layer and the ground metal layer widths are carefully calculated so that they have necessary current carrying capacity and the IR drop across is within the accepted range. The metal area connected to the gate of a MOSFET is carefully chosen to avoid the antenna effect. In order to avoid the antenna effect a diode can be connected to the metal near the gate. This diode (antenna diode) can protect the gate oxide from excessive charge build up. Antenna diodes are inserted adjacent to the gates where ever necessary [71, 72]. The Calibre® design rule checker is used to check the layout for the violation of design rules. The DIVA® Layout vs. Schematic (LVS) checker is used for layout verification.

This full custom designed DEMUX will be connected to the input of the standard-cell designed DSPU and both the DEMUXs and the DSPU are integrated on a single chip. This chip consists of both SCFL (analog) blocks and CMOS logic (digital) blocks in a single device. The DSPU generates a lot of switching noise. Therefore it is necessary to isolate the full-custom DEMUX from the standard-cell design as much as possible by using substrate-to-ground contacts all around the full-custom circuit parts. The main circuitry of the DSPU fits to the center square in the middle of the layout. 10 Gbit/s data inputs are routed from the top and the bottom of the chip and are passed on in demultiplexed form to the DSPU in the chip center while the clock input comes from the side. There is an unavoidable overlap between the full-custom and standard-cell layouts. Apart from the 10 Gbit/s inputs, low speed CMOS outputs, various supply voltages, and clock phase control, the chip includes a ¼ clock frequency divider output, which is used to test the functionality of the chip.

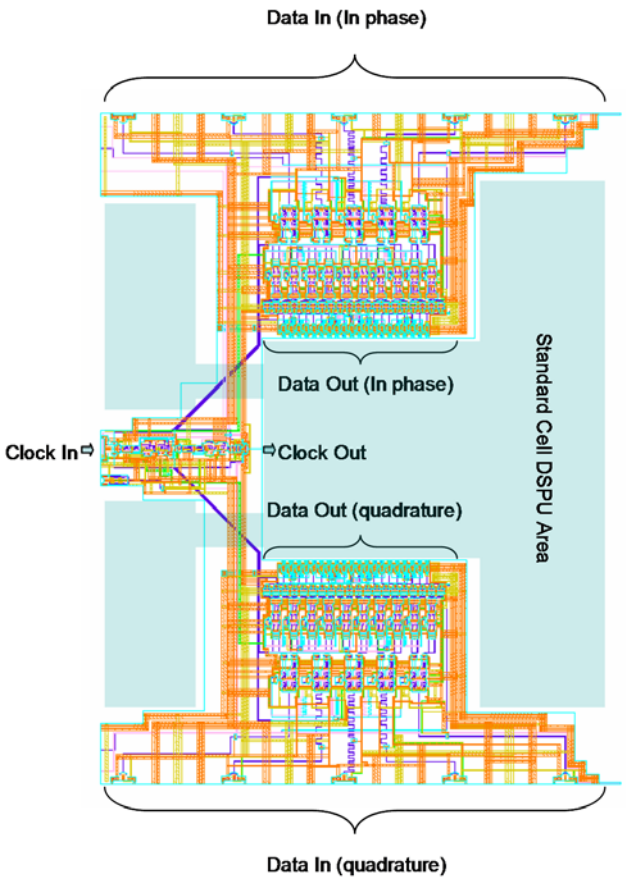



**Figure 3.31:** Layout of the 5-bit (I & Q) 1:8 DEMUX

The full-custom DEMUX and the standard-cell DSPU have to be integrated on the same chip in order to form a mixed-signal chip [73]. When the full-custom design is finished completely, it is then characterized for all process corners that are available in the standard-cell flow. The timing information is written into a standard-cell library, and the routing information of the abstract-views of the cell are written into LEF-library files that are readable by the tools for the standard-cell flow. *Cadence Aptivia* is a tool that supports these steps. The full-custom part is then included into the standard-cell design and treated as an IP (Intellectual Property) core. The layout is finished with *Cadence SoC Encounter* or Silicon Ensemble. The full-custom design is treated as a digital black-box with a certain behavior that was defined during characterization. Sign-off is done with *SoC-Encounter* and the abstract data models, which eases simulations and verification. If the interface of the full-custom DEMUX is well defined, routing between full-custom and standard-cell flow is done automatically by the tools and wire delays are taken into account. This approach is mostly used for large, complex systems that include some critical IP-cores. The main part of the system is based on standard-cells, or more IP-Cores are connected together on a high abstraction level (VHDL) and the external interface used standard-cell IO-Buffers. Figure 3.32 shows the layout and die photograph of the CMOS chip version A.

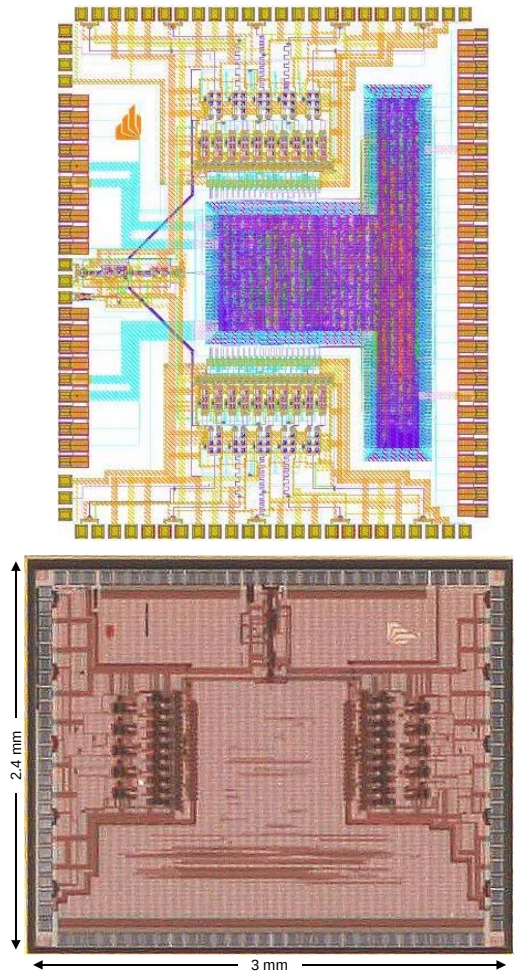



**Figure 3.32:** Layout of the chip version A (top), and die photograph (bottom)

Figure 3.33 shows the prototype ceramic board layout of the CMOS chip version A. The board is fitted with two 5 bit A/D converters and a CMOS chip. The board is 5cm×2.5 cm.

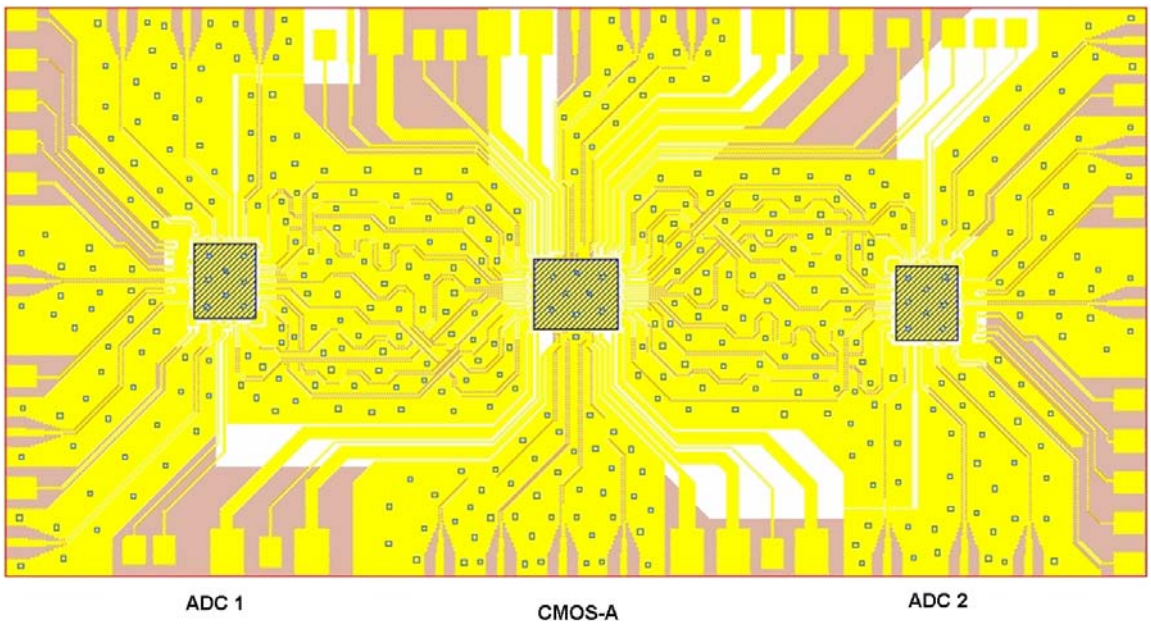



**Figure 3.33:** Ceramic board layout for CMOS version A

## 3.5.5. Simulation and Test Results

Simulations were done with a pseudo-random bit sequence (PRBS length $2^7$-1 bits) input data stream and a sinusoidal clock input signal. All input signals have a nominal peak-to-peak amplitude of 400 mV. All the input data channels were given identical PRBS patterns. The current consumption of the SCFL block is about 370 mA (1.8 V supply) in the testing. and the peak current drawn by the CMOS block is about 80 mA (1.2 V supply) at 10 Gbit/s as shown in the simulations. The average current drawn by 1.2 V block is 43 mA. Total power consumption is about 720 mW at the same data rate. This is equivalent to 72 mW of power per input data channel. Chip power consumption is a critical parameter because the chip contains not only the DEMUX but also the CMOS digital signal processing unit. Therefore it is necessary to minimize the overall power consumption. All the simulations were conducted at a temperature of 75° C.

The measurement results at the clock test output (1/4 of input clock frequency) is shown in the Figure 3.34. It operates between 0.1 GHz and 7 GHz for sinusoidal clock input signals. This frequency range is in accordance with the expected range of operation of the DEMUX. The loss of sensitivity at low input frequencies is caused by the limited slew rate of the sinusoidal input signal in combination with the transconductance of the used MOS transistors,

which were sized appropriately. In reality the clock generator output signal at low frequencies is not sinusoidal but rather rectangular with good slew rate. Figure 3.35 shows the output clock signals at 5 GHz input clock frequency (corresponding to 10 Gbit/s input data rate) and 1 GHz input clock frequency (corresponding to 2 Gbit/s input data rate).

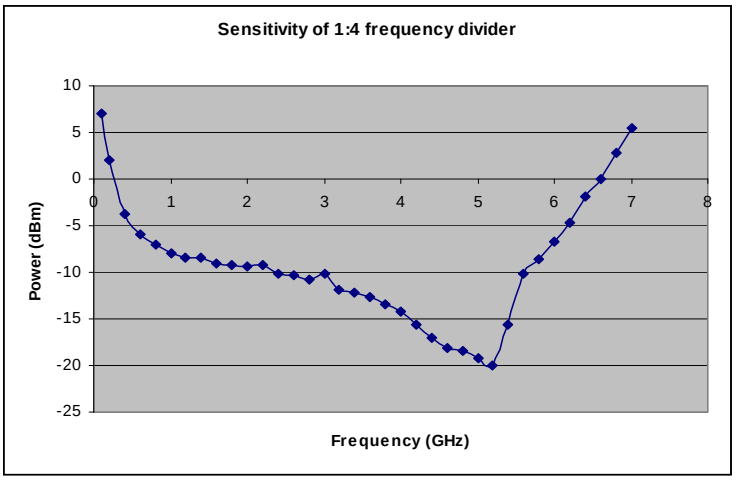



**Figure 3.34:** 1:4 frequency divider sensitivity curve

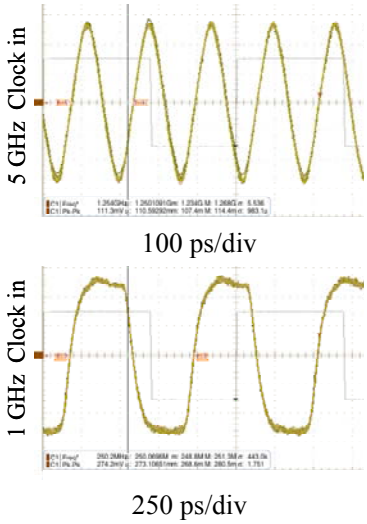



**Figure 3.35:** Output clock signals at 5 GHz input clock (top) and 1 GHz input clock (bottom)

Simulations were done also with parasitic capacitances taken into account. The parasitic capacitances are automatically extracted from the layout of the circuit. Figure 3.36 shows

simulated input and 1:8 DEMUXed output eye diagrams for input data rates of 5 Gbit/s and 10 Gbit/s, respectively. A degradation of the output eye opening with the increasing data rate is visible, but negligible. Rise and fall times are about 20 ps.

With parasitic elements included the DEMUX works properly up to about 11 Gbit/s input data rate in the simulations. The testing showed that some parts of the CMOS chip version A face thermal failure after less than an hour of operation. Therefore the DEMUX output results could not record. The more optimized layout and ceramic board design in the CMOS version B avoided this issue as shown in the next section. The proper operation of SCFL to CMOS interface is also verified by checking input and output signals in the testing.

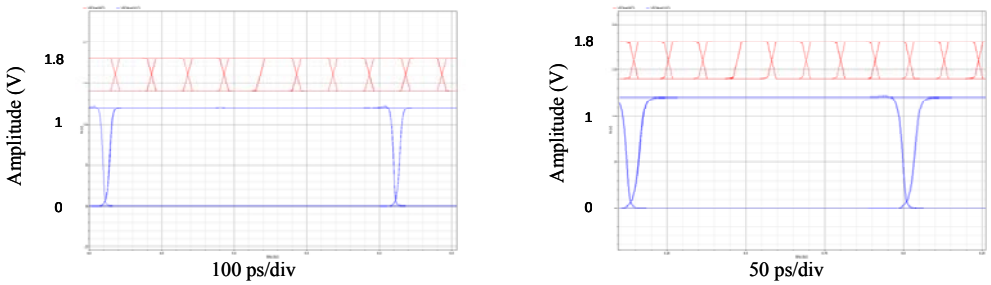



**Figure 3.36:** Input and output (1:8) eye diagrams at 5 Gbit/s (left) and 10Gbit/s (right) input data rate

Phase shifter and bit rotator functions were verified by switching the static control voltage between ground and open condition manually (control pin is either connected to ground or left open which is the default setting). It is also verified that the clock controllers (includes a phase shifter followed by a bit rotator as shown in Figure 3.28 ) in the stages 2 and 3 operate independently. To synchronize the incoming data and the half rate clock signal, the clock phase must be aligned externally. The clock alignment of the second and third DEMUX stages is then adjusted internally.

## 3.6 Full Custom Design of 5 bit (5×4 channel) 10 Gbit/s 1:8 DEMUX

The CMOS chip version B processes received synQPSK signals with polarization multiplex. The version B of the CMOS chip includes a 5 bit (5×4 channels), 10 Gbit/s 1:8 DEMUX in a full-custom design and the signal processing unit in a standard-cell design. The DEMUX connects high speed (10 Gbit/s) ADC output data to the low speed (1.25 Gbit/s) digital signal

processing unit (DSPU). The input of the DEMUX has 20 differential input data channels (5 each for the inphase and quadrature components of two orthogonal polarizations) each operating at 10 Gbit/s. The clock input frequency is 5 GHz, due to the half rate design of the DEMUX. All inputs are terminated with 50 Ω to the +1.8 V supply to obtain optimum transmission line matching to the ADC output. The 1:8 DEMUX consists of three 1:2 DEMUX stages. The first stage is designed to operate up to 10 Gbit/s input data rate, the second stage up to 5 Gbit/s, and the third stage up to 2.5 Gbit/s, respectively.

The aim is to design a DEMUX that satisfies above requirements while using minimum possible area and consuming minimum possible power. Most of the circuit details are identical to that of CMOS chip version A. Therefore this section discusses clock distribution issues, layout design issues, and simulation test results only.

### 3.6.1. Clock Distribution System

Clock distribution is a critical issue in large area circuits. This issue was discussed in detail in the design of CMOS chip version A. This circuit has a larger clock distribution system because there are twice as many 1:8 DEMUX blocks as in CMOS chip A. Even though the tree-type architecture provides excellent high-speed performance, special care has to be taken to achieve the appropriate phase relationship between the different clock frequencies latching the data of every stage.

The final clock distribution system is shown in the Figure 3.37. The clock signals for all the three 1:2 DEMUX stages are symmetrically distributed to each polarization component (P1 and P2) of the 1:8 DEMUX block. The clock signals are routed between inphase (I) and quadrature (Q) DEMUX blocks of each polarization in order to maintain clock line lengths equal. There are several buffer stages before a clock signal reaches a 1:8 DEMUX block. Within each 1:8 DEMUX block clock signals are distributed using the tree architecture as discussed in the CMOS version A.

### 3.6.2. Layout Design

A great effort has been made to optimize the layout compared to the DEMUX for CMOS chip A. Each individual block has been designed in such a way that it occupies minimum possible space while adhering to the design rules and the metal layer current carrying capacity [71-73]. A great deal of effort has been taken to minimize the IR drop or the voltage drop across the conducting metal of the power and ground lines in the chip. The measures such as increasing the number of ground and supply pads, designing the layout more compact, and increasing the width of the supply and ground metal lines as much as possible reduce the IR drop. All the internal signal lines are designed identical. Therefore, the main focus of the size reduction was the optimization of the signal and more importantly the clock paths inside the DEMUX cell. Figure 3.38 shows the comparison between 1:8 DEMUX core areas of this DEMUX and the DEMUX discussed in the CMOS version A.

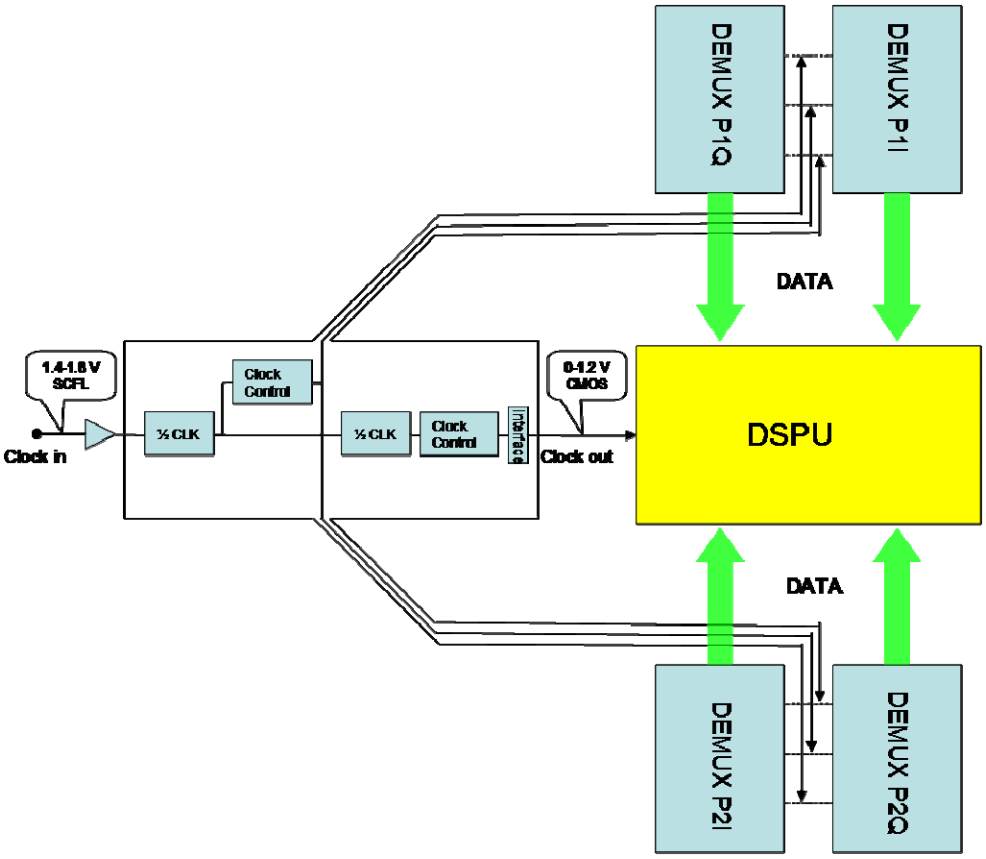



**Figure 3.37:** Clock distribution system of the CMOS B

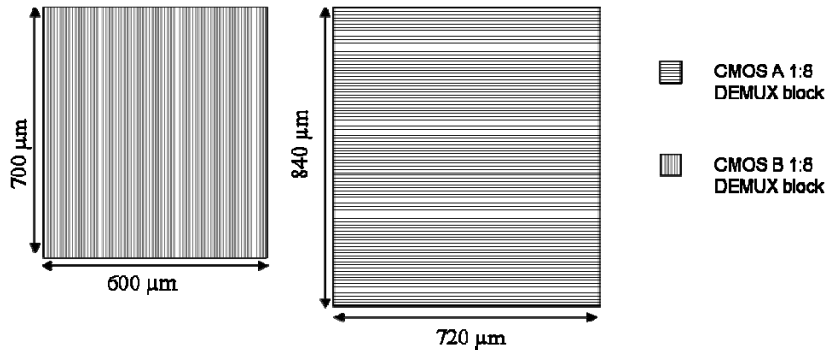



**Figure 3.38:** Size comparison of 1:8 DEMUX blocks

Figure 3.39 shows the layout of the core of a single 1:8 DEMUX cell. All demultiplexing stages and the interface stage are depicted in that figure, which consumes and area of 600 µm×700 µm. As a result of the layout optimization process it was possible to compress the size of a 1:8 DEMUX core by 30% when compared to the DEMUX discussed in the CMOS version A. Further size reduction is possible, but was omitted since the overall size of the chip is limited by the necessary number of pads and not the active circuit area. Each 1:8 DEMUX

block is among other things encircled by a guard ring (connecting the substrate to the ground) in order to suppress the switching noise generated by the DSP block.

This full custom designed DEMUX will be connected to the input of the standard-cell-designed DSPU and both the DEMUXs and the DSPU are integrated on a single chip. This chip consists of both SCFL (analog) blocks and CMOS logic (digital) blocks in a single device. The DSPU generates a lot of switching noise. Therefore it is necessary to isolate the full-custom DEMUX from the standard-cell design as much as possible by using substrate-to-ground contacts all around the full-custom circuit parts. The main circuitry of the DSPU fits to the center square in the middle of the layout. 10 Gbit/s data inputs are routed from the top and the bottom of the chip and are passed on in demultiplexed form to the DSPU in the chip center while the clock input comes from the side. There is an unavoidable overlap between the full-custom and standard-cell layouts.

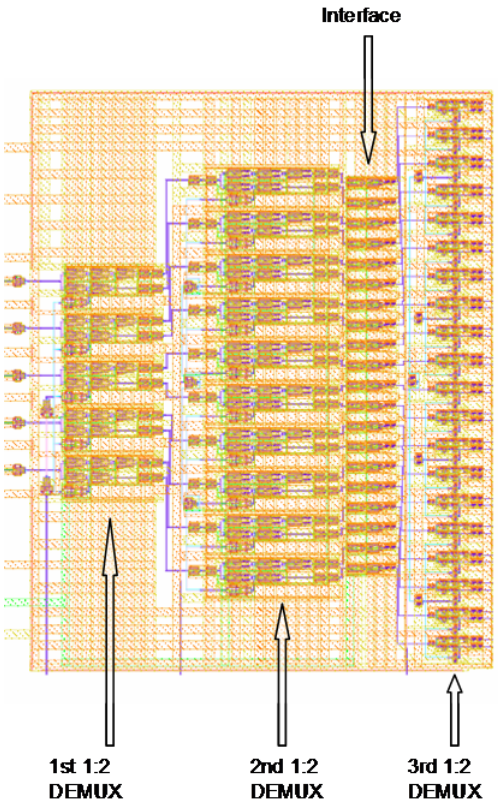



**Figure 3.39:** Layout of a single 5 bit 1:8 DEMUX core

Apart from the 10 Gbit/s inputs, low speed CMOS outputs, various supply voltages, and clock phase control, the chip includes several outputs (1/4 clock divider output and 3rd stage DEMUX output), which are used to test the functionality of the chip. Figure 3.40 shows the complete layout of the 1:8 DEMUX with the area for the standard-cell part left open. The total device count of the DEMUX chip is 11838 including 9890 transistors. The total DEMUX layout area, including all input buffer stages, interconnections and voltage supply metallization, amounts to 5.952 mm².

Integrating the full custom and standard cell based designs of CMOS chip version B is the major issue for the synQPSK project as data must be passed seamlessly from the demultiplexers to the standard cell system. Therefore, the output stage of the demultiplexers was designed as standard CMOS buffers with similar behaviour as the buffers of the standard cell libraries. During all design stages of the full custom demultiplexers, the outputs were loaded with a standard cell from the technology library with a typical input capacitance.

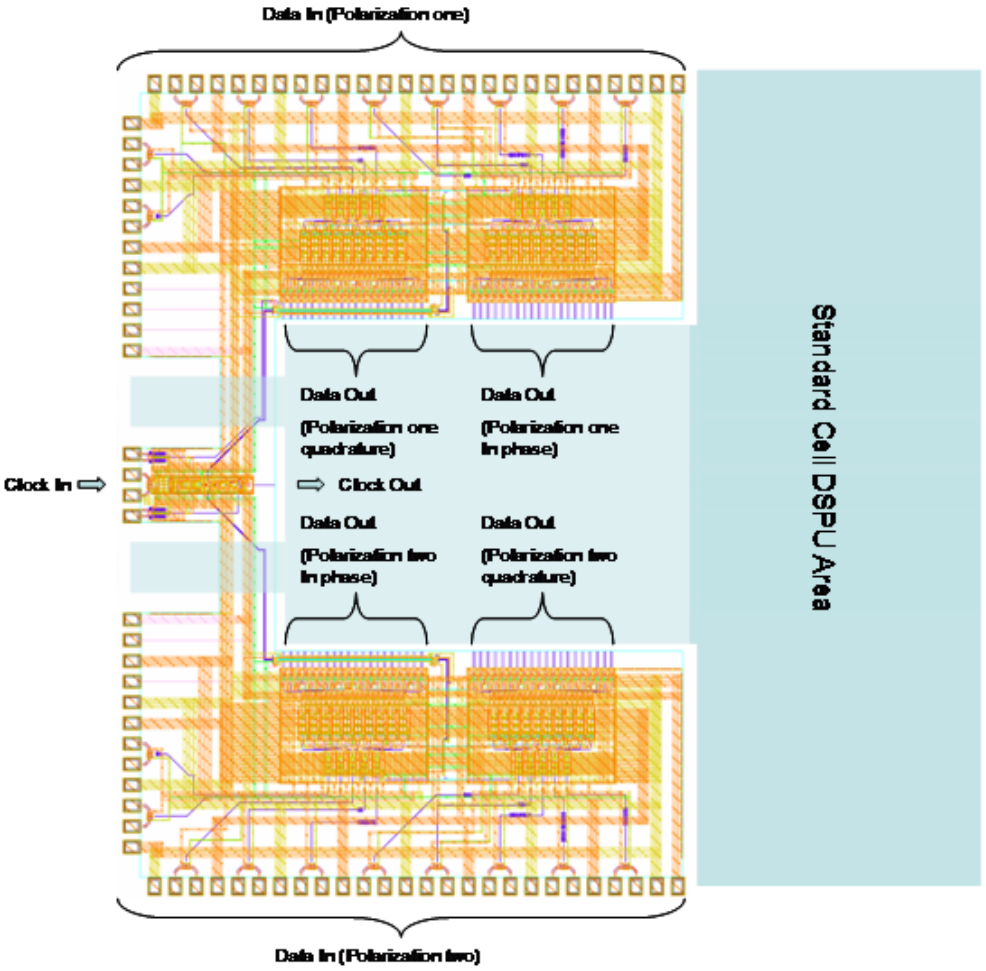



**Figure 3.40:** Layout of the 5 bit (5X4 channel) 1:8 DEMUX

The exact positions of all blocks and pins of CMOS chip version B were defined during the creation of the floorplan for the mixed design. Therefore, both designs could be finished individually with all block and pin positions specified. Routing and placement obstructions in both layouts prevented shorts between both layouts. Therefore, manual adaptations during the layout integration step were reduced to a minimum.

Figure 3.41 shows the full layout of the CMOS chip version B and the die photograph. This layout consists of interface (10 Gbit/s 20 channel 1:8 DEMUX) and the DSPU. The die size is 4 mm×4 mm.

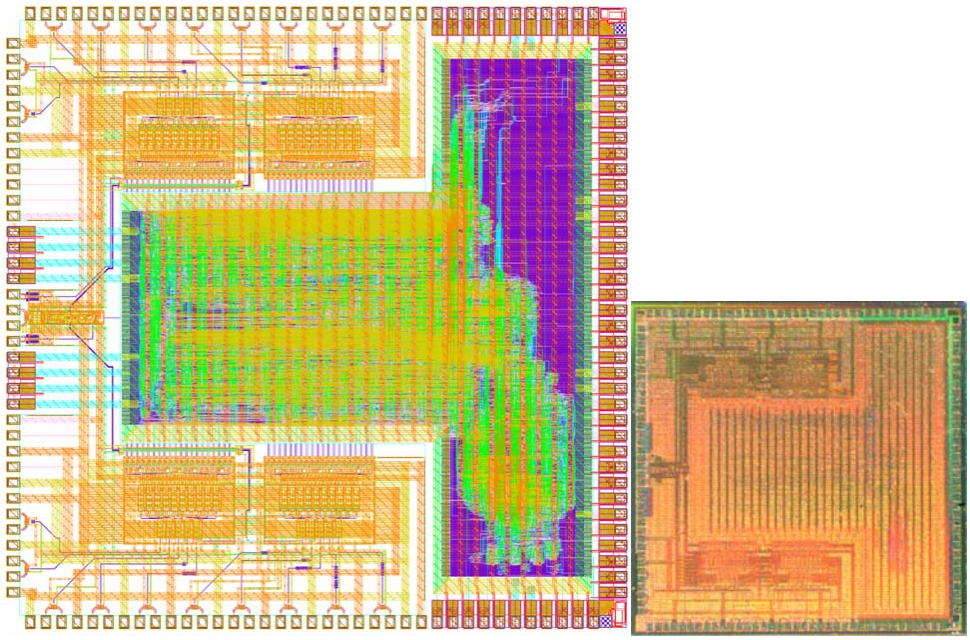


**Figure 3.41:** Final layout of the combined full-custom and standard cell based design (CMOS chip version B) (left) and the die photograph (right)

Figure 3.42 shows the ceramic prototype board of the synchronous QPSK with the polarization multiplex receiver which includes four A/D converter chips and the CMOS chip version B. The board is 8.5cm×6cm in size.

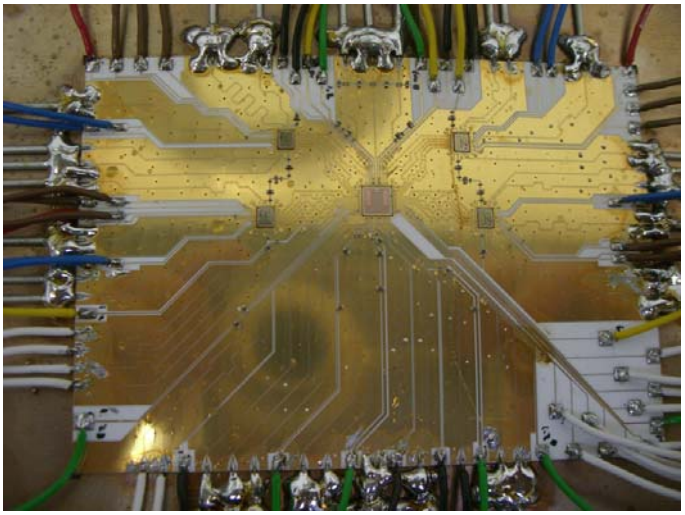


**Figure 3.42:** Ceramic prototype board used for the CMOS chip version B

### 3.6.3. Simulation and Test Results

Simulations were done with a pseudo-random bit sequence (PRBS length $2^7$-1 bits) input data stream and a sinusoidal clock input signal. All input signals have a nominal peak-to-peak amplitude of 400 mV. All the input data channels were give identical PRBS patterns. The parasitic capacitances are automatically extracted from the layout of the circuit in the simulation.

With parasitic elements included the DEMUX works properly up to about 11 Gbit/s input data rate in the simulation. But there were further performance degradations in the real chip because of the variations in the fabrication process and the effects of chip mounting. As this design is more optimized with respect to the layout than chip version A, the performance is better than that in the chip version A. The proper operation of SCFL to CMOS interface was also verified by checking input and output signals.

The current consumption of the SCFL block is about 750 mA (1.8 V supply) in the testing. The peak current drawn by the CMOS block is about 140 mA (1.2 V supply) at 10 Gbit/s in the simulations. The average current drawn by 1.2 V supply is 68 mA. Total power consumption is about 1.5 W at the same data rate. This is equivalent to 72 mW of power per input data channel. All the simulations were conducted at a temperature of 75° C.

The clock frequency divider was tested using a single-ended AC-coupled signal generated by a synthesizer. The divide-by-four clock divider test output was connected to the oscilloscope. The input signal power was adjusted in order to get the proper test output. The testing showed that the divide-by-four clock divider operates between 0.1 GHz and 6.8 GHz input frequency that confers with the DEMUX nominal operating range. Figure 3.43 (a) shows the 1:4 clock divider sensitivity characteristics. Figure 3.43 (b) shows the output clock signal corresponding to the 5 GHz input clock signal.

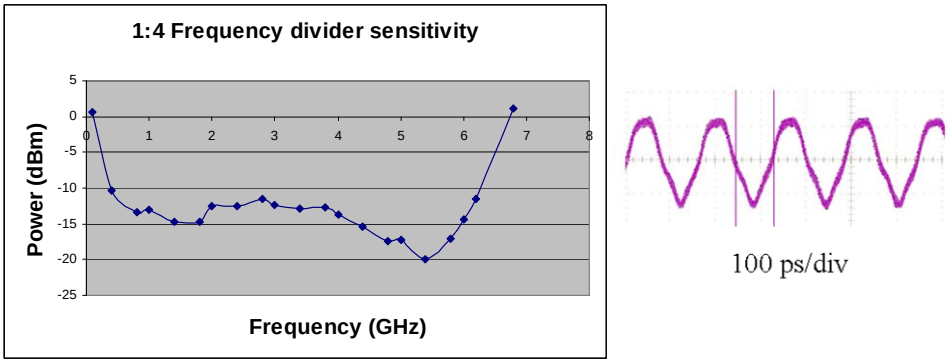



**Figure 3.43:** The divided by four frequency divider sensitivity (a) and the clock output signal correspond to the 5 GHz input clock signal (b)

The data inputs of the A/D converters were connected to the output signals generated by a 10 Gbit/s transmission system. The A/D converters generate half-rate clock output signals apart from the A/D converted data. The A/D half-rate clock output and the CMOS version A clock input were connected through an adjustable delay line to compensate any phase mismatch. The phase control switches (PC1 and PC2) were activated whenever necessary to achieve synchronization. The input data were generated using a $2^7$-1 pseudorandom bit

sequence. The DEMUX output test terminal was connected to an oscilloscope to check the eye diagram. The eye diagrams were observed with the CMOS logic standard cell module switched on and switched off. Figure 3.44 shows the output eye diagrams when the input data rate is 5 Gbit/s. It can be observed that with the CMOS DSPU switched on the eye diagrams become worse. The reason for this is the switching noise generated by the DSPU. The BER testing shows that at 5 Gbit/s BER is zero when the DSPU is switched off and the BER is $2X10^{-2}$ when the DSPU is switched on.

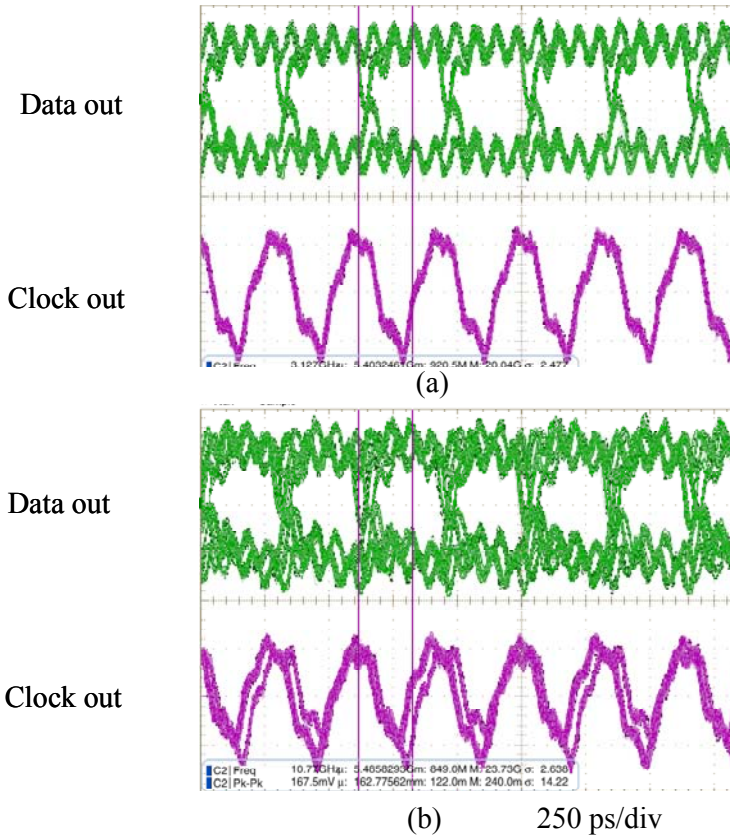



**Figure 3.44:** Output clock and data eye diagrams when input data rate is 5 Gbit/s with (a) CMOS DSPU switched off (b) CMOS DSPU switched on

The opening eye diagram is obtained at the output up to 9.5 Gbit/s input data rate when the DSPU was switched off. Figure 3.45 (a) and Figure 3.45 (b) show the output eye diagrams when the input data rate is 9.5 Gbit/s and 10 Gbit/s, respectively, with the DSPU switched off. It is evident that at 10 Gbit/s the output eye diagram closes due to phase noise.

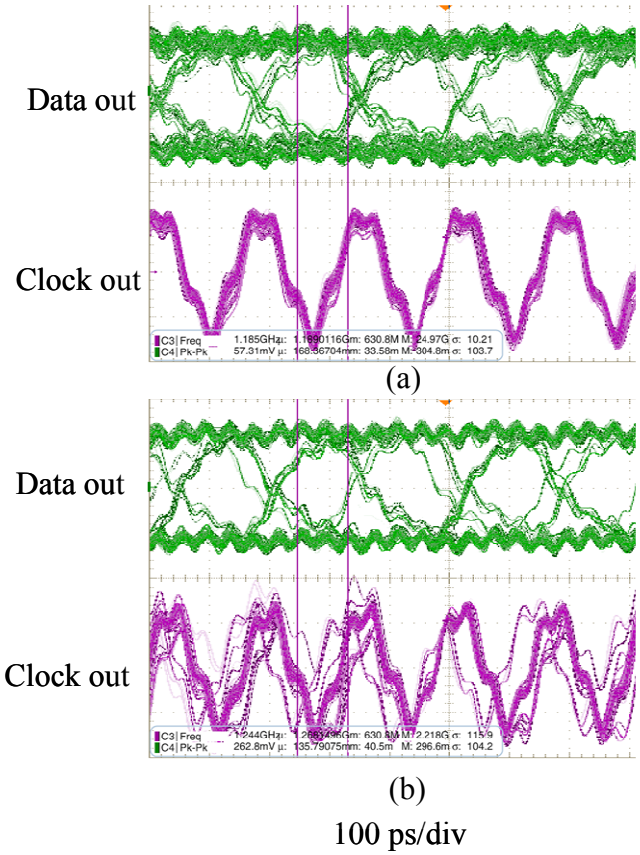



**Figure 3.45:** Output eye diagrams when the input data rate is (a) 9.5 Gbit/s and (b) 10 Gbit/s when CMOS DSPU switched off

## 3.7 Investigating Ultra High Speed Capabilities of the 130 nm CMOS Process

So far this thesis discussed the MOS IC design in the context of the synchronous QPSK receiver signal processing unit. The circuit components were not designed to extract speedwise the highest possible performance form the 130 nm CMOS technology because of the following reasons.

(1) The synchronous QPSK system was designed to operate at 40 Gbit/s. Therefore a single 1:8 DEMUX channel needed to operate only at 10 Gbit/s. The SCFL design did not need to be pushed to its speed limit to achieve the performance objective.

(2) In order to achieve ultrahigh-speed performance the transistor current should be increased several fold and as a result the power consumption also increases several fold. For a standalone circuit block such an increase in power consumption is not a difficult issue. But in the interface system where many circuit blocks are incorporated the increase in power consumption is a real challenge. The resulting

temperature increase of the chip while in operation could degrade the chip performance if the heat exchange system is not designed properly.

(3) The standard cell CMOS logic components which followed the DEMUX interface could operate only up to 1.25 Gbit/s. Therefore should the input data rate increase beyond 10 Gbit/s, 1:8 DEMUX would not be sufficient. Rather a 1:16 DEMUX could be necessary. That means an increase in circuit size and further increase in power consumption. Increase in the circuit size makes clock distribution even more difficult.

(4) In the large-scale synchronous circuit design the clock distribution is the most challenging task. Even if the standalone circuit blocks can function at ultrahigh speed the clock skew in the system limits the maximum achievable system speed. This fact is relevant to the CMOS chips version A and B. Therefore even when the component parts of the system operate at ultrahigh speed the whole system does not operate at ultrahigh speed due to the clock synchronization limit.

The next section discusses the simulations results of the effort to push the 130 nm CMOS technology to achieve speeds beyond 20 GHz.

### 3.7.1. Ultra High Speed Circuit Simulation Results

Several basic circuits used in previous designs were redesigned to achieve ultrahigh speed performance. These circuits include differential buffer, static frequency divider, and 1:2 DEMUX. As discussed earlier, SCFL achieve maximum possible speed performance from the CMOS technology. The transit frequency ( $f_T$ ) of a MOSFET can be expressed as

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}, \qquad \textbf{3.5}$$

where $g_m$ is the transconductance, $C_{gs}$ is the gate-source capacitance, and $C_{gd}$ is the gate drain capacitance [46, 74]. The transconductance ( $g_m$ ) can be expressed as

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \qquad \textbf{3.6}$$

where $\mu_n$ represent the mobility of the electrons, $C_{ox}$ is the gate oxide capacitance per unit length, *W* is the gate width, and *L* is the gate length [46, 74]. As *W* and *L* remains constant for a given transistor (technology). Transconductance ( $g_m$ ) is proportional to the square root of the drain current ( $I_D$ ). Consequently $f_T$ also increases accordingly. As a result the bandwidth of the differential amplifier also increases although the bandwidth is not a strong function of $f_T$ . Therefore increasing the drain current is one way of increasing the bandwidth. With larger currents larger resistors are necessary to carry the current. As a result the system capacitance increases. This limits the maximum achievable bandwidth of the system. A less

conservative resistor sizing eases this problem. Figure 3.46 shows the frequency response of a differential buffer similar to the one shown in the Figure 3.22. The transistor width is 10µm. The load resistor is 340 Ω and the source current is 2.5 mA. The current per contact was assumed 0.6 mA, which was close to the maximum current per contact. In the earlier designs the current per contact was assumed conservative 0.2 mA. The gain of this buffer is 3.2 dB and the 3 dB bandwidth is 29 GHz.

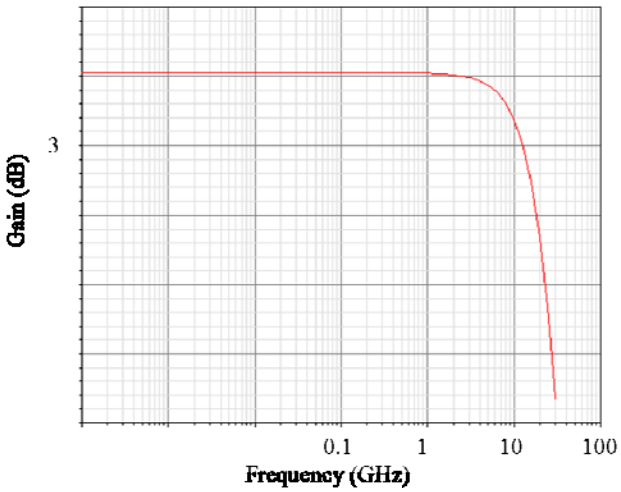



**Figure 3.46:** Frequency response of the differential buffer when drain current is 2.5 mA

Figure 3.47 shows the sensitivity curve of the static frequency divider module designed to carry 2.5 mA drain current in the ON state. As seen from the graph the static frequency divider operates up to 21.7 GHz. The minimum sensitivity is achieved around 15 GHz input frequency.

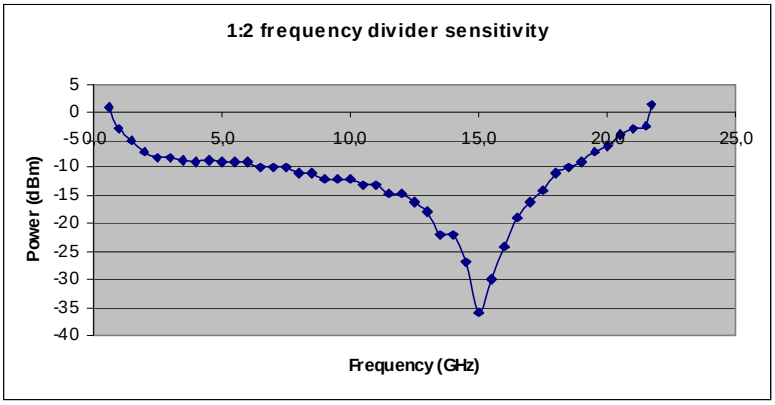
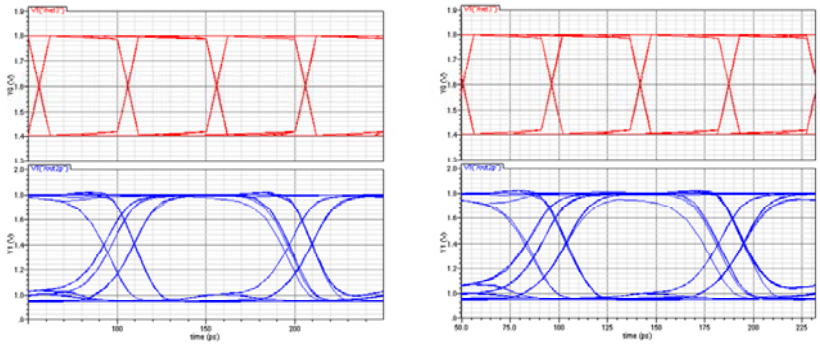



**Figure 3.47:** Sensitivity curve of the ultrahigh-speed static frequency divider

A 1:2 DEMUX similar to the one shown in the Figure 3.18 was simulated. The latch current was 2.5 mA. So at the ON state a load resistor carries 2.5 mA of current. Active current sources were used to generate source current. The Figure 3.48 shows the input and output eye diagrams when the input data rate of the DEMUX is 20 Gbit/s (left) and 22 Gbit/s (right). The input was a $2^7$-1 pseudorandom signal. As it is evident from the eye diagrams an error free transmission is possible up to 22 Gbit/s input data rate. In par with the earlier prediction it is evident that the power consumed by ultra high speed blocks will be several fold higher than the power consumption of the SCFL blocks in the CMOS versions A and B.



10 ps/div 5 ps/div

**Figure 3.48:** Input and output eye diagrams of the 1:2 DEMUX when the input data rate is 20 Gbit/s (left) and 22 Gbit/s (right)

Figure 3.49 shows the frequency response of a differential buffer similar to the one shown in the Figure 3.22. The transistor width is 20µm. The load resistor is 180 Ω and the source current is 4 mA. The current per contact was assumed 0.6 mA. The gain of this buffer is 3.2 dB and the 3 dB bandwidth is 33.5 GHz.

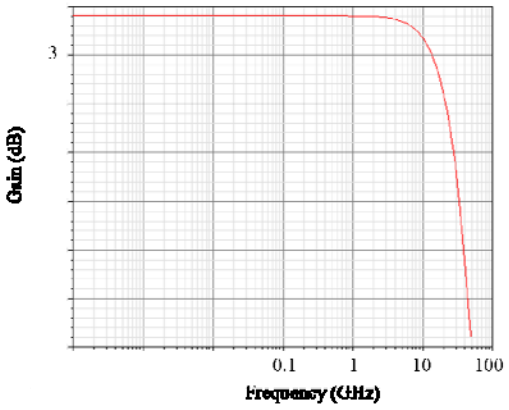



**Figure 3.49:** Frequency response of the differential buffer when drain current is 4 mA

Figure 3.50 shows the sensitivity curve of the static frequency divider module designed to carry 4 mA drain current in the ON state. As seen from the graph the static frequency divider operates up to 24.4 GHz. The minimum sensitivity is achieved around 17 GHz input frequency.

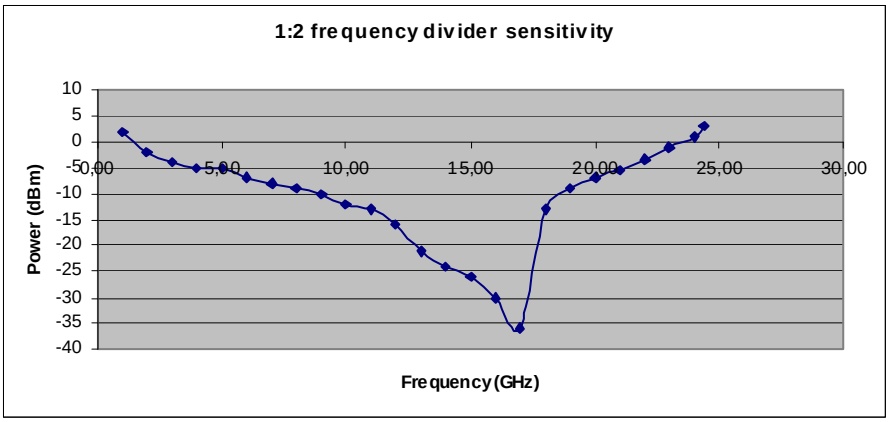
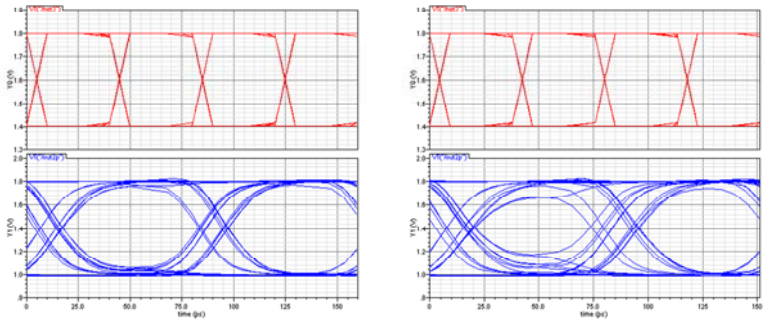



**Figure 3.50:** Sensitivity curve of the ultrahigh-speed static frequency divider

A 1:2 DEMUX similar to the one shown in the Figure 3.18 was simulated. The latch current was 4 mA. So at the ON state a load resistor carries 4 mA of current. Active current sources were used to generate source current. Figure 3.51 shows the input and output eye diagrams when the input data rate of the DEMUX is 25 Gbit/s (left) and 26.5 Gbit/s (right). The input was a $2^7$-1 pseudorandom signal. As it is evident from the eye diagrams an error-free transmission is possible up to 26.5 Gbit/s input data rate.



5 ps/div

**Figure 3.51:** Input and output eye diagrams of the 1:2 DEMUX when the input data rate is 25 Gbit/s (left) and 26.5 Gbit/s (right)

It is a interesting exercise to predict the performance of 90 nm and 65 nm CMOS processes using the experience obtained from 130 nm CMOS process. An alternative expression for the $g_m$ can be written as

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}), \quad \textbf{3.7}$$

where $V_{GS} - V_{TH}$ is the overdrive voltage [46, 74]. As can be seen from previous equation

$$g_m \propto \frac{1}{L}. \quad \textbf{3.8}$$

But the threshold voltage ($V_{TH}$) does not scale at the similar rate as gate length. Therefore overdrive capability reduces with the reduction of gate length. So $g_m$ does not increase at the same rate as expected. Furthermore $C_{gs}$ changes proportional to the gate length. The supply voltage ($V_{DD}$) also scales down. The ratio between gate length (L) of the 90 nm technology and 130 nm technology is 1.44 [75]. The $V_{DD}$ is reduced to 1.2 V from 1.8 V in the 130 nm technology. Therefore the ideal achievable speed in the 90 nm technology is 2 times that of 130 nm. Therefore 90 nm could achieve beyond 40 Gbit/s speeds with 1:2 DEMUX in the ideal case [76]. Furthermore with the reduced feature size leakage current also increases. The low supply voltage makes the voltage allotment of the stacked SCFL topology critical because threshold voltage ($V_{TH}$) does not scale down at the same rate as supply voltage. For the 65 nm technology assuming $V_{DD}$ = 1 V the system speed can ideally increase by 4 times or beyond 80 Gbit/s.

# Chapter 4

# Modeling Clock Skew in the Presence of Random Process Variations and Non-Uniform Substrate Temperature

## 4.1 Introduction

In Chapter three the importance of having a symmetric clock distribution network in a synchronous system was discussed. In a synchronous system, the clock edges should reach all the blocks that are synchronous at the same time. Normally these blocks are spread across the die area. The most common way of achieving clock synchronization is to design the clock distribution network with a tree architecture. In the tree architecture, all interconnects connected to a single branch point are designed to have identical length. Meandering of lines is used when necessary. In order to maintain clock signal strength, intermediate buffers are used in all branch points and in long interconnects. All end-to-end paths must have same number of intermediate buffers. Balanced H-tree clock distribution networks have a binary tree architecture and are commonly used to reduce clock skew (Figure 4.1). The clock period of a clock distribution network is generally determined by both the clock skew and the maximal clock delay of the network. Even if careful consideration is given to the design of clock distribution networks so that all to signal paths are identical, the fabrication process introduces random variations to the interconnect parameters. These random variations normally take a normal distribution. As a result even a most carefully designed clock distribution will have a clock skew.

The rapid growth of the size and the speed of ultra large scale integrated (ULSI) circuits makes clock distribution a vital issue. The advanced Intel and AMD processors now work above 2 GHz. At such high speeds clock skew becomes a very significant problem. Clock skew arises mainly from unequal clock path lengths to various modules, process variations, and non uniform temperature profile in the substrate [77-79]. To model the clock skew either a worst case or a statistical approach may be used. A worst-case approach causes an unnecessarily long clock period. In a statistical approach the clock parameters may be chosen so that the probability of timing failure is very small. This usually results in a shorter clock period. The available literature deals separately with the statistical clock skew modeling in the presence of process variations [77, 81] and the clock skew in the presence of non-uniform thermal profile in the chip [80, 82]. However, the effect of both phenomena simultaneously on clock skew has not been investigated. The earlier assumption that the temperature profile is uniform in the substrate is generally invalid and becoming increasingly inaccurate for nanometer-scale high-performance integrated circuits (ICs), where large temperature gradients can occur in the substrate. In fact it has been recently reported that the thermal gradients as large as 50°C can exist across high-performance microprocessor substrates [83].

Based on the cell-level power consumption map of the substrate, researchers have proposed efficient techniques to obtain the temperature profile of the substrate surface [84].

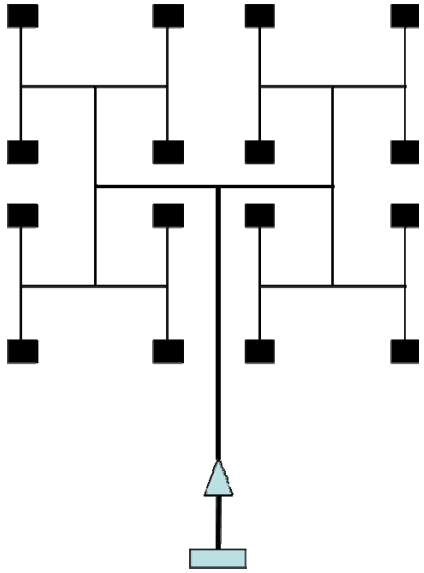


**Figure 4.1:** A balanced H-tree clock distribution network with 16 processors

This chapter focuses on providing a recursive approach for estimating the expected value of the clock skew of a balanced H-tree clock distribution network (CDN). The effect of the change in the signal propagation delay due to non-uniform temperature profile on the clock skew is included in this estimate. In a balanced H-tree CDN clock paths are identical. CDNs are designed as balanced H-trees in order to reduce clock skew. It should be noted that with increase in number of processors, resistance and capacitance between clock source and sink increase.

The rest of the chapter is organized as follows: First, a general skew model for clock distribution networks is described. Then, the Elmore delay model for the interconnect delay is described. Next a new clock skew estimation method which is the essence of this work is introduced. Finally, simulation results are given and compared with calculated results.

## 4.2 Clock Skew Modeling

Due to variations in process parameters and non-uniform temperature profile, the actual circuit delay will deviate from the designed value. For a given CDN let $t(l_o, l_i)$ denote the signal propagation time on the unique path from the clock source $l_o$ to the sink $l_i$. The maximal clock delay $\xi$ and the minimal clock delay $\eta$ of the CDN can be defined as [77]

$$\xi = \max_i \{t(l_o, l_i)\}, \quad \textbf{4.1}$$

$$\eta = \min_i \{t(l_o, l_i)\}. \quad \textbf{4.2}$$

The clock skew $\chi$ of the CDN is in general defined as

$$\chi = \max_{i \neq j} |t(l_o, l_i) - t(l_o, l_j)| = \xi - \eta. \quad \textbf{4.3}$$

When the random process variations are considered, variations of path delay are modeled by normal distributions. To model the clock skew $\chi$, random variables $\xi$ and $\eta$ should be first characterized. The model developed in this paper is based on following assumptions.

*Assumption 1*

A CDN in general can be represented by a binary tree, we assume that both the maximal clock delay and the minimal clock delay in each sub-tree (and also whole binary tree) of the CDN can be modeled by normal distributions when process variations are considered.

*Assumption II*

The delay along a clock path is the sum of the uncertain independent delays of the branches along the given path. Correlation between the delays of any two paths is determined only by the overlapping parts of their length.

*Assumption III*

The delay introduced by the elevated temperature with reference to the ambient temperature to each interconnect in the CDN simply shifts the delay distribution curve of each interconnect to a higher value by an amount equal to the additional time delay incurred due to elevated temperature.

Consider an interconnect with length $L$ and uniform width $w$ that is driven by a driver with on-resistance $R_d$ and junction capacitance $C_p$ terminated by a load with capacitance $C_L$ as depicted in Figure 4.2. The line is partitioned into $n$ equal segments, each with length $\Delta x$. By using the distributed *RC* Elmore delay model, the delay of signal propagation through the line *d* can be written as

$$d = R_d \left\{ \sum_{i=1}^{n} c_0(x_i)\Delta x + C_L \right\} + \sum_{i=1}^{n} r_0(x)\Delta x \left\{ \sum_{j=i}^{n} c_0(x_j)\Delta x + C_L \right\}, \quad \textbf{4.4}$$

where $c_o(x)$ and $r_o(x)$ are the capacitance per unit length and resistance per unit length at location *x*, respectively [80]. As the number of partitions approaches infinity, we can rewrite Elmore delay as

$$d = R_d\left\{\int_0^L c_0(x)dx + C_L\right\} + \int_0^L r_0(x)\left\{\int_x^L c_0(\tau)d\tau + C_L\right\}dx. \qquad \textbf{4.5}$$

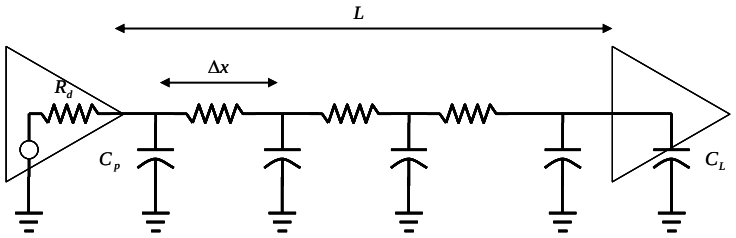



**Figure 4.2:** Distributed RC interconnect line model

It is assumed that the capacitance per unit length does not change with the temperature variation along the interconnect length. It is also assumed that the temperature distribution inside the driver is uniform under the steady-state condition. Hence, $R_d$ is constant at a chosen operating temperature of a cell. The electrical resistance of the interconnect line $R_E$ has a linear relationship with its temperature and can be written as $R_E(x) = R_0(1 + \beta T(x))$ where $R_0$ is the resistance per unit length at a reference temperature, $\beta$ is the temperature coefficient of the resistance (1/°C), and $T(x)$ is the temperature profile along the length of the interconnect line [80]. The interconnect delay (*d*) when there is nonuniform temperature profile along the interconnect is

$$d = d_o + (c_o L + C_L)\rho_o\beta\int_0^L T(x)dx - c_o\rho_o\beta\int_0^L x\cdot T(x)dx \qquad \textbf{4.6}$$

where $d_o = R_d(C_L + c_o L) + \left(c_o\rho_o\frac{L^2}{2} + \rho_o L C_L\right)$.

$\rho_0$ is the electrical resistively at the reference temperature, $d_o$ is the Elmore delay of the interconnect corresponding to the unit length resistance at reference temperature [79].
The interconnect delay can also be expressed as

$$d = d_o + d^T \qquad \textbf{4.7}$$

where $d^T$ is the additional delay due to the elevated temperature.

For the $N$ hierarchical-level, balanced H-tree, let $\xi_i$ be the maximal clock delay and $\eta_i$ be the minimal clock delay of the sub H-tree starting from the level $i$ split point (Figure 4.3). Then we have [77]

$$\xi_i = \max\left\{\left(d_{i+1,1}+\zeta_{i+1,1}\right),\left(d_{i+1,2}+\zeta_{i+1,2}\right)\right\},$$

$$\xi_i = \frac{\left\{\left(d_{i+1,1}+\xi_{i+1,1}\right)+\left(d_{i+1,2}+\xi_{i+1,2}\right)+\left|\left(d_{i+1,1}+\xi_{i+1,1}\right)-\left(d_{i+1,2}+\xi_{i+1,2}\right)\right|\right\}}{2},$$

$$\eta_i = \min\left\{\left(d_{i+1,1}+\zeta_{i+1,1}\right),\left(d_{i+1,2}+\zeta_{i+1,2}\right)\right\},$$

$$\eta_i = \frac{\left\{\left(d_{i+1,1}+\eta_{i+1,1}\right)+\left(d_{i+1,2}+\eta_{i+1,2}\right)-\left|\left(d_{i+1,1}+\eta_{i+1,1}\right)-\left(d_{i+1,2}+\eta_{i+1,2}\right)\right|\right\}}{2}, \qquad \textbf{4.8}$$

where $d_{i+1,1}$ and $d_{i+1,2}$ are independent samples of $d_{i+1}$ (interconnect delay), $\xi_{i+1,1}$ and $\xi_{i+1,2}$ are independent samples of $\xi_{i+1}$, $\eta_{i+1,1}$ and $\eta_{i+1,2}$ are independent samples of $\eta_{i+1}$.

The interconnect delay ($d_{i+1}$) can be expanded as $d_{i+1} = d_{i+1}^{o} + d_{i+1}^{T}$ where $d_{i+1}^{o}$ is the delay at reference temperature and $d_{i+1}^{T}$ is the additional delay due to elevated temperature.

Let $R_1$ and $R_2$ be two independent normal random variables, and let $R = R_1 - R_2$. Then $R$ is also a normal random variable with mean $\mu$ and standard deviation $\delta$ given by [77]

$$\mu = E(R) = E(R_1) - E(R_2),$$
$$\delta = \sqrt{D(R)} = \sqrt{D(R_1) + D(R_2)}. \qquad \textbf{4.9}$$

$E(\cdot)$ and $D(\cdot)$ are mean value and variance of a random variable.

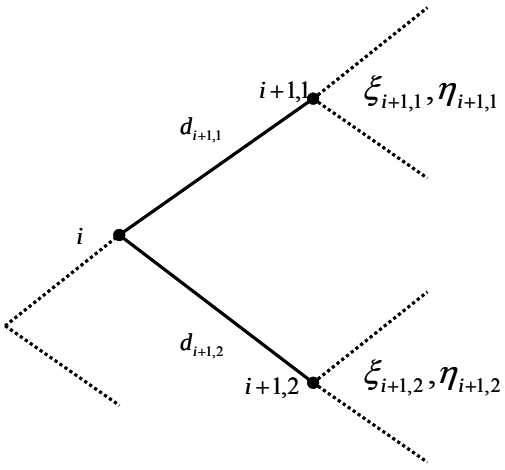



**Figure 4.3:** Illustration binary clock tree (sub H-tree)

The distribution function $F_{|R|}(x)$ of $|R|$ can be determined as

$$F_{|R|}(x) = P(|R| < x) = \frac{1}{\sqrt{2\pi}\delta}\int_{-x}^{x} e^{-\frac{1}{2}\left[\frac{t-\mu}{\delta}\right]^2} dt,$$

$x > 0$.

Therefore the density function $f_{|R|}(x)$ of $|R|$ is

$$f_{|R|}(x) = \frac{1}{\sqrt{2\pi}\delta}\left\{e^{-\frac{1}{2}\left[\frac{x-\mu}{\delta}\right]^2} + e^{-\frac{1}{2}\left[\frac{x+\mu}{\delta}\right]^2}\right\},$$

$x > 0$.

The mean value $E(|R|)$ of $|R|$ is given by

$$E(|R|) = \int_0^\infty x \cdot f_{|R|}(x)dx,$$

$$= \frac{1}{\sqrt{2\pi}\delta}\int_0^\infty x\left\{e^{-\frac{1}{2}\left[\frac{x-\mu}{\delta}\right]^2} + e^{-\frac{1}{2}\left[\frac{x+\mu}{\delta}\right]^2}\right\}dx.$$

By making substitutions, $t_1 = \frac{x-\mu}{\delta}$ and $t_2 = \frac{x+\mu}{\delta}$, the mean value can be expressed as

$$E(|R|) = \frac{1}{\sqrt{2\pi}}\left\{\int_{-\frac{\mu}{\delta}}^{\infty}(\delta t_1 + \mu)e^{-\frac{1}{2}t_1^2}dt_1 + \int_{\frac{\mu}{\delta}}^{\infty}(\delta t_2 - \mu)e^{-\frac{1}{2}t_2^2}dt_2\right\},$$

$$= \underbrace{\frac{\delta}{\sqrt{2\pi}}\left\{\int_{-\frac{\mu}{\delta}}^{\infty} t_1 e^{-\frac{1}{2}t_1^2}dt_1 + \int_{\frac{\mu}{\delta}}^{\infty} t_2 e^{-\frac{1}{2}t_{12}^2}dt_2\right\}}_{A} + \underbrace{\frac{1}{\sqrt{2\pi}}\left\{\int_{-\frac{\mu}{\delta}}^{\infty}\mu e^{-\frac{1}{2}t_1^2}dt_1 - \int_{\frac{\mu}{\delta}}^{\infty}\mu e^{-\frac{1}{2}t_2^2}dt_2\right\}}_{B}.$$

Now it is possible to evaluate *A* and *B* separately.

$$B = \frac{1}{\sqrt{2\pi}}\left\{\int_{\frac{-\mu}{\delta}}^{0}\mu e^{-\frac{1}{2}t_1^2}dt_1 + \int_0^{\frac{\mu}{\delta}}\mu e^{-\frac{1}{2}t_2^2}dt_2\right\}.$$

By using the even symmetry of the function, $e^{-\frac{1}{2}t^2}$

$$B = \frac{2|\mu|}{\sqrt{2\pi}} \int_0^{\frac{|\mu|}{\delta}} e^{-\frac{1}{2}t^2}\, dt .$$

$$A = \frac{\delta}{\sqrt{2\pi}} \left\{ 2 + \int_{\frac{-\mu}{\delta}}^{0} t_1 e^{-\frac{1}{2}t_1^2}\, dt_1 - \int_0^{\frac{\mu}{\delta}} t_2 e^{-\frac{1}{2}t_2^2}\, dt_2 \right\}.$$

By using the odd symmetry of the function, $te^{-\frac{1}{2}t^2}$

$$A = \frac{2\delta}{\sqrt{2\pi}} e^{-\frac{1}{2}\left[\frac{\mu}{\delta}\right]^2} .$$

Therefore, $E(|R|) = \frac{2\delta}{\sqrt{2\pi}} e^{-\frac{1}{2}\left[\frac{\mu}{\delta}\right]^2} + \frac{2|\mu|}{\sqrt{2\pi}} \int_0^{\frac{|\mu|}{\delta}} e^{-\frac{1}{2}t^2}\, dt$ . **4.10**

$$D(|R|) = \int_0^{\infty} [x - E(|R|)]^2 f_{|R|}(x) dx,$$
$$= \int_0^{\infty} x^2 f_{|R|}(x) - 2\int_0^{\infty} xE(|R|) f_{|R|}(x) dx + \int_0^{\infty} (E(|R|))^2 f_{|R|}(x) dx,$$
$$= \int_0^{\infty} x^2 f_{|R|}(x) dx - [E(|R|)]^2 ,$$

$$D(|R|) = \mu^2 + \delta^2 - [E(R)]^2 . \quad \textbf{4.11}$$

If $\mu = 0$ then, $E(|R|) = \frac{2\delta}{\sqrt{2\pi}}$, and $D(|R|) = \delta^2\left(1 - \frac{1}{\pi}\right)$. Using the variables in the 4.8, $R_1$ and $R_2$ can be defined as, $R_1 = d_{i+1,1} + \xi_{i+1,1}$, $R_2 = d_{i+1,2} + \xi_{i+1,2}$. By separating the delay at the reference temperature and the additional delay due to elevated temperature

$$R_1 = d_{i+1,1}^0 + d_{i+1,1}^T + \xi_{i+1,1} ,$$
$$R_2 = d_{i+1,2}^0 + d_{i+1,2}^T + \xi_{i+1,2} , \quad \textbf{4.12}$$

the expression of μ can be expanded as

$$\mu = E(R) = E(R_1) - E(R_2),$$
$$\mu = E(d_{i+1,1}^0) + E(d_{i+1,1}^T) + E(\xi_{i+1,1}) - E(d_{i+1,2}^0) - E(d_{i+1,2}^T) - E(\xi_{i+1,2}). \quad \textbf{4.13}$$

In a balanced H-tree $E(d_{i+1,1}^0) = E(d_{i+1,2}^0)$ and $E(\xi_{i+1.1}) = E(\xi_{i+1.2})$. The interconnect delay

induced by the elevated temperature is a constant for a given interconnect and therefore $E\left(d_{i+1,1}^{T}\right)=d_{i+1,1}^{T}, E\left(d_{i+1,2}^{T}\right)=d_{i+1,2}^{T}$.

When $\Delta d_{i+1}^{T}=d_{i+1,1}^{T}-d_{i+1,2}^{T}$ the mean $\mu=\Delta d_{i+1}^{T}$. **4.14**

By substituting above results the expression for $E\left(\left|R\right|\right)$ gives

$$E\left(\left|R\right|\right)=\frac{2\delta}{\sqrt{2\pi}}e^{-\frac{1}{2}\left[\frac{\Delta d_{i+1}^{T}}{\delta}\right]^{2}}+\frac{2\left|\Delta d_{i+1}^{T}\right|}{\sqrt{2\pi}}\int_{0}^{\frac{|\mu|}{\delta}}e^{-\frac{1}{2}t^{2}}\,dt\,. \qquad \textbf{4.15}$$

For a comparatively small $x$ [85]

$$e^{-x}=1-x+\frac{x^{2}}{2!}-\frac{x^{3}}{3!}+\ldots\approx 1-x+\frac{x^{2}}{2!}-\frac{x^{3}}{3!},$$

$$\int_{a}^{b}e^{-x^{2}}dx=\left[x-\frac{x^{3}}{3}+\frac{x^{5}}{2!5}-\ldots\right]_{a}^{b}\approx\left[x-\frac{x^{3}}{3}+\frac{x^{5}}{2!5}\right]_{a}^{b}. \qquad \textbf{4.16}$$

Let $x=\frac{1}{\sqrt{2}}t$ then $E\left(\left|R\right|\right)$ can be expressed as

$$E\left(\left|R\right|\right)\approx\frac{2\delta}{\sqrt{2\pi}}\left\{1-\frac{1}{2}\left(\frac{\Delta d_{i+1}^{T}}{\delta}\right)^{2}+\frac{1}{8}\left(\frac{\Delta d_{i+1}^{T}}{\delta}\right)^{4}-\frac{1}{48}\left(\frac{\Delta d_{i+1}^{T}}{\delta}\right)^{6}\right\}$$
$$+\frac{2\sqrt{2}\left|\Delta d_{i+1}^{T}\right|}{\sqrt{2\pi}}\left[x-\frac{x^{3}}{3}+\frac{x^{5}}{2!5}\right]_{0}^{\frac{1}{\sqrt{2}}\frac{\left|\Delta d_{i+1}^{T}\right|}{\delta}}, \qquad \textbf{4.17}$$

$$E\left(\left|R\right|\right)\approx\frac{2\delta}{\sqrt{2\pi}}-\frac{2\delta}{\sqrt{2\pi}}\frac{1}{2}\left(\frac{\Delta d_{i+1}^{T}}{\delta}\right)^{2}+\frac{2\delta}{\sqrt{2\pi}}\frac{1}{8}\left(\frac{\Delta d_{i+1}^{T}}{\delta}\right)^{4}-\frac{2\delta}{\sqrt{2\pi}}\frac{1}{48}\left(\frac{\Delta d_{i+1}^{T}}{\delta}\right)^{6}$$
$$+\frac{2\left|\Delta d_{i+1}^{T}\right|^{2}}{\sqrt{2\pi}\delta}-\frac{2\left|\Delta d_{i+1}^{T}\right|^{4}}{6\sqrt{2\pi}\delta^{3}}+\frac{2\left|\Delta d_{i+1}^{T}\right|^{6}}{40\sqrt{2\pi}\delta^{5}}, \qquad \textbf{4.18}$$

$$E\left(\left|R\right|\right)=\frac{2\delta}{\sqrt{2\pi}}+\frac{1}{\sqrt{2\pi}}\frac{\left(\Delta d_{i+1}^{T}\right)^{2}}{\delta}-\frac{1}{\sqrt{2\pi}}(0.083)\frac{\left(\Delta d_{i+1}^{T}\right)^{4}}{\delta^{3}}+\frac{1}{\sqrt{2\pi}}(0.0083)\frac{\left(\Delta d_{i+1}^{T}\right)^{6}}{\delta^{5}}. \qquad \textbf{4.19}$$

Let $\delta=\sqrt{2}\sqrt{D\left(d_{i+1}^{o}\right)+D\left(\xi_{i+1}\right)}=\sqrt{2}\Phi_{i+1}$.

From 4.8, 4.12, 4.13, and 4.19 it can be deduced that

$$E(\xi_i) = E\left(d_{i+1}^{o}\right) + E(\xi_{i+1}) + E\left(d_{i+1}^{T}\right) + \frac{1}{\sqrt{\pi}}\left\{\begin{array}{l}\Phi_{i+1} + 0.25\dfrac{\left(\Delta d_{i+1}^{T}\right)^2}{\Phi_{i+1}} - 0.0104\dfrac{\left(\Delta d_{i+1}^{T}\right)^4}{\Phi_{i+1}^{\ 3}} \\ + 0.00052\dfrac{\left(\Delta d_{i+1}^{T}\right)^6}{\Phi_{i+1}^{\ 5}}\end{array}\right\}, \qquad \textbf{4.20}$$

$$E(\xi_i) = E\left(d_{i+1}^{o}\right) + E(\xi_{i+1}) + \frac{\sum_{j=1}^{2} d_{i+1,j}^{T}}{2} + \frac{1}{\sqrt{\pi}}\left\{\begin{array}{l}\Phi_{i+1} + 0.25\dfrac{\left(\Delta d_{i+1}^{T}\right)^2}{\Phi_{i+1}} - 0.0104\dfrac{\left(\Delta d_{i+1}^{T}\right)^4}{\Phi_{i+1}^{\ 3}} \\ + 0.00052\dfrac{\left(\Delta d_{i+1}^{T}\right)^6}{\Phi_{i+1}^{\ 5}}\end{array}\right\}. \qquad \textbf{4.21}$$

Because elevated temperature only moves the delay distribution curve upwards increasing the mean value, the variance remains unchanged and $D(d_{i+1}) = D\left(d_{i+1}^{o}\right)$.

Let $\sqrt{D\left(d_{i+1}^{o}\right) + D(\eta_{i+1})} = \Psi_{i+1}$ then by a similar approach to the equation 4.21 $E(\eta_i)$ can be expressed as

$$E(\eta_i) = E\left(d_{i+1}^{0}\right) + E(\eta_{i+1}) + \frac{\sum_{j=1}^{2} d_{i+1,j}^{T}}{2} - \frac{1}{\sqrt{\pi}}\left\{\begin{array}{l}\Psi_{i+1} + 0.25\dfrac{\left(\Delta d_{i+1}^{T}\right)^2}{\Psi_{i+1}} - 0.0104\dfrac{\left(\Delta d_{i+1}^{T}\right)^4}{\Psi_{i+1}^{\ 3}} \\ + 0.00052\dfrac{\left(\Delta d_{i+1}^{T}\right)^6}{\Psi_{i+1}^{\ 5}}\end{array}\right\}. \qquad \textbf{4.22}$$

The variance of $\xi_i$ and $\eta_i$ can be calculated recursively as follows [77]

$$D(\xi_i) = \frac{\pi - 1}{\pi}\left[D(d_{i+1}) + D(\xi_{i+1})\right], \qquad \textbf{4.23}$$

$$D(\eta_i) = \frac{\pi - 1}{\pi}\left[D(d_{i+1}) + D(\eta_{i+1})\right]. \qquad \textbf{4.24}$$

In a balanced H-tree clock distribution network (CDN) the initial conditions of the equations 4.23 and 4.24 are equal. Therefore from 4.23 and 4.24 it can be deduced that $D(\xi_i) = D(\eta_i)$ and as a result $\Phi_i = \Psi_i$. The expected value of the clock skew at the branch point *i* is expressed as follows

$$E(\chi_i) = E(\xi_i) - E(\eta_i),$$

$$E(\chi_i) = E(\xi_{i+1}) - E(\eta_{i+1}) + \underbrace{\frac{2}{\sqrt{\pi}}\left\{\begin{array}{l}\Phi_{i+1} + 0.25\dfrac{\left(\Delta d_{i+1}^{T}\right)^2}{\Phi_{i+1}} - 0.0104\dfrac{\left(\Delta d_{i+1}^{T}\right)^4}{\Phi_{i+1}^{\ 3}} \\ + 0.00052\dfrac{\left(\Delta d_{i+1}^{T}\right)^6}{\Phi_{i+1}^{\ 5}}\end{array}\right\}}_{\theta_{i+1}}, \qquad \textbf{4.25}$$

$$E(\chi_i) = E(\chi_{i+1}) + \theta_{i+1}. \quad \textbf{4.26}$$

Therefore according to 4.26 the expected value of the clock skew at the branch point *i* can be calculated recursively using the results of the branch point *i+1*. Using this result a recursive algorithm can be developed to calculate the clock skew of the whole CDN. The following section discusses such algorithm.

### 4.2.1. Uniform Temperature Profile

When the temperature throughout the die is constant $\Delta d_i^T = 0$ for all *i* and $\theta_i = \frac{2}{\sqrt{\pi}}\Phi_i$. The equation 4.26 can be recursively applied to the CDN and obtain the mean value of clock skew as seen by the root node

$$E(\chi_{N-1}) = \theta_N,$$
$$E(\chi_{N-2}) = E(\chi_{N-1}) + \theta_{N-1},$$
$$\vdots$$
$$E(\chi_o) = E(\chi_1) + \theta_1,$$

$$E(\chi_o) = \sum_{i=1}^{N} \theta_i. \quad \textbf{4.27}$$

### 4.2.2. Nonuniform Temperature Profile

When the temperature in the die is non-uniform it can be assumed that for some *i*, $\Delta d_i^T \neq 0$ and therefore $\theta_i$ takes the following form

$$\theta_i = \frac{2}{\sqrt{\pi}}\left\{\Phi_i + 0.25\frac{\left(\Delta d_1^T\right)^2}{\Phi_i} - 0.0104\frac{\left(\Delta d_i^T\right)^4}{\Phi_i^{\,3}} + 0.00052\frac{\left(\Delta d_i^T\right)^6}{\Phi_i^{\,5}}\right\} \quad \textbf{4.28}$$

For a balanced H-tree CDN all the branches in the level $i$ $(i = 1,.....N)$ are assumed to be statistically identical (i.e., both the mean value and the standard deviation of delay distribution are identical). It can be assumed that the delays imposed by non-uniform temperature profile moves the delay probability distribution function (pdf) forward by various quantities depending on the amount of increase in the temperature. This increases the mean delay of interconnects by various quantities, but the standard deviation of the delay remains the same. Therefore it is logical to assume, in the clock skew calculation, that the mean delay difference

between the branches at branch point $i$ ($\Delta d_i^T$) be the maximum delay difference between any two branches in the $i^{th}$ level due to non-uniform thermal profile.

## 4.3 Mean Skew Estimation Algorithm

In the calculation of the mean skew of an N-level balanced H-tree CDN it is assumed that each branch in the level $i$ has identical delay distribution characteristics. The delay increase in each branch from the base value due to the elevated temperature is not uniform because of the non-uniform thermal profile.

Define $\Delta d_i^T$ as the maximum delay difference between any two branches of the $i^{th}$ level due to non-uniform thermal profile.

The computational effort necessary to compute the mean skew of a balanced H-tree CDN using the above algorithm is $O(N)$ where $N$ is the number of levels.

***Algorithm***

**Initialization**

Let $i := N$

$\Phi_N = \sqrt{D(d_{sink})}$ where $d_{sink}$ is the delay at the last branch (sink branch).

**Step 1**

Calculate $\theta_N = f(\Phi_N, \Delta d_N^T)$ (4.28)

**Step 2**

$i := i-1$

Calculate $D(\xi_i)$ (4.23)

Calculate $\Phi_i$

Calculate $\theta_i = f(\Phi_i, \Delta d_i^T)$ (4.28)

**Repeat step 2 until** $i = 1$

The mean clock skew $E(\chi) = \sum_{i=1}^{N} \theta_i$

**End**

## 4.4 Results

Balanced H-tree clock distribution networks with $N$= 2, 3, 4, 5, and 6 were simulated for uniform and non-uniform temperature distributions in the die for different branch delay standard deviations ($\sqrt{D(d_i)} = 2.5,\ 5,\ 10$ ps). The mean skew values for both the cases (uniform and non-uniform temperature distribution) were calculated using the given algorithm. The maximum delay difference in the each level of the clock tree imposed by non-uniform temperature profile in the die is tabulated in the Table 4.1. It is assumed that all the branches in the CDN are statistically identical.

| Level ($i$) | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| $\Delta d_i^T$ (ps) | 0 | 4 | 6 | 7 | 7 | 7 |

**Table 4.1:** The maximum delay difference in each level of CDN (due to non-uniform temperature distribution)

The Figure 4.4 shows the simulation results when $\sqrt{D(d_i)} = 5\,\text{ps}$ and the number of processors vary form 1 to 64. The error with 64 processors and $\sqrt{D(d_i)} = 5\,\text{ps}$ is negligible as shown in Figure 4.4. For a smaller number of processors the error also becomes smaller. The mean clock skew values for different standard deviations and number of processors are compared in Figure 4.5. The comparison between theoretical and simulated results for different delay standard deviations can also made using Figure 4.5.

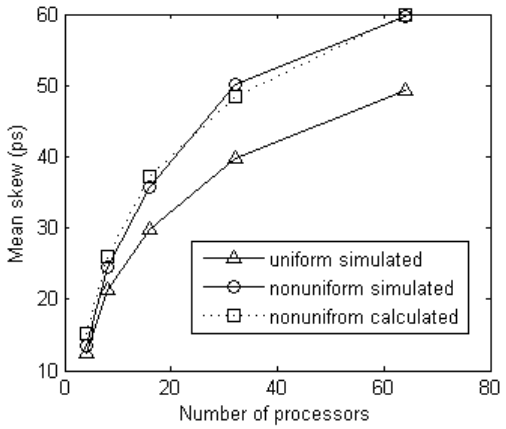



**Figure 4.4:** Comparison of mean skew vs. number of processors, using simulation and theoretical results with $\sqrt{D(d_i)} = 5$ ps

The comparison between calculated and simulated mean clock skew when the delay standard deviation of different levels are as given in the Table 4.2 is shown in the Figure 4.6.

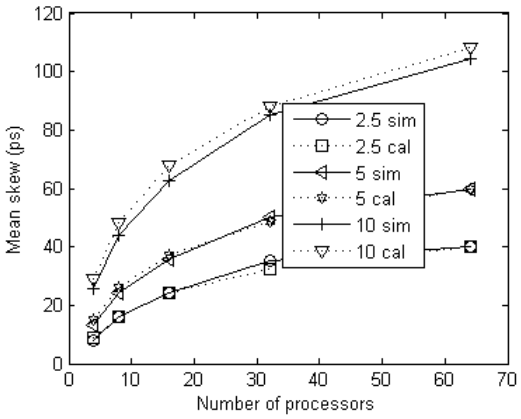



**Figure 4.5:** Comparison of mean skew vs. number of processors curves for simulation and theoretical results for $\sqrt{D(d_i)}$ = 2.5, 5, 10 ps

| Level ($i$) | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| $\sqrt{D(d_i)}$ (ps) | 5 | 4.5 | 4 | 3.5 | 3 | 2.5 |

**Table 4.2:** The delay standard deviation at different levels

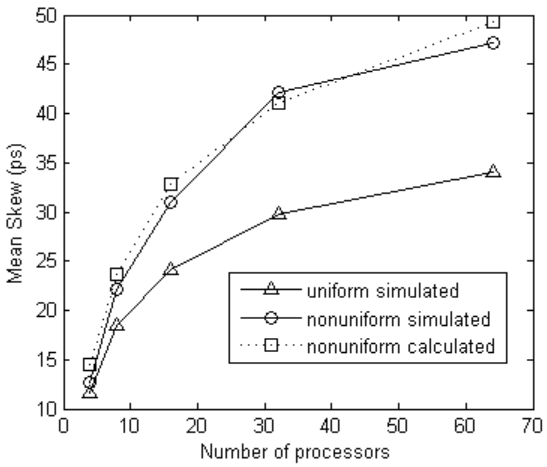



**Figure 4.6:** Comparison of mean skew vs. number of processors when different levels have different delay standard deviations

# Chapter 5

# Conclusions

The global internet traffic is predicted to increase dramatically on the back of the rise of user numbers in emerging markets and the increase of bandwidth-intensive applications like video sharing. Therefore the need for higher communication bandwidth is apparent as ever before. Optical data transmission systems form the backbone of the global telecommunication system. Therefore, in order to cope with increased bandwidth demand optical data transmission systems should increase their capacity. This can be achieved by either increasing the fiber density (i.e.: laying new fibers) or increasing the spectral efficiency of existing optical transmission systems. In order to increase the spectral efficiency a modulation format other than intensity modulation direct detection (IM/DD) should be used. Quadrature phase shift keying (QPSK) based multilevel modulation formats allow better performance and dispersion tolerance in upgraded or newly laid fiber links. The coherent optical polarization diversity receivers permit a fully electronic polarization control. The equalization of the polarization mode dispersion (PMD) and chromatic dispersion (CD) in the electronic domain is also possible with the coherent receivers.

Synchronous QPSK (synQPSK) transmission combined with the return-to-zero (RZ) coding and polarization division multiplex can upgrade existing 10 Gbit/s fiber links to 40 Gbit/s. Therefore this is an attractive modulation format for metropolitan area and long haul fiber data transmission. Because a synQPSK transmission system has a coherent receiver, all linear optical distortions can be equalized electronically without losses. Also, the RZ format together with PSK guarantees a superb resistance against nonlinear degradations due to cross phase modulation.

The key components necessary to realize the synQPSK transmission system were not available. The traditional phase locked loop (PLL) based solution would fail because the product of laser linewidth and loop delay is too large. The novel PLL free feedforward carrier and data recovery scheme would eliminate the need for OPLL. This scheme relaxes the laser linewidth requirements so that standard DFB lasers can be utilized. The project ´´synQPSK - key components for synchronous quadrature PSK`` funded by the European Commission, aims at the realization of all key components which are not commercially available for the implementation of a 40 Gbit/s synchronous optical RZ QPSK transmission system with polarization multiplex.

One of the integral parts of the synQPSK receiver is the DSP module which performs the clock-and-data recovery (CDR) operation after the A/D conversion of the input electrical QPSK signal. The signal processing module uses CMOS logic which operates at relatively low speeds compared to the A/D converter output which uses ECL in SiGe technology. The A/D output signal has a symbol rate of 10 Gbit/s. Therefore the input interface of the DSP unit should be able to convert 10 Gbit/s input signals to 1.25 Gbit/s signals at the output. In addition the interface must convert SCFL input stage signals to CMOS logic output stage signals. This dissertation discussed the design of the input interface of the DSPU of the synQPSK receiver. The issues like power consumption, layout design, clock control, and clock distribution were discussed in the context of a large scale analog IC design. All the

designs were done using 130 nm bulk CMOS technology with six metal layers. The DSPU and interface unit were combined to form a mixed signal IC.

The basic building blocks of the interface (i.e.: static frequency divider and 1:2 DEMUX) were built as stand-alone chips in order to establish the design cycle and gauge the performance of various circuit topologies. Using these circuits the use of the active loads, passive current sources, and voltage reference generation among other things were tested. Subsequent testing of these MOS chips allowed gauging the performance of the MOS technology and various circuit components. Furthermore testing of chips helped to decide the alterations needed in the actual interface circuit such as replacing active loads by resistive loads.

Different transmission line models which were used within chips and in prototype ceramic boards were simulated in order to obtain the transmission line dimensions so as to maintain the transmission line characteristic impedance at 50 Ω. The transmission line types that were modeled includes microstrip line, co-planar line, co-planar line with ground plane underneath, and edge-coupled co-planar line with ground plane underneath.

The input interface of the CMOS DSPU of the synQPSK receiver was designed. The interface includes two 5-bit synchronized 1:8 DEMUX blocks operating at 10 Gbit/s input data rate. The input of the interface is connected to two 5-bit A/D converters that convert I and Q components of the received signal to the digital domain. The differential SCFL signals at the input are converted to 1.25 Gbit/s CMOS logic signals at the output. The SCFL →CMOS conversion is done between $2^{nd}$ and slow $3^{rd}$ DEMUX stages. This allows to reduce the power consumption and the layout area of the $3^{rd}$ DEMUX stage, which are critical design variables in large-scale analog ICs. The design of the clock distribution network (CDN) was the most critical design challenge. The CDN was designed so that whole DEMUX is synchronized. This was achieved by designing the CDN as symmetric as possible and inserting meander lines in order to maintain clock signal line lengths equal whenever necessary. In order to maintain the intra-DEMUX stage synchronization, clock control modules were implemented after every clock divider stage. Intermediate buffers were inserted at various points of the CDN in order to maintain the clock signal strength. In the layout design process the metallization widths were chosen to maintain the IR drop within reasonable limits and to have sufficient current carrying capacity. The layout was done as symmetric as possible in order to maintain the synchronization. The interface module was integrated to the DSPU which forms a mixed-signal system. In order to suppress switching and other forms of noise the substrate around interface and circuitry is grounded.

The input interface of the CMOS DSPU chip of the synQPSK receiver with polarization multiplex (CMOS-B) was designed. The interface includes four 5-bit synchronized 1:8 DEMUX blocks designed to operate at 10 Gbit/s input data rate. Most design details are similar to that of the input interface of the CMOS-A. But this interface is two times the input interface of the CMOS-A chip. Therefore the clock distribution network is also about twice as large. This posed a greater challenge in designing the CDN. The CDN in both cases has tree topology. The layout of this interface was more compact than that of CMOS-A interface. That kept the layout area at a minimum. The CMOS-B chip was tested in a low-speed and in a high-speed setup. First, a PCB was designed to test the standalone chip in low-speed (upto 1.5 Gbit/s). Then a high-speed ceramic prototype board was designed in order to test the CMOS-B chip in combination with the four A/D converters. This ensamble forms an electrical signal processing domain of the synQPSK receiver with polarization multiplex.

Simulation results were presented with regard to ultra-high-speed performance of the 130 nm CMOS process. Furthermore estimates were made with regard to the achievable speed in 90 nm and 65 nm CMOS technologies.

The clock distribution emerged as a major design challenge in the design of large scale analog ICs because of the size of the layout. The clock distribution was done symmetrically in order to maintain the synchronization of the system. In such circuits, clock skew limits the maximum achievable speed of the system. Even though at the design stage the clock distribution network was designed symmetrically and end-to-end clock path lengths were maintained identical, the random chip fabrication process variations and non-uniform substrate temperature could introduce clock skew. A method to estimate the mean clock skew in a balanced H-tree CDN was introduced. The proposed algorithm computes the skew of a N-level balanced H-tree CDN in N steps. The simulated and calculated clock skew values for varying number of processors with uniform and non-uniform temperature profile was compared.

One drawback in the synQPSK receiver module is that A/D conversion units and CMOS DSPU are in separate chips. They have to be integrated using a custom made ceramic prototype board. This process introduces transmission losses and contact losses due to the wire bonding process. The cost of integration and the performance degradation can be avoided if both A/D units and DSPU are integrated to a single die. This can be achieved by using a circuit technology like BiCMOS as it combines BJT and CMOS technologies. As discussed in [87] use of smaller CMOS technology (90 nm or 65 nm) will reduce the power consumption and chip area.

According to the test results the switching noise of DSPU limits the performance of the mixed signal chip considerably. Therefore, stringent noise suppression measures should be included in any future design.

The synQPSK scheme with polarization multiplex is designed to upgrade 10 Gbit/s systems to achieve 40 Gbit/s. If 8-PSK is used instead of QPSK the achievable speed rises up to 60 Gbit/s but at the cost of BER performance. This issue was discussed in [29]. It is worth investigating the implementation of an 8-PSK receiver.

As CDN is a critical issue in synchronous ICs, it would be useful to extend the results obtained in this thesis to a general CDN. An algorithm which calculates skew of a general CDN when the die area has a non uniform thermal profile could also be investigated.

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