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Metal- insulator- semiconductor- structures and AlGaN/GaN hetero-junctions based on cubic group-III nitrides

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Abstract

Cubic AlGaN/GaN hetero-junction field effect transistor structures were fabricated by plasma assisted molecular beam epitaxy on 3C-SiC (001) substrates. The structural quality of the layers was controlled *in-situ* by reflection high energy electron diffraction and *ex-situ* by high resolution x-ray diffraction, atomic force microscopy and time of flight secondary ion mass spectroscopy. Metal-Insulator-Semiconductor structures were realized using plasma assisted molecular beam epitaxy and plasma enhanced chemical vapour deposition. The characterization of the structures was performed using electrical techniques like capacitance-voltage-, current-voltage-, Hall effect-measurements and admittance spectroscopy.

The absence of spontaneous and piezoelectric fields in the cubic AlGaN/GaN system allows the fabrication of normally-on and normally-off hetero-junction field-effect transistors. However, there were two critical issues in the operation of the fabricated transistor devices. On the one hand it was the insufficient insulation of the gate contact and on the other hand it was the deficient electrical insulation to the high conductive 3C-SiC substrates. Both effects act as parasitic leakage current mechanisms and drop the device performance.

To improve the gate characteristics an insulating layer is required. Insulating SiO_2 and Si_3N_4 layers were produced using plasma enhanced chemical vapour deposition. An *in-situ* method of deposition of Si_3N_4 directly inside the molecular beam epitaxy chamber is discussed. The metal-insulator-hetero-junction-semiconductor-structures were characterized by capacitance-voltage- and admittance-spectroscopy-measurements.

Several techniques were analysed to electrically isolate the conductive substrate from the active transistor device. The growth on alternative semi-insulating carbonized silicon substrates is discussed. In case of the free standing high conductive 3C-SiC substrate to drop the conductivity of the cubic GaN buffer layer carbon doping was used. Due to a large conduction band offset between cubic GaN and cubic AlN asymmetric multi quantum well structures were grown to prohibit current flow towards the substrate. The investigations were performed by current-voltage analysis.

Using standard ultra violet lithography, thermal metal evaporation, lift-off process, reactive ion etching and plasma enhanced chemical vapour deposition transistor devices have been fabricated. A cubic GaN field effect transistor operation is presented. Metal-insulator-semiconductor-hetero-junction field effect transistors with normally-on and normally-off characteristic were realized. However, this work will also show that ohmic metal contact formation on c-AlGaN/GaN still have to be optimized.

Contents

1. Introduction

One of the most important fields of research in modern physics is the reduction of dimensionality of optoelectronic and electronic devices. The growth of hetero-junction-structures causes the formation of a two dimensional electron gas (2DEG) at the hetero-interface. This feature allows an ultra-fast and a high-efficiency electron and data transport. The outstanding electronic features are attributed to the characteristic density of states in such low dimensional systems.

AlGaN/GaN hetero-junction field-effect transistors (HFETs) are presently of major interest for use in electronic devices, in particular for high-power and high-frequency amplifiers. This is motivated by their potential in commercial and military applications, e. g. in communication systems, radar, wireless stations, high-temperature electronics and high-power solid-state switching [1-2]. This is affected by extraordinary high thermal, mechanical and chemical stability of the group-III nitrides. State of the art HFETs are currently fabricated of the *c*-plane surface of wurtzite (hexagonal) AlGaN/GaN hetero structures. Their inherent spontaneous and piezoelectric polarization fields produce extraordinary large sheet carrier concentrations at the AlGaN/GaN hetero-interface. Only a few *c*-plane orientated AlGaN/GaN HFETs exhibiting normally-off behaviour have been reported [3-4]. Therefore nearly all of these devices are of normally-on type.The growth of wurtzite GaN along a non-polar direction (*a*-plane or *m*-plane) is an alternative way to reach normally-off HFET characteristics [5-7]. It turned out that the output characteristics depend on the gate finger orientation using non-polar directions in wurtzite material. However, for switching devices and digital electronics field-effect transistors with normally-off characteristics are desirable.

A direct way to eliminate this polarization fields in HFETs is the growth of non-polar cubic (c-) AlGaN/GaN [8-10]. The first HFET with normally-off characteristics based on c-AlGaN/GaN hetero-structure [11] was recently realized. However, this device revealed two critical issues in the operation of the c-AlGaN/GaN HFET: The gate leakage current and the parallel substrate leakage current. The gate leakage current is undesirable for high-power and low-noise applications and severely reduces the device performance. Therefore the use of metal-insulator layers instead of a Schottky gate contact, leading to the metal-insulator-semiconductor (MIS-) HFETs, is proposed for improved device characteristics [12-13].

Over the years various insulating materials like SiO_2, SiO_xN and Si_3N_4 for III-V compounds have been widely studied. These insulators are mainly deposited by plasma enhanced chemical vapor deposition. However, during transport to the deposition chamber the c-GaN surface is exposed to the atmosphere which may lead to the formation of additional defect states. A sufficient high quality of the interface between the insulator and nitride epilayer is one critical issue of any MIS structure. Growing Si_3N_4 *in-situ,* directly in the MBE chamber after the growth of c-GaN, may prevent the formation of such defect states [14-15]. Two types of insulating layers were investigated in this work [16-17]: Si_3N_4 and SiO_2.

The insulators were mainly deposited by plasma enhanced chemical vapor deposition (PECVD). Si_3N_4 layers were also successfully produced *in-situ* inside the molecular beam epitaxy (MBE) chamber. The MIS structures were electrically investigated by current-voltage

(IV), capacitance-voltage (CV) and by admittance spectroscopy. The results are discussed in chapter 5.

The most suitable substrate for the growth of cubic AlGaN/GaN hetero-structures is 3C-SiC (001) with an effective lattice mismatch of -3.5 %. However, one of the critical issues in the HFET-Operation on this substrate is its high conductivity. It increases the parallel conductance of the device resulting in a substrate shunt current. An alternative substrate to the free standing 3C-SiC is the so called carbonized Si. The carbonized Si substrate consists of a thin (3-40) nm 3C-SiC layer epitaxially grown on 400 µm Si substrate. In consequence of an effective lattice mismatch of about 19.7 % between Si and 3C-SiC, the 3C-SiC layer is fully relaxed resulting in an increased dislocation density. This is undesirable for high-power and low-noise applications and severely reduces the device performance. Hall-Effect measurements of c-GaN, grown on the carbonized Si substrates, yield p-type conductivity. This feature is also undesirable for n-type HFET operation.

In chapter 6 several ways of electrical device isolation are discussed. One possibility is the use of a carbonized silicon substrate consisting of a thin 3C-SiC layer grown on a semi-insulating Si substrate. Another solution is carbon doping of cubic GaN, at a certain carbon incorporation the conductance of c-GaN reduces by more than two orders of magnitude [18] [19]. The third method of electrical separation of the active device from the substrate is an incorporation of c-AlN barrier layers, due to a large conduction band discontinuity between c-GaN and c-AlN of 2.03 eV [20]. An asymmetric multi quantum well (MQW) structure which is embedded within the c-AlN barriers prevents the quantum-mechanical tunneling process of conduction band electrons [21].

In chapter 7 FET based on cubic GaN is presented. Also cubic AlGaN/GaN MISHFETs are introduced and devices with both normally-on (depletion-mode) and normally-off (enhancement-mode) output characteristics are demonstrated. Finally a summary of achieved results and a short outlook is given in chapter 8.

2. Fundamentals

The basic properties of a semiconductor material are mainly described by the arrangement of atoms. The crystal symmetry of the semiconducting material affects it´s optical and electrical properties. In this chapter, basic properties of the hexagonal (wurtzite) GaN and cubic (zinc-blende) GaN will be briefly presented. The main focus of attention is given on the cubic structure of GaN and AlN and their alloys.

2.1 Properties of GaN

Basically GaN crystallizes in wurtzite (hexagonal) or in zinc-blende (cubic) structure. The wurtzite crystal structure of GaN is the thermodynamically stable phase under ambient conditions. Only a very narrow parameter window is available to produce the metastable cubic GaN phase. **Fig.2.1** illustrates the unit cells in wurtzite and zinc-blende structures. The wurtzite structure has a hexagonal unit cell, having two lattice constants; *a* and *c* while the zinc-blende structure is formed from a group of cubic unit cells and has a higher degree of crystallographic symmetry as its lattice constants are equal in three perpendicular directions.
Due to this high symmetry no internal spontaneous and piezoelectric polarization fields occur in growth direction [001]. The gallium atoms are localized in a face-centered cubic arrangement, their base is $a/2$ x {(1,1,0);(1,0,1);(0,1,1)}. The nitrogen atoms have the base $a/4$ x {(1,1,1)}, a = 4.53 Å is the lattice parameter of the cubic unit cell [22].The zinc-blende structure of GaN features strong covalent bindings between the atoms resulting in high thermal, chemical and mechanical stability. These properties make cubic GaN an excellent candidate for electronic and optoelectronic high-power devices. Additionally the material is distinguished by high isotropy of the dielectric function and the electrical conductivity.
In **Tab.1** the basic parameter of cubic GaN (c-GaN) and c-AlN are presented.

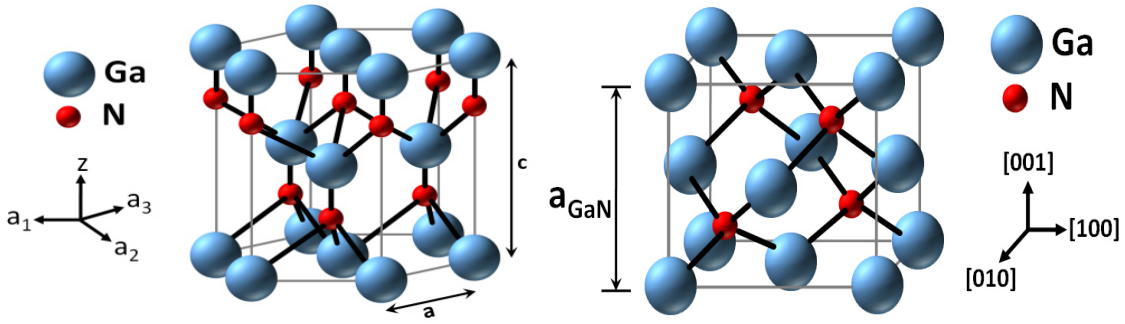


Figure 2.1 *Arrangement of Ga and N atoms in wurtzite a) and zinc-blende b) unit cell GaN*

parameter	c-GaN	c-AlN	3C-SiC
lattice parameter [Å]	4.53 [22]	4.37 [23]	4.359 [24]
band gap [eV]	3.26 (dir) [22]	5.93 (dir) [25] 5.3 (ind) [25]	2.4 (ind) [26] 6.7 (dir) [26]
static dielectric constant	9.44 [27]	8.07 [25]	9.66-9.72 [28, 29]

Table 2.1 *Basic parameter of c-GaN, c-AlN and 3C-SiC*

The lattice parameter of c-$Al_xGa_{1-x}N$ is calculated using Vegard`s law:

$$a(Al_xGa_{1-x}N) = xa(AlN)+(1-x)a(GaN) \quad (2.1)$$

The band gap of $Al_xGa_{1-x}N$ alloys is evaluated using following expression:

$$E_g(Al_xGa_{1-x}N) = xE_g(AlN)+(1-x)E_g(GaN)+bx(1-x) \quad (2.2)$$

Equation 2.2 consists of a linear part (Vegard´s law) and a nonlinear expression containing the factor which is suggested in reference [30] to be b = -0.76 eV. The bowing parameter b represents the magnitude of the parabolic nonlinearity. Since there is a strong variation concerning the bowing factor in the literature only the linear part of **equ.(2.2)** was used in this work.

Another important parameter is the conduction band discontinuity ΔE_C at the c-AlGaN/GaN hetero-interface. C. Mietze et al. [20] have found a conduction band offset of 1.4 eV by infrared absorption measurements at coupled c-AlN/GaN super-lattice structures. However, in coupled super-lattice structures a convolution in k-space occurs. Only the indirect band gap of c-AlN of $E_g(\Gamma-X)$ = 5.3 eV plays a role in this case. Since c-$Al_xGa_{1-x}N$ is a direct material up to an Al content of 0.71[31] only the direct band gap of $E_g(\Gamma-\Gamma)$ = 5.93 eV has been taken into account in this work. Therefore the conduction band offset was calculated as follows:

$$\Delta E_C(AlN/GaN) = 1.4\ eV+\{E_{g,AlN}(\Gamma-\Gamma)-E_{g,AlN}(\Gamma-X)\} \quad (2.3)$$

Thus the conduction band offset between c-GaN and c-AlN is 2.03 eV.

2.2 Molecular Beam Epitaxy of III-Nitrides

A Riber 32 molecular beam epitaxy (MBE) system was used to grow the c-AlGaN/GaN hetero-structures. The growth of the meta-stable cubic phase of GaN and AlN takes place in a narrow parameter window. The optimum conditions for the growth of cubic GaN are mainly determined by two parameters, namely the surface stoichiometry and the substrate temperature [9]. Both parameters are interrelated therefore an *in-situ* control of both is necessary. This is achieved by monitoring the growth process by reflection high-energy-electron-diffraction (RHEED) [32]. In **Fig.2.2** a schematically drawing of the used MBE system is shown.

Using a transfer system the 3C-SiC substrate was placed on the substrate manipulator inside the ultra-high vacuum (UHV) chamber. Solids like Al, Ga and Si were evaporated from effusion cells. The molecular nitrogen was dissociated using a plasma source. The CBr_4 molecules were cracked on the sample surface. Metallic shutters allow the interruption of the molecular beams with a delay time beyond one second. As the quantity of the evaporated material is directly proportional to the temperature of the effusion cell, the material fluxes are controlled by the temperature. The atomic flux of each source is measured with ionization (Bayard-Alpert) gauge. The knowledge of the atomic fluxes of the different materials allows the control of composition of ternary compounds by the temperatures of the cells. In order to incorporate as less impurities as possible, high purity (99.9999 %) source materials are used.

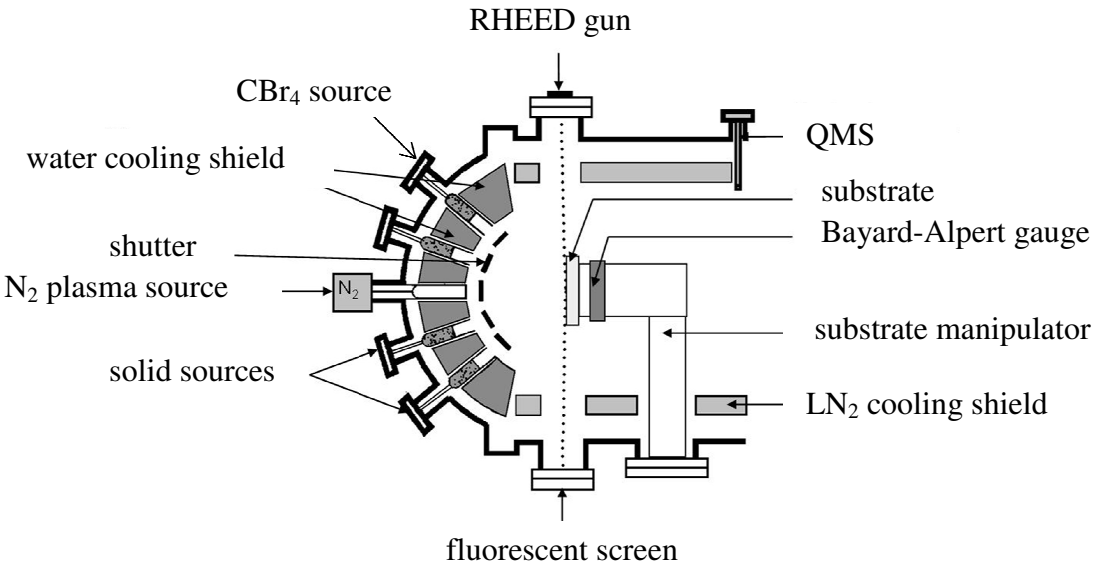


Figure 2.2 *Schematically drawing of the used Riber 32 MBE system*

Cubic AlGaN/GaN layers were grown at 720 °C on free standing, highly n-doped 3C-SiC (001) substrates. The growth rate of c-GaN was determined *ex-situ* by reflectance measurements, although the growth rate of the c-AlGaN layers were obtained *in-situ* measuring RHEED oscillation periods during initial growth process. In order to minimize hexagonal inclusions in our layers and to obtain an optimum interface roughness, the coverage of one monolayer (ML) Ga was established during growth [33-34]. The background

pressure during the growth was $7x10^{-6}$ mbar, the atomic fluxes of nitrogen, gallium and aluminum were in the range of $2x10^{14}$ $cm^{-2}s^{-1}$, $3.6x10^{14}$ $cm^{-2}s^{-1}$ and $3.5x10^{14}$ $cm^{-2}s^{-1}$, respectively. N-type doping was achieved using Si which was evaporated from a solid effusion cell. P-type doping was realized by carbon incorporation. For a carbon source a CBr_4 sublimation source was used and was directly connected to the MBE chamber. No-carrier gas was used and the CBr_4 flux was set by a high precision needle valve at a constant source temperature of 20 °C. A detailed description of the C doping can be found in section 6.2. More details about the MBE are given in ref. [35].

2.3 Characterization methods

2.3.1 Atomic Force Microscopy

Atomic force microscopy (AFM) was used to investigate the topological quality of the epitaxially grown samples. Values like peak-to-valley-ratio or the surface roughness are determined by this method on an atomic length scale. A tip mounted on a cantilever scans the surface of the sample in contact mode in the x-y-plane. The atomic interaction of the tip atoms and the surface atoms can be described by the Lennard-Jones Potential.
Depending on the features of the surface repulsive or attractive forces occur resulting in a deviation of the cantilever. In **Fig.2.3** the principle function of an AFM is demonstrated. The deviation is measured by a laser beam which is pointed to the backside of the cantilever and is reflected to a four quadrant position sensitive photo detector. After collecting this information a program creates a color-coded 2D view of the sample surface. Since the AFM method is very impact-sensitive the sample is placed on a vibration free scan table.

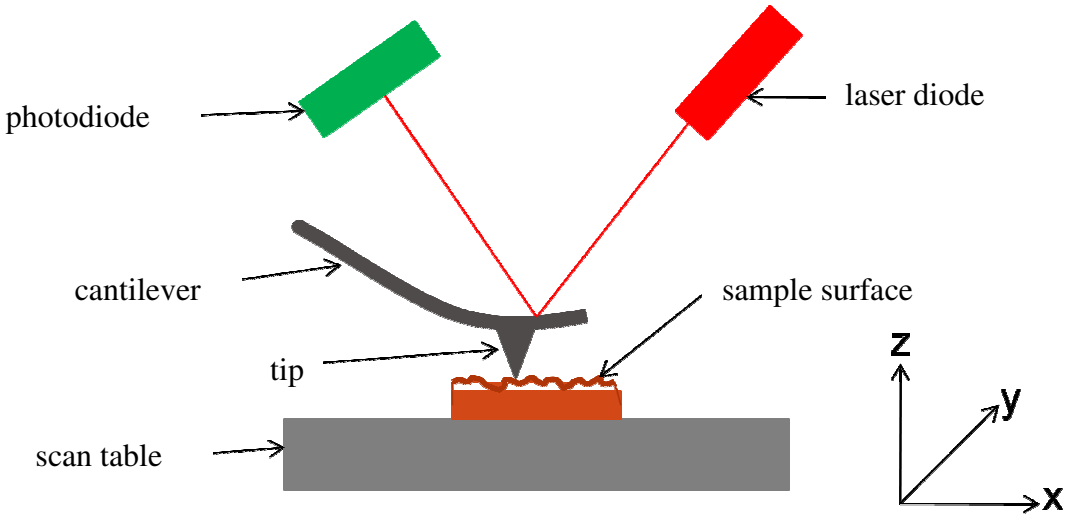


Figure 2.3 *AFM measurement arrangement, the deflection of the cantilever is detected by a laser beam (light detector/photodiode, laser diode, piezo arrangement, cantilever with the AFM tip, sample)*

The following expression was used to determine the surface root-mean-square (RMS) roughness of the grown samples:

$$S_q = \sqrt{\frac{1}{MN}\sum_{k=0}^{M-1}\sum_{l=0}^{N-1}\left(\Delta z(x_k, y_l)\right)^2} \qquad (2.4)$$

Where M and N are the quantities of pixels in x- and y-direction, $\Delta z = z - \langle z \rangle$ is the deviation from the mean value $\langle z \rangle$ at the data point position (x_k, y_l).

2.3.2 High Resolution X-Ray Diffraction

A sensitive non-destructive method to characterize semiconductor epitaxial layers is the high resolution x-ray diffraction (HRXRD) method. Therefore informations about the crystal strain, the crystal quality (dislocations), the composition of ternary compounds and possible hexagonal inclusions in c-GaN can be obtained. X-ray measurements are described by Bragg-condition [36]:

$$2d_{hkl}\sin(\theta_m) = m\lambda \tag{2.5}$$

Where d_{hkl} is the spacing of the lattice planes indicated by the Miller indices (hkl) triplet, θ_m is the angle of incidence for the diffraction maximum in the m´th order and λ is the used x-ray wavelength. For cubic lattice symmetry and a given lattice parameter a_0 the spacing of the lattice planes d_{hkl} is given by:

$$d_{hkl} = \frac{a_0}{\sqrt{h^2 + k^2 + l^2}} \tag{2.6}$$

In **Fig.2.4** the schematically HRXRD measurement arrangement is pictured. A Phillips X-Pert materials research diffractometer was used with a copper anode emitting the $K_{\alpha 1}$ radiation with a wavelength of λ = 1.5406 Å. The tube is equipped with a line focus and a hybrid monochromator which guarantees a beam divergence of maximum 47 arcsec. The monochromator system consists of a graded parabolic mirror in connection with a (220) channel cut Germanium crystal. The mirror parallelizes the beam and the Germanium crystal removes the $K_{\alpha 2}$ line. The samples are mounted onto a Euler cradle which allows the independent changes of angle of incidence ω, the diffraction angle 2θ, the rotation around the surface normal Φ and the incident axisΨ, as well a linear motion in the three directions x, y, and z. The measurements were performed in double axis configuration using a 1/2 ° divergence slit in front of the detector. The diffracted beam is detected by a scintillation counter mounted on a rotatable detection circle 2θ. Measurements in 2θ direction imply that the angular speed of the detector is twice as fast as the speed of the incident angle. In case of scanning symmetrical lattice points it is equal to reflections from lattice planes parallel to the sample surface.

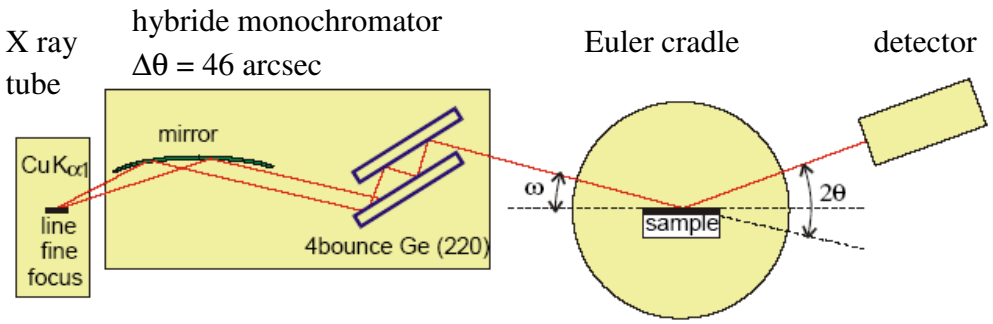


Figure 2.4 *Schematically drawing of the HRXRD measurement arrangement*

We get information with respect to vertically aligned properties, like the composition of ternary alloys or the relative lattice parameter of the grown epilayer. The rocking curve is a scan with the detector angle in a fixed position, while only the angle of incidence ω is changed. From the width of the reflex perpendicular to the surface the density of defects can be evaluated using [37]:

$$D = \frac{(\Delta\omega)^2}{9\left|\vec{b}\right|^2} \tag{2.7}$$

$\Delta\omega$ is the full width of half maximum (FWHM) of the rocking curve and $\left|\vec{b}\right| = \frac{a}{\sqrt{2}}$ is the absolute value of the Burger´s vector assuming a 60 ° dislocation orientation. Measuring c-AlGaN/GaN hetero-structures in a mapping mode allows the determination of the Al mole fraction within the c-AlGaN layer and the degree of relaxation of the c-GaN buffer. More details of x-ray diffraction are given in ref. [38].

2.3.3 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy (SIMS) is an analytical technique to characterize the surface and near surface (approximately up to 30 µm) region of solids. The technique uses a beam of energetic (0.5-20 keV) primary ions to sputter the sample surface, producing ionized secondary particles that are detected using a mass spectrometer. **Fig.2.5** illustrates schematically the operation of time of flight (ToF) SIMS.

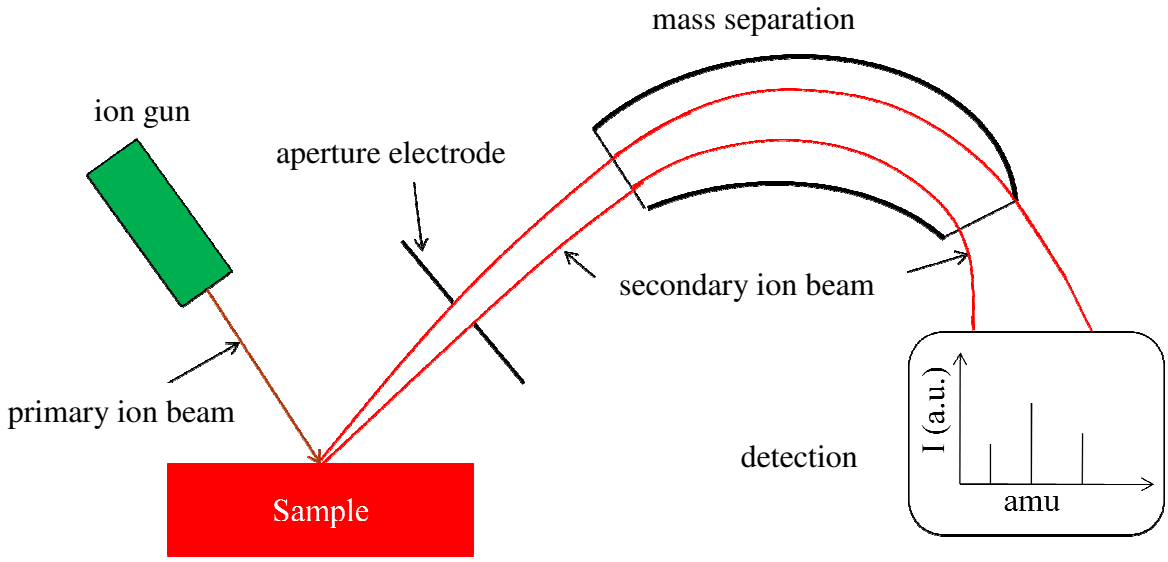


Figure 2.5 *Schematically drawing of the SIMS measurement arrangement*

The primary beam can be O_2^+, O^-, Cs^+, Ar^+, Xe^+, Ga^+, or any other species that have been used successfully for various applications. O_2^+ is typically used for the detection of electropositive species, Cs^+ for electronegative species, and Ga^+ for improved lateral resolution. The sample can incept the primary beam at different angles of incidence, with a typical range from normal to 60 ° degrees from normal. The sputtering process is not just a surface layer phenomenon but consists of the implantation of the primary species into the ample and the removal of surface atoms by the energy loss of the primary ions in the form of a collision cascade. Many species are formed by the interaction of the beam with the sample atoms, but the positive and negative secondary ions are the species of interest for SIMS. Most of the secondary particles are neutrals. Either they are lost for SIMS detection or they can be detected by post ionization. The secondary ions are extracted by electric fields and then energy and mass analyzed. The mass separation is carried out by mass separators like quadrupole mass spectrometer (QMS) or ToF mass separator. Hereby the element separation is done by the specific mass to charge ratio (m/q). Detection is by electron multiplier, Faraday cup, or ion sensitive image amplifier for imaging. SIMS is usually used to determine material composition a depth profile of the samples. Depth profiles are obtained by sputtering the sample with the primary ion beam. One or more masses are monitored sequentially by switching rapidly among masses. More details about secondary mass spectroscopy are for example given in [39 - 40].

2.3.4 Capacitance- and current- voltage measurements

In this chapter capacity-voltage (CV) [41] and current-voltage (IV) measurements at c-AlGaN/GaN hetero- structures are described. **Fig.2.6** shows a typical CV measurement of a metal- insulator- semiconductor (MIS) arrangement. On top of a c-AlGaN/GaN hetero-structure a thin (5-30) nm SiO_2 layer is deposited. A metal contact was thermally evaporated on the insulating SiO_2 layer. The contact structure is accurately defined using UV illumination lithography. The ohmic back contact was realized by soldering the high conductive 3C-SiC substrate on a Cu plate with In.

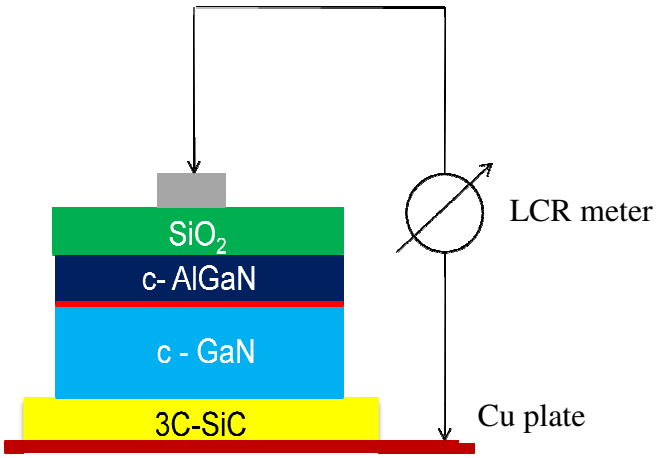


Figure 2.6 *Schematically drawing of the capacitance-voltage and the admittance-spectroscopy measurement arrangement*

The measurements were performed using an *Agilent Precision LCR-meter E4980A*. The instrument was controlled by a Labview PC program. **Fig.2.7** shows a typical CV profile of a c-AlGaN/GaN MISH structure. The capacitance distribution can be divided in three main parts. At positive voltages the capacity saturates and reaches the oxide capacitance as indicated in **Fig.2.7**. The part between 0.3 V and 1.4 V belongs to the 2DEG. The third part is the depletion zone formed in c-GaN. Overall the CV curve gives information about the oxide thickness, the electron accumulation at the c-AlGaN/GaN interface and the background net donor concentration in the c-GaN buffer layer.
To calculate the background net donor concentration and the electron distribution as a function of the distance from the sample surface within the hetero-structure the following relationships were used [42]:

$$N_D - N_A = -\frac{2}{q\varepsilon_0\varepsilon_r A^2} \Big/ \frac{dV}{dC^{-2}} \tag{2.8}$$

and

$$z_{CV} = \frac{\varepsilon\varepsilon_0 A}{C} \tag{2.9}$$

Where N_D-N_A is the net donor concentration, q the single electron charge, ε_0 is the electric field constant, ε_r the relative dielectric parameter of the particular semiconductor material, dV/dC^{-2} is the first deviation of the applied voltage and the squared inverse of the measured capacitance, and A is the area of the top metal contact.

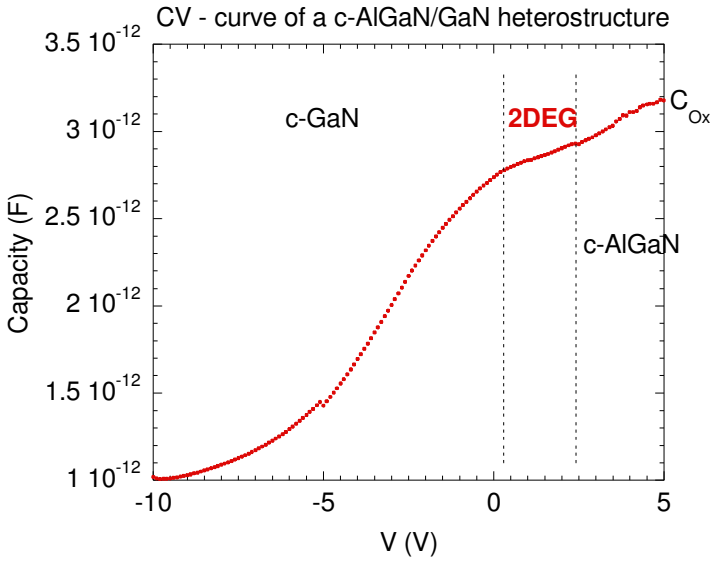


Figure 2.7 *Measured capacity vs. applied voltage profile for a c-AlGaN/GaN MISH system*

Fig.2.8 shows a doping profile of a measured MISH structure. In the diagram the measured electron concentration is symbolized by red dots, the blue solid line was a calculated electron distribution using 1D Poisson-Schrödinger solver. A clear electron accumulation [43] was detected at the c-AlGaN/GaN interface by using the CV technique [44].
To determine the capacity C and the conductance G, the LCR-meter collects the pair of values for the admittance Y and for the phase angle θ. Separating the absolute Y value using sinus and cosines function the ohmic and the capacitive resistance can be evaluated.
IV- curves of the grown structures were vertically measured using well defined ohmic, or Schottky-Contacts, on top of the sample and a grounded ohmic contact at the backside of the 3C-SiC substrate. For horizontal IV measurements, such as transmission line method (TLM) and transistor output characteristics, no ohmic back contact was used. IV measurements were performed using an *Agilent Precision Parameter Analyzer 4156C*. The samples were contacted using a *SüssMicroTec PM5* manual probe system. In this setup *PH100 ProbeHeads* with tungsten carbide probe needles with a tip radius of 7 µm were used. All electrical measurements were performed under light-tight and electrically shielded environment.

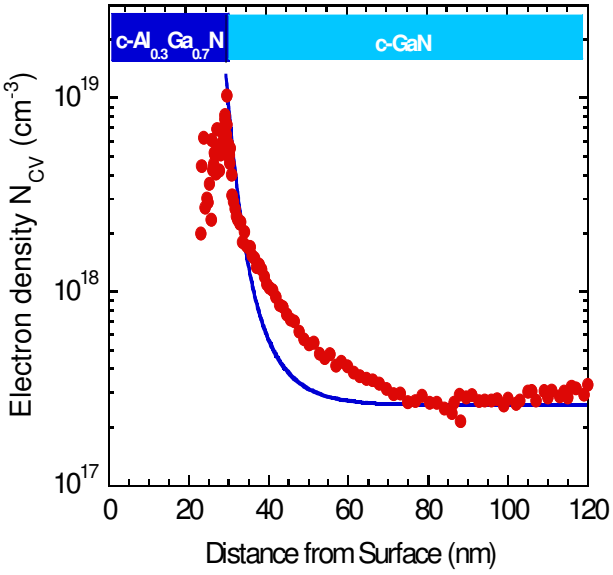


Figure 2.8 *Measured (red dots) and calculated (blue solid line) capacity vs. applied voltage for a c-AlGaN/GaN MISH system*

2.3.5 Hall- and specific layer resistance-measurements

An approved method to determine the specific layer resistivity ρ and the quantity of majority charge carrier *n*- or *p*-type is the Hall-effect measurement. Performed in van der Pauw geometry, it is possible to obtain the electrical parameter without an extensive sample preparation. A huge advantage of the van der Pauw method is that the measurement is independent from the sample geometry and the distance of the contact electrodes [45]. **Fig.2.9** shows the schematically Hall-effect measurement arrangement in van der Pauw geometry.

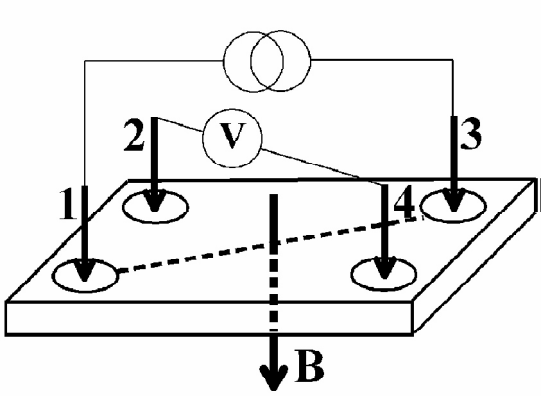


Figure 2.9 *Schematically drawing of the Hall-effect measurement arrangement in van der Pauw geometry. A current is impressed between the contacts 2 and 4, the Hall-voltage is measured between 1 and 3. B represents the applied homogeneous magnetic field perpendicular to the sample surface*

The sample dimensions are (5x5) mm², at the four edges of the samples In contact electrodes are fixed by soldering. The voltage is applied using Au wires to contact the sample with the measuring station. Applying a dc voltage between contacts 2 and 4 results in a current $I_{2,4}$ flow between these two electrodes. The Hall-voltage $U_{1,3}$ is measured between the electrodes 1 and 3. A Helmholtz arrangement of magnets generates a homogeneous magnetic field of B = 400 mT perpendicular to the sample surface resulting in a shift of the Hall-voltage by $\Delta V_{1,3}$. Hall-coefficient R_H is given by:

$$R_H = \frac{d \cdot \Delta V_{2,4}}{B \cdot I_{1,3}} \tag{2.10}$$

where d is the layer thickness, $\Delta V_{2,4}$ the effective Hall-voltage, B is the applied magnetic field and $I_{2,3}$ is the impressed current between the points 2 and 3. The sign of $\Delta V_{2,4}/I_{2,3}$ determines the type of the majority carriers, electrons or holes.
A *KEITHLEY 2612* system source-meter is used as a current generator and for the voltage measurement. The source-meter is controlled by a *Labview*-program. A schematically drawing of the measurement arrangement for the specific resistance is plotted in **Fig.2.10**. A dc current $I_{2,3}$ is applied between the points 2 and 3, the voltage $V_{1,4}$ is measured between the points 1 and 4. The measured resistances $R_{23,14}$ and $R_{31,24}$ are given by **equ.2.11**:

$$R_{23,14} = \frac{V_{1,4}}{I_{2,3}} \quad \text{and} \quad R_{31,24} = \frac{V_{2,4}}{I_{3,1}} \tag{2.11}$$

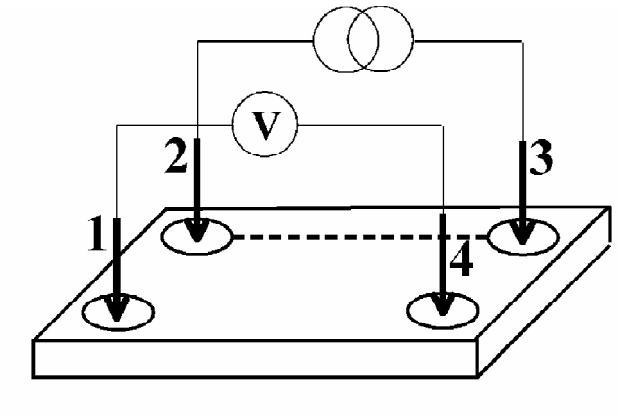


Figure 2.10 *Schematically drawing of specific resistivity measurement arrangement. A current is impressed between the contacts 1 and 4; the voltage is measured between 2 and 3*

The specific layer conductance is interrelated to the measured resistance by following expression:

$$\exp\left(-\pi \cdot d \cdot \sigma \cdot R_{23,14}\right) + \exp\left(-\pi \cdot d \cdot \sigma \cdot R_{31,24}\right) = 1 \tag{2.12}$$

Provided that the four contacts have mirror symmetry and the electrical properties are independent of crystal orientation, **equ.(2.12)** can be solved. That means:

$$R_{23,14} = R_{31,24} \text{ and } R_{31,24} = R_{24,31} \tag{2.13}$$

So the specific conductance σ is given by the following expression:

$$\sigma = \frac{\ln 2}{\pi \cdot d \cdot R_{23,14}} \cdot f \tag{2.14}$$

In **equ.(2.14)** the correction factor *f* plays a role in case of not perfectly symmetrically arranged contacts. The correction factor is a number between zero and one and can be calculated using **equ.(2.15)**:

$$\frac{R_{12,34} - R_{23,41}}{R_{12,34} + R_{23,41}} = \frac{f}{\ln(2)} ar\cosh\left(\frac{\exp\left(\ln(2)/f\right)}{2}\right) \tag{2.15}$$

This relationship can be solved either numerically or graphically. With the obtained specific conductance σ and the Hall-coefficient $R_{H,}$ the Hall-mobility is given by:

$$\mu^{Hall} = \sigma \cdot \left| R_H \right| \tag{2.16}$$

In case of a two conductive layer system (e.g. layer and substrate) equations (2.10) and (2.14) have to be modified as follows

$$\sigma_{tot} = \frac{\sigma_l d_l + \sigma_{sub} d_{sub}}{d_{tot}} \tag{2.17}$$

$$R_{H_{tot}} = \frac{d_{tot}\left(d_l \sigma_l^2 R_{H_l} + d_{sub} \sigma_{sub}^2 R_{H_{sub}}\right)}{\left(\sigma_l d_l + \sigma_{sub} d_{sub}\right)^2} \tag{2.18}$$

In these expressions σ_{tot}, R_{Htot} and d_{tot} stand for the measured values of both layer and substrate, the footnotes *l* and *sub* indicate the parameter of the measured layer and the substrate, respectively.

2.3.6 Admittance spectroscopy

Admittance spectroscopy is commonly used to characterize majority-carrier trapping defects. It is a very sensitive technique for characterizing insulator-semiconductor interface properties and it relies on characterizing the interface trap conductance by directly measuring the energy loss during capture and emission of the majority carriers (electrons) between conduction band and interface trap levels under an applied ac signal [46 - 47]. **Fig.2.11** illustrates an insulator-c-GaN structure. Two possibilities of unintentional charge incorporation are assumed, namely mobile charge Q_m and interface trapped charge Q_{it}.

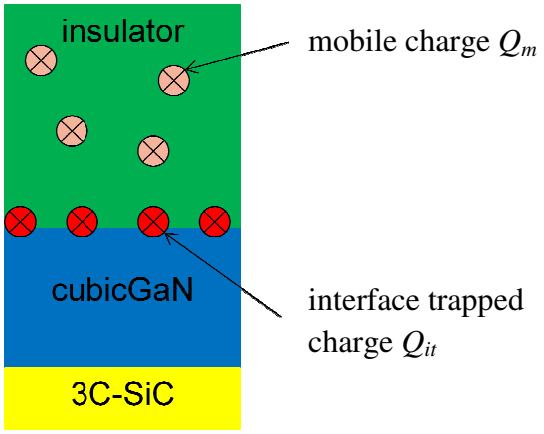


Figure 2.11 *An insulator-c-GaN semiconductor structure is shown. Two types of possible incorporated charge types, the mobile charge and the interface trapped charge; they are indicated by arrows*

Mobile charges are assumed to be incorporated during the insulator deposition process. Mobile charges Q_m cause hysteresis effects and are responsible for parasitic electric fields. It is assumed that the optimization of the insulator deposition method will reduce the amount of mobile charges. Interface trapped charges Q_{it} occur due to the interruption of the periodic lattice structure of c-GaN at the interface. The result are Ga- or N-dangling bonds. Where N-dangling bonds are donor like and act as electron traps, the Ga-dangling bonds are acceptor like and act as hole traps. These features are disadvantages for field effect transistor application and drop the device performance. The behaviour of the two dangling bond types and their energetic position within the band gap is illustrated in **Fig.2.12**. The density of interface states is plotted against the band gap energy. In analogy to GaAs, it is assumed that Ga dangling bonds cause an interface state density near the conduction band edge E_C. Replacing As- by N-atoms, nitrogen dangling bonds cause states near the valence band edge E_V within the band gap. Whereas Ga- and N-vacancies are responsible for mid-gap defects states.

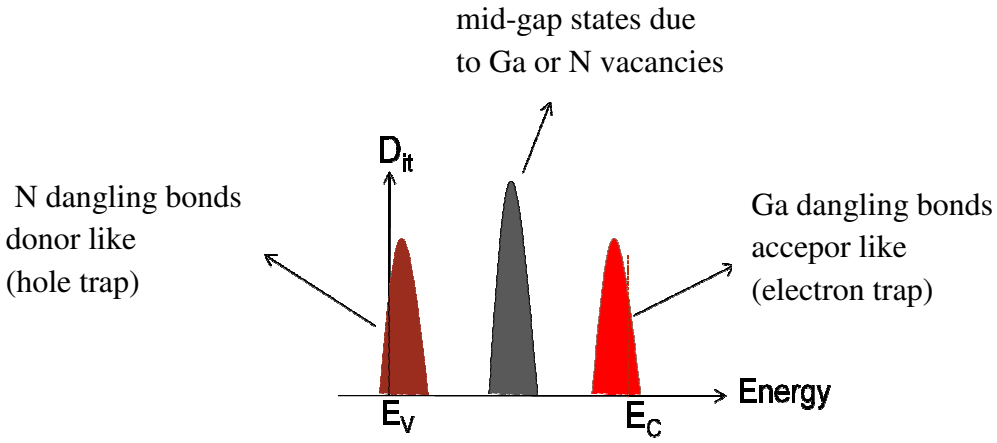


Figure 2.12 *Schematically plot of possible interface defect states within the band gap of c-GaN*

Fig.2.13 illustrates the admittance spectroscopy measurement arrangement of the electric contacted sample structure (left part) and an equivalent circuit (right part). The sample structure consists of the high conductive 3C-SiC substrate, a c-GaN buffer layer and an insulation layer. Defects at the semiconductor-insulator interface are indicated by red circles. On top of the insulator, an electrical contact was realized by UV-lithography, thermal metal evaporation and lift-off process. The ohmic back contact was realized by brazing the substrate on a Cu plate by In. The equivalent circuit consists of an insulator related capacity $C_{insulator}$. In series it is coupled with a parallel arrangement of the depletion capacity $C_{Depletion}$ and an interface defect states related capacitive $C_{interface}$ and ohmic part $R_{interface}$.

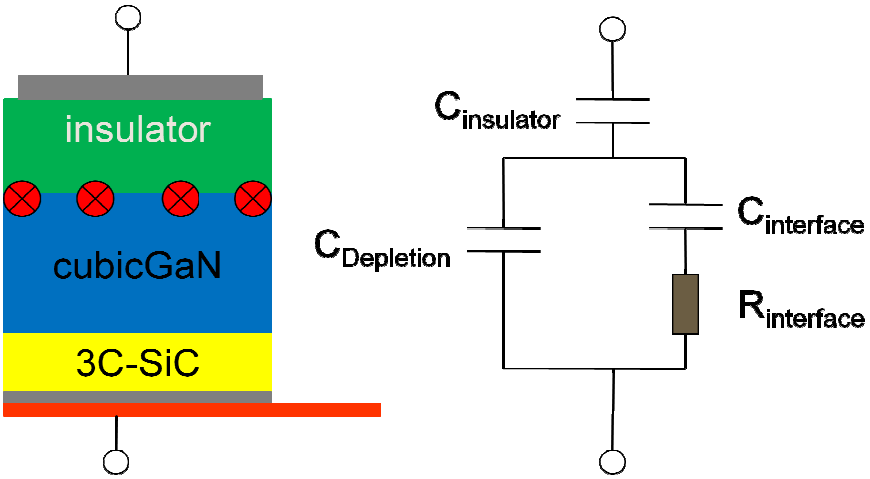


Figure 2.13 *Schematically drawing of the measurement arrangement and applied to the produced sample structure including the 3C-SiC substrate, the c-GaN layer and the insulator layer (left hand side); Equivalent circuit of the sample structure including the insulator-, depletion zone-, interface-capacity and the ohmic resistance of the interface states (right hand side)*

After series and insulator capacitance correction, the remaining parallel conductance G_p value only includes interface trap information. The equivalent parallel conductance G_p divided by ω is given by

$$\frac{G_p}{\omega} = \frac{C_{it}\omega\tau_{it}}{1+\omega^2\tau_{it}^2} \tag{2.19}$$

where $\omega_{it}=2\pi f$, C_{it} the interface trap referred capacitance and τ_{it} is the interface trap lifetime [48]. **Fig.2.14** shows the results of admittance spectroscopy measurement of a metal-Si_3N_4-c-GaN structure. The equivalent parallel conductance G_p, divided by the measurement angular frequency ω, is plotted as a function of ω. Characteristic maxima occur when the applied frequency is equal to the reciprocal value of the interface trap lifetime $\omega_{it} = 1/\tau_{it}$.

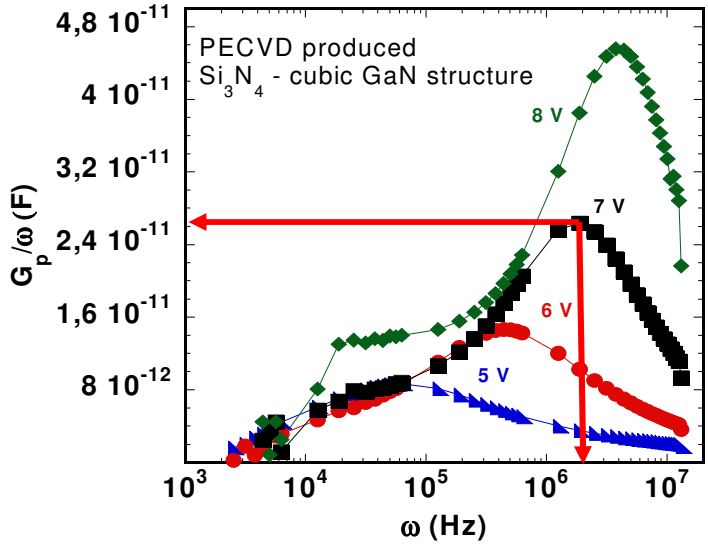


Figure 2.14 *G_p/ω plotted against ω; Results are obtained from meta-Si_3N_4-c-GaN structure; G_p/ω curves for 5 V (blue), 6 V (red), 7 V (black), and 8 V (green)are demonstrated; relevant peak information is indicated by red arrows*

The value of G_p/ω at the maximum is $C_{it}/2$, where C_{it} is the capacity associated to the interface traps. Once C_{it} is known, the interface trap density is obtained by using the relationship:

$$D_{it} = \frac{C_{it}}{q_{el}A} \tag{2.20}$$

where A is the top metal contact area and q_{el} the single electron charge. However, the interface trap life time τ_{it} is given by the Shockley-Read-Hall model [49]:

$$\tau_{it}(E_{it}) = \frac{1}{\sigma_{0n}v_{th}N_C}\exp\left(\frac{E_C - E_{it}}{k_BT}\right) \tag{2.21}$$

Here N_C is the effective density of states in the conduction band, v_{th} the thermal velocity of electrons, σ_{0n} the capture cross section of the trap, E_C the conduction band edge, E_{it} is the trap energy level below the conduction band edge, k_B the Boltzmann constant and T the temperature.

The frequency ω_{max} at the maximum of G_p/ω gives $\tau_{it}=1/\omega_{max}$ and correlates ω_{max} to a corresponding trap energy level E_{it} below the conduction band edge. The thermal velocity and density of states are well known for a specific semiconductor whereas the capture cross section of the traps depends strongly on the nature of the trap. The capture cross section can take values varying from 10^{-12} cm² to 10^{-18} cm² affecting on the energetic position of the traps within the c-GaN band gap. Since up to now this value is not known for cubic GaN, in analogy to MBE grown GaAs an average capture cross section of 10^{-15} cm² is assumed [50] to convert τ_{it} into trap level energies. An aberration of the capture cross section value of +/- three orders of magnitude results in a shift of the energetic position of +/- 170 meV within the band-gap.

3. Device Fabrication

3.1 UV Photolithography

The Lithography process is one of the most important steps in surface structuring techniques. Field effect transistor device structuring was done by contact exposition using a high pressure Hg vapour discharge lamp. Several lithography steps are needed to produce the final MIS-HFET device, which are specified in chapter 3.5. The positive photoresist ARP 3510 was used in this work, to ease the lift-off process and to get sharp edges. The resist was thinned 1:1 with a special diluter AR 300-12. Before applying the photoresist the sample surface was cleaned by acetone, propanol and DI- water. Since the c-AlGaN/GaN samples were grown under metal rich conditions the formation of Al- or Ga-droplets on the surface is possible. To remove the metal residues the samples were dipped in a HCl:DI-H_2O 1:1 bath, to remove possible Ga- or Al-droplets from the surface, for two minutes.
The diluted photoresist was applied using the spin coating technique. The rotation speed was 9000 rot/min resulting in a final resist thickness of 250 nm. The coated samples were dried for two minutes on a heating plate at 100 °C at atmosphere. The lithography positioning table is movable in x-y-directions to place the coated sample exactly beneath the mask and an additional screw is applied to adjust possible contortion in the x-y-plane. By the time the sample is in the right position under the mask, the positioning table is carefully moved in z-direction until the contact with the mask occurs. The sample is exposed for 20 s. The developing process takes place in a developer AR 300-35: DI H_2O 1:4 mixture for 30 s followed by a 30 s stop bath in DI H_2O. More details about lithography technique are given in e.g. [51 - 53].

3.2 Thermal evaporation of contact metals

In this work thermal evaporation of metals was used to deposit the contacts on top of the grown transistor structures. The thermal evaporation was performed in a high vacuum chamber where the background pressure lay at (5-8) $x10^{-7}$ mbar. Each metal material was placed in a tungsten boat which was connected to a power supply unit. The applied voltage led to a current flow through the boats resulting in heating the boats and the metal materials inside. At certain temperatures the metals began to melt and evaporate in a directed cone. In this case the temperature was indirectly controlled by the electric current. During adjusting the right current flow the chamber walls and the electric mains were also heated evaporating their possible adsorbate atoms, to protect the semiconductor surface from the adsorbate impurities a shutter was built in. At a given material density a crystal oscillator evaluates the deposited thickness recording the change in the oscillation frequency. It turned out that a deposition rate of 0.1 nm/s led to optimum metal contacts concerning the lift-off process. After evaporating 5 nm of the metal material the shutter was opened. Ohmic contacts were realized depositing Ti/Al/Ti/Au or Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) stacking structures. After depositing ohmic contacts the samples were rapidly thermal annealed (RTA) for 30 s at 850 °C in N_2 atmosphere in a heating oven. For a Schottky contact application the following metal sequence was used Pd/Ni/Au (15 nm/15 nm/50 nm). The Schottky contacts were annealed on a heating plate for 10 min at 400 °C in atmosphere [54]. In case of MIS structures a metal sequence of Ni/Au (15nm/50nm) was used. These structures were not annealed.

3.3 Reactive Ion Etching

The fabricated transistor devices in this work were placed on mesa structures. The use of this method reduced the possibility of parasitic parallel current flow and possible bypass between neighboured transistors. However etching of c-GaN (also h-GaN) was a serious challenge, responsible was the strong covalent binding of the gallium- and nitrogen-atoms. A wet chemical etching method is described in [55-56], using potassium base(KOH) diluted in DI H_2O additionally an electric field applied to the GaN crystal is needed to get an etching effect. This method proved not very practical due to a big experimental effort and very low etching rates.

An alternative is the dry chemical- or the reactive-ion-etching-method (RIE). The etching rates are 200 nm/min and 50 nm/min for c-GaN and for c-$Al_{0.3}Ga_{0.7}N$, respectively. An *OXFORD Instruments Plasmalab 80* machine was used for the dry etching experiments. Reactive ion etching is a dry etching process. It provides reproducible etching results and allows both an isotropic and an isotropic-etch profile. The principal working method of c-AlGaN/GaN RIE is shown in **Fig.3.1.**A gaseous medium is excited in a high-frequency alternating electric field and passes into a plasma state. The electric field (indicated with grey arrows in **Fig.3.1**) accelerates the ionized etching gas atoms towards the sample surface. Chemical etching occurs by the reaction of the accelerated ions with the surface atoms. The volatile reaction product is removed by the pump system. The physical etching process occurs by sputtering the surface atoms by the accelerated ions.

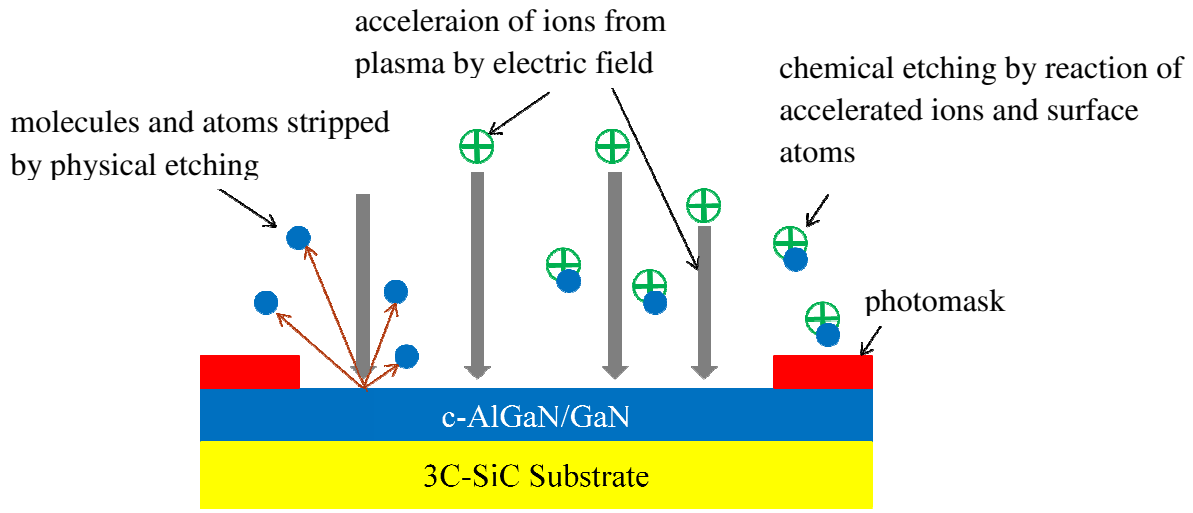


Figure 3.1 *Schematically drawing of the RIE process*

In this work RIE was used to etch the c-AlGaN/GaN hetero-structures as well as SiO_2 and Si_3N_4 insulator layers. RIE process parameter like etching gases, fluxes, substrate temperatures pressures during the etch process, rf power, and the etching rates are summarized in **Tab.3.1**.

Parameter	c-GaN	c-$Al_xGa_{1-x}N$; x < 0.35	SiO_2	Si_3N_4
Gas	$SiCl_4$	$SiCl_4$	Ar:CHF_3	O_2:CHF_3
Flux (sccm)	10	10	10.5:10.5	1.4:26.4
Temperature (°C)	20	20	20	20
Pressure (mTorr)	10	10	35	35
rf Power (W)	300	300	150	150
Etching Rate (nm/min)	200	50	40	70

Table 3.1 *RIE process parameter for c-GaN, c-$Al_xGa_{1-x}N$ (x <0.35), SiO_2 and Si_3N_4*

3.4 Plasma Enhanced Chemical Vapour Deposition

For the production of MIS- or MISH-structures an insulator or oxide layer is required. In this work MIS-structures, including Si_3N_4 and SiO_2 as insulators, were investigated. For the manufacture of MIS-structures used for CV measurements the insulators were deposited by plasma enhanced chemical vapour deposition (PECVD). The samples were cleaned prior to deposition in acetone, propanol and DI (de- ionized) water. The deposition of the insulating layers was done in a *Plasmalab 80 Plus* unit from the *OXFORD Instruments* company. The operating principle of a PECVD system is shown in **Fig.3.2**. The process gases were introduced in defined amounts (sccm) in the sample chamber. The desired process pressure was set by means of a vacuum pump which was connected via a control valve to the chamber. The plasma phase was ignited at a certain rf power, an alternating electric field working at 13.56 MHz accelerated the ionised atoms and molecules.

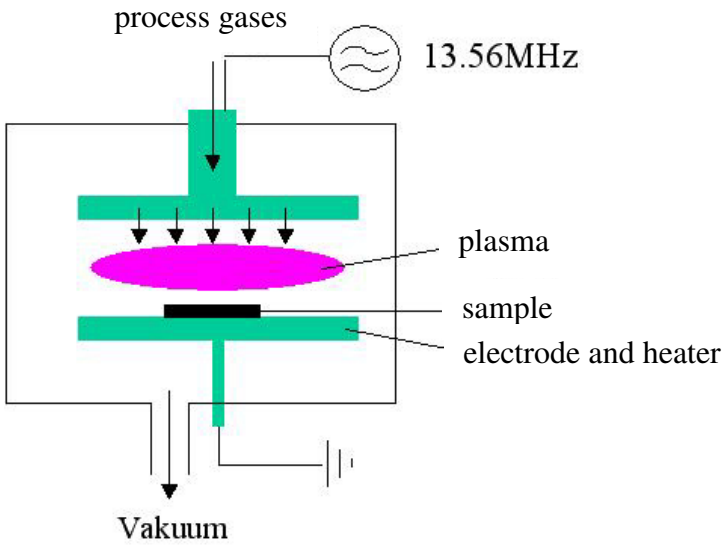


Figure 3.2 *Schematically drawing of the working principle of the PECVD chamber*

Two types of SiO_2 insulating layers were deposited at high and at low deposition rates. Also Si_3N_4 and SiO_xN_y were produced using PECVD method. The deposition formulas including gases, gas fluxes, deposition temperature, pressures, rf power and deposition rates are summarized in **Tab.3.2**.

Parameter	SiO_2 (high rate)	SiO_2 (low rate)	Si_3N_4	SiO_xN_y
Gas	SiH_4:N_2O	SiH_4:N_2O	SiH_4:NH_3	SiH_4:N_2O:NH_3
Flux (sccm)	425:710	20:60	400:30	20:70:30
Temperature (°C)	300	300	300	300
Pressure (mTorr)	1000	1000	1000	1000
rf Power (W)	20	20	20	20
Deposition Rate (nm/min)	80	1.3	16	4.5

Table 3.2 *PECVD process parameter for high and low deposition rate SiO_2, Si_3N_4, and SiO_xN_y*

3.5 Transistor device fabrication

The MISHFET device fabrication includes several steps of preparation. To remove possible excessive metal residues from the c-AlGaN/GaN surface the grown sample is dipped into a HCl:DI H_2O 1:1 bath for one minute. AFM measurements before and after HCl treatment yield no influence on the surface roughness.
The first step of the MISHFET assembly is the deposition of the ohmic source and drain contacts.**Fig.3.3** illustrates the used lithography mask no.1 (a) and a photograph taken under a light microscope showing the source and drain contacts after metal deposition (b).

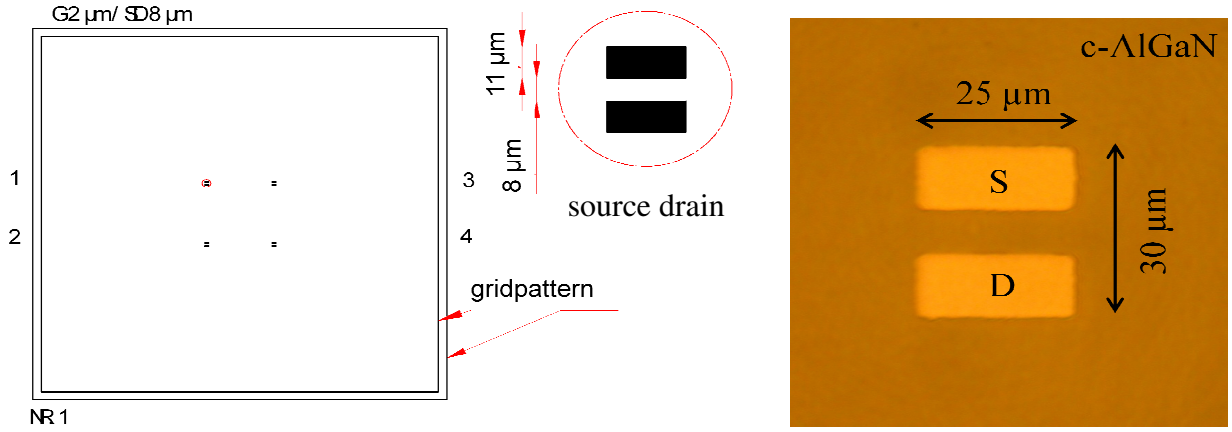


Figure 3.3a *UV- lithography mask no. 1 for the MISHFET production;* **b** *Photograph taken under a light microscope of the field number 3*

The lithography mask implies four pairs of source and drain contacts for the production of four separate MISHFET devices. The black coloured fields are free of photo-resist and the white coloured space is covered. Each device is indicated by a certain number on the left (1and2) and on the right hand (3and4) side. The mask is confined by grid patterns which provide the basis for further lithography steps as orientation lines. In **Fig.3.3b** a photograph of the device number 3 is shown. After the lithography step ohmic contacts were thermally evaporated on top of the c-AlGaN surface. In a next step evaporated ohmic contacts were rapidly thermal annealed, as described in chapter 3.2. The size of the ohmic source and drain contacts is (25x11) µm² with a spacing of 8 µm between them.
To avoid bypass current flow between each transistor device mesa structures were etched to the 3C-SiC substrate by RIE. Using lithography mask no.2 (**Fig.3.4a**) the transistor fields were covered by photo- resist to protect them from the etching process. **Fig.3.4b** shows the produced mesa structure after removal of the photo-resist. The mesa size is an area of (25x30) µm².
Since the source and drain contact area was too small to perform IV measurements, they have to be connected to larger (500x500) µm² contact pads. To electrically isolate the high conductive 3C-SiC from the contact pads a 240 nm thick SiO_2 layer was deposited by PECVD.

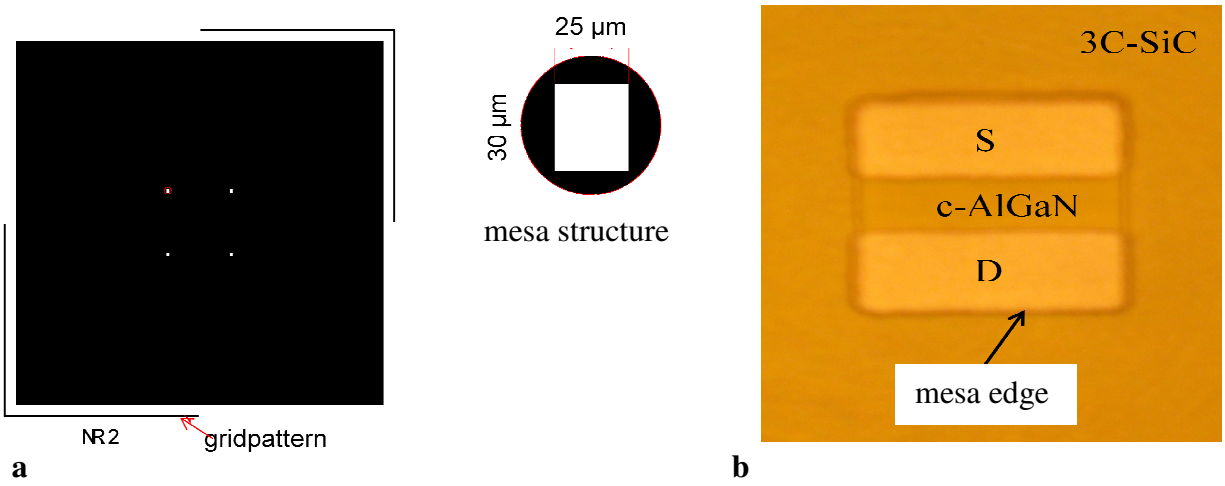


Figure 3.4a *UV-lithography mask no.2 for the MISHFET production;* **b** *Photograph showing the etched mesa structure*

After this step the substrate surface was covered by SiO_2 as well as the device area. Now mask no.3 was used to etch down the silicon oxide from the transistor device. **Fig.3.5a** illustrates the design of mask no.3. An area of (22x25) µm² was etched using RIE on the device field. The edge of the etched area is indicated by an arrow in **Fig.3.5b**.

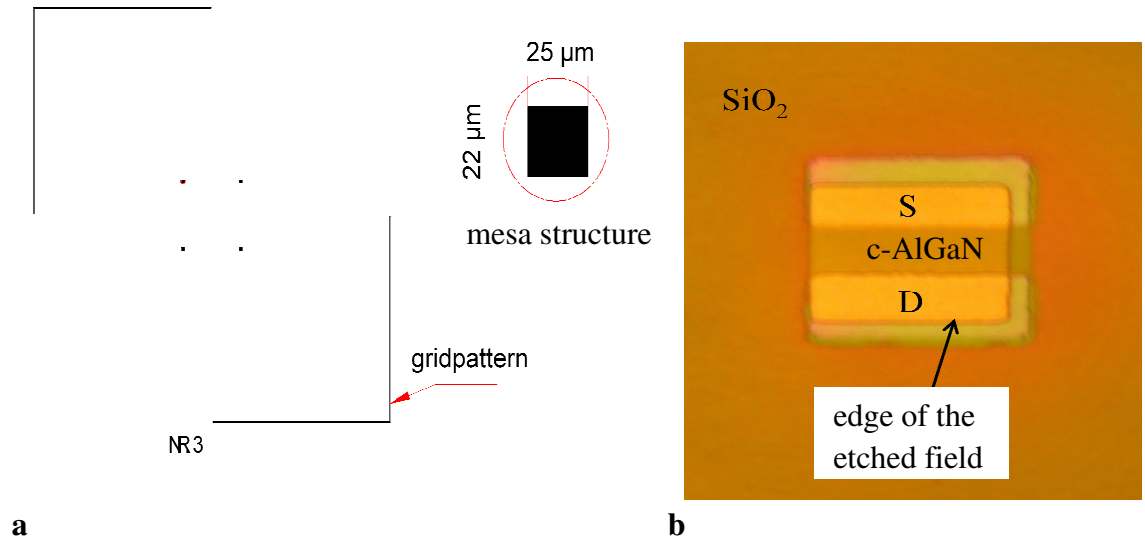


Figure 3.5a *UV-lithography mask no.3 for the MISHFET production;* **b** *Photograph showing the SiO_2 free etched area on top of the transistor field*

After the RIE step the source and drain contacts and the spacing in between were free of SiO_2. On purpose to form a MIS structure for gate operation a thin (3 nm - 10 nm) insulator (Si_3N_4 or SiO_2) layer was deposited using the PECVD method.
The positioning of mask no.4 to form the gate contact was the most delicate step in the MISHFET production. **Fig.3.6a** illustrates the design of mask no.4. The gate finger has a length of 2 µm and a width of 35 µm.

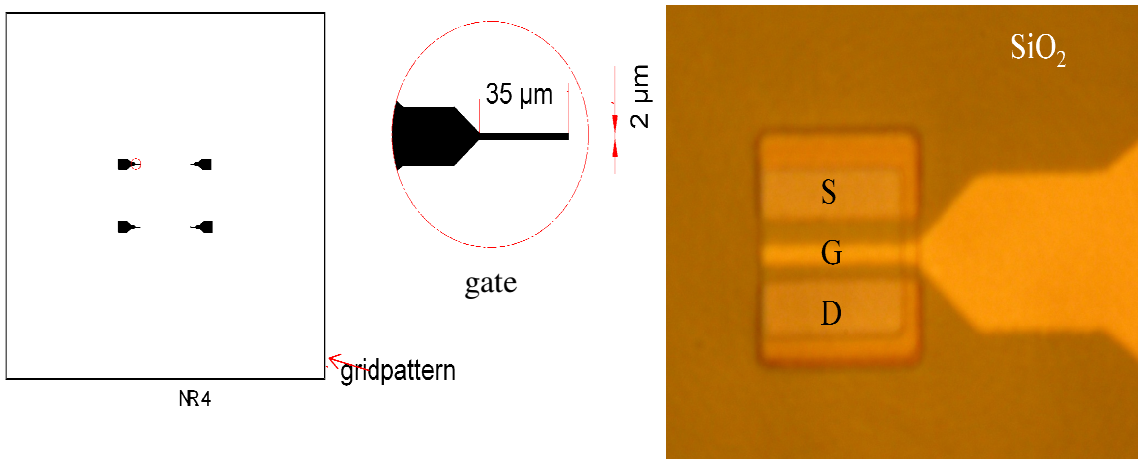


Figure 3.6a *UV-lithography mask no.4 for the MISHFET production ;***b** *Photograph showing the (2x35) µm² gate contact finger positioned between source and drain*

Fig.3.6b shows the device after the thermal evaporation of the gate metals and the photo-resist lift-off process. Ideally the gate contact is placed equally spaced from source and drain. The next step in the production of the transistor device was the removal of the thin insulator layer from the source and drain contacts. On this purpose mask no.5 was used (**Fig.3.7**).

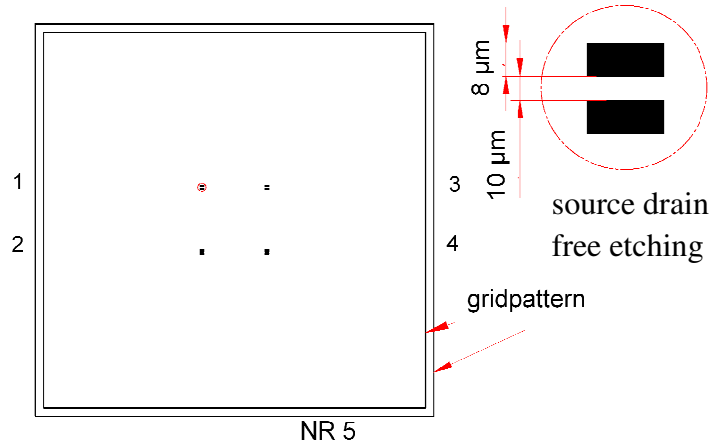
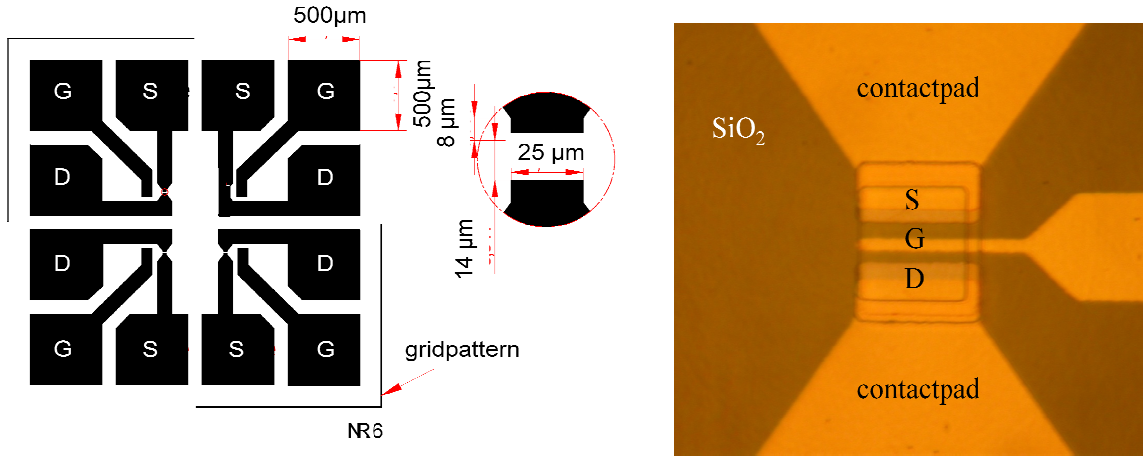


Figure 3.7 *UV-lithography mask no.5 for the MISHFET production for source and drain free etching*

The size of the etched fields is (8x20) µm² with a spacing of 10 µm. The source and drain contacts were connected to large contact pads, this is illustrated in **Fig.3.8**. The last lithography step was the use of mask no.6, on this purpose the source, drain and the gate contacts were connected to the large contact pads. The contact pads have the size of (500x500) µm². They had been electrically contacted with the IV- measurement device with probe needles or by soldering Au wires with In. **Fig.3.8b** shows the final MISHFET device.

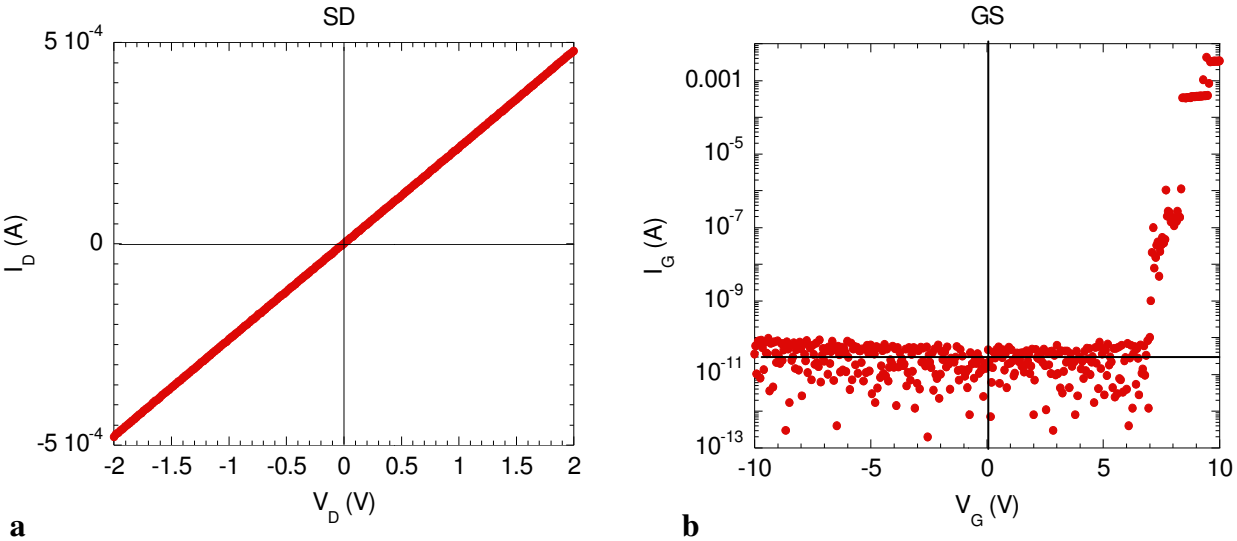
The large contact pads were isolated by SiO_2 from the high conductive 3C-SiC substrate, and were connected to source, drain and gate.



a **b**

Figure 3.8a *UV-lithography mask no.6 for the MISHFET production;* **b** *Photograph showing source, drain and gate connected to the large contact pads*

To prove that the insulation layer was removed from the source and drain, contacts IV measurements were done. The result is shown in **Fig.9a**: The IV curve shows a symmetrical, ohmic behavior. On the other hand the gate to source IV- measurement showed a rectifying behavior, shown in **Fig.9b**. The current between -10 V and 7 V was below 0.07 nA, so the transistor device was switchable in this wide voltage range without noticeable current flow through the gate contact.



a **b**

Figure 9a *Ohmic IV-curve measured between source and drain;* **b** *A typical IV-curve of a MIS diode, measured between gate and source*

4. Theoretical background of the field effect device

In this chapter the theoretical background of the field effect transistor device will be discussed and the basic device structure gets introduced. The structure and the voltage polarities shown here are for an n-channel HFET. The polarities are inverted in case of a p-channel. Current-voltage characteristics are derived.

4.1 Basic device structure

A schematically drawing of a HFET device is illustrated in **Fig.4.1**. The HFET consists of a c-AlGaN/GaN hetero-junction grown on 3C-SiC substrate.

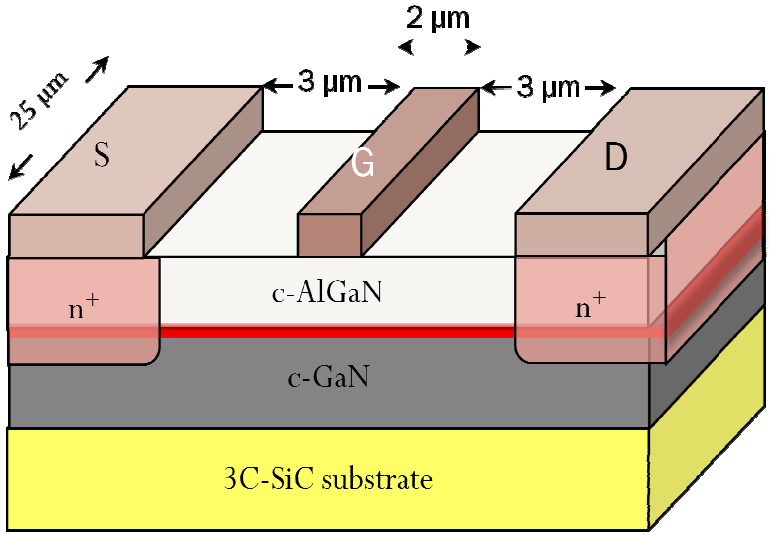


Figure 4.1 *Schematically drawing of a HFET device*

The c-GaN buffer layer is assumed to form an electrical shield towards the high conductive substrate. A detailed description of the electrical isolation to the substrate is given in section 6.2. The c-AlGaN layer is unintentionally doped with a donor background concentration in the range of (0.5-3) x10^{18} cm^{-3}. The 2DEG formed at the hetero-interface is the conductive channel of the transistor device. The channel is provided with two ohmic contacts, one acting as the source and the other as the drain. The n^+-regions under the ohmic contacts are formed by alloying the contact metals by RTA. When a positive voltage V_D is applied to the drain with respect to the source, electrons flow from source to drain. The carrier sheet density and consequently the channel conductivity are controlled by the gate bias V_G. The gate forms a rectifying junction with the channel. The gate electrode is of a Schottky- or of a MIS-type, forming a depletion zone into the c-AlGaN/GaN hetero-structure. MISHFET or HFET devices are voltage controlled resistors, and the resistance is controlled by varying the width of the depletion layer extending into the channel region. Increasing of the positive bias applied to the gate electrode the depletion zone decreases and causes higher channel

conductivity. By increasing the negative gate bias increases the depletion width. This causes a decrease of the channel conductivity and a pinch-off occurs at a certain negative gate voltage. The basic device dimensions are the channel length L_G, channel width Z, channel depth a, and depletion depth h. The source electrode is grounded, and the drain and gate electrodes are measured with respect to the source. When $V_G = V_D = 0$ the transistor is in equilibrium and no current flows. For a given V_G the channel current increases as the drain voltage increases. Eventually, for sufficient large V_D, the current will saturate at the value I_{Dsat}.
The basic current-voltage characteristics of a HFET are shown in **Fig.4.2** where drain current is plotted vs. drain voltage at different gate voltages. The difference of a normally-on (enhancement- mode **Fig.4.2a**) and a normally-off (depletion- mode **Fig.4.2b**) is depicted.

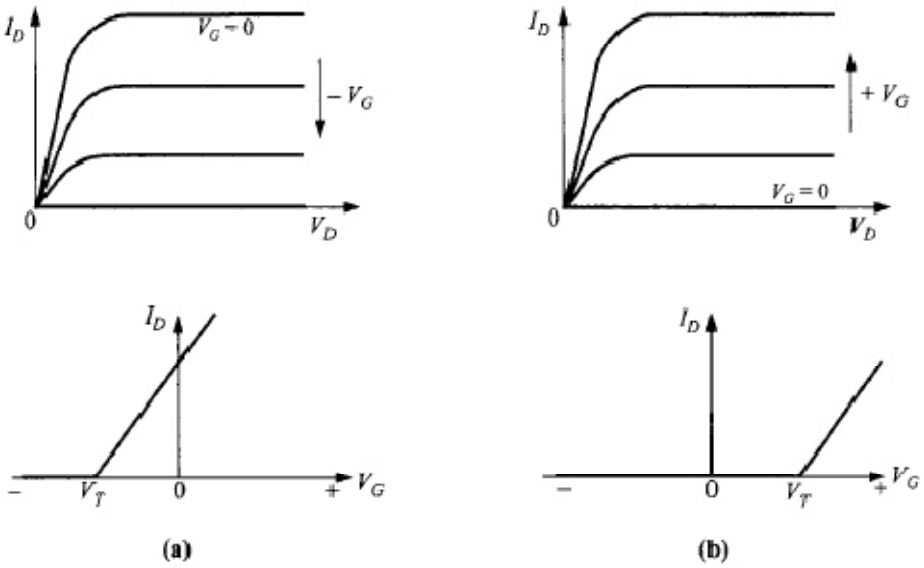


Figure 4.2 *Comparison of IV-characteristics:* **a** *normally-on HFET;* **b** *normally-off HFET* [48]

The output and transfer characteristics are compared. In case of an enhancement-mode transistor, the conduction of the electron channel is low and a positive gate voltage must be applied to fill the channel with carriers and so to increase channel conductivity. The counterpart is the depletion-mode device, if the channel is conductive with zero gate bias. Negative gate voltage must be applied to turn the transistor off. The IV-characteristics can be divided into two regions: The linear region, where the drain voltage is small and I_D is proportional to V_D; and the saturation region, where the current remains essentially constant and is independent of V_D. In case of a normally-off transistor device, as the reverse gate bias increases the saturation current I_{Dsat} decreases. This decrease occurs because of the reduced initial channel width, which results in larger initial channel resistance. Considering the transfer characteristics of normally-on and normally-off devise operation, the main difference is the shift of threshold voltage along the V_G axis. The normally-off device has no current conduction at $V_G = 0$, and the current increases as the gate voltage is bigger than the threshold voltage V_T.

4.2 Current-Voltage Characteristics

To derive the current-voltage characteristics for a long channel HFET, it means gate length L_G>> channel depth a, therefore the following assumptions have to be done:

1. gradual channel approximation
2. abrupt depletion layer
3. constant mobility

For an arbitrary charge distribution in the channel region the charge $Q(h)$ is given by the following integral expression:

$$Q(h) = \int_0^h \rho(y)\, dy \tag{4.1}$$

Where $\rho(h)$ is the charge density within the depletion zone. The dependence of the reverse bias voltage $V(h)$ on the depletion zone depth h and $\rho(h)$ can be derived from Poisson´s equation as follows:

$$F_y = -\frac{\partial V(y)}{\partial y} = \frac{1}{\varepsilon_S} \cdot \int_0^y \rho(y')\, dy' + c \tag{4.2}$$

The integration constant c can be determined from the boundary condition that $F_y = 0$ at $y = h$ for an abrupt depletion layer and is obtainable from **equ.(4.1)**, it becomes to:

$$c = -\frac{1}{\varepsilon_S} \cdot \int_0^h \rho(y)\, dy \tag{4.3}$$

Thus the derivation of the applied bias voltage $V(y)$ with respect to the channel depth y becomes:

$$\frac{\partial V(y)}{\partial y} = \frac{1}{\varepsilon_S} \cdot \left[\int_0^h \rho(y)\, dy - \int_0^y \rho(y)\, dy \right] = \frac{1}{\varepsilon_S} \left[Q(h) - Q(y) \right] \tag{4.4}$$

To obtain the voltage $V(h)$ predominating within the depletion layer **equ.(4.4)** has to be integrated from $y = 0$ to $y = h$. The voltage is now given by:

$$V(h) = \frac{1}{\varepsilon_S} \cdot \left[h \cdot Q(h) - \int_0^h Q(y)\, dy \right] = \frac{1}{\varepsilon_S} \cdot \int_0^h y \cdot \rho(y)\, dy \tag{4.5}$$

The maximum value for the upper limit of the integration occurs at $h = a$ (channel depth) and the corresponding voltage is the pinch-off voltage V_P.

Beyond this point the channel current remains essentially constant. The pinch-off voltage is given by:

$$V_P = V(h=a) = \frac{1}{\varepsilon_S} \cdot \int_0^a y \cdot \rho(y)\, dy \tag{4.6}$$

Differentiating **equ.(4.5)** yields:

$$\frac{\partial V(h)}{\partial h} = \frac{h \cdot \rho(h)}{\varepsilon_S} \tag{4.7}$$

It shows that the voltage change required moving the depletion boundary a given distance, increases with the value *h* and is proportional to the space-charge density at that boundary. The junction capacitance under the gate contact is given by:

$$C = A \cdot \frac{dQ(h)}{dV} = A \cdot \left(\frac{dQ}{dh}\right)\left(\frac{dh}{dV}\right) \tag{4.8}$$

Where *A* is the gate contact area. The depletion layer thus acts as a plane capacitor with plate distance *h*, and the capacitance is independent of the charge distribution profile.
To derivate the current-voltage characteristics first, the drain current density has to be taken into account and is given by the ohmic law:

$$J_x = \sigma(x) \cdot F_x \tag{4.9}$$

Here $\sigma(x)$ is the conductance and F_x the electric field in x-direction caused by the source to drain voltage V_D. Thus the drain current I_D is given by:

$$I_D = Z \cdot \mu \cdot \frac{\partial V(x)}{\partial x} \cdot \int_h^a \rho(y)\, dy \tag{4.10}$$

or

$$I_D\, dx = Z \cdot \mu \cdot \left(\frac{dV(h)}{dh}\right) \cdot dh \cdot \int_h^a \rho(y)\, dy \tag{4.11}$$

Where μ is the electron mobility and Z the channel width. Substituting **equ.(4.7)** and integrating with the boundary conditions $h = y_1$ at $x = 0$ and $h = y_2$ at $x = L$ leads to **equ.(4.12)**:

$$\int_0^L I_D\, dx = I_D \cdot L = \frac{2 \cdot Z \cdot \mu}{\varepsilon_S} \cdot \int_0^L h \cdot \rho(h)\, dh \cdot \int_h^a \rho(y)\, dy \tag{4.12}$$

Finally the drain current is given by:

$$I_D = \frac{2 \cdot Z \cdot \mu}{\varepsilon_S \cdot L} \cdot \int_{y_1}^{y_2} \left[Q(a) - Q(h) \right] \cdot h \cdot \rho(h)\, dh \tag{4.13}$$

Equation (4.13) is the basic equation of the long channel HFET. The transconductance g_m, defined as the derivative of the drain current I_D with respect to the gate voltage V_G can be obtained from **equ.(4.13)**. It is:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{\partial I_D}{\partial y_1} \frac{\partial y_1}{\partial V_G} + \frac{\partial I_D}{\partial y_2} \frac{\partial y_2}{\partial V_G} \tag{4.14}$$

The partial derivates are obtained from **equ.(4.7)** and **equ.(4.13)**:

$$g_m = \frac{2 \cdot Z \cdot \mu}{L} \cdot \left[Q(y_2) - Q(y_1) \right] \tag{4.15}$$

Which shows that g_m is equal to the conductance of the rectangular section of the semiconductor extending from $y = y_1$ to $y = y_2$.
In the case of an uniform charge distribution **equ.(4.13)** becomes:

$$I_D = \frac{Z \cdot \mu \cdot q^2 \cdot N_D^2 \cdot a^3}{6 \cdot \varepsilon_S \cdot L} \cdot \left\{ \frac{3 \cdot V_D}{V_P} - 2 \cdot \left[\frac{\left(V_D + V_G + V_{bi} \right)^{3/2} - \left(V_G + V_{bi} \right)^{3/2}}{V_P^{3/2}} \right] \right\} \tag{4.16}$$

V_{bi} is the built in voltage caused by the Schottky- or the MIS-contact, N_D is the effective density of states in the conduction band. The transconductance is given by the following expression:

$$g_m = \frac{2 \cdot Z \cdot \mu \cdot q \cdot N_D}{L} \cdot \left(y_2 - y_1 \right) \tag{4.17}$$

With depletion width at source (y_1) and drain (y_2):

$$y_1 = \left[\frac{2 \cdot \varepsilon_S \cdot \left(V_G + V_{bi} \right)}{q \cdot N_D} \right]^{1/2} \qquad x = 0 \tag{4.18}$$

$$y_2 = \left[\frac{2 \cdot \varepsilon_S \left(V_D + V_G + V_{bi} \right)}{q \cdot N_D} \right]^{1/2} \qquad x = L \tag{4.19}$$

A more detailed description of the current-voltage characteristics can be found elsewhere [47-48].

4.3 Design of a cubic AlGaN/GaN HFET

In contrast to the hexagonal AlGaN/GaN system there are no inherent, internal piezoelectric fields along the growth axis in cubic hetero-structures. The formation of the 2DEG is mainly caused by the background doping of the c-AlGaN barrier- and the c-GaN buffer-layer. The n-type unintentional background concentration is probably caused by the incorporation of oxygen impurities during the growth. SIMS measurements at c-GaN structures show clear incorporation of oxygen within the crystal matrix. A detailed description about the background doping concentration is given in chapter 6.2. The typical UID level N_D-N_A is (0.5-2) x10^{18} cm^{-3} and (1-3) x10^{17} cm^{-3} in c-AlGaN and c-GaN, respectively. The properties of the HFET device depend on the concentration of the 2DEG at the hetero-interface. In this chapter section the influence on the 2DEG electron concentration is discussed. Using Poisson-Schrödinger-solver software [57] the two dimensional electron concentrationn_{2DEG} at the c-AlGaN/GaN hetero-interface was calculated. The amount of the electron accumulation at the hetero-interface depends on parameter like the background donor concentration N_D–N_A in c-AlGaN and c-GaN, the thickness t of the barrier- and the buffer-layer, and the Al content x within the $Al_xGa_{1-x}N$ layer. **Fig.4.3** shows the calculated n_{2DEG} concentration as a function of the background donor concentration of the c-GaN buffer.

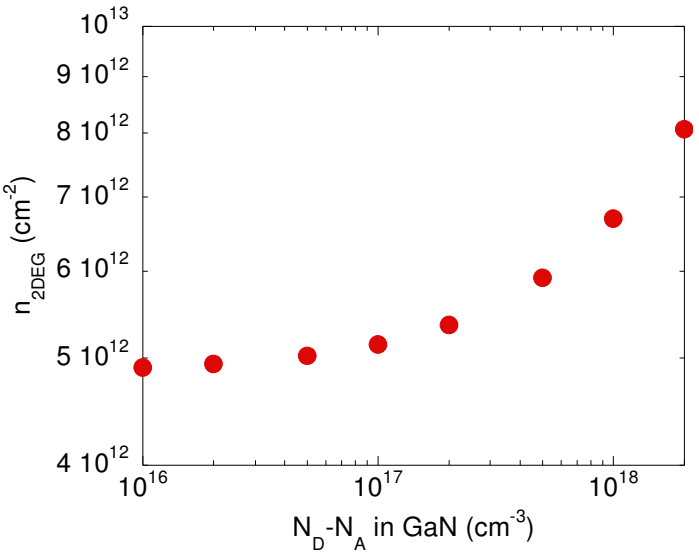


Figure 4.3 *Two dimensional electron gas (n_{2DEG}) concentration at the c-$Al_{0.3}Ga_{0.7}N$/GaN hetero-interface as a function of the background doping concentration ($N_D – N_A$) of the c-GaN buffer layer. Buffer layer thickness is 600 nm, barrier layer thickness is 30 nm, c-AlGaN doping concentration is 5x10^{17} cm^{-3}*

The donor surplus concentration N_D-N_A within c-GaN was varied between 1x10^{16} cm^{-3} and 2x10^{18} cm^{-3}. In case of the lowest assumed donor surplus concentration of 1x10^{16} cm^{-3} in c-GaN buffer layer the two dimensional electron gas concentrationn_{2DEG} amounts 5x10^{12} cm^{-2}.The two dimensional concentration increases to 8x10^{12} cm^{-2} increasing the donor concentration in c-GaN by more than two orders of magnitude. The result shows that

increasing the donor concentration in c-GaN is not an effective way to control the two dimensional electron gas accumulations at the c-AlGaN/GaN hetero-interface in a wide range. The main result is the fact that reducing the background donor concentration in the c-GaN layer does not have a significant effect on the 2DEG concentration. A reduced donor concentration was for example achieved by carbon doping as it is explained in chapter 6 more detailed.
Another important parameter of the c-AlGaN/GaN hetero-structure is the thickness of the c-AlGaN barrier layer. In **Fig.4.4** the 2DEG concentration dependence on the c-AlGaN barrier layer thickness is depicted. Thickness was varied between 10 nm and 50 nm.

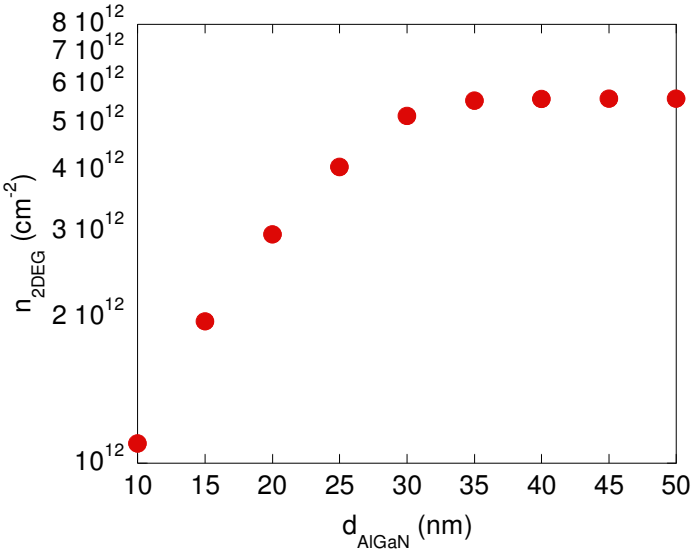


Figure 4.4 *Two dimensional electron gas (n_{2DEG}) concentration at the c-$Al_{0.3}Ga_{0.7}N$/GaN hetero-interface as a function of the thickness (d_{AlGaN}) of the c-AlGaN barrier layer. Barrier layer thickness is 30 nm, background donor concentrations in c-AlGaN and c-GaN are $5x10^{17}$ cm^{-3} and $1x10^{17}$ cm^{-3}, respectively*

Up to a thickness of 30 nm the two dimensional electron concentration increases exponentially by increasing the thickness factor of six. This result shows that the amount of trapped electrons at the hetero-interface is a function of the volume, and on this purpose of the included amount of donors of the c-AlGaN layer. The 2DEG concentration saturates increasing the c-AlGaN thickness from 30 nm to 50 nm. This behaviour can be explained consulting the diffusion length of electrons in cubic group III- nitrides. The diffusion length is in the range of 30 nm in c-GaN [58], so increasing the barrier thickness above 30 nm does not affect the 2DEG concentration. Further increasing the thickness of the barrier layer is not practicable for ohmic contact fabrication. To ensure that the contact metal contacts the 2DEG during the RTA process the barrier thickness has to be chosen appropriate. On this purpose a thickness between 20 nm and 30 nm of the c-AlGaN layer was preferred in this work. In this thickness range the 2DEG can be affected by a factor of two.
In **Fig.4.5** n_{2DEG} is plotted as a function of the Al mole fraction x within the barrier layer at a given barrier thickness and background donor concentrations

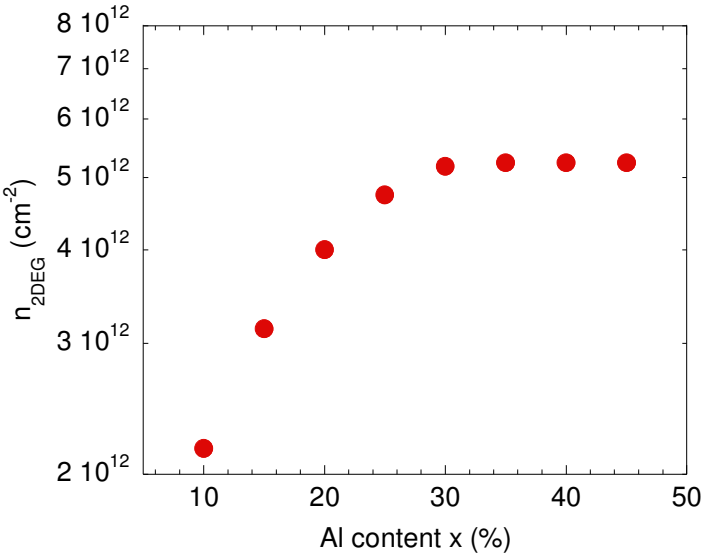


Figure 4.5 *Two dimensional electron gas (n_{2DEG}) concentration at the c-$Al_{0.3}Ga_{0.7}N$/GaN hetero-interface as a function of the Al content x. Barrier layer thickness is 30 nm, background donor concentrations in c-AlGaN and c-GaN are 5x10^{17} cm^{-3} and 1x10^{17} cm^{-3}, respectively*

Aluminium content was varied between 10 % and 50 %. The graph of the n_{2DEG} vs. x function is similar to that shown in **Fig.4.4**. Below an Al concentration of 30 % the two dimensional electron concentration increases exponentially. The increase is caused by the increased potential pocket and so the capability for electrons at the c-AlGaN/GaN interface. The two dimensional concentration saturates at a value of about 5.2x10^{12} cm^{-2} with increasing the Al content from 30 % to50 %. A potential explanation for this result is that the potential trap for electrons is filled at 30 % Al content at its maximum, since the repulsive Coulomb interaction prohibits further electron accumulation. In this work Al concentrations were used between 10 % and 30 % for transistor applications. Growing c-AlGaN with Al concentration of more than 35 % directly on the c-GaN buffer leads to relaxation process which strongly affects the structural crystalline properties of the c-AlGaN layer resulting in a low transistor device performance. Varying the Al mole fraction between 10 % and 30 % the amount of the 2DEG concentration can be varied by a factor of two.

The influence of the donor concentration within the c-$Al_{0.3}Ga_{0.7}N$ barrier layer on the two dimensional electron accumulation at the hetero- interface is depicted in **Fig.4.6**. The values for $N_D - N_A$ were varied between 1x10^{17} cm^{-3} and 2x10^{19} cm^{-3}. The n_{2DEG} versus $N_D - N_A$ shows a nearly linear behaviour. The 2DEG concentration increases from 6x10^{11} cm^{-2} to 5x10^{13} cm^{-2} by two orders of magnitude. Thus the transistor behaviour, enhancement- or depletion-mode, can be mainly adjusted by the donor concentration within the c-AlGaN barrier. Also a δ-doping within the c-AlGaN layer can be used to increase the two dimensional electron density as described in ref. [59-60].

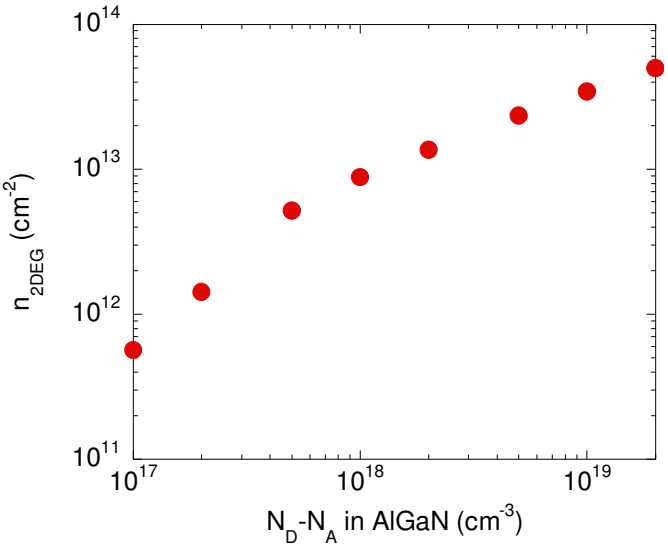


Figure 4.6 *Two dimensional electron gas (n_{2DEG}) accumulation at the c-$Al_{0.3}Ga_{0.7}N$/GaN hetero-interface as a function of the background doping concentration ($N_D - N_A$) of the c-AlGaN barrier layer. Barrier layer thickness is 30 nm, background donor concentration in the c-GaN buffer layer is 1x10^{17} cm^{-3}*

The combination of the discussed parameter is now used to design the field effect transistor device. **Fig.4.7 a** and **b** shows examples of the conduction band edge characteristic (red continuous line) and the distribution of electron concentration (blue dashed line) at the hetero-interface for a normally-on and a normally-off HFET, respectively. The continuous black line at 0 eV marks the Fermi level E_F. A Schottky barrier is applied to the structure surface to simulate gate conditions. The barrier height is 0.8 eV. No additional doping was used simulating both structures. The UID concentrations within c-AlGaN barrier layer and c-GaN buffer layer were assumed to be 5x10^{17} cm^{-3} and 1x10^{17} cm^{-3}, respectively. Thus the difference between normally-off and normally-on transistor devices determined only by the c-$Al_xGa_{1-x}N$ barrier layer. In case of normally-on HFET (**Fig.4.7a**) the thickness of the barrier layer is 30 nm, Al content amounts x = 0.35. Normally-off transistor (**Fig.4.7b**) consists of a thinner 15 nm thick c-AlGaN layer with an Al mole fraction of x = 0.15. As described above a larger barrier layer volume supplies more electrons to the c-AlGaN/GaN interface channel. A second important factor is the depletion width of the Schottky barrier, in case of the thin 15 nm barrier electrons are completely depleted from the interface. The third factor is the larger conduction band offset in c-$Al_{0.35}Ga_{0.65}N$/GaN sample generating an energetically deeper potential trap, compared to c-$Al_{0.15}Ga_{0.85}N$, for electrons. The result is that at zero bias at the Schottky contact the 2DEG within the normally-on device is in the range of 1x10^{12} cm^{-2}, while the 2DEG within the normally-off device is completely depleted.
All these theoretical results were taken into account to design and realize transistor devices presented in chapter 7.

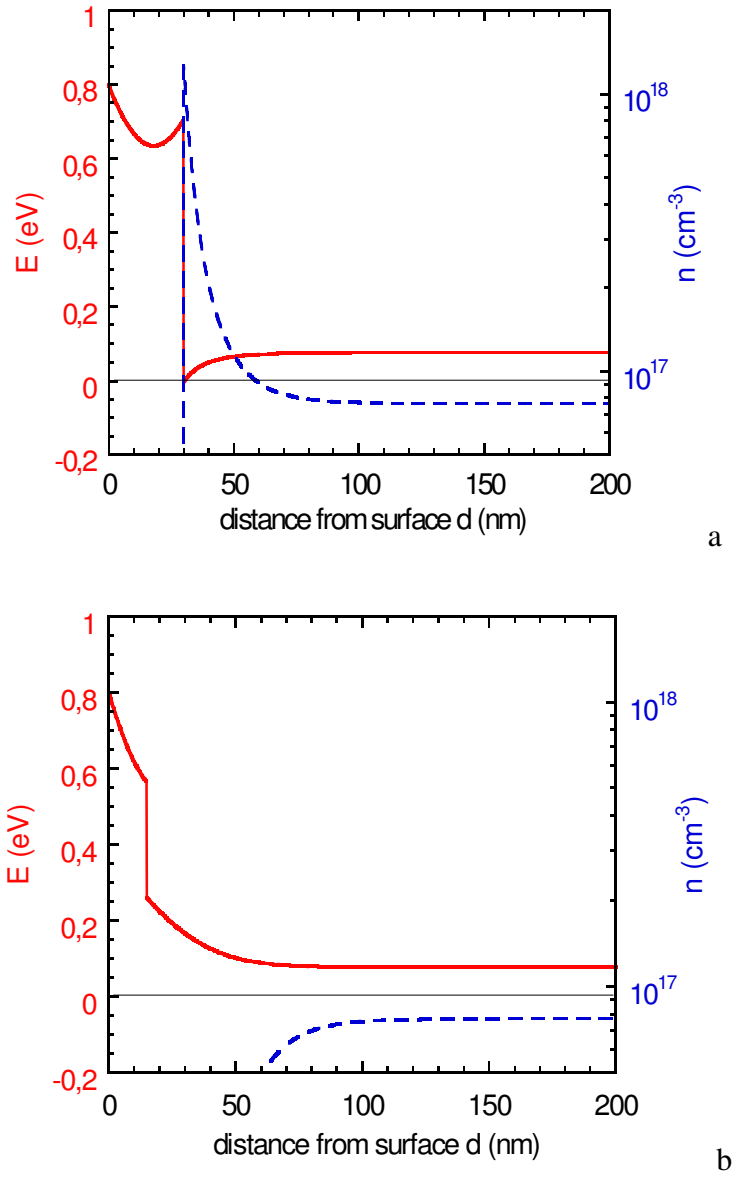


Figure 4.7 *1D Poisson calculation of the conduction band edge and electron concentration in c-AlGaN/GaN structures, gate conditions are simulated by a Schottky barrier of 0.8 eV applied to the sample surface* **a** *normally-on condition and* **b** *normally-off condition*

5. Suppression of Gate Leakage Current

Two types of insulators, namely Si_3N_4 and SiO_2 are compared. Also two types of insulator deposition methods are discussed. The main focus of this chapter is given to deposition of Si_3N_4 on c-GaN material. Especially the *in-situ* deposition process within the MBE chamber is discussed in detail.

5.1 Si_3N_4 as the gate insulator

Si_3N_4 layers were deposited *in-situ* on top of cubic GaN grown on 3C-SiC (001) substrates. The electric characteristics of the MIS structures are determined by current voltage measurements and by capacitance and admittance spectroscopy techniques. Time of flight secondary ion mass spectroscopy (TOF-SIMS) was used to investigate the composition of our samples.

From the flat band voltage in the MIS capacitors and a detailed band diagram analysis the conduction band discontinuity of Si_3N_4 and cubic GaN was evaluated to be 1.17 eV which is slightly lower than reported for hexagonal GaN [61]. By admittance spectroscopy interface state densities are calculated. Current-voltage characteristics were used to evaluate the influence of the substrate temperature on the insulating properties of the MIS structures.

In the described experiments two kinds of sample structures were investigated. In the first series the 600 nm thick c-GaN layers were taken out of the MBE chamber and Si_3N_4 layers were deposited by PECVD at a substrate temperature of 300 °C. The deposited insulator thickness was estimated from the saturation region of the CV curves assuming a dielectric constant of 7.5 for Si_3N_4 [48]. In the second series Si_3N_4 layers were deposited *in-situ* in the MBE chamber directly after the growth of the c-GaN buffer using the nitrogen plasma source and the silicon thermal evaporation source. The growth temperature of the Si_3N_4 layers was varied between 300°C and 700°C. The growth rate, which lay between 13 nm/h and 15 nm/h, was estimated from CV characteristics. The background pressure during the growth was $7x10^{-6}$ mbar and the atomic fluxes of atomic nitrogen and silicon were $2x10^{14}$ $cm^{-2}s^{-1}$ and $1.8x10^{15}$ $cm^{-2}s^{-1}$, respectively. Using standard lithography circular contact structures with a diameter of 100 µm were placed on top of the insulating layer. Metal gate contacts were thermally evaporated consisting of 15 nm Ni and 50 nm Au. The ohmic back contacts were realized by soldering the highly conductive 3C-SiC on Cu plates with In. The dc bias was varied from deep depletion to accumulation and back to deep depletion. An ac-amplitude of 50 mV was used. Interface trap density values D_{it} have been extracted by admittance spectroscopy.

Typical CV curves of c-GaN MIS structures measured at 1 MHz, at room temperature (RT), are shown in **Fig.5.1**. The bias voltage was varied from deep depletion (-10 V) to accumulation (+10 V). The accumulation capacitance was used to determine the equivalent insulator thickness (EIT) assuming a dielectric constant of 7.5 for Si_3N_4. The EIT of the MBE produced Si_3N_4 layers as a function of the deposition time are shown in the inset in **Fig.5.1**. The thickness of the silicon nitride layers increases linearly with the deposition time. From the slope of the linear approximation a growth rate of about 13.9 nm/h was estimated.

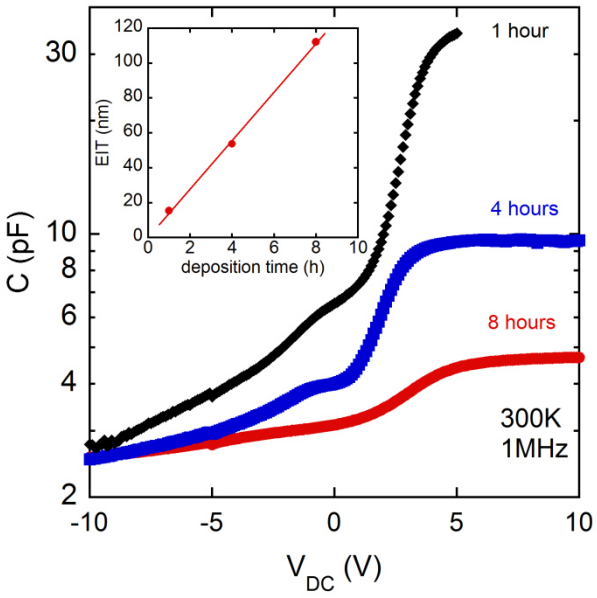


Figure 5.1 *Measured capacitance of the Si_3N_4/c-GaN capacitors versus the applied dc voltage; results of three grown structures are shown; growth temperature was 300 °C, the deposition time was varied from one to eight hours; the inset shows the linear function of the equivalent insulator thickness (EIT) as a function of the deposition time; the growth rate is 13.9 nm/h*

For negative bias voltages no inversion capacitance is observed. With decreasing voltage the capacitance drops and does not saturate. This deep depletion feature is typical for wide band gap semiconductor MIS structures, because the generation rate of the minority carriers (holes) is extremely low at room temperature. Due to the large time constant resulting from an extremely low generation rate of holes the electron quasi-Fermi level will remain unchanged.
Using **equ. (2.8)** the net donor concentration was calculated from the capacitance voltage characteristics for each structure.
The flat band voltage in the cubic GaN for each of the structures was derived from the donor concentration-voltage diagrams. **Fig.5.2** shows the calculated N_D-N_A versus applied bias voltage of each MIS structure near the flat band voltages (from -5V to+7V).The applied dc voltage is interrelated with the depletion width of the MIS structure. For the negative voltages a constant net donor concentration of approximately $1x10^{17}$ cm^{-3} is measured which is attributed to the background donor concentration of the unintentionally doped (UID) cubic GaN. This residual background carrier concentration is the same for all our samples and is indicated in **Fig.5.2** by the grey horizontal line. For a direct estimation of the flat band voltage V_{fb} the donor concentration is plotted versus the applied dc voltage instead of the depletion depth. In this way the exponential increase of N_D-N_A in the strong accumulation regime at positive bias can be used to determine the flat band voltage from the intercept point of the measured curves with the grey line, which correspond to the background doping in the semiconductor. In addition, at approximately 0 V, an additional charge accumulation is detected with a maximum of charge carriers of about $3x10^{17}$ cm^{-3}, which may be due to defect states at the surface of the c-GaN.

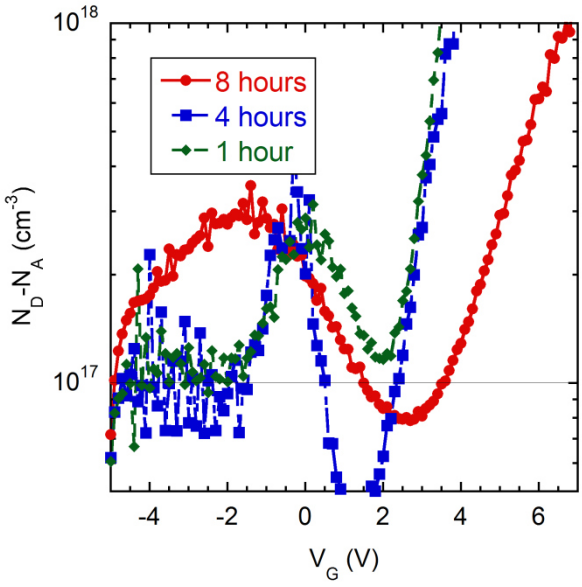


Figure 5.2 *Net donor concentration vs. the applied dc voltage; N_D-N_A was calculated from the CV curves of each MIS structure using equation (2.8)*

Fig.5.3 shows the evaluated flat band voltage V_{fb} as a function of the insulator thickness t_{in}. The shift of the flat band voltage is a clear indication of charges in the insulator. The experimental V_{fb} vs. t_{in} data points plotted in **Fig.5.3** show an increase of the flat band voltage with the insulator thickness.

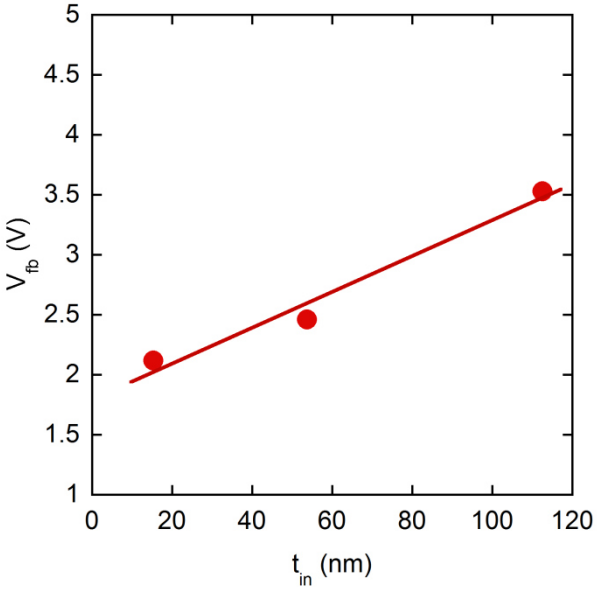


Figure 5.3 *Flat band voltage data (red dots) as a function of the insulator thickness; V_{fb} increases with the insulator thickness t_{in}*

An energy band diagram analysis is used to understand the physical properties of the interface. **Fig.5.4** shows a qualitative conduction band diagram of the MIS capacitors with different oxide thicknesses at flat band condition.

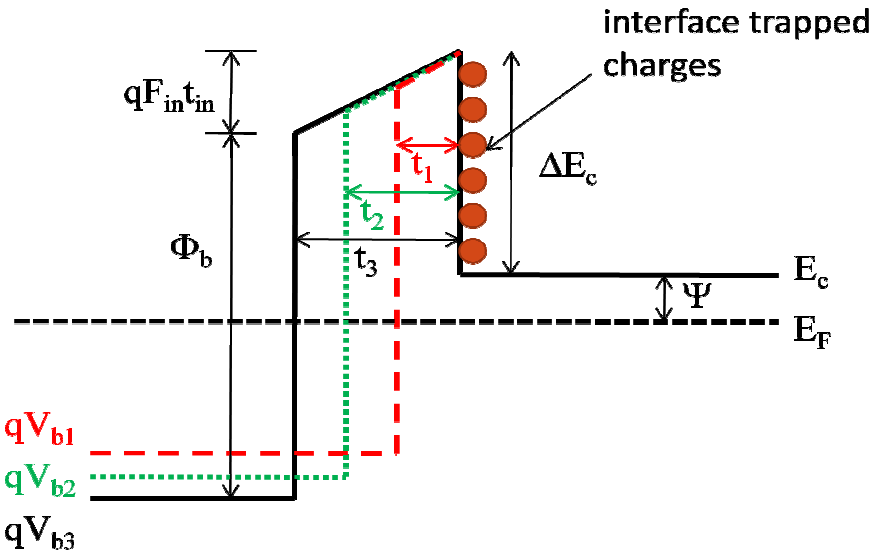


Figure 5.4 *Schematically drawing of the conduction band alignment of a Ni/Si_3N_4/c-GaN metal insulator semiconductor structure with different insulator thickness*

For a better overview the energy separation of the conduction band and the Fermi level Ψ is just shown for the structure with the insulator thickness t_3 (black full curve)V_g is the flat band gate bias for each thickness t_{in}, ϕ_b the energy barrier height at the Ni/Si_3N_4 interface, F_{in} the electric field in the silicon nitride layer, ΔE_c the conduction band discontinuity between Si_3N_4 and c-GaN, ψ the energy separation of the conduction band from the Fermi level in the cubic GaN layer, and q is the single electron charge. Assuming an interfacial charge at the Si_3N_4/c-GaN interface, a simple analytical expression relating the applied flat band voltage to the interfacial parameters can be derived from **Fig.5.4**:

$$qV_{fb} = qF_{in}t_{in} + (\phi_b - \Delta E_C - \psi) \qquad (5.1)$$

Where V_{fb} is the flat band voltage for the given insulator thickness t_{in}. Assuming a fixed interface trapped charge and a linear increase of the flat band voltage with the insulator thickness (**Fig.5.3**), the electric field dropping across the insulator at flat band condition is 0.148 MV/cm and the (ϕ_b - ΔE_C - ψ) band offset is 1.807 eV. The non-zero electric field dropping across the Si_3N_4 insulation layer can be attributed to a net negative charge at the Si_3N_4/c-GaN interface, of approximately 6.1×10^{11} cm^{-2}. Based on the doping density, the conduction band distance from the Fermi level ψ is estimated to be 75.9 meV. Assuming a work function of 5.15 eV for Ni [48] and an electron affinity of 2.1 eV for Si_3N_4 [61] the barrier height at the Ni/Si_3N_4 interface is 3.05 eV. Thus a conduction band discontinuity to be ΔE_C = 1.17 eV is found. This value is slightly lower compared to the value of 1.3 eV for hexagonal GaN reported in ref. [61].

The following discussion is affected to the influence of the substrate temperature during the deposition of the Si_3N_4 layers on their electrical properties. Five silicon nitride layers on top of c-GaN samples were grown at temperatures between 300 °C and 700 °C in 100 °C steps. The deposition duration was one hour for each sample, so the Si_3N_4 layers have approximately the same thickness. In **Fig.5.5** current voltage characteristics of the MIS capacitors are shown to illustrate the effect of insulation.

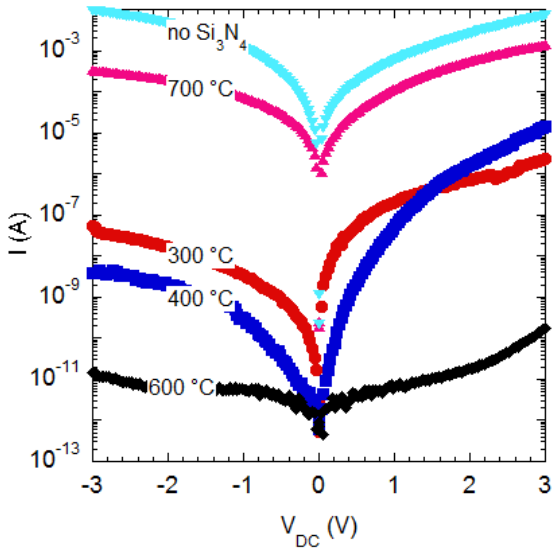


Figure 5.5 *Current voltage characteristics of the MIS capacitors with Si_3N_4 as insulator grown at different temperatures; to illustrate the effect of insulation the IV curve of a metal/semiconductor is also shown (no Si_3N_4)*

A simple metal-semiconductor reference sample was also measured (no Si_3N_4). For positive bias voltages a clear reduction of the current flow by three orders of magnitude for the MIS structures grown at 300 °C and at 400 °C compared to the reference sample is observed. The sample grown at 600 °C shows a conductivity minimum. Within the measured voltage range the current is in the range of 0.1nA at +3 V. This value is more than seven orders of magnitude lower as measured for the reference sample. The sample grown at 700 °C shows an insufficient insulation and the current is only a factor of five lower than for the sample without an insulator at +3 V.

The current in reverse voltage direction depends also on the Si_3N_4 growth temperature and decreases with higher temperatures. In the sample grown at 600 °C the current is reduced to a minimum of 1.5 x 10^{-11} A at -3 V. The sample grown at 700 °C shows nearly the same conductivity like the reference sample. Supposedly the reason for this behaviour is due to the high growth temperature which is only 20 °C beneath the growth temperature of cubic GaN. Although the exact nature of this effect is still unknown, a diffusion of Si atoms into the c-GaN layer, acting as shallow donors, may explain the insufficient insulation and further investigations have to be done in future works. From the increase of the IV curves in forward

direction the serial conductance $1/R_S$ was calculated. **Fig.5.6** shows the results with a clear conductivity minimum in the sample produced at 600 °C.

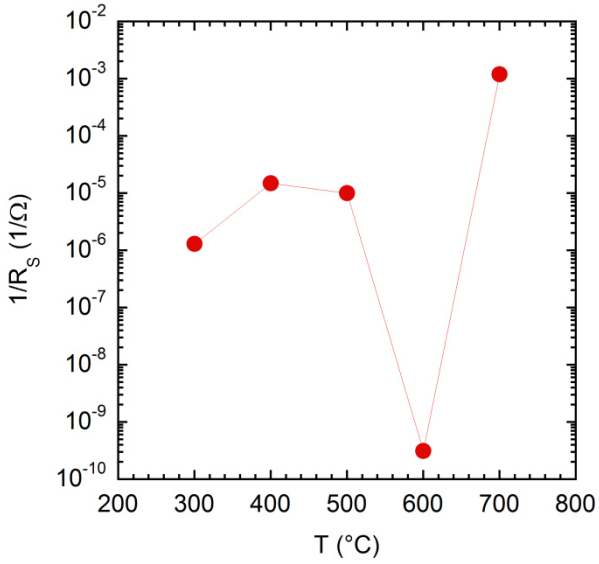
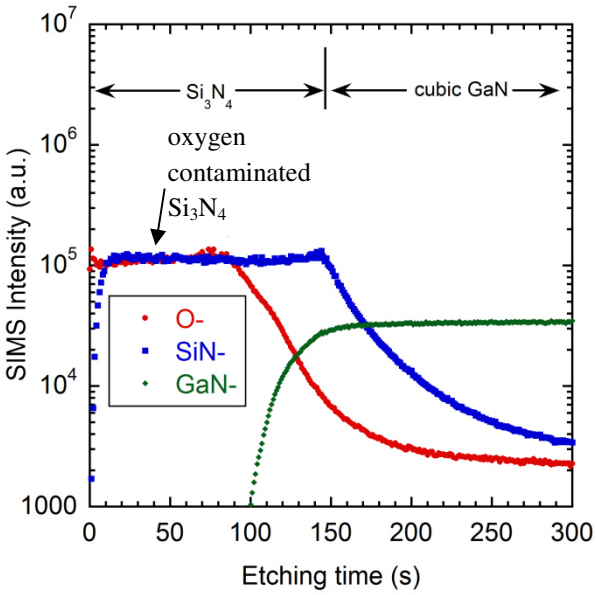
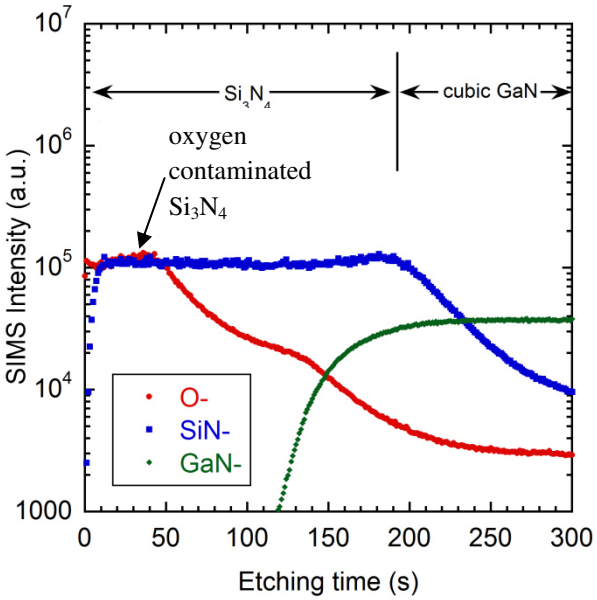


Figure 5.6 *Calculated serial conductivity $1/R_S$ of the MIS capacitors; a minimum of conductivity is reached in the MIS structure grown at 600 °C*

Two further investigations were performed to understand the conductivity minimum in the MIS structure with Si_3N_4 grown at 600 °C. In the first experiment time of flight secondary ion mass spectroscopy was conducted.TOF-SIMS measurements were done by Dr. J. Gerlach from the IOM Leipzig. A pulsed 15 keV Ga^+ ion analysis beam and a pulsed 0.5 keV Cs^+ erosion beam were used. To avoid sample charging a pulsed electron shower was applied. The negative ion mass spectrum was measured. From this data a depth profile was made for selected, representative signals.
In **Fig.5.7** SIMS profiles of insulator c–GaN samples grown at 300 °C (**Fig.5.7a**) and at 600°C (**Fig.5.7b**) are depicted.



a



b

Figure 5.7 *SIMS profiles of Si_3N_4/c-GaN structures:* **a** *silicon nitride was grown at 300 °C and* **b** *at 600 °C; for a better overview only the signals for O (red curve), SiN (blue curve) and GaN (green) are shown*

The diagrams show the SIMS intensity plotted versus the sputtering time for oxygen (red dots), silicon nitride (blue squares) and the GaN signal (green diamonds). A silicon nitride layer was detected on top of the c-GaN layer. A noticeable incorporation of oxygen is measured in all samples. Probably this oxide contamination is formed during the exposition of the samples to the atmosphere after the MBE growth process, since the oxygen incorporation in the c-GaN layer is more than three orders of magnitude lower than in the Si_3N_4 layer. The oxygen contamination inside the c-GaN layer is due to residual oxygen in the nitrogen gas source, which is the same for the c-GaN growth and the Si_3N_4 growth. Since the nitrogen flux

was not changed for Si_3N_4, the growth rate between c-GaN and Si_3N_4 varies only by a factor of 10.The conclusion is that the oxide contamination does not originate from the growth process. At the surface SiO_2 or SiO_xN may be formed, the fraction of the oxygen contaminated Si_3N_4 decreases at higher deposition temperatures and is a function of $1/T$ as illustrated in **Fig.5.8**.

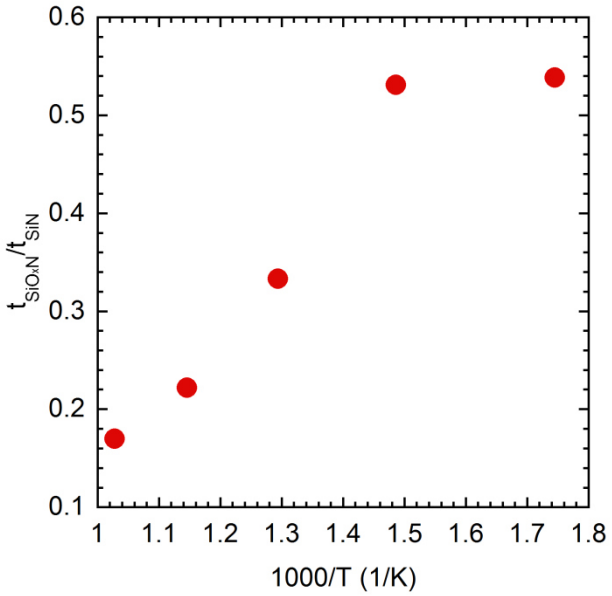


Figure 5.8 *Fraction of oxygen contaminated Si_3N_4 as a function of 1/T; at temperatures between 400 °C and 600 °C a nearly linear regime with 1/T is observed*

The oxygen contamination is probably due to the formation of SiO_2 and SiO_xN on the Si_3N_4 layers. With higher temperatures the porosity may decrease minimizing the oxide contamination and also the leakage current through the insulator. However, this approach does not explain the increase of the conductivity in the sample grown at 700 °C.

The second step of investigation is the flat band condition in the grown samples. As discussed in this section before the non-zero electric field dropping across the insulator is caused either by charges inside the insulator or by interface trapped charges at the Si_3N_4/c-GaN interface. To improve the insulating properties of the Si_3N_4 layer this parasitic charge should be reduced to a minimum. A hint of the reduction of these charges is a decrease of the flat band voltage. **Fig.5.9** shows CV characteristics of the samples which were reported in the IV analysis above (**Fig.5.5**).

A drop of the capacitance at zero bias is observed for the sample grown at 700 °C indicating that the ohmic regime becomes dominant in this structure at positive voltages. This observation fits very well with the high current in this sample (see **Fig.5.5**). The samples grown at 300 °C and 400 °C show a slightly lower accumulation capacitance than the samples grown at 500 °C and 600 °C that indicates a different insulator thickness. The Si_3N_4 thickness was calculated to be approximately 14 nm for the low temperature samples and 12 nm for higher temperatures. As reported in our discussion before, the flat band voltage was extracted from N_D-N_A vs. applied voltage profiles. The flat band voltage decreases with increasing the growth temperature and reaches a minimum in the sample grown at 600 °C.

In **Fig.5.10** the measured flat band voltage is plotted as a function of the inverse growth temperature (red circles).

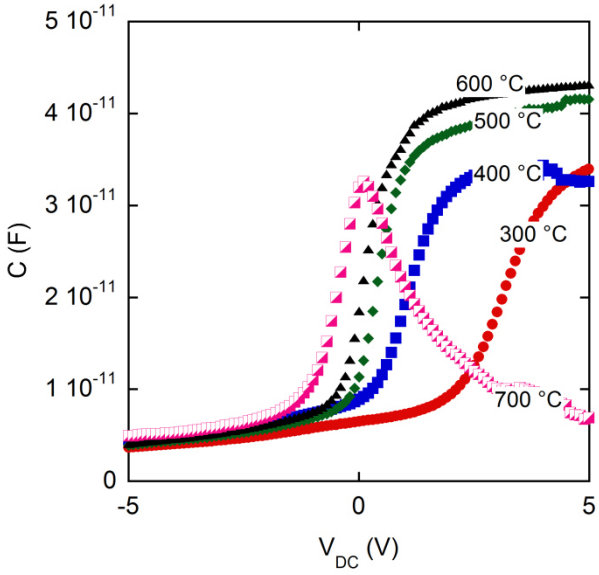


Figure 5.9 *Capacitance voltage characteristics of the MIS capacitors; the growth temperature for in-situ MBE grown Si_3N_4 was varied between 300 °C and 700 °C*

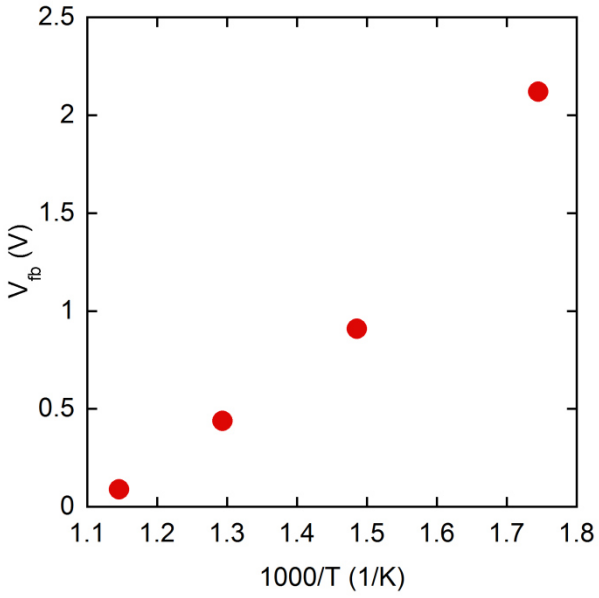


Figure 5.10 *Extracted values for the flat band voltages of the MIS capacitors as a function of the reverse growth temperature*

A nearly linear behaviour of V_{fb} vs. $1/T$ with a high degree of correlation is observed. Summarizing these results the flat band voltage is reduced to a minimum for Si_3N_4 grown at 600 °C. The consequence is the reduction of the non-zero electric field across the insulator. This may cause the outstandingly insulation properties of this layer.

5.2 SiO_2 as gate insulator

SiO_2 insulating layers were deposited by PECVD method. Two different types of SiO_2 were produced. The first type is deposited under high SiH_4 and N_2O fluxes, consequently the deposition rate was high it was 80 nm/min. To produce the second type of SiO_2 the gas fluxes were reduced (also compare with **Tab.3.2**), the deposition rate was 1.5 nm/min. The SiO_2 MIS diodes were compared with Si_3N_4 diodes by admittance spectroscopy.
In **Fig.5.11** the obtained density of interface states D_{it} is plotted versus energy of the trap level within the gap of c-GaN. For calculation **equ.(2.21)** was used.

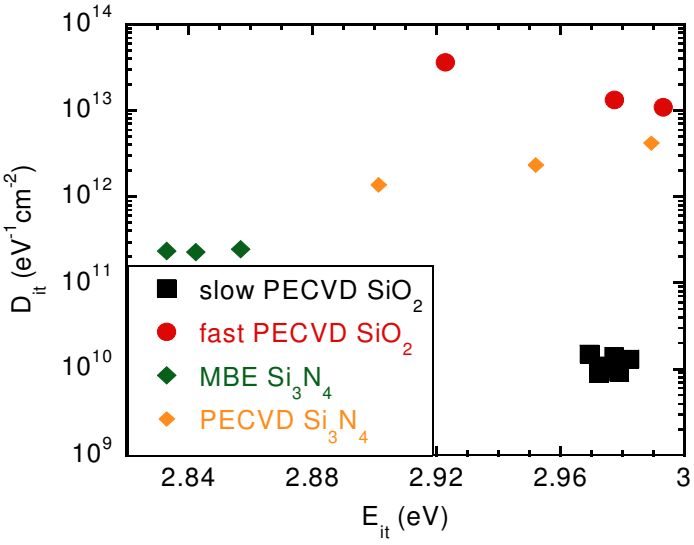


Figure 5.11 *Interface defect state densities D_{it} versus energy E_{it} within the band gap of c-GaN. The data from the MBE produced structure (green diamonds) are compared with PECVD produced Si_3N_4 (orange diamonds) fast deposition SiO_2 (red circles), and slow deposition SiO_2 (black squares) capacitors*

An increase of D_{it} (E_{it}) with increasing energy is observed in structures with Si_3N_4 produced by PECVD, indicating a distribution of interface defect levels at about 0.3 eV below the conduction band with a maximum trap density of about $2x10^{12}$ $cm^{-2}eV^{-1}$. In structures with Si_3N_4 produced by plasma assisted MBE the trap states seem to have less energy spread. A maximum trap density of $2.5x10^{11}$ $cm^{-2}eV^{-1}$ at about 0.4 eV below the conduction band edge is found. Thus growth of Si_3N_4 under high vacuum conditions in the MBE chamber directly after the growth of c-GaN reduces the interface trap density by more than one order of magnitude. Since the interface is not in contact with the atmosphere the incorporation of impurities causing traps or mobile charges in the Si_3N_4 layer is significantly reduced. In case of SiO_2 as the insulating layer the high flux PECVD produced layers show a maximum amount of defect states it is in the range of $1x10^{13}$ $cm^{-2}eV^{-1}$ and $4x10^{13}$ $cm^{-2}eV^{-1}$ [62]. On the other hand the reduction of the gas fluxes within the PECVD chamber produces SiO_2 layers with a minimum interface related defect states. The amount of the defect states is in the range of $(1\text{-}2)x10^{10}$ $cm^{-2}eV^{-1}$ the energetic position is around 0.22 eV below the conduction band

edge E_C. This extremely low interface trap concentration is the lowest ever reported in c-GaN/SiO_2 system. The value is comparable to the well investigated Si/SiO_2 system of 10^{10} $cm^{-2}eV^{-1}$ reported in [48]. Assuming a surface density of atoms of about 10^{15} cm^{-2} it means one interface trap per 10^5 surface atoms is present. This extremely low amount of interface traps is supposedly caused by the slow deposition method by PECVD at low SiH_4 and N_2O gas fluxes. At a deposition rate of 1.5nm/min, the c-GaN surface is passivated in an optimal way so the most interface traps could be neutralized. Since this is only an approach it needs further investigations to understand completely the c-GaN/SiO_2 interface effects.

Summarizing this chapter it should be mentioned that all the detected interface related defect states are located between 0.2 eV and 0.4 eV below E_C. We assume that these defects are caused by Ga dangling bonds which capture electrons and therefore act as acceptors. In the further work only the low interface traps SiO_2 insulating layers were used for MIS structures for gate application.

6. Electrical separation between the substrate and the HFET device

6.1 Carbonized Si substrates

One possibility to avoid parasitic substrate leakage current is the use of carbonised Si (001) substrates. The substrates were produced by the group of Dr. J. Pezoldt at the Technical University of Ilmenau. In any case, as already reported in [63] growth on the carbonized Si (001) substrates leads to an increase of the dislocation density of the cubic GaN layers, compared to the growth on free standing 3C-SiC. Additionally Hall-measurements on this substrates yield a p-type conductivity of the grown c-GaN layers. This feature is disadvantageous for n-type HFET realization. In this subchapter I will show that the amount of dislocations is correlated with the amount of the free hole concentration *p*.

Generally, dislocation lines are electrically charged so that the region surrounding a dislocation is either coulombically attractive or repulsive to a free carrier. The nature of the coulombic interaction depends on the polarity of the dislocation line and the polarity of the carrier. As an example, **Fig.6.1** shows a positively charged dislocation line which is attractive to electrons and repulsive to holes.

Initially, electrons are attracted but holes are repelled due to the potential created by the dislocation. However, the continued collection of electrons will screen the dislocation potential thereby reducing the repulsive barrier for holes. As a result free holes get over the potential barrier. The electronic states of the dislocation exist within the forbidden energy gap. Under applied bias holes are accelerated along the crystal while a large amount of electrons are captured in the dislocation line potentials. In this case holes are the predominating, the majority charge carriers.

Measuring rocking curves by HRXRD [37] of the grown c-GaN layers dislocation densities have been evaluated. To calculate the amount of the dislocation densities **equ.(2.7)** was used, thus the dislocation density is proportional to the square FWHM of the rocking curve.

To investigate the influence of the c-GaN buffer layer thickness on the dislocation density five samples with a thickness between 100 nm and 1300 nm were measured by HRXRD. The result is shown in **Fig.6.2**. Dislocation density decreases nearly linearly with increasing the layer thickness. In the investigated thickness range it decreases from 6.5×10^{10} cm^{-2} at 100 nm to 9×10^{9} cm^{-2} at 1300 nm by one order of magnitude. Due to self-annihilation of dislocation lines at certain layer thickness this result is not further surprising and is a well known feature [48].

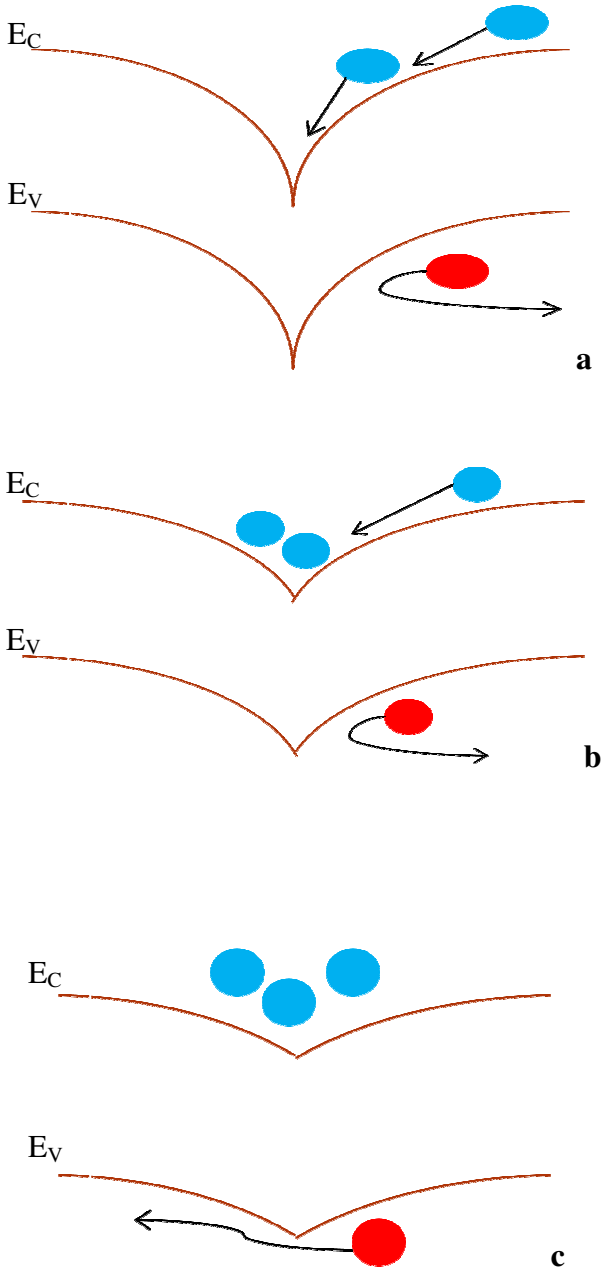


Figure 6.1 *Schematically drawing of the energetic conduction and the valence band in the surrounding of a positively charged dislocation line;* **a–c** *sequence shows electrons (blue circles) accumulating in the potential minimum thereby screening the dislocation potential and allowing holes (red circles) to bypass the potential barrier*

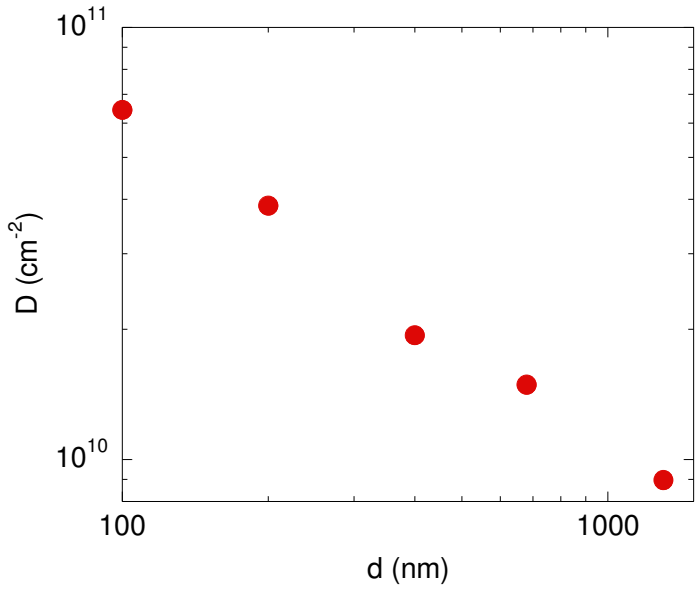


Figure 6.2 *Dislocation density D as a function of the c-GaN layer thickness d; the dislocation density values were calculated from the FWHM of the rocking curves measured by HRXRD*

To investigate the influence of the dislocation lines on electrical properties of the c-GaN layers Hall measurements were done and the results are illustrated in **Fig.6.3**.

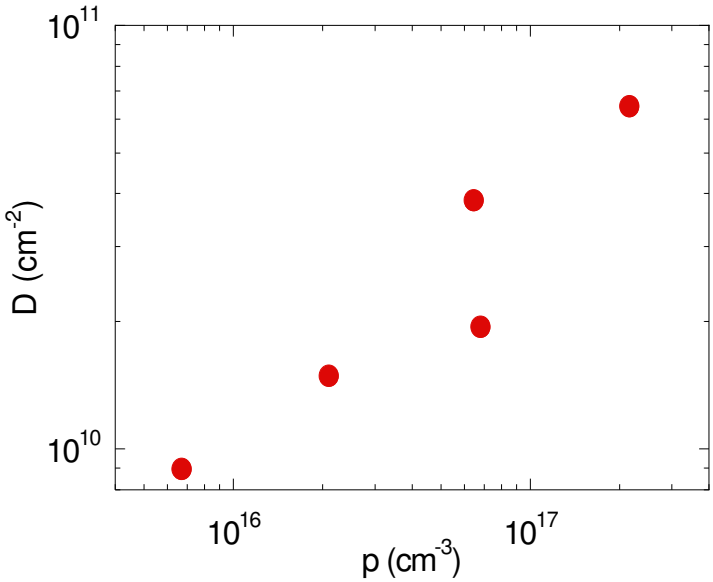


Figure 6.3 *Dislocation density D as a function of free hole concentration p measured by Hall-effect measurement*

Dislocation density D is plotted as a function of the free holes concentration p in a double logarithmic scale. In samples with high dislocation densities the amount of free positively charged carriers is increased. The $D(p)$ function shows a nearly linear behaviour, since the hole concentration is 6.5×10^{15} cm^{-3} in the sample with a dislocation density of 9×10^{9} cm^{-2}

(thickness d = 1300 nm) and increases to 2.1×10^{17} cm^{-3} in the sample with 6.5×10^{10} cm^{-2} (thickness d = 10 nm) dislocations. This clearly proved the dependency of free hole concentration on dislocation density and supports the assumption made before in this chapter. Dislocation lines in c-GaN grown on carbonized Si substrates are electrically charged and act as electron traps resulting in p-type conductivity.

However, for n-type c-AlGaN/GaN based HFET application, carbonized Si substrates are not suitable. Beside the p-type conductivity the high amount of threading dislocation lines in the range of 1×10^{10} cm^{-2} is disadvantageous for high mobility device application. The amount of dislocation lines is between 5 and 10 times higher compared to c-GaN layers grown on free standing 3C-SiC. Increasing the c-GaN layer thickness is one possibility to reduce the average number of dislocation lines. Disadvantages of this possible solution are increased hexagonal inclusions and an increased surface roughness by increasing c-GaN layer thickness. In general the surface roughness is two times higher compared to samples grown on free standing substrates. For example it is RMS = 8 nm measured on a 600 nm thick c-GaN sample grown on carbonized Si and it is RMS = 4 nm on c-GaN grown on 3C-SiC with the same thickness. Since the interface roughness is one of the most significant parameter which characterize high electron mobility devices, it is very important to have a smooth c-AlGaN/GaN interface. Summarizing all this facts about the growth of c-GaN on carbonized Si substrates our resume is that this substrate is not suitable for c-AlGaN/GaN HFET application. In the further subchapters 6.2 and 6.3 I will present alternative epitaxial methods to electrically separate the active device and the high conductive 3C-SiC substrate.

6.2 Carbon doping of c-GaN

Controlled p-type doping is crucial for advanced electronic and optoelectronic devices based on group-III nitrides, like hetero- junction bipolar transistors (HBTs), light emitting diodes (LEDs) or laser diodes (LDs) [64-65]. In HFETs, carbon doping can be used to reduce the conductivity of the UID GaN bulk layer, which typically shows n-type character.
In this chapter I report on doping experiments of GaN with cubic crystal structure. Compared to other dopants in cubic (Al) GaN materials, such as magnesium, carbon has a very low diffusion coefficient [66]. It is also known from p-doping in (Al) GaAs system that carbon doping is less sensitive on the composition of ternary compounds [67]. Carbon-tetra-bromide (CBr_4) has become widely used as carbon source in molecular beam epitaxy since high doping concentrations can be reached using CBr_4. Further on, no carrier gas is needed to transport the CBr_4 molecules to the sample surface and a CBr_4 doping system can be easily incorporated into the MBE without modifying the existing pumping system.
This chapter is subdivided in four parts. In the first part **a** the MBE growth of c-GaN:C is described and SIMS results of the grown c-GaN:C samples are presented in part **b**. The quantification of incorporated carbon is discussed. Part **c** contains electrical qualification of the c-GaN:C samples by CV measurements. The discussion of the results includes both the donor compensation effect of the n-type UID c-GaN at moderate carbon fluxes and an acceptor surplus caused by carbon doping at higher fluxes. In part **d** the results of IV experiments are presented. IV measurements were performed to investigate the insulating properties of c-GaN:C samples at different doping levels, in this case IV measurements were arranged parallel to the growth axis [001]. Further IV measurements were done perpendicular and to the growth axis [001] to check which metal is able to form an ohmic contact to high carbon doped c-GaN:C samples. The aim of this investigation is to realize pn-junctions with appropriate metal contacts in future work.

a) MBE growth of C doped c-GaN

Carbon doping of cubic GaN was realized by supplying CBr_4 during plasma-assisted molecular beam epitaxy. The C source was a self-made CBr_4 sublimation source connected directly to the Riber 32 MBE chamber. The cylinder with solid CBr_4 powder was kept at a constant temperature by a heating jacket with a temperature controller, a gas line connected the source to the MBE system. To avoid sublimation in the gas line, it was permanently heated to 70 °C. No carrier gas was used and the CBr_4 flux was set by a high precision needle valve at constant source temperature of 20 °C. Cubic GaN:C samples were doped at different CBr_4 beam equivalent pressure between $2x10^{-9}$ mbar and $6x10^{-6}$ mbar. The CBr_4 beam equivalent pressure (BEP) was established by a high precession needle valve. For BEP calibration the temperature of the CBr_4 source was kept constant at 20 °C, and the BEP was measured at the sample position. The CBr_4 BEP was controlled by varying the setting of the needle valve. **Fig.6.4** shows the measured CBr_4 BEP as a function of the setting of the high precession needle valve.

The CBr_4 BEP increases exponentially with the needle valve setting and thus can be varied in the range between $2x10^{-9}$ mbar and $6x10^{-6}$ mbar. **Fig.6.5** illustrates the growth of C doped c-GaN, for that purpose the RHEED intensity transient of the (00) reflection was measured.

The value of I_0 marks the RHEED intensity during a growth break. After opening the Ga source shutter, Ga atoms enter the surface and the intensity drops linearly with a certain slope. At the kink position I_k one ML of Ga coverage is reached. Furthermore, the accumulation of Ga atoms causes a drop of the RHEED intensity which is not any more proportional to the amount of the adsorbed Ga. After opening the nitrogen source shutter, the RHEED intensity saturates cubic GaN grows now under a top layer of Ga and the constant regime of the RHEED intensity transient indicates a constant amount of Ga coverage. However, the intensity increases after opening the CBr_4 source shutter and saturates at $I_{k,}$ the cubic GaN grows under one ML of Ga coverage which is the optimum growth condition of cubic GaN [33-34].

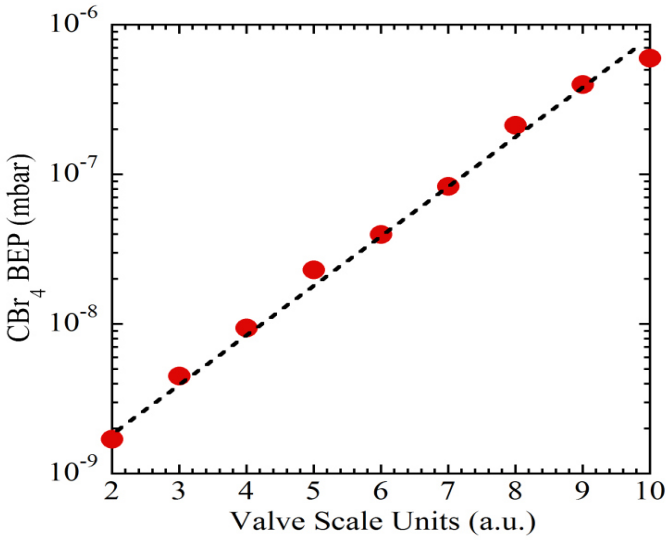


Figure 6.4 *The CBr_4 beam equivalent pressure (BEP) plotted versus the high precision needle valve scale units. The dashed line is a guide for the eye*

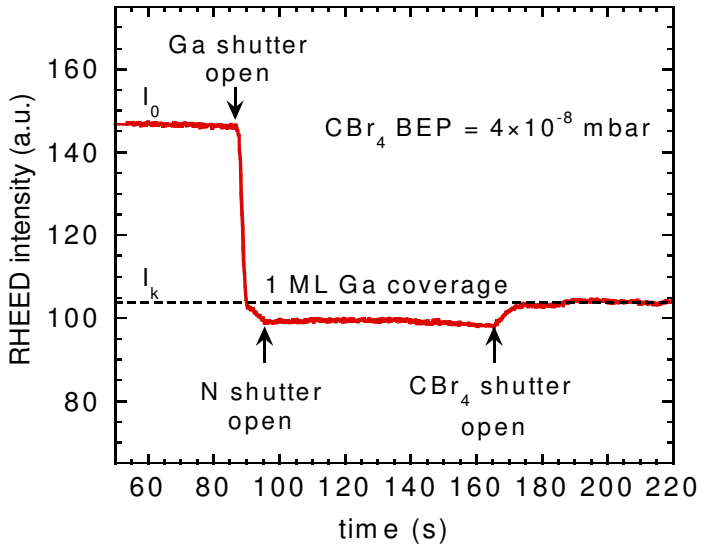


Figure 6.5 *RHEED intensity transient during the growth of c-GaN:C. The CBr_4 BEP is $4x10^{-8}$ mbar. The dashed line indicates the condition of one single ML of Ga coverage*

The consequence of opening the CBr_4 source shutter is the increase of the RHEED intensity indicating a removal of Ga atoms from the surface. Thus, in order to reach the optimum growth condition of one ML Ga coverage the Ga flux has to be increased when increasing the CBr_4 BEP. In **Fig.6.6** the Ga flux is plotted as a function of the CBr_4 BEP, the inset shows a QMS measurement between 140 atomic mass units (amu) and 160 amu.

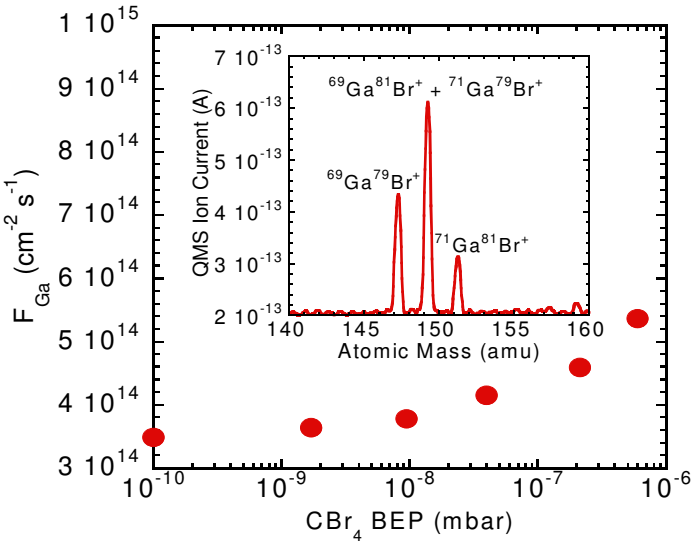


Figure 6.6 *Atomic Ga flux as a function of the CBr_4 BEP. The inset shows a quadrupole mass spectrum in the range between 140 and 160 atomic mass units during the growth of c-GaN:C*

The CBr_4 molecule dissociates at the 720 °C hot sample surface in C, carbon-bromine and bromine-gallium compounds. The three possible permutations of bromine-gallium compounds are clearly identified by QMS. This halogen etching effect of III-V compounds by CBr_4 or CCl_4 is well known, e.g. in GaAs and AlAs system [68-72].

b) SIMS characterization of C doped c-GaN

ToF-SIMS was used to quantify the C incorporation behaviour. To illustrate the effect of C incorporation an 840 nm thick c-GaN/c-GaN:C stacking structure was used. Each layer had a thickness of 70 nm. In **Fig.6.7** the measured depth profiles of ^{69}GaN, O, CN and C negative secondary ion signals upon 1 keV Cs^+ ion sputtering are depicted.
Whereas the ^{69}GaN concentration is constant all over the c-GaN layer thickness, five clear regions with different C concentrations can be identified in the C- and in the CN-profile. In the doped regions the CN signal has a higher intensity and is very sensitive to the applied CBr_4 BEP. Therefore, the intensity ratio of the CN/^{69}GaN signal will be used for further analysis. The Br concentration was at the SIMS detection limit of 10^{15} cm^{-3}. Additionally, the O contamination level is constant all over the layer thickness and is probably responsible for the n-type concentration of 10^{17} cm^{-3} in our unintentionally doped c-GaN samples. For the calibration of the measurement data ToF-SIMS profiles of C^+ ion implanted c-GaN layers were done. For room temperature C^+ ion implantation doses of $1x10^{15}$ cm^{-2} (sample A) and of $1x10^{14}$ cm^{-2} (sample B) at 60 keV were used. For the calibration of the C concentration scale the integrated C concentration of samples A and B were calculated using the C^+ ion implantation doses. The red dotted curve is the simulated C^+ implantation profile of the calibration sample A using the Monte-Carlo simulation software SRIM-2008. Thus, a maximum C concentration of $9x10^{19}$ cm^{-3} was achieved in sample A and a carbon concentration of $9.6x10^{18}$ cm^{-3} in sample B.

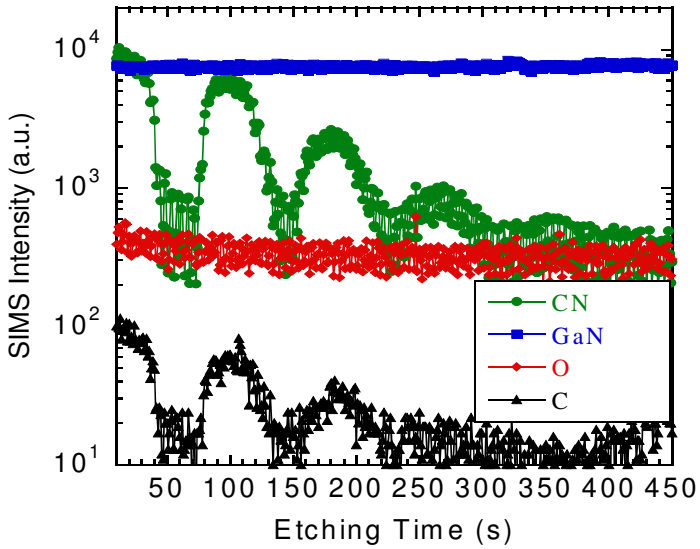


Figure 6.7 *Relevant ToF-SIMS negative ion signal intensities a function of the Cs^+ ion sputtering time. The signals for CN (circles), GaN (squares), O (diamonds) and C (triangles) are depicted*

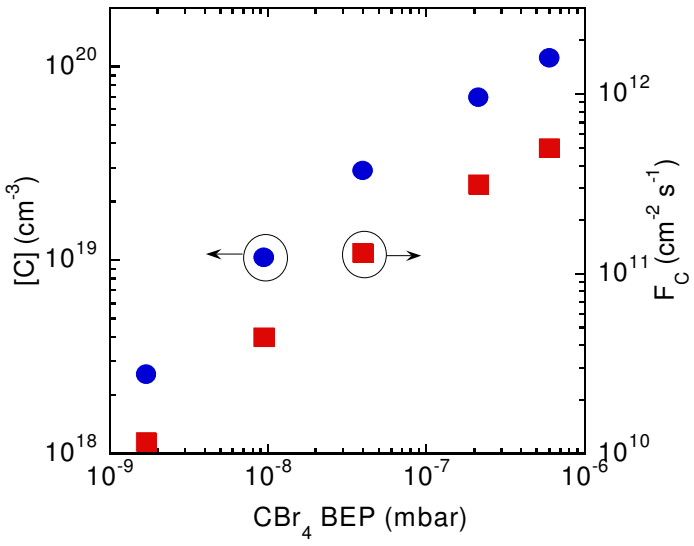


Figure 6.8 *Incorporated C concentration [C] (circles) measured by ToF-SIMS and from the c-GaN:C growth rate calculated atomic carbon flux F_C (squares) vs. the CBr_4 BEP*

In **Fig.6.8** the incorporated C concentration and the equivalent C flux of our samples are plotted vs. the CBr_4 BEP. This diagram shows that the amount of the incorporated carbon is almost linearly related to the incident CBr_4 flux. The equivalent C flux was calculated from the amount of the incorporated C and the cubic GaN growth rate of 0.2 ML/s. A maximum C incorporation of $1x10^{20}cm^{-3}$ was reached with the used system without any diminishing effect on the structural properties of the c-GaN crystal.

c) CV characterization of carbon doped c-GaN

The net donor/acceptor concentration was obtained by evaluation of capacitance-voltage data. Capacitance-voltage measurements on nominally undoped c-GaN showed n-type conductivity. With increasing CBr_4 flux the conductivity type changed to p-type and for the highest CBr_4 flux an acceptor surplus of 1×10^{19} cm^{-3} was obtained. The electrical properties of the c-GaN:C layers were investigated by current-voltage measurements and a decrease of the serial conductance by two orders of magnitude is demonstrated in c-GaN:C.

First a 70 nm thick undoped c-GaN buffer layer was deposited to adjust the growth conditions followed by a 550 nm thick GaN:C layer. Five c-GaN:C samples grown at CBr_4 beam equivalent pressures between 2×10^{-9} mbar and 6×10^{-6} mbar and an undoped c-GaN layer as a reference were investigated. Due to the high conductivity of the 3C-SiC substrates the doping concentration of the fabricated samples could not be obtained by Hall-effect measurements. Thus, the net donor N_D-N_A and acceptor N_A-N_D concentrations were calculated using capacitance-voltage data. Metal contacts of MIS structures were formed by a metal stack of 15nm Ni and 50nm Au. Metals were thermally evaporated on top of the insulator. Large area ohmic contacts at the back side of the samples were prepared by soldering with In.

Fig.6.9 shows $C_{insulator}/C$ curves as a function of applied voltage V. The results of the undoped reference c-GaN sample (red curve) and two low C doped c-GaN samples (blue and green curves) are shown. Two main regions are indicated in **Fig.6.9,** namely the saturation region and the depletion region. From the saturation behaviour of the CV curve the insulator thickness is evaluated. The depletion behaviour was analysed to determine the background donor concentration of the grown samples. In **Fig.6.10** CV characteristics of a heavy C doped sample is depicted. CBr_4 BEP was $6x10^{-7}$ mbar. Two important regions of the CV curve were identified here. The voltage range between -20 V and -13.2 V is referred to the background carrier concentration of the 3C-SiC substrate. It was evaluated to be $3x10^{18}$ cm^{-3} by CV analysis this value is comparable to $2.6x10^{18}$ cm^{-3} as measured by the Hall-effect. The second marked voltage range is between -13.2 V and -1 V. This part of the CV profile is referred to the c-GaN:C. The positive slope of the CV curve indicates p-type conductivity in the grown layer. To determine the type and the amount of the background carrier concentration $1/C^2$ vs. V curves were calculated. The results are shown in **Fig.11 a** (n-type background concentration) and **b** (p-type background concentration).

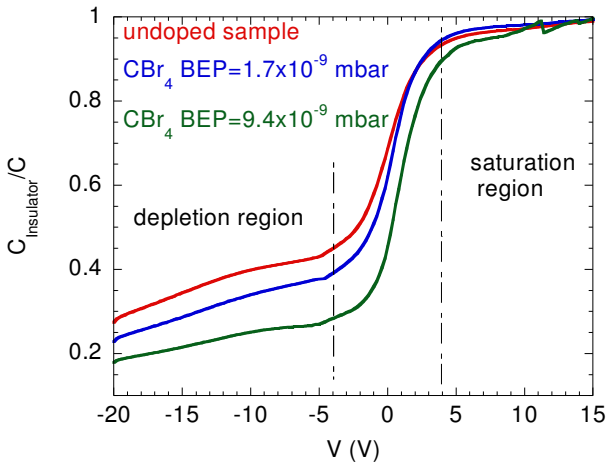


Figure 6.9 *CV characteristics of the reference sample (red), a sample C doped at 1.7x10^{-9} mbar (blue), and a sample C doped at 9.4x10^{-9} mbar (green) measured from -20 V up to +15 V; For a better overview the capacitances were normalized by the insulator capacitance $C_{insulator}$*

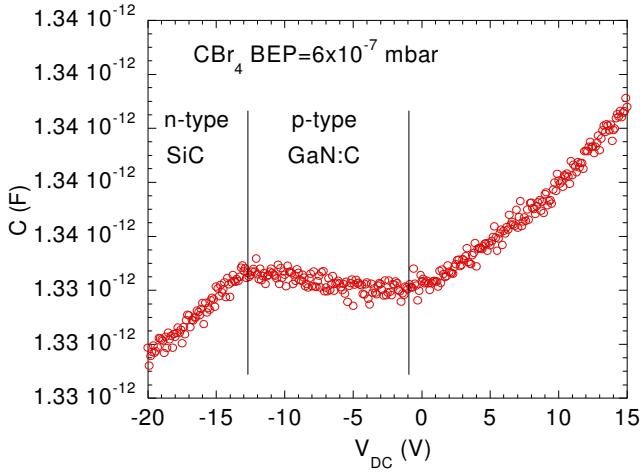


Figure 6.10 *CV- profile of a C doped sample at a CBr_4 BEP of 6x10^{-7} mbar measured from -20 V to +15 V*

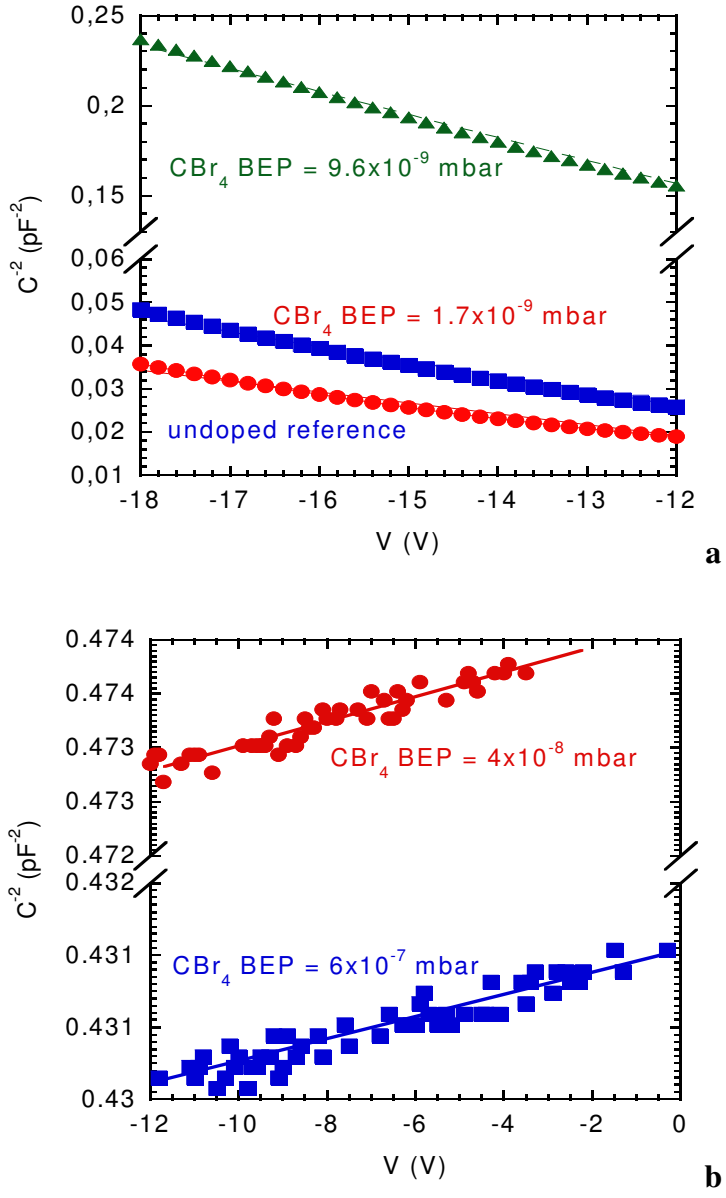


Figure 6.11 *Room temperature C^{-2}-V characteristics of c-GaN:C with low-level C doped samples* ***a*** *showing a donor surplus and high-level C doped samples* ***b*** *exhibiting a distinct acceptor surplus*

The nearly linear behaviour of the data points is the evidence for homogenous doping profiles of the samples in the measured depth section. In the nominally undoped and low-level C doped samples (**Fig.6.11a**), we observe negative slopes of the C^{-2} vs. V curves indicating n-type character. The slope of these curves increases with higher CBr_4 BEP indicating a decrease of the net donor concentration. For the high-level C doped samples (**Fig.6.11b**) the sign of the slopes changes and becomes positive, which is a clear indication of p-type character. In order to investigate the doping profiles the model of a parallel-plate capacitor was used with the abrupt approximation that the charge density ρ is nearly qN_D for $x < W_D$, ρ is zero for $x > W_D$, where x is the distance from the sample surface and W_D is the depletion width. The net donor N_D-N_A and acceptor N_A-N_D concentration of the samples was calculated

from CV data using **equ.(2.8)**.The calculated N_{CV} data are plotted vs. the CBr_4 BEP in **Fig.6.12**.

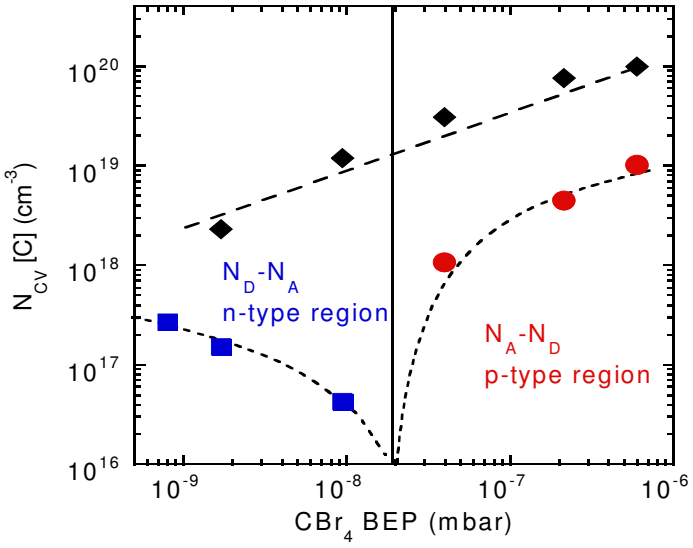


Figure 6.12 *Incorporated carbon concentration [C] (diamonds) and net carrier concentration N_{CV} (squares and dots, respectively) plotted versus the CBr_4 BEP. The dashed lines are guides for the eye*

The net donor concentration values with donor surplus are indicated by squares and with acceptor surplus by circles. The net donor concentration of the undoped c-GaN was approximately $2.7\text{x}10^{17}$ cm^{-3}. At low concentrations the incorporated C causes a decrease of the net donor concentration N_D-N_A. At CBr_4 BEP around $2\text{x}10^{-8}$ mbar the incorporated C produces an acceptor surplus in c-GaN:C and at higher C flux the net acceptor concentration increases with increasing CBr_4BEP. ToF-SIMS measurements revealed that the density of incorporated carbon is at least one order of magnitude higher than the net donor/acceptor density N_{CV}. It is assumed that about 10 % of the incorporated C atoms act as acceptors, whereas about 90 % form self-compensated defects. To obtain the fraction of incorporated carbon acting as an acceptor the carbon concentration in the fabricated samples is calculated under following assumptions:

1. The donor concentration is constant in all measured samples. Its value is $N_D = 1\text{x}10^{17}$ cm^{-3}.
2. The incorporated carbon concentration is proportional to the CBr_4 BEP.

In order to explain the experimental results I further assume that about 10 % of the incorporated carbon atoms act as acceptors whereas about 90 % form self-compensated defects. Thus the net acceptor concentration N_D-N_A in my samples may be calculated by following equation:

$$N_A - N_D = [C] \cdot 0.1 - N_D(const) \qquad (6.1)$$

where *[C]* is the total carbon concentration in c-GaN layers and N_D= 1x10^{17} cm^{-3} the residual donor concentration. Results are shown in **Tab.6.1** together with experimental data of N_D-N_A extracted from **Fig.6.12**.

Carbon concentration (cm^{-3})	measured N_A-N_D (cm^{-3})	calculated N_A-N_D (cm^{-3})
-	-2.7x10^{17}	-
2.3x10^{18}	-1.6x10^{17}	-1.3x10^{17}
1.2x10^{19}	-4.3x10^{16}	-2.0x10^{16}
3.1x10^{19}	+1.1x10^{18}	+3.0x10^{18}
7.7x10^{19}	+4.6x10^{18}	+7.6x10^{18}
9.9x10^{19}	+1.0x10^{19}	+9.8x10^{18}

Table 6.1 *Comparison of the via CV measured N_A-N_D and the calculated N_A-N_D concentration depending on the carbon concentration*

The calculated and the measured data agree with each other and these results support the assumptions made above in the text.

d) IV characterization of C doped c-GaN

To analyse the insulating properties of c-GaN:C layers at different carbon doping levels current-voltage measurements were performed parallel to the growth axis [001] . In **Fig.6.13** the sample structure for the IV investigation is shown.

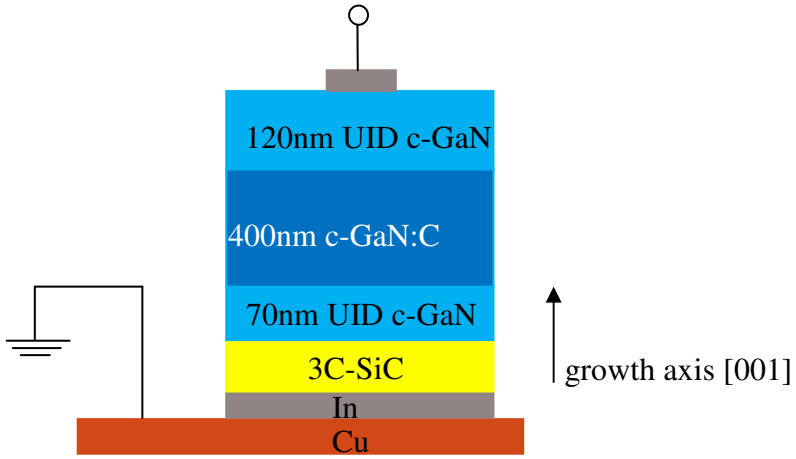


Figure 6.13 *Schematically drawing of the IV-measurement arrangement; c-GaN:C samples consist of 3C-SiC substrate; 70nm UID c-GaN buffer layer; 400nm c-GaN:C layer at different carbon doping levels; 120nm top layer*

IV curves were measured at voltages between -5 V and +5 V. All curves exhibited a slightly non-ohmic behaviour. The serial conductance (**Fig.6.14**) was determined from the linear part of the IV curves at positive voltages. The conductance of samples with donor surplus is indicated by squares and of samples with acceptor surplus by circles. The dashed lines are guides for the eye.
Up to a CBr_4 BEP of about $1x10^{-7}$ mbar C doping of c-GaN causes a decrease of the sample conductivity by more than two orders of magnitude. Cubic GaN:C samples grown with higher CBr_4 BEP offer increasing serial conductance. It is noticeable that the serial conductance of samples with an acceptor surplus of $1x10^{18}$ cm^{-3} and $4.5x10^{18}$ cm^{-3} is one order of magnitude lower than that of the c-GaN:C with the lowest donor surplus of $4.4x10^{16}$ cm^{-3}. Additionally, the serial conductance of the c-GaN:C sample with highest net acceptor concentration of N_A-N_D=$1x10^{19}$ cm^{-3} is one order of magnitude lower than the conductance of the undoped sample with net donor concentration of N_D-N_A=$2.7x10^{17}$ cm^{-3}. This result can be explained by extremely low hole mobility caused by ionized impurity scattering and compensation effects [33].

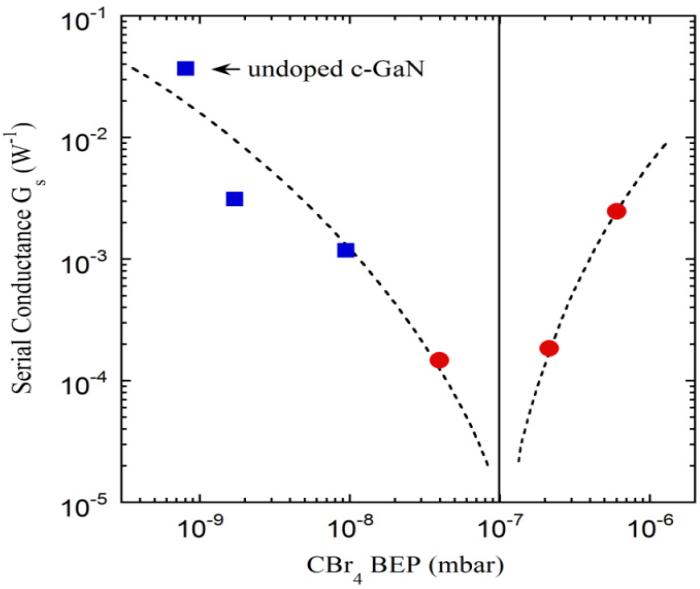


Figure 6.14 *Serial conductance vs. CBr_4 BEP. Serial conductance of samples with donor and acceptor surplus is indicated by squares and dots, respectively; dashed lines are guides for the eye*

However, the results from subchapter **c** showed extraordinary high acceptor concentrations resulting from C doping without change of the structural features of the grown samples. Thus a great possibility is given to realize the first c-GaN pn-junction devices, based on carbon doping on the p-side. For p-n-diode operation ohmic contact on both p and n side are desirable. As already reported above the n-side ohmic contact was realized by thermally evaporation of a metal stack, where Ti formed the ohmic contact to c-GaN. The situation is more difficult to find an appropriate metal for p-side ohmic application. In literature mainly three metals can be found which form a suitable low resistance contact for p-type h-GaN. There is no appropriate metal for ohmic application on p-type c-GaN reported up to now. The suggested metals are Pt [73], Pd [74] and Ni [75-76] promising low contact resistance. In this work Pd (work function 5.12 eV) and Ni (work function 5.15 eV) are often used for Schottky or MIS application. They can be easily thermal evaporated, whereas an electron beam evaporator is required for Pt application. In the following discussion the possibility of an ohmic application Pd and Ni on p-type c-GaN:P is carried out. To investigate ohmic character of the mentioned metals IV measurements perpendicular to the growth axis were performed. Contact metal stacks consisting of Pd/Au (30 nm/60 nm) and Ni/Au (30 nm/60 nm) were thermally evaporated on top of the sample. Four round metal contact structures arranged in a square formation were used, the diameter of each contact is 100 µm and the spacing between two adjacent contacts is 500 µm. IV measurements were firstly performed directly after thermal evaporation and after RTA treatment at different temperatures. IV-measurements were performed using an *Agilent Precision Parameter Analyzer 4156C*. All electrical measurements were performed under light-tight and electrically shielded environment. A cross sectional view of the measured sample is shown in **Fig.6.15**. The sample consists of free standing 3C-SiC substrate followed by 70 nm UID c-GaN buffer layer and highly carbon doped 600 nm c-GaN:C. The carbon doping concentration is assumed to be

$N_A - N_D$= 4.6x10^{18} cm^{-3} resulting from a CBr_4 BEP of 2x10^{-7} mbar (compare **Fig.6.12**). The IV-measurement arrangement is also indicated in **Fig.6.15**.

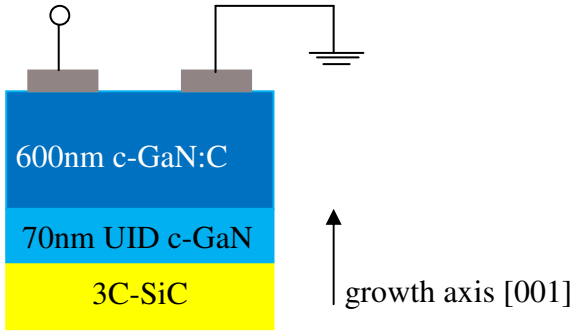


Figure 6.15 *Schematic drawing of the IV-measurement arrangement; samples consist of 3C-SiC substrate; 70nm UID c-GaN buffer layer; 600nm c-GaN:C layer*

Current-voltage characteristics of Pd/Au contacts measured directly after thermal evaporation and after several RTA steps are shown in **Fig.6.16**. RTA treatments were performed for 30 s in N_2 atmosphere at temperatures between 400 °C and 850 °C. Current density vs. voltage curves were recorded between -5 V and +5 V applied dc voltage. To protect the produced device current limitation was set to 15 A/cm².

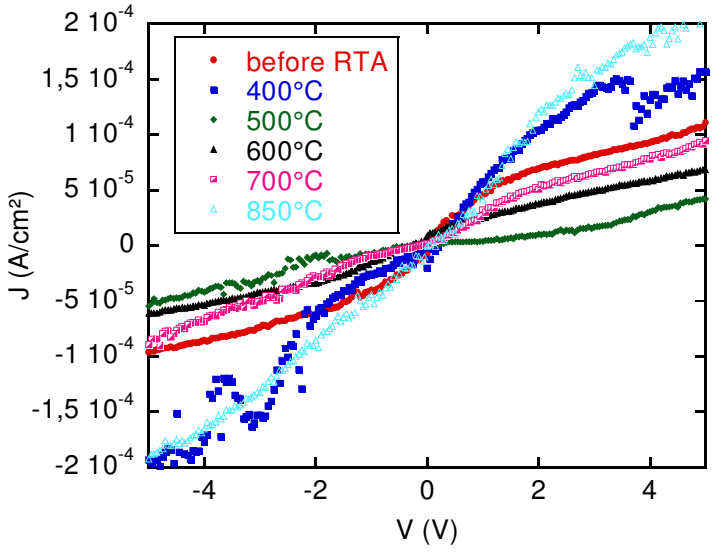


Figure 6.16 *Current density plotted versus applied voltage, from -5 V to 5 V; Pd was used as p-type ohmic contact on top of the sample; IV curves were measured directly after thermal metal evaporation and after RTA treatment for 30s between 400 °C and 850 °C in N_2 ambient*

All measured IV curves show a slightly non-ohmic behaviour. After the annealing step of 400 °C (blue) current density increases compared to IV-measurement before RTA (red) by a factor of two. Current density increases from -1x10^{-4} A/cm^2 to 2x10^{-4} A/cm^2 at -5 V and from 1x10^{-4} A/cm^2 to 1.5x10^{-4} A/cm^{-2} at +5 V. IV characteristics measured after annealing steps at

500 °C, 600 °C and 700 °C show a slightly decrease of current density. Whereas the RTA step at 850 °C (cyan blue) shows the best improvement in ohmic behaviour. It is similar to the curve at 400 °C in reverse direction but it shows a higher current density in forward direction. The value is $2x10^{-4}$ A/cm^2 at +5 V. However, it is noticeable that the current density is very low and the current magnification caused by RTA at 850 °C is only a factor of two. It is assumed that the contact resistance of Pd and c-GaN:C is relatively high. Transition-line-method (TLM) measurements should be done in future works to prove the assumption.
Current-voltage characteristics of Ni/Au contacts measured directly after thermal evaporation and after several RTA steps are shown in **Fig.6.17**. RTA treatments were performed for 30 s in N_2 atmosphere at temperatures between 400 °C and 600 °C. Current density vs. voltage curves were recorded between -5 V and +5 V applied dc voltage.

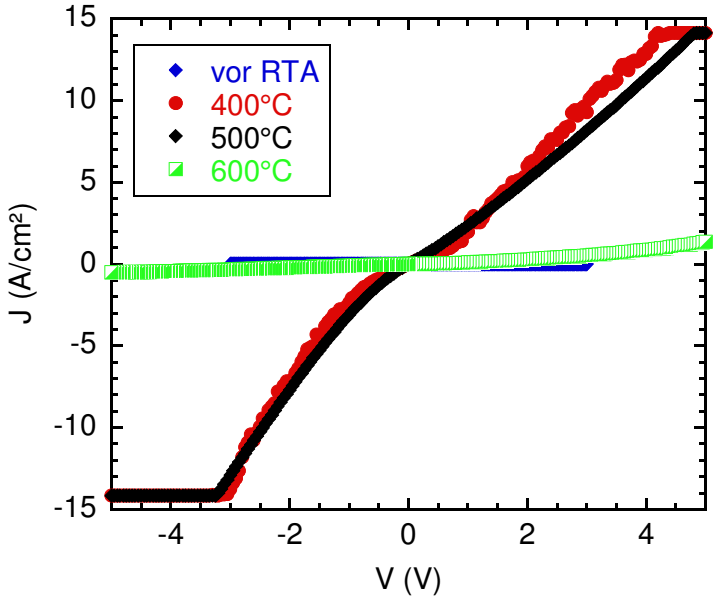


Figure 6.17 *Current density plotted versus applied voltage, from -5 V to 5 V; Ni was used as p-type ohmic contact on top of the sample; IV curves were measured directly after thermal metal evaporation and after the RTA treatment for 30s between 400 °C and 600 °C in N_2 ambient*

IV characteristics of Ni/c-GaN:C contact device measured after RTA at 400 °C (red) and 500 °C (black) show the best ohmic character and the highest current density. Compared to the IV curve before the (blue) RTA treatment the current density is ten times higher at +4V. It amounts about 1 A/cm² before RTA and 10 A/cm² after RTA at 400 °C and 500 °C. Current saturation at +4 V and -3 V is due to a current limitation of the parameter analyser. The IV curve, after annealing at 600 °C, shows contact degradation. The current density vs. voltage curve recorded after RTA at 600 °C shows nearly the same current density like before RTA. Contact degradation probably occurs due to chemical reactions at the Ni/c-GaN:C interface. Also oxygen incorporation is possible at higher annealing temperatures forming NiO_x layer, which could cause an increase of the contact resistance [77-80].
However, Ni shows an outstanding low resistance ohmic contact to p-type c-GaN:C compared to Pd. A comparison of IV characteristics of Pd contact annealed at 850 °C and Ni annealed at

400 °C at +4 V applied voltage results in a factor of 8.5×10^5 higher current density using Ni as contact metal. Further the metal stack Ni/Au was used as ohmic contact to c-GaN:C to realize an pn-diode.
The pn-junction consists of n-type 3C/SiC substrate, 70 nm n-type UID c-GaN buffer layer, and 600 nm p-type c-GaN:C top layer. In **Fig.6.18** a cross sectional view of the sample structure and IV-measurement arrangement is illustrated. An ohmic top contact consisting of Ni/Au (30 nm/60 nm) was applied to GaN:C. The contact was thermally annealed for 30 s in N_2 ambient at 400 °C to improve the ohmic behavior as described above. Ohmic back contact was realized by soldering the high conductive n-type 3C-SiC substrate to a copper plate. The measurements were performed under light-tight and electrically shielded conditions at RT. IV measurements were performed using a high precision parameter analyzer *Agilent Precision Parameter Analyzer 4156C*. Current limitation was set to 100 mA according to a current density value of 500 A/cm².

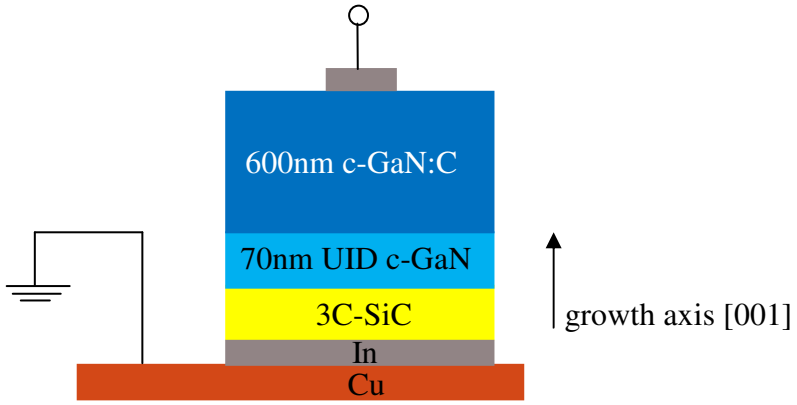


Figure 6.18 *Cross sectional view of the current–voltage measurement arrangement of pn-junction formed by n-type 3C-SiC/ UID c-GaN and p-type c-GaN:C; positive potential is applied to Ni/Au top contact, negative pole is applied to Cu/In/3C-SiC back contact*

IV-measurement of the fabricated pn-structure was performed in forward direction. Voltage was applied to top contact from 0 V to +5 V and between 0 V to -10 V, whereas the back contact was grounded. The measured current vs. voltage characteristic shows rectifying behaviour (s. **Fig6.19**). The current flow is suppressed in back direction, whereas it increases linearly in forward direction until it reaches current saturation at +4.7 V. The Shockley [81] equation predicts an exponential increase of current at positive voltages:

$$I(V) = I_S\left(\exp\left(\frac{eV}{k_B T}\right) - 1\right) \tag{6.1}$$

In **equ.(6.19)** I_S is the saturation current, e the elementary charge, k_B the Boltzmann constant, T the temperature and V the applied voltage.
Exponential increase of the current flow in forward direction could not be observed. The current increase is linear. The slope correlates to serial conductivity of 2.471 mS or to a serial resistance of 0.405 kΩ. Total resistance R_{tot} consists of a serial connection of several resistances as shown in **equ.(6.2)**.

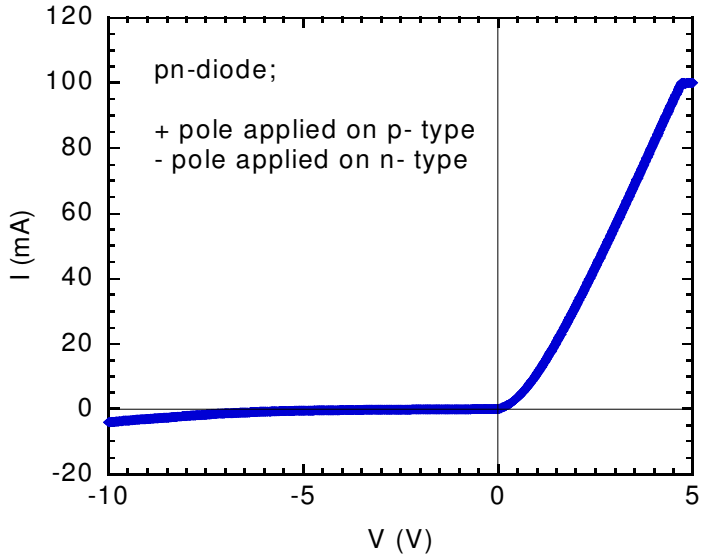


Figure 6.19 *Current vs. voltage characteristic of the fabricated 3C-SiC/c-GaN/c-GaN:C pn-structure; pn-diode is measured in forward direction; voltage is applied to the top contact, back contact is grounded*

$$R_{tot} = R_{C,SiC} + R_{SiC} + R_{SiC,GaN} + R_{GaN} + R_{GaN:C} + R_{C,GaN:C} \tag{6.2}$$

where $R_{C,SiC}$ is the contact resistance of In and 3C-SiC, R_{SiC} the 3C-SiC bulk resistance, $R_{SiC,GaN}$ the transfer resistance at the 3C-SiC/c-GaN hetero-interface, R_{GaN} and $R_{GaN:C}$ are bulk resistances of c-GaN and c-GaN:C, and $R_{C,GaN:C}$ is the contact resistance of c-GaN:C and Ni metal contact. Hall measurements yielded a free carrier concentration of $n = 2\text{x}10^{18}$ cm^{-3} and a specific resistivity of $\rho = 6.6$ mΩcm for 3C-SiC (001) substrates. Thus it can be assumed that the major part of total resistivity in **equ.(6.2)** is given by bulk resistances of c-GaN and c-GaN:C. Hall measurements of 3-C-SiC/c-GaN structures led to a free carrier concentration of approximately $n = 9\text{x}10^{16}$ cm^{-3}, a Hall mobility of $\mu_H = 40$ cm²/Vs and a specific layer resistance of $\rho = 1.7$ Ωcm in UID c-GaN. For calculation relationships in **equ.(2.16)-(2.18)** were used. A two layer model was applied. The resistance of c-GaN is three orders of magnitude higher than for 3C-SiC, additionally the resistance of c-GaN:C is unknown. The relatively high resistance of c-GaN and c-GaN:C is probably caused by its low mobility and high dislocation density ($9\text{x}10^{9}$ cm^{-2}). Current loss caused by these circumstances probably prevents an exponential increase of current flow in forward direction.
Nevertheless the results shown in **Fig.6.19** are promising for future works. Rectifying behavior of the fabricated pn-device was shown.

6.3 Asymmetric multi c-AlN/GaN quantum well structures

In this section a combination of two methods of device insulation is presented, namely carbon doping and the growth of c-AlN/GaN multi quantum wells. To avoid tunneling leakage current asymmetric c-GaN (1 nm/2 nm) multi quantum well (MQW) structures with 3nm thick c-AlN barriers were grown. Additionally the structure was doped by carbon using $CBr_4$to compensate the unintentionally incorporated donors during MBE growth.

This possibility is a novel method of the electrical separation of the substrate and the HFET device. For the epitaxial growth of my structures free standing 3C-SiC (001) substrates with a free carrier concentration of $n = 2x10^{18}$ cm^{-3} and a resistivity of $\rho = 6.6$ mΩcm were used. On a 50 nm c-GaN buffer layer an asymmetric multi quantum well structure consisting of 10 cubic GaN:C asymmetric (1 nm/2 nm) QWs with 3 nm c-AlN:C barriers had grown. A 50 nm c-GaN cap layer completed the sample structure. A detailed conduction band profile and the quantized electron states within the asymmetric quantum well were calculated using a 1D Poisson-Schroedinger-Solver. The structural properties were analyzed by an atomic force microscopy and a high resolution x-ray diffraction. Current-voltage measurements of these structures showed an increase of the serial resistivity from $5x10^{-3}$ Ω to $8x10^{3}$ Ω by six orders of magnitude compared to an unstructured c-GaN reference sample.

In the described experiments three kinds of samples were investigated. Sample A consists of a150 nm thick c-GaN layer grown on the 3C-SiC substrate and was used as a reference. Sample B and C consisted of a 50 nm c-GaN buffer layer followed by an asymmetric multi QW structure (**Fig.6.20**). The asymmetric MQW structures consisted of five alternating 1 nm and 2 nm thick c-GaN quantum wells and eleven 3 nm thick c-AlN barriers. In sample C the quantum wells and the barriers were doped with carbon at a CBr_4 BEP of $1.2x10^{-8}$ mbar. To ensure equivalent surface conditions for ohmic contacts in all three samples a 50 nm c-GaN cap layer was grown.

The MBE growth of the 1 nm/2 nm QWs and the 3 nm barrier layers had been a challenging task. To obtain the exact thickness of the layers RHEED technique was used. **Fig.6.21** illustrates the time transient of the RHEED intensity during initial c-AlN:C growth. The growth oscillations indicated an atomically smooth two dimensional growth of the c-AlN:C layer. A growth rate of 5.1 s/ML was obtained from the oscillation period. The exact growth periods were calculated using the lattice parameters of c-GaN and c-AlN which are a_{GaN} = 0.453 nm [22] and a_{AlN} = 0.437 nm [23] respectively. Using a 1D Poisson-Schroedinger-Solver a detailed band structure analysis of the grown samples at RT is done [57]. QWs of 1 nm and 2 nm thickness were chosen to ensure that the formed electron states have energetic distance from the Fermi energy level. Additionally the asymmetry causes an energetic separation between the adjacent WQs to avoid tunnelling current. For the calculation of the carbon doped sample C I assumed a net donor concentration of $2x10^{16}$ cm^{-3} in the c-GaN layers [19] and $1.5x10^{17}$ cm^{-3} in the c-AlN barrier layers. These values were one order of magnitude lower than the background concentrations in the UID c-GaN/c-AlN layers of the samples A and B. In case of the 2 nm QW two electron states around 0.31eV and 1.25 eV above the Fermi level are formed. In the 1 nm c-GaN QW the electron state is 0.78 eV above the Fermi level for the UID sample B. In sample C electron states were energetically

localized at 1.32 eV and 0.4 eV within the 2 nm QW and at 0.86 eV within the 1 nm QW. To avoid electron wave function overlap of quantized electron states 3 nm c-AlN layers were grown as barriers. The approximate penetration depth of the electron wave functions were 2.5 nm in the 1 nm QW and 1.9 nm in the 2 nm QW. **Fig.22 a** and **b** show the entire MQW structure of samples B and C, respectively.

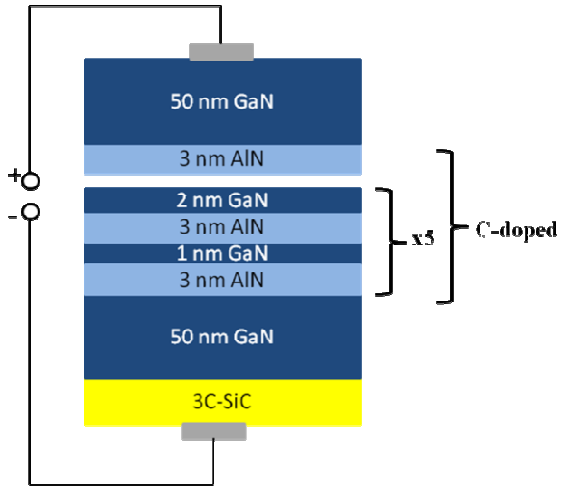


Figure 6.20 *Schematic drawing of the IV-measurement arrangement; samples B (undoped) and C (carbon doped) consist of a 50 nm c-GaN buffer followed by 10 asymmetric (1 nm/2 nm) c-GaN quantum wells with (3 nm) c-AlN barriers*

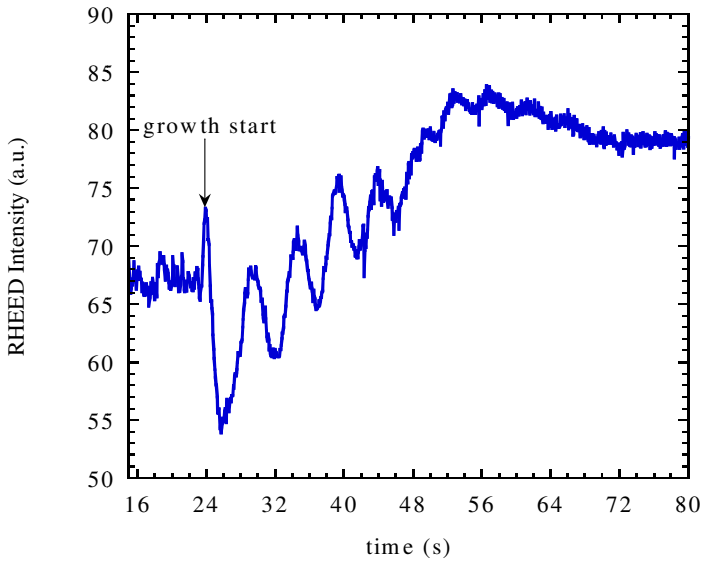


Figure 6.21 *RHEED intensity transient during the initial growth of c-AlN:C; RHEED intensity oscillations indicate a two dimensional atomically smooth growth; the growth rate of 5.1s/ML was obtained from the oscillation period*

The c-AlN/GaN conduction band discontinuity was assumed to be 2.05 eV as mentioned in chapter 2.1. Using alternating 2 nm and 1 nm QWs ensured a maximum energetic difference of the quantized states of the adjacent QWs. The net donor concentration in samples A and B were $2x10^{17}$ cm^{-3} for c-GaN and $1.5x10^{18}$ cm^{-3} for c-AlN. In sample C these values had been

reduced by one order of magnitude. E_c(GaN) – E_F is the energetic distance between the c-GaN conduction band and the Fermi level. E_1 and E_2 are the energy values of the quantized states within the QWs.

To investigate the isolation properties of the grown layers IV-measurements parallel to growth direction [001] were performed. According to **Fig.6.20** ohmic top and back contacts were used. The voltage was varied from -5 V to 5 V. The results of the measurement are plotted in **Fig.6.23**.

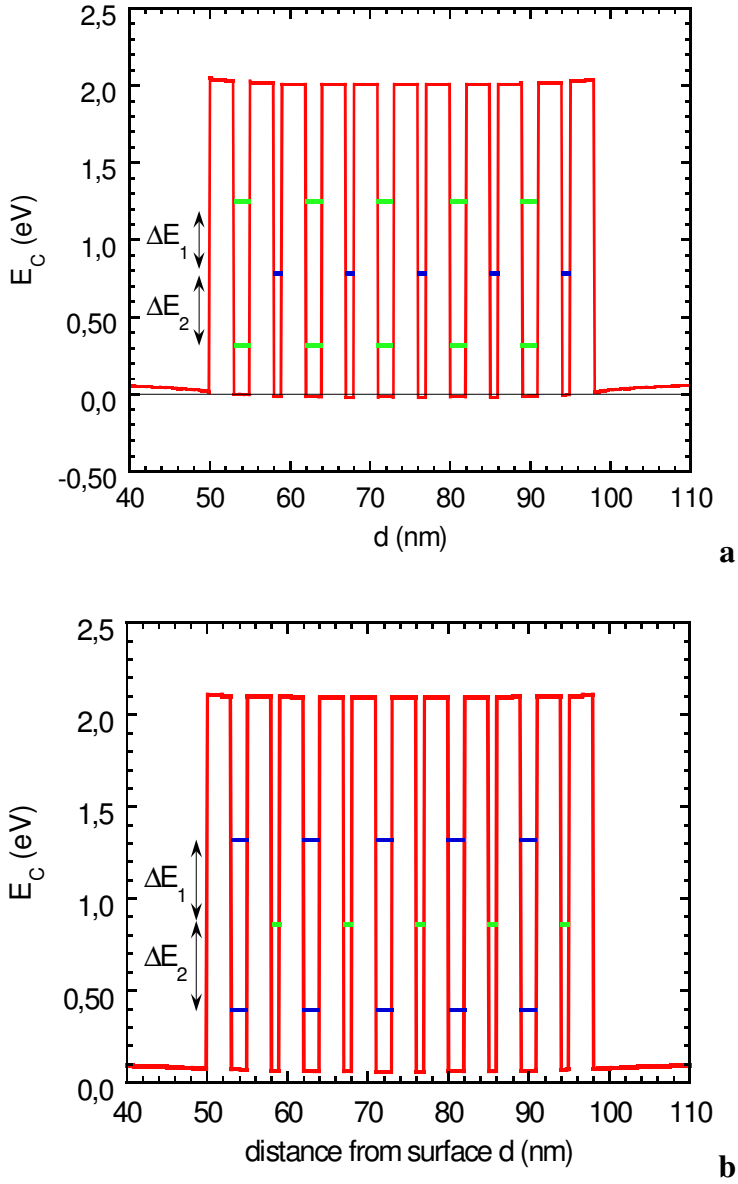


Figure 6.22 *Gamma point conduction band edge as a function from the distance from the surface; the quantized electron states within the QW structure are also shown (blue for 2 nm QWs, red for 1 nm QWs); line at zero energy marks the Fermi level; calculations were performed using 1D Poisson-Schroedinger-Solver*

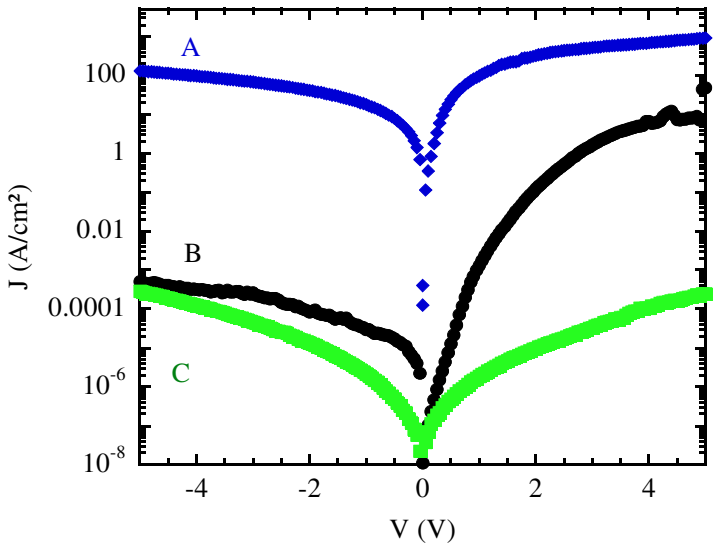


Figure 6.23 *Current density of our three fabricated samples plotted versus the applied voltage; sample A is the reference sample (blue diamonds), sample B is the sample with UID MQWs (black circles) and sample C contains carbon doped 10 MQWs (green squares)*

Sample A was unstructured and was used as a reference sample. The current density versus applied voltage curves showed a slightly non-ohmic behavior affected by the hetero-interface between the 3C-SiC substrate and the c-GaN buffer layer. The measurement at sample A yielded the maximum current density at +5 V and the current density amounted 925 A/cm². This high conductivity originates from the UID c-GaN and from the high conductive 3C-SiC substrate. The current density in sample B was reduced to 48 A/cm² at 5 V of applied voltage. The reduction of the current flow had been a clear evidence for the isolating properties of the MQW structure. Due to a large conduction band offset between c-GaN and c-AlN electrons had to cross eleven barrier layers. In addition the asymmetric arrangement of the QWs suppressed the tunneling current. In case of sample C the current density at 5 V amounted 25×10^{-3} A/cm², thus the serial resistivity had increased to a maximum. We explained this result by compensation of the unintentionally build in donors by carbon acceptors. At the adjusted carbon flux we expected a decrease of the donor density by one order of magnitude. Thus the conduction band edge of the c-GaN QWs was 0.08 eV above the Fermi level on the energetic scale. Whereas in sample B the conduction band edge was 0.02 eV below the Fermi energy. From the linear increase of the IV curves in forward direction the serial resistivity of the samples was calculated. The results are depicted in **Fig.6.21**.

The values for the serial resistivity of samples A, B and C were 5×10^{-3} Ω, 0.25 Ω and 8×10^{3} Ω, respectively (**Fig.6.24**). In sample C we observed an increase of the serial resistance by more than six orders of magnitude compared to the unstructured reference sample A. This extraordinary high resistivity was mainly caused by three factors. The first was the large c-GaN/AlN conduction band offset forming potential barriers for electrons. The second circumstance was the asymmetric arrangement of the MQW structure causing the energetic separation of the quantized electron states of the adjacent wells. Additionally the penetration depth of the electron wave functions was below the c-AlN barrier thickness.

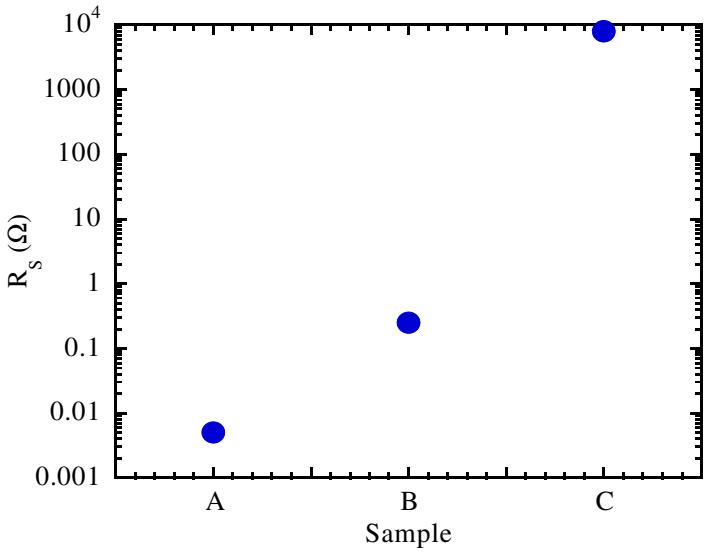


Figure 6.24 *Serial resistivity R_S of the fabricated samples A, B and C; the values were obtained from the linear increase of the current in forward direction*

Thus the tunnelling current is reduced to a minimum. The third factor had been the compensation of the donor concentration in the UID layers by carbon incorporation during the MBE growth. In conclusion non-polar cubic AlN/GaN carbon doped asymmetric quantum well structures were grown. *In-situ* MBE growth control by RHEED ensured the intended layer thickness. Current-voltage measurements have shown that the carbon doped samples were of extraordinary electric isolation quality in comparison to asymmetric undoped quantum wells and to cubic GaN bulk structure. A reduction of the serial conductivity of six orders of magnitude compared to a c-GaN reference sample was observed.

7. Properties of the fabricated field effect devices

In this chapter the properties of the fabricated FETs and HFETs are described. The output and transfer characteristics of fabricated devices are discussed. The fabrication of the devices and contact assembly was carried out according to the description in chapter 3.2 and 3.5. For all shown transistor devices gate dimensions were: Width Z = 25 µm, length L_G = 2 µm and source and drain distance is 8 µm. All transistor devices were electrically investigated at RT in electrically shielded and light-tight conditions.

7.1 Cubic GaN field effect transistor

The sample for transistor application was grown by MBE on a 3C-SiC substrate. To provide electrical separation between the substrate and the active device a 200 nm c-GaN:C buffer was grown. As mentioned in chapter 6 carbon doping was used to decrease the conductivity of the UID c-GaN. A CBr_4 BEP of $2x10^{-7}$mbar was established during the doping process to get the optimum insulating conditions for transistor operation (compare **Fig.6.14**). A 120 nm c-GaN top layer formed the conductive channel for the transistor operation. A schematically cross sectional view of the basic device structure and the field effect measurement arrangement is illustrated in **Fig.7.1**.

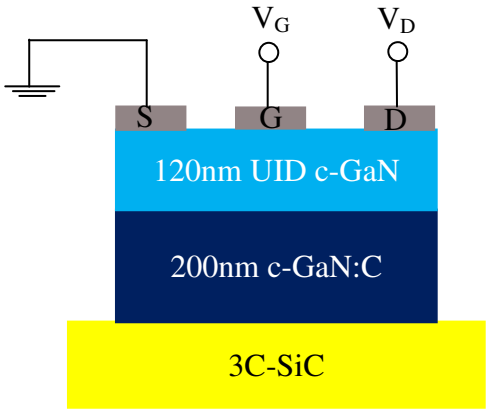


Figure 7.1 *Schematically drawing of the fabricated sample structure; field effect measurement arrangement is also shown (sample 2174)*

Source and drain contacts were applied to the n-type UID c-GaN layer using Ti as ohmic contact metal. A Schottky contact was used for gate operation, therefore Ni was applied. A Schottky barrier of 0.9 eV [82] was assumed to the semiconductor/metal interface. Before that a positive drain voltage V_D had been applied between the ohmic source and drain contacts. Free electrons within the conductive channel layer (120 nm UID c-GaN) follow the electrical potential and flow from source to drain.

The principle of the field effect device is to control the current flow between source and drain by narrowing and widening the conductive channel by an electric field forming a depletion zone. The required electric field is generated applying a voltage V_G to the Schottky gate contact. At V_G = 0 V the depletion zone is determined by the Schottky barrier at the metal semiconductor interface. At negative gate voltages the depletion zone increases resulting in narrowing the conductive channel. This leads to a decreased drain current I_D and at a certain negative V_G current flow is pinched off. However, at positive gate voltages depletion zone decreases allowing more electrons pass the conductive channel resulting in an increased drain current.

As indicated in chapter 3.5 with our available lithography mask four transistors were fabricated simultaneously on each sample. Due to several sample treatments like RIE, lift-off processes after photo lithography and thermal metal evaporation, not every transistor "survived" the assembly to a complete functional device. Two functional transistor devices were fabricated on the sample schematically shown in **Fig.7.1**. The only difference between both fabricated devices is their spatial separation on the sample of 1 cm. Since parameter like background doping level, dislocation density and surface roughness vary across the sample output characteristics of the fabricated transistors are also different. These factors influence, for example, the electron mobility and contact resistance, which for their part directly affect the drain current. This fact is clearly obvious in **Fig.7.2 a** and **b**. Output characteristics of transistor No. 1 (**Fig.7.2a**) and No. 2 (**Fig7.2b**) are shown. Drain current I_D is plotted as a function of drain voltage V_D at different gate voltages V_G. A drain voltage V_D = 0 V to V_D = +3 V was applied between the ohmic source and drain contacts. Therefore source contact is set to negative potential for the source-drain measurement as well as for the control of the gate voltage. Drain and gate voltage are set to positive potential, which can be independently controlled from each other. Gate voltages of V_G = -5 V to V_G = +2 V and V_G = -3 V to V_G = +1 V were applied at the Schottky gate contact for transistor 1 and transistor 2, respectively. Source-drain voltage V_D vs. source-drain current I_D characteristics were measured at different gate voltages V_G. Drain current of transistor one was approximately a factor of two lower then for transistor 2. As mentioned before this difference in drain current was probably caused by different electron mobility and/or different contact resistivity.

However, a clear field effect was observed in both fabricated transistor devices. By increasing the gate voltage the drain current also increases. At lower drain voltages the drain current rises linearly between V_D = 0 V and V_D = 0.4 V. This linear slope increases and continues to approximately V_D = 1 V. A possible explanation for the low increase of initial drain current up to V_D = 0.4 V is a high contact resistance of the ohmic source and drain contacts resulting in a diode like rectifying behaviour at low voltages. A slight saturation occurs at drain voltages > 1 V, which is typical for transistor output characteristics, as described in chapter 4.1. The saturation observed, especially in transistor 1 (**Fig.7.2a)**, demonstrates a successful electrically separation between the transistor c-GaN channel and the high conductive 3C-SiC substrate by carbon doping of the initial c-GaN buffer layer. However transistor 2 shows less saturation behaviour of drain current. This is probably caused by insufficient insulation properties caused by a lower carbon doping level in the initial c-GaN layer compared to transistor 1. The result is that a not negligible part of the drain current flows through the high

conductive 3C-SiC substrate preventing current saturation. At least the higher drain current could also originate from additional shunt current in transistor 2.

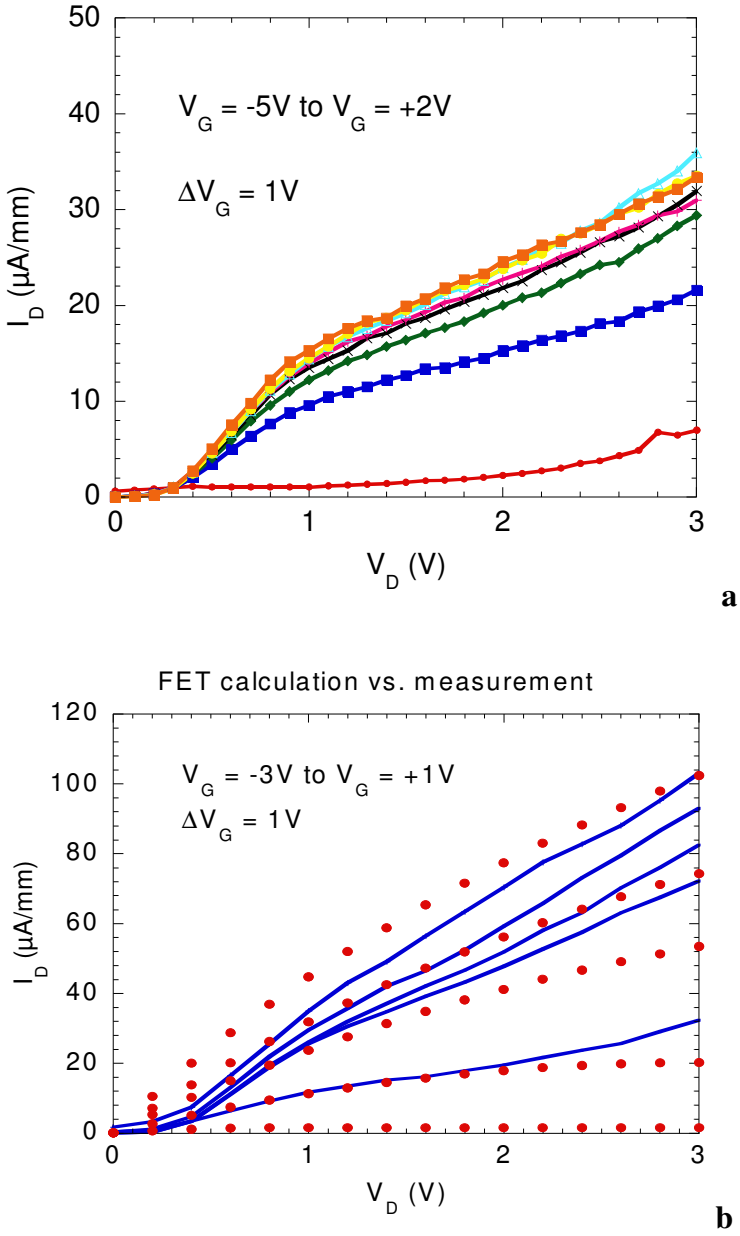


Figure 7.2 a *FET No.1: Drain current I_D as a function of applied drain voltage V_D at gate voltages V_G between -5 V and +2 V;* **b** *FET No.2: Drain current I_D as a function of applied drain Voltage V_D at gate voltages V_G between -3 V and +1 V, additionally I_D calculation results are also illustrated*

To evaluate the magnitude of the mobility output characteristics were calculated using the description in chapter 4.2. Using the analytical expression, shown in **equ.4.16,** drain current I_D was calculated for the given FET structure. A comparison of calculation (red dots) and measurement (blue solid lines) results is shown in **Fig.7.2 b**. Gate voltage V_G was varied from -3 V to +1 V in ΔV_G = 1 V steps. For the calculation the channel depth was assumed to be a = 90 nm, channel width Z = 25 µm, channel length L_G = 2 µm, the UID background

concentration in c-GaN N_D = 9x10^{16} cm^{-3}, relative permittivity $\varepsilon_{\text{c-GaN}}$ = 9.7. The mobility was fitted to the measured drain current. As a result a mobility of μ = 5 cm²/Vs was evaluated for the fabricated c-GaN FET. This value is lower than measured by Hall using the two layer model of approximately 40 cm²/Vs, as described above in chapter 6.2. This difference is caused by several uncertainties like e.g. layer thicknesses, channel length or channel depth. This relatively low mobility value is caused by several scattering mechanisms. The most reasonable mechanisms in the group-III nitrides are acoustic phonon scattering, impurity and donor scattering and dislocation scattering [83, 84]. Additionally scattering is also possible at domain boundaries, so called anti phase domains [85].
Nevertheless, the calculation agrees very well with the measured results. A depletion mode field effect operation is presented using c-GaN grown on highly conductive free standing 3C-SiC.

7.2 Depletion mode c-AlGaN/GaN MIS-HFET

Depletion (normally-on) mode c-AlGaN/GaN MIS-HFET device will be presented in this chapter. **Fig.7.3** shows a schematic cross-sectional view of the grown sample. A 150 nm thick low conductive c-GaN:C buffer layer is grown on 3C-SiC substrate. For efficient electrical isolation between the active device and the highly conductive substrate a CBr_4 BEP of $2x10^{-7}$ mbar was applied during buffer growth. Buffer layer is followed by 50 nm n-type UID c-GaN. UID n-type c-GaN is needed to form the 2DEG with n-type c-$Al_xGa_{1-x}N$. On top of c-GaN a 4 nm $Al_{0.3}Ga_{0.7}N$ spacer layer is grown. The spacer layer is important to spatially separate the donors and the electrons within the 2D channel to minimize Coulomb scattering. Donors originate from the 6 nm c-$Al_{0.3}Ga_{0.7}N$:Si layer. The free carrier concentration of Si doped layer is $n = 4x10^{18}$ cm^{-3}. The structure is completed by 10 nm UID c-$Al_{0.3}Ga_{0.7}N$ cap layer and 6 nm SiO_2 gate insulation layer. For source and drain application the insulating SiO_2 was removed by RIE. Gate contact consisting of 15 nm Ni and 50 nm Au was not thermally annealed. Ohmic source and drain contacts consist of a 15 nm/50 nm/15 nm/50 nm Ti/Al/Ni/Au metal stack. They were thermally annealed for 30 s in nitrogen ambient at a temperature of 850 °C. The aim of thermal annealing treatment is reducing the contact resistivity by thermal diffusion of the contact metal into the c-AlGaN layers and to contact the transistor channel at the c-AlGaN/GaN interface. Contacting the hetero-interface by deposited ohmic source and drain contacts is also indicated in **Fig.7.3**.

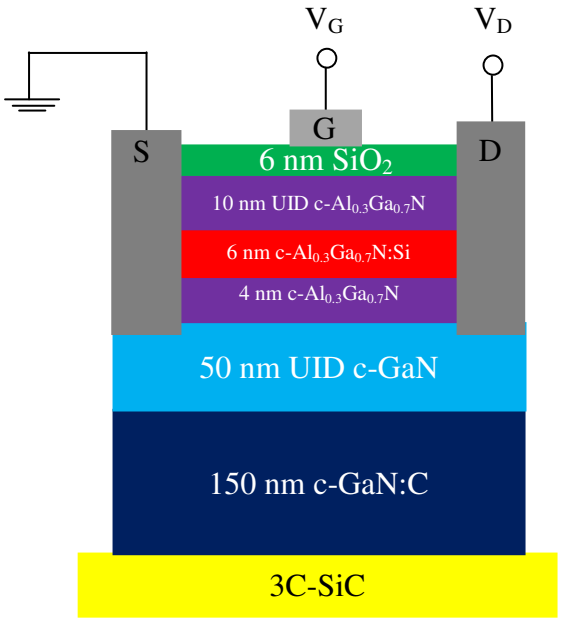


Figure 7.3 *Schematic cross sectional view of the fabricated modulation doped metal insulator semiconductor hetero-junction field effect transistor structure; sample consists of 3C-SiC substrate, 150 nm c-GaN:C, 50 nm UID c-GaN, 4 nm UID c-$Al_{0.3}Ga_{0.7}N$, 6 nm c-$Al_{0.3}Ga_{0.7}N$:Si with a free carrier concentration of n = $4x10^{18}$ cm^{-3}, 10 nm UID c-$Al_{0.3}Ga_{0.7}N$, 6 nm SiO_2 (sample 2130)*

For a better understanding of the shown transistor sample 1D Poisson-Schroedinger calculations were performed. The results are illustrated in **Fig.7.4**.

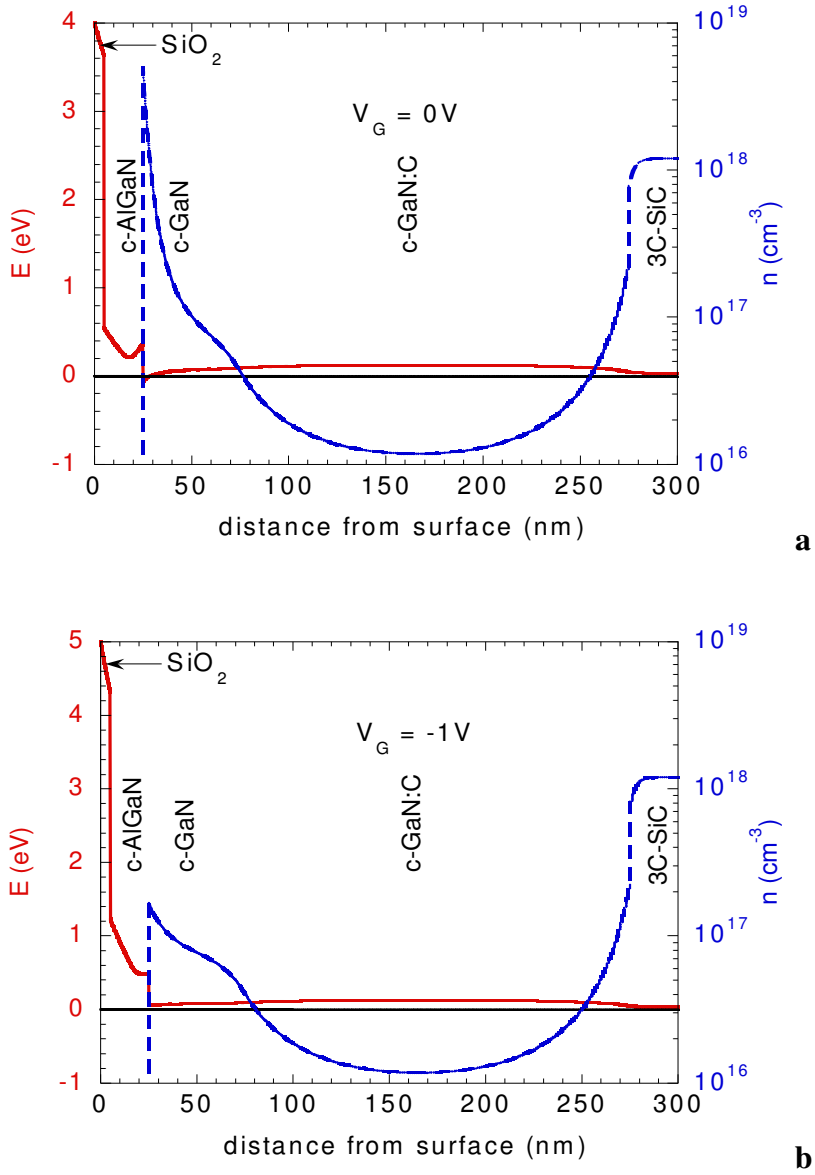
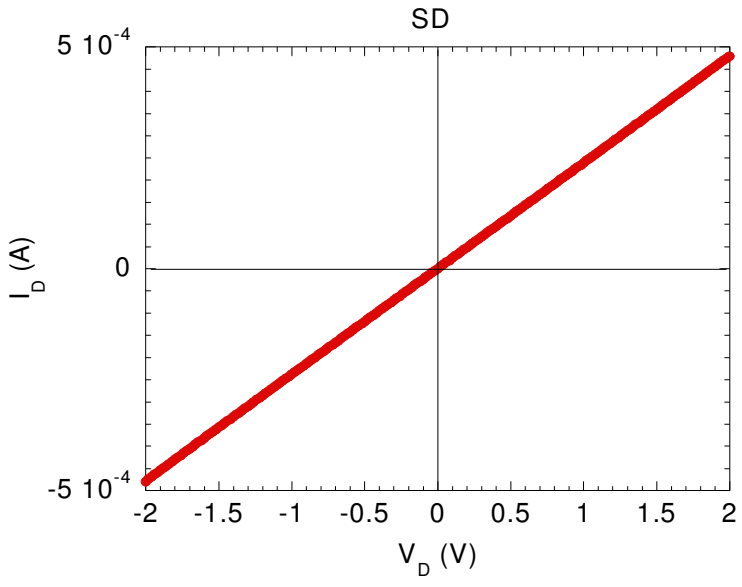


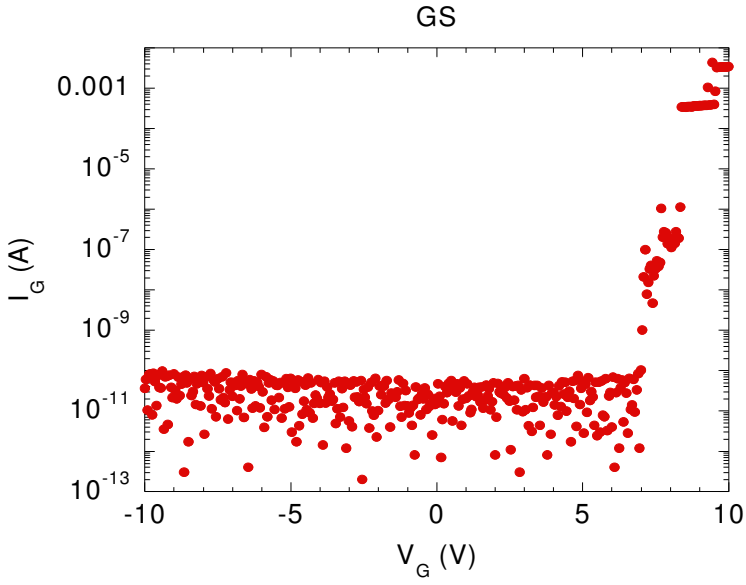
Figure 7.4 *1D Poisson-Schroedinger gamma point conduction band edge (red full line) and electron distribution (blue dashed line) as a function of the distance from surface of a MISHFET structure, black full line at E = 0 eV marks the Fermi level E_F;* **a** *at a gate voltage of V_G = 0 V and,* **b** *at a gate voltage of V_G = -1 V*

Gamma point conduction band edge and electron distribution are plotted vs. the distance from sample surface under the gate contact. Depletion mode behaviour of the fabricated transistor structure is illustrated by calculating the conduction band edge structure and free electron distribution at zero gate voltage (**Fig.7.4a**) and at negative gate voltage (**Fig.7.4b**). At V_G = 0 V the two dimensional electron channel at the c-AlGaN/GaN interface is filled and amounts approximately $n_{2D} = 5\text{x}10^{12}$ cm^{-2}. The conduction band edge at the hetero-interface is bended below the Fermi level E_F at E = 0 eV. This relatively high electron accumulation

originates from 6 nm of Si doped c-AlGaN layer as shown in **Fig7.2**. As a result the transistor device is normally-on. Applying negative gate voltages to the gate contact the electron channel can be depleted. This is shown in **Fig.7.4b** at a gate voltage of V_G = -1 V. As a result of the negative voltage at the gate contact the conduction band bends away from the Fermi level. This causes a depletion of the amount of electrons accumulated at the c-AlGaN/GaN interface. The 2D concentration is reduced to n_{2D} = 1.7x10^{11} cm^{-2}. This means by increasing negative gate voltage the transistor can be switched off.
To make sure that the insulation layer was removed from the source and drain contacts IV-measurements were done. The result is shown in **Fig.7.5a**. The IV curve shows a symmetrical, ohmic behavior.



a



b

Figure 7.5 *IV characteristics of* **a** *source-drain contacts and* **b** *source gate contacts*

On the other hand the gate to source IV-measurement shows a rectifying behavior, shown in **Fig.7.5b**. The current between -10 V and 7 V is in the range of 0.04 nA, so the transistor device is switchable in this wide voltage range without significant current flow through the gate.

Output characteristics of the fabricated transistor structure are shown in **Fig.7.6**. The source drain voltage is varied in a range of V_D = 0 V and V_D = +7 V. For all IV curves a linear increase of drain current is observed with increasing drain voltage. The results are comparable to those measured on h-AlGaN/GaN [84] and c-AlGaN/GaN [63] HFETs without a semi-insulating buffer. There are several approaches to explain the observed shunt current. One possibility is an insufficient electrical insulating properties of the carbon doped c-GaN layer, causing a parallel shunt current through the 3C-SiC substrate. Another explanation might be the parallel conductance of the UID c-GaN layer, caused by it`s relatively high background donor concentration. This assumption is confirmed by the Poisson calculation of the conduction band shown in **Fig.7.4a** and **b**.

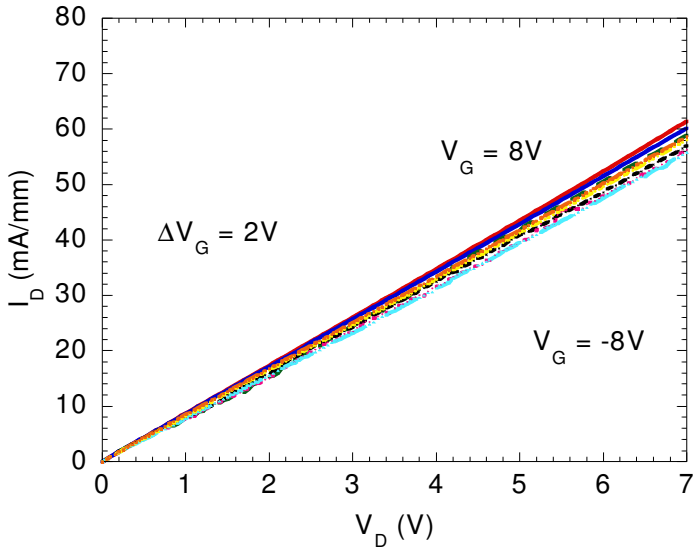


Figure 7.6 *MIS HFET output characteristics: Drain current I_D as a function of applied drain voltage V_D at gate voltages V_G between -8 V and +8 V*

Additionally, the diagram in **Fig.7.6** shows that the slope of the source-drain current varies as a function of the source-gate voltage. With increasing the gate voltage from -8 V to +8 V in ΔV_G = 1V steps the slope also increases by the field effect of the metal-insulator gate. To illustrate the field effect the source-drain current vs. source-drain voltage curve for a gate voltage of V_G = -4 V is subtracted from each other and the plotted again as a function of the gate voltage. This result is shown in **Fig.7.7**. Neglecting the influence of parallel conductivity a clear field effect can be observed.

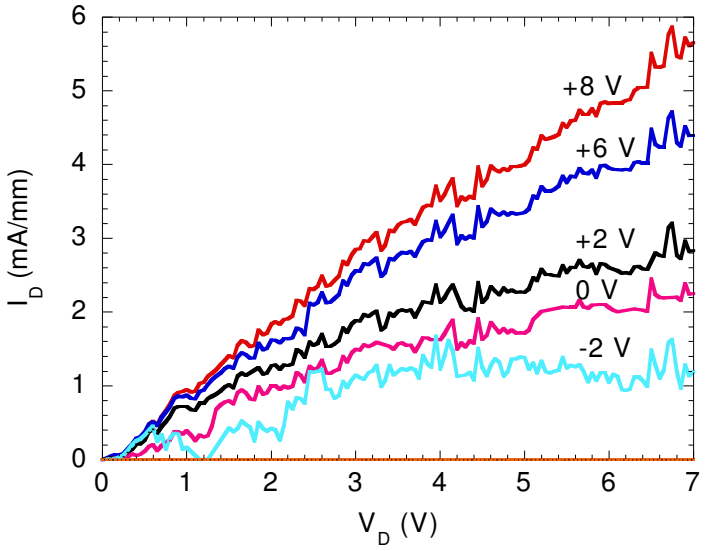


Figure 7.7 *Corrected MIS HFET output characteristics: Drain current I_D as a function of applied drain voltage V_D at gate voltages V_G between -4 V and +8 V; drain current at a gate voltage of -4 V was subtracted from drain current characteristic at higher gate voltages*

An additional feature is, that saturation of the drain current can be observed at approximately above V_D = +3 V, which is a clear evidence of a current transport via a 2D system caused by the c-AlGaN/GaN hetero-interface. At this voltage the channel reaches the maximum filling level with carriers and an increase of voltage cannot increase the current. The saturation current increases as a function of applied gate voltage due to the increasing depth of the 2DEG channel. This behaviour is demonstrated plotting the transfer characteristics of the fabricated device, which are shown in **Fig.7.8**.

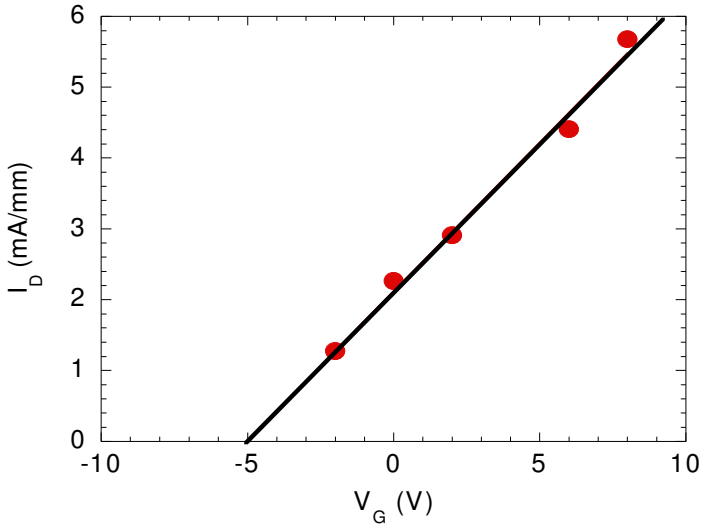


Figure 7.8 *MIS HFET transfer characteristics: Drain current I_D as a function of applied gate voltage V_G =-2 V to +8 V at a fixed drain voltage V_D = 7 V (red full circles), extrapolation (black solid line)*

Therefore the drain current is plotted as a function of gate voltage at a fixed drain voltage value of V_D = 10 V. The linear extrapolation to zero drain current of the measured data points yields a turn on or threshold voltage of -5.08 V. This result clearly indicates normally-on or depletion-mode behaviour of the fabricated device.
However, these results show that a not negligible shunt current is present in fabricated transistor device. The highly doped c-AlGaN:Si layer may cause a parallel current bypass, also the electrically separation between the active device and the highly conductive 3C-SiC substrate is insufficient. Additional insulating layers are required. Therefore a carbon doped asymmetrical c-AlN/GaN MQW structure is suggested as an effective insulation posisbility in the following chapter.

7.3 Enhancement mode c-AlGaN/GaN MIS-HFET

Enhancement (normally-off) mode c-AlGaN/GaN MIS-HFET device will be presented in the following discussion. **Fig.7.9** shows a schematic cross-sectional view of the grown sample. A 50 nm thick low conductive c-GaN:C buffer layer is grown on 3C-SiC substrate. For efficient electrical isolation between the active device and the highly conductive substrate an asymmetric c-AlN:C/GaN:C MQW structure was grown.The MQW structure consists of 10x1 nm c-GaN:C QWs included in 11x2.5 nm c-AlN:C barrier layers. CBr_4 BEP of $2x10^{-7}$ mbar was applied during buffer and the MQW growth. The structure is completed by 30 nm UID c-GaN forming a hetero structure with 25 nm c-$Al_{0.2}Ga_{0.8}N$ barrier layer and 6 nm SiO_2 gate insulator. The background donor concentrations in UID c-$Al_{0.2}Ga_{0.8}N$ is $5x10^{17}$ cm^{-3}. SiO_2 layer was deposited *ex-situ* by PECVD. Again for the source-and-drain contact application the insulating SiO_2 was removed by RIE. Gate contact consisting of 15 nm Ni and 50 nm Au was not thermally annealed. The ohmic source and drain contacts consist of a 15 nm/50 nm/15nm /50 nm Ti/Al/Ni/Au metal stack. They were thermally annealed for 30 s in nitrogen ambient at a temperature of 850 °C. Contacting the hetero-interface by deposited ohmic source and drain contacts is also indicated in **Fig.7.9**.

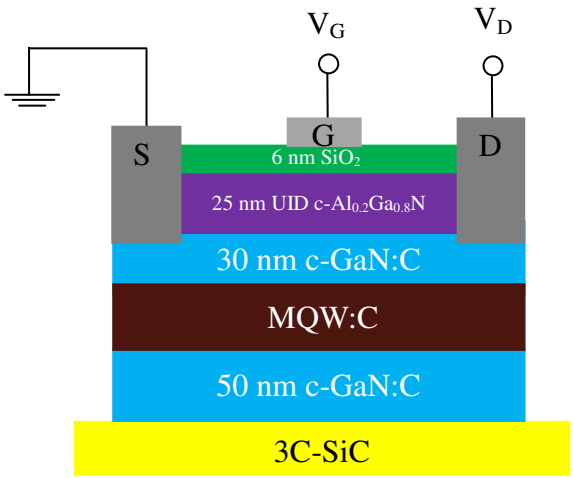


Figure 7.9 *Schematic cross sectional view of the fabricated metal insulator semiconductor hetero-junction field effect transistor structure; sample consists of 3C-SiC substrate, 50 nm c-GaN:C, 48 nm carbon doped asymmetric c-AlN/GaN MQW structure, 30 nm c-GaN:C, 25 nm UID c-$Al_{0.2}Ga_{0.8}N$, 6 nm SiO_2 (sample no. 2292)*

To confirm the normally-off characteristics of the design shown in **Fig.7.9** 1D Poisson-Schroedinger calculations were performed. The results are illustrated in **Fig.7.10**. Gamma point conduction band edge and free electron distribution are plotted as a function of the distance from sample surface. Two different gate voltages were applied at the gate contact to highlight the depletion mode transistor operation. At gate voltage of V_G = 0 V (**Fig.10a**) no electron accumulation is observable at the cAlGaN/GaN interface. This is the consequence of the conduction band alignment at zero gate voltages. The potential trap for electrons at the hetero-interface is shallow and the conduction band is above the Fermi level E_F at E = 0 eV.

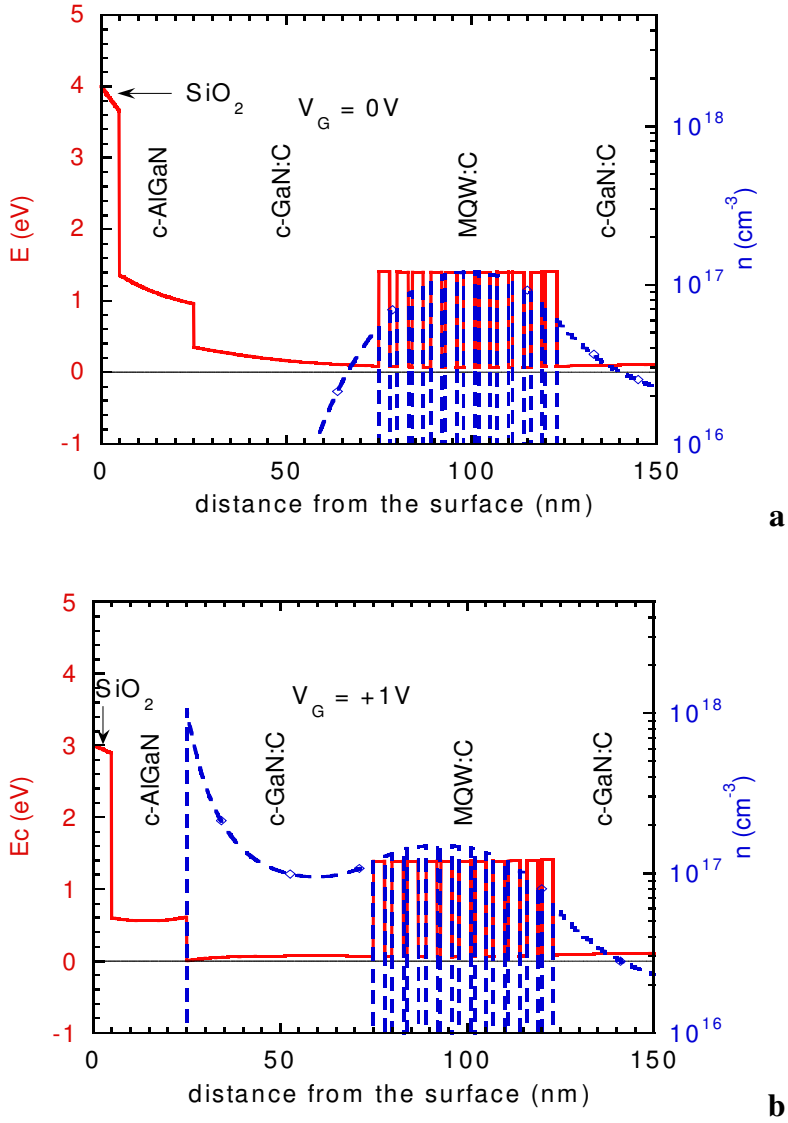


Figure 7.10 *1D Poisson- Schroedinger gamma point conduction band edge (red full line) and electron distribution (blue dashed line) as a function of the distance from surface of a MISHFET structure, black full line at E = 0 eV marks the Fermi level E_F;* **a** *at a gate voltage of V_G = 0 V and,* **b** *at a gate voltage of V_G = 1 V*

Therefore the condition for a normally-off transistor is fulfilled. The 2D electron channel is completely depleted at zero gate voltage.
The situation is different at V_G = +1 V. The conduction band edge bends towards E_F. As a consequence electron accumulation occurs at the c-AlGaN/GaN hetero-interface. The electron concentration is increased to approximately n_{2D} = 1x10^{12} cm^{-2} forming a conductive channel for the transistor operation. Increasing the positive gate voltage will lead to a further increase of the 2D electron amount at the interface and consequently the drain current increases. This behaviour is typical for an enhancement-mode transistor device.
As already described in chapter 7.2 IV curves were recorded between source-and-drain and source-and-gate contacts. The results are shown in **Fig.7.11**. The IV curve shows a symmetrical and ohmic behavior.

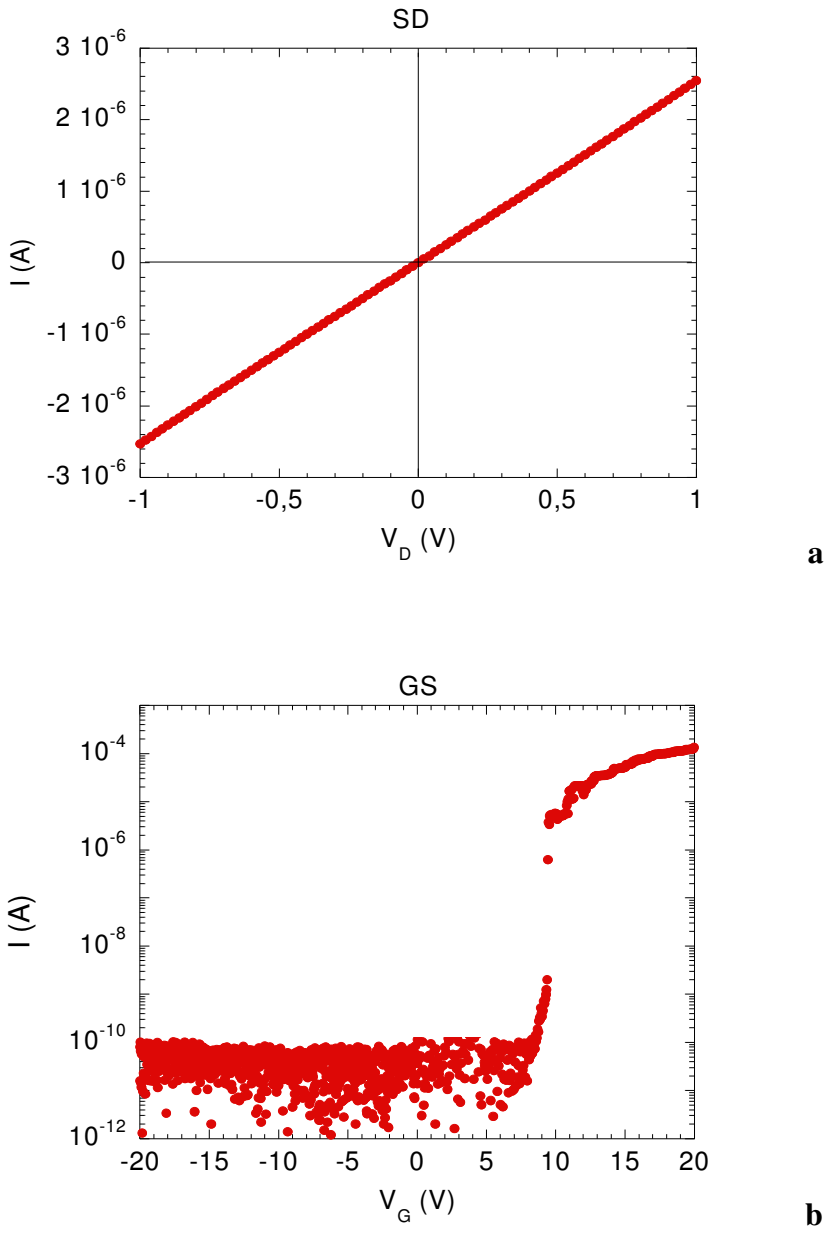


Figure 7.11 IV characteristics of **a** source-drain contacts and **b** source-gate contacts

Compared to the source-drain IV curve of transistor device shown in chapter 7.2 the current is reduced by two orders of magnitude. This observation is mainly caused by two factors. The first one is the absence of the Si doped c-AlGaN layer. The second factor is probably a decreased shunt current through the 3C-SiC substrate. This is caused by the higher insulating property of carbon doped MQW structure compared to a simple c-GaN:C layer as it was carried out in chapter 6. Gate to source IV curve shows rectifying behavior (**Fig.7.5b**). The current between -20 V and 9 V is in the range of 0.13 nA, so the transistor device is switchable in this wide voltage range without significant current flow through the gate contact.

In **Fig.7.12** output characteristics of the fabricated transistor device are illustrated. Drain current is plotted as a function of the drain voltage between V_D = 0 V and V_D = 3 V. The gate voltage was varied between V_G = -3 V to V_G = 4 V in 1 V steps. Drain current increases with increasing gate voltage. All measured I-V curves show a non-linear increase with different slopes. These output characteristics are unconventional. Additionally no saturation current was observed. We believe this behaviour originates from high serial contact resistivity of source and drain contacts placed on top of the c-$Al_{0.2}Ga_{0.8}N$ layer. This transistor output characteristics were also observed in ref. [63], which were also explained by non ohmic behaviour of the source and drain contacts. The high resistivity of the contacts is also observable in the relatively low drain current. It is in the range of 5 µA/mm to 40 µA/mm. Of course scattering effects like acoustic phonon scattering, impurity and donor scattering and dislocation scattering [83, 84] play also a role. A not negligible scattering mechanism is the c-AlGaN/GaN hetero-interface roughness scattering. It was carried out in ref. [85], that interface roughness scattering is the most important scattering mechanism in cAlGaN/GaN hetero-structures.

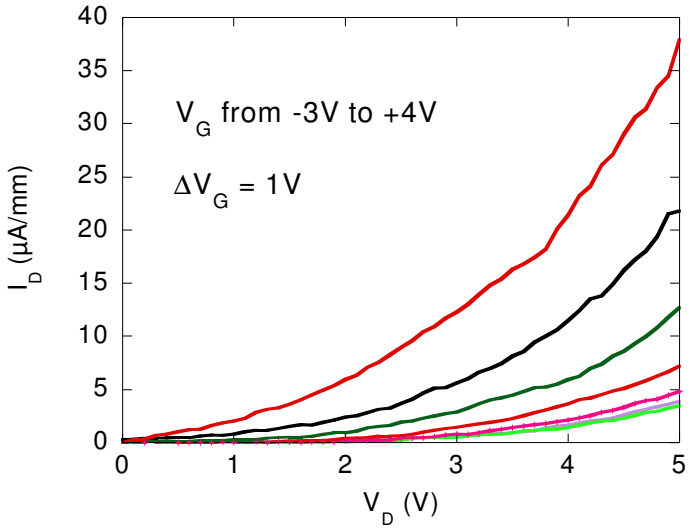


Figure 7.12 *MIS HFET output characteristics: Drain current I_D as a function of applied drain voltage V_D at gate voltages V_G between -3 V and +4 V*

Nevertheless, a clear field effect is observable in our measurements. Drain current I_D increases with increasing the gate voltage V_G. A transistor device is fabricated with normally-off behaviour. Transfer characteristics are illustrated in **Fig.7.13**. At gate voltages below V_G = 2 V the drain current is very low I_D < 5 µA/mm. A rapid increase of the drain current occurs at a gate voltage of V_G = 2 V and above. The transistor threshold voltage is approximately at V_{th} = 1.9 V. This positive value of the threshold voltage is a clear evidence for normally-off or enhancement mode transistor operation. A threshold voltage of +1.9 V achieved in this work is much higher than reported in c-AlGaN/GaN system with V_{th} = 1.2 V [63], c-plane hexagonal system with V_{th} = 0.4 V [86], and a-plane hexagonal system with V_{th} = -0.5 V [87] with gate length of L_G = 2 µm. This feature is desirable for save circuit designs.

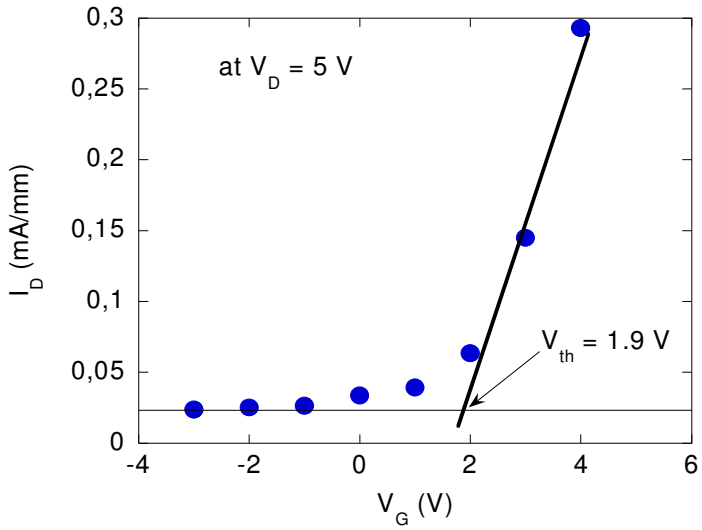


Figure 7.13 *MIS HFET transfer characteristics: Drain current I_D as a function of applied gate voltage V_G at a fixed drain voltages V_D = 5 V (blue full circles), extrapolation (black solid line)*

8.Summary

The aim of this work was to carry out the possibilities to improve c-AlGaN/GaN based field effect transistor devices. Although the molecular beam epitaxy of cubic GaN is already well investigated and optimized in previous works, the improvements consider the problems of leakage current caused by gate leakage and shunt current caused by parallel conductance of UID c-GaN buffer and the highly conductive 3C-SiC substrate. The establishment of device fabrication process including a gate insulator was successfully carried out. Carbon doping and the possibility of a cubic AlN/GaN multi quantum well structure were investigated. Effective electrical separation between the active device and the substrate is achieved.

Phase-pure cubic $Al_xGa_{1-x}N$/GaN structures were fabricated using rf-plasma assisted molecular beam epitaxy. The growth process was controlled by the reflection of high energy electron diffraction. Phase purity and surface roughness were investigated by high resolution x-ray diffraction and by atomic force microscopy, respectively. Information about depth profiles and composition of our samples were delivered by secondary ion mass spectroscopy. Electrical investigations were performed by admittance spectroscopy, capacitance voltage and current-voltage measurements. The device fabrication was achieved by using standard UV lithography, thermal evaporation of contact metals, reactive ion etching and plasma enhanced chemical vapour deposition.

For effective gate insulation *in-situ* and *ex-situ* insulator deposition were compared. Si_3N_4 was successfully deposited *in-situ* within the MBE chamber directly after growth of cubic GaN/AlGaN. Best isolating Si_3N_4 layers deposited by molecular beam epitaxy at a substrate temperature of 600 °C were found. With admittance spectroscopy, interface trap densities were investigated. Best results were achieved in *in-situ* deposited Si_3N_4 with $D_{it} = 2.5x10^{12}$ $cm^{-2}eV^{-1}$ and *ex-situ* plasma assisted chemical vapour deposited SiO_2 with $D_{it} = 2x10^{10}$ $cm^{-2}eV^{-1}$ fabricated at low SiH_4 and N_2O fluxes. All detected interface related defect states are located between 0.2 eV and 0.4 eV below E_C. We assume that these defects are caused by Ga dangling bonds, which capture electrons and therefore act as acceptors. However, slow deposition rate SiO_2 was successfully used as gate insulator, no gate leakage current was observed.

Several methods of protection of the transistor device from shunt current caused by parallel conductance of UID c-GaN buffer and the 3C-SiC substrate were discussed in this work. It turned out that carbonized 3C-SiC/Si substrates are not suitable for field effect transistor devices based on c-AlGaN/GaN. The extremely high dislocation density measured by the high resolution x-ray diffraction method in the order of 10^{10} cm^{-2} to 10^{11} cm^{-2} prohibits an efficient transistor operation. Additionally Hall-effect analysis yielded p-type conductivity in c-GaN layers grown on 3C-SiC/Si substrates. This feature is disadvantageous for n-type HFET application. Due to structural advantages of c-AlGaN/GaN layers in terms of dislocation density and surface smoothness the high conductive 3C-SiC substrate was used for growth.

Carbon doping of c-GaN was realized using CBr_4 as a carbon source, which was directly connected to the MBE chamber. An incorporated carbon concentration of $1x10^{20}cm^{-3}$ was achieved without degradation of the crystalline properties of c-GaN. A decrease of the net donor concentration with increased carbon concentration and a surplus of net acceptor concentration at carbon densities higher than $10^{19}cm^{-3}$ were observed. It was shown that carbon doping causes a decrease of c-GaN:C conductance by two orders of magnitude at carbon densities lower than $5x10^{19}cm^{-3}$. At higher carbon concentrations the conductance of c-GaN:C increases again, yielding p-type conductivity. However, at moderate carbon fluxes a reduction of conductivity of c-GaN:C layers was observed. Also very promising results were reached by developing the first cubic GaN:C/GaN/3C-SiC pn-junction diodes. Rectifying current-voltage characteristics were observed.

A further possibility of an electrical isolation between the active device and the substrate was investigated by growing of c-AlN/GaN and c-AlN/GaN:C multi quantum well structure on top of UID c-GaN buffer layer. The Layer thicknesses of the grown MQW structure were accurately controlled by RHEED. Current-voltage characteristics measured parallelly to growth direction [001] at c-AlN/GaN:C structures have shown a reduction of serial conductivity of six orders of magnitude compared to UID c-GaN layers.

FET and MIS HFET structures were realized based on c-GaN and c-AlGaN/GaN grown on free standing 3C-SiC. Field effect transistor operation was realized using a UID c-GaN/GaN:C/3C-SiC structure. Calculated and measured output characteristics are comparable using a mobility value of μ = 5 cm²/Vs. This relatively low mobility is caused by several electron scattering mechanisms. Mainly the low value is due to a relatively high dislocation density in c-GaN/3C-SiC structures.

Both depletion mode and enhancement mode MIS HFET devices were realized based on c-AlGaN/GaN/3C-SiC system. A positive threshold voltage of V_{th} = 1.9 V was achieved in a normally-off HFET device which is desirable for save circuits.

My results also exhibited that the ohmic contact technology has to be improved in future works. The unconventional transistor output characteristics showed no or insufficient saturation behaviour. This is probably caused by a relatively high contact resistance. For example, Si ion implantation has to be considered for source-and-drain application. Also the possibility of applying a self-aligned gate technology is thinkable.

Another possible improvement to the transistor devices is a replacement of the UV lithography by electron beam lithography to down scale the device dimensions. Smaller spacing between source-and-drain causes less scattering of charge carriers, consequently the electron mobility and therefore the device performance increases.

Appendix

Appendix I: List of Abbreviations

2DEG	Two Dimensional Electron Gas
AFM	Atomic Force Microscope/Microscopy
BEP	Beam Equivalent Pressure
BOE	Buffer Oxide Etching
c-$Al_xGa_{1-x}N$	Cubic $Al_xGa_{1-x}N$
c-AlN	Cubic AlN
c-GaN	Cubic GaN
CV	Capacitance Voltage
D	Drain
DBR	Distributed Bragg Reflector
dir	Direct (Bandgap)
ECV	ElectrochemicalCapacitance Voltage
EIT	Equivalent Insulator Thickness
FET	Field Effect Transistor
FWHM	Full Width of Half Maximum
G	Gate
HBT	Hetero- junction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HFET	Hetero- junction Field Effect Transistor
HRXRD	High Resolution X Ray Diffraction
ind	Indirect (Bandgap)
IV	Current Voltage
LD	Laser Diode
LED	Light Emitting Diode
MBE	Molecular Beam Epitaxy
MESA	Free standing structure on one substrate
MESFET	Metal Semiconductor Field Effect Transistor
MISFET	Metal Insulator Field Effect Transistor
MISHFET	Metal Insulator Semiconductor Hetero- junction Field Effect Transistor
MODFET	Modulation Doped Field Effect Transistor
MOCVD	Metal Organic Chemical Vapour Deposition
MQW	Multiple Quantum Well
n-channel	Electron Channel
PAMBE	Plasma Assisted Molecular Beam Epitaxy
PECVD	Plasma Enhanced Chemical Vapour Deposition
PL	Photoluminescence
QMS	Quadrupole Mass Spectrometer
QW	Quantum Well
rf	Radio Frequency
RHEED	Reflection High Energy Electron Diffraction
RIE	Reactive Ion Etching
RSM	Reciprocal Space Map
RTA	Rapid Thermal Annealing
RT	Room Temperature
S	Source
SCU	Scale Units (needle valve at CBr_4 source)
SIMS	Secondary Ion Mass Spectroscopy

TLM	Transition Line Method
UHV	Ultra High Vacuum
UID	Unintentional Doping/Doped
UV	Ultraviolet
VCSEL	Vertical Cavity Surface Emitting Laser

Appendix II: List of Symbols

Symbol	Description	Unit
A	Area	cm^2
a_0	Lattice Parameter	Å
a	Channel Depth	nm
B	Magnetic Induction	T
b	Bowing Parameter	eV
$\|b\|$	Absolute Value of the Burgers Vector	Å
C	Capacity	F
C_D	Depletion Capacitance	F
C_{in}	Insulator Capacitance	F
C_{it}	Interface Trap Capacitance	F
c	Lattice Parameter	Å
D	Dislocation Density	cm^{-2}
d	Layer Thickness	nm
d_{hkl}	Spacing of the Lattice Planes	nm
D_{it}	Interface Trap Density	$eV^{-1}cm^{-2}$
E_C	Conduction Band Edge	eV
E_F	Fermi Level	eV
E_g	Gap Energy	eV
E_{it}	Interface Trap Energy Level	eV
E_V	Valence Band Edge	eV
F	Electric Field	V/cm
f_P	van der Pauw Correction Factor	-
f	Frequency	Hz
F_C	Carbon Flux	$s^{-1}cm^{-2}$
g_m	Transconductance	Ω^{-1}
G_P	Parallel Conductance	Ω^{-1}
h	Depletion Depth	nm
hkl	Miller Indices Triplet	-
J	Current Density	A/cm^2
I	Current	A
I_D	Drain Current	A
I_{Dsat}	Saturation Drain Current	A
I_G	Gate Current	A
k_B	Boltzmann Constant	J/K
L_G	Gate/Channel Length	µm
N_A	Acceptor Concentration	cm^{-3}
N_C	Conduction Band Effective Density of States	cm^{-3}
N_D	Donor Concentration	cm^{-3}
n	Free Electron Concentration	cm^{-3}
n_{2DEG}	Two Dimensional Electron Gas Concentration	cm^{-2}
P	Pressure	mbar
p	Free Hole Concentration	cm^{-3}
Q	Electronic Charge	C
Q_{it}	Interface Trapped Charge	C
Q_m	Mobile Charge	C
q	Single Electron Charge	C
R	Resistivity	Ω

R_H	Hall Coefficient	$C^{-1}cm^{-3}$
R_{it}	Interface Trap Resistivity	Ω
Sq	Root Mean Square Roughness	nm
T	Temperature	K
t_{in}	Insulator Thickness	nm
V	Voltage	V
V_{bi}	Built- in Voltage	V
V_D	Drain Voltage	V
V_{fb}	Flat Band Voltage	V
V_G	Gate Voltage	V
V_P	Pinch- off Voltage	V
V_T	Threshold Voltage	V
v_{th}	Electron Thermal Velocity	cm/s
x	Al mole fraction in AlGaN	%
x	Length	µm
Y	Admittance	Ω^{-1}
y	Depletion Width	nm
Z	Channel Width	µm
z_{CV}	Distance from Sample Surface	nm
ΔE_C	Conduction Band Discontinuity	eV
$\Delta\omega$	Full Width at Half Maximum	arcmin
ε_0	Electric Field Constant	$AsV^{-1}m^{-1}$
ε_s	Semiconductor Permittivity	-
Φ_b	Energy Barrier	eV
λ	Wavelength	nm
μ	Mobility	$cm^2V^{-1}s^{-1}$
ρ	Specific Layer Resistance	Ωcm
ρ	Charge Density	C/cm^3
σ	Specific Layer Conductance	$(\Omega cm)^{-1}$
σ_{0n}	Capture Cross Section	cm^2
τ_{it}	Interface Trap Lifetime	s
θ_m	Diffraction Angle	°
Ψ	Energy Separation (Conduction Band Edge – Fermi Level)	eV
ω_m	Angle of Incidence	°
ω	Angular Frequency	Hz

Appendix III: List of Samples

Note: The first layer in column “Sample Structure” is the first layer grown on substrate.

Sample Number	Substrate Declaration	Substrate Type	Sample Structure
1891	100-C500	3C-SiC/Si	960 nm c-GaN
1909	100-C500	3C-SiC/Si	690 nm c-GaN (T_S = 682 °C)
1910	100-C500	3C-SiC/Si	680 nm c-GaN (T_S = 669 °C)
1911	100-C500	3C-SiC/Si	680 nm c-GaN (T_S = 690 °C)
1912	100-C500	3C-SiC/Si	680 nm c-GaN (T_S = 701 °C)
1913	100-C500	3C-SiC/Si	680 nm c-GaN (T_S = 710 °C)
1914	100-C500	3C-SiC/Si	680 nm c-GaN(T_S = 719 °C)
1915	100-C500	3C-SiC/Si	680 nm c-GaN(T_S = 719 °C)
1916	100-C500	3C-SiC/Si	680 nm c-GaN(T_S = 731 °C)
1917	100-C500	3C-SiC/Si	680 nm c-GaN(T_S = 737 °C)
1957	SFB 21AA	3C-SiC	380 nm c-GaN
1958	SFB 21AA	3C-SiC	60 nm c-GaN 270 nm c-GaN:C (10 SCU) 40 nm c-GaN
1959	SFB 21AA	3C-SiC	60 nm c-GaN 230 nm c-GaN:C(15 SCU) 60 nm c-GaN
1960	SFB 21AA	3C-SiC	60 nm c-GaN 200 nm c-GaN:C (15 SCU) 120 nm c-GaN
1961	SFB 21AA	3C-SiC	60 nm c-GaN 100 nm c-GaN:C (20 SCU) 120 nm c-GaN
1962	SFB 21AA	3C-SiC	60 nm c-GaN 355 nm c-GaN:C (15 SCU) 120 nm c-GaN:Si (T_{Si} = 1050 °C)
1963	SFB 21AA	3C-SiC	520 nm c-GaN
1995	PC 570a	3C-SiC/Si	1050 nm c-GaN:Si (T_{Si} = 1050 °C)
1996	SFD 03 AF	3C-SiC	580 nm c-GaN
1997	PC 575a	3C-SiC/Si	580 nm c-GaN
1998	SFD 03 AF	3C-SiC	80 nm c-GaN 530 nm c-GaN:C (8 SCU)
1999	SFD 03 AF	3C-SiC	80 nm c-GaN 530 nm c-GaN:C (6 SCU)
2000	SFD 03 AF	3C-SiC	80 nm c-GaN 530 nm c-GaN:C (4 SCU)
2001	SFD 03 AF	3C-SiC	80 nm c-GaN 530 nm c-GaN:C (2 SCU)
2002	SFD 03 AF	3C-SiC	80 nm c-GaN 530 nm c-GaN:C (10 SCU)
2003	SFD 03 AF	3C-SiC	80 nm c-GaN 320 nm c-GaN:C (15 SCU)
2004	SFD 03 AF	3C-SiC	80 nm c-GaN 530 nm c-GaN:C (12 SCU)

2005	PC 575a	3C-SiC/Si	80 nm c-GaN 530 nm c-GaN:C (4 SCU)
2006	PC 575a	3C-SiC/Si	80 nm c-GaN 530 nm c-GaN:C (6 SCU)
2007	PC 575a	3C-SiC/Si	80 nm c-GaN 530 nm c-GaN:C (8 SCU)
2024	SFD 03 AF	3C-SiC	80 nm c-GaN 70 nm c-GaN:C (2SCU) 70 nm c-GaN 70 nm c-GaN:C (4SCU) 70 nm c-GaN 70 nm c-GaN:C (6SCU) 70 nm c-GaN 70 nm c-GaN:C (8SCU) 70 nm c-GaN 70 nm c-GaN:C (10SCU) 70 nm c-GaN 70 nm c-GaN:C (12SCU)
2025	SFD 03 AF	3C-SiC	570 nm c-GaN 225 nm c-AlN
2028	SFD 03 AF	3C-SiC	600 nm c-GaN 8 h 20 min SiN (T_{Si} = 1300 °C, T_S = 300 °C)
2043	SFD 03 AF	3C-SiC	8 h SiN (T_{Si} = 1300 °C, T_S = 300 °C)
2050	100-C615	3C-SiC/Si	475 nm c-GaN
2051	UP-10-02	3C-SiC/Si	580 nm c-GaN
2052	UP-10-02	3C-SiC/Si	85 nm c-GaN 255 nm c-GaN:Si (T_{Si} = 1010 °C) 255 nm c-GaN:C (10 SCU)
2053	UP-10-02	3C-SiC/Si	80 nm c-GaN 425 nm c-GaN:C (10 SCU) 80 nm c-GaN:Si (T_{Si} = 1010 °C)
2054	UP-10-02	3C-SiC/Si	40 nm c-GaN 410 nm c-GaN:C (10 SCU)
2055	PC 606a	3C-SiC/Si	1075 nm c-GaN
2056	PC 604a	3C-SiC/Si	1080 nm c-GaN
2057	PC 603a	3C-SiC/Si	1045 nm c-GaN
2058	PC 602a	3C-SiC/Si	1090 nm c-GaN
2065	PC 602a	3C-SiC/Si	1200 nm c-GaN
2084	PC 602a	3C-SiC/Si	100 nm c-GaN 20 nm c-$Al_{0.1}Ga_{0.9}N$
2085	PC 602a	3C-SiC/Si	100 nm c-GaN 20 nm c-$Al_{0.1}Ga_{0.9}N$
2086	PC 602a	3C-SiC/Si	100 nm c-GaN 20 nm c-$Al_{0.1}Ga_{0.9}N$
2087	PC 602a	3C-SiC/Si	100 nm c-GaN 20 nm c-$Al_{0.15}Ga_{0.85}N$
2088	PC 602a	3C-SiC/Si	100 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$
2089	PC 602a	3C-SiC/Si	120 nm c-GaN

2090	PC 602a	3C-SiC/Si	1000 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$
2091	PC 602a	3C-SiC/Si	100 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$
2092	PC 602a	3C-SiC/Si	200 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$
2093	PC 602a	3C-SiC/Si	200 nm c-GaN 4 nm c-$Al_{0.3}Ga_{0.7}N$ 6 nm c-$Al_{0.3}Ga_{0.7}N$:Si (T_{Si} = 1042 °C) 10 nm c-$Al_{0.3}Ga_{0.7}N$
2094	PC 618a	3C-SiC/Si	700 nm c-GaN (T_{Si} = 1042 °C)
2105	SFE 29 AL	3C-SiC	650 nm c-GaN 4 h SiN (T_{Si} = 1300 °C, T_S = 300 °C)
2106	SFE 29 AL	3C-SiC	650 nm c-GaN 2 h SiN (T_{Si} = 1300 °C, T_S = 300 °C)
2107	SFE 29 AL	3C-SiC	650 nm c-GaN 1 h SiN (T_{Si} = 1300 °C, T_S = 300 °C)
2120	SFE 29 AL	3C-SiC	650 nm c-GaN
2121	SFE 29 AL	3C-SiC	650 nm c-GaN 1 h SiN (T_{Si} = 1300 °C, T_S = 400 °C)
2122	SFE 29 AL	3C-SiC	650 nm c-GaN 1 h SiN (T_{Si} = 1300 °C, T_S = 500 °C)
2123	SFE 29 AL	3C-SiC	650 nm c-GaN 1 h SiN (T_{Si} = 1300 °C, T_S = 600 °C)
2124	SFE 29 AL	3C-SiC	650 nm c-GaN 1 h SiN (T_{Si} = 1300 °C, T_S = 700 °C)
2125	SFE 29 AL	3C-SiC	250 nm c-GaN
2126	SFE 29 AL	3C-SiC	265 nm c-GaN:C (5 SCU)
2127	SGM 01 AC	3C-SiC	200 nm c-GaN 4 nm c-$Al_{0.3}Ga_{0.7}N$ 6 nm c-$Al_{0.3}Ga_{0.7}N$:Si (T_{Si} = 1047 °C) 10 nm c-$Al_{0.3}Ga_{0.7}N$
2128	SGM 01 AC	3C-SiC	200 nm c-GaN 4 nm c-$Al_{0.3}Ga_{0.7}N$ 6 nm c-$Al_{0.3}Ga_{0.7}N$:Si (T_{Si} = 1047 °C) 10 nm c-$Al_{0.3}Ga_{0.7}N$ 50 min SiN (T_{Si} = 1300 °C, T_S = 600 °C)
2129	SGM 01 AC	3C-SiC	150 nm c-GaN:C (6 SCU) 50 nm c-GaN 4 nm c-$Al_{0.3}Ga_{0.7}N$ 6 nm c-$Al_{0.3}Ga_{0.7}N$:Si (T_{Si} = 1047 °C) 10 nm c-$Al_{0.3}Ga_{0.7}N$ 50 min SiN (T_{Si} = 1300 °C, T_S = 600 °C)
2130	SGM 01 AC	3C-SiC	200 nm c-GaN:C (6 SCU) 50 nm c-GaN 4 nm c-$Al_{0.3}Ga_{0.7}N$ 6 nm c-$Al_{0.3}Ga_{0.7}N$:Si (T_{Si} = 1047 °C) 10 nm c-$Al_{0.3}Ga_{0.7}N$
2134	PC 618a	3C-SiC/Si	400 nm c-GaN
2135	PC 618a	3C-SiC/Si	200 nm c-GaN

2136	PC 618a	3C-SiC/Si	100 nm c-GaN
2137	PC 618a	3C-SiC/Si	50 nm c-GaN
2138	PC 618a	3C-SiC/Si	25 nm c-GaN
2139	PC 618a	3C-SiC/Si	12.5 nm c-GaN
2140	PC 618a	3C-SiC/Si	430 nm c-GaN:Si (T_{Si} = 954 °C)
2141	PC 618a	3C-SiC/Si	430 nm c-GaN:Si (T_{Si} = 993 °C)
2142	PC 618a	3C-SiC/Si	430 nm c-GaN:Si (T_{Si} = 1010 °C)
2143	Sapphire	Al_2O_3	50 nm h-GaN 500 nm h-GaN:C (8 SCU) 50 nm h-GaN
2144	PC 618a	3C-SiC/Si	430 nm c-GaN:C (8 SCU)
2145	PC 618a	3C-SiC/Si	430 nm c-GaN:C (6 SCU)
2146	PC 618a	3C-SiC/Si	430 nm c-GaN:C (4 SCU)
2147	PC 618a	3C-SiC/Si	400 nm c-GaN 400 nm c-GaN:Si (T_{Si} = 948 °C)
2148	PC 618a	3C-SiC/Si	430 nm c-GaN:Si (T_{Si} = 1060 °C)
2149	PC 618a	3C-SiC/Si	1300 nm c-GaN
2150	PC 618a	3C-SiC/Si	650 nm c-GaN 55 nm c-GaN:Si (T_{Si} = 1060 °C)
2158	PC 618a	3C-SiC/Si	40 nm c-GaN 160 nm c-$Al_{0.25}Ga_{0.75}N$
2159	PC 618a	3C-SiC/Si	40 nm c-GaN 160 nm c-$Al_{0.6}Ga_{0.4}N$
2160	PC 618a	3C-SiC/Si	100 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$
2161	SGM 01 AC	3C-SiC	25 nm c-GaN 600 nm c-GaN:C (5 SCU)
2171	SGM 01 AC	3C-SiC	320 nm c-GaN
2172	SGM 01 AC	3C-SiC	25 nm c-GaN 200 nm c-GaN:C (5 SCU) 120 nm c-GaN
2173	SGM 01 AC	3C-SiC	25 nm c-GaN 200 nm c-GaN:C (6 SCU) 120 nm c-GaN
2174	SGM 01 AC	3C-SiC	25 nm c-GaN 200 nm c-GaN:C (7 SCU) 120 nm c-GaN
2175	PC 618a	3C-SiC/Si	650 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$
2176	PC 618a	3C-SiC/Si	100 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 10 nm c-GaN
2177	PC 618a	3C-SiC/Si	650 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 1 h SiN (T_{Si} = 1300 °C, T_S = 600 °C)
2219	SGM 01 AC	3C-SiC	600 nm c-GaN
2220	SGM 01 AC	3C-SiC	100 nm c-GaN 3 nm c-AlN 10 asym. MQWs 1 nm/2 nm c-GaN QWs

			3 nm c-AlNbarriers 55 nm c-GaN
2221	SGM 01 AC	3C-SiC	50 nm c-GaN 3 nm c-AlN 10 asym. MQWs 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 100 nm c-GaN
2222	SGM 01 AC	3C-SiC	50 nm c-GaN 3 nm c-AlN:C (6 SCU) 10 asym. MQWs 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 100 nm c-GaN
2223	SGM 01 AC	3C-SiC	25 nm c-GaN:C (6 SCU) 3 nm c-AlN 10 asym. MQWs 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN
2224	SGM 01 AC	3C-SiC	25 nm c-GaN 400 nm c-GaN:C (6 SCU) 600 nm c-GaN:C (8.5 SCU) 50 nm c-GaN:Si (T_{Si} = 1125 °C)
2225	SGM 01 AC	3C-SiC	25 nm c-GaN 400 nm c-GaN:C (6 SCU) 3 nm c-AlN 45 nm c-GaN:C (5 SCU) 10 nm c-GaN:Si (T_{Si} = 1125 °C)
2247	SFE 29 AL	3C-SiC	100 nm c-GaN 60 nm c-$Al_{0.2}Ga_{0.8}N$
2248	SFE 29 AL	3C-SiC	100 nm c-GaN 60 nm c-$Al_{0.25}Ga_{0.75}N$
2249	SFE 29 AL	3C-SiC	100 nm c-GaN 60 nm c-$Al_{0.3}Ga_{0.7}N$
2250	SFE 29 AL	3C-SiC	100 nm c-GaN 60 nm c-$Al_{0.35}Ga_{0.65}N$
2251	SFE 29 AL	3C-SiC	5 nm c-AlN 50 nm c-GaN 3 nm c-AlN:C (5 SCU) 10 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$
2252	SFE 29 AL	3C-SiC	50 nm c-GaN 3 nm c-AlN:C (5 SCU) 10 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers

			50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$
2253	SFE 29 AL	3C-SiC	50 nm c-GaN 3 nm c-AlN:C (5 SCU) 10 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$
2254	SFE 29 AL	3C-SiC	10 nm c-AlN 50 nm c-GaN 3 nm c-AlN:C (5 SCU) 10 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 5 nm c-GaN:Si (T_{Si} = 1070 °C)
2255	SFE 29 AL	3C-SiC	3 nm c-AlN:C (5 SCU) 10 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 5 nm c-GaN:Si (T_{Si} = 1070 °C)
2256	SGM 01 AC	3C-SiC	growth failed
2257	SGM 01 AC	3C-SiC	10 nm c-AlN:C (4 SCU) 50 nm c-GaN:C (5 SCU) 3 nm c-AlN:C (5 SCU) 10 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 5 nm c-GaN:Si (T_{Si} = 1120 °C)
2258	SGM 01 AC	3C-SiC	10 nm c-AlN:C (6 SCU) 50 nm c-GaN:C (6 SCU) 3 nm c-AlN:C (6 SCU) 10 asym. MQWs:C (6 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 5 nm c-GaN:Si (T_{Si} = 1120 °C)
2259	SGM 01 AC	3C-SiC	10 nm c-AlN:C (5 SCU) 50 nm c-GaN:C (5 SCU) 3 nm c-AlN:C (5 SCU) 10 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers

			50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 5 nm c-GaN:Si (T_{Si} = 1120 °C)
2260	SFJ 14 AK	3C-SiC	10 nm c-AlN:C (5 SCU) 50 nm c-GaN:C (5 SCU) 3 nm c-AlN:C (5 SCU) 10 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 5 nm c-GaN:Si (T_{Si} = 1100 °C)
2261	SFJ 14 AK	3C-SiC	10 nm c-AlN:C (5 SCU) 50 nm c-GaN:C (5 SCU) 3 nm c-AlN:C (5 SCU) 4 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 5 nm c-GaN:Si (T_{Si} = 1100 °C)
2262	SFJ 14 AK	3C-SiC	10 nm c-AlN:C (5 SCU) 10 nm c-$Al_{0.8}Ga0_{.2}N$ 10 nm c-$Al_{0.6}Ga_{0.4}N$ 10 nm c-$Al_{0.4}Ga_{0.6}N$ 10 nm c-$Al_{0.2}Ga_{0.7}N$ 10 nm c-$Al_{0.1}Ga_{0.9}N$ 50 nm c-GaN:C (5 SCU) 20 nm c-$Al_{0.3}Ga_{0.7}N$ 5 nm c-GaN:Si (T_{Si} = 1100 °C)
2263	SFJ 14 AK	3C-SiC	30 nm c-AlN
2264	SFJ 14 AK	3C-SiC	30 nm c-AlN:C (5 SCU)
2265	SGB 04 AG	3C-SiC	50 nm c-GaN:C (5 SCU) 3 nm c-AlN:C (5 SCU) 10 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 5 nm c-GaN:Si (T_{Si} = 1100 °C)
2266	SGB 04 AG	3C-SiC	50 nm c-GaN:C (5 SCU) 3 nm c-AlN:C (5 SCU) 10 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 5 nm c-GaN:Si (T_{Si} = 1100 °C)
2267	SGB 04 AG	3C-SiC	50 nm c-GaN:C (5 SCU) 2 nm c-AlN:C (5 SCU)

			10 asym. MQWs:C (5 SCU) 1 nm/2 nm c-GaN QWs 2 nm c-AlN barriers
2285	SHH 17 AB	3C-SiC	10 nm c-AlN 750 nm c-GaN
2286	SHH 17 AB	3C-SiC	215 nm c-GaN 20 nm c-$Al_{0.3}Ga_{0.7}N$ 5 nm c-GaN:Si (T_{Si} = 1100 °C)
2287	SJK 25 AE	3C-SiC	210 nm c-GaN:C (4 SCU) 15 nm c-GaN 10 nm c-$Al_{0.3}Ga_{0.7}N$
2288	SJK 25 AE	3C-SiC	210 nm c-GaN:C (5 SCU) 15 nm c-GaN 10 nm c-$Al_{0.3}Ga_{0.7}N$
2289	SJK 25 AE	3C-SiC	210 nm c-GaN:C (6 SCU) 15 nm c-GaN 10 nm c-$Al_{0.3}Ga_{0.7}N$
2290	SJK 25 AE	3C-SiC	210 nm c-GaN:C (7 SCU) 15 nm c-GaN 10 nm c-$Al_{0.3}Ga_{0.7}N$
2291	SJK 25 AE	3C-SiC	50 nm c-GaN:C (5 SCU) 3 nm c-AlN:C (5 SCU) 8 asym. MQWs:C (5 SCU) 1.5 nm/2.5 nm c-GaN QWs 3 nm c-AlN barriers 50 nm c-GaN:C (5 SCU) 15 nm c-GaN 10 nm c-$Al_{0.3}Ga_{0.7}N$
2292	SJK 25 AE	3C-SiC	50 nm c-GaN:C (5 SCU) 3 nm c-AlN:C (5 SCU) 10 asym. MQWs:C (5 SCU) 1.5 nm/2.5 nm c-GaN QWs 3 nm c-AlN barriers 30 nm c-GaN:C (5 SCU) 25 nm c-$Al_{0.2}Ga_{0.8}N$

Appendix IV: Poisson-Schrödinger-Solver

The 1D Poisson/Schrödinger program uses the finite-difference method for the one-dimensional band diagram of a semiconductor structure to be calculated. This method provides the ability for the numerical solution of ordinary and partial differential equations represent the program calculates band diagrams at various applied voltages and it is also able to determine CV characteristics. It is written for III-V compound semiconductors, but it is general enough to work for other material systems. The program is driven by a pseudo-Mac interface, but the user needs to use separate document processing and graphics processing programs. One outstanding feature of the program is that the semiconductors can be accessed with their "names". The program automatically searches the relevant physical parameters. The parameters for ternary compounds are calculated for a given content of the respective elements. Semiconductor in the "materials" file are divided into family classes so that parameters such as Band offsets are defined within this class, and do not interfere with the parameters of the other classes. The mobile charge concentrations are determined using the Boltzmann statistics. In addition, the Unger-approximation for weak degeneracy and Sommerfeld approximation is used for deep degeneracy, the dopant ionization is also considered. The charge distribution can be calculated as well with the Poisson equation. The program calculates both the course of the conduction band and the valence band as well as the electron and hole-concentration as a function of distance from the semiconductor surface. The dopant ionization is taken into account for the flat and the deep doping level. The current flow cannot be simulated, so the calculations are based only on the thermal equilibrium. Three possible boundary conditions can be defined for the semiconductor surface and the substrate: 1 Schottky barrier, 2nd ohmic contact, or 3 Energy band slope is zero. If a Schottky barrier is used, the program can simulate the effect of an applied voltage, which has no significant current flow to the sequence. An ohmic contact as a boundary condition is used, then the voltage applied to the Fermi level of the adjacent layer the same. The condition "zero slope" is selected, if the simulation is to be performed only for a limited area, which is relatively far away from the sample surface and from the substrate rear side. For example in a hetero-junction contact the interesting effects in the range of the transition. So it is not necessary, the sample structure of the sample to simulate the front side to the back of sample.
An example of a simulation input file for a HFET with included asymmetric MQW structure is given by following input file text:

Input	**Description**
#test comment	Simulation parameter description start
substrate v1	3C-SiC substrate
3C-SiC t=10000 Nd=3e18	
GaN t=50nm dy=1 Nd=1e17	c-GaN buffer layer
AlGaN t=3nm dy=1 x=1 Nd=1e18	asymmetrical MQW structure consisting of
GaN t=1nm dy=1 Nd=1e17	alterning c-AlN/GaN layers
AlGaN t=3nm dy=1 x=1 Nd=1e18	Nd is net donor concentration in cm^{-3}
GaN t=2nm dy=1 Nd=1e17	t is the layer thickness in nm
AlGaN t=3nm dy=1 x=1 Nd=1e18	dy is the increment
GaN t=1nm dy=1 Nd=1e17	of each calculation step in nm
AlGaN t=3nm dy=1 x=1 Nd=1e18	
GaN t=2nm dy=1 Nd=1e17	
AlGaN t=3nm dy=1 x=1 Nd=1e18	
GaN t=1nm dy=1 Nd=1e17	
AlGaN t=3nm dy=1 x=1 Nd=1e18	
GaN t=2nm dy=1 Nd=1e17	
AlGaN t=3nm dy=1 x=1 Nd=1e18	
GaN t=1nm dy=1 Nd=1e17	
AlGaN t=3nm dy=1 x=1 Nd=1e18	
GaN t=2nm dy=1 Nd=1e17	
AlGaN t=3nm dy=1 x=1 Nd=1e18	
GaN t=1nm dy=1 Nd=1e17	
AlGaN t=3nm dy=1 x=1 Nd=1e18	
GaN t=2nm dy=1 Nd=1e17	
AlGaN t=3nm dy=1 x=1 Nd=1e18	
GaN t=50nm dy=1 Nd=1e17	c-GaN layer
AlGaN t=20nm dy=1 x=0.25 Nd=5e17	c-$Al_xGa_{1-x}N$ barrier layer
surface schottky=0.9 v2	surface condition: Schottky barrier=0.9 eV
schrodingerstart=10500	find quantization between
schrodingerstop=10980	10500x0.1 nm and 10980x0.1 nm
v1 0.0	applied bias at v1 (substrate)
v2 0.0	and v2 (surface)
temp=300K	temperature

Hereby Nd is the measured or assumed background donor concentration, t is the layer thickness in nm, dy means the Poisson and Schödinger equation is solved every 0.1 nm counted from the substrate to the surface, x is the Al mole fraction, v1 and v2 mark the points bias voltage is applied (in this case v1 at the substrate and v2 at the surface Schottky contact), schrodingerstart and stop mark the thickness boundaries where Schödinger equation is solved (in this case it is the MQW structure between 10500x0.1 nm and 10980x0.1 nm). Since the transistor devices were characterized at room temperature, the simulation temperature was 300 K.

Appendix V: List of Figures

Appendix VI: List of Tables

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1. **A. Zado**, E. Tschumak, K. Lischka, and D.J. As: Electrical characterization of an interface n-type conduction channel in cubic AlGaN/GaN heterostructures, *physica status solidi* (c) **7** (1), 52 (2010)
2. **A. Zado**, E. Tschumak, J. Gerlach, K. Lischka, and D.J. As: Doping of MBE grown cubic GaN on 3C-SiC (001) by CBr_4, *AIP Conference Proceedings* **1292**, 181 (2010)
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7. D. Bouguenna, A. Boudghene Stambouli, **A. Zado**, D.J. As, N. Mekkakia Maaza: 2D Simulations of current-voltage characteristics of cubic $Al_xGa_{1-x}N$/GaN modulation doped hetero-junction field effect transistor structures, *Electrical and Electronic Engineering* **2** (5), 309 (2012)
8. **A. Zado** and D.J. As: Carbon doped asymmetric cubic AlN/GaN multi quantum well structures for high electrical isolation to 3C-SiC substrates, *physica status solidi* (c) **10** (3), 486 (2013)
9. D.J. As, **A. Zado**, Q.Y. Wei, T. Li, J.Y. Huang, and F.A. Ponce: Capacity voltage characteristics and electron holography on cubic AlGaN/GaN heterojunctions, *Japanese Journal of Applied Physics*, **52** (8), 08JN04 (2013)
10. D. Bouguenna, A. Boudhene Stambouli, N. Mekkakia Maaza, **A. Zado**, D.J. As: Comparative study on performance of cubic $Al_xGa_{1-x}N$/GaN nanostructures MODFETs and MOS-MODFETs, *Superlattices and Microstructures* **62**, 260 (2013)

Conference Contributions

06/2009	**European Materials Research Society** (Strassbourg, France) Symposium: Group III Nitride Semiconductors, poster presentation: "Electrical characterization of the 2-DEG in cubic AlGaN/GaN heterostructures"
06/2010	**European Materials Research Society** (Strassbourg, France) Symposium: Wide Band-gap Cubic Semiconductors: from growth to devices, poster presentation: "Doping of MBE grown cubic GaN on 3C-SiC (001) by CBr_4"
08/2010	**International Conference on Molecular Beam Epitaxy** (Berlin, Germany) Poster presentation: "Carbon as an acceptor in cubic GaN/3C-SiC (001)"
05/2011	**European Materials Research Society** (Nice, France) Symposium: Group III nitrides and their hetero-structures for electronics and photonics, oral presentation: "Electrical properties of MBE grown Si_3N_4 – cubic GaN MIS structures"
07/2012	**International Symposium on Group III – Nitrides** (St. Petersburg, Russia) Poster presentation: "Carbon doped asymmetric cubic AlN/GaN multi quantum well structures for high electrical isolation to 3C-SiC substrates"

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