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Digital Control for Interleaved Boost Power Factor Correction (PFC) Rectifiers

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» Flick of the switch «

AC/DC

Vorwort

Diese Arbeit entstand während meiner Tätigkeit als wissenschaftlicher Mitarbeiter am Fachgebiet „Leistungselektronik und Elektrische Antriebstechnik (LEA)“ an der Universität Paderborn, wobei große Teile in enger Zusammenarbeit mit der Delta Energy Systems (Germany) GmbH entstanden sind.

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Tobias Grote

Köterberg, im April 2014

Abstract

Rectifiers with low power factor cause line interferences due to harmonics in the line current and reactive power and therefore reduce the power available from the grid. For this reason power factor correction (PFC) rectifiers have been established as front end stage of AC-DC converters, which should emulate a resistor on the supply side while providing a fairly regulated DC output voltage. Widely utilized topology for this purpose is a boost converter together with a diode rectifier. In order to increase the power level and to reduce the high-frequency interferences it is common to operate two or more boost converters in parallel with phase shifted switching cycles.

For those interleaved boost PFC rectifiers three different control tasks must be achieved at the same time:

- The inner current control loop needs to achieve nearly unity power factor by forcing the input current to track the shape of the sinusoidal line voltage as close as possible.
- The outer voltage control loop has to maintain a nearly constant DC output voltage.
- The current balancing control must ensure equal rail power for the paralleled converters.

Realization of these complex control tasks for interleaved boost PFC rectifiers was dominated by analog technique for many years. Due to cost-efficient digital signal processors (DSP) and microcontrollers (μC) with increased computational power and appropriate peripherals, digital control is widely used in PFC applications nowadays.

With applying digital control a multitude of benefits such as flexibility and programmability, decreased number of active and passive components, and as a consequence improved reliability, negligible and/or compensable offsets and thermal drifts arise. However, full digital control is not the panacea for all PFC applications. Sometimes it can be beneficial to retain some parts of the PFC control in analog technique, smartly combined with digital control parts.

The purpose of this dissertation is the utilization of digital control for interleaved boost PFC rectifiers. After providing basic information regarding the converter topology, digital control loops and state of the art PFC control, four advanced control concepts utilizing digital control are presented:

- In a semi-digital PFC control concept analog and digital control parts are smartly combined. High bandwidth control parts like the current controller as well as time-critical protection functions retain in conventional analog technique. Whereas the slow voltage compensator, load feed-forward control, multiplier and non-time-critical protection functions are implemented in the digital control part.
- By using DSPs or μCs containing analog on-chip comparators, digital peak current control is basically feasible with little effort. In order to eliminate the drawbacks of peak current control, a digital slope compensation is introduced which does not use an analog ramp signal, but instead an algorithm to pre-calculate the desired

comparator switch-off threshold. Adaptive algorithms are employed to adjust the compensation and to ensure sinusoidal shape of the average inductor current.

- For PFC converters operating in boundary conduction mode (BCM) interleaving of several converters is challenging, because of the variable switching frequency. The introduced digital phase shift control enables multi-rail interleaving. With the flexibility of the digital implementation it is possible to apply phase shedding and limit the switching frequency by maintaining optimal interleaving.
- Multi-rail interleaving of PFC converters operating in BCM and DCM is realized by a feed-forward control. The feed-forward algorithm can be applied alone as open-loop control without the requirement of any current measurement or together with a parallel current controller in a closed-loop version. With adjustable DCM ratio an additional degree of freedom results, which can be used to improve the performance in different ways. The switching losses can be reduced at light load and even within a line half cycle or the switching frequency can be kept within a narrow band. A promising method is introduced which tracks the DCM ratio for every operating point in order to minimize the THD in the input current.

The introduced innovations on digital control provide additional functionality for interleaved PFC rectifiers and improve the performance in different categories. The investigations have shown that digital control is not a general solution for enhanced performance. Often it is beneficial to combine digital control with suitable analog parts such as analog comparators.

Zusammenfassung

Netzgleichrichter mit nicht-sinusförmiger Stromaufnahme verursachen Oberschwingungen im Eingangsstrom, welche die Netzqualität beeinträchtigen und die verfügbare Eingangsleistung reduzieren. Aus diesem Grund besitzen moderne elektronische Stromversorgungen eingangsseitig eine netzfreundliche Pulsgleichrichterstufe (PFC), die einen hohen Leistungsfaktor gewährleisten, so dass sich die Geräte im Idealfall wie ein ohmscher Widerstand am Netz verhalten. Zusätzlich zu der sinusförmigen Stromaufnahme muss die Eingangswechselspannung in eine möglichst konstante Gleichspannung gewandelt werden. Für diesen Zweck wird überwiegend die Topologie des Hochsetzstellers mit vorgeschaltetem Brückengleichrichter eingesetzt. Zur Erhöhung der Geräteleistung und um die schaltfrequenten Störanteile im Eingangsstrom zu reduzieren werden üblicherweise zwei oder mehr Hochsetzsteller parallel betrieben und phasenversetzt angesteuert.

An die Regelung solcher parallel betriebenen, netzfreundlichen Pulsgleichrichterstufen ergeben sich hohe Anforderungen. Gleichzeitig müssen drei verschiedene Regelungsaufgaben bewältigt werden:

- Die innere Stromregelschleife muss einen möglichst idealen Leistungsfaktor gewährleisten, indem der Eingangsstrom der sinusförmigen Netzspannung nachgeführt wird.
- Mit der äußeren Spannungsregelschleife soll am Ausgang eine möglichst konstante Gleichspannung bereit gestellt werden.
- Eine geeignete Stromsymmetrierung wird benötigt, um eine gleichmäßige Leistungsaufteilung auf alle parallel betriebenen Konverter zu erzielen.

Die Umsetzung dieser komplexen Regelung wurde seit vielen Jahren von analoger Schaltungstechnik dominiert. In den letzten Jahren sind digitale Signalprozessoren (DSP) und Mikrocontroller (µC) stetig leistungsstärker und kostengünstiger geworden und besitzen für die Schaltnetzteilregelung speziell ausgelegte Peripherie. Aus diesem Grund kommen heute häufig digitale Regelungen für PFC Anwendungen zum Einsatz. Dies bringt eine Reihe zusätzlicher Vorteile mit sich. Durch die Implementierung adaptiver Regelungen und komplexer Vorsteueralgorithmen erhöht sich die Flexibilität und Leistungsfähigkeit der Geräte. Die Anzahl der aktiven und passiven Bauelemente verringert sich und mögliche Offsets und Temperaturabhängigkeiten können kompensiert werden.

Allerdings ist die Implementierung einer volldigitalen Regelung nicht immer die optimale Lösung für netzfreundliche Pulsgleichrichterstufen. Für einige Anwendungen ist es vorteilhaft, nur einige Teile der Regelung digital zu realisieren und mit analogen Komponenten zu ergänzen.

Die vorliegende Arbeit beschäftigt sich mit digitalen Regelungsstrategien für parallel betriebene, netzfreundliche Pulsgleichrichterstufen. Zunächst werden die grundlegenden Eigenschaften der Konvertertopologie und digitaler Regelschleifen behandelt. Nach der Betrachtung analoger PFC Regelungen und dem Stand der Technik bei digitalen PFC

Regelungen werden vier neuartige Regelungskonzepte vorgestellt, bei denen Teile oder die komplette Regelung auf einem DSP oder µC implementiert sind:

- Bei dem semi-digitalen Regelungskonzept sind die Regelungsaufgaben sinnvoll auf digitale und analoge Teile gesplittet. Dort wo hohe Bandbreite gefordert ist, z.B. Stromregler und zeitkritische Schutzfunktionen kommen die herkömmlichen analogen Schaltkreise zum Einsatz. Die langsame Spannungsregelung, der Multiplizierer zur Generierung des Stromsollwerts, die Eingangsleistungs-vorsteuerung und nicht zeitkritische Schutzfunktionen sind auf einem kostengünstigen µC implementiert.
- Mit DSPs und µC mit auf dem Chip integrierten analogen Komparatoren lässt sich ohne großen Aufwand eine digitale Spitzenstromregelung realisieren. Um die Nachteile der Spitzenstromregelung zu eliminieren, wird eine sogenannte Slope-Kompensation benötigt. Anstelle einer analogen Sägezahn-funktion wurde für die digitale Implementierung ein Algorithmus entwickelt, der direkt die erforderliche Komparatorabschaltschwelle zu Beginn jeder Schaltperiode berechnet. Mit weiteren adaptiven Algorithmen lässt sich zum einen die Slope-Kompensation für jeden Arbeitspunkt anpassen und zum anderen der Mittelwert des Eingangsstroms der sinusförmigen Eingangsspannung nachführen.
- Beim Parallelbetrieb mehrerer Konverter an der Lückgrenze ist das Einstellen der optimalen Phasenverschiebung aufgrund der variablen Schaltfrequenz sehr schwierig. Die Implementierung einer digitalen Phasenwinkelnachführung ermöglicht das Einhalten der optimalen Phasenverschiebung mit hoher Dynamik. Durch gezieltes lastabhängiges zu- oder abschalten einzelner Konverter wird zusätzlich die maximale Schaltfrequenz begrenzt.
- Der synchrone Parallelbetrieb an der Lückgrenze oder im Lückbetrieb lässt sich auch ausschließlich mittels Vorsteuerung erreichen, der keine Strommessung benötigt. Mit optionaler Eingangsstrommessung und einem Stromregler parallel zur Vorsteuerung kann der Konverter auch mit geschlossenem Regelkreis betrieben werden. Der Vorsteueralgorithmus bietet aufgrund der einstellbaren Länge des Lückintervalls einen zusätzlichen Freiheitsgrad, mit dem sich die Betriebsweise der PFC Stufe in verschiedenen Bereichen optimieren lässt. So kann die Schaltfrequenz damit innerhalb vorgegebener Grenzen gehalten werden. Durch Absenkung der Schaltfrequenz in Abhängigkeit der Ausgangsleistung und dem Augenblickswert der Eingangsleistung können die Schaltverluste reduziert werden. In einem weiteren Anwendungsfall wird das variable Lückintervall genutzt, um in jedem Arbeitspunkt die gesamten harmonischen Verzerrungen (THD) zu minimieren.

Mit den entwickelten digitalen Regelungsstrategien ergeben sich zusätzliche Möglichkeiten für die Betriebsführung, mit denen sich die Leistungsfähigkeit von netzfreundlichen Pulsgleichrichterstufen steigern lässt. Die Untersuchungen haben aber auch gezeigt, dass eine digitale Realisierung kein Patentrezept für eine Steigerung der Leistungsfähigkeit ist. Oftmals ergibt sich erst durch die Kombination digitaler Regelung mit analogen Komponenten wie Komparatoren das optimale Regelungskonzept.

Contents

1 Introduction

The largest part of the electrical energy is not consumed in the form that the power grid provides. Before usage the line voltage needs to be changed in amplitude and frequency. In many applications the AC line voltage must be transformed into a DC voltage. Consequently, suitable rectification is required.

Rectifiers with low power factor cause line interferences due to harmonics in the line current and reactive power and therefore reduce the power available from the grid. In order to guarantee high quality of the line voltage, norms like EN61000-3-2 have been released, which indicate limits for line interferences. Thus, power factor correction (PFC) rectifiers have been established as front end stage of AC-DC converters. An ideal PFC rectifier should emulate a resistor on the supply side, while maintaining a fairly regulated DC output voltage [Ros94]. Beyond that high efficiency and power density, low high-frequency distortions and a cost-effective realization are important design objectives.

The widely utilized topology for the PFC stage is the boost converter together with a diode rectifier. This topology is beneficial for this task because the inductor is connected to the input and allows low-distorted input currents. Furthermore, the output voltage is always higher than the amplitude of the line voltage, for which reason a worldwide usage of the same PFC rectifier at different line voltages and line frequencies is possible.

Nevertheless, it is the way of controlling the boost switch which let a simple boost converter with diode rectifier become a PFC rectifier. Generally, a cascaded control structure with outer output voltage control loop and inner current control loop is utilized. As for most converters the voltage control loop must provide a nearly constant DC output voltage. The task of the current control loop is to achieve unity power factor by forcing the average inductor current to track the shape of the sinusoidal input voltage as close as possible.

In order to increase the power level of the rectifier, it is common to operate two or more boost converters in parallel. The paralleled converter rails are typically phase shifted in order to reduce the filter size and costs and high-frequency interferences. With this interleaving technique a further task for the converter control arises. A balance control needs to ensure equal rail power.

The implementation of these complex control tasks for interleaved PFC rectifiers was dominated by analog technique for many years. Accordingly, a multitude of dedicated control ICs was developed, which provides the basic control functions for PFC applications. However, due to cost-efficient digital signal processors (DSP) and microcontrollers (μC) with increased computational power and appropriate peripherals digital control is widely used in PFC applications nowadays.

Digital control offers a multitude of benefits such as flexibility and programmability, decreased number of active and passive components, and as a consequence improved reliability, negligible and/or compensable offsets and thermal drifts [Mak04]. With employing digital control the demand on additional functionality of the PFC control has raised, consequently. In order to fulfill these demands it typically does not suffice to implement the traditional control structure in digital, but rather advanced control concepts needs to be invented. Furthermore, full digital control is not the panacea for all PFC applications. Sometimes it can be beneficial to retain some parts of the PFC control in analog technique combined with digital control parts.

In this thesis different control concepts for interleaved PFC rectifiers utilizing digital control are presented.

Thesis Outline

Chapter 2 of this thesis gives some basic information concerning interleaved boost PFC rectifiers. First the structure of distributed power systems (DPS) for server farms and communication networks is described with special focus on the tasks of the PFC rectifiers in those systems. The topology of the commonly used boost PFC rectifier and the basic structure of the PFC control are illustrated together with some typical shapes of voltages and currents. The interleaving technique for power converters is explained including its beneficial effect on the reduction of the total harmonic distortion (THD) in the input current. Before examining the control, the basics of the boost converter are reviewed and the differences between continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are depicted. After that the three most utilized control methods voltage mode, peak current mode and average current mode control are explained. For PFC rectifiers only current mode control is suited to ensure sinusoidal input current and consequently high power factor. For this reason the control-to-inductor-current transfer functions for CCM and DCM are derived and applied for a design example for the average current control loop of a boost PFC rectifier. In order to complete the PFC control also the design of the outer voltage control loop is explained as well as the multiplier unit, which is utilized to generate the sinusoidal current reference value and to realize a load feed-forward control.

In Chapter 3 the properties of digital control and its associated parts are described in general. The sampling process and the quantization effect of the analog-to-digital conversion (ADC) are explained and their impact to the control performance is presented. Likewise the digital implementation of the pulse width modulation (PWM) is analyzed. Advantageous of digital control is the synchronization of the sampling instance and the switching cycle. On the other hand the sample-and-hold process inserts a dead-time into the control loop, which can reduce the phase margin significantly.

In Chapter 4 state of the art analog and digital PFC control is reviewed. First the traditional analog realization of PFC control is explained. Often the same control structure is retained for full digital PFC control. This is described in addition with some required or valuable

functions such as the correction of the inductor current sample in DCM and a duty-ratio feed-forward control for CCM and DCM.

In Chapter 5 - Chapter 8 advanced control concepts for interleaved boost PFC rectifiers utilizing digital control are presented.

As a first mixed-signal solution a semi-digital PFC control concept with smart combination of analog and digital control parts is described in Chapter 5. High bandwidth control parts like the current controller as well as time-critical protection functions retain in conventional analog technique, whereas the slow voltage compensator, load feed-forward control, multiplier and non-time-critical protection functions are implemented in the digital control part. It is shown that already with such a partial digitalization appropriate power management features can be realized in order to improve the light load efficiency.

For the control concept presented in Chapter 6 digital control is combined with analog comparators in order to realize digital peak current control for interleaved PFC rectifier. With available DSPs and µCs including analog on-chip comparators digital peak current control is basically feasible with little effort. In order to eliminate the drawbacks of peak current control, slope compensation is required. Thus, a digital slope compensation is introduced, which does not use an analog ramp signal, but instead an algorithm to pre-calculate the desired comparator switch-off threshold. This method furthermore enables adaptive slope compensation, which is beneficial for PFC applications where the operating point varies extremely. Several control structures are depicted and compared with respect to performance and computational effort.

A popular control concept for PFC rectifiers is to operate the boost converter at the boundary of DCM and CCM. This boundary conduction mode (BCM) can be easily realized by utilizing a comparator to detect the instance where the inductor current becomes zero, in order to switch on the boost switch. However, due to the resulting variable switching frequency interleaving of several converters is challenging. For this reason a digital phase shift control for interleaved BCM rails is developed in Chapter 7. Because of the analog comparator in the control structure this concept strictly speaking is also a mixed-signal control concept.

In Chapter 8 a pure digital control concept is presented, which enables multi-rail interleaving of PFC converters operating in BCM and DCM by applying a feed-forward control. The feed-forward algorithm is derived for BCM and extended to DCM operation. It can be utilized either alone without any current measurement in an open-loop control or together with a parallel current controller in a closed-loop version. The DCM ratio, e.g. the duration within the switching cycle where the inductor current is zero, can be adjusted individually for every single converter rail. This additional degree of freedom can be utilized for several features. If the inductor values of the rails differ, every rail can get its individual DCM ratio in order to balance the inductor currents. A novel continuous phase shedding method is introduced, which adjusts the DCM ratio of all rails in order to vary the effective number of energized converter rails transition-free. Further investigations show how this continuous phase shedding method can be utilized to reduce the THD in the input

current of paralleled converters in general and especially for PFC rectifiers with its continuous varying operation point.

All the presented innovations were verified in simulation and on a prototype with two or three parallel converter rails. Meaningful practical results are shown to illustrate the effectiveness of the proposed control concepts.

The conclusions are given in Chapter 9.

2 Basics of Boost Power Factor Correction Rectifier

The boost power factor correction (PFC) rectifier is widely used as front-end stage for AC-DC switched-mode power supplies (SMPS). The main task of PFC rectifiers is to generate a fairly regulated DC output voltage from the sinusoidal AC line voltage by providing almost unity power factor [Ros94].

For adequate performance of the PFC rectifier suitable dynamics need to be applied to the control loops by precisely designing the compensators. For this purpose the static and dynamic behavior of the controlled converter needs to be well known.

In this chapter the application of PFC rectifiers in distributed power systems (DPS) is explained. The structure of the cascaded PFC control loops is described and a short review of the boost converter functionality and its modes of operation are given. The basic control methods are described and the control-to-inductor-current transfer function is derived. Finally, the design of the current control loop, the voltage compensator and the PFC specific multiplier unit are explained.

2.1 PFC in Distributed Power Systems (DPS)

Since the largest part of the electrical energy is not consumed in the form that the power grid provides, the line voltage needs to be changed in amplitude and frequency before usage.

In particular the energy demand for server farms and communication networks has increased heavily in the last decades. In order to achieve higher processing speed with minimized power consumption, the supply voltages have been reduced in new logic families [Tab92]. Thus, DC voltages of only a few volts are required to supply the processors and electronic circuits. Transformation of the AC line voltage for this purpose is usually carried out by several conversion stages. This converter structures are also referred to as distributed power systems (DPS) [Tab92, Mam93, Luo05]. The structure of DPS can slightly vary depending on the application and mainframe manufacturer. A widely-used layout of a DPS with 12V bus voltage is depicted in Figure 2.1.

In the first step the AC line voltage is transformed into a DC voltage of 12V by a power supply unit (PSU). Single line phase PSUs typically have a power range up to 4kW. By paralleling of several PSUs the overall power can be scaled and the requirements for redundancy and reliability can be fulfilled. On the output side all paralleled PSUs are connected to a DC bus, which distributes the DC voltage within the system.

In many applications uninterrupted power supply also in the case of temporary power grid failure is required. For this reason battery backups are commonly utilized to supply the DC voltage bus temporarily.

In the second step the DC bus voltage is converted to the required voltage levels, for instance 3.3V, 1.8V, 1.1V. These last DC-DC converter stages are also referred to as voltage regulator modules (VRM) or point of load (POL) converter and are located close to the loads. With this method excellent dynamic and noise immunity of the supply voltages can be achieved.

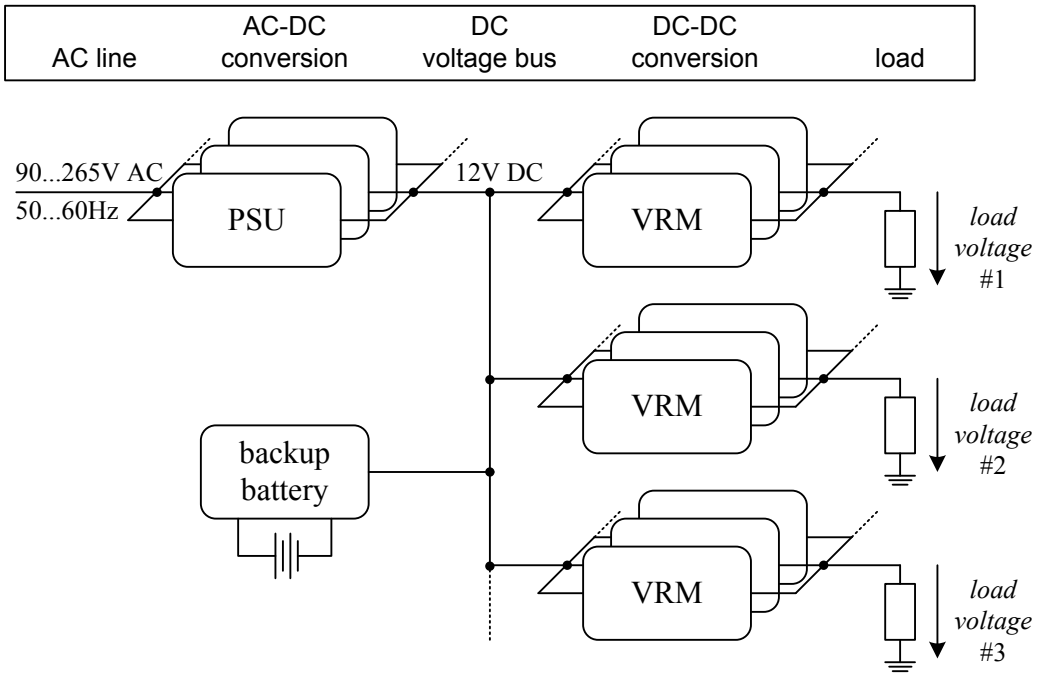

Figure 2.1: Typical structure of a distributed power system (DPS) with 12V *DC bus voltage*

The PSUs are predominantly realized with two converter stages (cf. Figure 2.2) [Wet06]. The front-end stage is the power factor correction (PFC) rectifier, which is examined in detail in this thesis later on. The PFC rectifier transforms the AC line voltage into a DC voltage of typically 400V. In the second stage a DC-DC converter steps down this DC link voltage to the desired PSU output voltage. This converter stage needs suitable dynamic to ensure constant DC bus voltage during load steps and input voltage variations. Besides providing a stable output voltage this stage has a transformer to isolate the system from the power grid. Most utilized topologies for this purpose are the two-switch-forward converter, the phase-shift full-bridge (PSFB) converter and the LLC resonant converter.

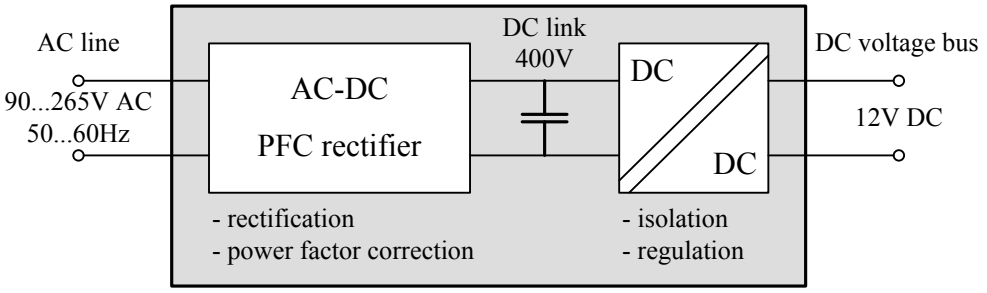

Figure 2.2: Classical PSU topology with two converter stages

2.2 Boost PFC Rectifier

As mentioned in the previous section the PFC rectifier has to convert the AC line voltage into a DC voltage. This task could also be done with a simple passive diode bridge rectifier connected to the line voltage and feeding a bulky filter capacitor. However, this would result in a poor power factor reducing the power available from the power grid, while high harmonic distortions in the line current would cause electromagnetic interferences (EMI) problems [Ros94]. Thus, the second major task of the rectifier stage is to maintain an ideal power factor [Adr02]. This means that the input current of the PSU needs to have the same sinusoidal shape like the line voltage (cf. Figure 2.4), i.e. the PSU must act like a resistor on the supply side.

The definition of the power factor is given in Appendix A.1.

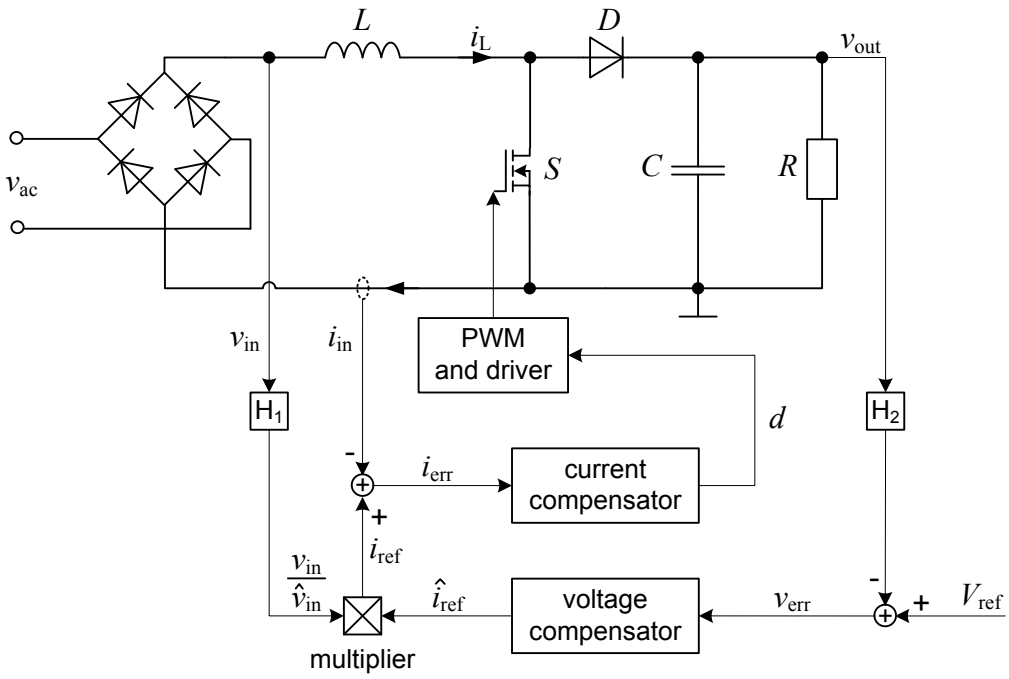

Figure 2.3: Boost PFC rectifier with cascaded control structure

Most suitable for implementing PFC and widely utilized for this purpose is the boost converter together with a diode bridge rectifier (c.f. Figure 2.3). This topology is very simple and due to the fact that the boost inductor is connected in series with the line input, smaller input current ripple is achieved and easy control of the average input current is enabled [Xie03]. An additional EMI filter is typically applied to further reduce the high-frequency ripple in the input current. Figure 2.3 shows the schematic of the boost PFC rectifier with its cascaded control structure without EMI filter. The PFC control usually consists of an outer voltage loop, controlling the DC output voltage, a multiplier unit and an inner current loop.

There are also several topologies where one diode is eliminated from the line-current path, so that the line current simultaneously flows through only two semiconductors [HJJ08]. Consequently, the efficiency of these bridgeless PFC topologies is increased. However, the control usually is the same than for the conventional topology with bridge rectifier.

Strictly speaking it is the way of controlling the boost switch which let the converter act as a PFC. The controller has to operate the boost switch in such a way to properly shape the input current i_{in} according to the shape of the rectified line voltage v_{in} [Ros94]. In order to generate the semi-sinusoidal current reference i_{ref}, the DC reference current value $\hat{\imath}_{ref}$ is multiplied with the normalized input voltage signal. The DC reference current is determined by the outer voltage loop to adjust the DC output voltage v_{out}. Later in this chapter the boost converter and the corresponding control for PFC applications are described in detail.

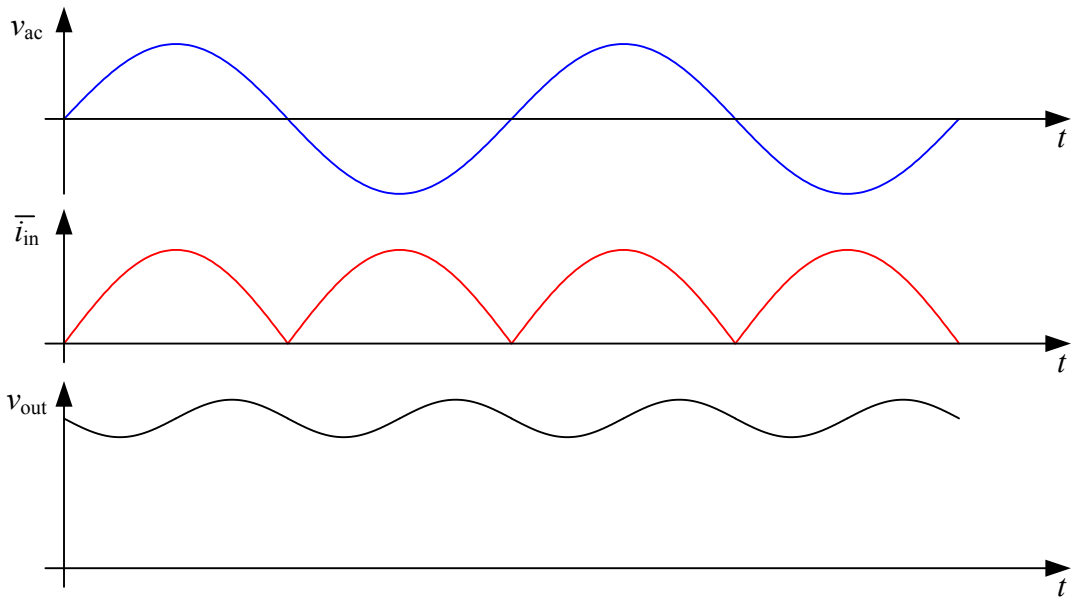

Figure 2.4: Typical voltage and current waveforms of PFC rectifiers

Because of the boost topology the output voltage will be larger than the amplitude of the input voltage $\hat{v}_{in}$. In order to enable a worldwide usage of the PSUs in different power

grids the PFC rectifier normally must provide operation at wide line voltage range of 90V-265V and at line frequencies in the range of 50Hz-60Hz. A typical value for the rectified output voltage is around 400V. However, the output voltage is not a pure DC voltage, but has an AC ripple of twice the line frequency (cf. Figure 2.4). This is caused by the sinusoidal shape of the input voltage and the input current, which cause a pulsating input power. To keep the AC ripple in a certain range a large output capacitor is required. But in many applications a bulky output capacitor is applied anyway, because it is additionally utilized as an energy storage, which ensures continuing operation of the system during short term power line failures of up to one line period.

2.3 Interleaving

The interleaving technique is characterized by operating two or more identical converters in parallel (c.f. Figure 2.5) with phase shifted gate signals and is topic of numerous publications, e.g. [Lou06, Bal93, Miw92]. With this method the overall switching frequency of the paralleled converters is increased, while the switching frequency of every single converter cell remains at its origin value. Hence, the power level can be easily extended without increasing the device stress. Due to the overlapping inductor currents the ripple of the input current and the output voltage are reduced significantly (c.f. Figure 2.6). At certain duty-ratios the ripple Δi_{in} is even eliminated completely (e.g. at $D = 50\%$ for two interleaved converters). In Figure 2.7 the reduction of the ripple in the input current is illustrated versus duty-ratio for two interleaved converters. With reducing the input current ripple also the RMS current in the DC link capacitor and the EMI of boost PFC rectifiers are reduced significantly. This enables easier observance of the standards for line current harmonics and conducted EMI with less filter volume and filter components [Zum04].

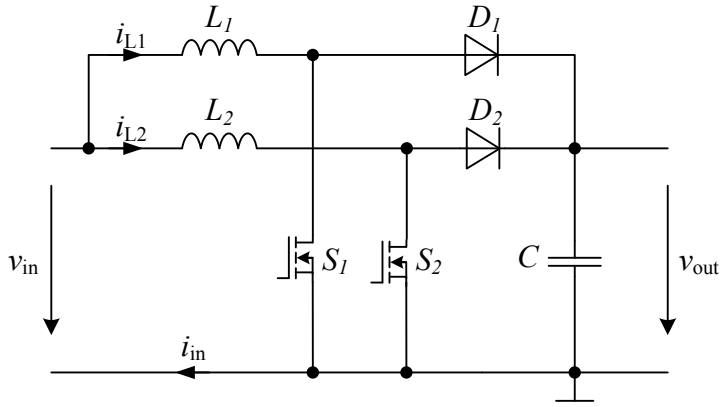

Figure 2.5: Dual interleaved boost converter

Furthermore, interleaving offers potential to improve the light load efficiency by adjusting the number of paralleled converters at partial load [Gro09, ChMa10, QLi09]. Due to employment of several small inductances instead of a single bulky inductor faster dynamic

response can be achieved. In addition a better thermal management results by spreading of the hot spots.

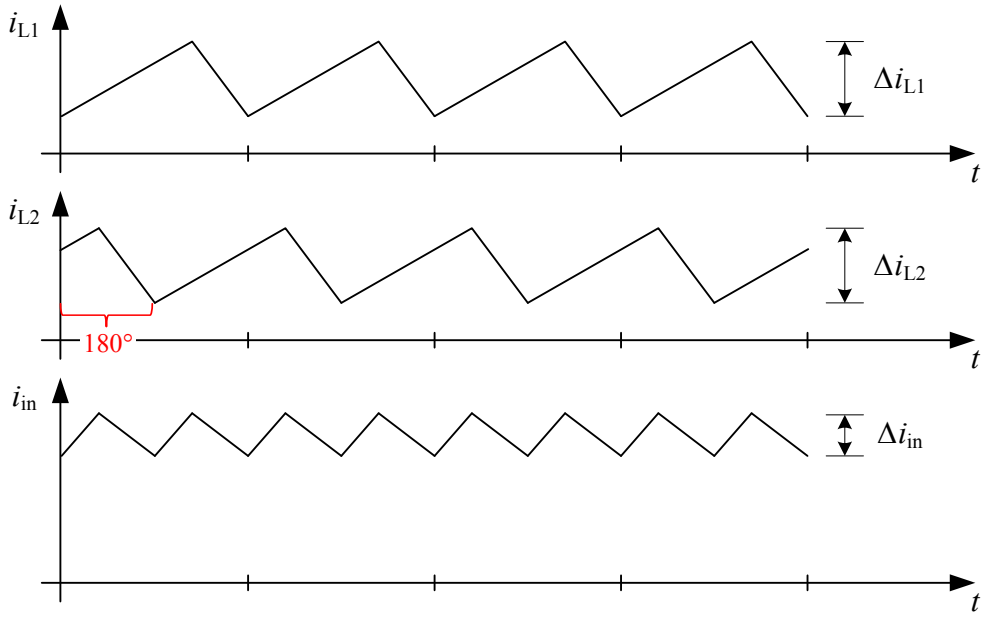

Figure 2.6: Interleaved inductor currents and resulting input current

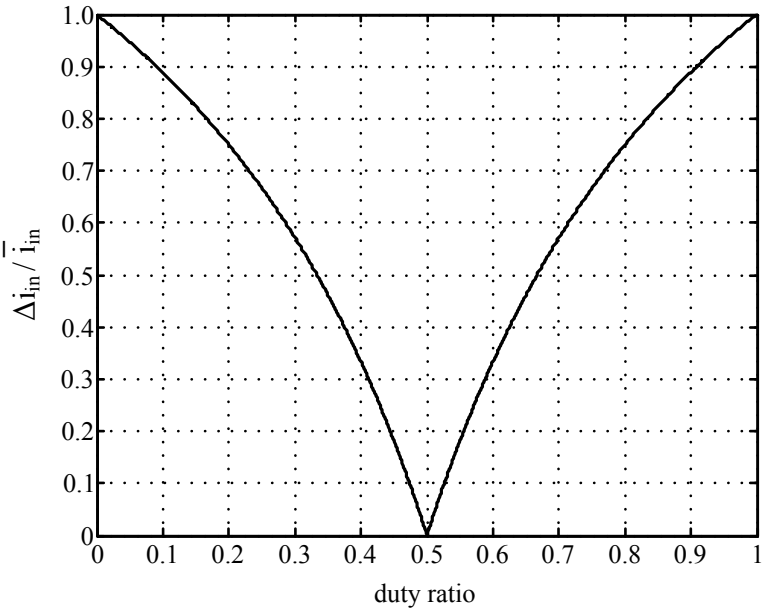

Figure 2.7: Ripple reduction in the input current for dual interleaved converter

One drawback of interleaving is the need of balancing the currents of the paralleled converters to ensure uniformed spread stress of the devices. Thus, an adequate current balancing strategy is one of the design goals for interleaved converter control.

2.4 Boost Converter Basics

The boost converter (cf. Figure 2.8) provides a higher output voltage than the input voltage [Eri00, Kas91, Zac90a]. For this purpose one active switch (MOSFET), one passive switch (diode) and two passive energy storage elements (inductor and capacitor) are utilized.

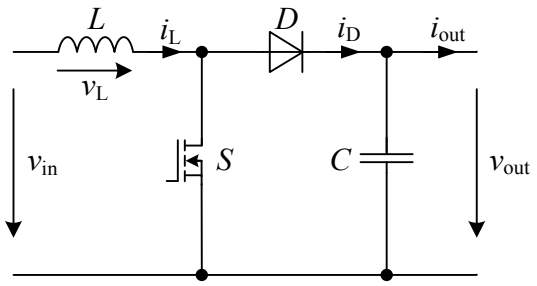

Figure 2.8: Boost converter

The gate of the MOSFET acts as control input port. If the switch is closed, the inductor voltage is equal to v_{in} and the current through the inductor changes with

$$\frac{di_L}{dt} = \frac{v_{in}}{L}. \tag{2.1}$$

During this interval the energy stored in the inductor increases. When the switch is open, the inductor voltage is $(v_{in} - v_{out})$ and the current flows through the diode and releases the inductive energy to the converter output and decreases with

$$\frac{di_L}{dt} = \frac{v_{in} - v_{out}}{L}. \tag{2.2}$$

In Figure 2.9 the equivalent circuits of the different switching conditions are illustrated.

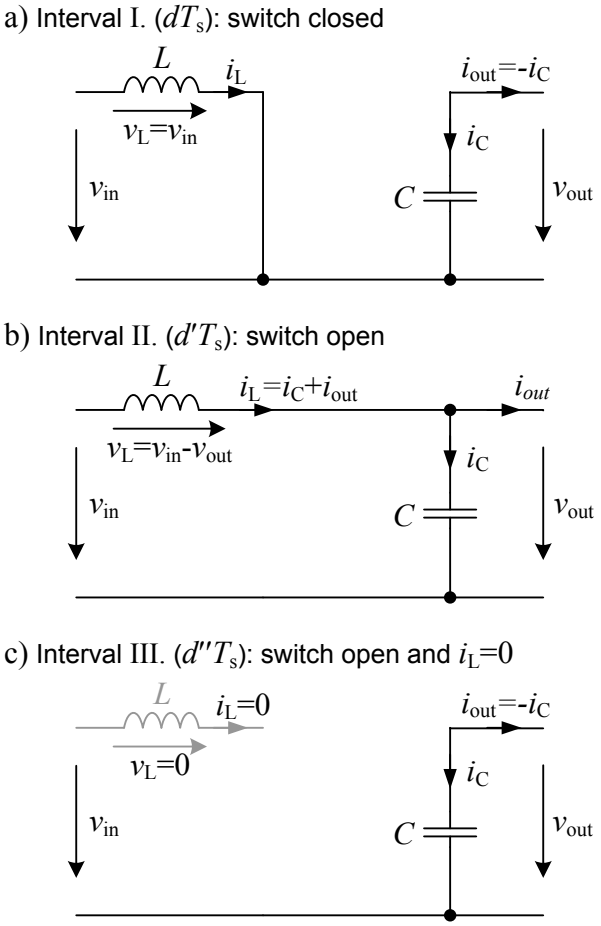

Figure 2.9: Equivalent circuits of the switching intervals during one switching cycle

Figure 2.10 shows the waveform of the inductor voltage and current, as well as the waveform of the current which flows through the boost diode under steady state conditions. This means that the inductor current values at the beginning and at the end of the switching period T_s are equal. From this it follows, that the conversion ratio M is determined by interval:

$$M = \frac{v_{out}}{v_{in}} = \frac{T_s}{T_s - T_{on}} = \frac{1}{1-d} = \frac{1}{d'} \tag{2.3}$$

The range of the duty-ratio $d = T_{on}/T_s$ goes from zero to one.

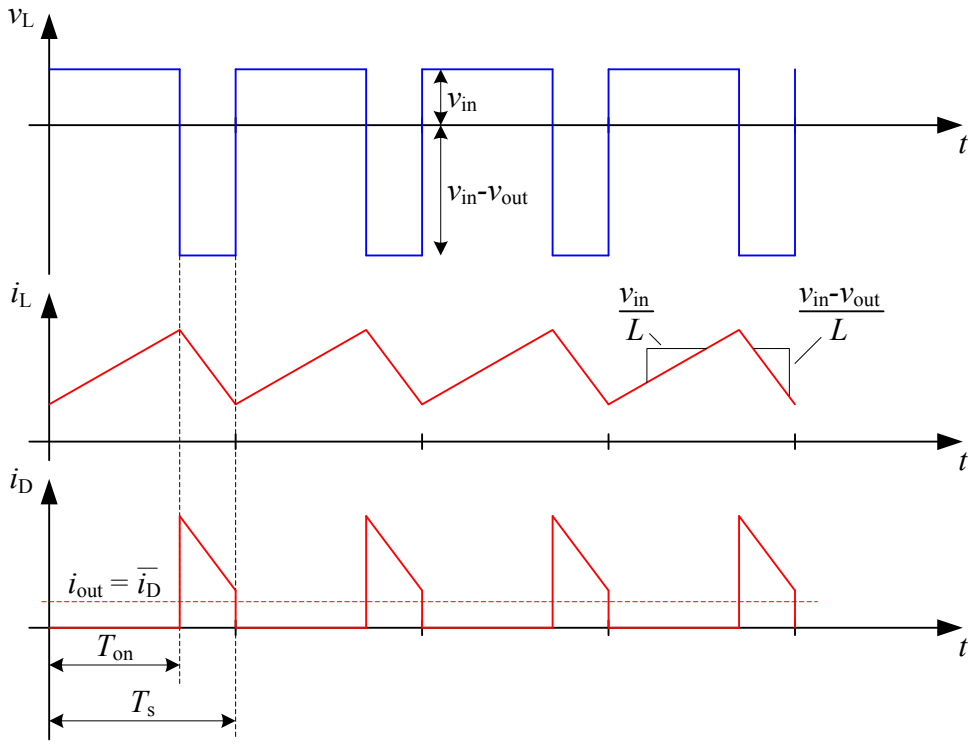

Figure 2.10: Steady state voltage and current waveforms of an ideal boost converter

2.4.1 Operation Modes

The operation modes of switching converters can be classified into two modes: firstly the continuous conduction mode (CCM), where the inductor current never comes down to zero and secondly the discontinuous conduction mode, where the inductor current resets to zero within the switching cycle.

A. Continuous Conduction Mode (CCM)

In CCM the switching cycle portions in two intervals. First, if the switch is closed, the inductor current rises and secondly, the current falls, if the switch is open (cf. Figure 2.11 a)). In this mode the AC component of the inductor current typically is much smaller than the DC component.

B. Discontinuous Conduction Mode (DCM)

In DCM a third interval within the switching cycle appears (cf. Figure 2.9 c)). During the switch-off time the inductor current decays to zero and the converter remains in this state until the next switch-on event. This happens for example at light load operation of the converter, if the peak-to-peak inductor current ripple becomes larger than twice the average current. In some applications the converter is intentionally designed to operate only in DCM in order to avoid problems caused by the reverse recovery effect of the diode [Gro11]. Another reason to employ DCM can be avoiding the right half plane zero in the

control-to-output transfer function of the boost converter [Ara09]. Figure 2.11 b) shows the inductor current waveform in DCM.

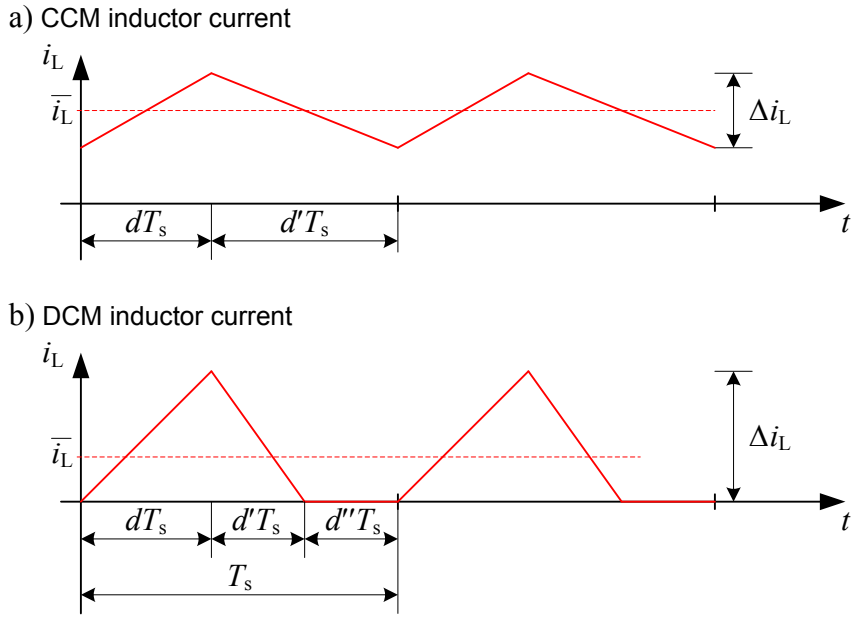

Figure 2.11: Inductor current waveform in
a) CCM and
b) DCM

The converter properties in DCM are significantly different to CCM. Consequently, a rigorous change in the small and large signal transfer characteristic occurs with changing the mode of operation. In DCM the conversion ratio M becomes dependent of the load resistance R [Eri00]:

$$M_{DCM}(d,R) = \frac{v_{out}}{v_{in}} = \frac{1}{2}\sqrt{\frac{1}{2} + \frac{d^2 R T_s}{L}} \tag{2.4}$$

2.4.2 Control Methods

2.4.2.1 Voltage mode control

Beyond the converter control methods voltage mode control is the oldest and simplest one. The control structure is illustrated in Figure 2.12 and significant signal waveforms are depicted in Figure 2.13. The output voltage is compared with the reference value and the resulting error voltage is passed to the voltage compensator. The compensator determines the comparator turn-off threshold. Together with the RS-flip-flop the comparator acts as a pulse width modulator (PWM), where the sawtooth signal on the negative comparator input is utilized as carrier signal. The RS-flip-flop turns on the boost switch at the

beginning of each switching cycle and turns off, if the sawtooth signal exceeds the error amplifier output value. Due to the fact that the duty-ratio is directly determined by the voltage error this method is also known as direct duty-cycle control (DDC) [Zac90].

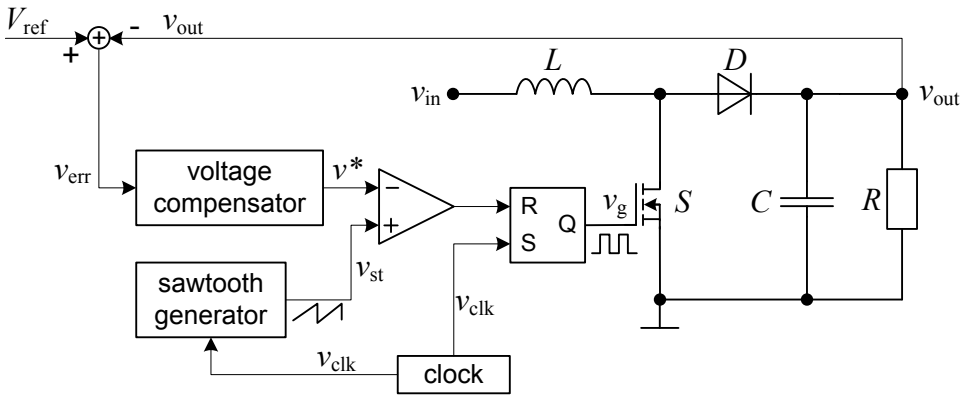

Figure 2.12: Boost converter with voltage mode control

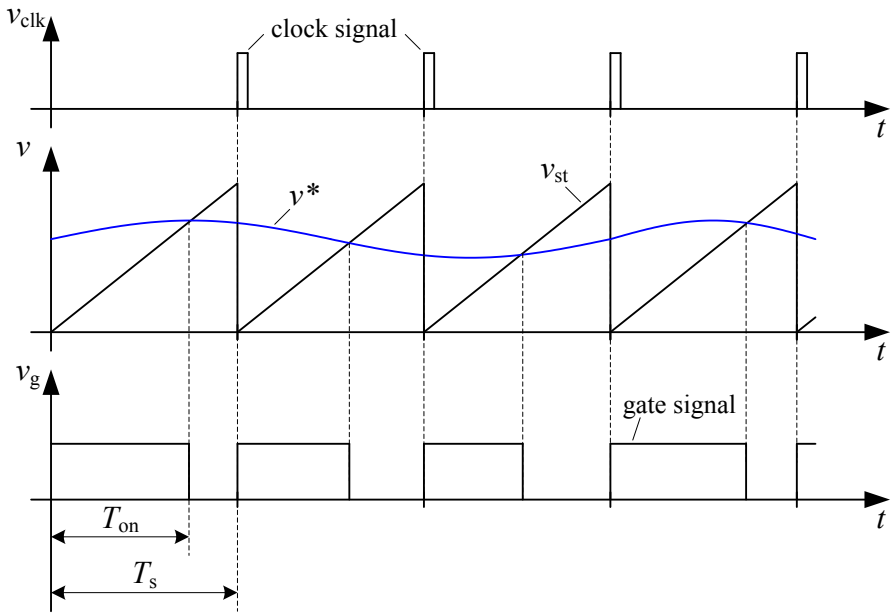

Figure 2.13: Generation of the gate signal with voltage mode control

With adequate amplitude of the sawtooth signal this control method provides a good signal-to-noise ratio. Another advantage is the simple design of the feedback loop [Zac90]. However, since the loop gain changes with the input voltage a poor control dynamic under input voltage variation results. To overcome this drawback an extension of the control method can be applied. Thereby the amplitude of the sawtooth signal is changed proportional to the input voltage. This method is also known as voltage feed-forward control (VFC) [Zac90].

For PFC applications voltage mode control is not suitable, because it is essential to control the shape of the input current which is not provided with this control method.

2.4.2.2 Current mode control

With current mode control the inductor current which also influences the output voltage is implicated as an additional control value. Compared to voltage mode control it exhibits a high frequency bandwidth resulting in improved control loop dynamics and leads to a better line noise rejection. With reducing the small-signal dynamics from second-order to first-order, it additionally simplifies the outer voltage loop design [Hsu79, Don96]. A cascaded control structure results where the inner current control loop operates the boost switch. The reference value for the current controller is provided by the outer voltage controller.

There is a multitude of methods of implementing the current control, which can be separated in fixed and variable switching frequency methods. Widely utilized is the peak current mode control. Thereby the switch is turned on with an external clock signal and turned off if the current reaches a certain level. Very similar but rarely used is valley current mode control, where the clock signal turns off and a comparator turns on the switch, if the current falls below the threshold level. A further fixed frequency method is average current control. As the name implies with this method the average value of the inductor current is controlled. Depending on the current error a compensator determines the duty-ratio which is passed to a PWM to generate the switching command. In particular, in boost-type PFC rectifiers, average current control ensures very low current distortions [Che03].

Examples for variable switching frequency methods are constant on-time control, constant off-time control and hysteretic control [Zac90]. At hysteretic control two comparators are utilized to determine the switching instances. The switch is turned on if the lower threshold is reached and turned off at the specified peak value. A special case for hysteretic current control is the boundary conduction mode (BCM) (often also called critical conduction mode or transition mode). With this method the lower current threshold is set to zero in order to operate the converter at the boundary of continuous and discontinuous conduction mode.

In the following peak and average current control are described in detail.

A. Peak current mode control with slope compensation

The scheme of a boost converter with outer voltage loop and inner peak current control loop is illustrated in Figure 2.14. Again the clock signal turns on the switch at the beginning of each switching cycle. The duty-ratio now is terminated when the inductor current reaches a threshold level defined by the outer voltage controller (cf. Figure 2.15).

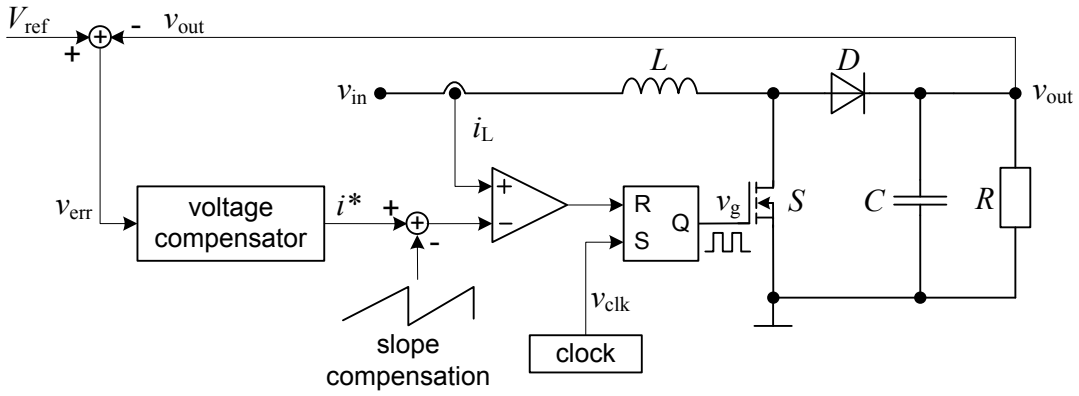

Figure 2.14: Peak current controlled boost converter with slope compensation

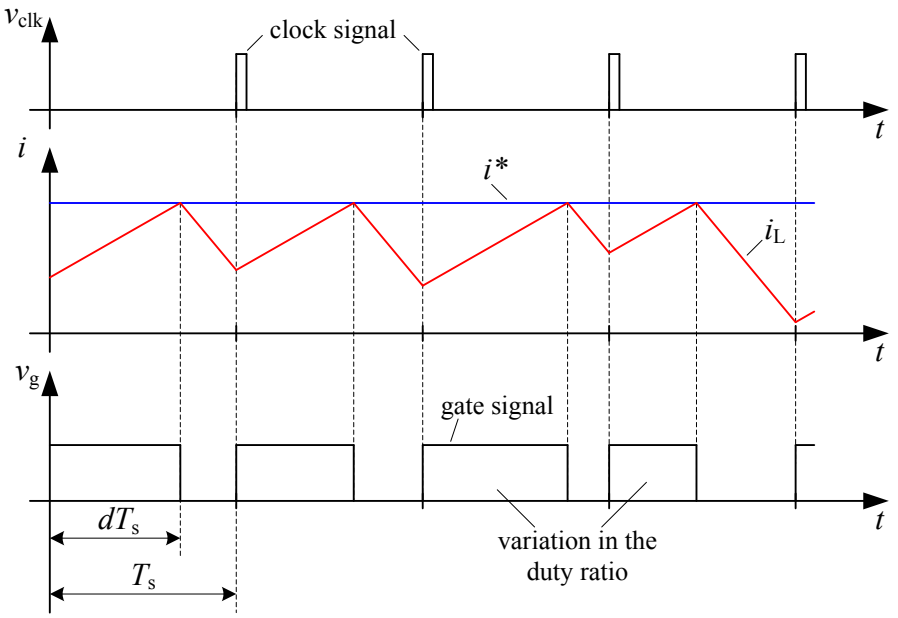

Figure 2.15: Generation of the gate signal with peak current mode control without slope compensation

Additionally to the excellent control dynamics this technique features some inherent advantages such as simple cycle-by-cycle current limiting and good current sharing of paralleled converters [Hsu79, Don96]. Instead of measuring the inductor current it suffice to sense the current in the switch path for peak current control. Thus, instead of a shunt resistor, which is always a trade-off between good signal-to-noise ratio and additional losses, a simple current transformer can be utilized. However, there are several drawbacks of peak current mode control in CCM [Hol84, JLu07]. Sensing of the peak instead of the average current value causes non ideal control response. Spikes in the current signal due to noise or the reverse recovery current of the boost diode can lead to faulty switch-off, particularly at small inductor current ripple. However, the major drawback is the loss of

stability, if the duty-ratio exceeds 50%, resulting in subharmonic oscillations. This situation is depicted in Figure 2.15, where the peak current reference value i^* is constant but the disturbance in the inductor current increases resulting in high variation in the duty-ratio. A common approach to regain stability at duty-ratios above 50% is to apply a so called slope compensation [GrSc09, Hsu79, Don96, Hol84, JLu07, Sam08, YLi2007, Sak05]. Therefore an additional sawtooth signal with appropriate slope is either added to the current signal or subtracted from the reference value (cf. Figure 2.14). The behavior without and with slope compensation is analyzed in the following.

A.1 Situation without Slope Compensation

In order to derive the stability criterion of peak current mode controlled CCM converters which characterizes the transition to subharmonic oscillations, the operation without slope compensation shall be analyzed in a first step [GrSc09]. Therefore inductor currents are plotted in Figure 2.16 versus a single switching period T_s for the undisturbed (solid stroke) and a disturbed (dashed stroke) case. Both inductor current shapes have the same rising slope m_1, falling slope m_2 and peak value $\hat{\imath}_L$. For the undisturbed case (solid line in Figure 2.16) it can be directly derived

$$\hat{\imath}_L = m_1 T_1 + I_0 \tag{2.5}$$

as well as

$$\hat{\imath}_L - m_2 T_2 = I_0 \,. \tag{2.6}$$

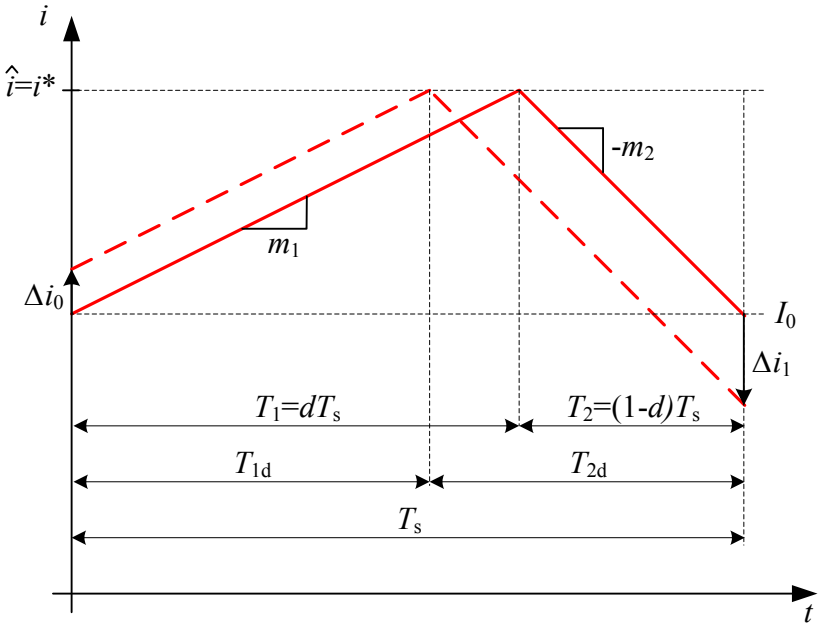

Figure 2.16: Growing disturbances in the inductor current under peak current control for $m_1 > m_2$

Whereas for a disturbance of Δi_0 (dashed line in Figure 2.16)

$$\hat{\imath}_L = \Delta i_0 + m_1 T_{1d} + I_0 \tag{2.7}$$

and

$$\hat{\imath}_L - m_2 T_{2d} = I_0 + \Delta i_1 \tag{2.8}$$

applies.

In both cases the duration of the switching period is identical. This is because of clock-triggered turn-on. Thus, it follows

$$T_s = T_1 + T_2 = T_{1d} + T_{2d}. \tag{2.9}$$

After solving Eq. (2.5) for T_1, Eq. (2.6) for T_2, Eq. (2.7) for T_{1d} and Eq. (2.8) for T_{2d} , Eq. (2.9) can be rewritten as

$$\frac{\hat{\imath}_L - I_0}{m_1} + \frac{\hat{\imath}_L - I_0}{m_2} = \frac{\hat{\imath}_L - \Delta i_0 - I_0}{m_1} + \frac{\hat{\imath}_L - \Delta i_1 - I_0}{m_2} \tag{2.10}$$

and directly simplified to

$$0 = -\frac{\Delta i_0}{m_1} - \frac{\Delta i_1}{m_2}, \tag{2.11}$$

which is equivalent to

$$\Delta i_1 = -\frac{m_2}{m_1} \Delta i_0. \tag{2.12}$$

If the magnitude of the current falling slope m_2 is larger than that of the rising slope $m_1 < m_2$, the current perturbation Δi obviously grows. The current error drift propagates with every switching period and after n cycles the perturbation will become

$$\Delta i_n = \left(-\frac{m_2}{m_1}\right)^n \Delta i_0. \tag{2.13}$$

For steady state conditions the ratio of current falling slope to rising slope can be expressed as

$$\frac{m_2}{m_1} = \frac{d}{1-d}, \tag{2.14}$$

where d is the duty-ratio (cf. also Figure 2.17).

From Eq. (2.13) and Eq. (2.14) it follows that the instability inherently occurs as long as the duty-ratio exceeds 50% ($d > 0.5$).

A.2 Situation with Slope Compensation

The instability for $d > 0.5$ can be eliminated, if a compensation ramp is added to the switch-off threshold as shown in Figure 2.17 [GrSc09, Hsu79, Don96, Hol84]. When introducing the additional compensation slope m_{sc} the calculation similar to Eq. (2.5) - Eq. (2.13) directly yields as a modified formula for the current perturbation after n cycles

$$\Delta i_n = \left(-\frac{m_2 - m_{sc}}{m_1 + m_{sc}}\right)^n \Delta i_0. \tag{2.15}$$

From Eq. (2.15) it follows that for a stable current loop $\left|\frac{m_2 - m_{sc}}{m_1 + m_{sc}}\right| < 1$ must be fulfilled and therefore the required slope for the compensation ramp results as

$$m_{sc} > \frac{1}{2}(m_2 - m_1). \tag{2.16}$$

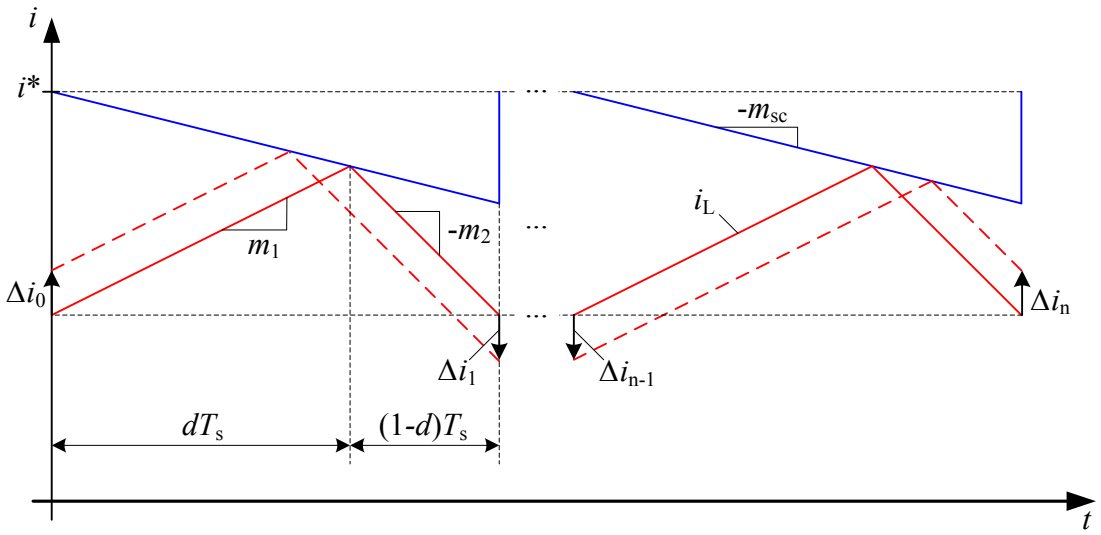

Figure 2.17: Inductor current under peak current control with slope compensation

Assuming a constant inductance L, the slope is proportional to the inductor voltage. Table 2.1 contains the corresponding voltages $m_1 L$, $m_2 L$ and the required compensation $m_{sc} L$ for buck, boost and buck-boost converter.

From Eq. (2.15) it can be seen that a perturbation can be compensated within only one cycle, if the slope of the compensation ramp m_{sc} is equal to the falling current slope m_2. This characteristic is called *dead-beat* control and represents the fastest possible transient response [GrSc09, Hsu79, Don96, Hol84]. If applying higher values of m_{sc} than m_2, the settling takes several cycles without overshoot.

	$m_1 L$	$m_2 L$	$m_{sc} L$
buck	$v_{in} - v_{out}$	v_{out}	$> v_{out} - 0.5 v_{in}$
boost	v_{in}	$v_{out} - v_{in}$	$> 0.5 v_{out} - v_{in}$
buck-boost	v_{in}	v_{out}	$> 0.5(v_{out} - v_{in})$

Table 2.1: Current slope generating voltages and minimum required compensation for basic converters

B. Average current mode control

Most converters only need to adjust the output voltage accurately. For that purpose the outer voltage control loop requests higher current from the inner current control loop to increase or less current to decrease the output voltage. In fact it is the average value of the output current which needs to be varied, but the exact quantity of the average current is not essential. With peak current control with slope compensation there is no direct link to the average current value. But due to the fact that the output current can be varied very easily, it is well suited for those applications.

However, especially in PFC applications the situation is different. Besides controlling the output voltage also the average value of the input current must follow the reference value as good as possible to achieve unity power factor. Consequently, it is the inductor average current which needs to be controlled in boost PFC rectifiers.

Figure 2.18 shows the scheme of the boost converter with average current control. The voltage loop is similar to peak current control, but it now determines the average inductor current for the inner control loop. Based on the difference between that reference value and the actual current average value the current compensator defines the duty-ratio. Similar to voltage mode control a comparator and a RS-flip-flop form a PWM unit to generate the switching pulses. If the sawtooth signal exceeds the duty-ratio signal, the flip-flop turns off the switch and a clock signal turns on the switch at the beginning of each switching cycle. By applying an external sawtooth as carrier signal with arbitrary amplitude instead of the current slope, average current control is less noise sensitive [Zac90]. There is no need of any slope compensation and spikes in the current signal are filtered and cannot lead to faulty switch-off events.

However, to achieve the desired control dynamic and stability an accurate design of the compensation network is required. The resulting bandwidth of average current control is lower compared to peak current control, but it is quite enough for PFC applications.

Interleaving with good current sharing is possible, if every rail gets its own current control loop. But challenging is the cost effective sensing of the rail inductor currents. For single rail a shunt resistor in the ground connection path is mostly utilized, but for interleaved rails this method can only be used to sense the overall input current. By placing the shunt

resistor in the inductor path it has no direct connection to the signal ground and therefore needs resistive voltage divider at the input of a differential amplifier. The use of compensated Hall Effect current transducers in the inductor path is easy to implement, but too expensive for cost sensitive applications. By measuring in the switch path the inductor current information is not available during the switch-off interval. In some analog controller ICs a current synthesizer is applied to reconstruct the complete inductor current signal from the switch current [TI11].

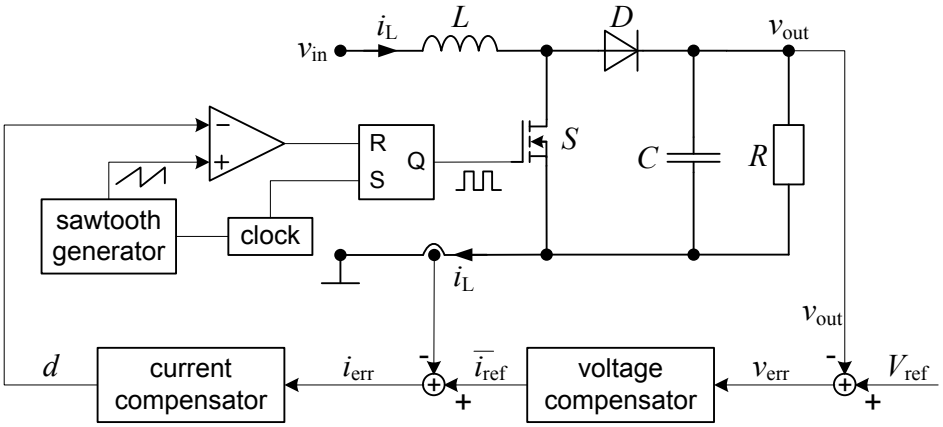

Figure 2.18: Average current control for boost converter

2.4.3 Modeling of the Boost Converter

For the analysis and design process of power electronic circuits it is essential to have adequate converter models available. They are helpful early in the design process to choose the suitable topology, select appropriate circuit components and run simplified simulations in order to estimate the converter performance. Furthermore, converter models are indispensable for control loop design to ensure stability and meet the dynamic requirements.

There are several modeling methods which are addressed in a multitude of publications, for example [Rid90, Zac90, Eri00, Mak01, Kas91]. Elementary circuit modeling of power converters usually yields detailed continuous-time nonlinear time-varying models in state-space form [Mak01]. Those models focus only on the components which are essential to the power conversion and control processing. Dynamics occurring at frequencies higher than the switching frequency are neglected, e.g. dynamics due to snubber networks.

Additionally to the multitude of modeling methods there are several different transfer functions, which can be derived representing the dynamic behavior of a state variable (inductor current or capacitor voltage) under variation of an input variable (duty-ratio, input voltage, load, etc.).

In this work the state space modeling method is utilized to derive the small signal control-to-inductor-current transfer function

$$G_{id}(s) = \frac{\bar{i}_{L\Delta}}{d_{\Delta}} \tag{2.17}$$

in order to design the current controller later on. Thereby the inductor current represents the control variable and the duty-ratio the actuating variable. The small signal values are indicated by 'Δ'.

Transfer functions can only be determined for linear systems. For this reason linearization around a certain operating point is required in order to analyze the small signal dynamic behavior of the non-linear system. With state space modeling only the average values of the variables within each switching cycle are considered.

In CCM the two different positions of the boost switch result in two different linear systems depicted in Figure 2.9 a) and b). Considered are the state variables inductor current i_L and capacitor voltage v_C.

Interval I. (dT_s): switch closed

$$\frac{di_L}{dt} = \frac{1}{L} v_{in} \tag{2.18}$$

$$\frac{dv_C}{dt} = -\frac{1}{C}\frac{v_C}{R} \tag{2.19}$$

Interval II. ($d'T_s$): switch open

$$\frac{di_L}{dt} = \frac{1}{L}(v_{in} - v_C) \tag{2.20}$$

$$\frac{dv_C}{dt} = \frac{1}{C}\left(i_L - \frac{v_C}{R}\right) \tag{2.21}$$

By averaging both intervals over one switching cycle the dynamic average values for the state-variables result (cf. Figure 2.19) [Böc09]. For the inductor current the dynamic average value is

$$\begin{aligned} \frac{d\bar{i}_L}{dt} &= \frac{1}{T_s}\frac{1}{L}\left[\int_0^{dT_s} v_{in}\,dt + \int_{dT_s}^{T_s} (v_{in} - \bar{v}_C)\,dt\right] \\ &= \frac{1}{L}(v_{in} - d'\bar{v}_C). \end{aligned} \tag{2.22}$$

With similar calculation the equation for the dynamic average value of the capacitor voltage results as

$$\frac{d\bar{v}_C}{dt} = \frac{1}{C}\left(d'\bar{i}_L - \frac{\bar{v}_C}{R}\right). \tag{2.23}$$

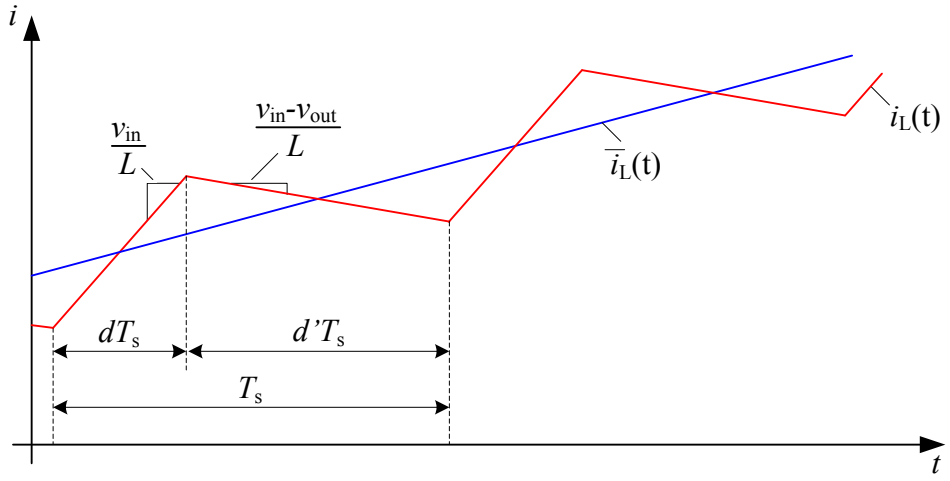

Figure 2.19: Dynamic average value of the inductor current

The required small signal dynamic model is determined by applying a small perturbation around a steady-state operating point. The operating point for this linearizing process is given by

$$\begin{aligned} \overline{i}_L &= \overline{i}_{L0} + \overline{i}_{L\Delta} \\ \overline{v}_C &= \overline{v}_{C0} + \overline{v}_{C\Delta} \\ d' &= d'_0 + d'_\Delta \\ v_{in} &= v_{in0} + v_{in\Delta} \end{aligned} \quad . \tag{2.24}$$

The '0' indicates the steady state value of the observed operating point.
Inserting Eq. (2.24) into Eq. (2.22) and Eq. (2.23), it follows

$$\frac{d\overline{i}_{L\Delta}}{dt} = \frac{1}{L}(-d'_0\overline{v}_{C0} - d'_0\overline{v}_{C\Delta} - d'_\Delta\overline{v}_{C0} + v_{in0} + v_{in\Delta}) \tag{2.25}$$

and

$$\frac{d\overline{v}_{C\Delta}}{dt} = \frac{1}{C}\left(d'_0\overline{i}_{L0} + d'_0\overline{i}_{L\Delta} + d'_\Delta\overline{i}_{L0} - \frac{\overline{v}_{C0}}{R} - \frac{\overline{v}_{C\Delta}}{R}\right). \tag{2.26}$$

Since $d'_0\overline{v}_{C0} = v_{in0}$ and $d'_0\overline{i}_{L0} = \overline{v}_{C0}/R$, these terms eliminates each other.
Both equations are transferred into Laplace domain in order to derive the required transfer function:

$$s\overline{i}_{L\Delta} = \frac{1}{L}(-d'_0\overline{v}_{C\Delta} - d'_\Delta\overline{v}_{C0} + v_{in\Delta}) \tag{2.27}$$

$$s\overline{v}_{C\Delta} = \frac{1}{C}\left(d'_0\overline{i}_{L\Delta} + d'_\Delta\overline{i}_{L0} - \frac{\overline{v}_{C\Delta}}{R}\right) \tag{2.28}$$

With inserting Eq. (2.28) in Eq. (2.27) and solving for $\bar{i}_{L\Delta}$, it follows

$$\bar{i}_{L\Delta} = -d'_{\Delta}\frac{\overline{v}_{C0}(sRC+2)}{s^2LRC+sL+{d'_0}^2R} + v_{in\Delta}\frac{(sRC+1)}{s^2LRC+sL+{d'_0}^2R}. \tag{2.29}$$

This equation indicates that the average inductor current is not only influenced by the control variable d'_{Δ}, but also due to variations in the input voltage $v_{in\Delta}$. The small signal model can be separated in the control-to-inductor-current and the line-voltage-to-inductor-current transfer function (cf. Figure 2.20). The control-to-inductor-current transfer function results from the first term on the right side of Eq. (2.29). However, typically d' is not the applied control variable but d. Therefore the substitution $d'_{\Delta} = -d_{\Delta}$ is performed for the small signal model. Thus, the control-to-inductor-current transfer function for the boost converter in CCM results as

$$G_{id}(s) = \frac{\bar{i}_{L\Delta}}{d_{\Delta}} = \frac{\overline{v}_{C0}(sRC+2)}{s^2LRC+sL+{d'_0}^2R}. \tag{2.30}$$

In the high-frequency region the following approximation can be done to simplify the transfer function [Zac90]:

$$G_{id}(s) = \frac{\bar{i}_{L\Delta}}{d_{\Delta}} \approx \frac{\overline{v}_{C0}}{sL} \tag{2.31}$$

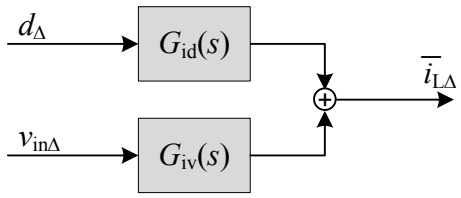

Figure 2.20: Block diagram of the small signal average inductor current model

From the second term of Eq. (2.29) the line-voltage-to-inductor-current transfer function results as

$$G_{iv}(s) = \frac{\bar{i}_{L\Delta}}{v_{in\Delta}} = \frac{(sRC+1)}{s^2LRC+sL+{d'_0}^2R}. \tag{2.32}$$

This equation describes the influences on the inductor current due to line voltage variation. The line voltage acts as a disturbance variable on the control loop and especially in PFC applications the variation in the line voltage is significant. Because the variation in the line voltage occurs periodically with line frequency the disturbances is predictable and can be partly compensated by a disturbance variable feed-forward control. Such an approach is proposed in [Keu13]. But since the switching frequency is typically in the range of several

10kHz, the change of the input voltage during a few switching cycles is small and therefore can be neglected for the design of the current compensator.

The control-to-inductor-current transfer function of Eq. (2.30) is only valid, if the boost converter operates in CCM. Consequently, a separate model for DCM operation needs to be generated. In DCM there is the third interval within each switching cycle where the switch is open and the inductor current is zero (cf. Figure 2.9 c)).

Interval III. ($d''T_s$): switch open and $i_L = 0$

$$\frac{di_L}{dt} = 0 \tag{2.33}$$

$$\frac{dv_C}{dt} = -\frac{1}{C}\frac{v_C}{R} \tag{2.34}$$

In order to change the average inductor current in CCM, the current value at the end of the switching cycle must be different to the value at the beginning of the switching cycle. In DCM the inductor current does not behave as a true state space variable anymore, since it has no free boundaries but is fixed to zero at the beginning and the end of each switching cycle. Consequently, the inductor current of each cycle is independent and does not carry any information to the following cycle [Ara09]. For the dynamic behavior of the converter average model this means that with changing from CCM to DCM the order of the system is reduced by one (from one to zero) [Böc09]. Instead of a differential equation the inductor average current in DCM is represented by the algebraic equation

$$\overline{i}_L = \frac{d^2 T_s}{2L}\frac{\overline{v}_C v_{in}}{\overline{v}_C - v_{in}}. \tag{2.35}$$

However, within each switching cycle, the inductor current is still a dynamic variable and does contribute to the fast dynamics of the converter [Ara09]. Figure 2.21 illustrates that the average inductor current can be influenced as usual by changing the duty-ratio. The change of the average current from cycle to cycle is given by

$$\overline{i}_{L\Delta} = \overline{i}_L(k+1) - \overline{i}_L(k). \tag{2.36}$$

For the small signal dynamic model the steady-state operating point for the linearizing process is defined by

$$\begin{aligned} \overline{i}_L &= \overline{i}_{L0} + \overline{i}_{L\Delta} \\ d &= d_0 + d_\Delta \end{aligned}. \tag{2.37}$$

Applying this operation point on Eq. (2.35) and inserting in Eq. (2.36) it follows

$$\bar{i}_{L\Delta} = \frac{(d_0 + d_\Delta)^2 T_s}{2L} \frac{\overline{v}_C v_{in}}{\overline{v}_C - v_{in}} - \frac{d_0^2 T_s}{2L} \frac{\overline{v}_C v_{in}}{\overline{v}_C - v_{in}}. \tag{2.38}$$

With rearranging this equation one gets

$$\bar{i}_{L\Delta} = \frac{T_s}{2L} \frac{\overline{v}_C v_{in}}{\overline{v}_C - v_{in}} (2 d_0 d_\Delta + d_\Delta^2). \tag{2.39}$$

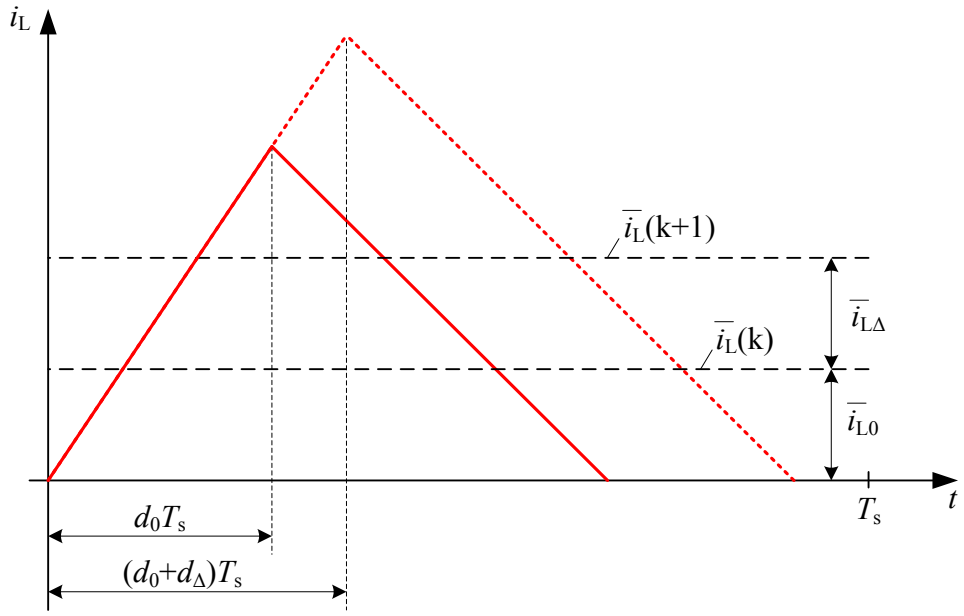

Figure 2.21: Dynamic inductor average current in DCM

Typically the small signal change in the duty-ratio is small compared to the large signal duty-ratio ($d_\Delta^2 \ll d_\Delta$). Consequently, the second term of the equation can be neglected and the duty-ratio-to-inductor-current transfer function for DCM can be stated as

$$G_{id,DCM}(s) = \frac{\bar{i}_{L\Delta}}{d_\Delta} \approx \frac{\overline{v}_C v_{in} d_0 T_s}{(\overline{v}_C - v_{in}) L}. \tag{2.40}$$

2.5 Current Control Design

Responsible for a good power factor in PFC applications is the current control loop. The most common current control method for PFC, average current control in CCM, is described in this section. For this purpose a well designed current compensator is required, which lets the average inductor current track the sinusoidal reference value as good as

possible. In the cascaded control structure of PFC rectifiers the current control loop is the inner loop with the highest bandwidth.

The model of the boost converter derived in the previous section depends on the operating point. Especially in PFC applications with its continuously varying input voltage and current the operation point changes extremely within each line half-cycle (cf. Figure 2.22). But, since the switching frequencies of PFC rectifiers are generally well above line frequency, input and output voltage can be considered as constant values during several switching cycles (Quasi-Static Approach) [Jov06]. Thus, the known small signal model Eq. (2.30) can be utilized for the control loop design.

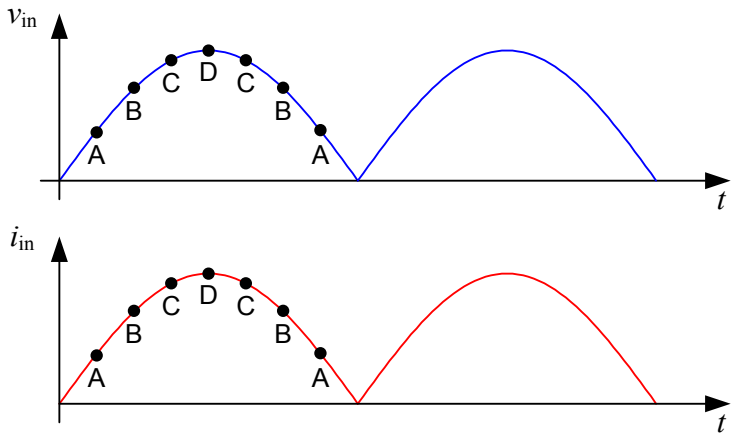

Figure 2.22: Varying operation point within line half-cycle

In the small signal block diagram of Figure 2.23 additionally the transfer characteristics F_m of the PWM and R_s of the current sensing are depicted and need to be considered. They typically have a constant gain and are assumed to be unity in the following design example. In [Rid90] the characteristic $H_e(s)$ of the data-sampling nature for the boost converter current loop is derived. However, since the current loop crossover frequency f_{ci} satisfies $f_{line} \ll f_{ci} \ll f_s/2$, the high-frequency block diagram can be simplified by neglecting $H_e(s)$ [Jov06].

Due to the permanently varying operating point in PFC applications the complete operation range needs to be considered and the worst-case operating point must be identified for controller design. Figure 2.24 shows Bode plots of the boost converter control-to-inductor-current transfer function $G_{id}(s)$ of different operating points. Note that for all Bode Plots normalized transfer functions are utilized, e.g. $G_{id}(s) = \left(\bar{i}_{L\Delta}/1\mathrm{A}\right)/d_\Delta$. In Figure 2.24 it can be seen that the gain of $G_{id}(s)$ is low at low frequencies and depend on the instantaneous line voltage and load current. However, at high frequencies the gain of $G_{id}(s)$ does not depend on input voltage or load current. Since the current loop is a fast control loop the high-frequency approximation of $G_{id}(s)$ Eq. (2.31) can be utilized for design purpose.

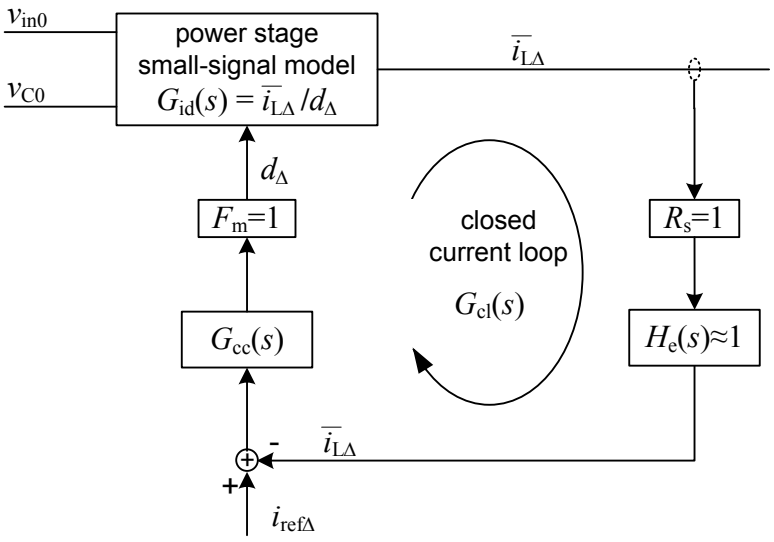

Figure 2.23: Block diagram of closed average current control loop $G_{cl}(s) = \frac{\bar{i}_{L\Delta}}{i_{ref\Delta}}$

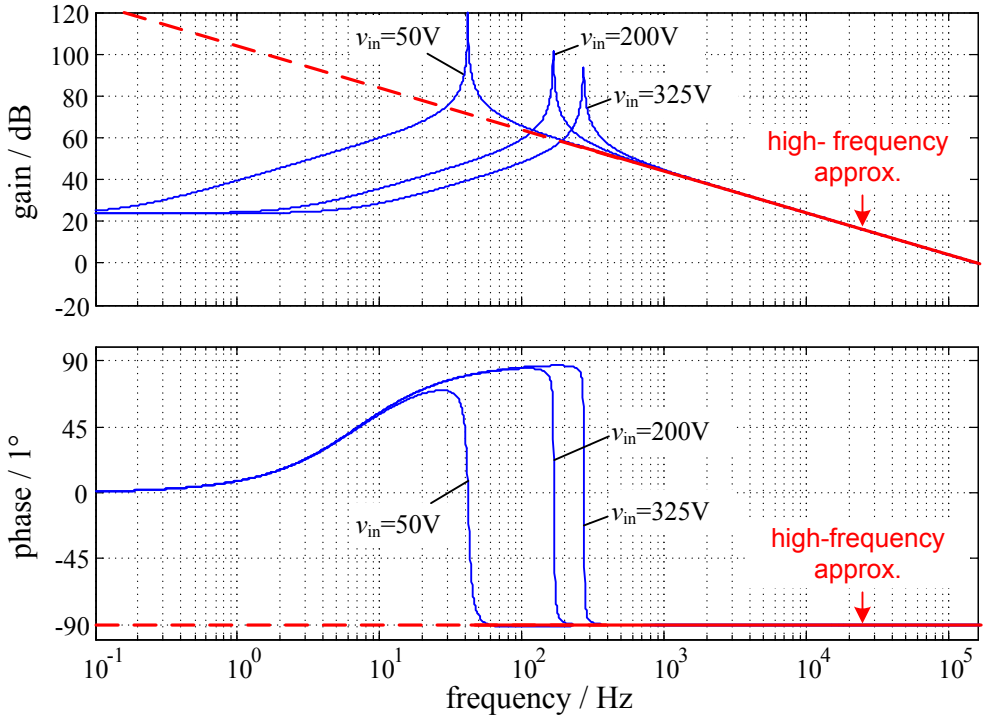

Figure 2.24: Bode plot of the normalized boost converter control-to-inductor-current transfer function $G_{id}(s)$ *for different operating points*

Typically a PI type compensator for the current loop is applied. Its pole at zero frequency (integrator) increases the low-frequency gain of the control loop. The zero is required to get sufficient phase margin at crossover frequency f_{ci}. For adequate stability a phase margin of at least 45° is recommended. Therefore the frequency of the zero f_{zi} should be

approximately at $f_{zi} = f_{ci}/4$ [Jov06, Zac90b]. A good choice for the crossover frequency is $f_{ci} = 2 - 8$ kHz. In order to attenuate switching noise in the current signal, it is advisable to add an additional pole well above crossover frequency without affecting the stability of the current loop. A good choice for this pole is at $f_{pi} = f_s/2$ [Jov06].

In Figure 2.25 the asymptotic Bode plots of the current compensator $G_{cc}(s)$, the high-frequency approximation of $G_{id}(s)$ and of the resulting open-loop transfer function $G_{oc}(s)$ are illustrated.

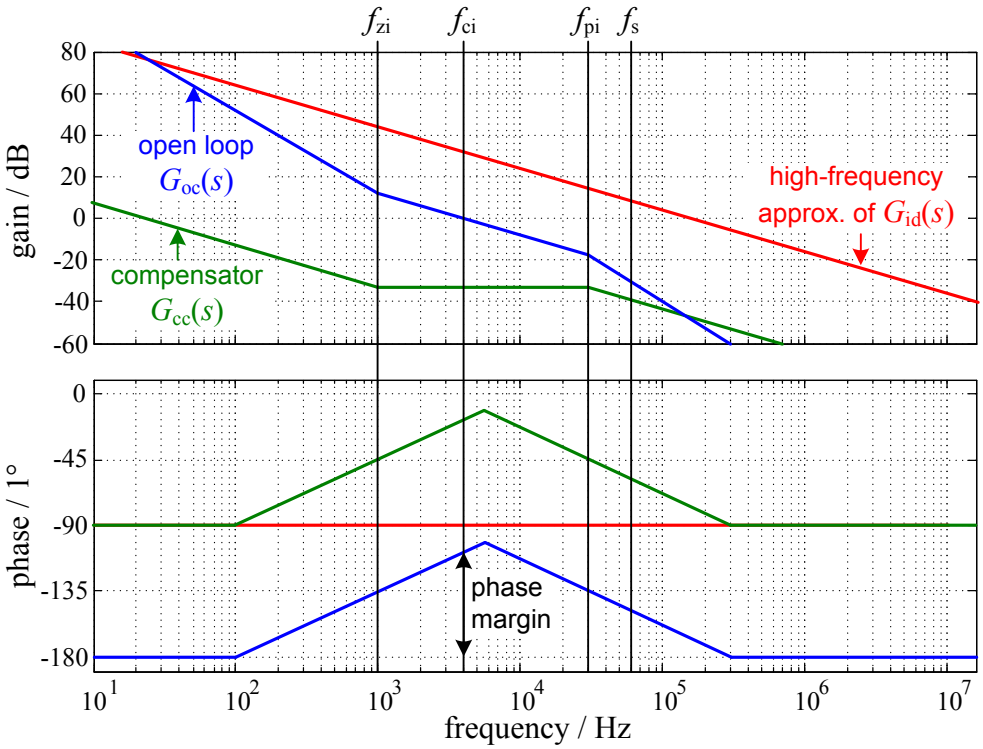

Figure 2.25: Asymptotic Bode plots of high-frequency approximation of the normalized control-to-inductor-current transfer function, compensator transfer function and open loop transfer function

The design of the current compensator is done for CCM to achieve good power factor, but stable operation with adequate dynamic during DCM needs also be ensured. The DCM transfer function (Eq. (2.40)) has a constant gain versus frequency of only a few dB (cf. Figure 2.26). This results in a cross over frequency of the open current loop of only several 10Hz up to few 100Hz. Thus, the current loop has not suitable dynamic to track the current reference value in DCM. However, due to the fact that the loop gain and accordingly the current average value in DCM depends on the input voltage (cf. Eq. (2.35)), a reasonable tracking of the reference current is achieved. Especially at low input voltages, where DCM typically occurs, the average current follows the input voltage almost linearly.

The converter parameters which were used for the controller design are given in Table 2.2.

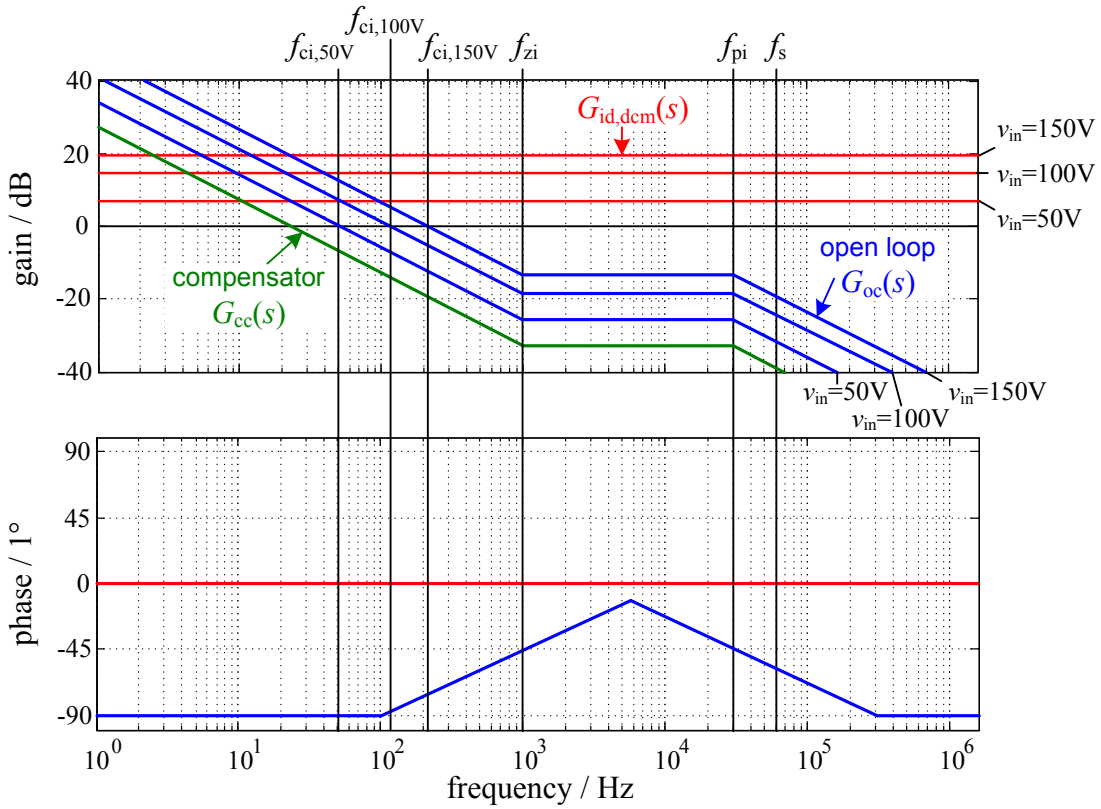

Figure 2.26: Asymptotic Bode plots of the normalized control-to-inductor-current transfer function in DCM for different input voltages at $P_{out} = 500\text{W}$, compensator transfer function and resulting open loop transfer functions

symbol	denotation	value
L	boost inductor	400µH
C	output capacitor	560µF
$R_{100\%}$	load resistance at full load	160Ω
$R_{50\%}$	load resistance at half load	320Ω
$v_{out} = v_C$	output voltage	400V
P_{out}	nominal output power	1000W
$f_s = 1/T_s$	switching frequency	60kHz

Table 2.2: Converter parameters utilized for the controller design

2.6 Voltage Control Design

Besides tracking the input current in order to get the same shape like the input voltage and consequently unity power factor, the second task for PFC rectifiers is to provide constant output voltage. Due to the sinusoidal input voltage and input current a pulsating input power occurs, which causes an unavoidable voltage ripple with twice the line frequency at the output. The amount of this ripple mainly depends on the average input power and the value of the output capacitance. Since the ripple in the output voltage is based on physical reasons, it cannot be compensated with the voltage loop without interfering the power factor. Consequently, a good PFC requires that the output of the voltage compensator is constant during half of the line period. For the voltage loop design this means, that the bandwidth needs to be much lower than twice the line frequency in order to sufficiently attenuate second-harmonic ripple of the output voltage at compensator output [Jov06]. On the other hand a too slow voltage loop cannot respond to load changes in reasonable time. Thus, determining the bandwidth of the voltage loop is a trade-off. A good range for the crossover frequency is $f_{cv} = 5 - 15\text{Hz}$.

Since the voltage-loop is much slower than the current-loop, both control loops can be designed independent from each other. Furthermore, it is not essential for the voltage loop design which current control method is implemented in the inner control, i.e. it can be the same for any type of current control. The closed current loop is part of the control path in the voltage loop and can be assumed to be unity at the low crossover frequency of the voltage loop.

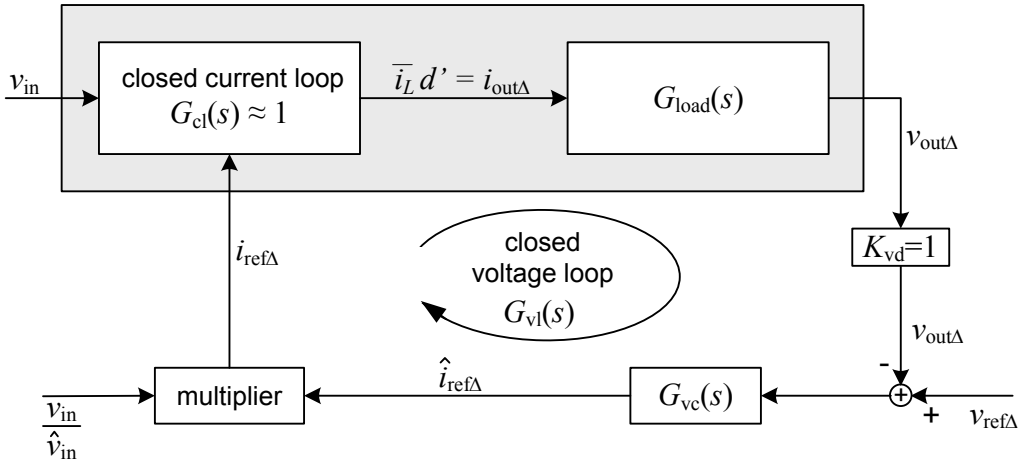

Figure 2.27: Block diagram of closed voltage control loop $G_{vl}(s) = \frac{v_{out\Delta}}{v_{ref\Delta}}$

The block diagram of the output voltage control loop is depicted in Figure 2.27. For the design example the voltage divider K_{vd} for the output voltage measurement and the multiplier are assumed to have a constant gain of $|G(s)| = 1$. Thus, only the transfer characteristic of the output capacitor with connected load remains, which needs to be

considered for the design of the voltage compensator. Assuming a resistive load with $R_{load} = R_{100\%}$ (cf. Table 2.2) the transfer characteristic of the load results to

$$G_{load}(s) = \frac{v_{out\Delta}}{i_{out\Delta}} = \frac{R_{100\%}}{1 + sR_{100\%}C_{out}}. \tag{2.41}$$

As voltage compensator a PI-type controller is applied, which has the zero at approximately $f_{zv} = f_{cv}$ to achieve a phase margin of at least 45° (55° is achieved with the applied values). Figure 2.28 shows the Bode plots of the load, the voltage compensator and the resulting open loop transfer function.

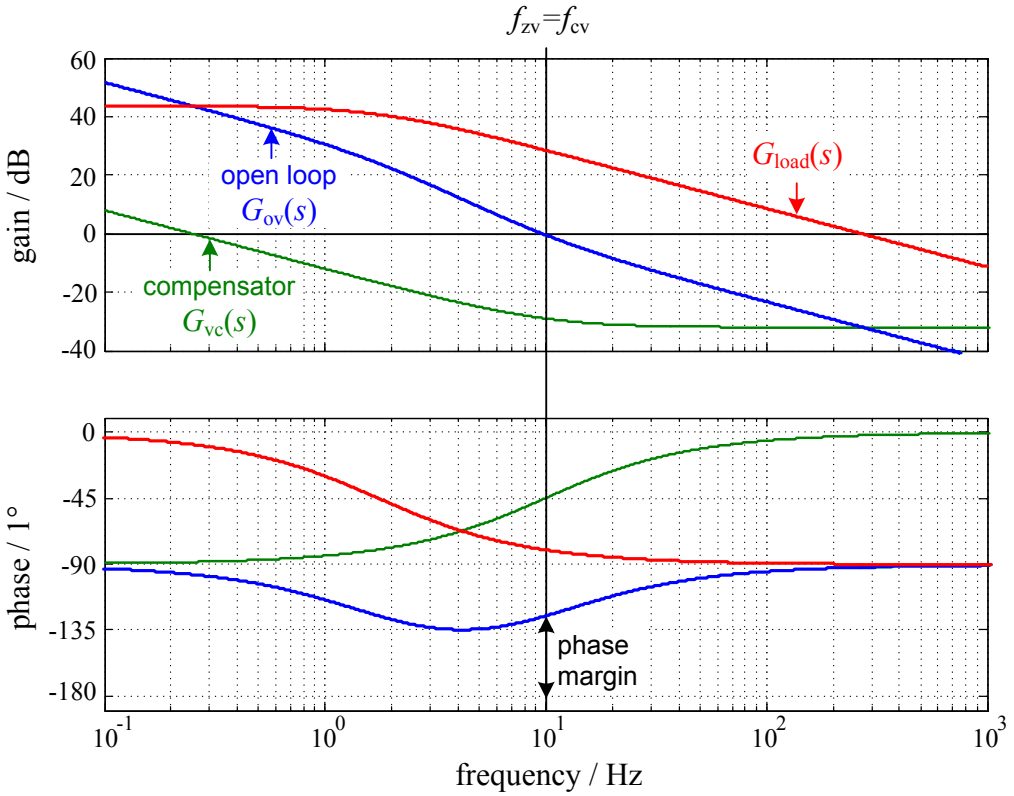

Figure 2.28: Bode plots of the normalized voltage loop control path $G_{load}(s)$, compensator transfer function $G_{vc}(s)$ and open loop transfer function $G_{ov}(s)$

2.7 Multiplier and Load Feed-Forward Control

The main difference between the PFC rectifier control structure and that of conventional DC-DC converters is the multiplier and load feed-forward unit depicted in Figure 2.29. The multiplier is utilized to generate the sinusoidal reference value for the current control loop in order to achieve unity power factor. For this purpose a normalized signal of the rectified input voltage needs to be generated. This means that the instantaneous value of the rectified input voltage needs to be divided by a value which is proportional to the DC

component of the rectified input voltage, e.g. the amplitude value $\hat{v}_{in}$ or root mean square (RMS) value V_{in}. By multiplying the normalized voltage signal with the voltage compensator output the sinusoidal current reference signal is generated.

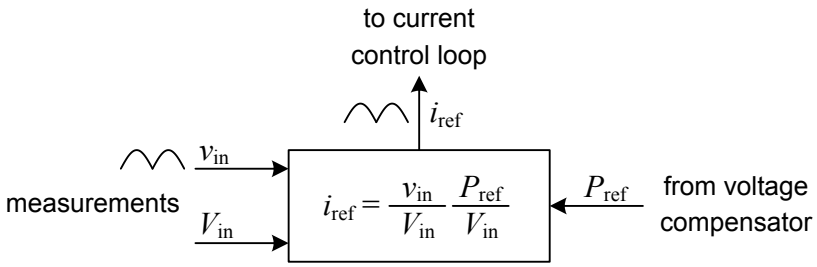

Figure 2.29: Multiplier and load feed-forward unit

Due to the fact that the bandwidth of the voltage loop is too low to compensate variations in the line voltage in adequate time, a load feed-forward (LFF) control is implemented in most PFC applications to achieve constant input power under fluctuation of the line voltage. With variation of the line voltage the input current needs to be changed in opposite direction in order to keep the input power constant. This task can be accomplished by a further division of the DC proportional signal of the rectified input voltage. Accordingly, with LFF the voltage compensator output signal physically is a power signal P_{ref} and the current reference value is generated by

$$i_{ref} = P_{ref} \frac{v_{in}}{V_{in}^2}. \tag{2.42}$$

With this LFF the voltage compensator does not need to respond to variations in the line voltage. However, for the generation of the feed-forward signal a further design tradeoff arises. This signal ideally should be pure DC and proportional to the rectified input voltage. Typically the feed-forward signal is generated by analog filtering and for high dynamic of the LFF higher bandwidth of the filter is required. But, higher bandwidth means higher line-frequency ripple in the feed-forward signal, which causes distortions in the current reference signal [Jov06]. Advantageous for this design problem is a digital implementation where the amplitude of the line voltage is identified within every half-cycle. Thus, a feed-forward signal is generated, which is constant during the next whole line half-cycle.

For improving the dynamic response during load variation a further feed-forward loop is practical [Zac90b]. For this purpose a feed-forward signal proportional to the load current can be utilized as additional input of the multiplier.

3 Digital Converter Control

As mentioned before digital control offers a multitude of advantages compared to analog control. However, the controlled converter is still in continuous time domain. Such systems with both continuous-time and discrete-time components are called sampled-data systems [Fra98]. To perform the digital control, continuous-time signals need to be converted into discrete-time domain and after processing in the DSP or µC the signals have to be converted back from digital-time to continuous-time domain. Dedicated DSPs and µCs with suitable built-in peripherals are available for that purpose. The optimal control loop design and optimization requires understanding and models of the sampling process, analog-to-digital conversion (ADC), digital PWM and of course digital controller design [BuMa06]. Figure 3.1 shows the structure of a digital current control for a boost converter.

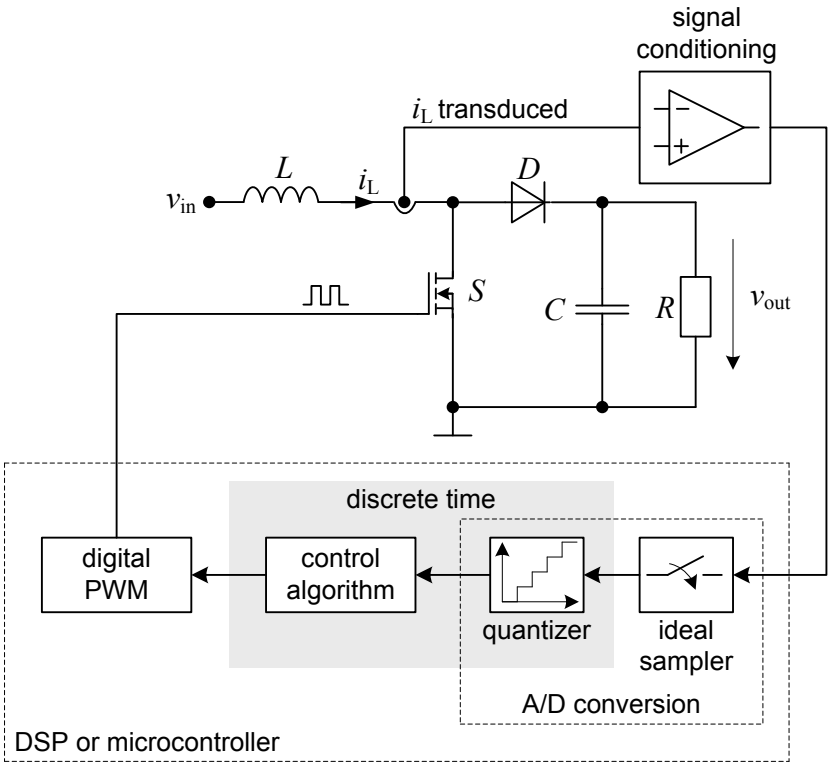

Figure 3.1: Typical structure of current control loop with digital controller

3.1 Analog to Digital Conversion (ADC)

One important part of the digital control loop is the signal acquisition for the digital controller. Therefore a suitable description of the ADC process is required, which can be

mathematically modeled as cascaded connection of an ideal sampler and an *n*-bit uniform quantizer [BuMa06].

3.1.1 Sampling Process

The sampling process converts a continuous-time signal into a discrete-time signal. The sampler can be represented by a simple switch, which is closed at the time instants $t = kT_s$ for a very short duration. For mathematical representation of the sampling process the impulse modulation can be utilized. Thus, the output of the sampler is considered as a stream of null duration impulses [Fra98]:

$$y^*(t) = y(t) \sum_{k=-\infty}^{\infty} \delta(t - kT_s) = \sum_{k=-\infty}^{\infty} y_a(k)\delta(t - kT_s), \tag{3.1}$$

with $y_a(k) = y(kT_s)$. The impulse coefficients are equal to the signal at the sampling instants (cf. Figure 3.2). The Laplace transform of $y^*(t)$ can be expressed by

$$Y^*(s) = \sum_{k=-\infty}^{\infty} y_a(k)\, e^{-skT_s}\,. \tag{3.2}$$

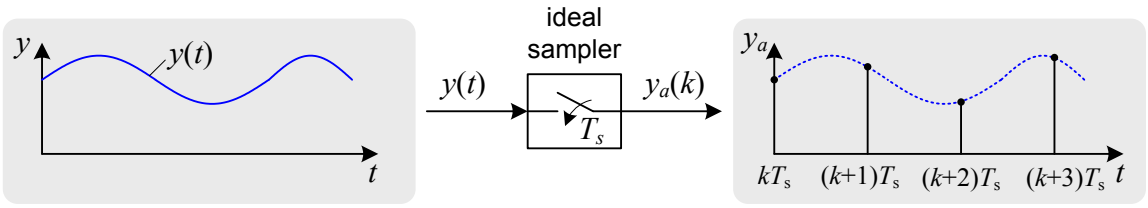

Figure 3.2: Sampling process

With the utilized constant sampling period T_s this process is called uniform sampling. From Shannon's Theorem it is known that it is necessary to choose the sampling frequency f_s at least two times larger than the frequency bandwidth of the sampled signal, in order to be able to reconstruct a continuous-time signal from samples. The consequence of violating Shannon's Theorem is the aliasing phenomenon illustrated in Figure 3.3. Hence, it is essential to limit the frequency spectrum of the sampled signal by filtering, in order to make it negligible above half of the switching frequency [BuMa06]. This limit frequency is also known as Nyquist frequency.

Since the filtering needs to be performed before the sampling process, the anti-aliasing filters are implemented as analog first- or second order filters [Jov12].

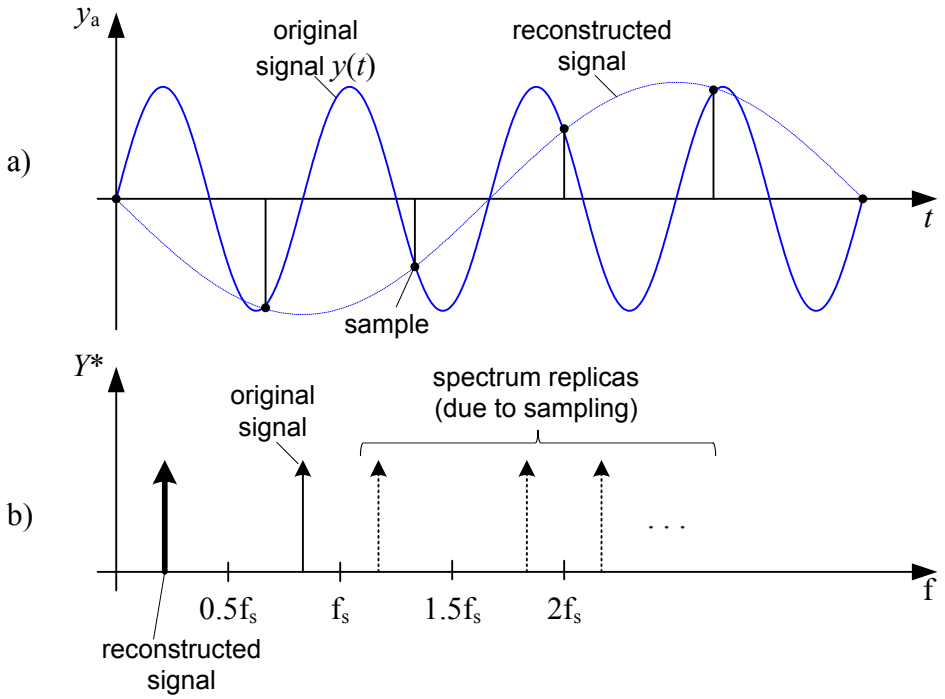

Figure 3.3: a) Reconstructed signal (aliasing) because of a too low sampling frequency b) Interpretation of the aliasing effect in frequency domain

3.1.2 Quantization

The signal after the sampling process is discrete in time, but it has still continuous amplitude values. The quantizer transforms the continuous amplitude values into discrete amplitude values. Because the sampled signal needs to be present at the input of the quantizer during the entire conversion time, the sample value is held constant by a hold circuit until the next sampling is performed. The output of the quantizer can only take a finite number of values, which depends on the number of bits (cf. Figure 3.4). An n-bit quantizer has 2^n quantization levels. With the full scale range (FSR) of the input voltage the resolution or quantization step q can be expressed by

$$q = \frac{FSR}{2^n}. \tag{3.3}$$

The embedded ADCs of today's DSPs and µCs typically provide $FSR = 3.3\text{V}$. Due to the fact that the resolution of the ADC is limited, a quantization error e_q occurs (cf. Figure 3.4). This loss of information from the input signal is inherent to the ADC process and unavoidable [BuMa06]. Thus, a key factor to reduce this quantization error is to fully exploit the ADC input voltage range.

For the control loop design it should be evident, that the quantizer as well as the ideal sampler is an essentially instantaneous function, which does not contribute to the dynamic of the system [BuMa06].

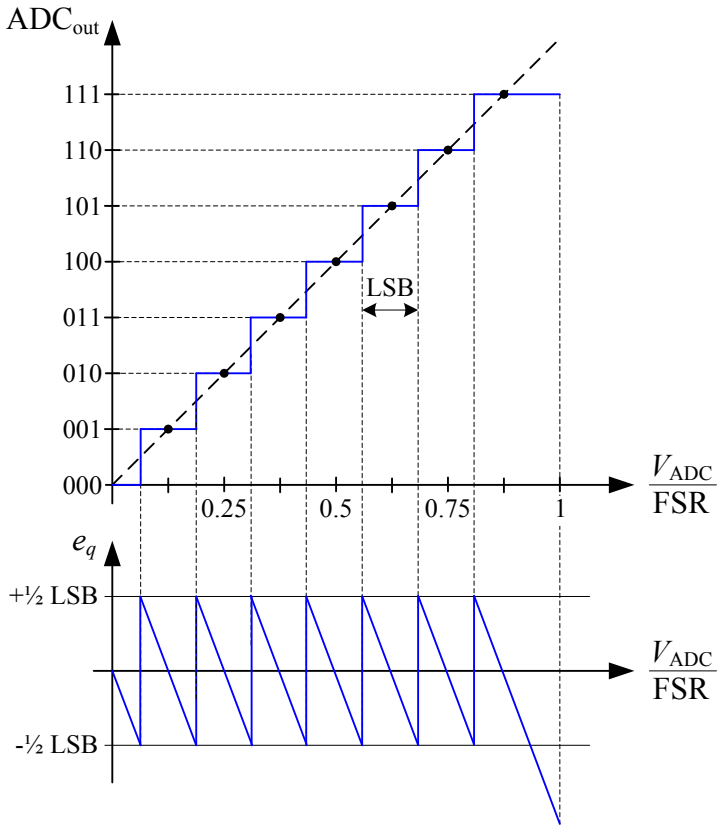

Figure 3.4: Transfer characteristic of a 3-bit rounding type quantizer and quantization error e_q

3.2 Digital Pulse Width Modulation (DPWM)

The conversion back from the discrete-time domain to continuous-time domain for switching converters is performed by a digital pulse width modulation (DPWM) unit. For the boost converter with fixed switching frequency the DPWM gets the computed duty-ratio and generates the continuous gate-drive signal for the switch.

Conventional analog PWMs use a triangular or a sawtooth carrier signal and an analog comparator. The analog implementation ensures minimum delay between the modulating signal and the duty-ratio. The delay is only caused by the non-ideal analog components and can always be considered negligible; concluding that the phase lag is actually zero [BuMa06].

For DPWM a discrete counter is utilized to generate the carrier signal and the analog comparator is replaced by a digital one. The counter is incremented with every clock pulse

and if the counter value is equal to the programmed duty-ratio, the digital comparator resets the gate-drive signal. The duty-ratio resolution of the DPWM is determined by the ratio between the modulation period T_s and the counter clock period T_{clk}:

$$\Delta d = \frac{T_{clk}}{T_s} = \frac{f_s}{f_{clk}} \tag{3.4}$$

The value Δd also represents the duty-ratio quantization step.

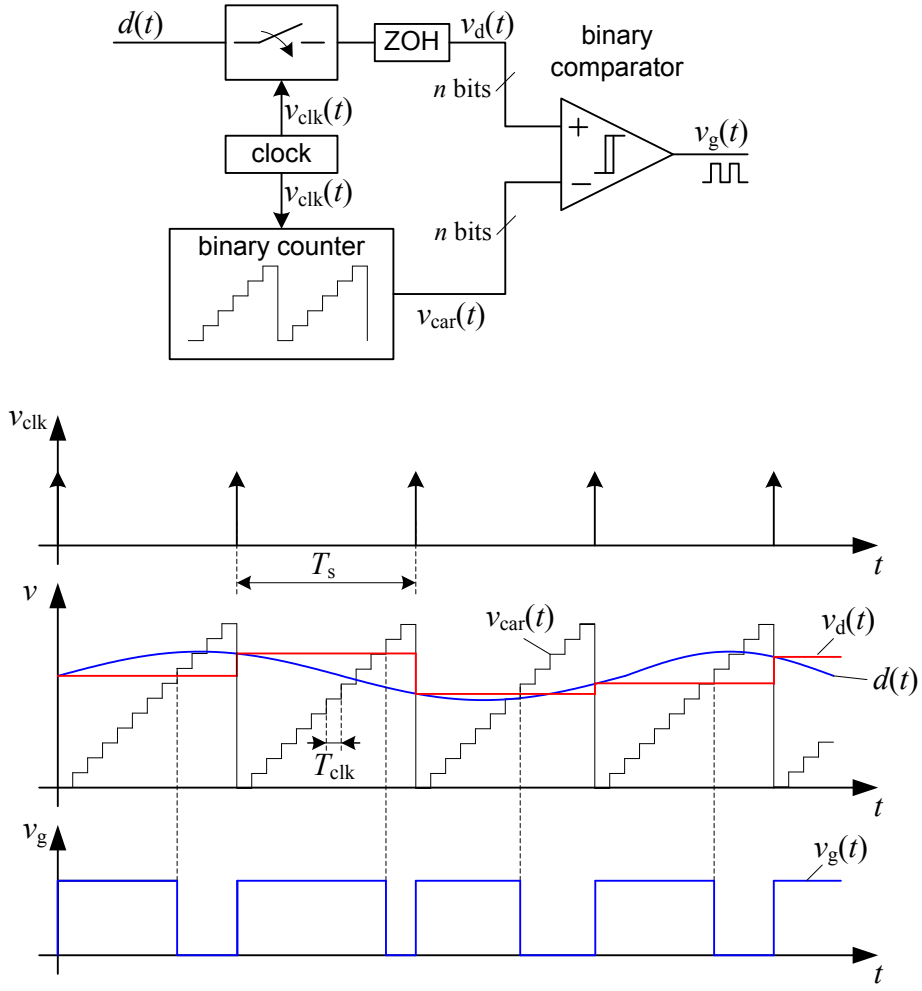

Figure 3.5: Structure of an digital PWM with signal waveforms versus time of clock signal, carrier signal $v_{car}(t)$, duty-ratio $d(t)$, duty-ratio after zero-order-hold (ZOH) $v_d(t)$ and gate signal $v_g(t)$

Typically the modulating signal update of the DPWM is performed only at the beginning of each PWM period (cf. Figure 3.5). This mode of operation can be modeled as a sample-and-hold effect [BuMa06]. This means that a change in the programmed duty-ratio during the modulation period has no effect on the output in the actual period. It can only be considered for the following PWM period. This inherent delay effect of DPWM is the major difference to the analog implementation, where a change in the duty-ratio during the

PWM period has effect on the output with negligible delay. The consequence of this systematic delay of the DPWM is a significant reduction of the control loop phase margin. However, the DPWM can also be implemented with a double or multi update mode to reduce the delay and consequently the loss of phase margin [BöBu13], but these modes of operation are not suitable for all SMPS applications.

For an appropriate small-signal model the DPWM can be represented by an ideal sampler followed by a zero-order hold (ZOH) [BuMa06]. The quantization effect is neglected. For triangular carrier signal, where modulating signal is sampled in the middle of the switch-on period the small-signal transfer function in Laplace domain can be derived as [BuMa06]:

$$G_{PWM}(s) = \frac{v_g(s)}{d(s)} = \frac{1}{2c_{PK}}\left(e^{-s(1-D)\frac{T_S}{2}} + e^{-s(1+D)\frac{T_S}{2}}\right) \tag{3.5}$$

Where $v_g(s)$ and $d(s)$ represent the Laplace transforms of $v_g(t)$ and $d(t)$.

3.3 Digital Controller

Compared to analog control, where the compensator is realized by operational amplifiers, the control law in digital control is realized by binary calculations [Xie03].

An important issue for an accurate control loop design is the implementation of a suitable data acquisition path. For the current control loop for example the data acquisition path is the cascaded connection of the current sensor, a signal conditioning electronic circuit and the ADC. A well designed signal conditioning circuit amplifies the sensor signal to fully exploit the input voltage range of the ADC and filters the signal to avoid aliasing effects [BuMa06].

Since the control path is still in continuous-time domain, it is often desired to design the controller also in continuous-time domain. Such a quasi-continuous sampling controller design can be employed, if the sampling period is 10-20% of the summarized time constants of the analog control path, if the order of the systems is at least two [Lat95]. The advantage of this approach is that no transformation of the converter model into discrete-time domain is required and the well known controller design methods of the Laplace domain can be applied.

Finally the transfer function of the designed converter needs to be transformed into a difference equation for implementing on a DSP or µC.

Synchronization between sampling and PWM

It was already mentioned that in order not to violate Shannon's theorem, the sampling frequency should be much higher than the frequency of the sampled signal. Consequently a sampling frequency, which is at least one order of magnitude higher than the switching frequency of the converter, would be required [BuMa06]. However, most of the utilized

standard DSPs and µCs do not support such high sampling frequencies. At least for the current control loop, where high bandwidth is desired, the sampling frequency should be typically as high as possible.

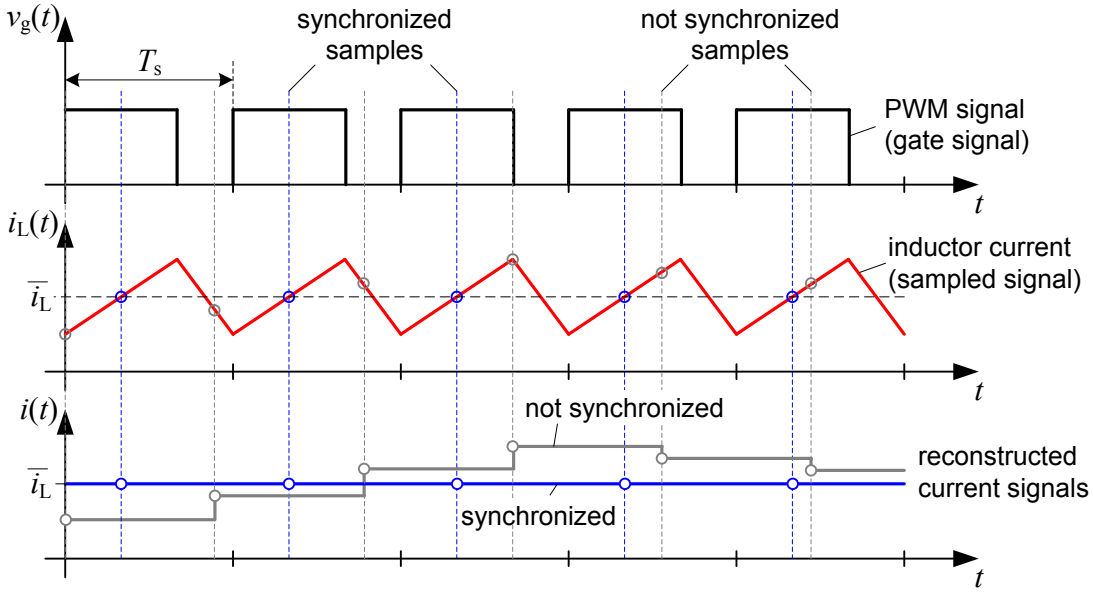

Figure 3.6: Synchronized sampling in the middle of the switch-on period and not synchronized sampling of a current signal

In most applications, especially in PFC applications, the average value of the inductor current needs to be controlled and the switching frequency ripple is only undesirable noise. Considering this fact the precise discrete sampling and the synchronization possibility of the sampling process and the PWM period can be utilized in order to directly sample the average value of the inductor current (cf. Figure 3.6). This synchronized sampling also known as regular sampling can be either done at the middle of the switch-on or the switch-off period. If double update mode of the DPWM is possible, also sampling at both instances can be performed to reduce the delay time of the control loop [BöBu13]. Of course, with this method Shannon's theorem is violated, but if the sampling and switching process are suitably synchronized, the normally undesirable aliasing effect is exploited to reconstruct the average value of the inductor current [BuMa06]. In addition there is no need of an analog anti-aliasing filter to eliminate the ripple from the sampled signal.

4 State of the Art of Interleaved PFC Rectifier Control

Before figuring digital PFC control a review of the traditional analog control realization is given. After that full digital implementation of the conventional cascaded PFC control, which is already state of the art, is described.

4.1 Review of Analog PFC Control

The analog technique has dominated the PFC control for many years. In particular for the fast current control loop the high bandwidth of analog controllers was essential in order to faithfully track the semi-sinusoidal current reference. Consequently, a multitude of specific analog controller ICs for PFC applications are available, which are easy to understand and featuring a variety of functionalities at relative low cost.

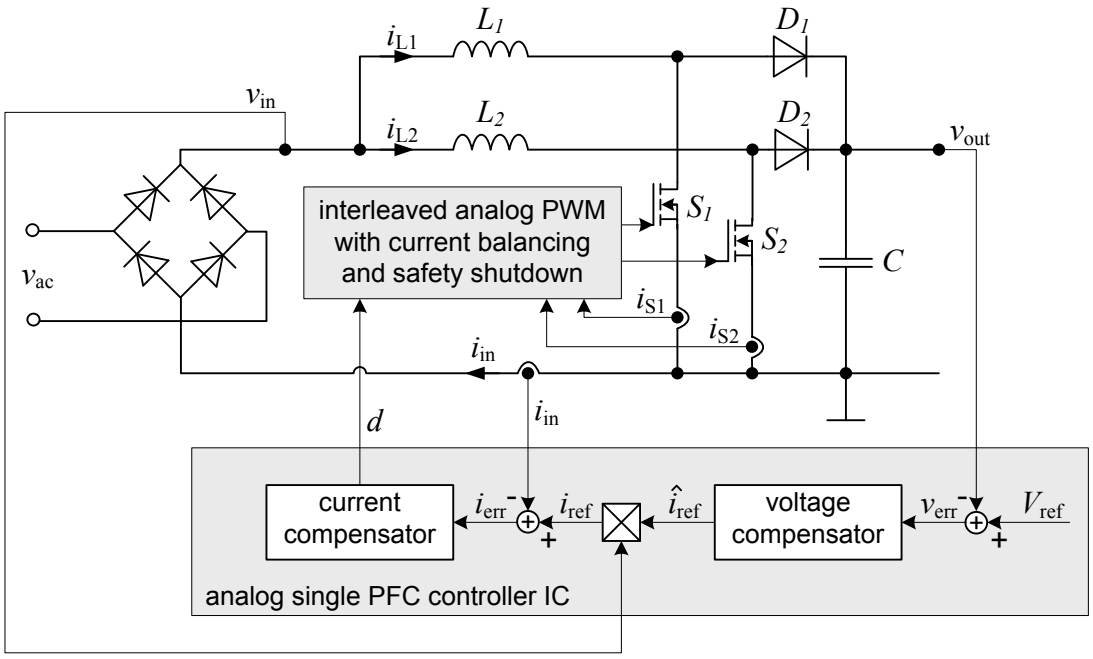

Figure 4.1: PFC rectifier control structure for two interleaved rails realized with a single PFC controller IC and additional analog circuitry for interleaved clock signals, PWM, current balancing and safety shutdown

For a long period only controller ICs for single PFC rectifiers were available (for instance UCC28019 [TI07], UCC2855 [TI05] and ML4824 [Fai03]). Consequently, these ICs were also used for interleaved PFC rails (cf. Figure 4.1) and the current balancing was implemented using additional discrete components. For this reason some features of the IC

like the PWM unit and some protection functions could not be used. Figure 4.2 shows the scheme for such a separate PWM with current balancing functionality [Gro09]. It is realized with an inner peak current loop, which inherently provides ideal current sharing. Interleaved clock signals are provided by a discrete timer IC to trigger the switching cycles and generation of sawtooth signals for the required slope compensation. The compensation ramp and the transistor current signal are added and passed to the comparator input. The current compensator for tracking the overall input current is realized with an operational amplifier (opamp), which is included in the controller IC. The desired dynamic for the current loop is determined by connecting external resistors and capacitors.

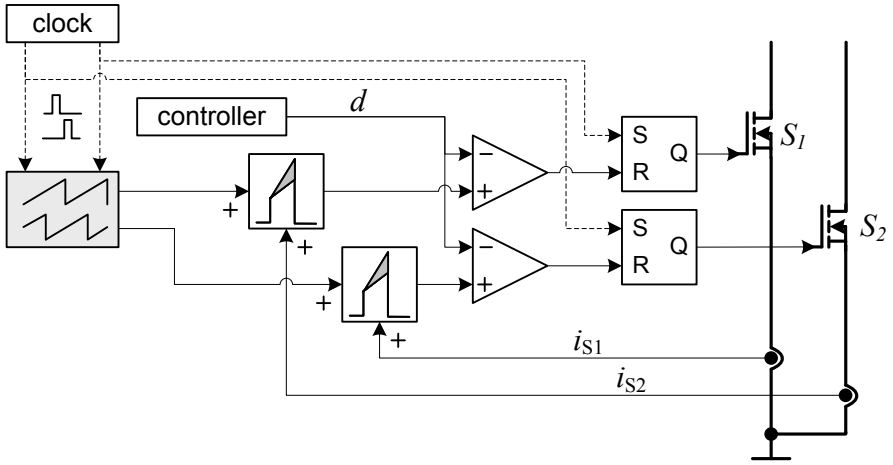

Figure 4.2: Scheme of an interleaved PWM with current balancing

By now there are also PFC control ICs for two interleaved rails available [TI11, Fai13]. Some of those even support multi-rail interleaving by operating several control ICs in parallel [TI11]. The ICs for interleaved PFC rectifiers have two independent current compensators which get the same set point value. The rail currents are typically measured in the switch path with simple current transformers. In order to control the current average values the absent current down slopes are reconstructed by a current synthesizer [TI11]. With this method the average current values in DCM are not covered correctly and the resulting error cannot be compensated completely.

The generation of the semi-sinusoidal current reference for single rail and interleaved rails control ICs does not differ. The measured output voltage is subtracted from the set point value and the resulting error signal is passed to the voltage compensator. The voltage compensator is also realized with an integrated opamp. The compensator output is proportional to the RMS value of the required input current. To generate the sinusoidal current reference this value is multiplied with the measured input voltage by an analog multiplier. Additionally the result is divided by the square of the RMS proportional value of the input voltage. This operation represents the load feed-forward control described in Section 2.7. Due to the very slow voltage control loop a variation of the input voltage cannot be compensated in acceptable time. Thus, the feed-forward compensation ensures

faster change of the current reference after input voltage variation in order to keep the input power equal to the requested output power. However, by the analog generation of the input voltage RMS proportional value there is also a trade-off between fast response and low line frequency ripple [Xie03, Jov06]. Ideally the RMS proportional value should be a pure DC signal. But in order to get a faster response that value is generated with higher bandwidth and therefore still has some line frequency ripple, which causes distortion in the current reference signal.

Another drawback of PFC control ICs is the analog realization of the multiplier and divider. Those have typically high tolerances and non-linear characteristic, which can cause distortions when operating in a wide input voltage range [FuCh01].

4.2 Full Digital Average Current Mode PFC Control

As a result of low cost DSPs and μCs with sufficient computing power and suitable peripherals full digital control of PFC rectifier is already state of the art. Numerous of publications on this topic have been published in the last years, for example [Mit96, FuCh01, AME05, Pro03, Pro06, Zha04, Zum02, QLi09].

In many of the digital implementations the structure of the PFC control is pretty much the same than those of traditional analog realizations. However, some modifications are obvious or need to be introduced. The main difference to analog control is the sampling process in digital control loops. While the analog controller receives the pure signal, only discrete samples of the time-continuous signal can be passed to the digital controller. As explained in Chapter 3 the signals need to be filtered before sampling to avoid aliasing or the required average value needs to be sampled directly with synchronized sampling. The most common method is to sample the switch current in the middle of the switch-on interval to get the inductor average current for the controller. By designing the current controller the phase lag, which is introduced by the digital delay, needs to be considered. Compared to the analog control the attainable bandwidth is decreased, accordingly.

Figure 4.3 shows the structure of a digital control for an interleaved PFC rectifier. In order to achieve balanced inductor currents, every rail is assigned its own current controller. With this technique there is no need of a shunt resistor for input current measurement. In addition this technique exhibits a good performance and can be implemented easily. The controller needs only to be designed one time and the parameters are used for each rail. However, the required computing power for executing the current control increases linearly with the number of interleaved rails.

If the computing power is limited, it is also possible to use a shunt resistor in order to control the overall input current with a single current controller. Hence, balanced rail currents are not ensured and additional balancing control is required. The balancing control is performed with lower bandwidth in this case by evaluating the sampled switch currents.

An appreciable improvement of the digital implementation is the precise generation of the semi-sinusoidal current reference signal.

From the multitude of equidistant samples the true RMS value of the input voltage can be computed and the amplitude value can be identified. This values are updated at every line voltage zero crossing. Thus, the normalized input voltage is used for multiplying with the voltage controller output value and the response of the power feed-forward is accelerated without introducing any line frequency ripple.

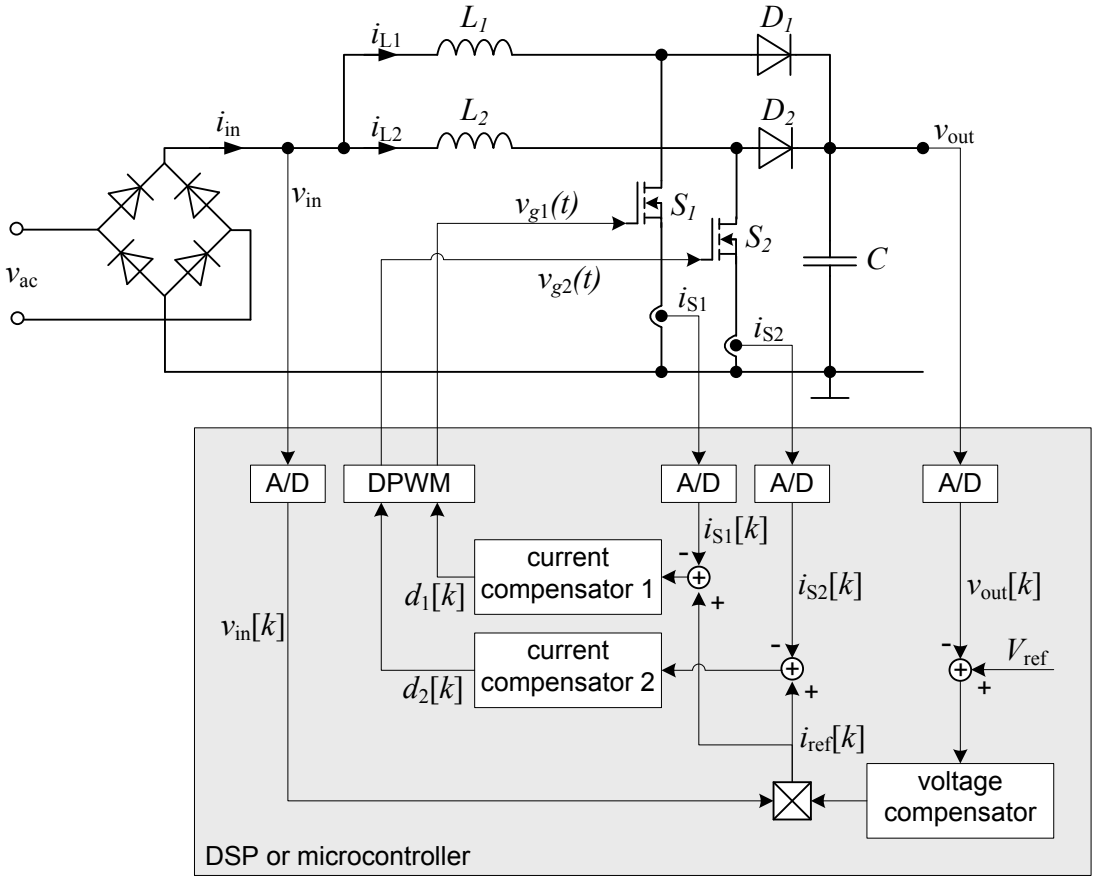

Figure 4.3: Digital control of an interleaved PFC rectifier with two independent current compensators for balanced rail currents

One essential advantage of digital control is the possibility to implement sophisticated control algorithms. In the following two valuable measures are described, which lead to improved current tracking especially in DCM. The first introduces a correction factor to compute the current average value from the current sample in DCM and the second describes the implementation of a duty-ratio feed-forward loop for DCM and CCM operation.

4.2.1 Sample Correction in DCM

Also in DCM the sampling of the inductor current is performed at half of the switch-on duration. However, this sample values are not equal to the inductor average value in DCM and consequently a systematic error occurs (cf. Figure 4.4). In [Gus03] a method is presented, which compensates this error.

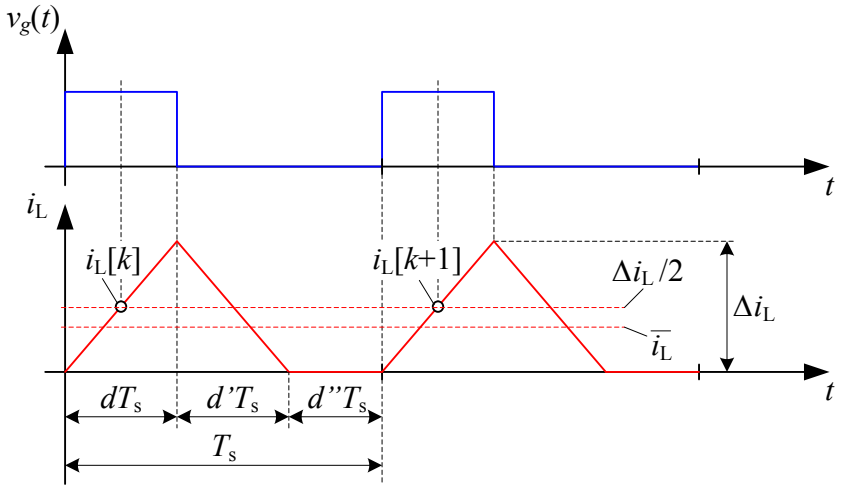

Figure 4.4: Systematic error in current average value due to sampling the inductor current in the middle of the switch-on time in DCM

The average current value in DCM can be computed by integrating the triangular current shape over one entire switching period. Therefore the current shape is splitted into two intervals, the current rising interval dT_s and the current falling interval $d'T_s$. By dividing the sum of this two current components by the switching period the current average value results:

$$\bar{i}_L = \frac{\Delta i_L}{2} \frac{(d + d')T_s}{T_s} \tag{4.1}$$

Consequently, the sampled current value $\Delta i_L/2$ needs only to be multiplied by the correction factor

$$\kappa = d + d'. \tag{4.2}$$

For the fraction d the value determined by the current controller is utilized directly to compute the correction factor. The fraction d' needs to be computed with

$$d' = \frac{\Delta i_L L}{T_s(v_{out} - v_{in})} = d\frac{v_{in}}{v_{out} - v_{in}}. \tag{4.3}$$

Thus, the algorithm for the correction factor results as

$$\kappa = d\frac{v_{out}}{v_{out} - v_{in}}. \tag{4.4}$$

In DCM the value of κ is always smaller than unity. With entering CCM the value would exceed unity, for which reason a limitation $\kappa \leq 1$ is required. Consequently, the correction factor can be applied in both DCM and CCM. A differentiation is not required, but beyond that the correction factor can be utilized to identify DCM and CCM operation for other purposes.

4.2.2 Duty-Ratio Feed-Forward Control for CCM and DCM

In PFC applications the operation point of the boost converter varies continuously in a wide range. Consequently, the current compensator needs to vary the duty-ratio in a wide range. Due to this fact it don't suffice to give the current compensator a good small signal disturbance response, but also to offer a suitable large signal reference-variable response.

Moreover, the converter operates not only in CCM. Typically the operation mode switches within the line period between CCM and DCM. From Section 2.4.3 it is known, that the duty-ratio-to-inductor-current transfer functions of both modes differ significantly. This results in abrupt steps in the converter dynamic during a line period. Since the current compensator is mostly designed for CCM, the current tracking in DCM is not satisfying, causing input current distortion.

In [Gus04] a duty-ratio feed-forward control is presented, which adjusts the large signal duty-ratio in CCM as well as in DCM. For this purpose the voltage ratio of the ideal boost converter for both conduction modes are computed with

$$d_{ff,CCM} = 1 - \frac{v_{in}}{v_{out}} \tag{4.5}$$

and

$$d_{ff,DCM} = \sqrt{\frac{2\bar{i}_L L}{v_{in} T_S}\,\frac{v_{out} - v_{in}}{v_{out}}} = \sqrt{\frac{2G_{in} L}{T_S}\,\frac{v_{out} - v_{in}}{v_{out}}}. \tag{4.6}$$

From Eq. (4.6) it becomes clear, that the duty-ratio in DCM also depends on the desired input conductance G_{in} of the converter. The curves of the feed-forward duty-ratios during a line half-cycle are depicted in Figure 4.5 for different G_{in}. The transition from DCM to CCM and back take place at the intersection of both curves. Accordingly, the valid value for the feed-forward loop can be identified simply by computing the CCM and DCM values and utilizing only the lower value. In Figure 4.6 a scheme of the generation of the duty-ratio is illustrated.

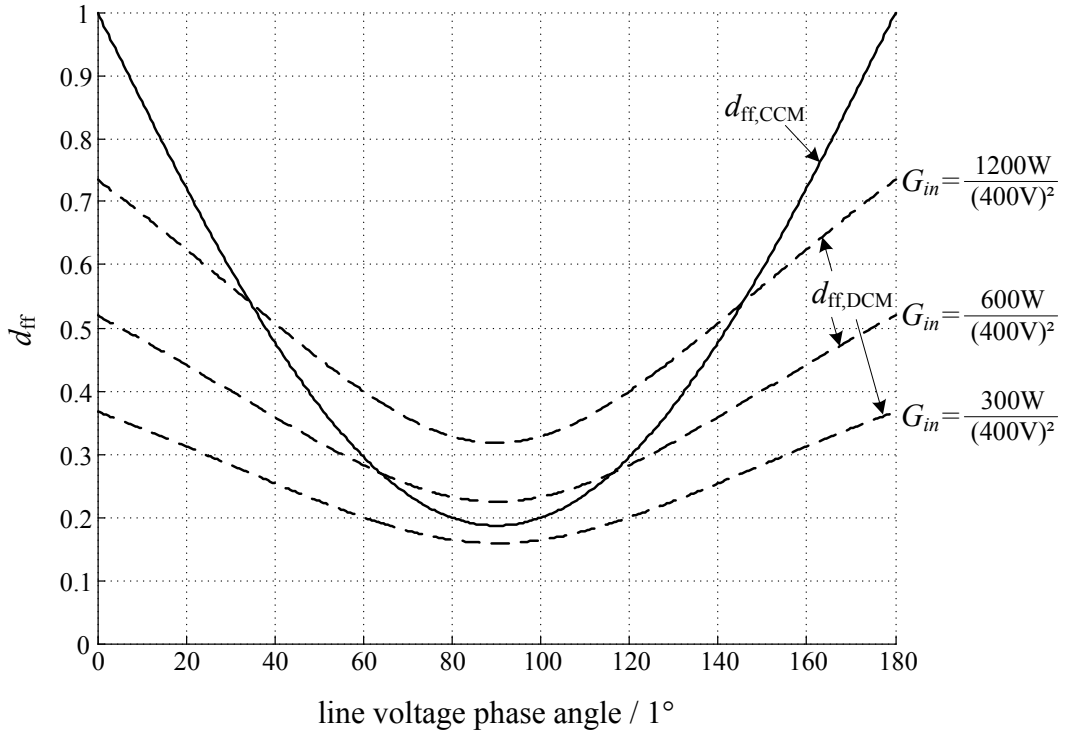

Figure 4.5: CCM and DCM feed-forward duty-ratio values during line half-cycle for different output powers ($V_{ac} = 230\text{V}$; $L = 450\mu\text{F}$; $f_S = 80\text{kHz}$)

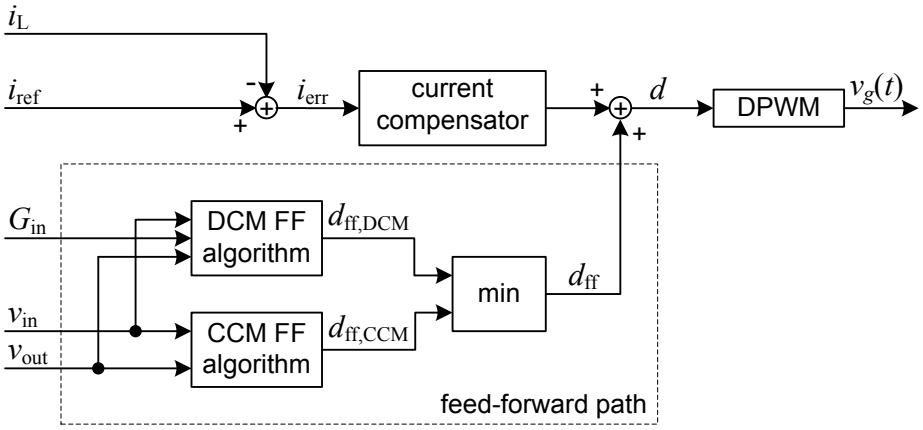

Figure 4.6: Generation of the duty-ratio with feed-forward control for CCM and DCM

In the next four chapters advanced control techniques for interleaved PFC rectifiers are presented, which utilize digital control. By describing the different control concepts focus is laid upon the implementation of the current control and the current balancing. The voltage compensator can be realized in the same way for all proposed control concepts and is not an issue.

5 Semi-Digital PFC Control (Mixed Signal Control)

As a smart combination of analog and digital control techniques a semi-digital control concept is presented, which already offers the potential for implementing a multitude of advanced power management features in digital.

5.1 Control Structure

In many cases available analog controller ICs for PFC applications do not meet adequately the required specifications of the power supply. To fulfill those requirements, additional analog circuitry is needed as already mentioned in Section 4.1. Thus, it is obvious to change over to a completely digital control structure like described in the previous section, in order to employ the benefits such as flexibility and programmability as well as decreased number of active and passive components. However, the current control loop has to provide a much higher bandwidth than the voltage control loop. Therefore, high computing power and costly DSPs or μCs are needed for applying fully digital PFC control. Even fully digital control still needs some analog circuits for time-critical safety shutdown or shunt signal amplification.

Considering these pros and cons, a semi-digital concept turns out as an attractive compromise [Gro09]:

- The current controller including time-critical protection functions retains the conventional analog structure.
- The voltage controller, feed-forward compensation, multiplier, PWM clock generator and non-time critical protection functions are implemented on a μC.

Such a solution is characterized as follows:

- Because the required bandwidth of the voltage control is usually small, a cost-effective DSP or μC is sufficient.
- High current control bandwidth is ensured by the analog circuitry.
- There is no need to apply specific analog controller ICs.
- Many innovations of digital control still can be realized, because issues of adaptive and nonlinear control, programmability etc. often focus on voltage control or rather on generating the current loop reference.

Figure 5.1 shows the semi-digital control structure with the separated analog current controller, analog PWM including current balancing and the digital voltage controller. ADCs provide the actual values of the rectified input voltage v_{in} and PFC rectifier output voltage v_{out}. There is no need of converting any currents for the control loop. Thus, only relatively slowly varying signals need to be converted, making costly ADCs with a high sample rate superfluous.

In addition the digital part observes the range of v_{out} and v_{in} and can trigger a safety shutdown at overvoltage or undervoltage conditions.

If no specific digital-to-analog converter (DAC) is available on the DSP or µC, the output value i_{ref} can be passed to the analog current controller as pulse width modulated signal and a simple RC low-pass acts as DAC (cf. Figure 5.1). For current control a PI type controller with additional low pass filtering is applied, which is implemented using a single opamp (cf. Figure 5.2). Another PWM channel also with RC low-pass filter is employed for digital offset compensation. The actual current value i_{in} is measured via a shunt resistor and after filtering and adequate scaling passed to the current controller. PWM and current balancing circuits form a complete analog subsection as depicted in Section 4.1. Analog comparators are used for time critical safety shutdown like pulse-by-pulse current limiting.

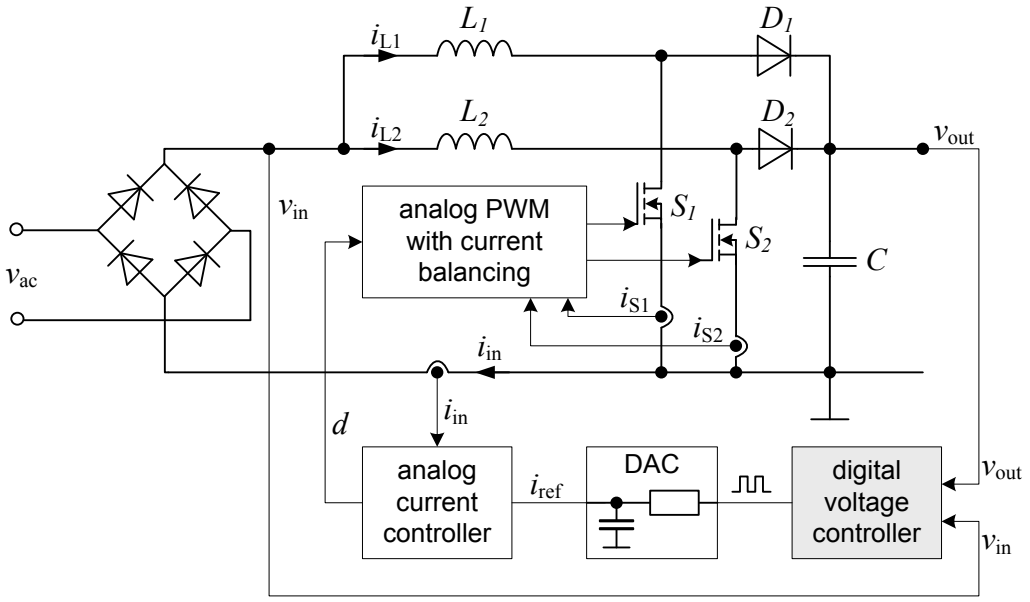

Figure 5.1: Semi-digital control structure for interleaved PFC rectifier

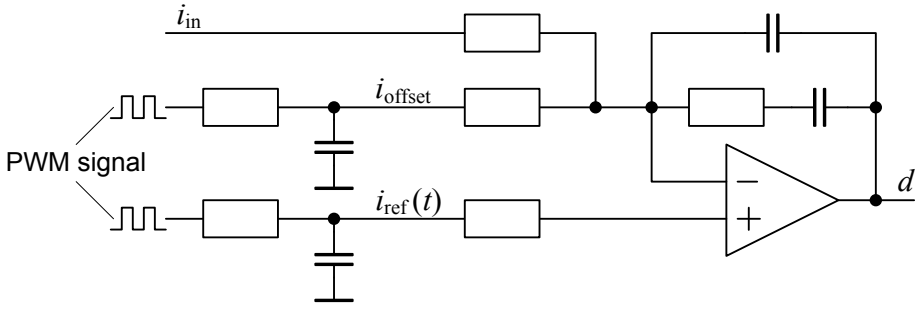

Figure 5.2: Scheme of the analog current controller with DAC

In Figure 5.1 the semi-digital control is depicted for an interleaved PFC rectifier with two converter rails, but it can easily be extended for multi-rail interleaved converters without the need of more computing power.

5.2 Digital Control Implementation

Along with the implementation of the voltage control loop, a multitude of additional functionality is feasible in digital. The structure of the digital control parts are shown in Figure 5.3. Particular functions are described in the following. Obviously, the presented functions can also be implemented in fully digital control structures.

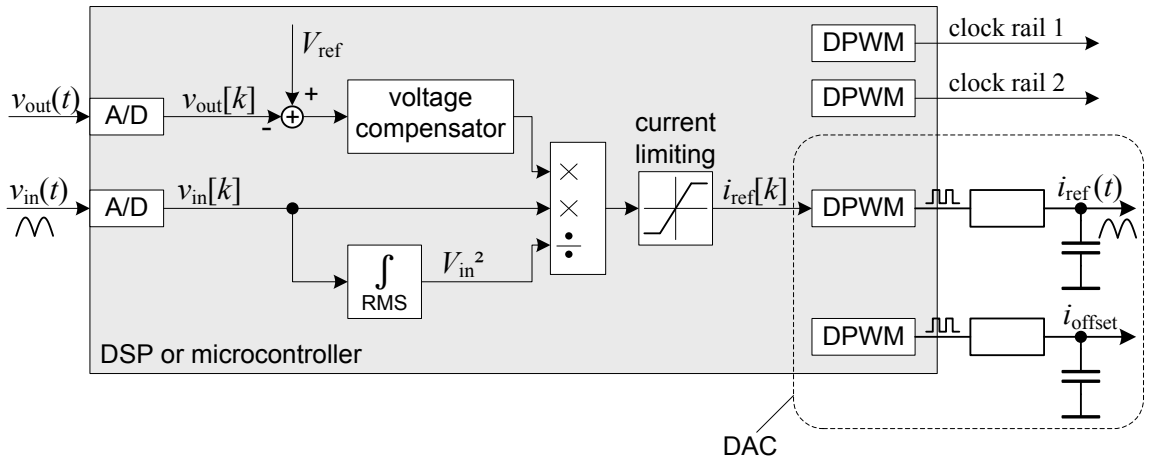

Figure 5.3: Block diagram of the digital control part with DAC

5.2.1 Voltage Control, Multiplier and Feed-Forward

The digital control tasks are computed in equally spaced time slices. A synchronization to the switching cycles is not necessary. Furthermore, the repetition frequency of the digital control tasks can be much lower than the converter switching frequency. In every cycle voltage control, multiplier and feed-forward compensation are computed.

The structure of the digital control parts is illustrated in Figure 5.3. By means of the control variable v_{out} and the nominal output voltage reference V_{ref} the offset v_{err} for the voltage control algorithm is calculated. The measured input voltage v_{in} is primarily needed to synthesize the sinusoidal input current reference i_{ref}. Therefore, typically the voltage regulator output, which is proportional to the current reference peak value, is multiplied by the normalized input voltage. Optionally, the digital implementation offers the possibility to utilize an artificial sinusoidal waveform for multiplying [Gro09]. In this case the measured input voltage is needed to detect zero crossing and line frequency. By using a sine table systematic phase errors caused by ADC, DAC, computational time, etc. can be compensated easily.

As described in Section 2.7, the line voltage RMS value V_{in} or the amplitude value $\hat{v}_{in}$ needs to be identified for the feed-forward compensation to achieve constant input power under fluctuation of the input voltage. The output value of the digital control part is the current reference value i_{ref} for the current controller, which is converted into a pulse width modulated signal.

Measured input voltage and current waveforms are shown in Figure 5.4. The input current replicates the line voltage waveform accurately. Only little disturbances after the zero-crossing are present, which are related to the analog current control loop. However, high power factors are achieved with the semi-digital control concept. The dynamic of the digital voltage control loop can be seen in Figure 5.5 during a load step transient response from 250W to 500W. The response time and the voltage overshoot are kept in an acceptable range and match the implemented controller dynamics.

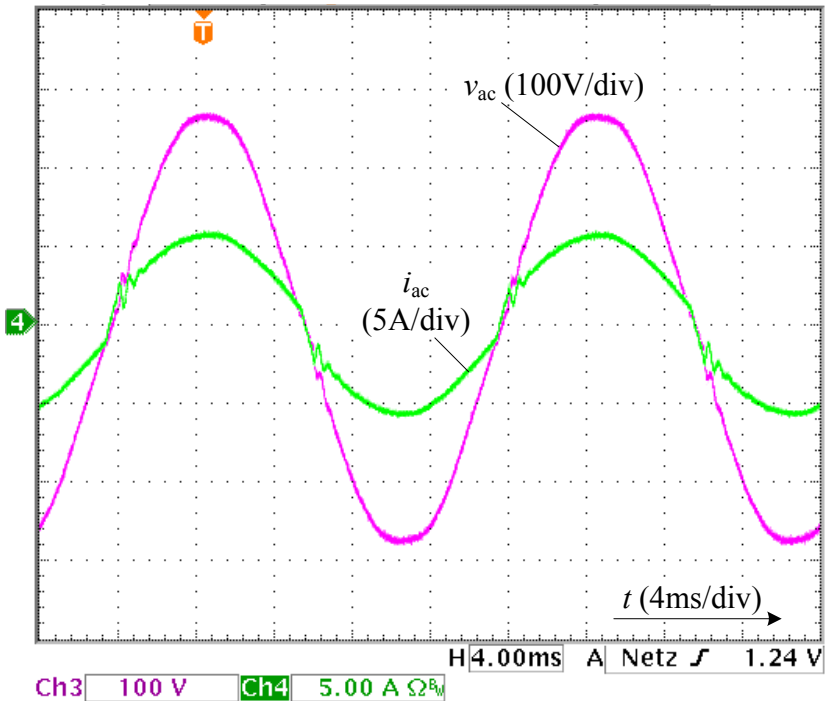

Figure 5.4: Line voltage and current waveform

5.2.2 PWM Clock

The clock signal for the analog PWM module is generated by the DPWM unit of the DSP or µC. Two DPWM channels are used in push-pull mode to generate two 180° phase shifted clock signals with half of the PWM frequency.

Because the PWM clock signal is generated in the digital control part, start and stop of the PFC operation can be controlled digitally. Furthermore, the switching frequency is kept adjustable.

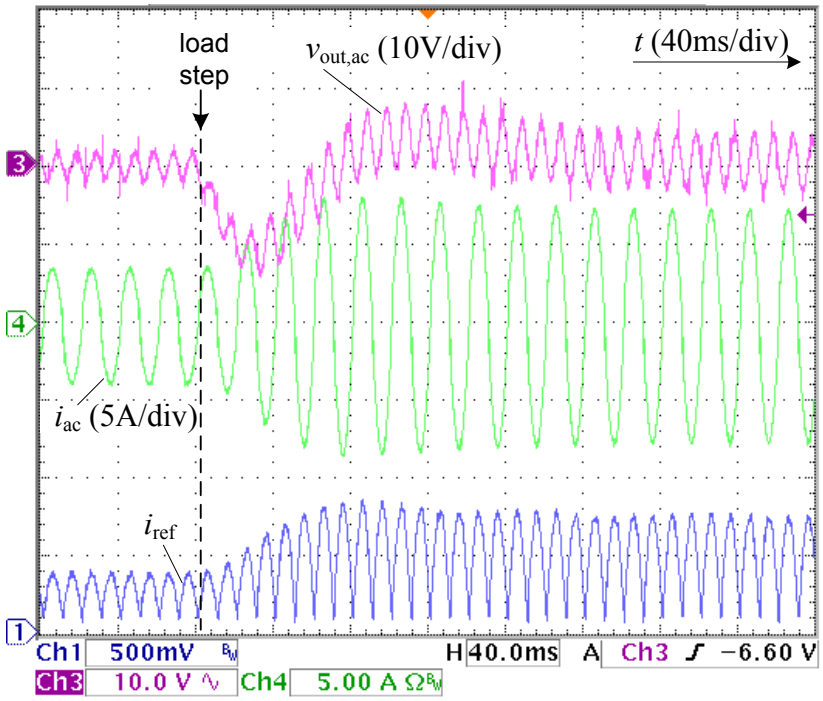

Figure 5.5: Transient response of the current reference after the DAC, the line current and the AC part of the output voltage during load change ($250\text{W} - 500\text{W}$*)*

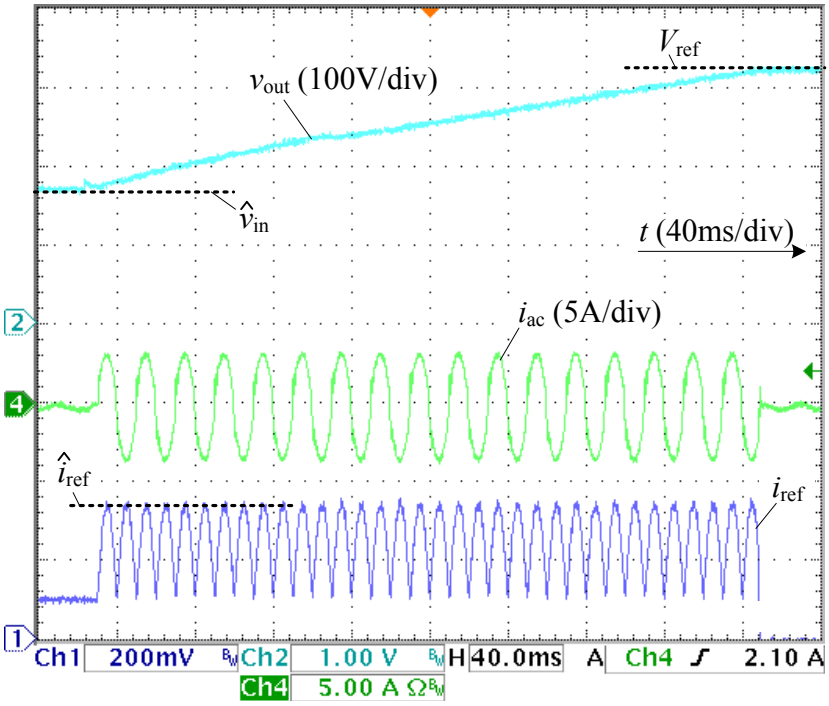

Figure 5.6: Current reference, line current and output voltage during soft start-up process

5.2.3 Soft Start-Up

At start-up the PFC output capacitor voltage has to be raised from the pre-charged level $\hat{v}_{in}$ to the nominal output voltage V_{ref}. In order to avoid high current surge, a soft start-up procedure needs to be implemented. To avoid a start-up current peak the soft-start process starts at zero crossing with multiplying a constant current reference peak value $\hat{\imath}_{ref}$ by the normalized input voltage. The result is the sinusoidal current reference value. It is passed via DAC to the analog current controller until the nominal output voltage is reached. After completing the soft-start procedure the program enters the repetitive loop with all control functions being activated. Waveforms of the analog reference current, the converter input current and the PFC output voltage during soft-start process are illustrated in Figure 5.6.

5.2.4 Power Management Features

A. Phase Shedding

One advantage of using paralleled converters is the potential to adjust the number of energized rails based on the load conditions. Thus it is possible to enhance the efficiency at light load conditions [Zum06, Wet06]. Switching between single-rail and interleaved operation occurs with hysteresis. For example one rail is switched off, if output power is below 40% of the rated power for a defined duration and switched on again when the output power exceeds 45%. While running in single rail mode, the energized rail can alternate between the converter rails in order to achieve equal thermal stress of all PFC components. This toggling can be performed without any disturbances at every line voltage zero crossing.

B. DC Link Voltage Reduction

In many applications the PFC output capacitor supports two functions: First filtering the inductor current and second providing energy in ‘hold-up’ case at line power failure (e.g. for one line period). However, since the stored energy depends on the output voltage, the output voltage can be reduced at light load. This measure leads to an improved efficiency of the PFC stage and the DC-DC stage at light load. Because the DC link voltage equals the semiconductor blocking voltage, the latter is strongly related to the switching losses of both stages. Hence, the losses decrease significantly with reduced voltage level.

C. Adaptive Switching Frequency

Another method to improve the efficiency is to reduce switching losses by an adaptive lowering of the switching frequency. This is feasible, if the PFC boost inductance is nonlinearly related to the actual current value. Hence, at lower current and therefore increased inductance the switching frequency can be reduced, while the current ripple is still kept within set limits. This circumstance can be utilized twofold, firstly within every sine half-cycle of the line current (cf. Figure 5.7) and secondly depending on the DC output current, which defines the line current amplitude (i.e. lower switching frequency at lower load).

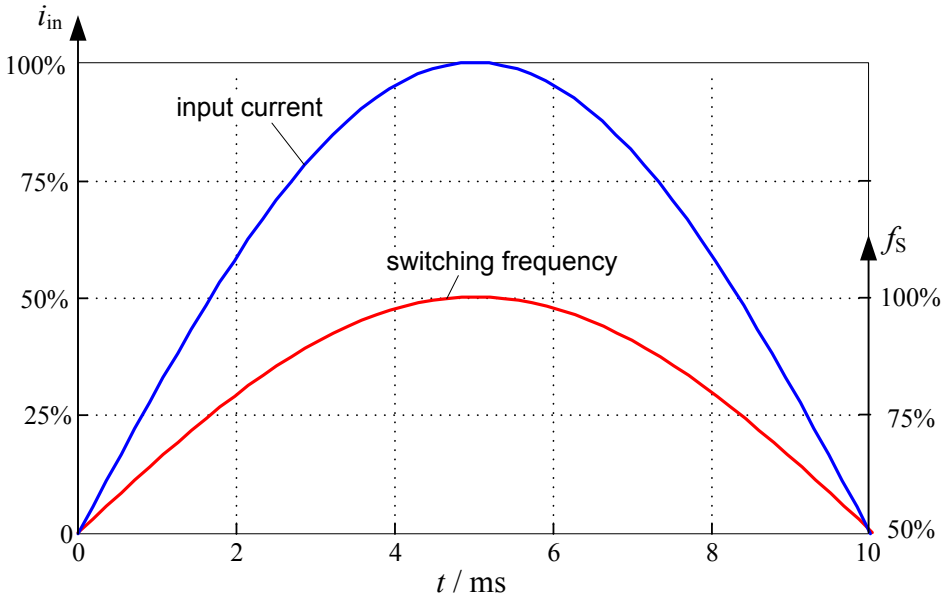

Figure 5.7: Switching frequency dependent on the instantaneous current value during line half-cycle

D. Zero Crossing Blanking

Yet another method to improve light load efficiency is to completely switch off the converter and operate it intermittently. This technique is commonly known as burst mode

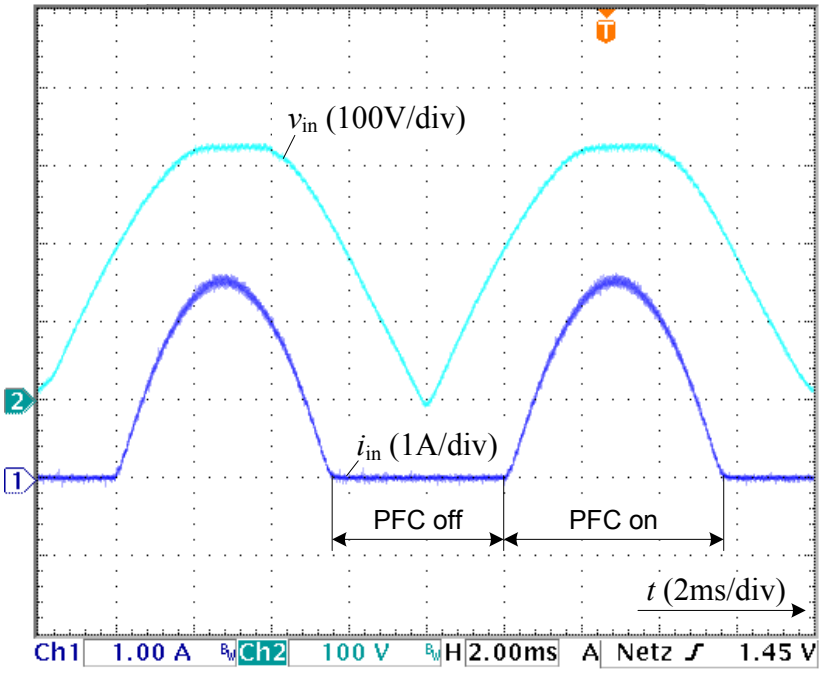

Figure 5.8: Rectified input voltage and average current waveform with zero crossing blanking

and can also be utilized in PFC applications [Zha11, Jan09]. For this purpose the PFC converter is kept off around the line voltage zero crossings and is activated for power processing near the line voltage amplitudes. This can be either done with enabling or disabling the drivers, which results in high current transients at the enable/disable instants [Zha11, Jan09]. Alternatively, a continuous current flow can be achieved, if still a sinusoidal reference current is applied only in the center of the line half-cycle. This process is shown in Figure 5.8. With this technique the light load efficiency is increased by slightly decreasing the power factor.

E. Adaptive Current Limiting

In order to avoid overstressing of the devices the current needs to be limited. However, in some applications for short-term duration an overcurrent up to 125% of $i_{100\%}$ is required (cf. Figure 5.9). This feature also can be realized in the digital part of the control structure. Therefore an algorithm is implemented which allows intermediate overcurrent considering the past load conditions of the converter. Contrary, no overcurrent is allowed, when the power supply is stationary running at full load.

Assuming that the current loop works correctly, the current reference value is used for the algorithm, thus there is no need to convert the actual current value into the digital world. Figure 5.9 illustrates the current limiting process from 20% and 80% initial load.

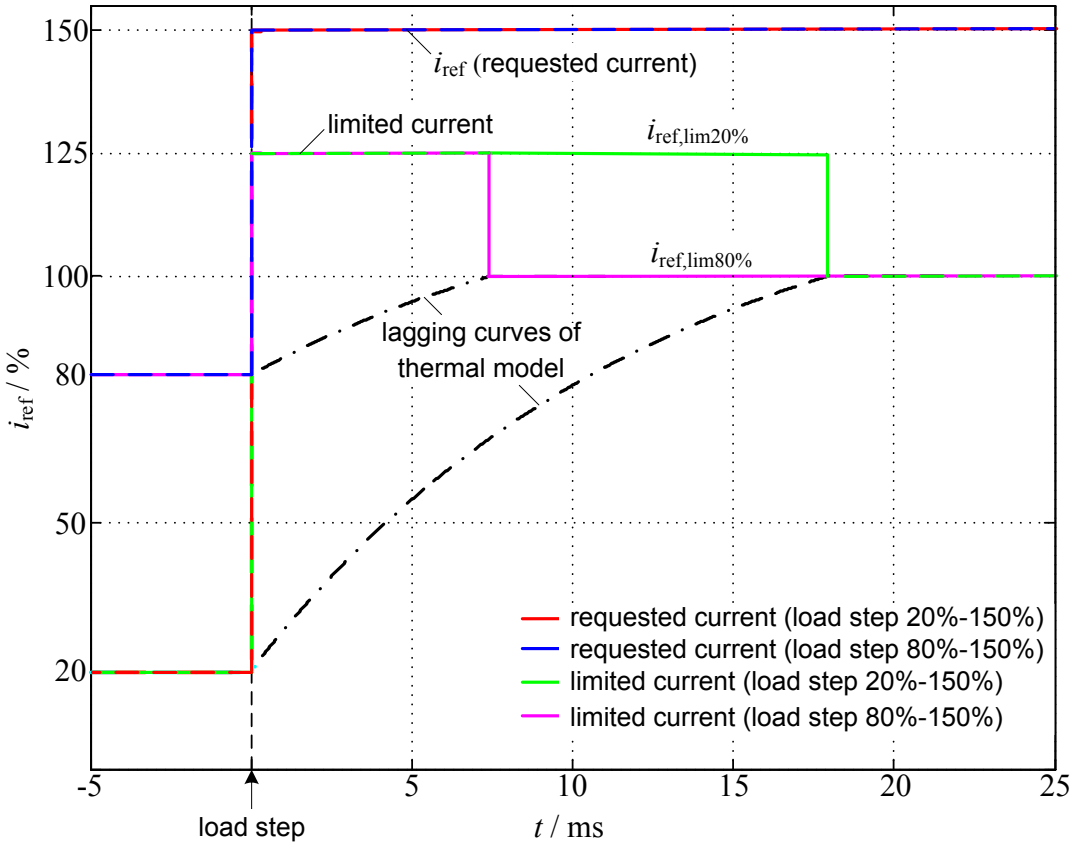

Figure 5.9: Current limiting after load step from 20% and 80% initial load into over load

5.3 Summary

Digital control offers potential for applying advanced algorithms to enhance the control performance. However, it is not essential to implement a full digital control structure to achieve high flexibility. It is possible to achieve almost the same performance when only realizing the low bandwidth voltage control in a digital manner. By retaining the relative fast control functions in analog technique, high control dynamic is ensured without the need of high computing power, which decreases DSP or μC costs significantly. By replacing the multitude of analog components by DSP or μC the required PCB space for PFC control is reduced considerable.

The semi-digital control can easily be extended from single-rail to multi-rail interleaved converters without the need of more computing power. Also a multitude of power management features can be implemented in the digital part of the semi-digital control structure with little effort. With capable measures the efficiency of the converter can be improved especially at light load.

Some functions like soft-start or inrush current limiting are only used during start-up but nevertheless require PCB space, if realized by analog components. Those functions are well suited for sequential DSP or μC processing, because they can be added without any extra costs and without losing any performance.

6 Digital Peak-Current Mode Control for PFC Rectifiers

Since some DSPs and μCs contain analog comparators an implementation of peak current control becomes feasible. For such a digital peak current mode control the realization of the required slope compensation in a digital manner is derived in this chapter. In order to achieve the sinusoidal shape for the average inductor currents in PFC applications different extensions of the control structure are proposed.

6.1 Control Structure with On-Chip Comparators

Peak current mode control was already described in Section 2.4.2. Due to the fact that analog comparators are used predominantly for this purpose, mostly the whole control structure is kept analog. However, with available DSPs and μCs including analog on-chip comparators and dedicated DACs at the internal input, a digital peak current control is basically feasible by utilizing a simple component (cf. Figure 6.1). By combining the advantages of peak current control with the benefits from digital control, a promising control method arises.

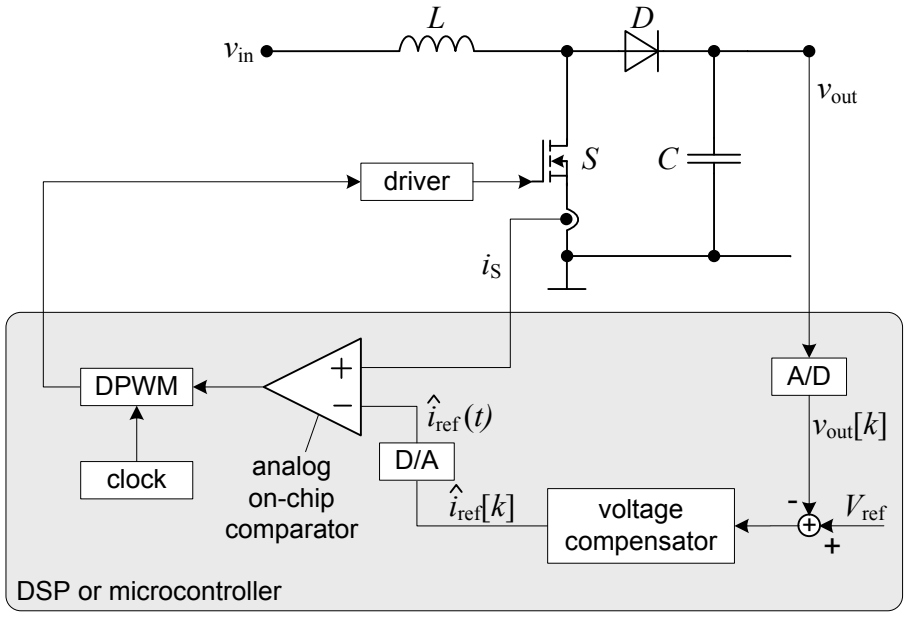

Figure 6.1: Digital implementation of peak current control utilizing on-chip comparator

The on-chip comparator is a common analog comparator with two analog inputs and one digital output. One input is connected to an external pin and the other input is connected to an internal DAC. A discrete threshold value can be set by software. The DAC converts this

discrete value into an analog voltage representing the peak current threshold level for the comparator. The comparator output is internally connected to the DPWM unit and is used to switch off the DPWM channel, if the threshold level is reached. The DPWM channel is switched on at the beginning of each new DPWM cycle. A preset maximum on-time limits the duty-ratio.

The current can be sensed either in the inductor or in the switch path and is directly passed to the comparator. Because no current has to be sampled and no code has to be executed to compute a duty-ratio, the introduced dead time is minimized for the current control loop.

6.2 Digital Slope Compensation

The basic functionality of peak current mode can be implemented in a digital way with little effort. But in order to eliminate the drawbacks of peak current control, slope compensation needs to be added. All slope compensation techniques described in Section 2.4.2 base on analog circuitry implementations. Thus, an obvious solution could be to let the slope compensation remain in analog technique and add a ramp to the inductor current signal. However, with using such an approach no benefits in terms of complexity and adaptivity can be achieved. A solution for a digital implementation of the ramp compensation could be realized by permanently decrementing the discrete threshold value within every switching cycle with minimal possible step size. But this appears to be impractically using a reasonable DSP or µC.

Hence, the task arises to propose a concept of digital slope compensation without using a ramp. Instead, the desired threshold level with integrated amount of compensation is pre-calculated by means of the valley current i_n, i.e. the inductor current $i_{L,min}$ at the beginning of the cycle n [GrSc09]. As indicated in Figure 6.2, the current threshold level i_{cmp} can be expressed as

$$i_{cmp} = i_n + m_1 dT_s \tag{6.1}$$

and

$$i_{cmp} = i_{ref} - m_{sc} dT_s. \tag{6.2}$$

From Eq. (6.1) and Eq. (6.2) it follows

$$dT_s = \frac{i_{ref} - i_n}{m_1 + m_{sc}}. \tag{6.3}$$

Using Eq. (6.3) to eliminate DT_s from Eq. (6.2) it results

$$i_{cmp} = i_{ref} - m_{sc} \frac{i_{ref} - i_n}{m_1 + m_{sc}}. \tag{6.4}$$

At this point a compensation factor k_{sc} is introduced as

$$k_{sc} = \frac{m_{sc}}{m_1}. \tag{6.5}$$

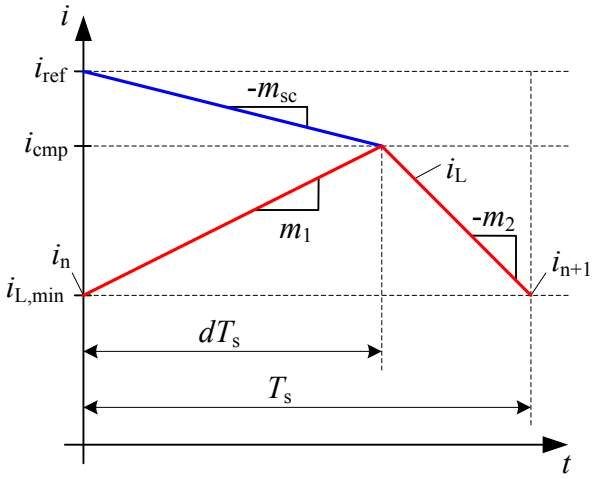

Figure 6.2: Inductor current characteristics to illustrate principle of digital slope compensation

Thus, Eq. (6.4) can be expressed as

$$i_{cmp} = i_{ref} - \frac{k_{sc}}{1 + k_{sc}} \left(i_{ref} - i_n\right) \text{ or } i_{cmp} = \frac{1}{1 + k_{sc}} \left(i_{ref} + k_{sc} i_n\right). \tag{6.6}$$

Hence, the required current threshold level for the comparator can be computed by the current reference value i_{ref} and the valley current value i_n. The current reference i_{ref} is obtained from the voltage controller and the valley current i_n has to be sampled every switching-on event and passed via ADC to the digital control.

Hence, the proposed digital slope compensation algorithm does not require any knowledge of the inductance value or other circuit parameters.

In order to fit the computed threshold value with adequate slope compensation, a proper value for the compensation factor k_{sc} has to be chosen. In Section 2.4.2 the conditions for a stable operation were already presented. From Table 2.1 the minimum desired values to avoid subharmonic oscillations and values for optimum slope compensation for the basic converters are extracted, in order to determine the corresponding values for k_{sc}. These characteristic values are summarized in Table 6.1. It must be considered, that k_{sc} has to be limited to positive values.

The desired compensation only depends on the input and output voltage. In PFC applications these values are measured anyway and therefore can easily be used to implement an algorithm for an adaptive compensation factor. Consequently, a desired dynamic over a wide range of operation can be guaranteed. This is advantageous in PFC

applications, where the input voltage varies continuously. Furthermore, the amount of the compensation can be adjusted according to requirements with a compensation gain $\gamma \geq 0.5$. For the considered boost converter it results

$$k_{sc} = \frac{\gamma\, v_{out} - v_{in}}{v_{in}}. \tag{6.7}$$

	min. k_{sc}	optimum k_{sc}
buck	$\frac{v_{out} - 0.5v_{in}}{v_{in} - v_{out}}$	$\frac{v_{out}}{v_{in} - v_{out}}$
boost	$\frac{0.5v_{out} - v_{in}}{v_{in}}$	$\frac{v_{out} - v_{in}}{v_{in}}$
buck-boost	$\frac{0.5(\, v_{out} - v_{in})}{v_{in}}$	$\frac{v_{out}}{v_{in}}$

Table 6.1: Compensation factor for minimum required and optimum slope compensation for basic converters

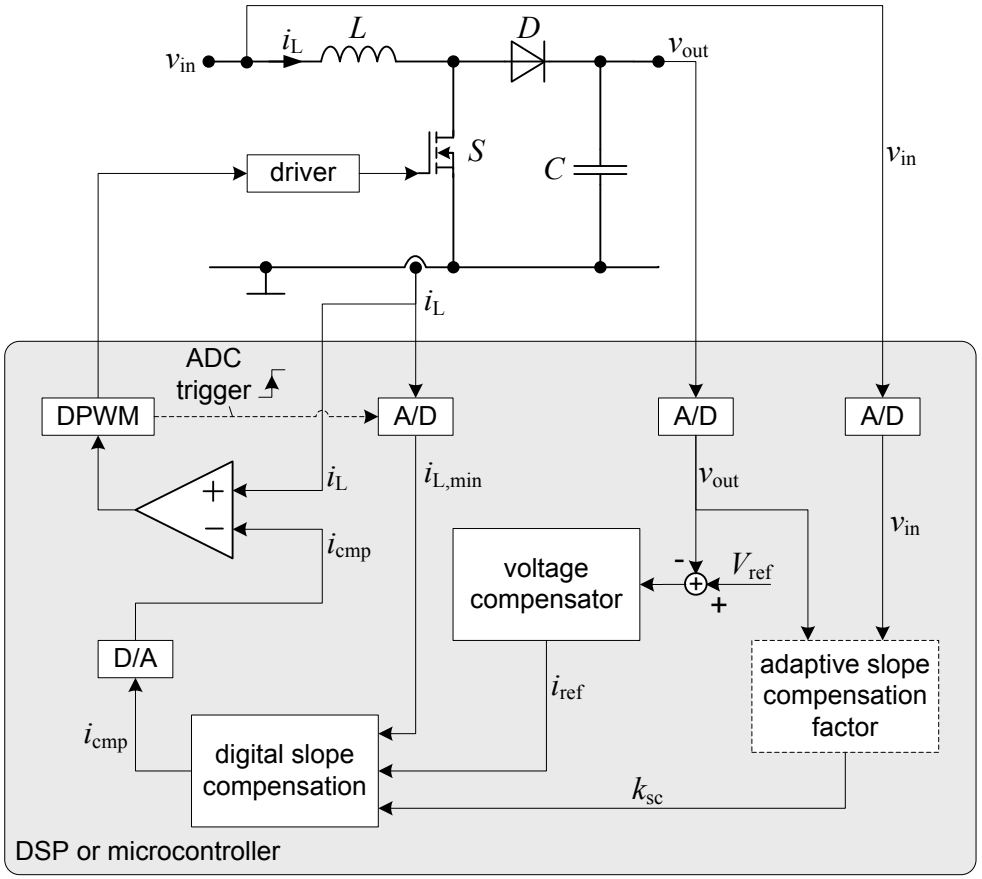

Figure 6.3: Scheme of the peak current control with digital slope compensation for a boost converter

With $\gamma = 0.5$ the minimum required compensation can be applied and with $\gamma = 1$ optimum compensation for dead-beat control is achieved. If values $\gamma > 1$ are applied, the settling of the inductor current takes several cycles without overshoot.

The block diagram of the digital peak current control implementation on a DSP or µC including digital slope compensation is illustrated in Figure 6.3. Computation of an adaptive compensation factor is an option and can be replaced by a constant value, if no adaptivity is required.

The following simulation results illustrate the effectiveness of the digital slope compensation. In order to verify the comparability with an analog compensation ramp, the equivalent conventional slope compensation is depicted, too.

Figure 6.4 shows the inductor current under steady state conditions with conventional compensation ramp and with digital slope compensation. As can be seen, there is no difference in the resulting current shapes.

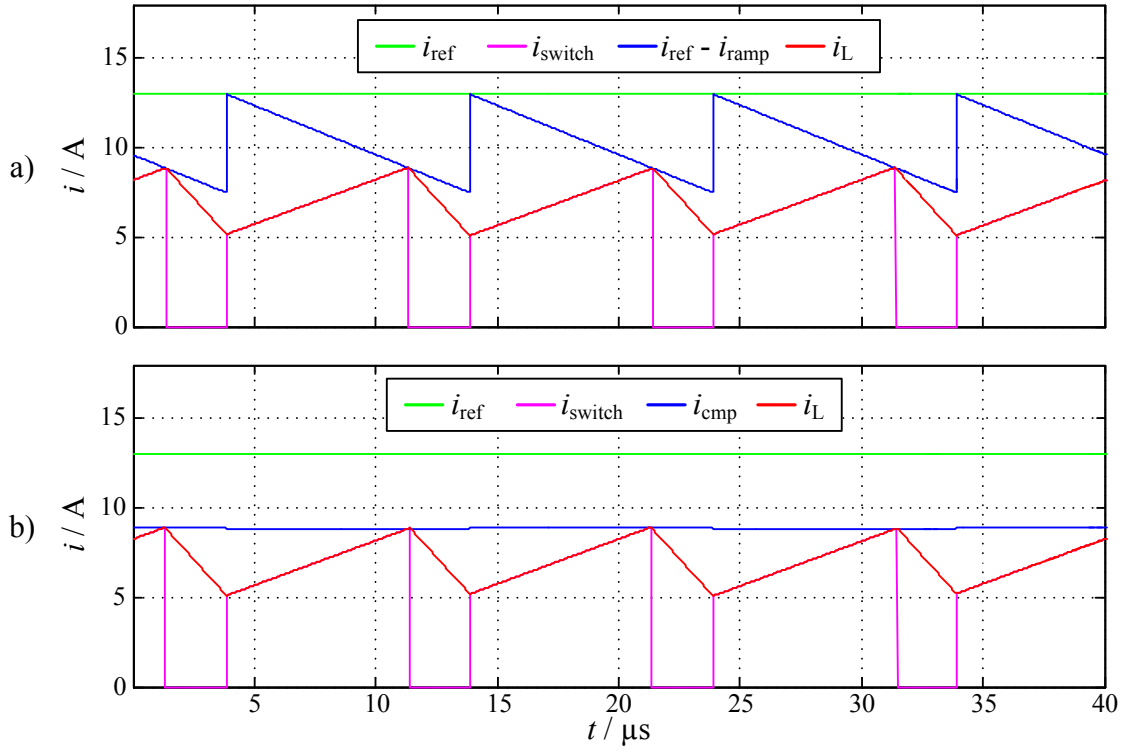

Figure 6.4: Simulation results of peak current control with slope compensation under steady state conditions ($d = 0.82$, $k_{sc} = 1.8$)
a) with conventional compensation ramp
b) with computed current threshold level

Figure 6.5 and Figure 6.6 illustrate the response of the peak current control to a simulated perturbation of the inductor current. In Figure 6.5 a small compensation factor close to the minimum required compensation was used, so that settling of the inductor current takes several cycles. When applying the optimum slope compensation, the settling of the inductor current occurs within one cycle, i.e. dead-beat control (cf. Figure 6.6).

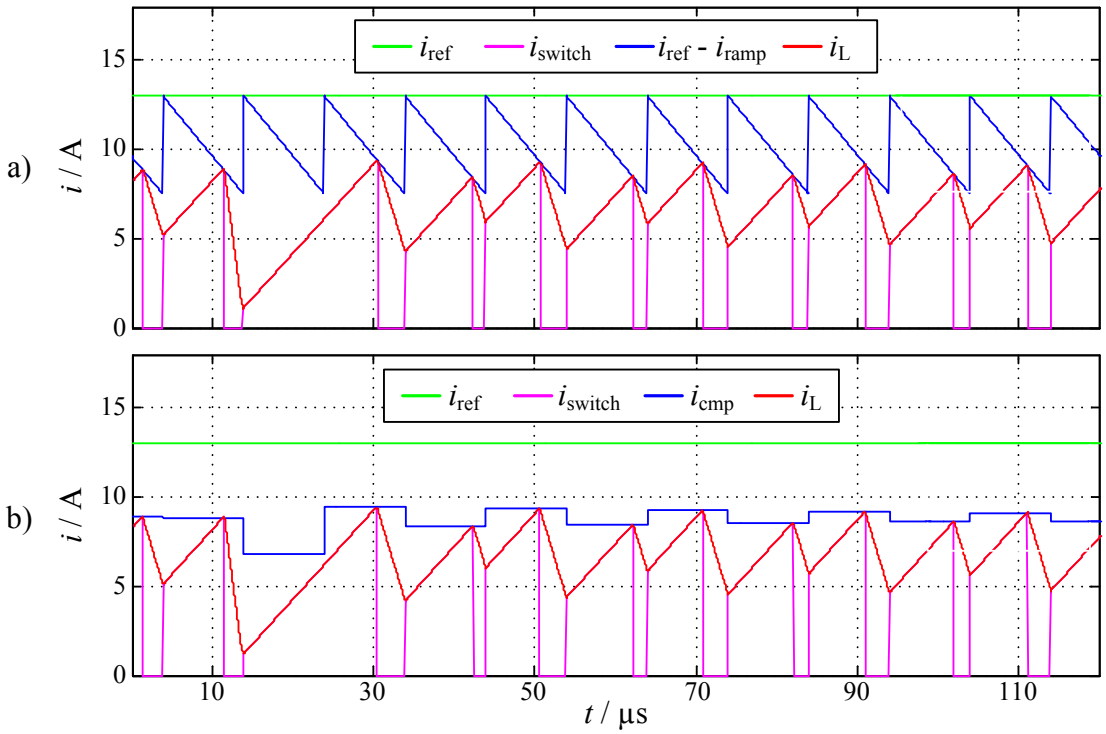

Figure 6.5: Simulation results with perturbed inductor current
a) with conventional compensation ramp
b) with computed current threshold level

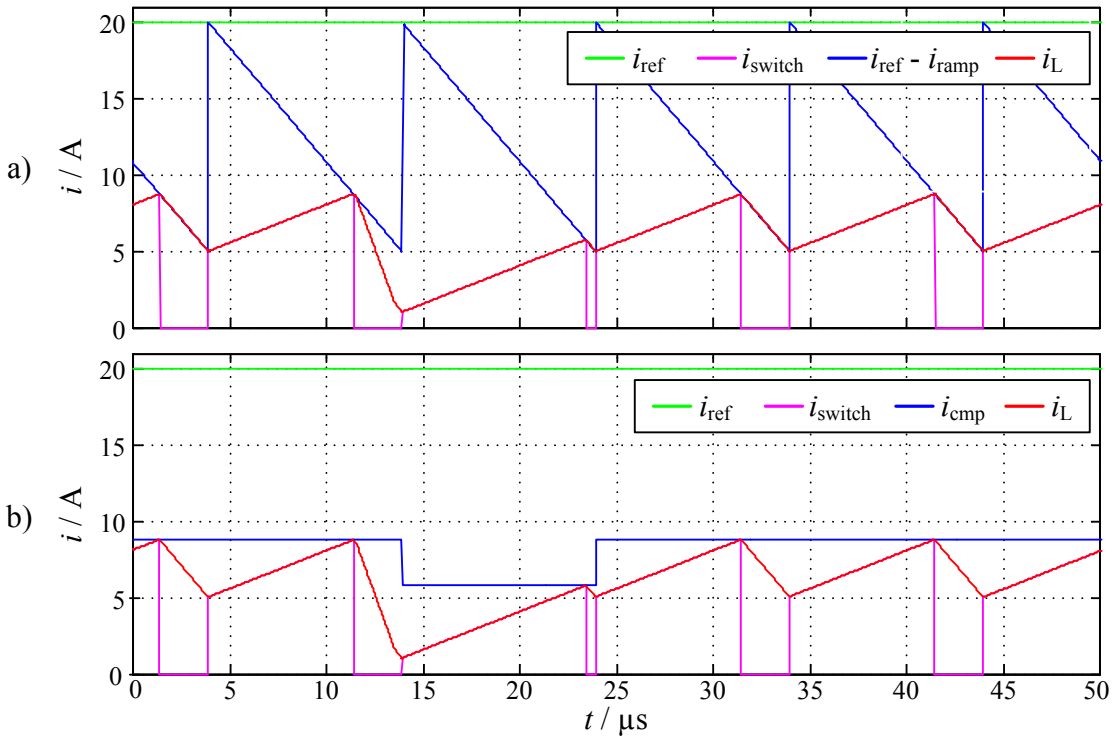

Figure 6.6: Simulation results with perturbed inductor current and optimum k_{sc} value
a) with conventional compensation ramp
b) with computed current threshold level

The practical capability of the proposed peak current control concept is illustrated in Figure 6.7 and Figure 6.8. The transient response of a current reference step with an implemented slope factor slightly above the minimum required value is shown in Figure 6.7 for a step-up and in Figure 6.8 for a step-down. This confirms the high dynamic performance and robustness of the peak current control method with applied digital slope compensation.

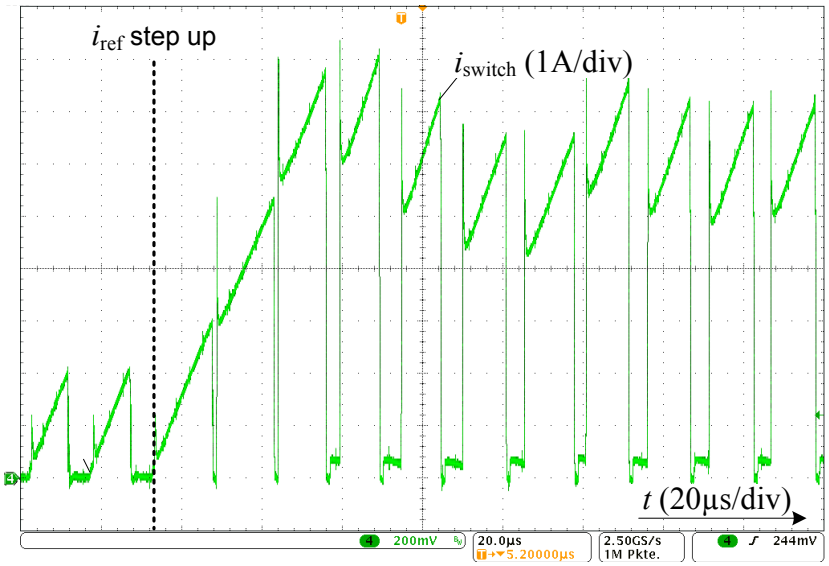

Figure 6.7: Transient response for a step-up in the current reference

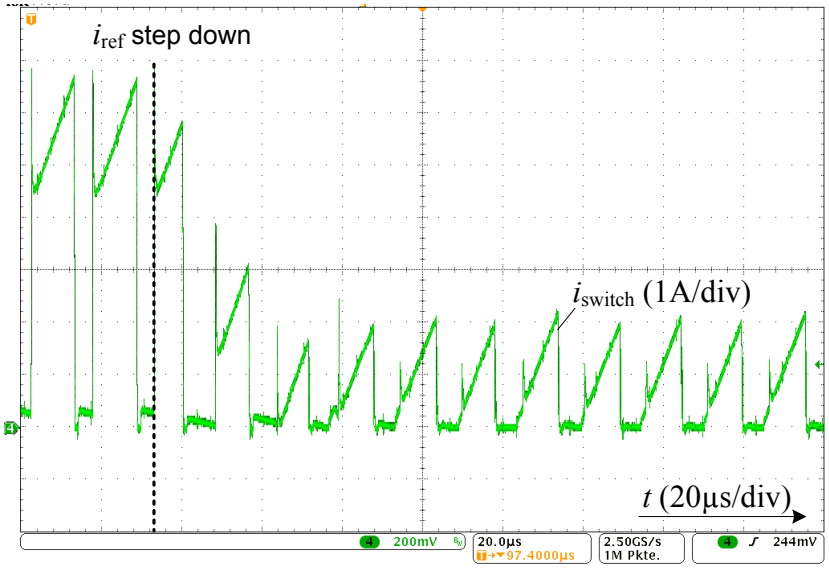

Figure 6.8: Transient response for a step-down in the current reference

6.3 Special Effects and Measures for Reliable Operation

6.3.1 How to Handle the Reverse Recovery Current

Because of the DC component, measuring the inductor current requires costly current sensors. For this reason the current is measured in the switch path in most applications. In this case a simple current transformer, which can demagnetize during every switch-off time, can be utilized.

Due to the reverse recovery effect of silicon diodes used in boost circuits, a current spike appears in the switch path at the beginning of each new cycle (cf. Figure 6.9). Consequently, the minimum inductor current cannot be sampled instantaneously at turn-on. However, with a short delay, until the reverse recovery process is completed, the current can be sampled and utilized for the slope compensation algorithm (cf. Figure 6.9). One restriction is that the sampling must be performed during the switch-on time, but this is feasible in common PFC application.

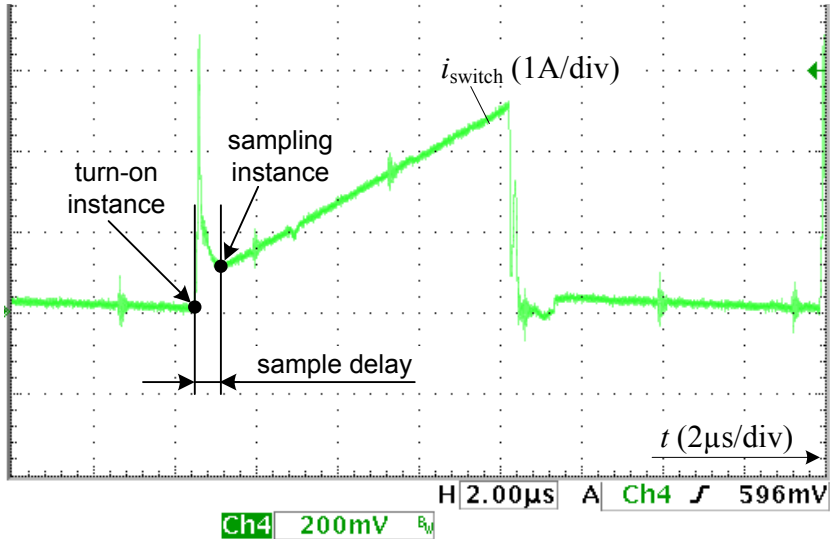

Figure 6.9: Switch current with current spike and delayed sampling instance

The sample delay T_{sd} has no influence on the stability and the dynamic of the peak current mode. This fact is depicted in Figure 6.10 with an extreme delay. The analog equivalent to the sample delay is delaying the start of the compensation ramp. The slope of the ramp remains constant and consequently the dynamic. However, a variation of $\Delta i_{L,min}$ in the inductor current occurs due to the sample delay:

$$\Delta i_{L,min} = m_{sc} T_{sd} \tag{6.8}$$

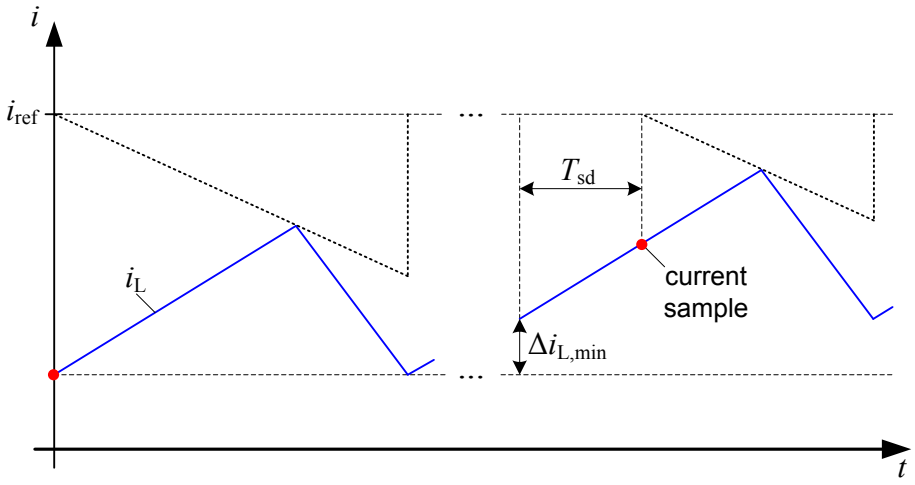

Figure 6.10: Influence on the inductor current due to delayed current sampling

Another problem also caused by the reverse recovery current is that a high current spike can exceed the comparator turn-off threshold and force a faulty trigger of the comparator. This leads to erratic subharmonic oscillations as indicated in Figure 6.11. In order to avoid this effect a leading edge blanking can be implemented in software by deactivating the comparator during the reverse recovery process. Also an analog implementation of the leading edge blanking is feasible by applying a low-pass filter.

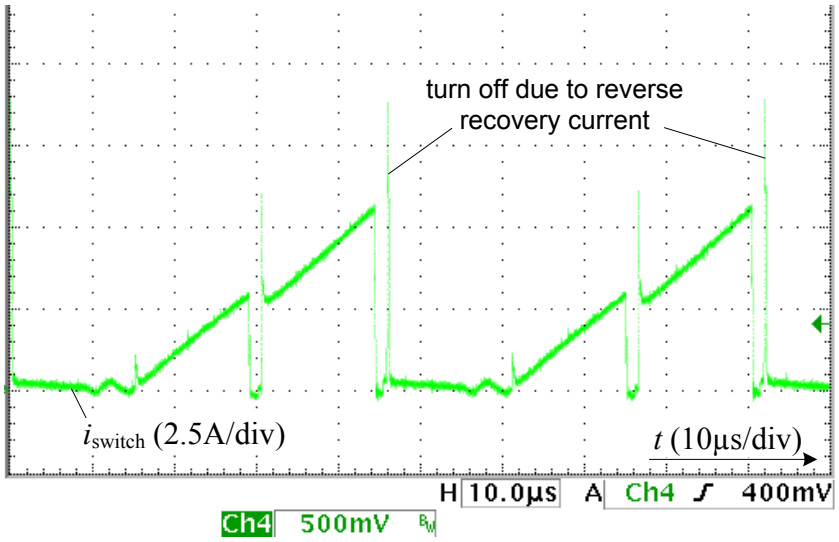

Figure 6.11: Subharmonic oscillation due to faulty activation at reverse recovery current spike

6.3.2 Timing

Another reason for an unreliable operation in practice is the delay due to the computing time. If the current reaches the old threshold value calculated in the previous cycle before the new threshold value is updated, a premature turn-off occurs. This can also result in

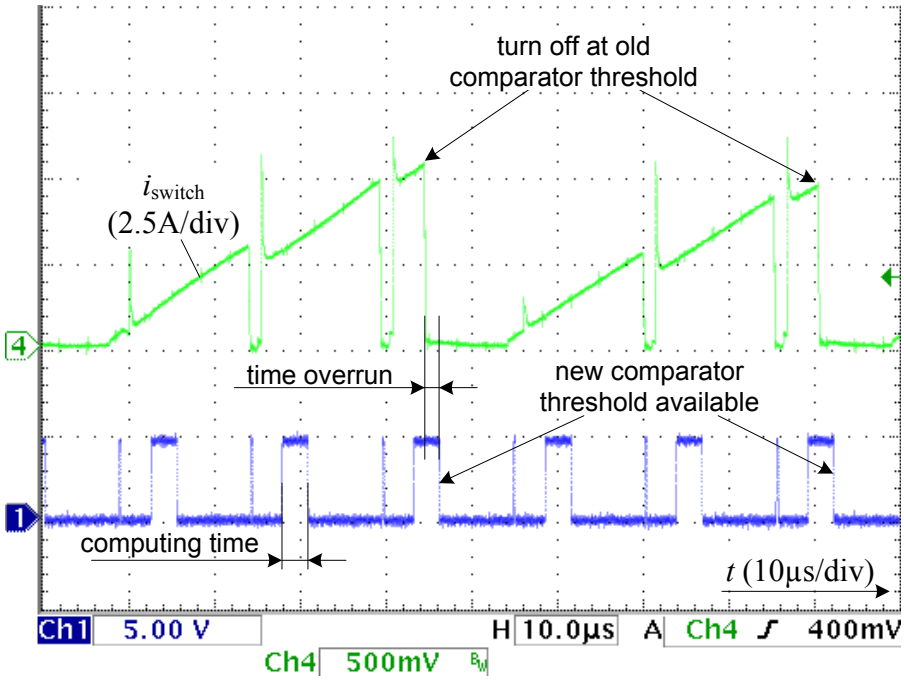

Figure 6.12: Subharmonic oscillation due to turn-off at comparator threshold value of previous cycle

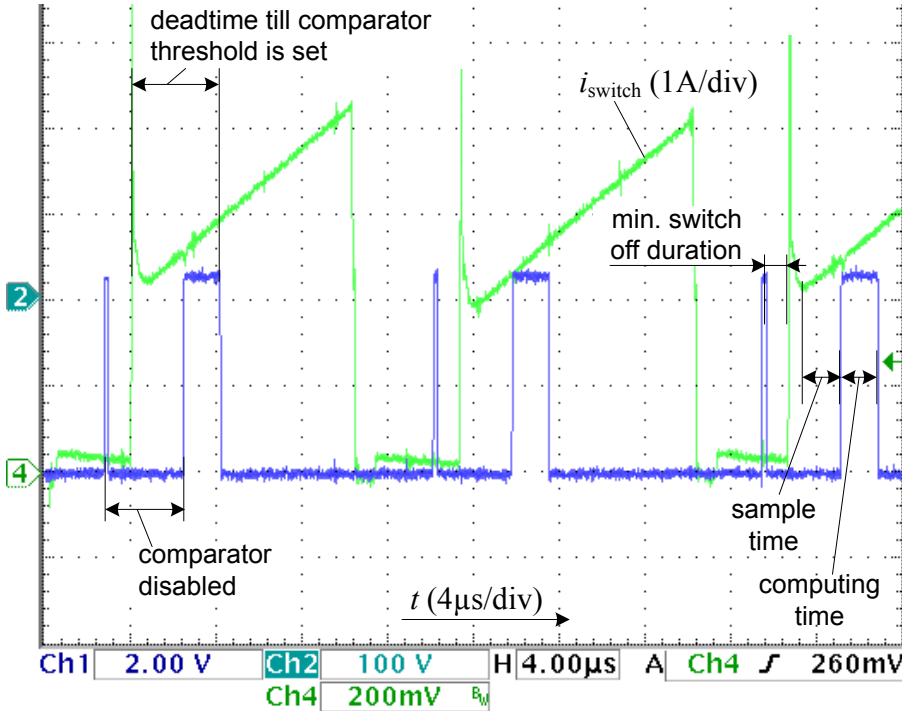

Figure 6.13: Time flow within the switching cycles

undesired subharmonic oscillation (cf. Figure 6.12). To avoid such accidental trigger of the comparator, the threshold value is set to the maximum valid value before each cycle until the computation of the new threshold value is finished. In order to minimize the resulting

dead time, the comparator threshold value is computed firstly in the interrupt routine. Thus, the threshold value is computed with the k_{sc} value of the previous cycle. However, this is not essential as k_{sc} only depends on the relative slowly varying voltage values (cf. Table 6.1).
Considering the mentioned practical aspects, the timing shown in Figure 6.13 results. With this implementation the control loop operates up to high duty-ratio values without subharmonic oscillation.

6.4 Digital Peak Current Control for PFC Application

In order to achieve a high power factor the average value of the input current must have the same sinusoidal shape like the input voltage. For this reason average current control is the obvious and most utilized control method in PFC applications. With peak current control there is no steady link to the average current, especially with additional slope compensation. However, peak current control offers a couple of advantageous like high dynamic and inherent overcurrent protection.

Since recently digital implementation of peak current control and slope compensation became feasible, novel opportunities arise to apply peak current control in PFC applications. Sophisticated and adaptive algorithms can be developed to achieve high power factors [Sch11].

It can be shown that primarily the inductor current ripple and the slope compensation cause the difference between the reference current i_{ref} and the average current i_{avg}. Furthermore, the influence of these factors changes with the duty-ratio. Consequently, with a sinusoidal reference current a non sinusoidal average current results.

In order to achieve high power factors with reasonable computational effort, four feasible implementations are presented in this contribution:

- Applying a constant compensation factor
- Applying the equivalent to a constant compensation ramp
- Applying a feed-forward algorithm
- Applying an outer average current controller

For the simulation results presented in the next sections the parameters listed in Table 6.2 were utilized.

Output voltage	$V_{out} = 400\text{V}$
Inductance value	$L = 470\mu\text{H}$
Sample delay	$T_{sd} = 1\mu\text{s}$

Table 6.2: Parameters utilized for the simulations

6.4.1 Constant Compensation Factor

In the first method a constant compensation factor k_{sc} is applied. This version will in fact not provide the best power factor. However, it represents the version with minimum computational requirements. The control structure is illustrated in Figure 6.14. The outer voltage controller determines the amplitude of the current reference $\hat{\imath}_{ref}$. This value is multiplied by the normalized input voltage $v_{in}/\hat{v}_{in}$. The resulting sinusoidal current reference i_{ref} as well as the sampled valley current $i_{L,min}$ and the constant compensation factor k_{sc} are utilized to compute the comparator threshold level i_{cmp} with Eq. (6.6).

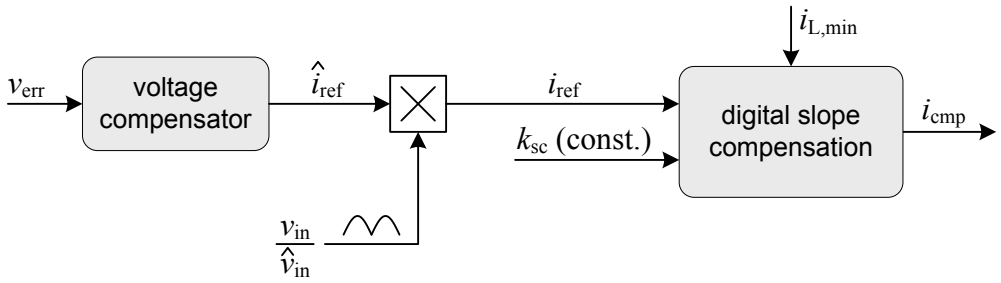

Figure 6.14: Control structure with constant compensation factor k_{sc}

A constant k_{sc} must not be compared with a constant ramp slope. Rather the equivalent slope

$$m_{sc} = k_{sc}\, m_1 = \frac{k_{sc}\, v_{in}}{L} \tag{6.9}$$

decreases at low input voltage. Due to this characteristic relative high values for k_{sc} needs to be chosen. However, higher k_{sc} values increase the deviation between the sinusoidal reference current i_{ref} and the average inductor current $\bar{i}_L$ and thereby impairs the power factor. Hence, a compromise must be found between high power factor and avoiding subharmonic oscillation. The following simulation results exemplify this characteristic.

Figure 6.15 shows the situation at low line voltage with an RMS input current of $I_{ac,ref} = 4\text{A}$ for two different values of k_{sc}. Due to the slope compensation and the inductor current ripple the voltage controller needs to increase the reference value $\hat{\imath}_{ref}$ to achieve the desired input current $I_{ac,ref}$. In Figure 6.15 a) the constant slope compensation factor of $k_{sc} = 1.5$ is not sufficient for the small input voltage after and before the line voltage zero crossing. Consequently, subharmonic oscillation occurs. With a higher value $k_{sc} = 3$ in Figure 6.15 b) subharmonic oscillation is eliminated completely. However, the shape of the average input current differs more from the sinusoidal shape with the larger compensation factor. The identified power factor degrades, accordingly.

At high line voltage smaller values of the compensation factor suffices (cf. Figure 6.16). Only at very low input voltage in the region of the line voltage zero crossing higher

compensation factors would be necessary theoretically. But typically the converter operates in DCM in this region, where no slope compensation is required.

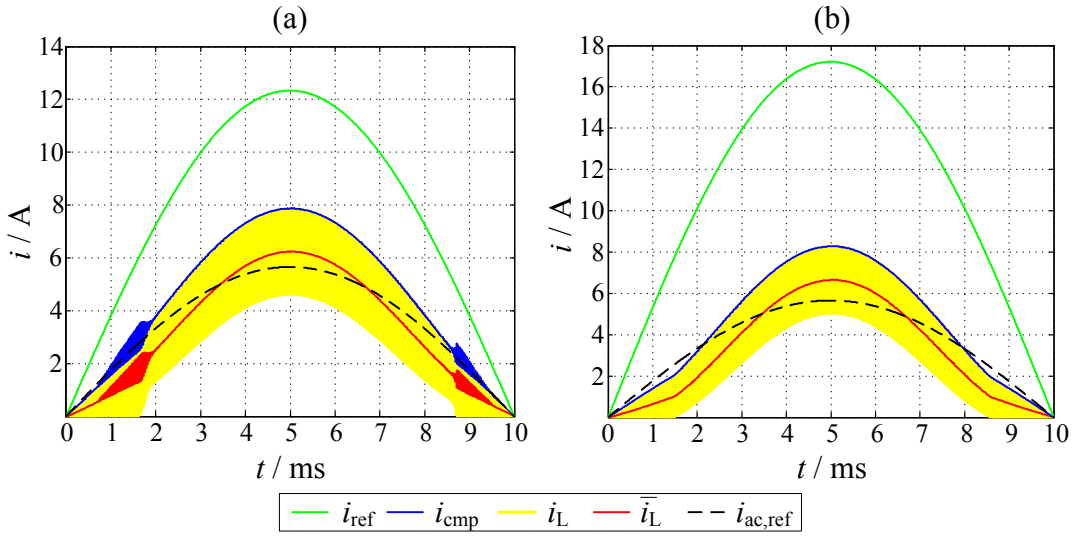

Figure 6.15: Current shapes with const. k_{sc} at $V_{ac} = 115\text{V}$
a) $I_{ac,ref} = 4\text{A};\ k_{sc} = 1.5;\ PF = 99.00\%$;
b) $I_{ac,ref} = 4\text{A};\ k_{sc} = 3;\ PF = 97.45\%$

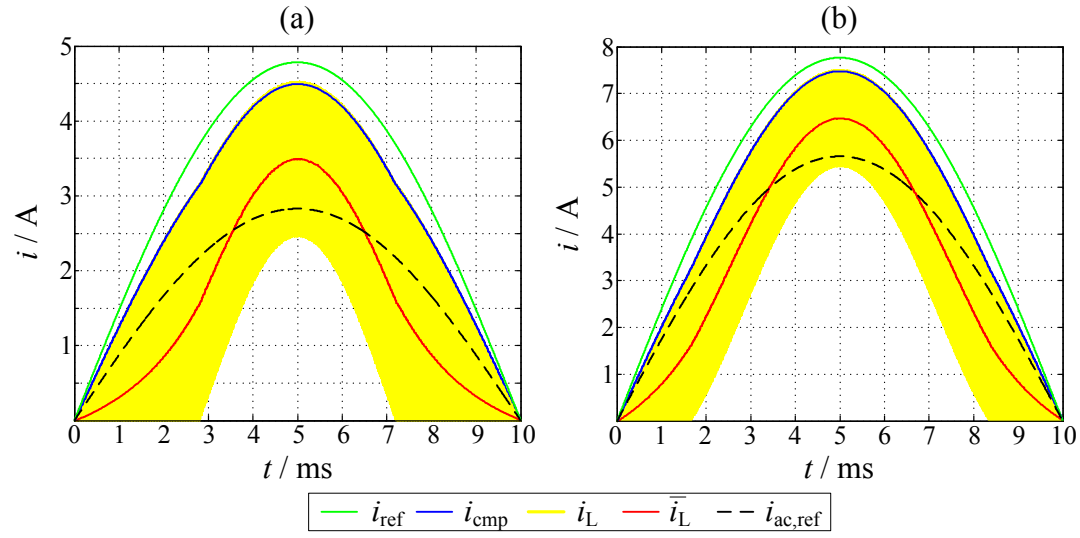

Figure 6.16: Current shapes with const. k_{sc} at $V_{ac} = 230\text{V}$
a) $I_{ac,ref} = 2\text{A};\ k_{sc} = 0.2;\ PF = 96.24\%$;
b) $I_{ac,ref} = 4\text{A};\ k_{sc} = 0.2;\ PF = 98.33\%$

Also the utilization of an adaptive compensation factor is possible to avoid subharmonic oscillations under all conditions. However, this would not naturally increase the power factor. Furthermore, the computational effort would increase.

6.4.2 Constant Compensation Ramp

Now a constant slope value m_{sc} is applied. This represents the equivalent to analog implementations with constant compensation ramp. Because of the algorithm for digital slope compensation, the compensation factor k_{sc} has to be computed with

$$k_{sc} = \frac{m_{sc}\, L}{v_{in}}. \tag{6.10}$$

In order to apply only a single factor and to utilize the normalized input voltage, the factor

$$k_r = \frac{m_{sc}\, L}{\hat{v}_{in}} \tag{6.11}$$

is introduced. The resulting control structure is given in Figure 6.17. The additional division increases the computational effort significantly.

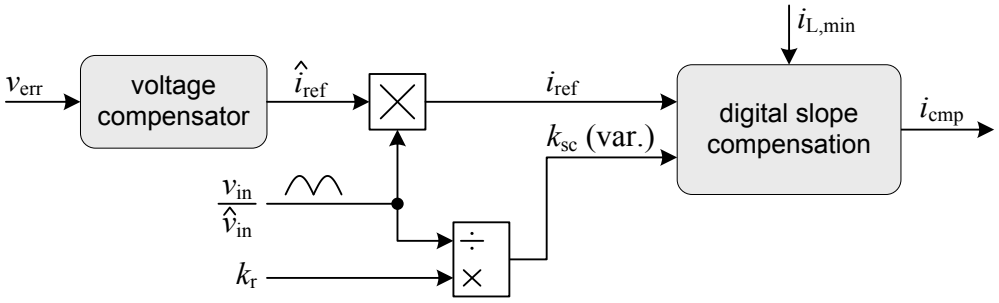

Figure 6.17: Control structure with constant compensation slope m_{sc}

The drawbacks of the constant k_{sc} method are still present, even though the negative effects on the power factor are moderated. This is illustrated by the simulation results.

Figure 6.18 illustrates the situation at low line voltage. Similar to the constant k_{sc} method the factor k_r can be slightly reduced at smaller input currents without causing subharmonic oscillation. Again this is because of the wider DCM range where no slope compensation is required. Also at high line voltage the DCM operation is beneficial for applying a smaller compensation (cf. Figure 6.19). Due to this effect even no slope compensation is necessary below a certain input current value (cf. Figure 6.19 a)).

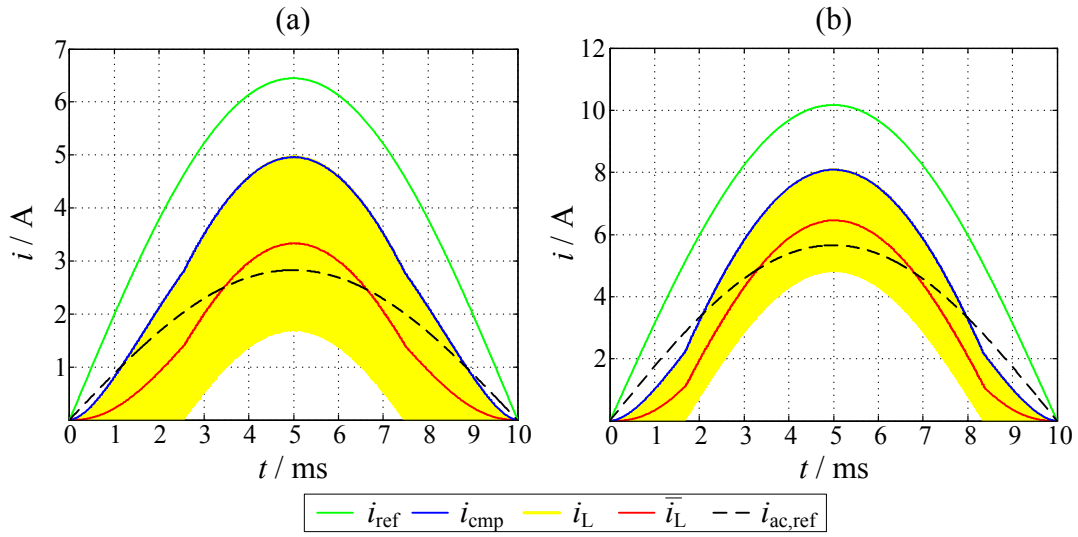

Figure 6.18: Current shapes with const. k_r at $V_{ac} = 115\text{V}$
a) $I_{ac,ref} = 2\text{A};\ k_r = 0.5;\ PF = 96.75\%$;
b) $I_{ac,ref} = 4\text{A};\ k_r = 0.7;\ PF = 97.17\%$

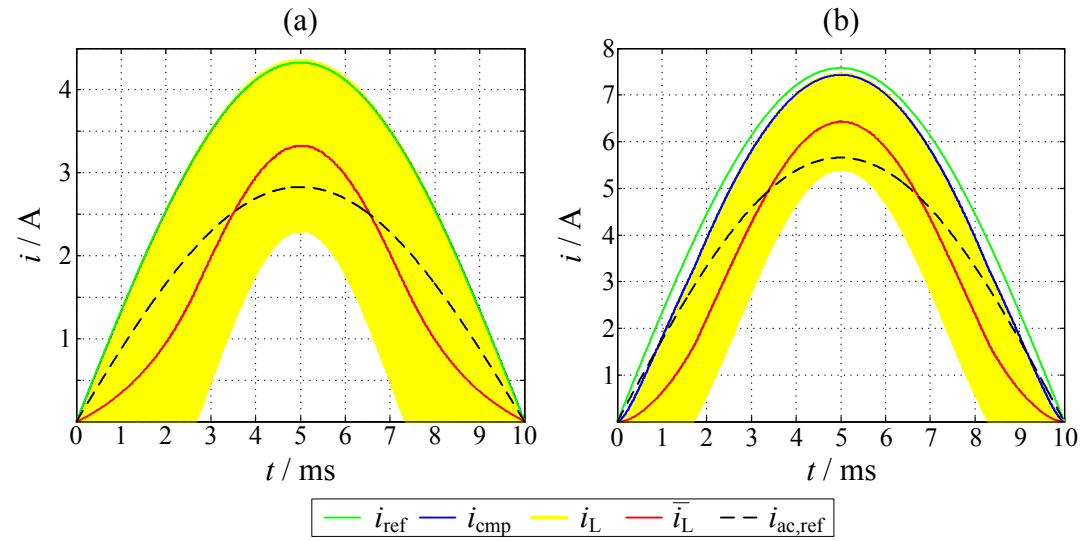

Figure 6.19: Current shapes with const. k_r at $V_{ac} = 230\text{V}$
a) $I_{ac,ref} = 2\text{A};\ k_r = 0.0; PF = 97.38\%$;
b) $I_{ac,ref} = 4\text{A};\ k_{sc} = 0.1;\ PF = 98.12\%$

6.4.3 Feed-Forward Algorithm

The previous methods were kept very simple and need only little computational effort. But they do not fulfill the power factor requirements of advanced PFC applications and therefore illustrate, why peak current control is not utilized in most PFC applications. However, with the digital implementation of peak current control and slope compensation new potentials for advanced PFC demands arise.

In order to enable an ideal sinusoidal shape of the average current a feed-forward algorithm is investigated, which computes from the sinusoidal reference current i_{ref} a feedforward reference current $i_{ref,ff}$ for the digital slope compensation. The control structure is illustrated in Figure 6.20. An adaptive k_{sc} is used to prevent subharmoic oscillation at all operating points.

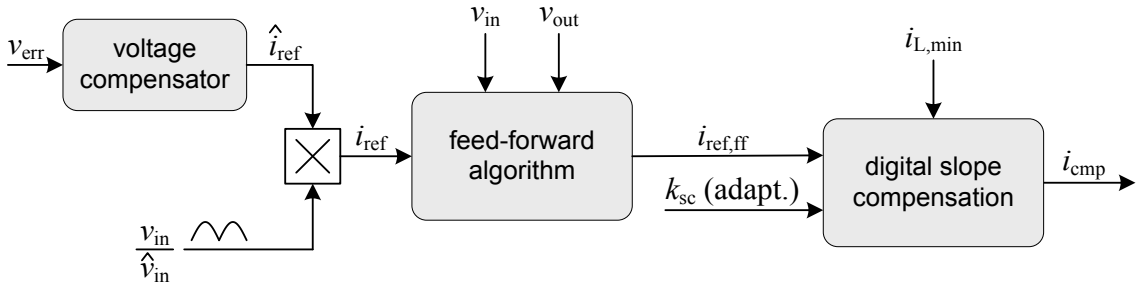

Figure 6.20: Control structure with feed-forward algorithm and adaptive compensation factor k_{sc}

The feed-forward algorithm needs to eliminate all deviations between the current reference value and the average inductor current. The deviations due to the inductor current ripple and the slope compensation were already mentioned. Other effects which cause deviations in the average current are the sample delay and operating in DCM partially. For this reason a distinction between CCM and DCM must be performed.

First, the conditions in CCM are examined. The difference between the inductor peak and average current in CCM is half the current ripple. The theoretical steady state value is computed with

$$\frac{\Delta i_L}{2} = \frac{v_{in}}{2L} \frac{v_{out} - v_{in}}{v_{out}} T_s. \tag{6.12}$$

The deviation caused by the slope compensation can be expressed as

$$\Delta i_{sc} = k_{sc} \frac{v_{in}}{L} \frac{v_{out} - v_{in}}{v_{out}} T_s. \tag{6.13}$$

In Section 6.3 the need of a delayed sampling of the valley current was exemplified. Delaying the sampling by T_{sd} increases the measured current. With using this increased

value for the digital slope compensation algorithm the inductor peak current and consequently the average current increase by

$$\Delta i_d = m_{sc} T_{sd} = k_{sc} \frac{v_{in}}{L} T_{sd}. \tag{6.14}$$

In order to compensate the deviations of Eq. (6.12), (6.13) and (6.14), these three components need to be integrated in the feed-forward reference current

$$i_{ref,ff} = i_{ref} + \frac{\Delta i_L}{2} + \Delta i_{sc} - \Delta i_d. \tag{6.15}$$

Consequently, the feed forward algorithm for CCM operation can be computed with

$$i_{ref,ff} = i_{ref} + \frac{v_{in}}{L} \frac{v_{out} - v_{in}}{v_{out}} T_s \left(\frac{1}{2} + k_{sc} \right) - k_{sc} \frac{v_{in}}{L} T_{sd}. \tag{6.16}$$

Figure 6.21 illustrates the three components which cause the deviation between the average current and the required feed-forward reference current.

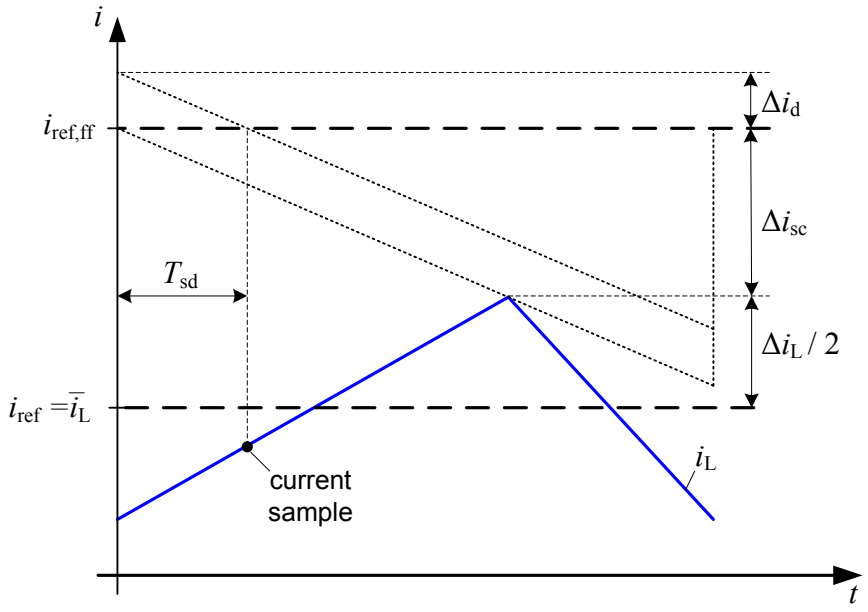

Figure 6.21: Deviation between the average inductor current and the feed-forward reference current

Now the situation at DCM is examined. Of course, the execution of slope compensation in DCM is not required to avoid subharmonic oscillations, however, in PFC applications a smooth transition during changes in the operation mode must be ensured. Thus, slope compensation is applied continuously.

In DCM where the current resets to zero in every switching cycle, the valley current is zero and can be ignored, if no sample delay is present. The digital slope compensation algorithm (cf. Eq. (6.6)) reduces to

$$i_{cmp,DCM} = \frac{1}{1 + k_{sc}}\, i_{ref}. \tag{6.17}$$

The current ripple $\Delta i_{L,DCM}$ is equal to the threshold level $i_{cmp,DCM}$. Consequently, for the required feed-forward reference current it follows

$$i_{ref,ff,DCM} = (1 + k_{sc})\Delta i_{L,DCM}. \tag{6.18}$$

There remains the calculation of the DCM current ripple with

$$\Delta i_{L,DCM} = \sqrt{2\,\bar{i}_L \frac{v_{in}}{L} \frac{v_{out} - v_{in}}{v_{out}} T_s} \tag{6.19}$$

to get a link to the inductor average current. Since for the feed-forward control $i_{ref} = \bar{i}_L$ must apply, the feed-forward algorithm for DCM is computed with

$$i_{ref,ff,DCM} = (1 + k_{sc}) \sqrt{2\, i_{ref} \frac{v_{in}}{L} \frac{v_{out} - v_{in}}{v_{out}} T_s} - k_{sc} \frac{v_{in}}{L} T_{sd}\,. \tag{6.20}$$

Where the last term is added to compensate a sample delay like in CCM.

Due to the permanent change between CCM and DCM in PFC applications the exact instant needs to be identified. In Section 4.2.2 this task is performed by evaluating the theoretical duty-ratios. The equal changeover instants are obtained by utilizing the theoretical current ripples. The ripple for CCM results from Eq. (6.12) and for DCM from Eq. (6.19). The smaller theoretical value determines the operation mode:

$$\Delta i_{L,CCM} \leq \Delta i_{L,DCM} \quad \rightarrow \text{CCM}$$
$$\Delta i_{L,CCM} > \Delta i_{L,DCM} \quad \rightarrow \text{DCM}$$

This process is illustrated with exemplary curves of current ripples in Figure 6.22. For DCM a series of curves results. The marked intersections with the curve for the CCM ripple indicate the changes of the operation mode. For $I_{ac} = 4\text{A}$ pure CCM and for $I_{ac} = 0.5\text{A}$ pure DCM would result theoretically.

For simulation an adaptive compensation factor k_{sc} with a constant compensation gain $\gamma = 2/3$ was utilized. Thus, a stable operation is ensured for all operating points. The resulting current shapes during one line cycle are shown in Figure 6.23 for low line voltage

and in Figure 6.24 for high line voltage with varied input currents. Depicted are the average inductor reference current i_{ref}, the computed feed-forward reference current $i_{ref,ff}$, the comparator threshold current i_{cmp}, the inductor current i_L and the resulting inductor average current $\bar{i}_L$.

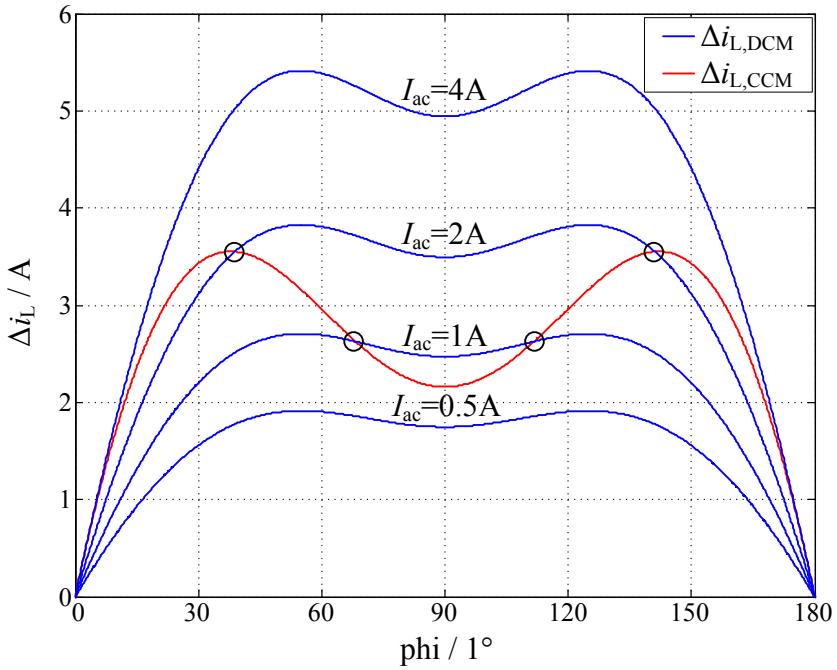

Figure 6.22: Theoretical current ripple during line half-cycle for CCM and DCM at different input power ($V_{in} = 230\text{V}, V_{out} = 400\text{V}, L = 470\mu\text{H}$)

In all simulations the average inductor current reveals a sinusoidal shape like the reference value, for which reason a power factor close to unity is achieved for all operation points. Consequently, with the applied feed-forward algorithm all deviations are eliminated effectively in CCM and DCM. In addition the transition between CCM and DCM occurs without any interference. The optimal shape of the computed feed-forward reference current differs significantly from the sinusoidal shape of the average current.

In practice the required input and output voltage are measured anyway and are available for the feed-forward control accordingly. However, one disadvantage is the need of the inductance value L. Due to tolerances the actual value can differ from the nominal value significantly and therefore impair the performance.

The complete feed-forward control algorithm consists of a multitude of operations including time-consuming calculations like square root and divisions. To get the best performance the feed-forward algorithm needs to be updated in each switching cycle. This method requires an appropriate DSP or µC. However, the feed-forward computation is not time critical. Thus, a feasible method is to spread the calculations on a few switching cycles. This impairs the performance slightly, but requires less computing power.

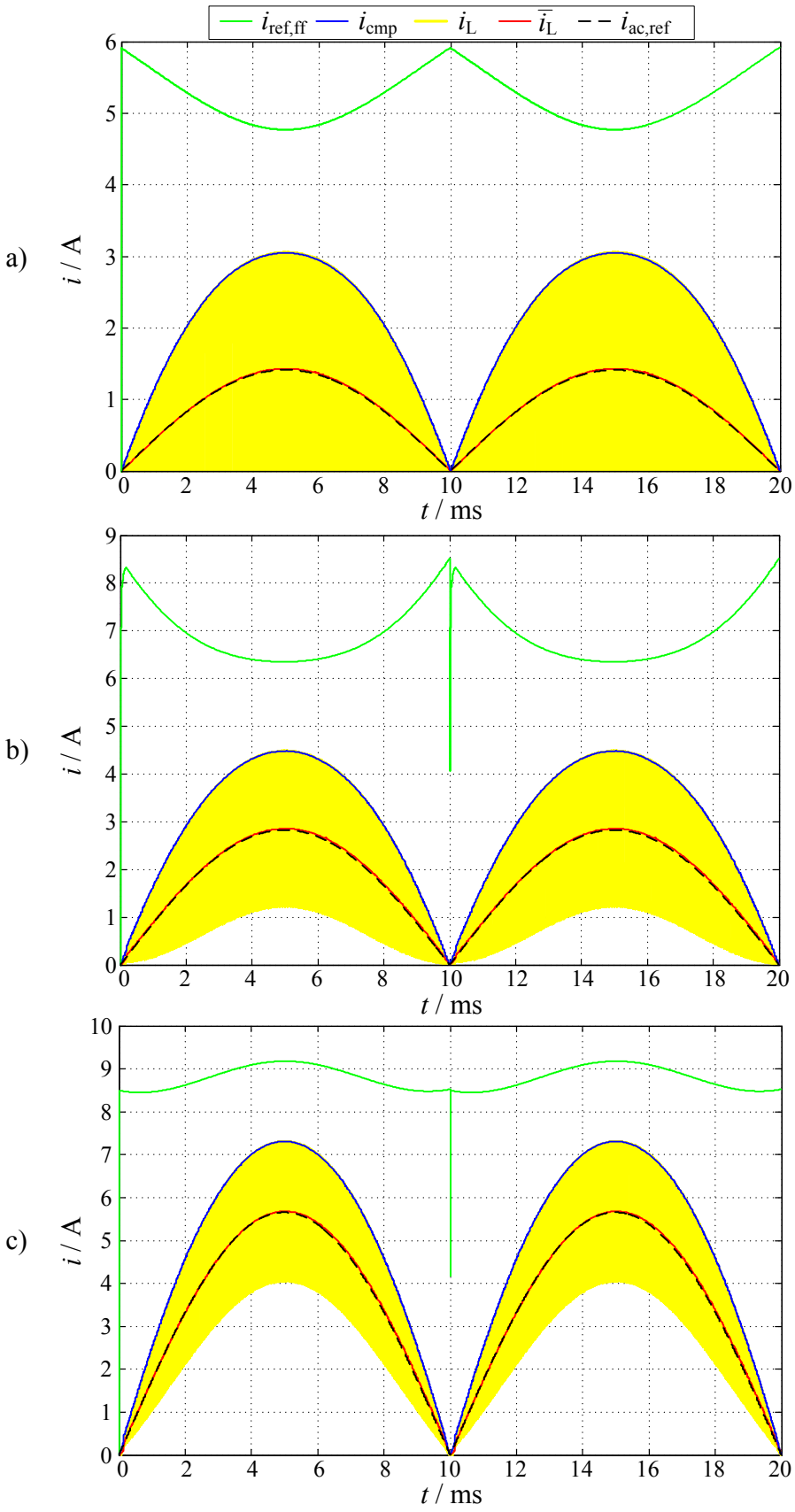

Figure 6.23: Current shapes with feed-forward algorithm at $V_{ac} = 115\text{V}$
a) $I_{ref} = 1\text{A}$, b) $I_{ref} = 2\text{A}$, c) $I_{ref} = 4\text{A}$

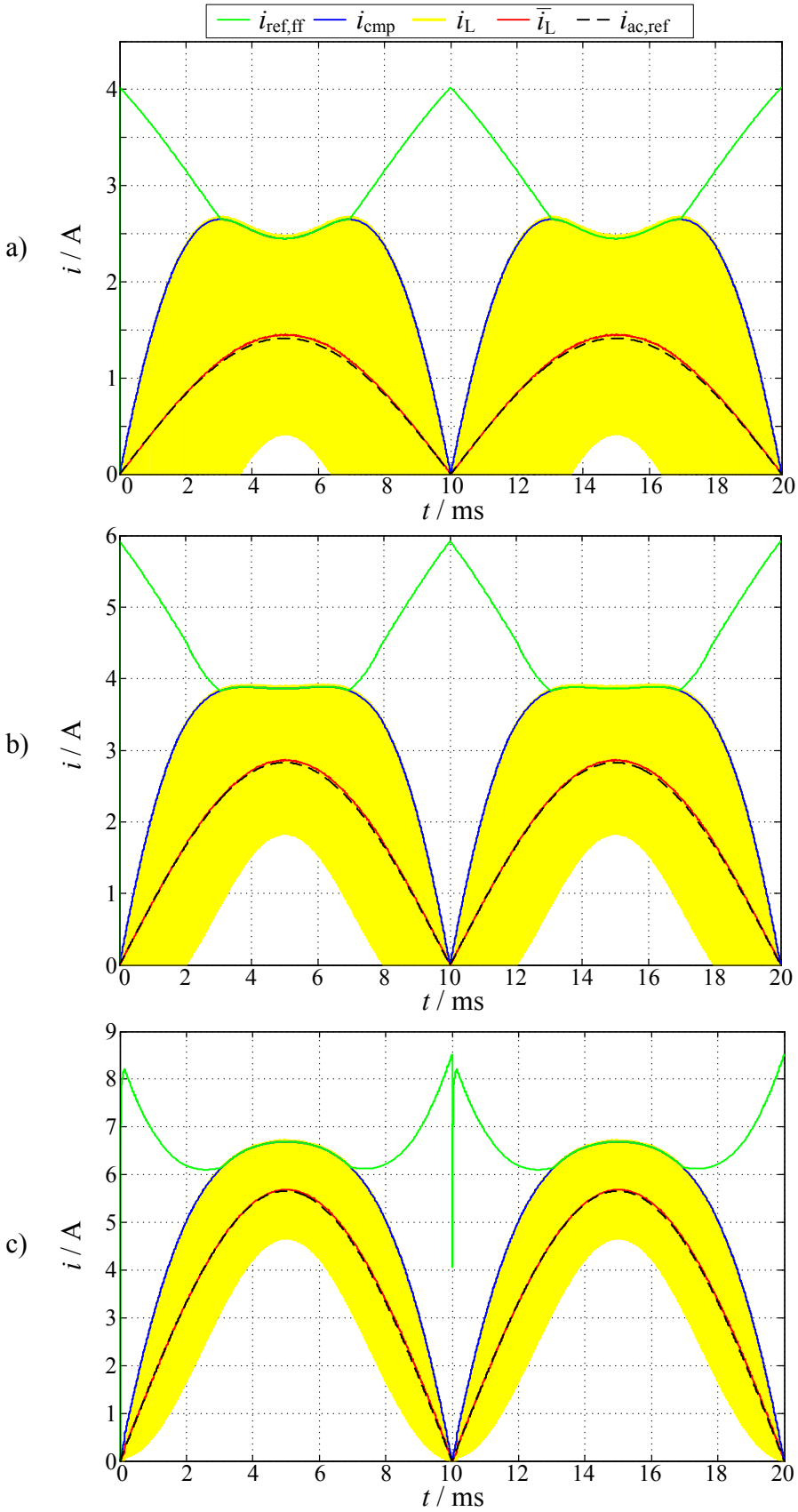

Figure 6.24: Current shapes with feed-forward algorithm at $V_{ac} = 230\text{V}$
a) $I_{ref} = 1\text{A}$, *b)* $I_{ref} = 2\text{A}$, *c)* $I_{ref} = 4\text{A}$

6.4.4 Outer Average Current Controller

Another promising method to compensate deviations in the average input current is the implementation of an average current controller. For this purpose the average input current needs to be captured and compared with the sinusoidal reference current to get the current error i_{err}. The current controller determines the reference value $i_{ref,cc}$ for the slope compensation algorithm. The resulting control structure is given in Figure 6.25. The structure is very similar to the feed-forward control. With an optimal current controller also the reference value for the digital slope compensation should have the same shape to achieve a sinusoidal average input current. However, compared to the feed-forward control the required computing power reduces significantly by using a low-order controller. Furthermore, no distinction between CCM and DCM is required. Another advantage is that no knowledge of the inductance value or other parameters is required. One drawback by applying an average current controller is the loss of dynamic in the entire current control loop.

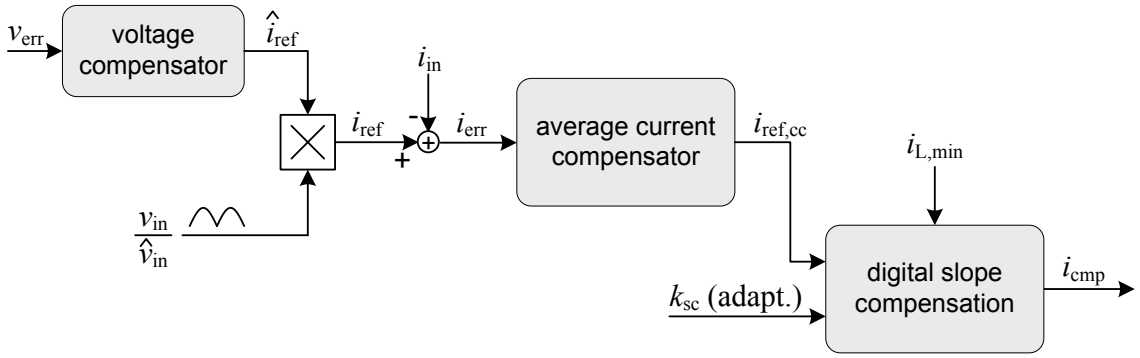

Figure 6.25: Control structure with average current controller and adaptive compensation factor k_{sc}

For the controller design the transfer function of the control path has to be identified. The control path consists of the closed peak current control loop. Compared to the dynamic of the current control loop the input and output voltage change very slowly, for which reason constant voltage values are assumed for the small signal model. The block diagram of the simplified model is given in Figure 6.26.

The corresponding control-to-inductor current transfer function is

$$G_{ic} = \left.\frac{i_{L\Delta}(s)}{i_{ref\Delta}(s)}\right|_{v_{in\Delta}=0} = \frac{F_m\, G_{id}(s)}{1 + F_m\, G_{id} + F_m F_v G_{vd}(s)}. \tag{6.21}$$

For the boost converter it follows [Eri00]

$$G_{id} = \frac{2v_{out}}{(1-D)^2 R} \frac{1 + s\frac{RC}{2}}{1 + s\frac{L}{(1-D)^2 R} + s^2 \frac{LC}{(1-D)^2}}, \tag{6.22}$$

$$G_{vd} = \frac{v_{out}}{(1-D)} \frac{1 - s\frac{L}{(1-D)^2 R}}{1 + s\frac{L}{(1-D)^2 R} + s^2 \frac{LC}{(1-D)^2}} \tag{6.23}$$

and

$$F_v = \frac{(1-D)^2 T_s}{2L}. \tag{6.24}$$

Where D represents the large signal duty-ratio

$$D = \frac{v_{out} - v_{in}}{v_{out}}. \tag{6.25}$$

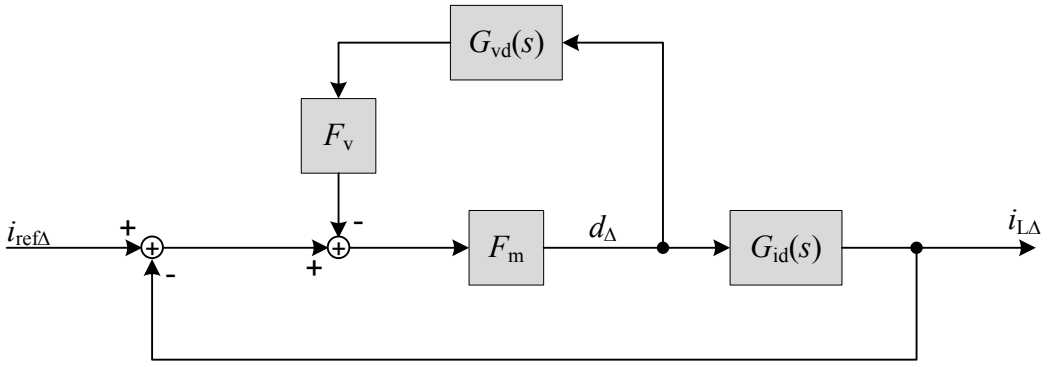

Figure 6.26: Block diagram of the simplified peak current control

The factor F_m includes the slope compensation. For digital slope compensation it contains the compensation factor k_{sc}:

$$F_m = \frac{L}{k_{sc} v_{in} T_s} \tag{6.26}$$

Thus, the control-to-inductor current transfer function Eq. (6.21) depends on the input and output voltage, the load and the preset compensation. The influence of the load is negligible, especial at higher frequencies. From Eq. (6.26) it follows that the dynamic reduces with higher compensation factors. Therefore the controller design is conducted with the value for optimum slope compensation. This also ensures that only positive values for the compensation factor are applied (i.e. $k_{sc} > 0$). The output voltage typically remains

constant and the input voltage varies continuously. Frequency curves for different steady-state input voltages are considered for the controller design, accordingly.

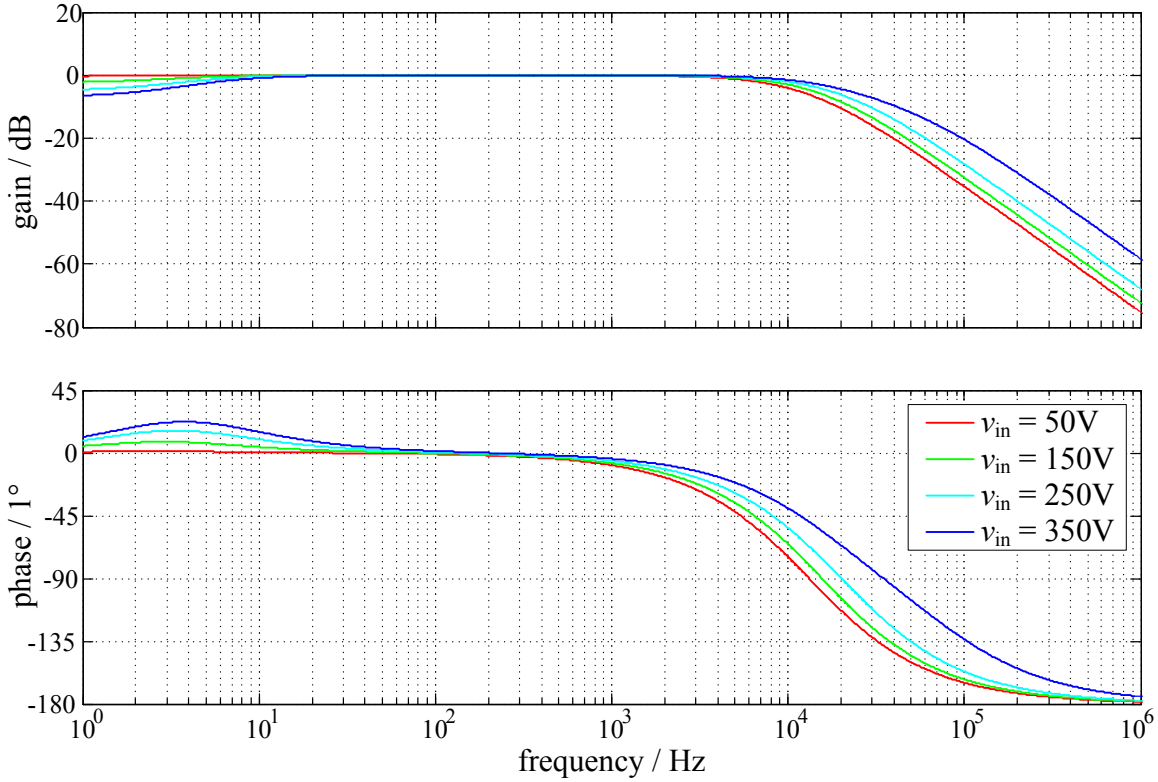

Figure 6.27: Bode plot of the normalized control-to-inductor current transfer function for different input voltages

From the set of frequency curves in Figure 6.27 it can be seen that the closed peak current control loop has almost unity transfer characteristic up to ca. 10kHz. For such a control path a simple I-type controller

$$G_I(s) = \frac{1}{s\,T_I} \tag{6.27}$$

can be applied. Additionally the dead time of the digital average current loop must be considered. For the utilized implementation a dead time of $T_d = 1.5\,T_s$ results. Consequently, the transfer function of the open average current loop results as

$$G_o(s) = G_{ic}(s)G_I(s)e^{-s\,T_d}\,. \tag{6.28}$$

In order to achieve an adequate dynamic with sufficient phase margin a proper value for T_I needs to determined. Therefore the control-to-inductor current transfer function for $v_{in} = 50\text{V}$ is employed. For a crossover frequency of $f_c = 2\text{kHz}$ it follows

$$T_I = 78\mu\text{s}\,. \tag{6.29}$$

The resulting phase margin $\varphi_c > 50°$ can be get form frequency curves in Figure 6.28.

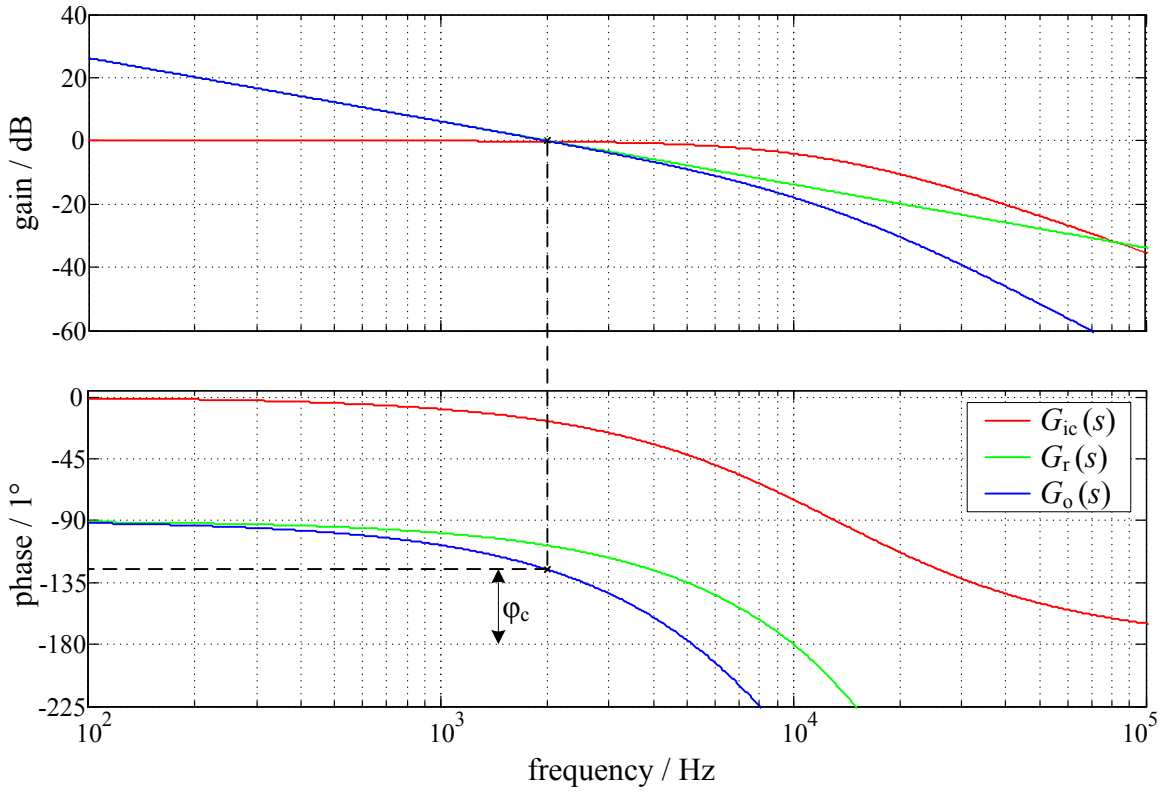

Figure 6.28: Frequency curves for the normalized closed peak current loop $G_{ic}(s)$, digital controller $G_r(s)$ with included dead time and open average current loop $G_o(s)$ ($v_{in} = 50\text{V}, T_I = 78\mu\text{s}, T_d = 1.5T_s$)

In order to compare the performance of the current controller with the feed-forward method the same operating points with equal parameters were utilized for simulation.

The resulting current shapes during one line cycle are shown in Figure 6.29 for low line voltage and in Figure 6.30 for high line voltage with varied input currents.

Instead of the feed-forward reference current the current controller output value $i_{ref,cc}$ is depicted. However, the shape is similar to the feed-forward results (cf. Figure 6.23 and Figure 6.24). This indicates an adequate current control. This is also confirmed by the shape of the average inductor current $\bar{i}_L$, which shows a nearly ideal sinusoidal shape.

Due to the inner peak current loop there is no change in the control path dynamic for the average current controller at the transition between CCM and DCM.

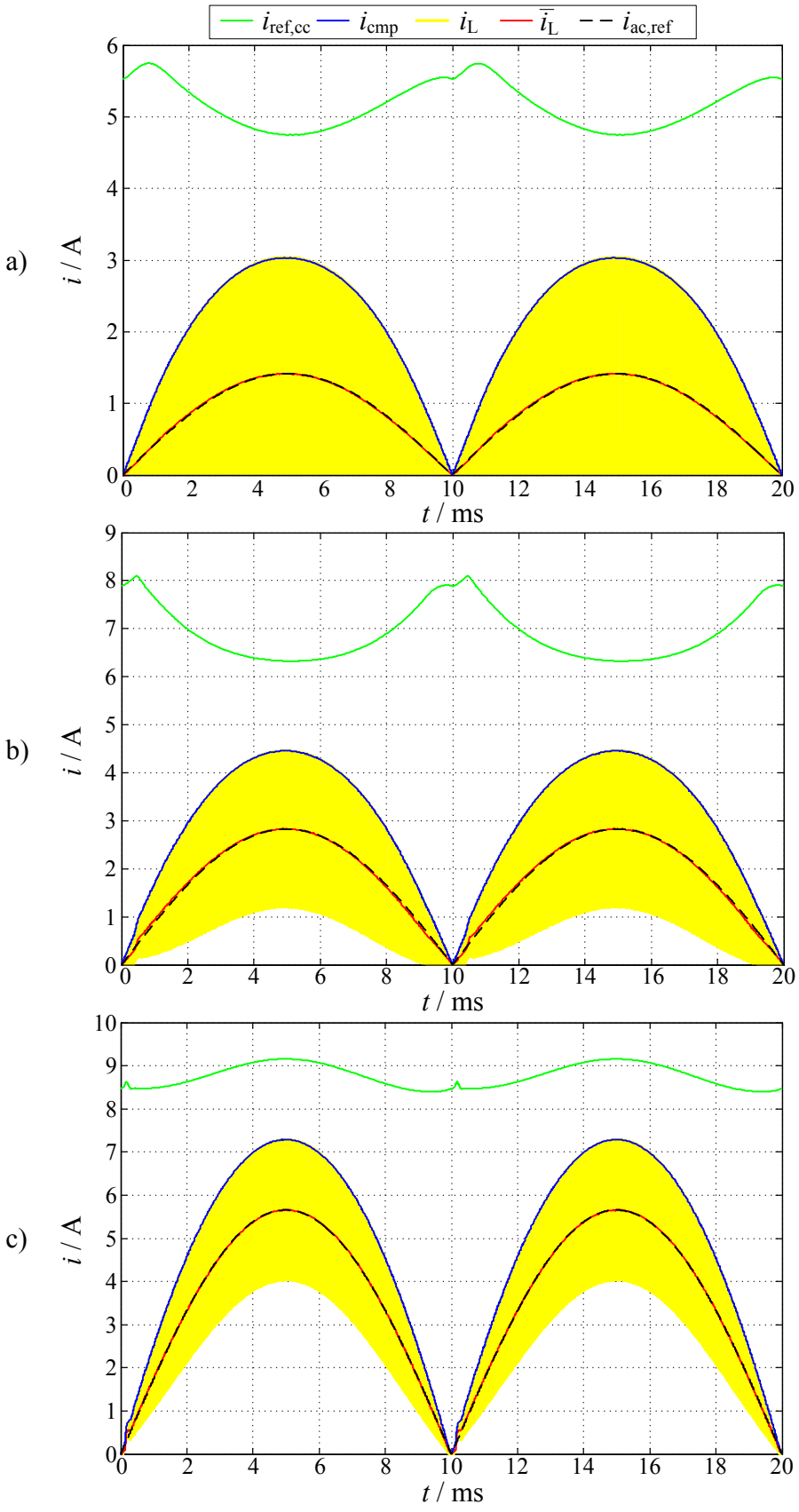

Figure 6.29: Current shapes with average current controller at $V_{ac} = 115\text{V}$ a) $I_{ref} = 1\text{A}$, b) $I_{ref} = 2\text{A}$, c) $I_{ref} = 4\text{A}$

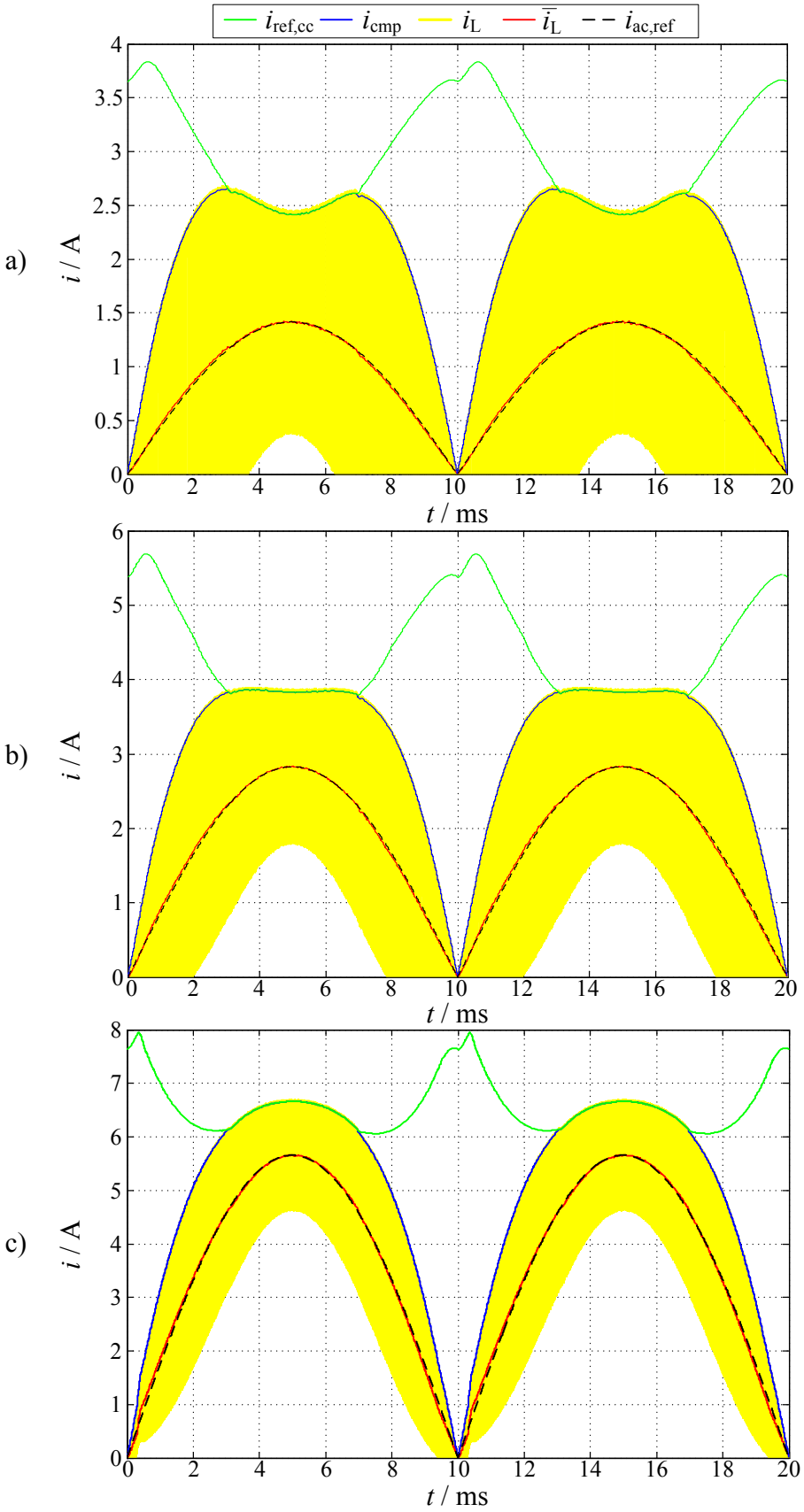

Figure 6.30: Current shapes with average current controller at $V_{ac} = 230\text{V}$ a) $I_{ref} = 1\text{A}$, b) $I_{ref} = 2\text{A}$, c) $I_{ref} = 4\text{A}$

6.4.5 Interleaved Operation

At interleaved operation every single converter rail has its own comparator. Thus, every rail requires an individual comparator threshold current i_{cmp}. Accordingly, all minimum inductor current values $i_{L,min}$ need to be sampled at the correct instant of time and the corresponding slope compensation algorithm has to be computed instantaneously. The resulting control structure for three interleaved converters is given in Figure 6.31. Optionally, the method with average current controller or with feed-forward algorithm can be chosen to determine the optimal reference current for the digital slope compensation. The digital slope compensation algorithm needs to be computed for each rail. The optimal reference current as well as the compensation factor k_{sc} is the same for all rails. Accordingly, the computational effort for these values does not increase with the number of paralleled converters.

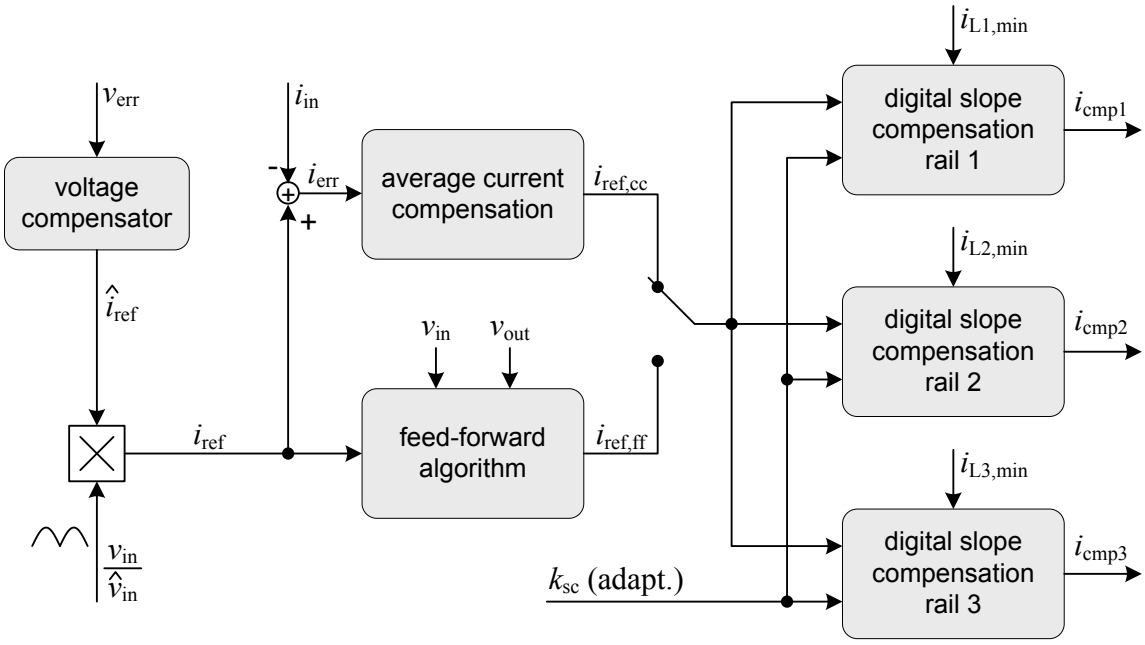

Figure 6.31: Control structure for three interleaved converters, optional with average current compensator or feed-forward algorithm

Generally, peak current mode provides good current sharing capability. Only if the inductance values differ, a slight difference in the average currents results consequently. With analog slope compensation the deviation in the average current in CCM is

$$\Delta\bar{i}_L = \left(\frac{1}{L_2} - \frac{1}{L_1}\right)\left(\frac{v_{in}}{2}\frac{(v_{out} - v_{in})}{v_{out}}T_s\right). \tag{6.30}$$

This deviation also occurs with digital slope compensation. However, additionally the compensation factor and the delayed sampling have influence on the average current (cf.

Section 6.3). Accordingly, the difference in the average current with digital slope compensation in CCM is quantized by

$$\Delta\bar{i}_L = \left(\frac{1}{L_2} - \frac{1}{L_1}\right)\left(\frac{v_{in}}{2}\frac{(v_{out} - v_{in})}{v_{out}}T_s + k_{sc}v_{in}\frac{(v_{out} - v_{in})}{v_{out}}T_s - k_{sc}v_{in}T_{sd}\right). \quad (6.31)$$

Thereby an increased compensation factor induces an increased current deviation, whereas the sample delay has a damping influence and compensates the error by the compensation factor partially.

Also for the deviation in DCM the inductor average currents needs to be subtracted. Thus, the average current is given by

$$\bar{i}_{L,DCM} = \frac{v_{out}L}{2\,(v_{out} - v_{in})v_{in}T_s}\left(\frac{i_{ref}}{1 + k_{sc}} + \frac{k_{sc}}{1 + k_{sc}}\frac{v_{out}T_{sd}}{L}\right)^2. \quad (6.32)$$

Theoretically, equal average currents under unequal inductance values can be achieved by using the feed-forward algorithm, if all inductance values are known and every converter rail gets its own feed-forward reference value. However, in most cases the exact inductance values are not known and furthermore the calculation of the feed-forward algorithm for each rail would significantly increase the computational effort. Thus, it is advisable to keep the compensation factor as small as possible for good current balancing.

The deviation in the average inductor currents of three interleaved rails are depicted in Figure 6.32. The inductance values of L_2 and L_3 were intentionally modified by 5% to L_1. The feedforward method with a sample delay of $T_{sd} = 1\mu s$ and an adaptive compensation factor k_{sc} with a compensation gain $\gamma = 2/3$ was applied.

As expected only the average current of L_1 follows the reference value accurately. The larger inductance L_2 gets an increased and the smaller inductance L_3 a decreased average current. However, this systematically error in the average currents should be acceptable for most applications. Furthermore, critical for most components are the maximum peak currents and since the smallest inductance affected by the highest current ripple is stressed by the smallest average current, this effect is beneficial for peak current limitation.

Because only the algorithm for the digital slope compensation has to be performed for every rail the computational effort in interleaved operation is feasible with a standard DSP or µC. However, fundamental for a reliable operation is the need of a precise timing within each switching cycle (cf. Section 6.3). With interleaving several converters this criterion becomes more challenging.

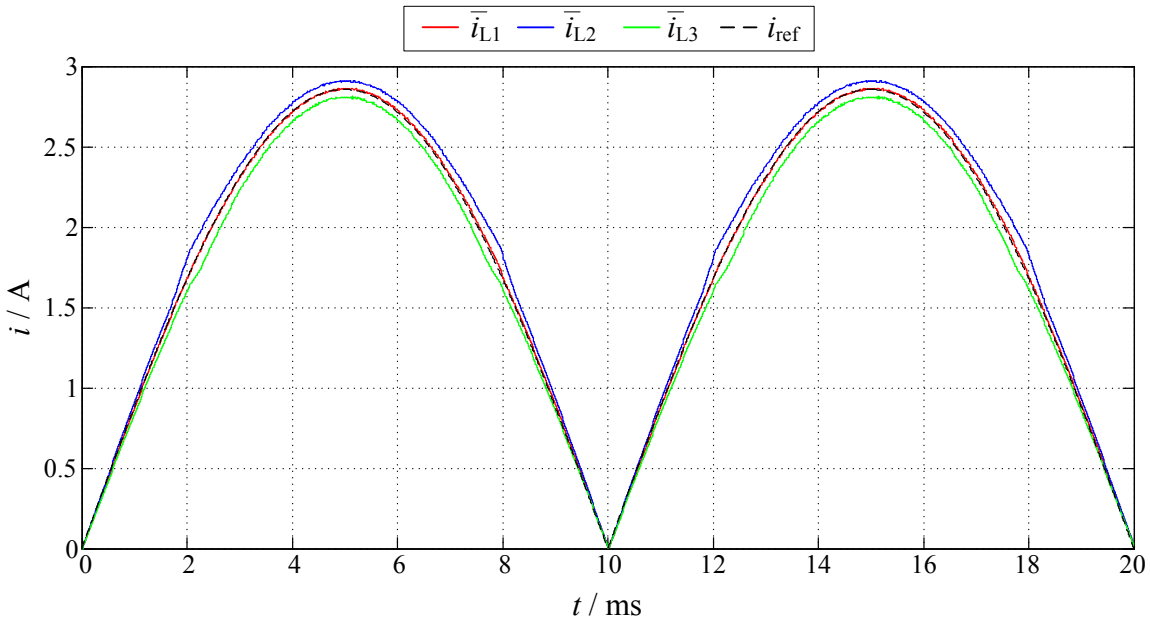

Figure 6.32: Inductor average currents during one line cycle with unequal inductance values ($L_1 = 470\mu H;\ L_2 = 1.05\ L_1;\ L_3 = 0.95\ L_1$) ($I_{ref} = 2A; V_{ac} = 230V; v_{out} = 400V;\ \gamma = 1/1.5$)

6.4.6 Measurements

In order to verify the practical effectiveness of the digital peak current control some exemplary measurements are presented. The component values of the prototype and the utilized parameters are identical to the simulation parameters of Table 6.2.

The measured input voltage, input current and inductor current waveforms for single-rail operation are depicted in Figure 6.33 and Figure 6.34 at full load. Figure 6.33 shows the waveforms at low line voltage and with average current controller. In Figure 6.34 the case with feed-forward algorithm is illustrated at high line voltage. In both cases the input current replicates the line voltage waveform accurately. This confirms the proper modeling and quality of simulations.

The inductor currents and the resulting input current with three interleaved rails are shown in Figure 6.35 for a few switching cycles. Waveforms during a complete line cycle of the interleaved operation are given in Figure 6.36.

The measured power factors versus the input current are depicted in Figure 6.37 for low and high line voltage with feed-forward and average current control. At low line voltage the power factor is already high at small input currents. At higher input currents excellent power factors above 99.5% are achieved in all cases. Thus, the high power factor requirements of advanced PFC applications are achieved with digital peak current control.

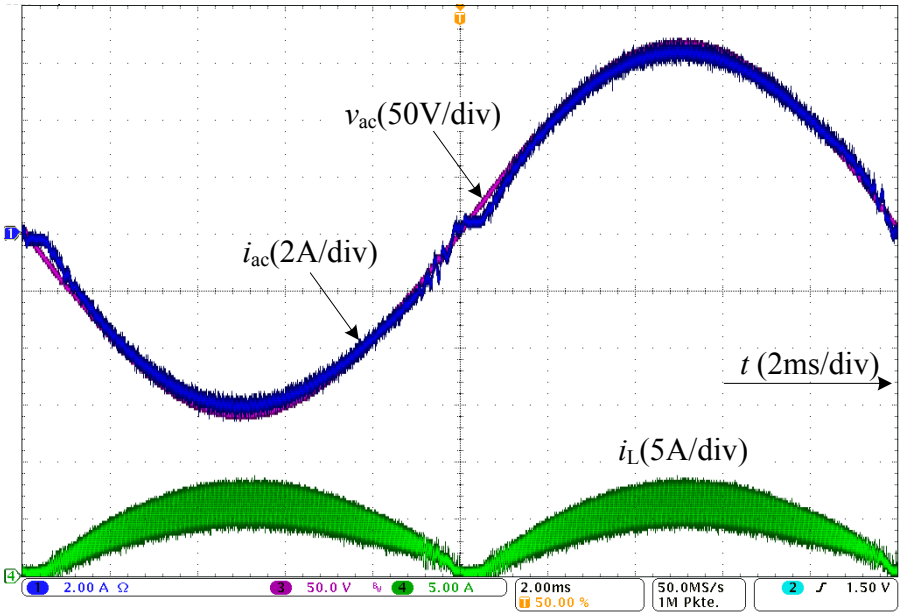

Figure 6.33: Current and voltage curves with average current controller ($V_{ac} = 115\text{V}; P_{out} = 500\text{W}; PF = 99.91\%$)

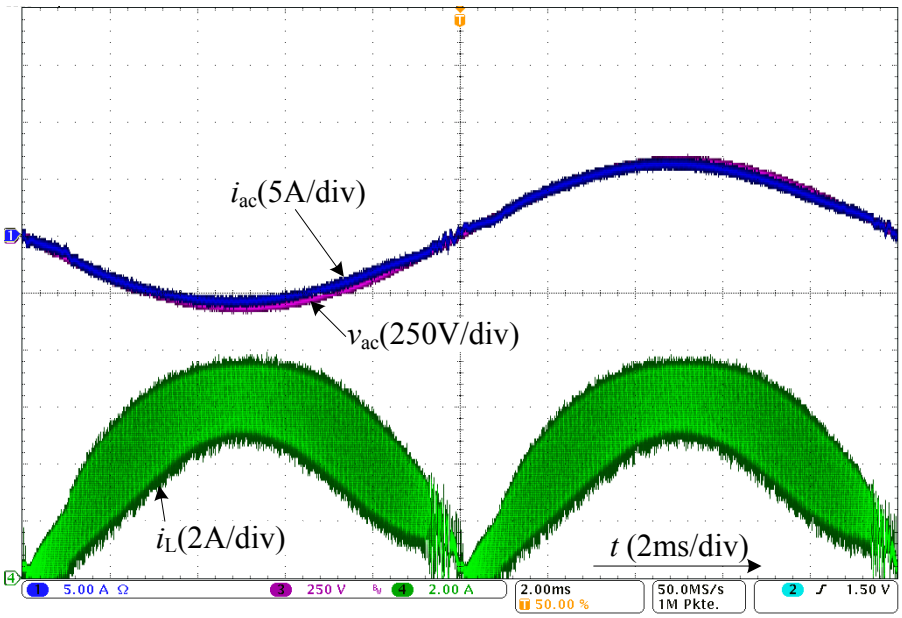

Figure 6.34: Current and voltage curves with feed-forward control ($V_{ac} = 230\text{V}; P_{out} = 1000\text{W}; PF = 99.92\%$)

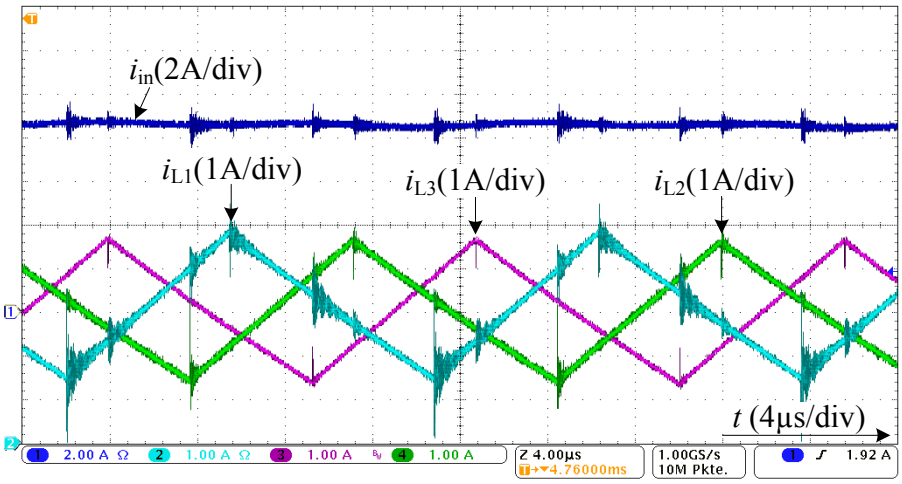

Figure 6.35: Inductor currents and resulting input current with three interleaved rails

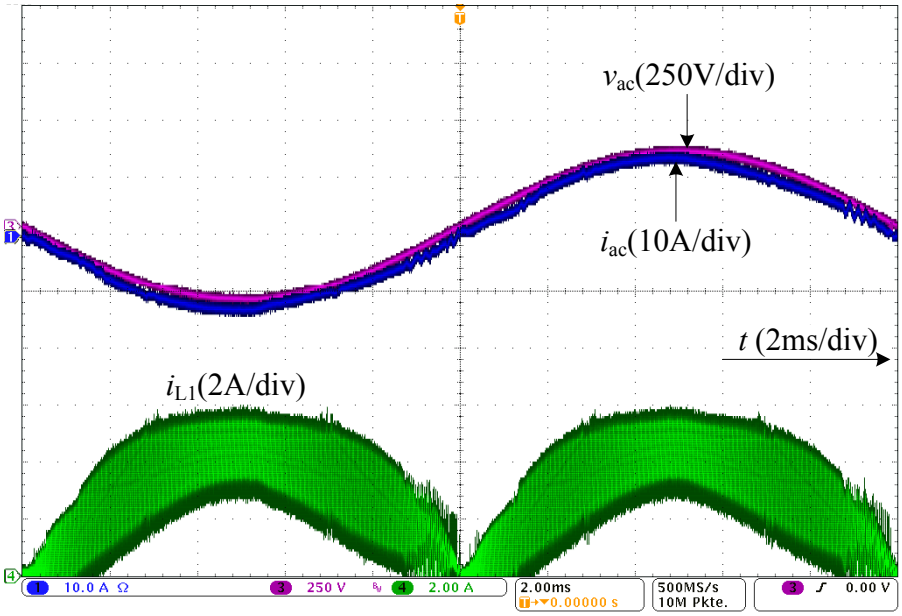

Figure 6.36: Current and voltage curves with feed-forward control and three interleaved rails ($V_{ac} = 230\text{V}; P_{out} = 2100\text{W}; PF = 99.92\%$)

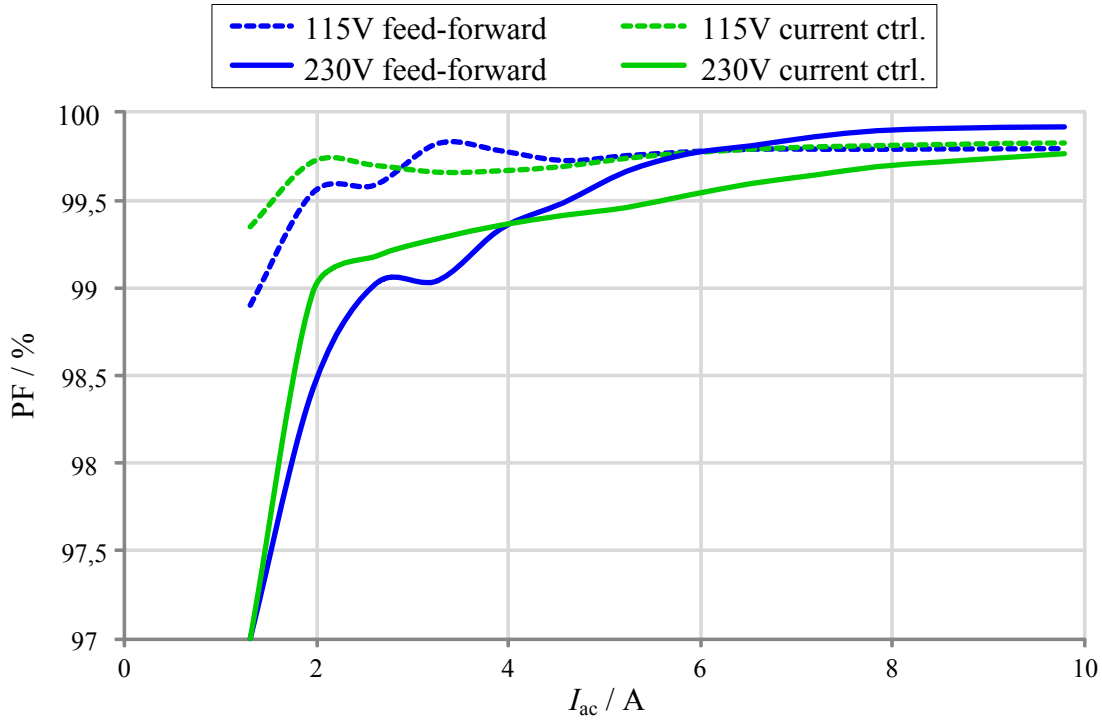

Figure 6.37: Measured power factor versus input current with three interleaved rails for low and high line voltage with feed-forward algorithm (blue) and average current controller (green)

6.5 Summary

Up to now peak current control was predominantly implemented in analog technique. However, by dint of available DSPs and µCs with on-chip comparators digital peak current control is feasible with little effort. The need of slope compensation at duty-ratios above 50% to avoid subharmonic oscillation can be solved with simple, but effective digital algorithms. Therefore, it suffices to sample only the valley inductor current. Knowledge of the inductance or any other specific values is superfluous. By directly triggering the PWM unit via on-chip comparator only little computing power is required for the current control. Problems occurring in practice due to the reverse recovery current spike and the computing time can be handled with simple measures. Hence, digital slope compensation turns out as a practical alternative in peak current controlled applications. Furthermore, the digital implementation offers the potential to apply adaptive slope compensation. Thus, the amount of slope compensation can be adjusted depending on the input and output voltage relation of the converter. This guarantees requested dynamic performance of the current control loop from dead-beat up to a desired settling time with or without overshoot.

For PFC applications the digital peak current loop offers several ways of implementations. Simple methods with constant compensation factor or constant compensation slope offer acceptable power factors with low computational effort. High power factors can be achieved with a feed-forward algorithm or with an additional average current controller.

The feed-forward algorithm requires significant additional computational effort and knowledge of the inductance value. An additional average current controller also enables excellent power factors. For this purpose less computation power is required and knowledge of the inductance value is not necessary. However, measurement of the average input current must be performed for the average current controller.

By interleaving several converters the slope compensation algorithm needs to be performed for every single rail. However, all rails receive the same reference currents and compensation factors, for which reason the feed-forward or average current control only needs to be computed once for all rails.

The attainable power factors are similar to other PFC control methods. In contrast to digital average current control good current sharing and peak current limitation is inherent with digital peak current control. For both control methods an accurate sampling of the inductor current is essential. Whereas for average current control directly the average current is sampled, the slope compensation algorithm for digital peak current control uses the valley inductor current.

Due to the quite simple algorithm for the digital slope compensation peak current control requires little computational effort. Especially with increasing numbers of paralleled converters the digital peak current control needs less computational power than average current control. However, a precise timing is essential for a reliable operation of interleaved converters with digital peak current control.

7 Digital Boundary Conduction Mode (BCM) PFC Control

One popular control strategy for PFC applications is the boundary conduction mode (BCM), where the boost converter is operated at the boundary of DCM and CCM [HIJ08]. Compared to CCM the reverse recovery losses of the boost diode are eliminated. Due to turn-on of the boost switch at zero drain-source voltage or in the voltage valley also the switching losses are reduced [Mar10]. Thus, high efficiencies are attained together with low cost Si-diodes.

However, the BCM induces relative large inductor currents. Due to this characteristic the power level is limited up to $400 - 500\mathrm{W}$ and larger differential mode electromagnetic interference (EMI) filters are necessary [Hub09, Cho10]. In order scale up the power levels two or more converters should be operated interleaved, whereby the input current ripple and consequently the EMI filter can be reduced significantly. However, BCM is characterized by variable switching frequency, for which reason optimal interleaving becomes challenging. This task is topic of several publications [HIJ09, Cho10, BLu08], which mostly focus on interleaving only two converters with an analog control strategy. Hence, a new digital phase shift control is proposed in Section 7.3 enabling multi-rail interleaving of BCM operated converters.

7.1 BCM Control Concept

In order to switch on again after the inductor current decayed to zero, it is necessary to detect this instant. A common method to analyze the inductor current is to give the inductor an extra winding. The signal of this winding is passed to a comparator to generate the binary zero crossing detection (ZCD) signal (cf. Figure 7.1). The resulting ZCD signal as well as the inductor current and the drain-source voltage of the boost MOSFET are illustrated in the measurement of Figure 7.2 at DCM operation. Note, that due to the parasitic capacitors of the MOSFET the current oscillates after the first zero crossing. Consequently, several ZCD pulses are generated. However, typically the switch is turned on with the first ZCD rising edge. If necessary, the turn-on can slightly be delayed, to achieve optimal switching in the valley of the drain-source voltage of the MOSFET.

In BCM the inductor average current is half of the peak current. This characteristic is beneficial for PFC applications, where the average current must follow the shape of the input voltage. Consequently, it suffices to control the peak current and employing peak current mode control is obvious. This can be easily realized, because there is no need of slope compensation in BCM.

However, for most boost PFC applications another control strategy is utilized. In this method the sinusoidal average current shape is attained by just applying a constant switch on-time. This is justified, because the peak current and consequently the average current are directly linked to the input voltage:

$$\bar{i}_L = \frac{1}{2}\frac{v_{in}}{L}T_{on} \tag{7.1}$$

Thus, very good power factors are attained with BCM spending little control effort.

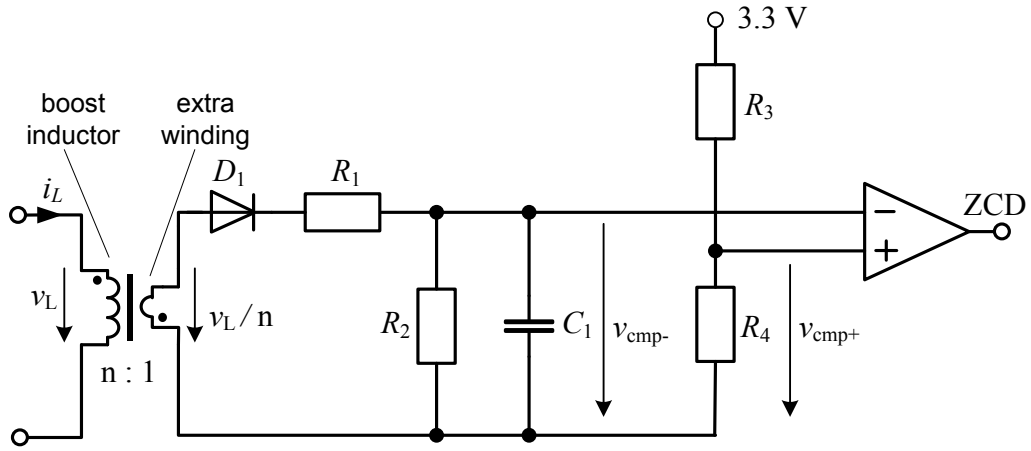

Figure 7.1: Schematic of the ZCD circuit

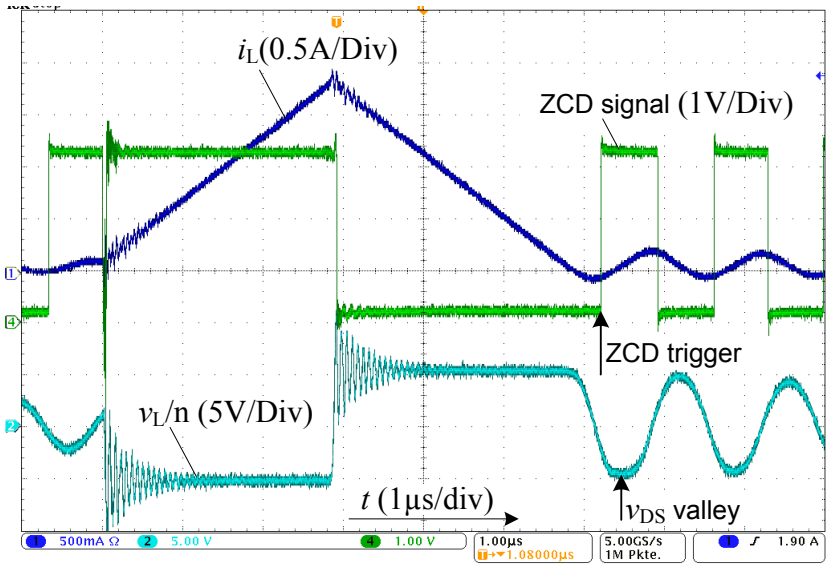

Figure 7.2: ZCD signals

7.2 Control Structure

For implementing the digital BCM control strategy a DSP with an additional state machine is utilized in order to perform the open loop current control. The state machine is realized on an FPGA, which provides more than enough logic elements. Thus, also the proposed phase shift control and frequency limitation are implemented on the FPGA. The block diagram of the BCM control structure is depicted in Figure 7.3.

The voltage control loop and the system management are still implemented on the DSP. The reference value for the current controller is the switch on-time T_{on}. Due to the fact that T_{on} is constant within the line period at steady state conditions the transmission of this value needs only be performed with low rate. Because the voltage controller is also very slow only little computing power is required for this part. For that reason a low-cost DSP or µC suffice.

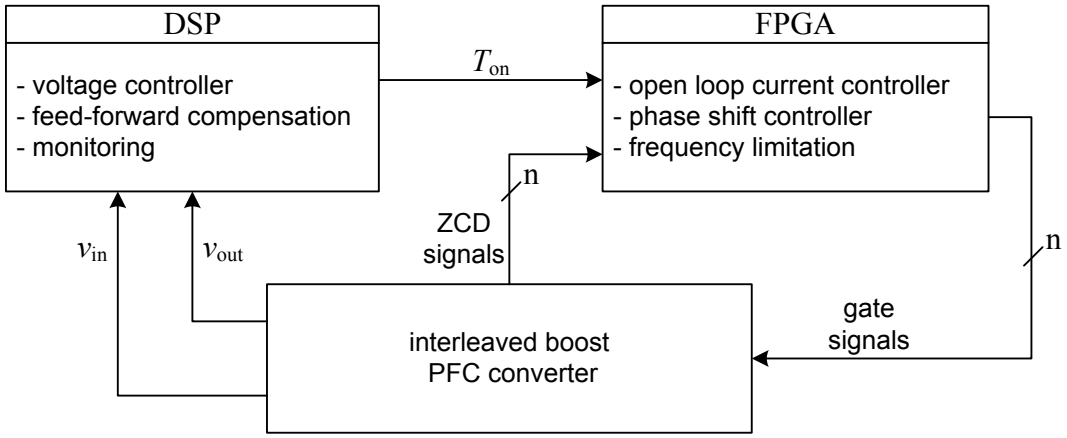

Figure 7.3: Structure of the digital open-loop BCM control

The on-time is passed to the FPGA as PWM signal for example. On the FPGA the received pulse width is converted into a binary number and passed to the current controller. The structure of the open loop current controller is shown in Figure 7.4. The rising edge of the ZCD signal is detected and utilized to reset a counter. With resetting the counter the gate signal is turned on until the counter value exceeds the requested on-time value.

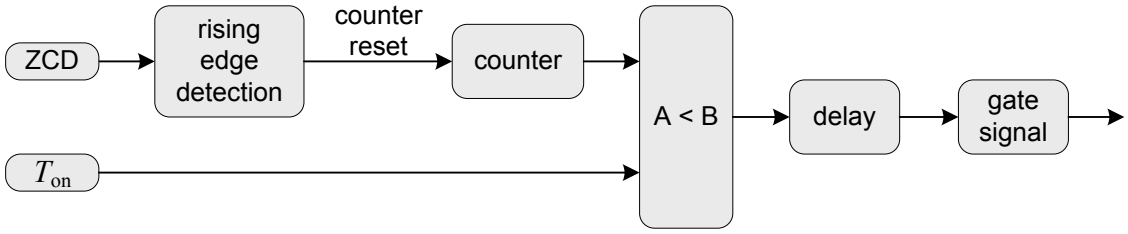

Figure 7.4: Structure of the open loop BCM current controller

7.3 Phase Shift Control for Interleaved BCM Rails

Higher power levels are attained by interleaving of two or more converter rails in BCM. However, due to the permanently varying switching frequency in PFC applications the tracking of the optimal phase shift for interleaved converters is challenging.

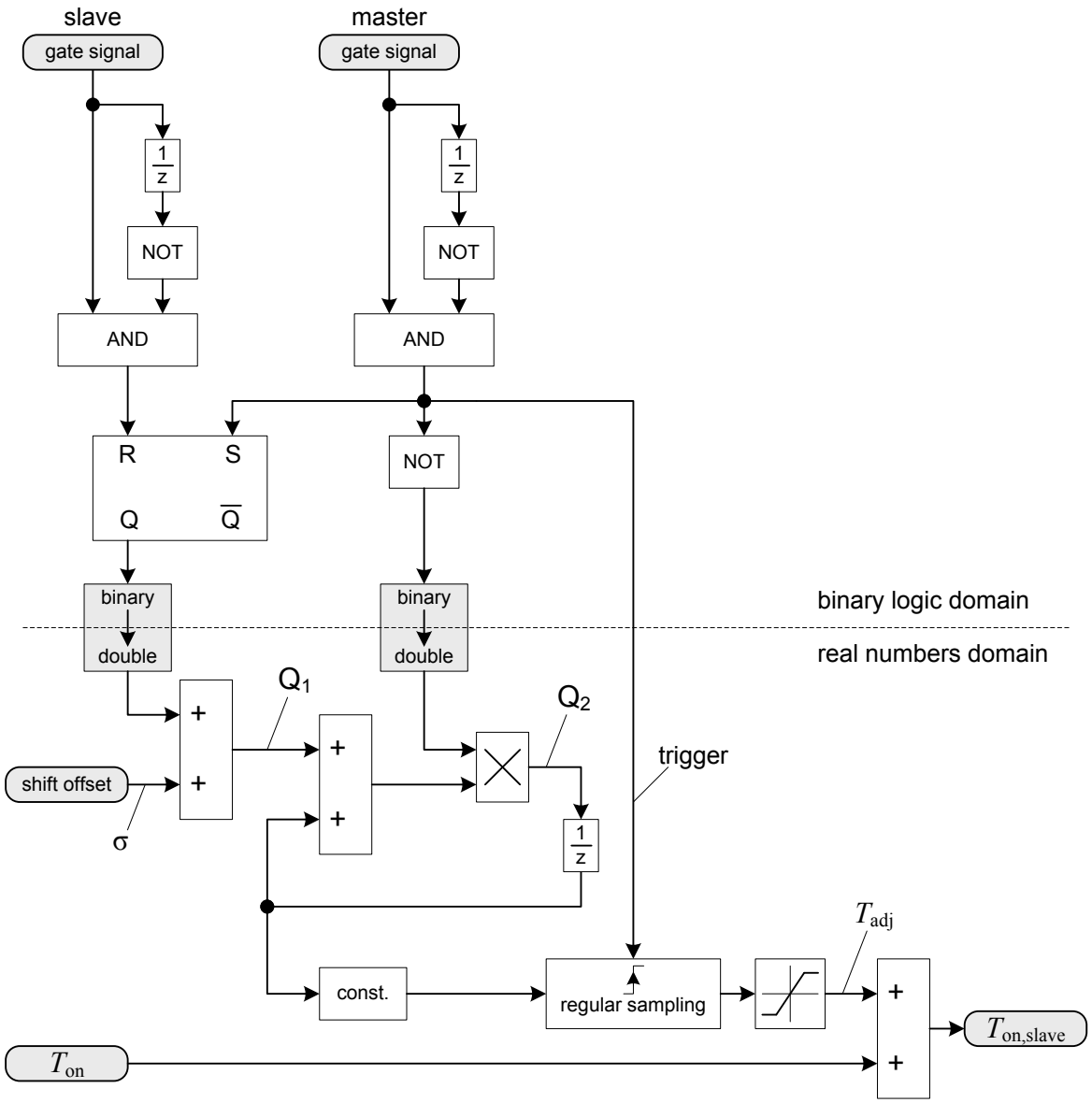

Figure 7.5: Scheme of the phase shift control simulation model

There are a multitude of publications for interleaving strategies for BCM PFC converters [HIJ09, Cho10, BLu08]. Most of these implementations are utilizing a master-slave strategy, where the master rail operates as a stand-alone converter. The phase shift of the slave converter is synchronized to the master rail to achieve optimal interleaving. This is either done with an open-loop or with a closed-loop method. The published interleaving

strategies are implemented in analog technique and are predominantly limited to only two interleaved rails.

In the following a closed-loop phase shift control method for optimal interleaving of BCM operated converters is presented, which is implemented fully digital on an FPGA. Withal, the number of interleaved rails is not limited. This digital implementation represents a master-slave method. Accordingly, every slave rail gets its own phase shift controller in order to be synchronized to the master rail. Thus, all phase shift controllers are running independent to each other.

The structure of the phase shift controller is depicted in Figure 7.5. The reference points are the switch-on instants of the master and the slave rail. These are passed to an RS-flip-flop. The switch-on instant of the master is used to set the flip-flop and with the switch-on pulse of the slave rail the flip-flop is reset. The binary output signal of the flip-flop is added to the negative phase shift offset. To determine the phase shift φ_k for the slave rail k the phase shift offset σ_k needs to be preset to

$$\sigma_k = -\frac{\varphi_k}{360°}. \tag{7.2}$$

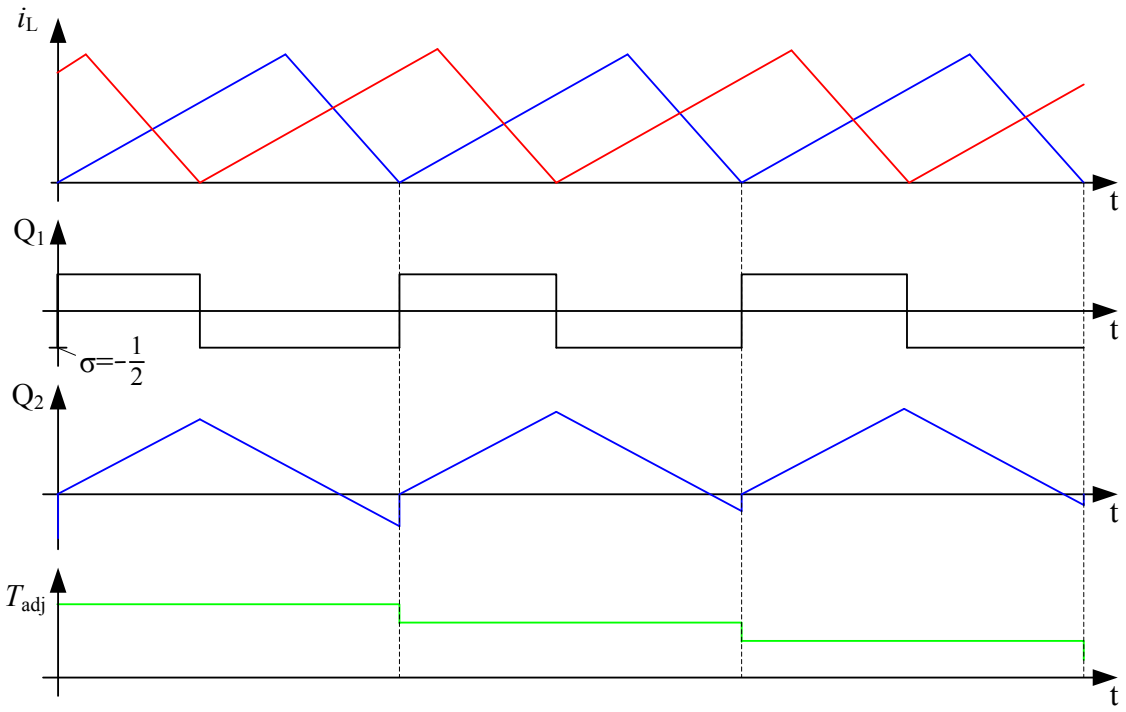

Figure 7.6: Signals of the phase control for phase shift of 180° *with phase error*

The DC component of the resulting signal represents the phase shift error, i.e. if there is no phase error the DC component is zero. The DC offset is identified by a discrete integrator. In order to get the phase error for every single switching cycle, the integrator is reset at every switch-on event of the master rail. Before the reset occurs a sample and hold element

stores the phase error for the next switching cycle. A simple constant controller gain is used to determine the correcting variable T_{adj}. This value is added to the master on-time T_{on} and the resulting sum represents the on-time for the corresponding slave rail.

To clarify the functionality of the phase shift controller two examples are illustrated in Figure 7.6 and Figure 7.7. Depicted are the waveforms of both inductor currents, of the integrator input and output signal and the resulting controller output value T_{adj}. Figure 7.6 shows the situation of two interleaved rails with requested 180° phase shift (i.e. $\sigma_2 = -1/2$). Due to the phase shift control the phase error reduces from cycle to cycle. In Figure 7.7 there is no phase error present and the requested phase shift is set to 120° (i.e. $\sigma_2 = -1/3$).

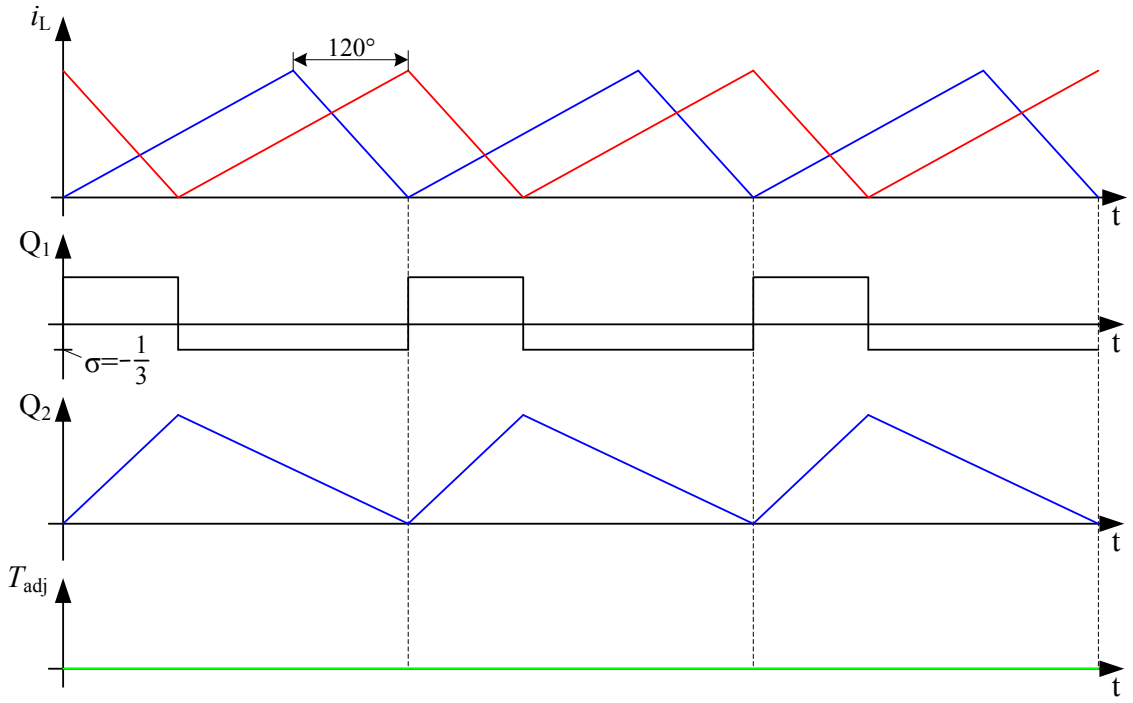

Figure 7.7: Signals of the phase control for phase shift of 120° *without phase error*

The effectiveness of the phase shift controller was verified in simulation (cf. Figure 7.8) and on the hardware prototype (cf. Figure 7.9). Employed were three paralleled boost converters, which start without phase shift. After a short delay the phase shift reference values $\varphi_2 = 120°$ (i.e. $\sigma_2 = -1/3$) and $\varphi_3 = 240°$ (i.e. $\sigma_3 = -2/3$) were applied. Depending on the momentary phase shift error the slave rails get slightly increased switch on-times and accordingly larger switching periods and higher peak values. In addition to the inductor current waveforms Figure 7.8 shows the time shift error. The initial error is compensated within a few switching cycles and therefore offers sufficient dynamic for PFC applications.

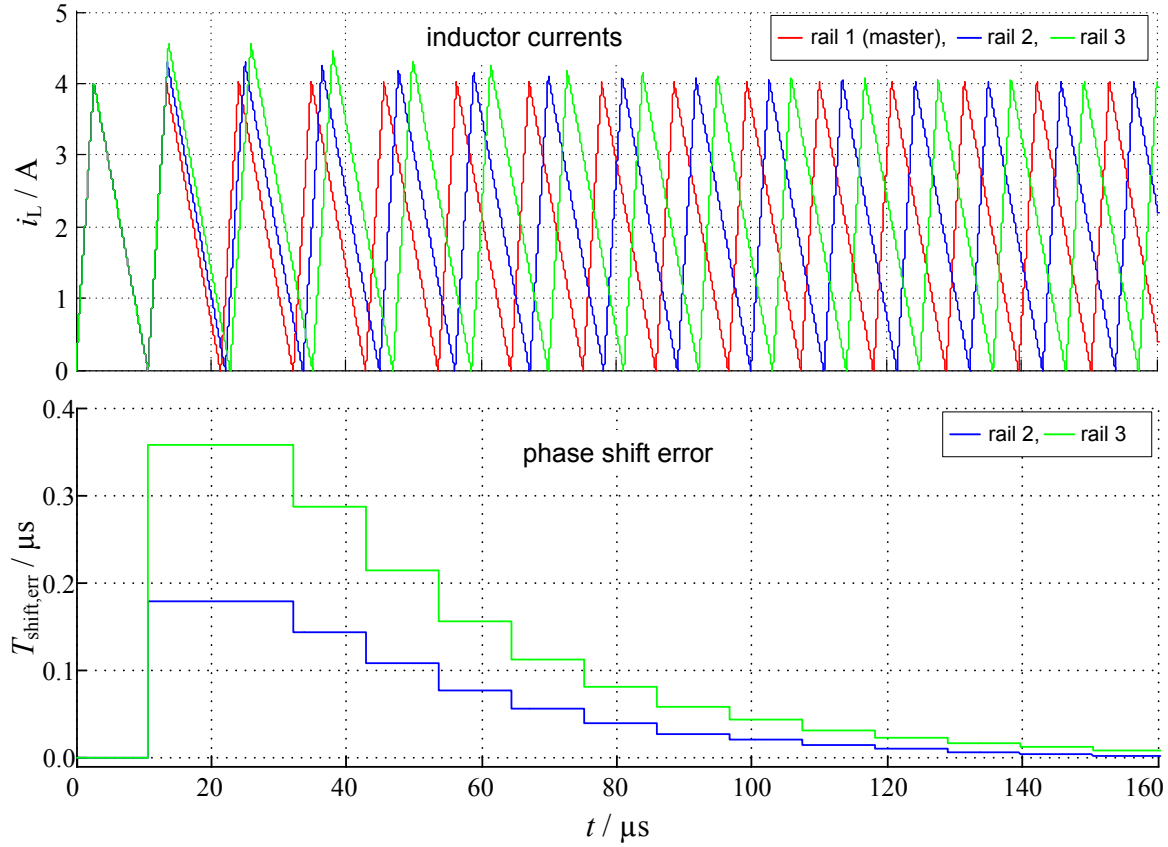

Figure 7.8: Phase shift control after common start

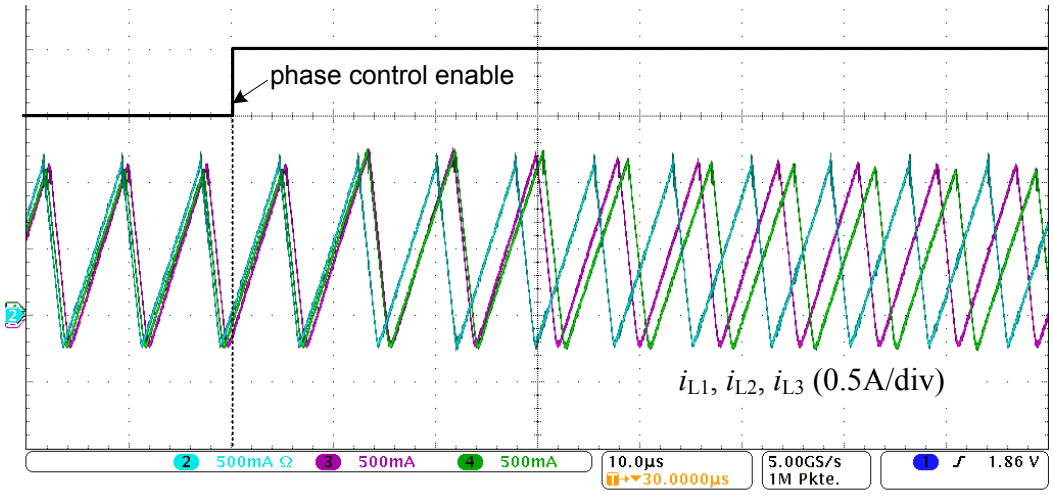

Figure 7.9: Transient response of the phase shift control
(channel 2 is master rail; $v_{in} = 100\text{V}$; $v_{out} = 400\text{V}$; $P_{out} = 130\text{W}$)

7.4 Switching Frequency Limitation

Another problem caused by the variable switching frequency in BCM is, that in some operating points the switching frequency increases to high values. Especially in the region of the line voltage zero crossing and at light load huge switching frequencies occur. For this reason a switching frequency limitation is strongly recommended. Two feasible methods are proposed in the following, which cause the converter to change to DCM, if the switching frequency surpasses set limits.

7.4.1 Frequency Limitation due to Bounded Switching Period

Method 1: Switch on after $T_{s,min}$, if ZCD signal is positive

Normally, each switching cycle starts with turning on the boost switch, if the ZCD signal is set. At the same time a counter whose final value equals the minimum valid period time $T_{s,min}$ is reset to zero. Only if the final counter value is reached, the ZCD signal is passed to trigger the next cycle. This is feasible, because after the current decayed to zero the inductor current oscillates with the parasitic capacitance of the boost switch. Accordingly, the ZCD signal occurs periodically until the next switch-on event.

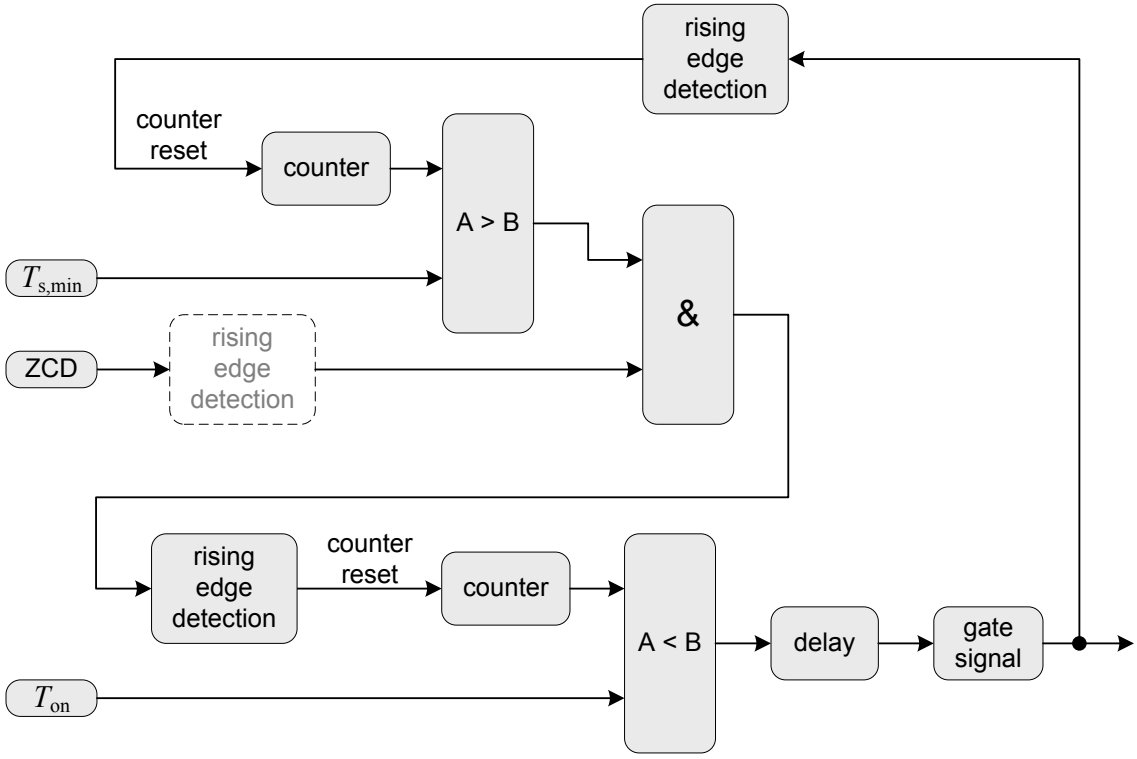

Figure 7.10: Structure of the pulse generation for BCM with frequency limitation (the dashed block is used for method 2)

To implement this method the origin pulse generation of Figure 7.4 was employed. The modified structure is depicted in Figure 7.10. But this method does not guarantee valley switching. If for example $T_{s,min}$ is reached near the end of the ZCD signal, the drain-source voltage v_{DS} is already growing and due to dead-time, which is implemented to achieve optimal valley switching during normal operation, a high v_{DS} can occur at the switch-on event (cf. Figure 7.11).

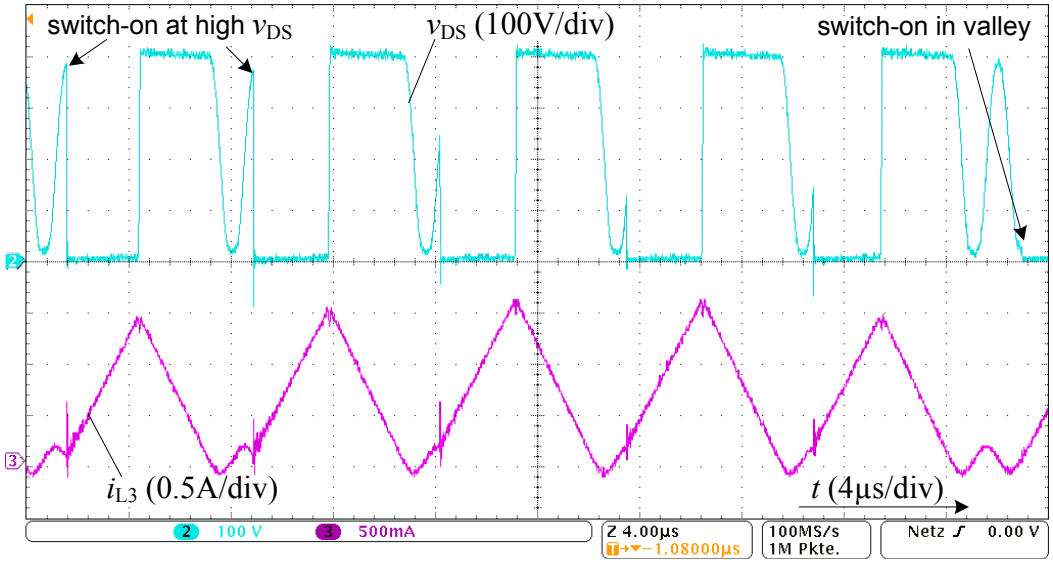

Figure 7.11: Changing switching conditions during frequency limitation

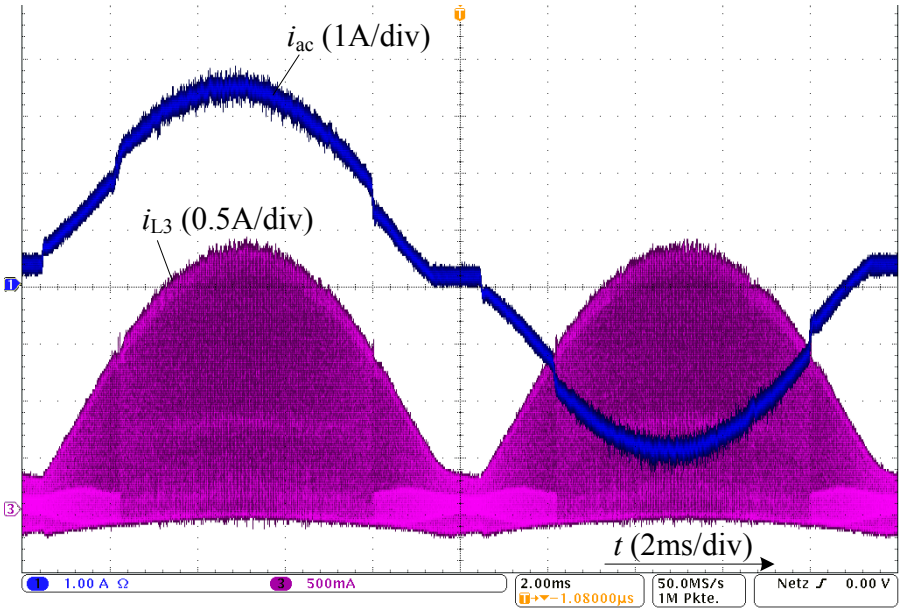

Figure 7.12: Measured line and inductor current with method 1

Another drawback occurs due to steps in the period time because of waiting for the ZCD signal of the next v_{DS} valley (cf. Figure 7.11). These steps cause interferences in the inductor average current and in the input current, consequently (cf. Figure 7.12). Additionally, the valley steps don't occur at the same time for all interleaved rails. This results in steps and therefore large errors in the phase shift. Due to this non-optimal interleaving also steps in the input current ripple occur. Because the $T_{s,min}$ value determines the period time, T_{adj} has no influence on the on-time anymore. Due to this fact the phase shift control does not work during frequency limitation.

Method 2: Switch on after $T_{s,min}$, if rising edge of ZCD signal occurs

Method 2 differs only little from method 1. Now, the switch-on is only performed at the rising edge of the ZCD signal. By doing so, optimal valley switching is achieved all the time (cf. Figure 7.13). But compared to method 1 the waiting time for the switch-on event can be significantly larger. Thus, the related drawbacks increase with method 2. This can be seen in the line current in Figure 7.14. Hence, by this method a higher efficiency is attained, but at the cost of a poorer power factor.

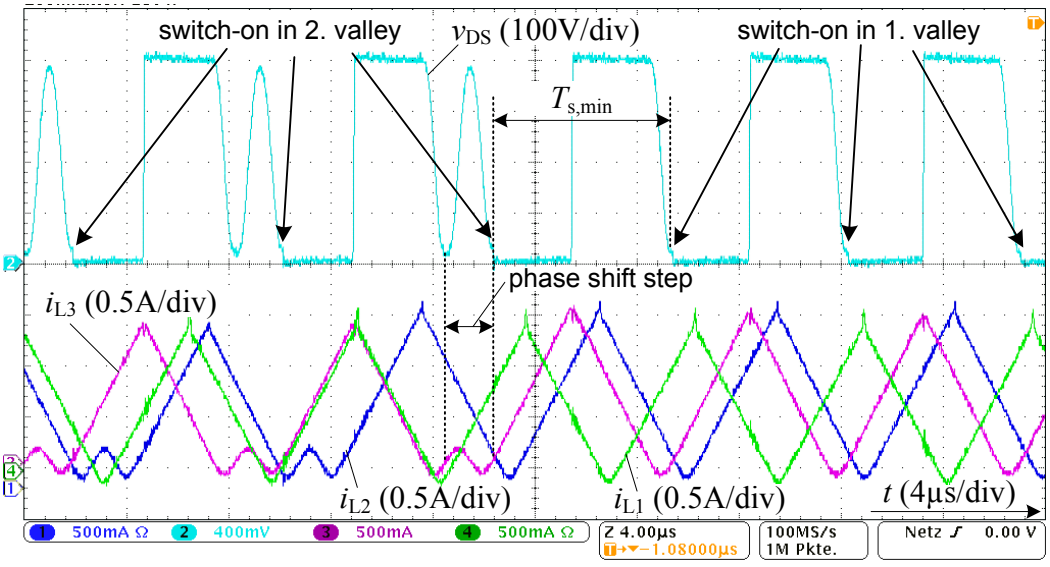

Figure 7.13: Phase shift step due to switching frequency limitation

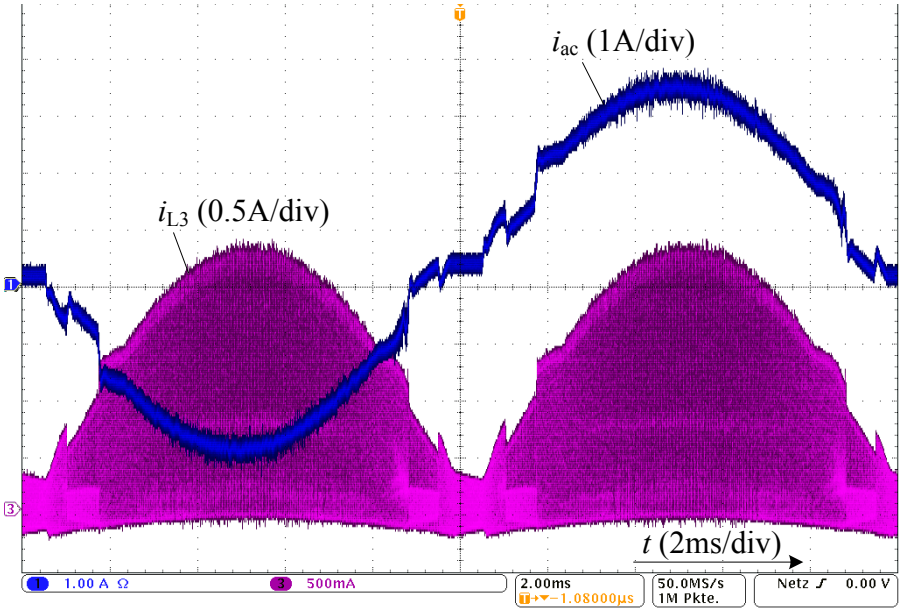

Figure 7.14: Measured line and inductor current with method 2

7.4.2 Frequency Limitation with Phase Shedding

For both described frequency limitation methods the main drawbacks result from improper phase shift in interleaved converters during the frequency limitation. To overcome this problem, it has to be ensured, that frequency limitation is only active in single-rail operation. This can be done by an appropriate phase shedding strategy.

It is well known, that with this method the number of energized converter rails is reduced with decreasing output power. To avoid frequency limitation the shutdown of one rail must occur before the frequency limit is reached.

In the following this method is described for a converter with the data of Table 7.1.

Number of rails	$n = 4$
Boost inductors	$L_1 = L_2 = L_3 = L_4 = 250\mu H$
Output voltage	$v_{out} = 400V$
Maximum RMS input voltage	$V_{in,max} = 265V$
Maximum output power	$P_{out,max} = 400W$ per rail

Table 7.1: Converter parameters

The shutdown of a rail is triggered, if the power for the remaining rails becomes 95% of the maximum power (380W). The critical operation points resulting to high switching frequency occur, if the power of each rail is low. Thus, the highest frequencies occur directly before another rail is to be shut down.

From Table 7.2 it can be seen, that the minimum rail power during interleaving occurs directly before single-rail operation. Hence, it has to be guaranteed that no frequency limitation appears above 190W rail power.

Transition	Power per rail before shutdown	Power per rail after shutdown
4 rails → 3 rails	285W	380W
3 rails → 2 rails	253W	380W
2 rails → 1 rails	190W	380W

Table 7.2: Transition levels for phase shedding

Since the maximum switching frequencies result at maximum input voltage, only the situation at $V_{in} = V_{in,max} = 265\text{V}$ is analyzed.

The resulting maximum switching frequency can be calculated with

$$f_s(\omega t) = \frac{v_{in}(v_{out} - v_{in})}{2\bar{i}_L L\, v_{out}} = \frac{V_{in}\sqrt{2}\sin(\omega t)\,(v_{out} - V_{in}\sqrt{2}\sin(\omega t))}{2v_{out} L\, P_{out}\sqrt{2}\sin(\omega t)\,/V_{in}}$$
$$= \frac{{V_{in}}^2(v_{out} - V_{in}\sqrt{2}\sin(\omega t))}{2v_{out}\, L\, P_{out}}. \tag{7.3}$$

By considering parasitic effects the switch on-time needs to be enlarged in the region of the line voltage zero crossing [Hub09]. Due to this behavior the maximum switching frequency occurs slightly before and after the zero crossing. Assumed is a line voltage phase angle of 20° respectively 160° for the largest switching frequency. Applying the values of this critical operating point, it follows

$$f_s(20°) = \frac{(265\text{V})^2(400\text{V} - 265\text{V}\sqrt{2}\sin(20°))}{2 \cdot 400\text{V}\ 250\mu\text{H}\ 190\text{W}} = 500\text{kHz}\,. \tag{7.4}$$

Thus, the maximum valid switching frequency needs to be set up to 500kHz. This is equivalent to a minimum switching period of $T_{s,min} = 2\mu\text{s}$.

In order to maintain optimal interleaving and to avoid disturbances in the input current it is advisable to perform phase shedding only at line voltage zero crossing.

7.5 Efficiency and Power Factor

Measured efficiencies are shown in Figure 7.15 at low and in Figure 7.16 at high line voltage. Separate measurements with single rail and 2 respectively 3 interleaved rails were performed. The maximum switching frequency was set to $f_{s,max} = 500\text{kHz}$ and the inductance value of all rails was $L = 400\mu\text{H}$. Only power levels with no switching frequency limitation were measured. From the separate curves an efficiency optimal phase shedding strategy can be easily derived.

Figure 7.17 illustrates that with the relative simple constant on-time control strategy very high power factors are attained in BCM.

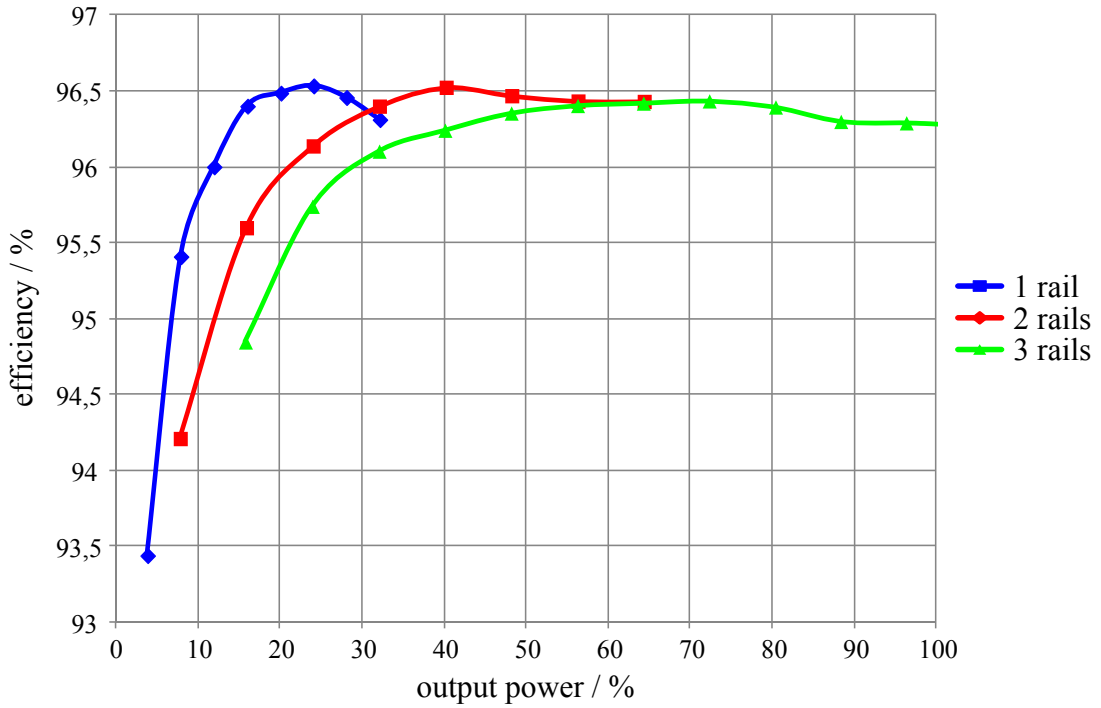

Figure 7.15: Efficiency curves at low line voltage with 1, 2 and 3 interleaved rails ($V_{ac} = 115\text{V}; v_{out} = 400\text{V}; P_{100\%} = 600\text{W}$)

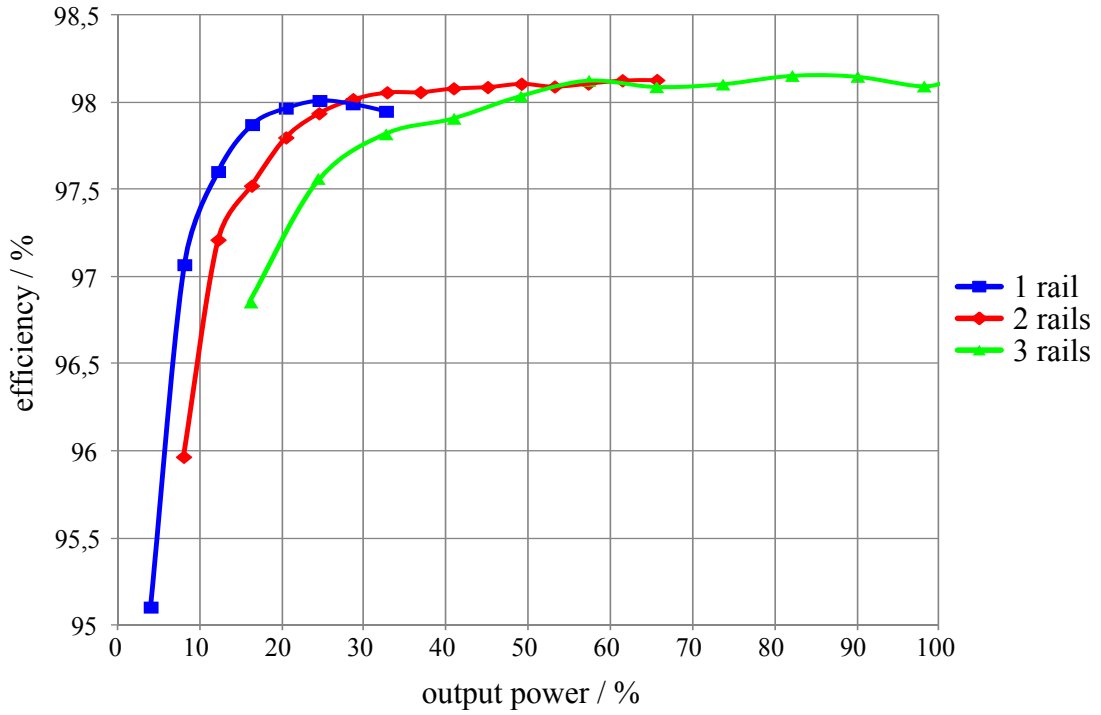

Figure 7.16: Efficiency curves at high line voltage with 1, 2 and 3 interleaved rails ($V_{ac} = 230\text{V}; v_{out} = 400\text{V}; P_{100\%} = 1200\text{W}$)

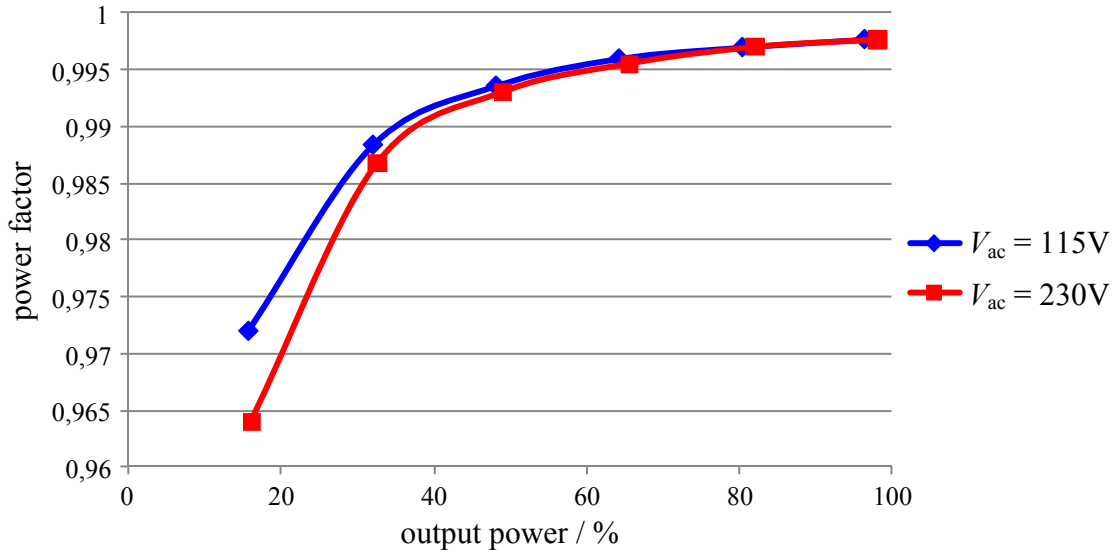

Figure 7.17: Measured power factor at high and low line voltage with 3 interleaved rails ($v_{out} = 400\text{V}; P_{100\%,low\ line} = 600\text{W}; P_{100\%,high\ line} = 1200\text{W}$)

7.6 Summary

The current control of PFC converters operated in BCM can be realized with little control effort. In order to achieve high power factors it suffices to turn on the boost switch for a constant duration, after the inductor current decayed to zero. High efficiency is attained due to the elimination of the reverse recovery losses of the boost diode and the reduction of the switching losses due to switching-on at zero voltage or in the voltage valley. By reason of the variable switching frequency specific phase shift control is required to ensure optimal interleaving. With the proposed digital phase shift controller multi-rail interleaving is achieved. By the use of an optimized phase shedding strategy frequency limitation only needs to be performed during single-rail operation. For this reason optimal interleaving and undisturbed average current is attained by keeping the switching frequency in the valid range. With well-directed phase shedding the efficiency can be optimized even at partial load.

8 Feed-Forward Control for BCM and DCM Operation

For the interleaved BCM control described in Chapter 7 extensive effort is required to detect the zero currents and provide optimal phase shifts. In order to bring down these extra costs a feed-forward algorithm for interleaved BCM is promising, which can handle multi-rail interleaving with relatively low computational effort [Gro11].

8.1 Feed-Forward Algorithm for BCM Operation

In BCM the peak inductor current is twice the average current and is determined by the input voltage v_{in}, the inductance value L and the switch on-time T_{on}:

$$\bar{i}_L = \frac{1}{2}\hat{\imath}_L = \frac{1}{2}\frac{v_{in}}{L}T_{on} \tag{8.1}$$

Thus, for n converter rails and a given average input current reference value i_{ref} the required on-time is

$$T_{on} = \frac{2L}{v_{in}}\frac{i_{ref}}{n}. \tag{8.2}$$

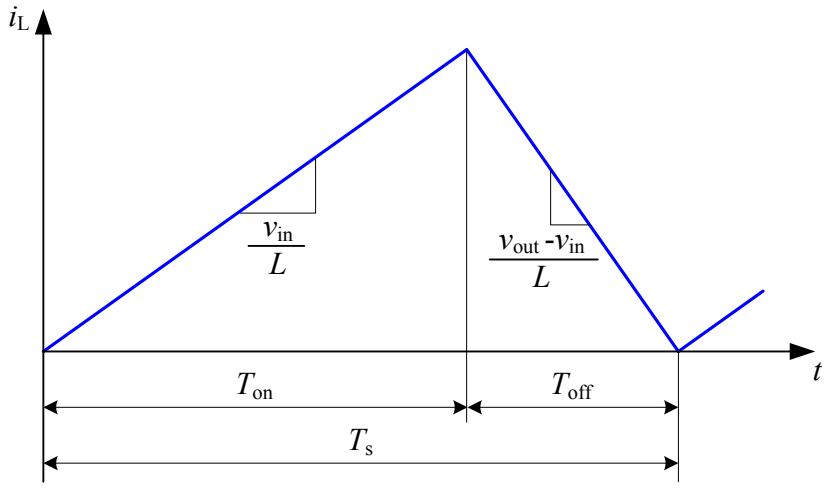

Figure 8.1: Inductor current in BCM

With the corresponding off-time

$$T_{off} = \frac{2L}{v_{out} - v_{in}}\frac{i_{ref}}{n} \tag{8.3}$$

the necessary switching period results as (cf. Figure 8.1)

$$T_s = T_{on} + T_{off} = \frac{2Li_{ref}}{n} \frac{v_{out}}{v_{in}(v_{out} - v_{in})}. \tag{8.4}$$

With the help of Eq. (8.2) T_s can be directly computed from T_{on}:

$$T_s = T_{on} \frac{v_{out}}{v_{out} - v_{in}} \tag{8.5}$$

Eq. (8.2) and Eq. (8.5) represent the complete current control law for the BCM. This control law can be easily implemented on a DSP or µC without any expensive calculations. In Figure 8.2 the control structure for a PFC rectifier with n interleaved rails is depicted.

The computed switching times are loaded into DPWM units of the controller to trigger the switching events.

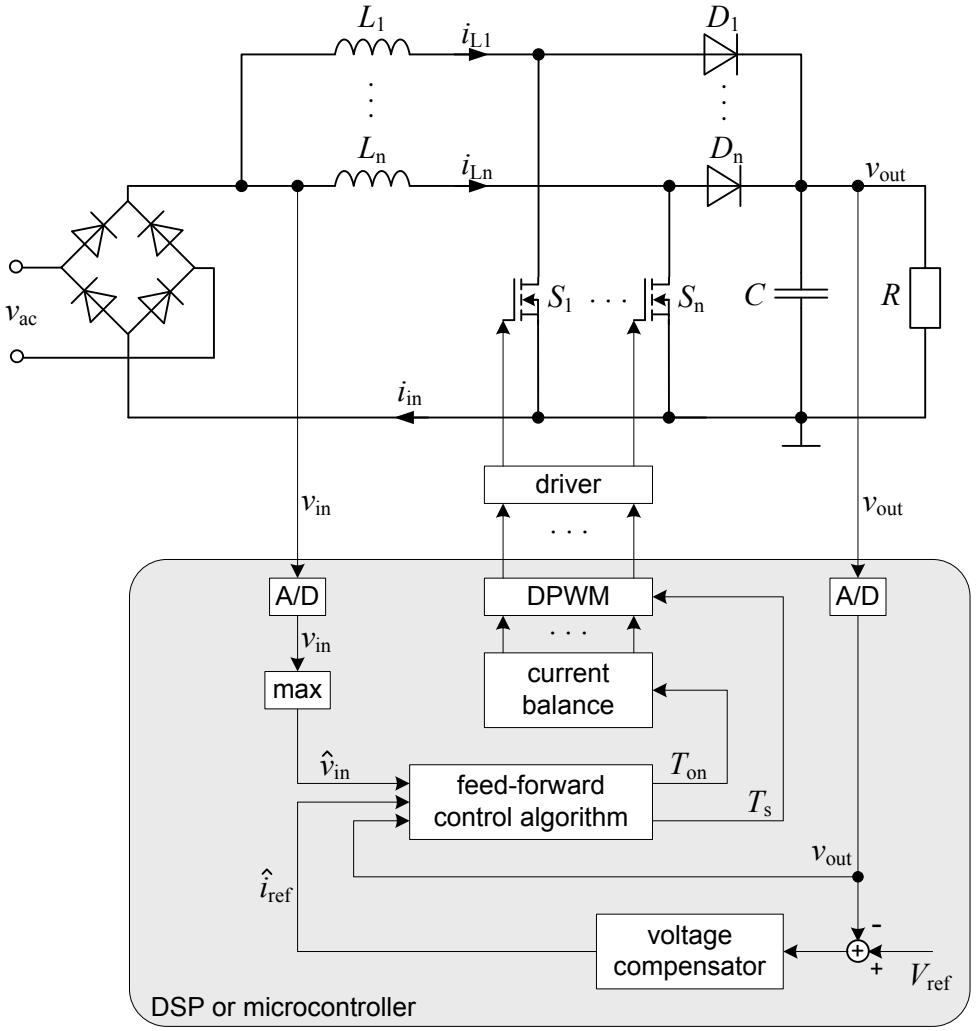

Figure 8.2: Control structure for the digital feed-forward BCM and DCM operation of multi-interleaved PFC converter

Since i_{ref} has the same sinusoidal shape as v_{in}, it follows from Eq. (8.2), that T_{on} is constant as long as the power demand does not change. Thus, it is not necessary to update the on-time for every switching cycle. Due to the relatively slow voltage controller, which generates the amplitude of the current reference value, it suffices to update the current amplitude and thus T_{on} only once in every line half-cycle.

Even though the calculation of T_{on} via Eq. (8.2) includes the inductance L, an exact knowledge of this value is not essential for BCM operation. Due to the fact that T_{on} is used to compute T_s, BCM operation only depends on v_{in} and v_{out}. A deviation in the inductance value would only cause a deviation in the inductor average current value and such an error would be compensated by the voltage controller. Furthermore, the calculation of Eq. (8.2) could be completely omitted, if the voltage controller directly determines T_{on}. But at least it is advisable to retain a division by the input voltage peak value to gain an input power feed-forward control.

8.2 Extension into DCM operation

Since there is no feedback of the zero current event, entering CCM could occur and could cause harmful overcurrent. Hence, it is advisable to move slightly into DCM to avoid CCM under all conditions. DCM operation can be attained by enlarging the switching period. From the BCM control of Chapter 7 it is already known, that a small extension of the switching period could also be beneficial for ZVS or near ZVS, if the switch-on instant is delayed until the occurrence of the first valley of the oscillating drain-source voltage.

For changing into DCM, a DCM ratio $K_{lag} \geq 1$ is introduced (cf. Figure 8.3). The period value for BCM is multiplied by the square of K_{lag} to get the enlarged DCM switching period

$$T_s' = T_s K_{lag}^2 \,. \tag{8.6}$$

In order to retain the same average current also during DCM, the on-time also needs to be modified. It results as

$$T_{on}' = \sqrt{\frac{2Li_{ref}(v_{out} - v_{in})}{n \cdot v_{in}\, v_{out}} T_s'} \,. \tag{8.7}$$

By substituting Eq. (8.2), (8.5) and Eq. (8.6) in Eq. (8.7), the equation for the required on-time simplifies to

$$T_{on}' = T_{on} K_{lag}. \tag{8.8}$$

Using the enlarged on-time, the enlarged switching period can be calculated as

$$T_s' = T_{on}' \frac{v_{out}}{v_{out} - v_{in}} K_{lag}. \tag{8.9}$$

Hence, Eq. (8.8) and Eq. (8.9) represent the control algorithm for DCM. Computation of any square root operation is not required. The inductor current waveform at DCM is shown in Figure 8.3.

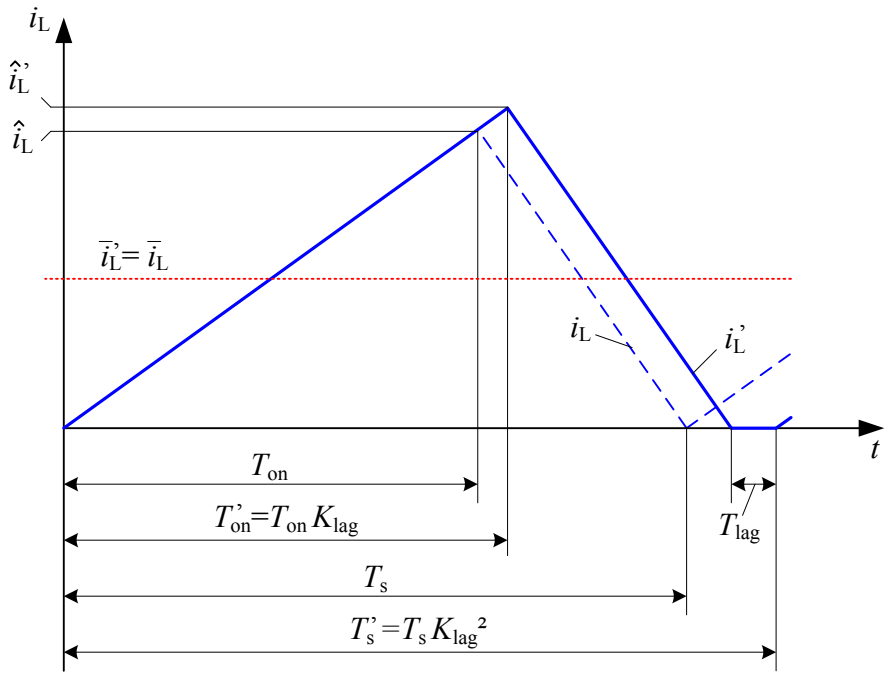

Figure 8.3: Inductor current shapes with DCM and BCM

8.3 Closed-Loop Control Strategy

8.3.1 Closed-Loop Control Structure

So far the switch on-time is determined by the feed-forward algorithm or can be obtained directly from the voltage controller. For this open-loop realization no current measurement is needed (cf. Figure 8.2). In an ideal converter without any losses or parasitic effects this suffices to achieve an ideal sinusoidal input current shape. However, deviations in the current shape result in a real converter. Thus, in order to achieve an optimal power factor under all conditions an additional current controller can be applied.

For this closed-loop implementation measurement of the input current is required, which can be realized with a single common shunt sensor. In Figure 8.4 the control structure with closed current loop is shown. The voltage controller determines the current reference peak value, which is divided by the normalized input voltage to get the sinusoidal input current reference. The deviation in the input current is passed to the current controller. Now T_{on} is

the global on-time and is generated by adding the controller output value $T_{on,adj}$ to the feedforward value $T_{on,ff}$ computed with Eq. (8.2):

$$T_{on} = T_{on,adj} + T_{on,ff} \tag{8.10}$$

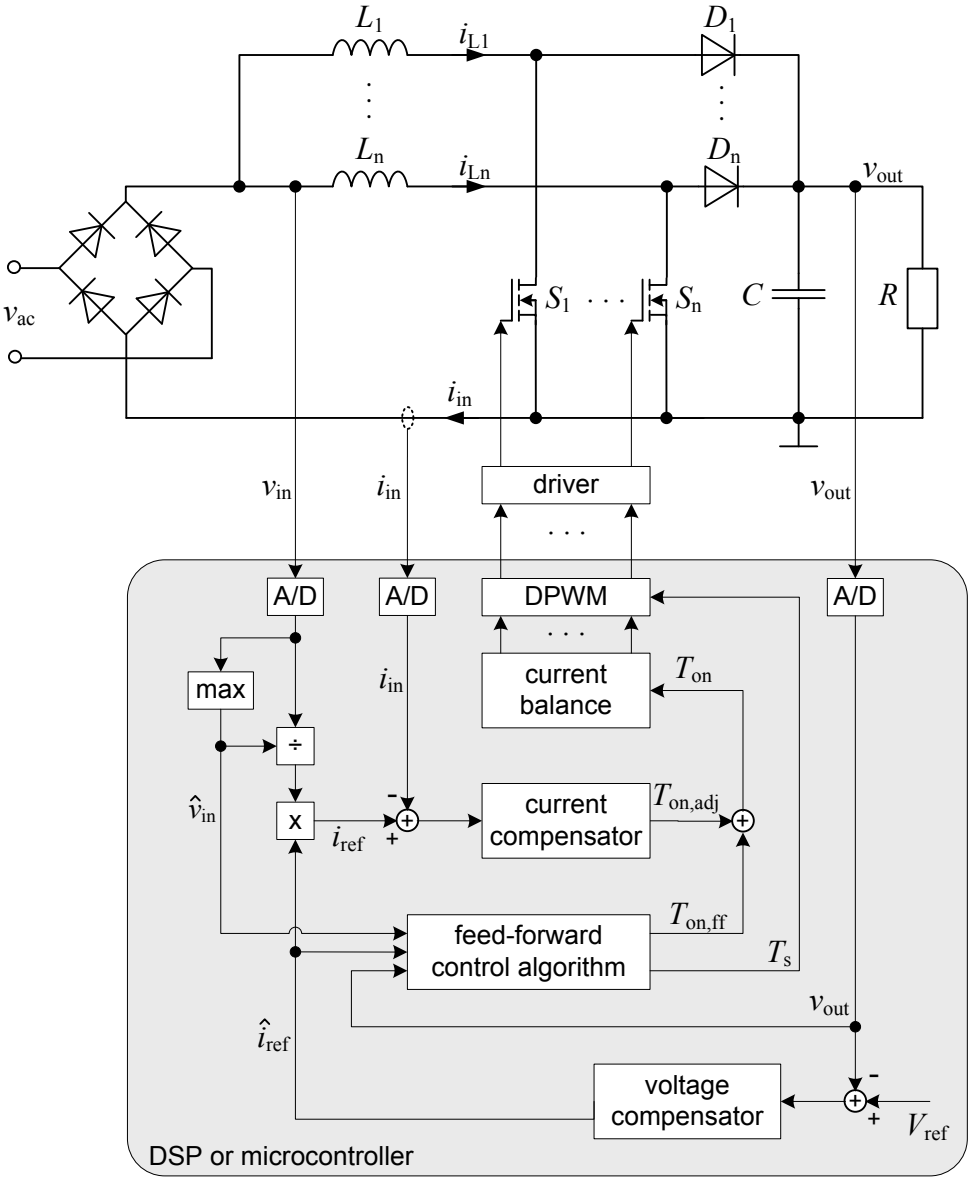

Figure 8.4: Closed loop control structure for the digital BCM and DCM operation of multi-interleaved PFC converter

With the DCM ratio it follows

$$T'_{on} = (T_{on,adj} + T_{on,ff})K_{lag}. \tag{8.11}$$

This value is used to compute the switching period with Eq. (8.9).

8.3.2 Transfer Function and Controller Design

In Section 2.4.3 the transfer function of the boost converter in DCM was derived. As the actuating variable the duty-ratio was utilized and the switching frequency was assumed to be constant. Due to the non linear behavior the transfer characteristic changes with the operating point and complicates the controller design.

Utilizing the feed-forward control strategy with variable switching frequency and the switch on-time as the actuating variable, a very simple linear system results.

The control-to-inductor-current transfer function for one rail operated in BCM can be directly derived from Eq. (8.1):

$$G_{i,BCM}(s) = \frac{\bar{i}_L}{T_{on}} = \frac{v_{in}}{2L} \tag{8.12}$$

This transfer function exhibits pure proportional behavior. Due to the variable switching frequency a variation in the resulting dead-time has to be considered in a digital control structure.

Considering n parallel rails and shifting into DCM by applying the ratio K_{lag}, the control-to-inductor-current transfer function becomes

$$G'_{i,BCM}(s) = \frac{\bar{i}_{in}}{T'_{on}} = \frac{n\, v_{in}}{2LK_{lag}}. \tag{8.13}$$

This indicates also a simple proportional behavior in DCM. But there are two aspects which have to be considered:

- By enlarging the switching period with K_{lag}, the dead-time in the digital control loop increases, respectively.
- Due to the sinusoidally varying input voltage v_{in} and the ratio K_{lag} the loop gain can vary significantly.

Thus, the dynamic of the system varies and complicates the controller design. Especially due to the large range of v_{in} a current controller with invariant parameters is unfeasible. An adaptive controller is required to compensate the variations in v_{in} and K_{lag}. Because these values are captured in the system, they can directly be used for an adaptive controller gain

$$K_a = \frac{K_{lag}}{v_{in}}, \tag{8.14}$$

which needs to be updated continuously. Since the control path offers pure proportional behavior, a simple integrating controller can be applied. The current controller transfer function can be expressed as

$$G_{cc}(s) = K_a \frac{K_r \omega_c}{s}, \tag{8.15}$$

with the crossover angular frequency ω_c and the constant controller gain

$$K_r = \frac{2L}{n}. \tag{8.16}$$

Considering the dead-time T_d, the open loop transfer function results to

$$G_o(s) = G'_{i,BCM}(s) G_{cc}(s) e^{-sT_d} = \frac{\omega_c}{s} e^{-sT_d}. \tag{8.17}$$

The dead-time in the control loop is not only introduced by the DCM ratio K_{lag}, but also influenced by the kind of implementation.

It has been mentioned, that for closed loop implementation the input current needs to be measured. However, there is still a significant ripple in the input current and the instants for directly sampling the average current values are not known and could only be computed with unreasonable effort. Hence, a regular sampling method is unsuitable for this application. But an oversampling with digital filtering or an additional analog filter can be utilized with little effort. The transfer function of such a low-pass filter has to be considered for the controller design.

8.4 Current Balancing

Because the inductor currents in BCM and DCM reset to zero in every switching cycle, there is no risk that a huge unbalance in the inductor currents occurs. However, due to tolerances in mass production the inductance value of each sample differs. This results in different inductor current slopes and consequently in a rail current mismatch of paralleled converters. Applying the same on-time for all inductors would result also in equal off-times and therefore collective BCM operation (cf. Figure 8.5 a)), or equal DCM ratios, respectively. In this case the current difference corresponds with the inductance mismatch.

In some applications or operating points it can be necessary to ensure identical rail average or rail peak currents. In such a case current balancing is required.

8.4.1 Balancing to Identical Average or Peak Currents

For a beat frequency-free interleaving all rails have to be operated with equal switching periods T_s. In order to obtain equal average or peak currents an individual on-time for every rail needs to be applied. For this purpose the rail with the largest inductance becomes master rail, which determines the master on-time $T_{on,m}$ and the global T_s. A balancing factor $K_b \leq 1$ is introduced to compute the individual on-time $T_{on,k}$ for each slave rail k with

$$T_{on,k} = T_{on,m}\, K_{bk}. \tag{8.18}$$

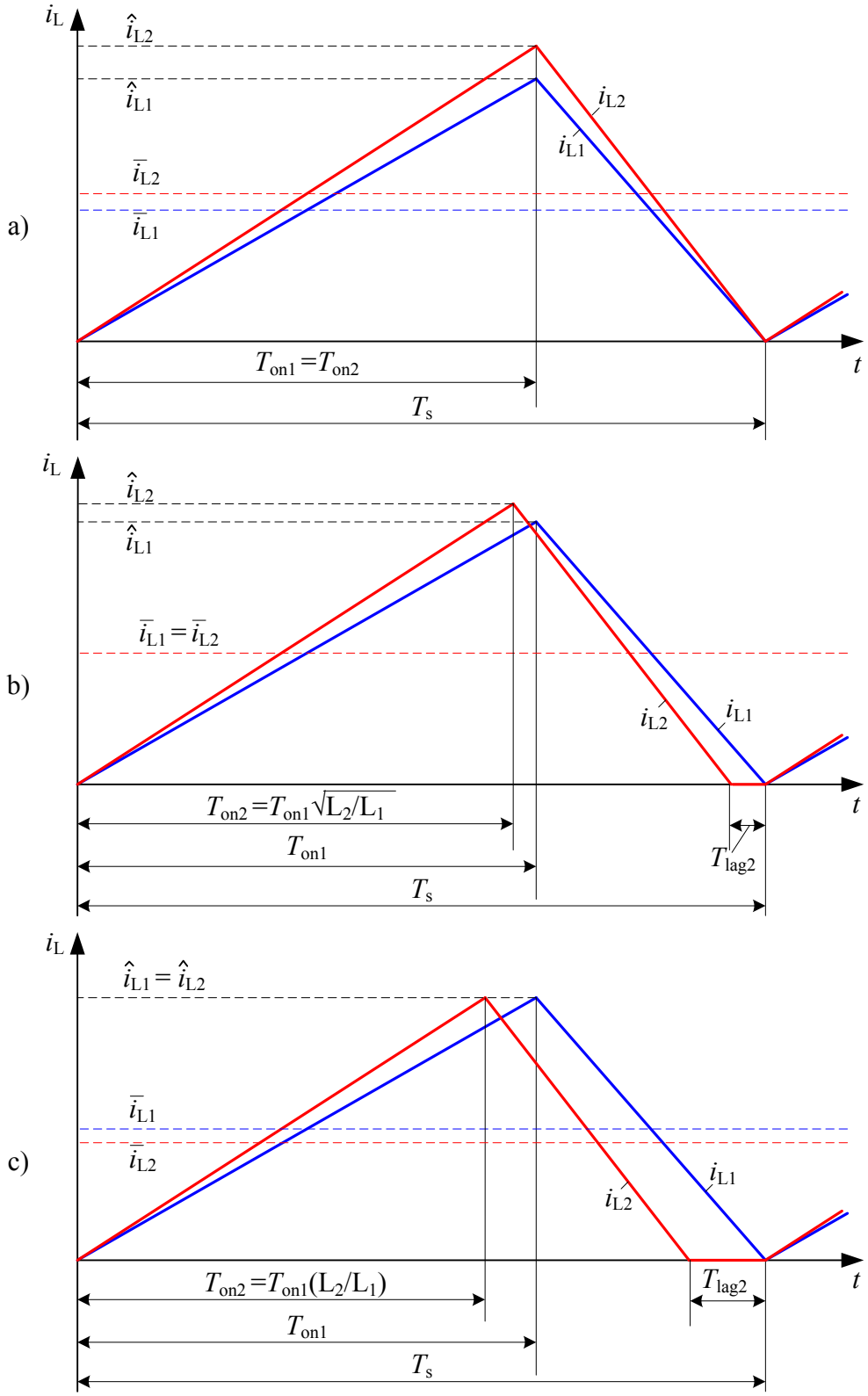

Figure 8.5: Inductor current waveforms for different inductance values ($L_1 > L_2$).
a) without current balancing
b) with average current balancing
c) with peak current balancing

In the example of Figure 8.5 with two rails, L_1 is larger than L_2 and becomes master ($L_m = L_1$), respectively. To achieve equal average currents (cf. Figure 8.5 b)) the on-time for the slave rail with inductance $L_k = L_2$ is calculated by multiplying the master on-time with the square-root of the inductance ratio [ScGr10, Gro11]. Thus, the balancing factor is

$$K_{b2} = \sqrt{\frac{L_k}{L_m}}. \tag{8.19}$$

For equal peak currents (cf. Figure 8.5 c)) the balancing factor must be set to the inductance ratio

$$K_{b2} = \frac{L_k}{L_m}. \tag{8.20}$$

The determination of the inductor values and the calculation of the correction factors are required only once and can be done during an initial calibration sequence before the regular operation starts. Such a calibration sequence is described in the next section.

8.4.2 Initial Calibration Sequence for Inductance Identification

In order to balance the rail currents to equal average or peak values, the ratios of the inductances are required. Also the largest inductance needs to be indentified for this purpose. As mentioned, the exact knowledge of the inductance values is not essential for a reliable BCM or DCM operation, but it is beneficial for current limitation.

To identify the inductance values and to calculate the ratios, an initial calibration sequence is utilized. This sequence is executed at the beginning of the soft-start process, when the output capacitor is charged to the peak value of the input voltage.

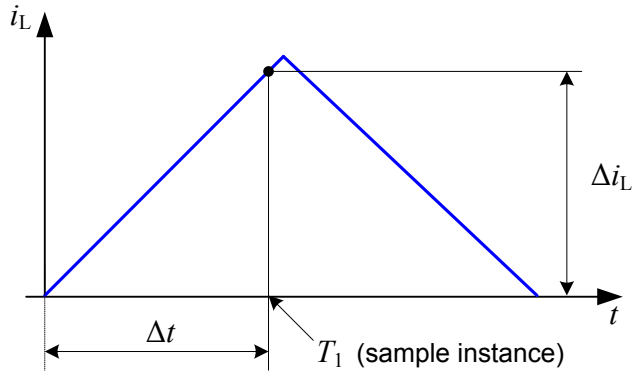

Figure 8.6: Defined current sample to identify inductance value

In order to identify an inductance value, current pulses with a defined on-time are applied. After a specified duration Δt the inductor current and input voltage are measured (cf. Figure 8.6). With this sampled values the inductance value is computed by

$$L_x = \frac{v_{in}\,\Delta t}{\Delta i_L} = \frac{v_{in}(T_1)\,T_1}{i_L(T_1)}. \tag{8.21}$$

Due to the fact that only the total input current is measured, only the inductance value of one rail can be identified at a time. Thus, the values are determined one after the other, each in a separate line half-cycle. To ensure sufficient voltage drop across the inductance during the turn-off time, the identifying process is performed at approx. 75% of the input voltage peak value (cf. Figure 8.7).

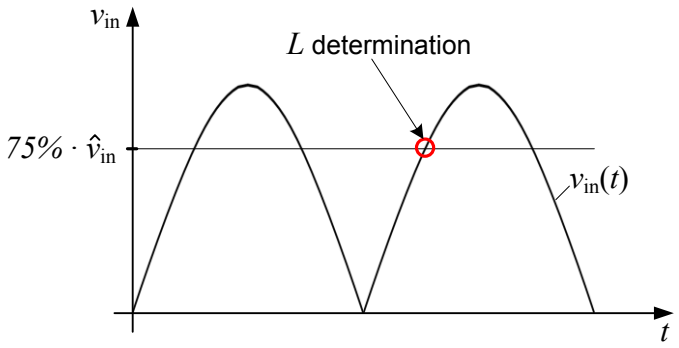

Figure 8.7: Operation point within the line cycle for identifying one inductance

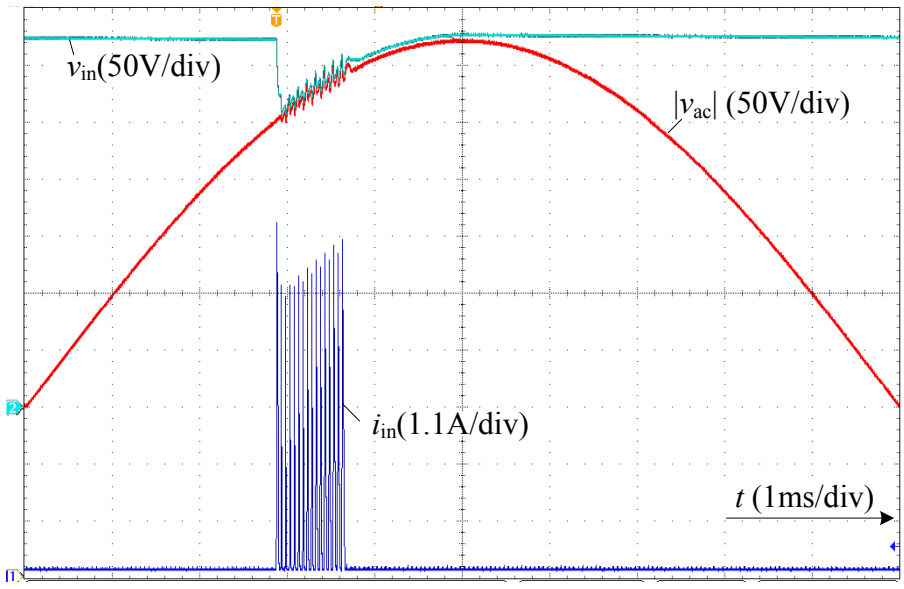

Figure 8.8: Initializing process for one inductor

Because typically an input capacitor is placed behind the diode-rectifier, the input voltage is equal to the output voltage at no load. Thus, at the beginning of the calibration sequence the input capacitor needs to be discharged down to the input voltage. Therefore 16 current pulses are generated. The first pulses should only ensure, that the input capacitor voltage is equal to the input voltage and only the last four pulses are evaluated for the inductance

identification. This process is shown in Figure 8.8 for one inductor and in Figure 8.9 for the whole calibration procedure of the prototype with three parallel converters. With looking at the current pulses in Figure 8.9, it is striking, that there are different peak currents in every line half-cycle. This already indicates different inductance values in each converter rail.

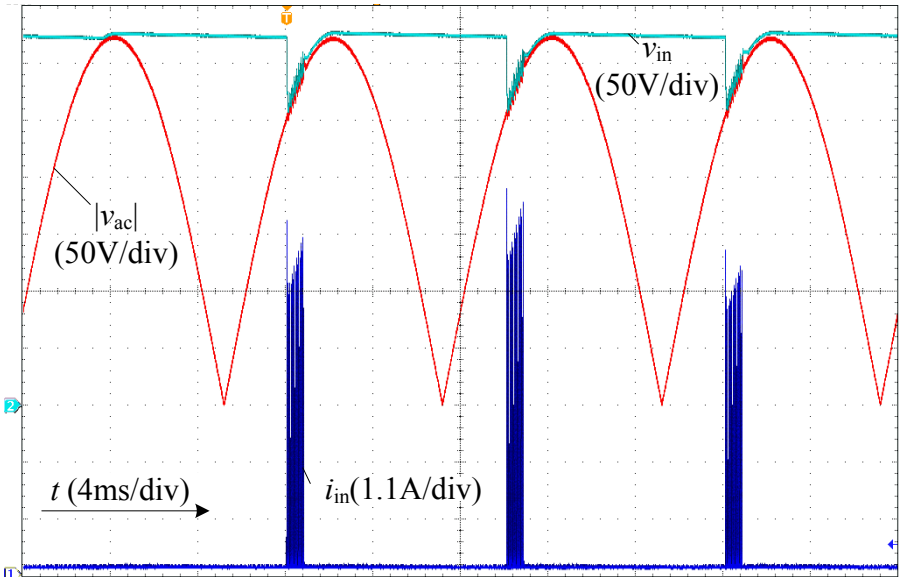

Figure 8.9: Complete calibration process

The calibration was performed at different input voltages while the on-time was kept constant. As can be seen in Figure 8.10 the determined inductance values decrease at higher input voltages. Because the on-time is the same for all input voltages, the current peaks are higher at higher input voltage. Due to saturation effects the inductance values reduce at higher currents. This characteristic results in lower inductance values at higher input voltage.

From the inductance values at different input voltages the average values have been calculated and are given in Table 8.1. Also the values measured with an impedance analyzer are shown. The resulting deviations are given in the last column.

	average value calibration sequence	measured with impedance analyzer	rel. deviation
L_1	183.3 µH	180 µH	1.8%
L_2	168.0 µH	166 µH	1.2%
L_3	198.7 µH	197 µH	0.9%

Table 8.1: Prototype inductance values

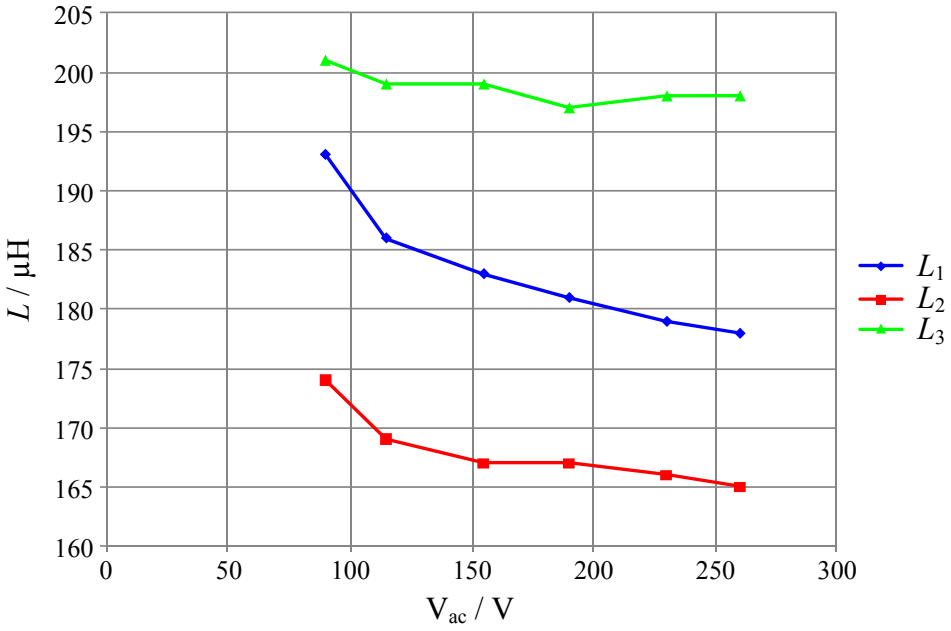

Figure 8.10: Determined inductance values vs. input voltage

With deviations below 2% an adequate accuracy can be attained. For a series production device the deviation could be expected a few percent higher. This is because of the good knowledge of the measurement scaling of the used prototype.

8.5 Phase Shedding

The benefit of adjusting the number of energized rails in order to enhance the efficiency at partial load has already been shown in Section 7.5. Usually this phase shedding method is applied based on the load conditions. However, in a PFC application, there is a continuing variation in the input power within every line half-cycle, for which reason phase shedding based on the instantaneous input power is promising. By changing the number of energized rails the average input current has to be allocated and results in a current reference step for every single rail. Since the inductor current in BCM and DCM is reset in every switching cycle, and a current reference step can be compensated within one switching cycle with the proposed control strategy, phase shedding can be performed at any time. Additionally, a inductor current variation results in a change of the switching period. This property can be utilized to limit the switching frequency.

8.5.1 Common Discrete Phase Shedding

In general the levels of phase shedding are limited by the discrete number of interleaved rails. For example in a converter with $n = 3$ parallel rails there are 3 discrete interleaving modes (3 rails, 2 rails and single rail).

With the introduced feed-forward control algorithm the adjustment of the average input current is performed by tracking the on-time, which is proportional to the inductor current:

$$T_{on,PS} = \frac{n}{k}\frac{2L}{v_{in}}\frac{i_{ref}}{n} = \frac{n}{k}T_{on} \tag{8.22}$$

Where k is the integer number of energized rails. For the corresponding switching period it follows

$$T_{s,PS} = \frac{n}{k}T_{on}\frac{v_{out}}{v_{out} - v_{in}} = \frac{n}{k}T_s\,. \tag{8.23}$$

Hence, with phase shedding the switching frequency in each remaining rail changes with the factor k/n. Furthermore, the number of energized rails where switching events occur, changes to k, so that the effective switching frequency seen by the EMI filter changes by the square of k and can be represented as

$$f_{s,total} = \frac{k^2}{n}\frac{1}{T_s}. \tag{8.24}$$

To retain optimal interleaving also the delay time of the phase shift needs to be adjusted. The phase shift delay is given by

$$T_{shift,PS} = \frac{T_{s,PS}}{k}. \tag{8.25}$$

Shapes of the input and the inductor currents in BCM during a phase shedding process from 3 to 2 active rails are shown in Figure 8.11 a). Due to the on-time adjustment with Eq. (8.22) the average input current is kept constant. The fundamental frequency of the input current is reduced by 55.5%.

8.5.2 Continuous Phase Shedding

The principle of the common discrete phase shedding is, that an integer number of converter rails are completely turned off, while the remaining rails transfer the energy. The idea of continuous phase shedding is to give every single rail a section within the switching period where no energy is transferred, i.e. all rails keep running with a required DCM ratio. For this purpose the factor K_{lag} is utilized to implement the needed DCM ratio. In order to achieve equal circumstances as compared to discrete phase shedding, K_{lag} needs to be calculated as

$$K_{lag} = \frac{n}{k}, \tag{8.26}$$

where k represents the comparable number of active rails of the discrete phase shedding method operated in BCM. However, since $K_{lag} \geq 1$ is the range for DCM operation, k is no

longer limited to integer values, but rather can be every fractional value in the range $n \geq k > 0$. This enables a continuous change for the effective number of energized rails. The on-time and switching period are calculated using Eq. (8.8) and Eq. (8.9). The resulting effective switching frequency

$$f_{s,total} = \frac{n}{T_s K_{lag}^2} = \frac{k^2}{n} \frac{1}{T_s} \tag{8.27}$$

is identical to the result from discrete phase shedding in Eq. (8.24).

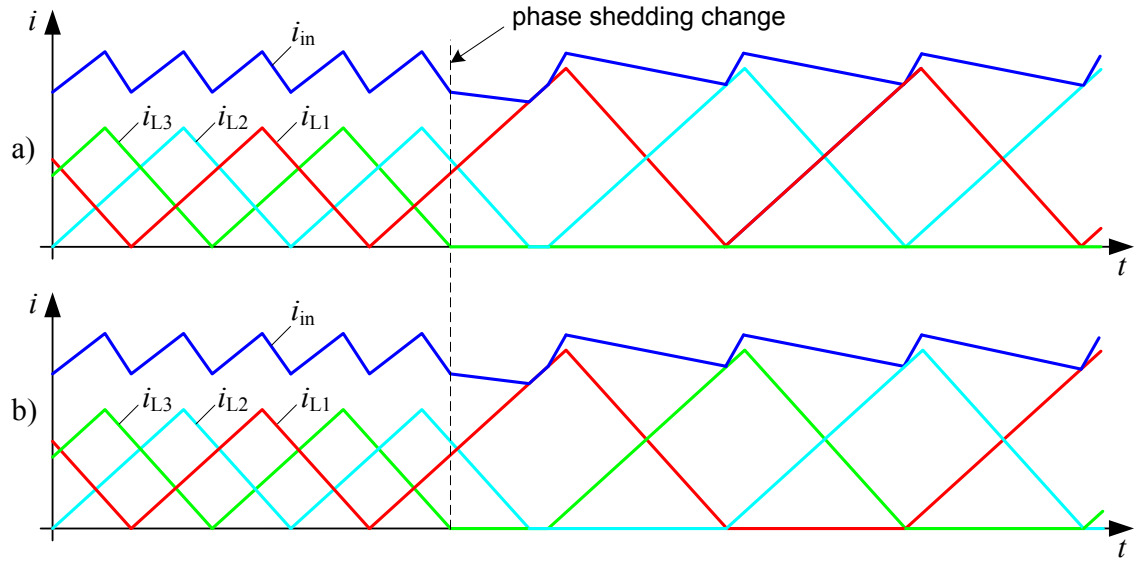

Figure 8.11: Total input current and inductor currents in principle during phase shedding from 3 to 2 rail operation at $D = 0.55$ with
a) conventional discrete phase shedding method
b) continuous phase shedding method

The current shapes during continuous phase shedding from $k = 3.0$ to $k = 2.0$ are illustrated in Figure 8.11 b). By comparing the current shapes of Figure 8.11 a) and b) it is obvious that both phase shedding methods result in equal switching instants and input current shapes. This circumstance can easily be verified via measurement on a real converter with the described DCM control strategy (cf. Figure 8.12).

All parallel converters should get equal load stress during their lifetime. With continuous phase shedding, where all converters keep running with equal DCM ratios, an equal load stress is inherent. However, with discrete phase shedding this request is not met naturally. An adequate rail management is required to equally spread the load stress during lifetime.

One drawback of continuous phase shedding are increased losses, because optimal turn-off in the first valley of the oscillating drain-source voltage cannot be achieved in DCM, while with conventional phase shedding the converter can be operated in BCM with valley switching.

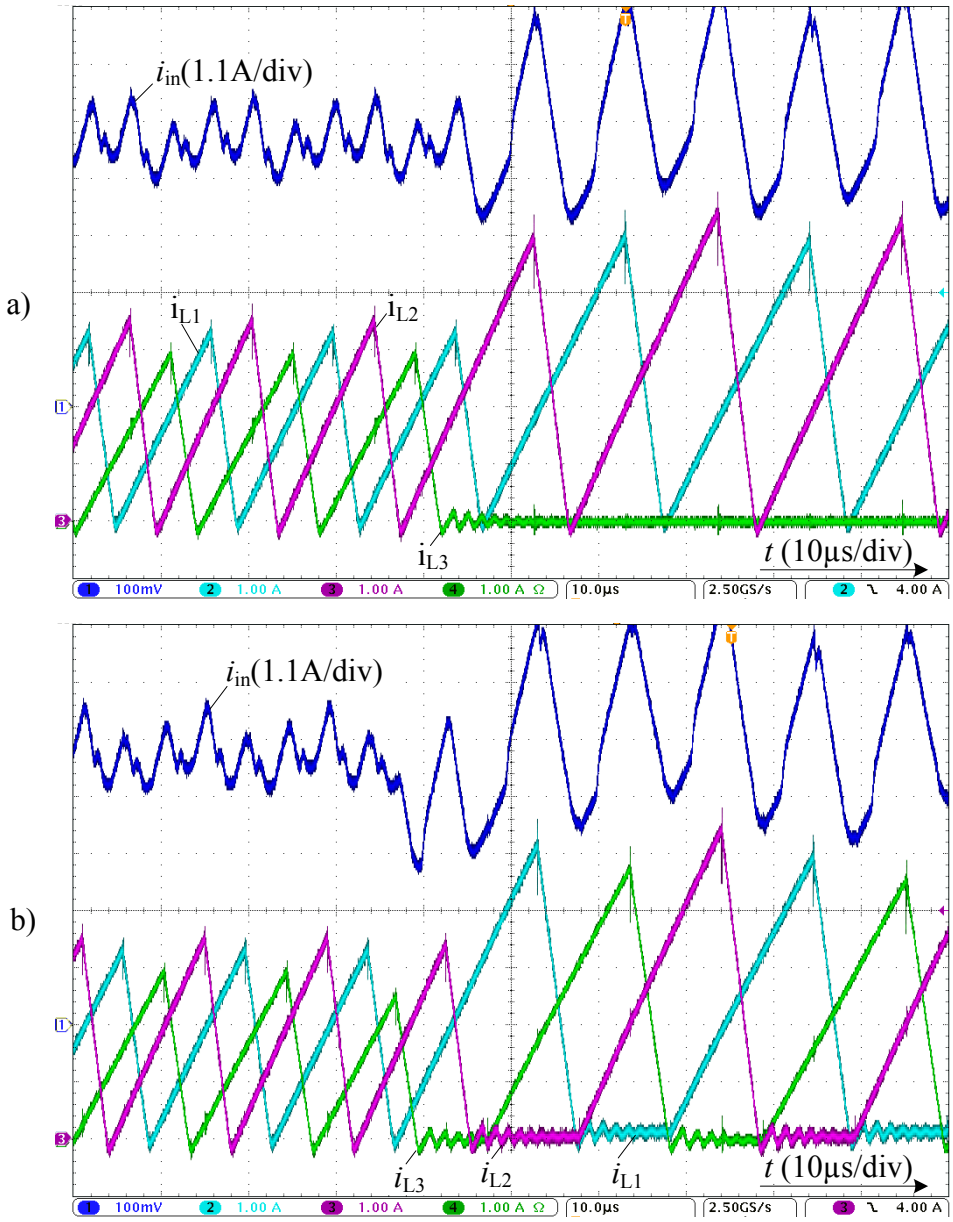

Figure 8.12: Total input current and inductor currents measured during phase shedding from 3 to 2 rail operation
a) conventional discrete phase shedding
b) continuous phase shedding

8.5.3 Switching Frequency Limitation

Due to the implementation of the control algorithms on a standard DSP or µC, the maximum sampling and switching frequency is limited. Thus, for practical use of the control concept a switching frequency limitation is required. Considering the frequency decreasing property of phase shedding (cf. Eq. (8.27)) such a feature can be implemented, which keeps the switching frequency in a desired range. For this purpose the factor k is decremented by a specified step size Δk, if the upper frequency limit is exceeded. When reaching the lower frequency threshold, k is increased, where the maximum value of k is n.

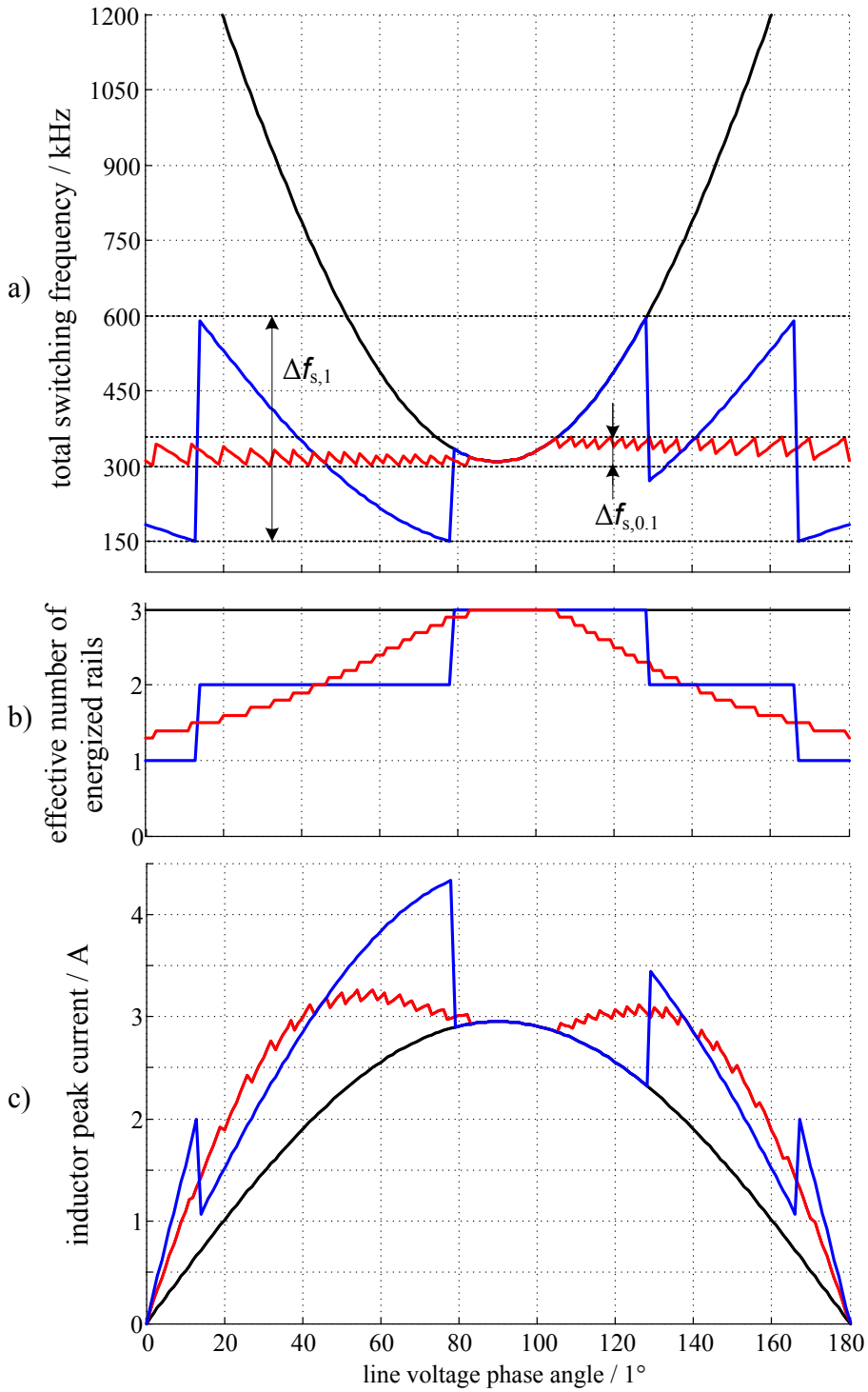

Figure 8.13: a) Total switching frequency,
b) effective number of energized converter rails k and
c) inductor peak current without phase shedding (black),
with conventional discrete phase shedding (blue) and with continuous phase shedding and step size of $\Delta k = 0.1$ *(red)*
($n = 3, v_{out} = 400\text{V}, V_{ac} = 230\text{V}$ *AC,* $P_{out} = 720\text{W}$*,* $L = 200\mu\text{H}$*)*

The curves of the total switching frequency for three parallel converters without phase shedding in BCM, with discrete phase shedding (i.e. $\Delta k = 1$) and for continuous phase shedding with $\Delta k = 0.1$ are illustrated in Figure 8.13 a) for one line half-cycle. The corresponding preset values of k are given in Figure 8.13 b). It can be seen, that without phase shedding very high frequencies occur. Also with discrete phase shedding a wide frequency range results. Additionally the switching frequency changes with high steps. This causes high steps in the inductor peak currents (cf. Figure 8.13 c)), which are not acceptable in PFC applications. Furthermore, due to the related step in the phase shift additional undesired current peaks can occur during discrete phase shedding. All this drawbacks can be eliminated by applying continuous phase shedding with an appropriate step size Δk. The switching frequency can be kept in a small band and changes only with small steps. Accordingly, the inductor currents and the phase shift delay changes only slightly.

Considering the converter efficiency, it can be seen in Figure 8.13 c), that by reducing the number of energized rails the peak currents and accordingly the RMS currents increase and cause higher ohmic losses. However, this effect is more than compensated due to less switching events and thus reduced switching losses.

8.6 Harmonic Reduction in Interleaved DCM PFC Rectifiers

It was already mentioned, that one major reason for interleaving several converters is the significant reduction of the input current ripple and the THD. The gain of improvement depends on the number of interleaved rails and the duty-ratio [Lou06]. At particular duty-ratios d the harmonics are totally eliminated, e.g. at two interleaved rails with $d = 0.5$ or with $d = 1/3$ or $d = 2/3$ at three interleaved rails. Thus, there is the potential to further reduce or to eliminate the input current ripple by changing the number of interleaved rails depending on the duty-ratio.

For this purpose a control law was developed, which minimizes the input current ripple and respectively the THD by utilizing the phase shedding method to adjust the number of interleaved rails [Gro12]. The definition of the THD is given in Appendix A.1. In DCM there is a direct link between the current ripple and the average value. For that reason a $\mathrm{THD_{DC}}$ is introduced for the following investigations, which is defined as the ratio of the the geometric sum of the harmonic components to the DC component:

$$\mathrm{THD}_{DC} = \frac{\sqrt{\sum_{n=1}^{\infty} I_n^2}}{\bar{i}_{in}} = \frac{\sqrt{I_1^2 + I_2^2 + I_3^2 + \cdots + I_n^2}}{\bar{i}_{in}} \tag{8.28}$$

Investigated is a converter with up to $n = 4$ parallel rails.

8.6.1 Control law for equal inductance values

8.6.1.1 Control law for discrete phase shedding

First the situation with discrete phase shedding is examined, where the energized converter rails are operated in BCM. In order to get comparable results for different numbers of interleaved converters a normalized input current ripple is used. Therefore the ripple of the input current Δi_{in} is divided by the average of the input current $\bar{i}_{in}$.

For $k = 2$ interleaved boost converters the normalized input current ripple as a function of the duty-ratio can be expressed as

$$\frac{\Delta i_{in}}{\bar{i}_{in}}(d) = \begin{cases} \dfrac{1-2d}{1-d} & \text{for } 0 < d \leq 0.5 \\ \dfrac{-1+2d}{d} & \text{for } 0.5 < d \leq 1 \end{cases}. \tag{8.29}$$

For $k = 3$ it results

$$\frac{\Delta i_{in}}{\bar{i}_{in}}(d) = \frac{2}{3} \cdot \begin{cases} \dfrac{1-3d}{1-d} & \text{for } 0 < d \leq \dfrac{1}{3} \\ \dfrac{2-9(d-d^2)}{3(d-d^2)} & \text{for } \dfrac{1}{3} < d \leq \dfrac{2}{3} \\ \dfrac{-2+3d}{d} & \text{for } \dfrac{2}{3} < d \leq 1 \end{cases}. \tag{8.30}$$

For $k = 4$ it follows

$$\frac{\Delta i_{in}}{\bar{i}_{in}}(d) = \frac{1}{2} \cdot \begin{cases} \dfrac{1-4d}{1-d} & \text{for } 0 < d \leq \dfrac{1}{4} \\ \dfrac{1-6d+8d^2}{2(-d+d^2)} & \text{for } \dfrac{1}{4} < d \leq \dfrac{1}{2} \\ \dfrac{3-10d+8d^2}{2(-d+d^2)} & \text{for } \dfrac{1}{2} < d \leq \dfrac{3}{4} \\ \dfrac{-3+4d}{d} & \text{for } \dfrac{3}{4} < d \leq 1 \end{cases}. \tag{8.31}$$

These functions are plotted in Figure 8.14. For most duty-ratios the smallest current ripple is attained with four interleaved rails. However, there are two regions around the zeros of the curve for three interleaved rails at $d = 1/3$ and $d = 2/3$, where the smallest ripple results with three interleaved rails. According to this the number of active converter rails needs to be reduced from $k = 4$ to $k = 3$, in order to minimize the current ripple in the whole duty-ratio range. With this knowledge a very simple control law can be derived which is illustrated in Figure 8.15.

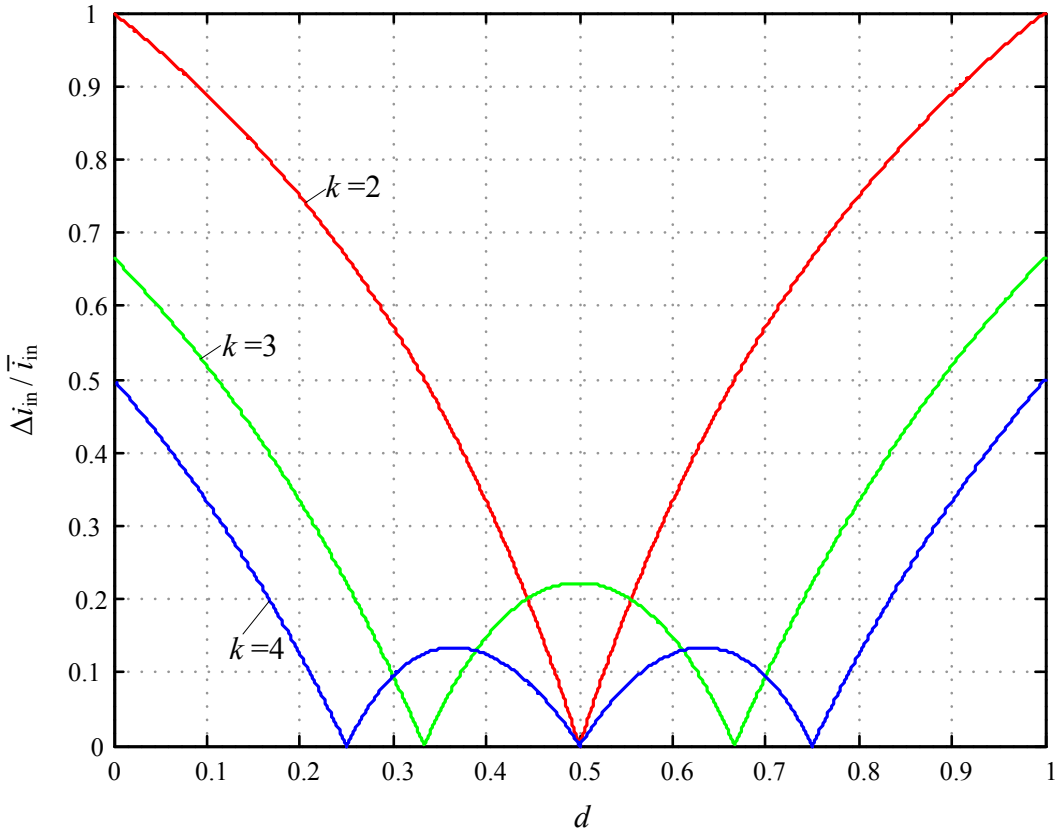

Figure 8.14: Normalized input current ripple versus duty-ratio for $k = 2$ (red) $k = 3$ (green) and $k = 4$ (blue) interleaved converter rails

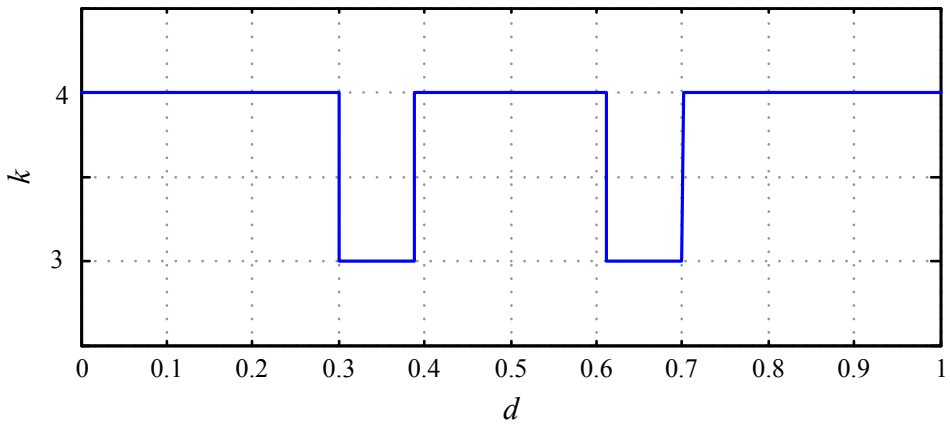

Figure 8.15: Control law to minimize the input current ripple with discrete phase shedding for a converter with $n = 4$ interleaved rails

8.6.1.2 Control law for continuous phase shedding

As described in Section 8.5 the usage of discrete phase shedding has the drawback of high switching frequency and peak current steps. Thus, in the next step continuous phase

shedding is utilized to minimize the input current ripple and a corresponding control law is developed.

At continuous phase shedding the input current is the sum of the four rail currents with determined DCM ratio. The ripple or rather the THD_{DC} of the input current has to be analyzed. Hence, a proper method is required to describe the input current mathematically. Well suited for this purpose is the Fourier synthesis. Necessary is the calculation of the Fourier coefficients Q_ν for the inductor currents depending on the variables average inductor current $\overline{i}_L$, duty-ratio D and DCM ratio K_{lag}.

Note: If the duty-ratio D is used in the following for DCM, it represents the voltage ratio

$$D = \frac{v_{out} - v_{in}}{v_{out}} \tag{8.32}$$

and not the ratio of the on-time and the switching period.

The resulting formula to compute the Fourier coefficients is

$$Q_\nu = \frac{\overline{i}_L \, K_{lag}^2}{2\pi^2 \nu^2 D(1-D)} \left[e^{-j\nu D\frac{2\pi}{K_{lag}}} - 1 + D - D\, e^{-j\nu\frac{2\pi}{K_{lag}}} \right]. \tag{8.33}$$

The detailed derivation of Eq. (8.33) is given in the Appendix A.2.

Since all converter rails have equal switching periods T_s, average inductor currents $\overline{i}_L$ and DCM ratios K_{lag}, the Fourier series are identical and need only to be phase shifted for an optimal interleaving. The phase shift to each current signal is added by multiplying with

$$G_\nu(\varphi) = e^{j\nu\varphi}. \tag{8.34}$$

The optimal phase shift between the rails for $n = 4$ parallel converters is $\varphi = \pi/2$. Thus, the Fourier series for the input current can be expressed as

$$I_\nu(\varphi) = Q_\nu \left[1 + G_\nu\left(\frac{\pi}{2}\right) + G_\nu(\pi) + G_\nu\left(\frac{3\pi}{2}\right) \right]. \tag{8.35}$$

By using the Fourier coefficients to describe the current signal, the exact amount of every harmonic component for the THD calculation is already available. In order to extract the ripple from the input current, the time signal is computed with

$$i_{in}(t) = \sum_{\nu=-\infty}^{\infty} I_\nu \, e^{j\nu\Omega t}. \tag{8.36}$$

For the following analysis the first 50 harmonic components are considered to determine the THD_{DC} and the current ripple.

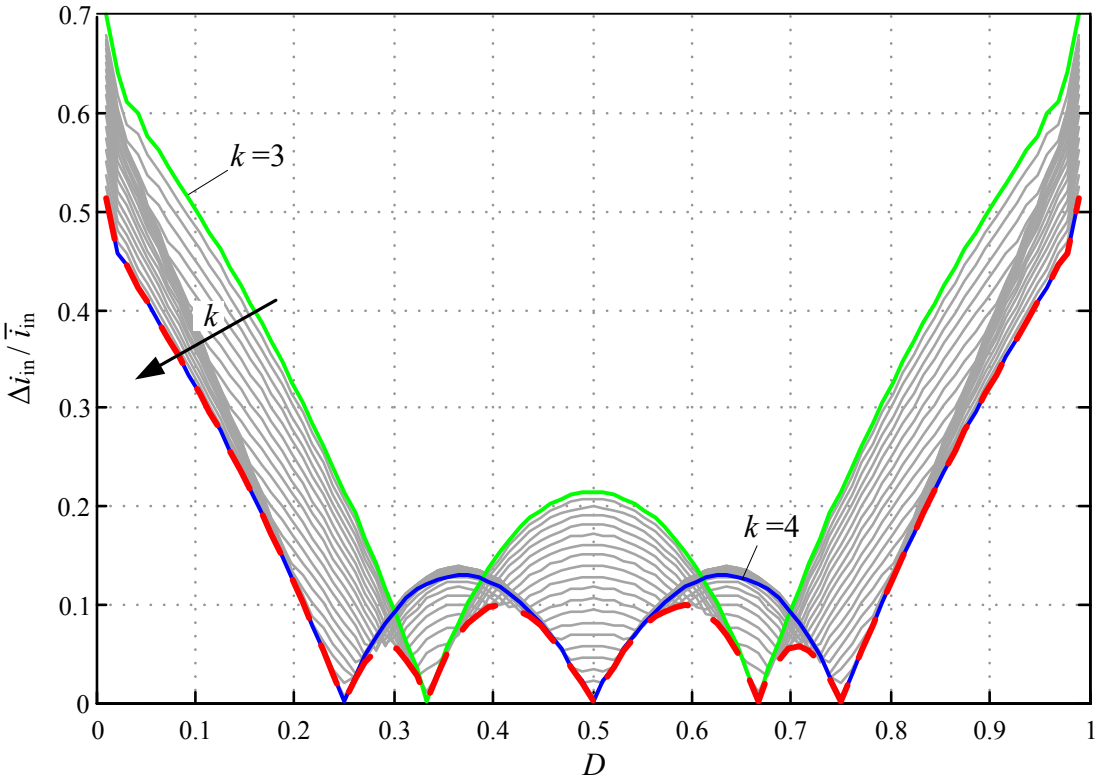

Figure 8.16: Normalized input current ripple vs. duty-ratio for $k = 3$ (green) and $k = 4$ (blue) interleaved rails, for fractional values $k = 3 \ldots 4$ (grey) and the minimum current ripple curve (dashed red)

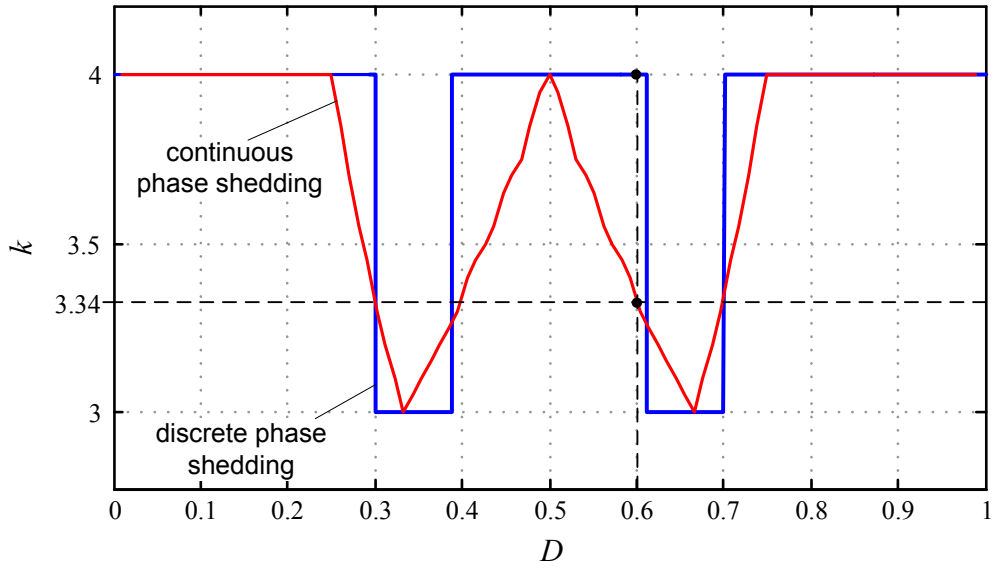

Figure 8.17: Control law for minimum input current ripple with discrete phase shedding (blue) and with continuous phase shedding (red)

The control law for minimizing the input current ripple with continuous phase shedding can be developed similar to that with discrete phase shedding. However, now the number of active converter rails k is not limited to integer values, for which reason the resolution increases. With the knowledge of the discrete phase shedding result only the range of $k = 3 \ldots 4$ is considered. In Figure 8.16 the normalized current ripples versus the duty-ratio are shown with a resolution of $\Delta k = 0.05$. Inspecting the curves with the minimum current ripple for each duty-ratio, it is obvious, that in a wide duty-ratio range the minimum ripple is further reduced due to the increased resolution of continuous phase shedding. Based on the minimum ripple curve (dashed red curve) the control law can be extracted (cf. Figure 8.17). Compared to the control law with discrete phase shedding there are no steps now. This is one basic requirement to apply this method in a PFC application, where a continuous duty-ratio variation occurs.

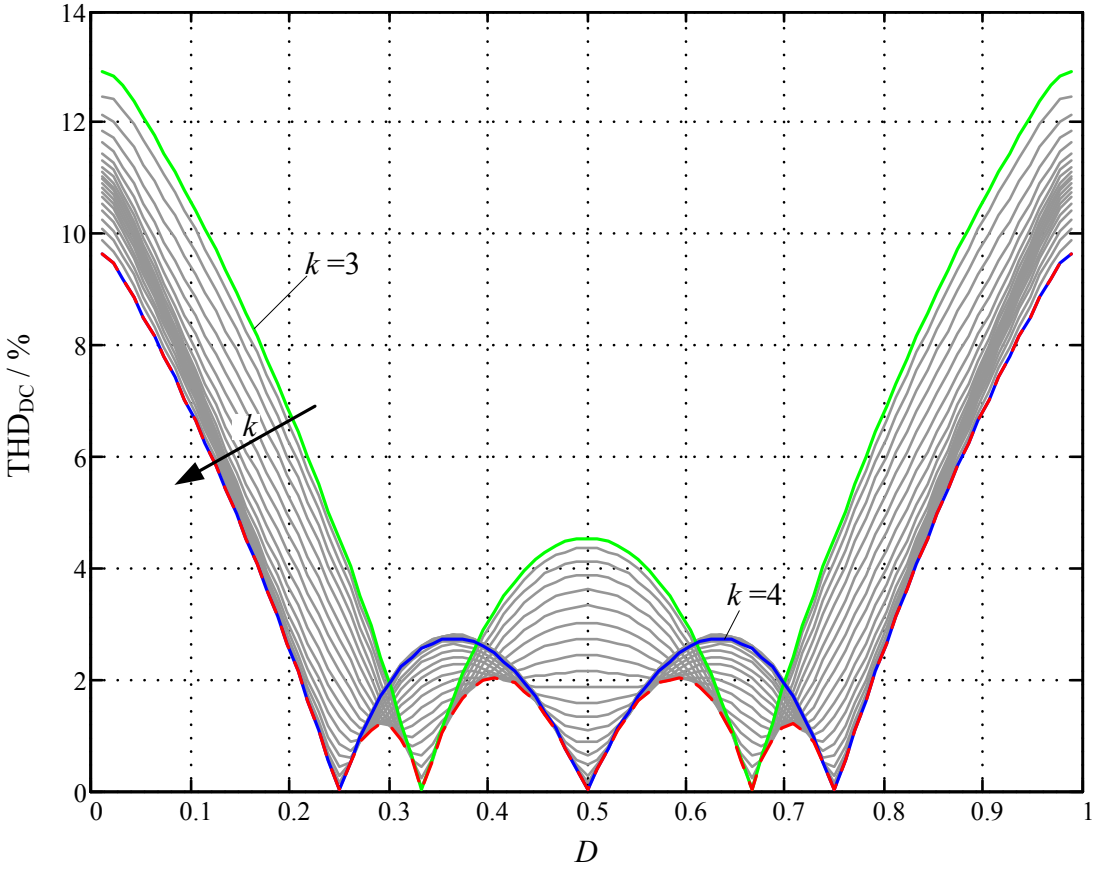

Figure 8.18: THD_{DC} of the input current vs. duty-ratio for $k = 3$ (green) and $k = 4$ (blue) interleaved rails, for fractional values $k = 3 \ldots 4$ (grey) and the minimum THD_{DC} (dashed red)

So far only the input current ripple was considered, but typically the THD should be minimized. In Figure 8.18 the THD_{DC} curves are shown for the same phase shedding values like in Figure 8.16. The qualitative shape of the curves is similar to those of the normalized input current ripple and the resulting control laws are equal. For this reason it is

sufficient in this application to minimize the current ripple in order to get an adequate reduction in the THD_{DC}. It should be noted, that with reducing the THD_{DC} by decreasing k the frequency spectrum moves to lower frequencies.

In Figure 8.19 the inductor currents and the resulting input current are illustrated for an exemplary duty-ratio of $D = 0.6$ to verify the effectiveness of the developed control law. In Figure 8.19 a) no phase shedding is applied, so that all four rails are operating in BCM. By applying the control law the effective number of energized rails is set to $k = 3.34$ at $D = 0.6$ (cf. Figure 8.17). Accordingly, all rails get a DCM ratio of $K_{lag} = 1.2$ (cf. Figure 8.19 b)). And even though the inductor peak currents increase, the ripple of the input current reduces by 21%.

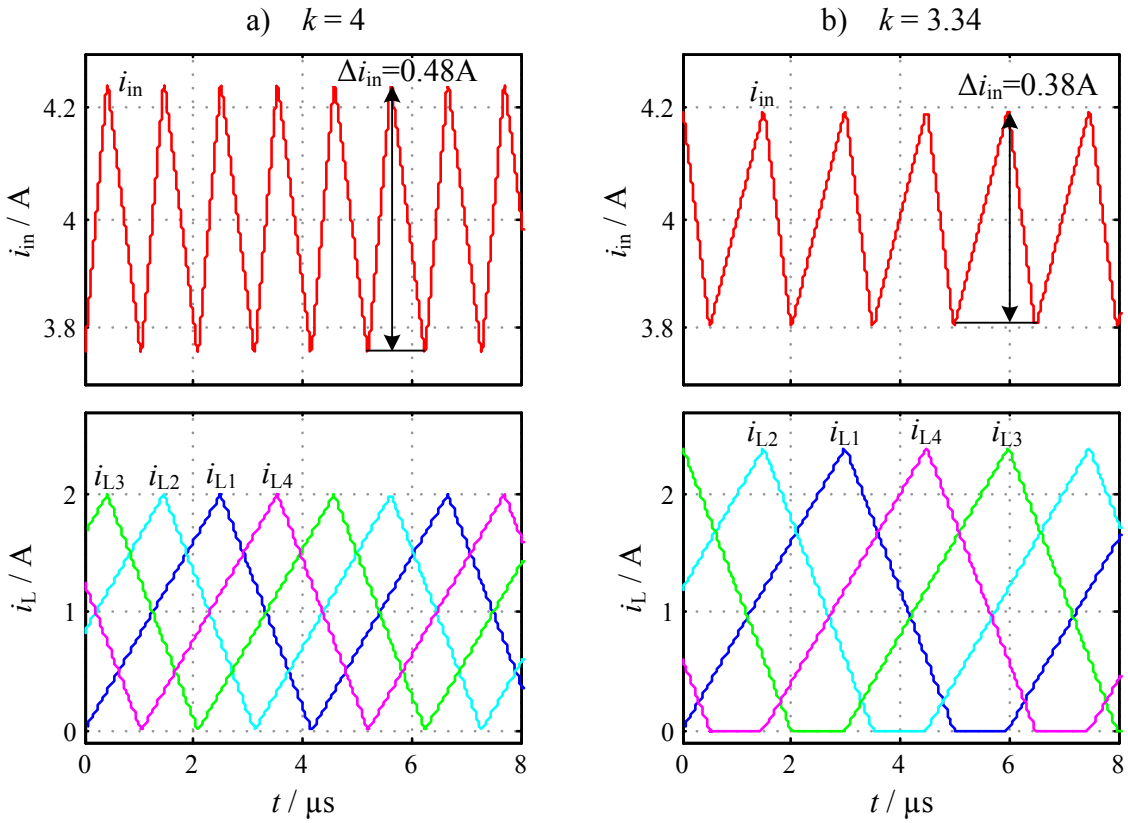

Figure 8.19: Inductor currents and resulting input current at $D = 0.6$
a) without phase shedding ($k = 4$)
b) with continuous phase shedding ($k = 3.34$)

8.6.1.3 Switching frequency and current limitation

It was shown, that the input current ripple can be reduced significantly by applying continuous phase shedding. However, the inductor peak currents grow with increased DCM ratio K_{lag}. Moreover in Section 8.5.3 the requirement of a switching frequency limitation especially in PFC applications was exemplified. Consequently, the limits in the switching frequency and the maximum valid peak current need also to be considered when

the current ripple is minimized with continuous phase shedding. For this reason the range of K_{lag} needs to be limited. The minimum value of K_{lag} is given by the switching period and the maximum switching frequency $f_{s,max}$

$$K_{lag,min} = \frac{1}{\sqrt{f_{s,max}\, T_s}}. \tag{8.37}$$

The inductor current average value $\bar{i}_L$ and the maximum allowable peak current $\hat{\imath}_{L,max}$ determine the maximum value of K_{lag} by

$$K_{lag,max} = \frac{\hat{\imath}_{L,max}}{2\,\bar{i}_L}. \tag{8.38}$$

With Eq. (8.37) and Eq. (8.38) the valid DCM ratio range is given by

$$\frac{1}{\sqrt{f_{s,max}\, T_s}} \leq K_{lag} \leq \frac{\hat{\imath}_{L,max}}{2\,\bar{i}_L}. \tag{8.39}$$

Expressing this operating range for the number of effective energized rails k, it follows

$$n \cdot \frac{2\,\bar{i}_L}{\hat{\imath}_{L,max}} \leq k \leq n \cdot \sqrt{f_{s,max}\, T_s}\,. \tag{8.40}$$

The dedicated borders $K_{lag} \geq 1$ and $k \leq n$ must still be maintained, respectively.

By reaching a limit it is obvious to operate the converter with this boundary value. But retaining this boundary value must not be the optimum valid value for the minimum current ripple. Strictly speaking the new optimal DCM ratio needs to be identified from the valid range. However, this could result in undesirable steps in the peak currents and switching frequency, for which reason an operation with the boundary value is the recommended way.

8.6.1.4 Verification in a PFC application

The effectiveness of the ripple minimization under varying duty-ratio and bounded DCM ratio can be clearly examined in a PFC application. For this purpose the control law of Figure 8.17 was implemented in a look-up table (LUT).

Characteristic curves during one line half-cycle are depicted in Figure 8.20 for low line voltage and in Figure 8.21 for high line voltage. In both figures the situation without and with limitation are shown. For limitation the maximum switching frequency is set to $f_{s,max} = 150\text{kHz}$ and the maximum peak inductor current is set to $i_{pk,max} = 5\text{A}$. In order to illustrate the difference to the situation without optimization, the curves for four interleaved converter rails in BCM are added (red curves). In all cases a significant reduction of the input current ripple is attained for a wide range within the line half-cycle.

The ripple reduction is accompanied by a decreasing of the switching frequency and an increasing of the inductor peak currents.

If the maximum switching frequency is reached, the operation at this boarder can be easily achieved by adjusting the number of effective energized rails k with the DCM ratio K_{lag}. By limiting the switching frequency the optimal ripple reduction cannot be ensured anymore. Rather the current ripple can increase significantly in that area. However, if a maximum switching frequency needs to be kept, this effect will occur anyway.

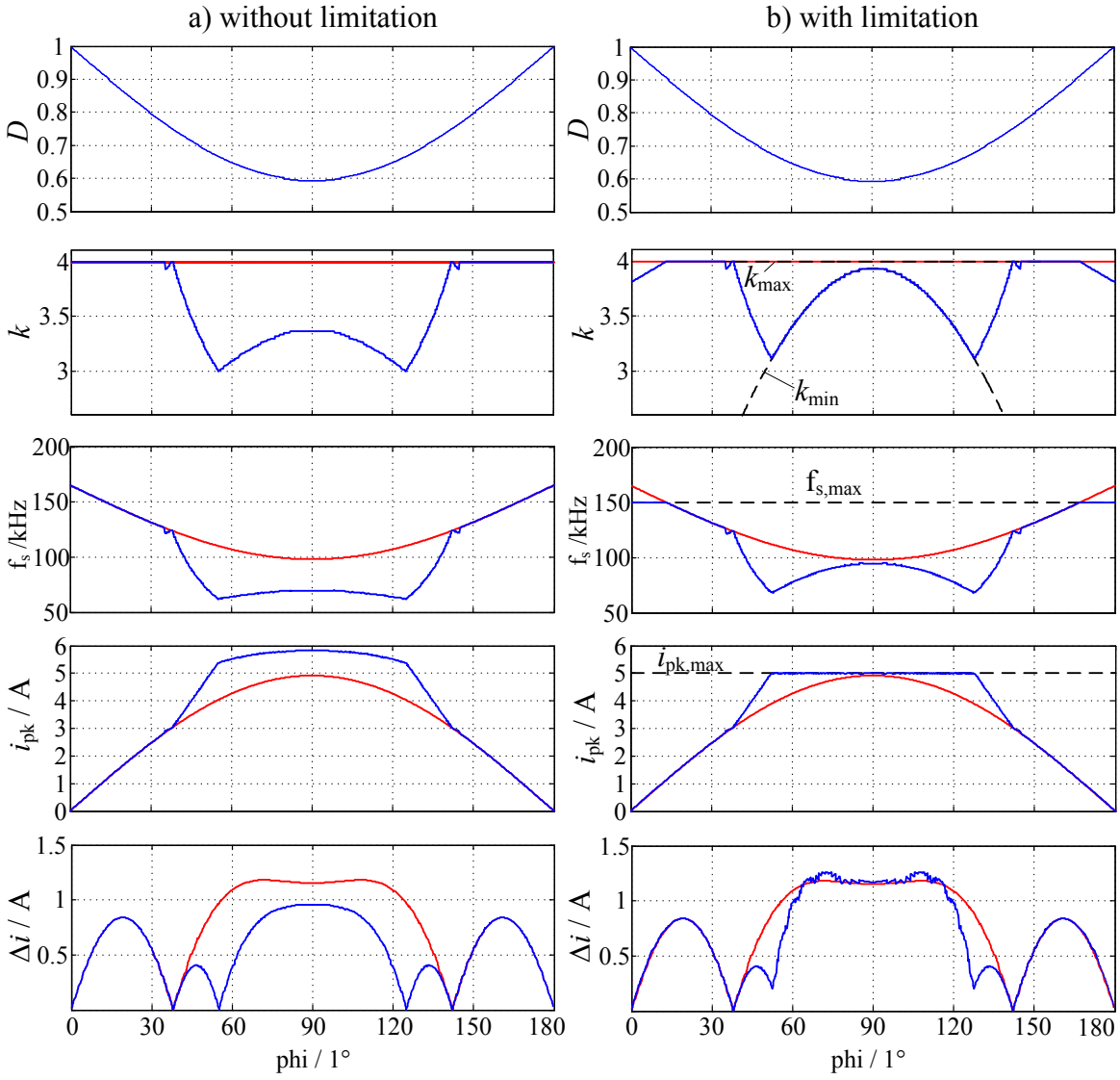

Figure 8.20: Curves of duty-ratio, number of active rails, switching frequency, peak current and input current ripple during one line half-cycle in a PFC application at $V_{ac} = 115\text{V}$. Without optimization (red), with optimization (blue), ($v_{out} = 400\text{V}, P_{out} = 800\text{W}$)

Also during peak current limitation an operation at the boarder can be guaranteed with this control concept. In most cases the current limitation still offers a decreased reduction in the current ripple, but at particular operating points a slightly higher current ripple results.

In Figure 8.22 the simulated input current is illustrated. The first line half-cycle was simulated without optimization and the second with optimization by dint of the derived control law. This simulation verifies the results of Figure 8.21. Complete ripple elimination is achieved at $D = 1/4$, $D = 1/2$ and $D = 3/4$ in both half-cycles. However, with the optimization the ripple is additionally eliminated at $D = 1/3$ and $D = 2/3$. Also a ripple reduction around this additionally elimination points yields.

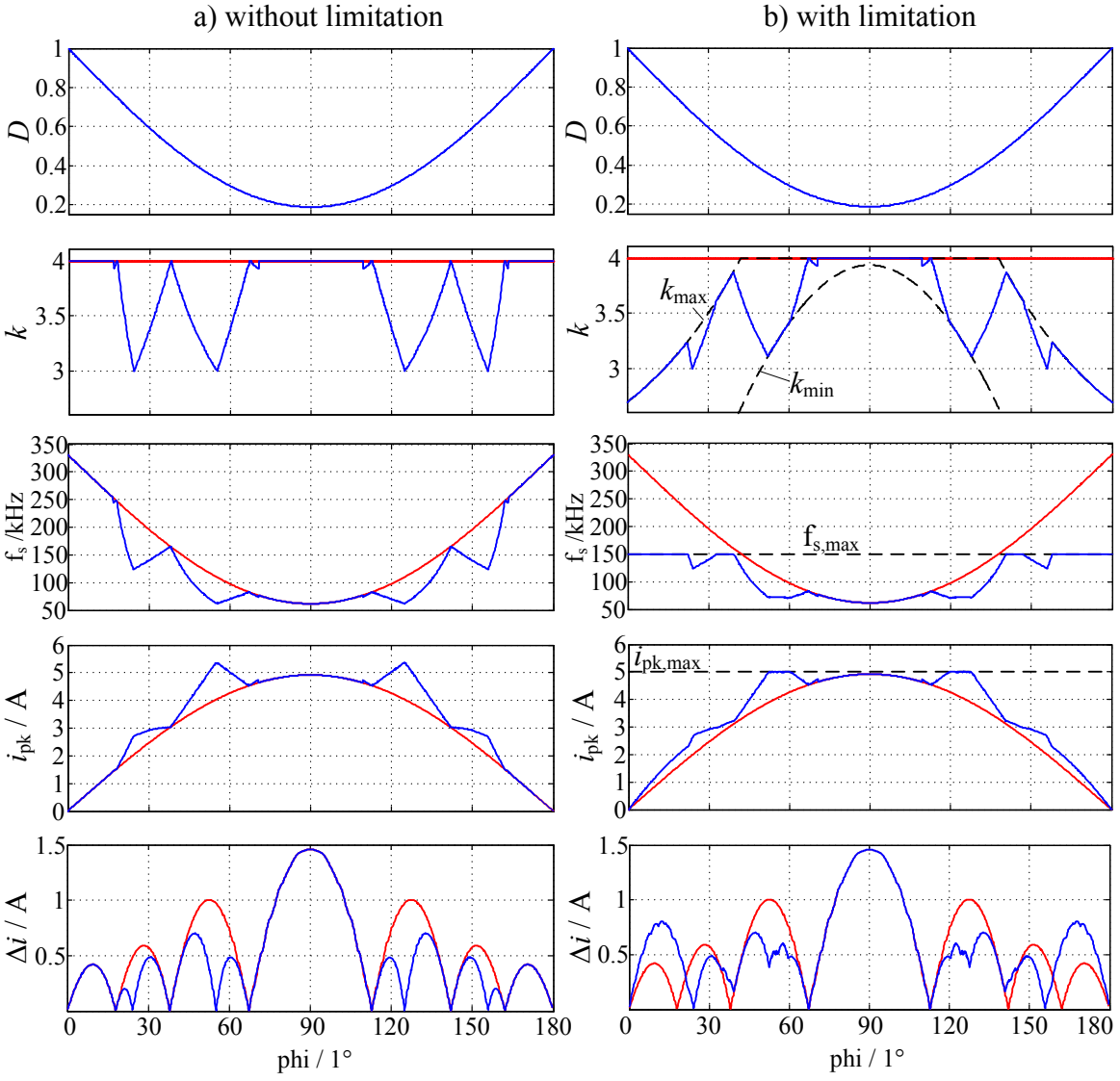

Figure 8.21: Curves of duty-ratio, number of active rails, switching frequency, peak current and input current ripple during one line half-cycle in a PFC application at $V_{ac} = 230\text{V}$. Without optimization (red), with optimization (blue), ($v_{out} = 400\text{V}, P_{out} = 1600\text{W}$)

8.6.1.5 Practical implementation

A significant reduction in the THD_{DC} can be achieved using this proposed optimization. However, only if this method can be implemented on a DSP or µC with reasonable effort, it will be utilized in practice. Thus, a suggestion for practical implementations is presented.

The control law illustrated in Figure 8.17 is valid for $n = 4$ parallel converters and determines the number of active rails depending on the duty-ratio, i.e. $k(D)$. It does not depend on the inductance values. Consequently, the control law is valid in general and can be applied for every converter with $n = 4$ parallel converters. For other numbers of interleaved converters universal control laws result respectively. These control laws can be easily implemented in LUTs, where the optimal values for k are stored for the duty-ratio range.

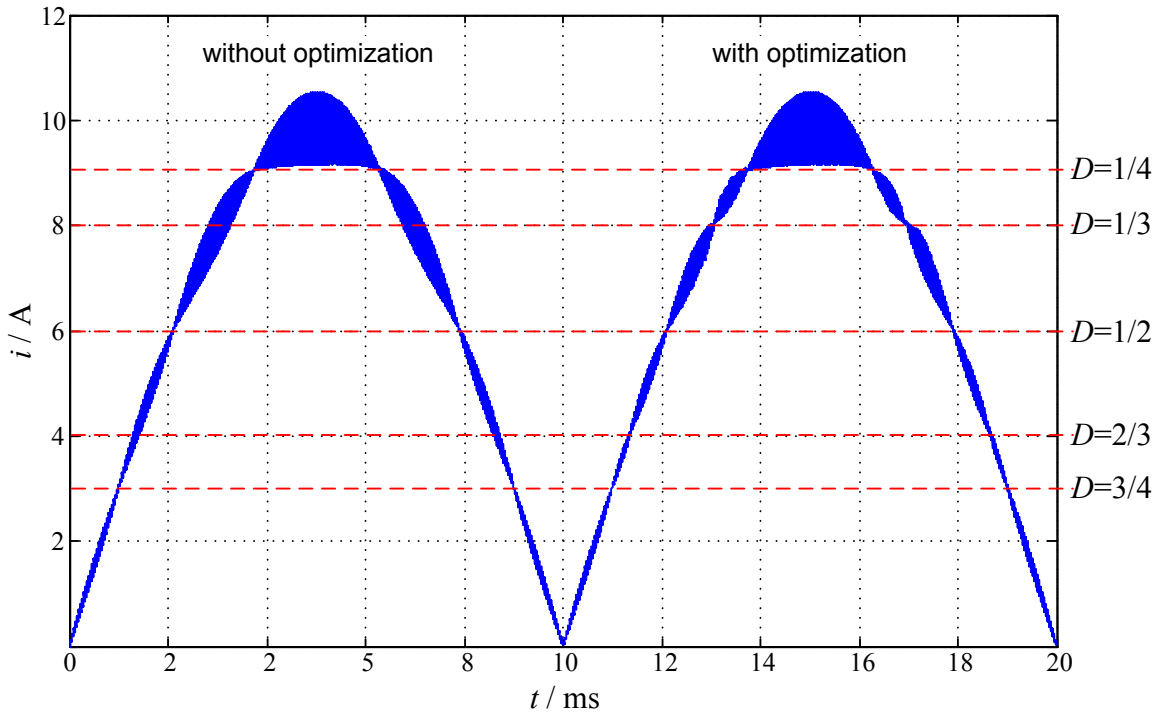

Figure 8.22: Input current of a PFC converter at $V_{ac} = 230\text{V}$ without and with optimization by dint of the control law ($v_{out} = 400\text{V}, P_{out} = 1600\text{W}$)

The limits of k due to the maximum peak current and switching frequency need to be updated continuously. By reaching a limit, this border value is used until the next valid value of the LUT can be applied.

This method was also utilized for the simulated PFC converter results (Figure 8.20 - Figure 8.22) and can be implemented on a DSP or µC with little effort.

Instead of k also the related values for K_{lag} can be used. This is recommended since this value is utilized for the DCM control algorithm.

8.6.2 Harmonic Elimination with Unequal Inductance Values

One major advantage of interleaving n converters with equal inductance values is the elimination of the first $n-1$ harmonics in the input current. The requirement is a time shift of T_s/n between the inductor currents. However, if there is a variation in the inductance values, this effect disappears and all harmonics are present. But with adjusted phase shift values it is possible to reduce or even to eliminate the first harmonics [BeSu09].

If there is no restriction due to current balancing demand, individual DCM ratios for each converter rail can be applied. This degree of freedom can be utilized to eliminate further harmonics.

In the following the elimination of harmonics at unequal inductance values is investigated with and without restriction due to current balancing. For both cases the introduced balancing factor K_b is utilized to enable an individual DCM ratio for each slave rail. The formula to compute the Fourier coefficients is modified to

$$Q_\nu = \frac{\bar{i}_L K_{lag}^2}{2\pi^2 \nu^2 D(1-D)} \left[e^{-j\nu D \frac{K_b}{K_{lag}} 2\pi} - 1 + D - D\, e^{-j\nu \frac{K_b}{K_{lag}} 2\pi} \right]. \tag{8.41}$$

The validation of the optimizations in this chapter is conducted with $n = 3$ parallel rails, but the methods can be easily modified for other numbers of interleaved rails. Inductance values with 5% deviation are utilized for the exemplary calculations (cf. Table 8.2). Furthermore, the master rail operates in BCM ($K_{lag} = 1$) and its average current is chosen to $\bar{i}_{L1} = 1\text{A}$ for the validations.

For analyzing the harmonic components the DC component of the currents is not significant. For this reason all currents are illustrated without the DC component.

	inductance value	relative inductance
L_1	200 µH	100%
L_2	190 µH	95%
L_3	180 µH	90%

Table 8.2: Variation in the utilized inductance values

The interference in the input current due to unequal inductance values is depicted in Figure 8.23 b). Compared to the situation with equal inductances (cf. Figure 8.23 a)) a significant higher input current ripple results. Also the appearance of a lower fundamental frequency can already be seen. The existence of the 1st and 2nd harmonic becomes even clearer by looking at the frequency spectrum in Figure 8.24. This illustrates that other measures are required to eliminate the harmonic components, if there are deviations in the inductance values.

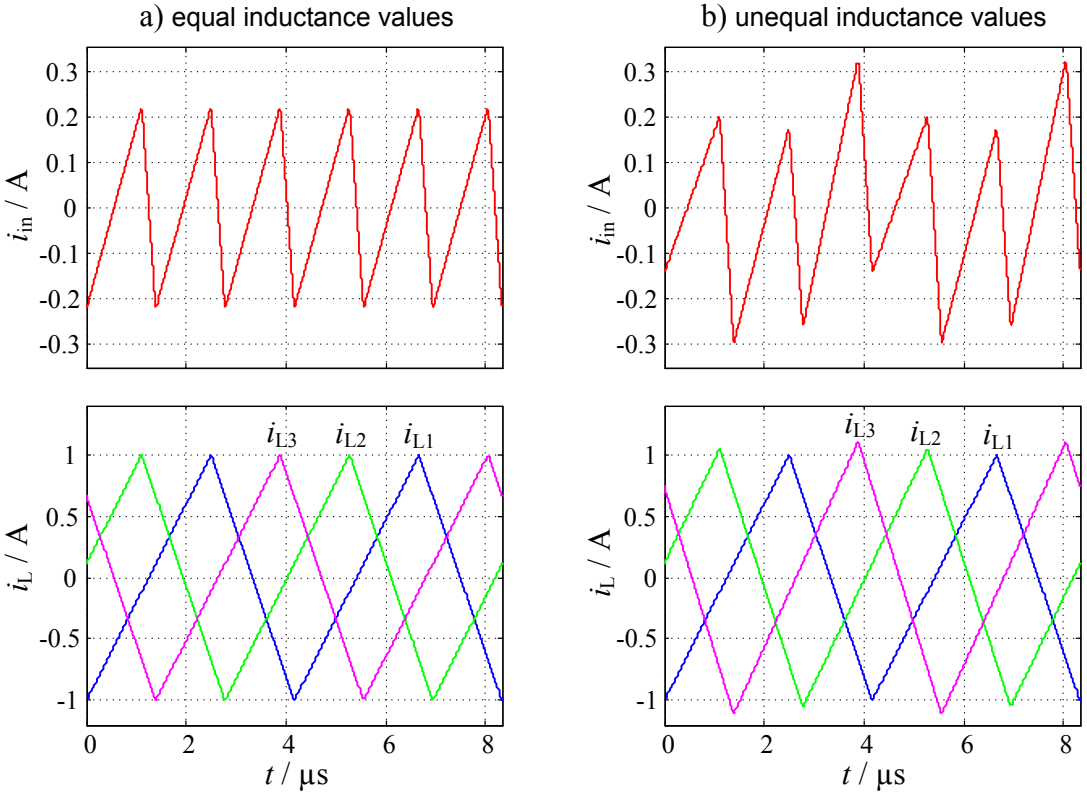

Figure 8.23: Inductor currents and resulting input current at $D = 0.6$
a) with equal inductance values ($L_1 = L_2 = L_3 = 200\mu H$),
b) with unequal inductance values (cf. Table 8.2)

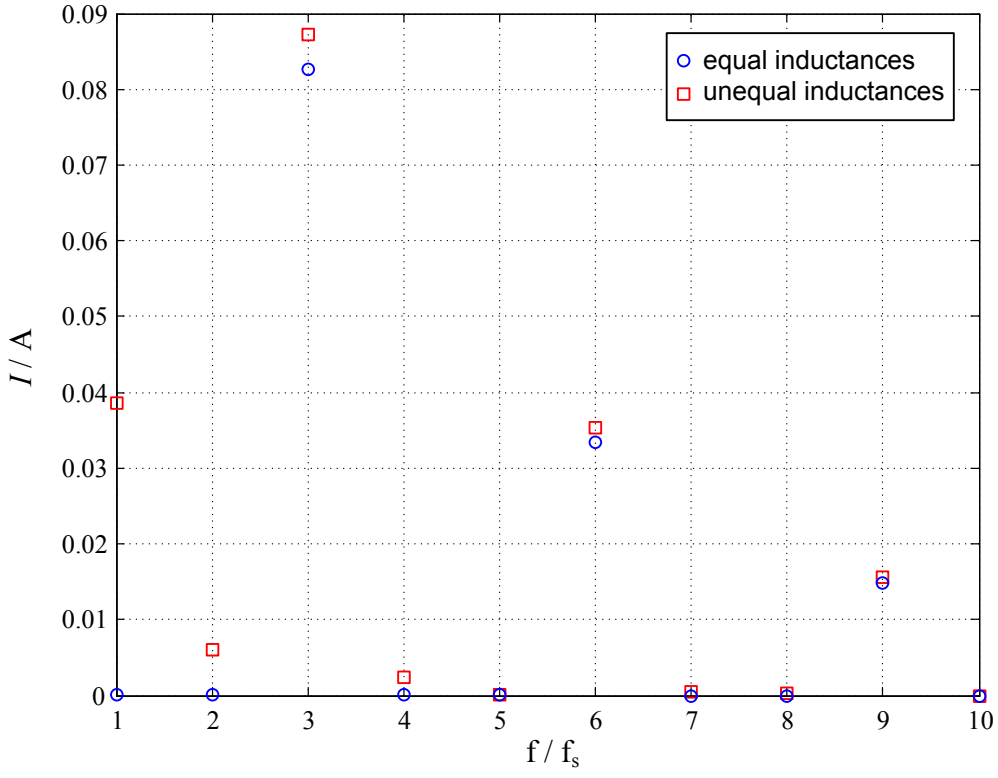

Figure 8.24: Harmonic components at $D = 0.6$ with equal and unequal inductance values

8.6.2.1 Harmonic elimination without balanced inductor currents

In order to eliminate harmonic components a system of equations needs to be prepared. For each harmonic, which should be eliminated, the real and imaginary part must be set to zero. Hence, two independent variables are required to eliminate one harmonic component. These independent variables are the phase shift angles φ_i of the slave rails and the balancing factors K_{bi}, which can give every slave rail an individual DCM ratio.

For example, with $n = 3$ parallel converter rails two harmonic components can be eliminated. The phase shift angle of the master rail is fixed to zero and the remaining two phase shift angles can be modulated. The balancing factor of the master rail must be set to $K_{b1} = 1$ and the balancing factors of the slave rails can be randomized, if there is no current balancing restriction. In this case the system of equations to eliminate the 1st and 2nd harmonic in the input current can be expressed as

$$\begin{aligned} Re\{Q_{1,1}\} + Re\{Q_{2,1}\} + Re\{Q_{3,1}\} &= 0 \\ Im\{Q_{1,1}\} + Im\{Q_{2,1}\} + Im\{Q_{3,1}\} &= 0 \\ Re\{Q_{1,2}\} + Re\{Q_{2,2}\} + Re\{Q_{3,2}\} &= 0 \\ Im\{Q_{1,2}\} + Im\{Q_{2,2}\} + Im\{Q_{3,2}\} &= 0 \end{aligned}, \tag{8.42}$$

where $Q_{i,\nu}$ represents the Fourier coefficient with the order ν of the current in rail i (cf. Eq. (8.33)).

Because the nonlinear system of equations cannot be solved analytically, the numeric Newton method is utilized. The appliance of the Newton method for this purpose is described in Appendix A.3 in detail.

With the Newton method, the phase shift angles and balancing factors for the entire duty-ratio range were determined. The resulting curves are depicted in Figure 8.25. It is striking, that a discontinuity appears in the curves of the phase angles at $D = 0.5$. This means, that the two slave rails needs to interchange their order to eliminate the 1st and 2nd harmonic. The curves of the balancing factors are continuously and have symmetry to the $D = 0.5$ axis.

In Figure 8.26 the spectrum of the input current is given for $D = 0.6$. The corresponding inductor and input current shapes are depicted in Figure 8.27. In this figures also the situation without optimization are shown, i.e. default values $K_{b2} = K_{b3} = 1$, $\varphi_2 = 120°$ and $\varphi_3 = 240°$ are applied. It can be seen, that due to applying the optimized phase angles and balancing factors the 1st and 2nd harmonic are eliminated successfully. A reduction of the other harmonic components cannot be guaranteed. Some components even get higher amplitudes. Due to this fact the reduction of the THD_{DC} is not inherent. However, at most duty-ratios an improvement of the THD_{DC} is achieved, additionally. This is illustrated in Figure 8.28, where the THD_{DC} without and with optimization is plotted for the entire duty-ratio range. Only in the regions of $D = 1/3$ and $D = 2/3$ the THD_{DC} is slightly better without the optimization.

The inductor currents in Figure 8.27 illustrate that all rails operate with individual DCM ratios and phase shifts in the optimized case. By looking at the input current it is distinguishable, that with eliminating the first and second harmonic also the peak-to-peak current ripple is reduced, significantly.

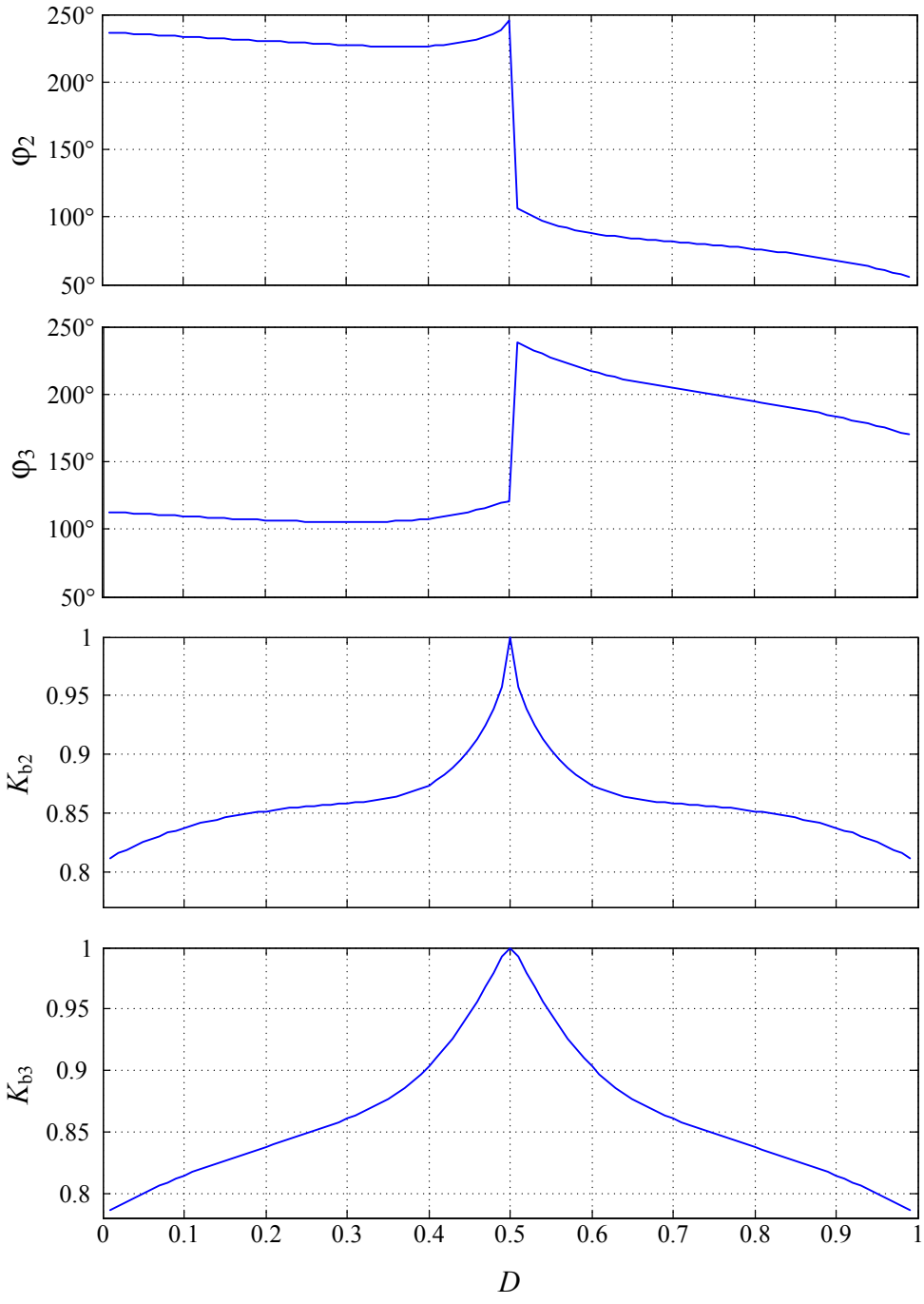

Figure 8.25: Characteristic of the phase angles φ_2, φ_3 and the balancing factors K_{b2}, K_{b3} versus duty-ratio in order to eliminate the 1st and 2nd harmonic

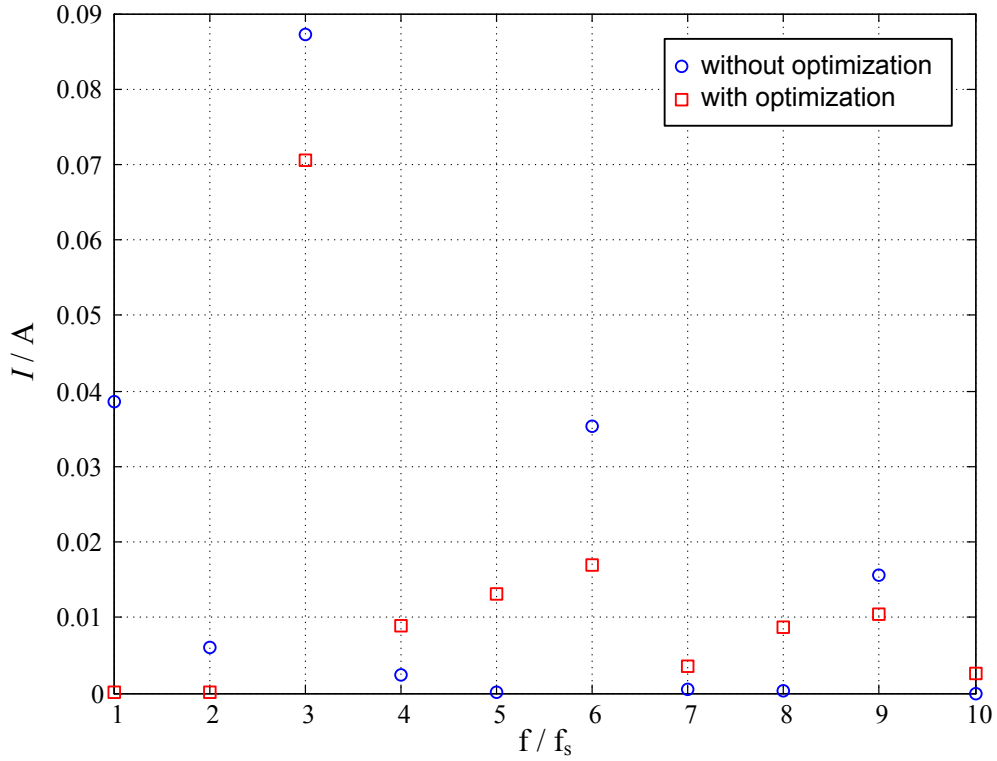

Figure 8.26: Harmonic components with and without optimization at $D = 0.6$

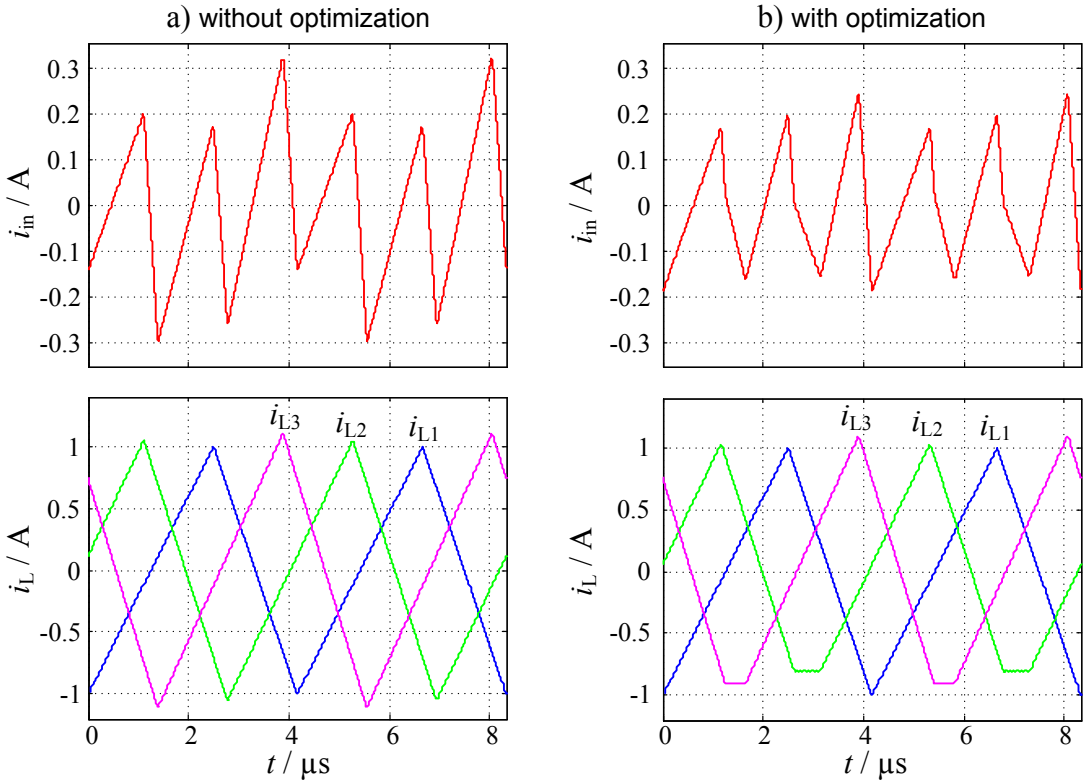

Figure 8.27: Inductor currents and resulting input current at $D = 0.6$
a) without optimization
b) with optimization

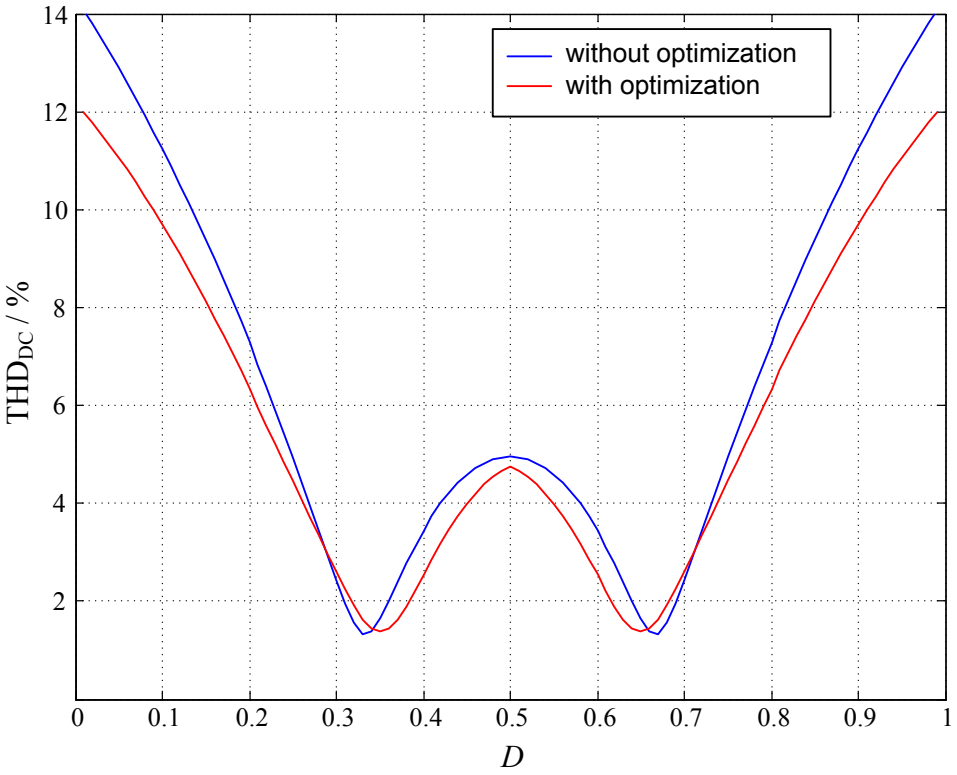

Figure 8.28: THD_{DC} versus duty-ratio without and with optimization

8.6.2.2 Harmonic elimination with balanced inductor currents

In Section 8.4.1 a current balancing functionality was presented. Therefore the balancing factor K_b is utilized to give every single rail an individual on-time. Thus, the only remaining variable to eliminate or reduce harmonics for balanced average inductor currents is the phase shift.

Again, two independent variables are required to eliminate one harmonic component. With $n = 3$ parallel converter rails two phase shift values can be modulated independently. Thus, one harmonic component can be eliminated. In this case the system of equations to eliminate the first harmonic in the input current is given by

$$\begin{aligned} Re\{Q_{1,1}\} + Re\{Q_{2,1}\} + Re\{Q_{3,1}\} &= 0 \\ Im\{Q_{1,1}\} + Im\{Q_{2,1}\} + Im\{Q_{3,1}\} &= 0 \end{aligned} . \tag{8.43}$$

Since two variables are required to eliminate one harmonic component, one variable is left, if the number of independent variables is odd, i.e. if the number of parallel rails is even. This variable can be utilized to minimize a harmonic component. This can be done by setting the derivation of the magnitude equal to zero. For example with two parallel rails it follows

$$\frac{d}{d\varphi_2}\left|Q_{1,1} + Q_{2,1}\right| = 0. \tag{8.44}$$

The verification of this method is done for three different balancing factors, respectively. The applied factors are $K_b = 1$ for equal on-times, $K_b = \sqrt{L_k/L_m}$ for equal average currents and $K_b = L_k/L_m$ for equal peak currents.

Again the numeric Newton method is utilized to solve the system of equation Eq. (8.43) for the entire duty-ratio range. The resulting phase shift values to eliminate the first harmonic are depicted in Figure 8.29. At equal on-times the optimal phase shift values are constant for all duty-ratios. However, by applying equal average or peak currents the phase shift values needs to be changed with the duty-ratio.

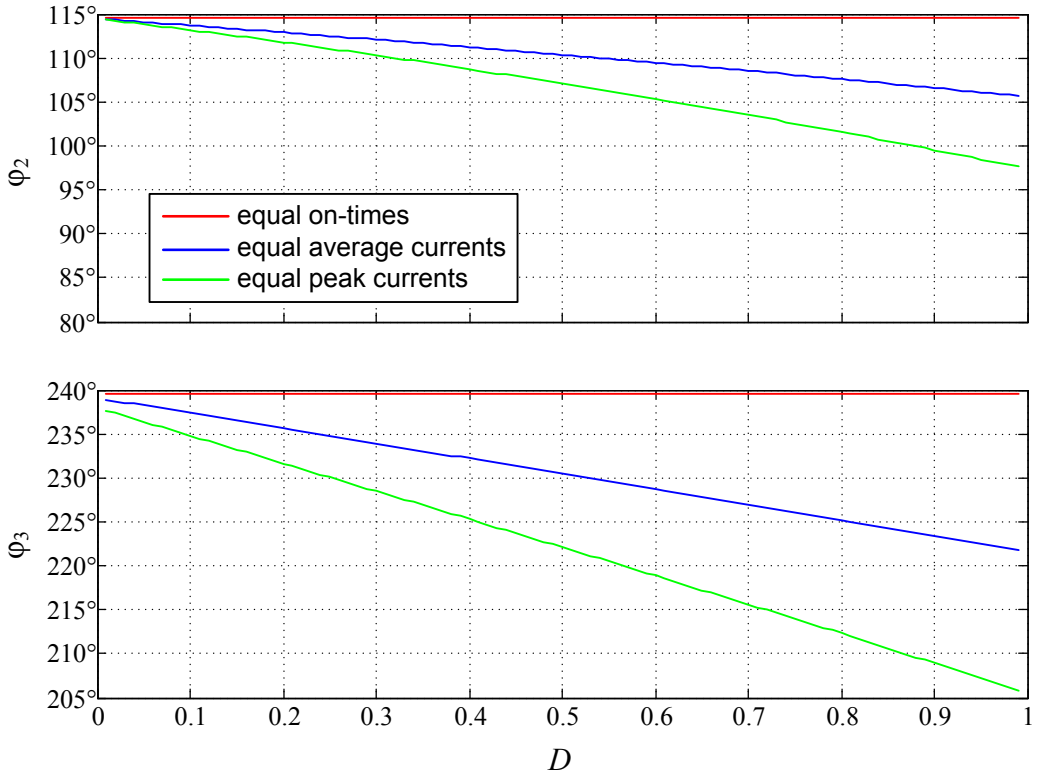

Figure 8.29: Characteristic of the phase angles φ_2, φ_3 versus the duty-ratio in order to eliminate the 1st harmonic, with equal on-times, with equal average currents and with equal peak currents

Exemplarily, the spectrums of the input currents for $D = 0.6$ are illustrated in Figure 8.30. The corresponding inductor and input current shapes are given in Figure 8.31. For the not optimized case the default values $\varphi_2 = 120°$ and $\varphi_3 = 240°$ are applied.

As stipulated the first harmonic can be eliminated for all applied balancing factors. By looking at the other harmonic components, it is visible, that the minimum amplitude varies

between the methods. However, an improvement of the THD_{DC} compared to the not optimized case is attained for all duty-ratios (cf. Figure 8.32). The best THD_{DC} for most duty-ratios is achieved with balancing the inductor currents to equal peak values.

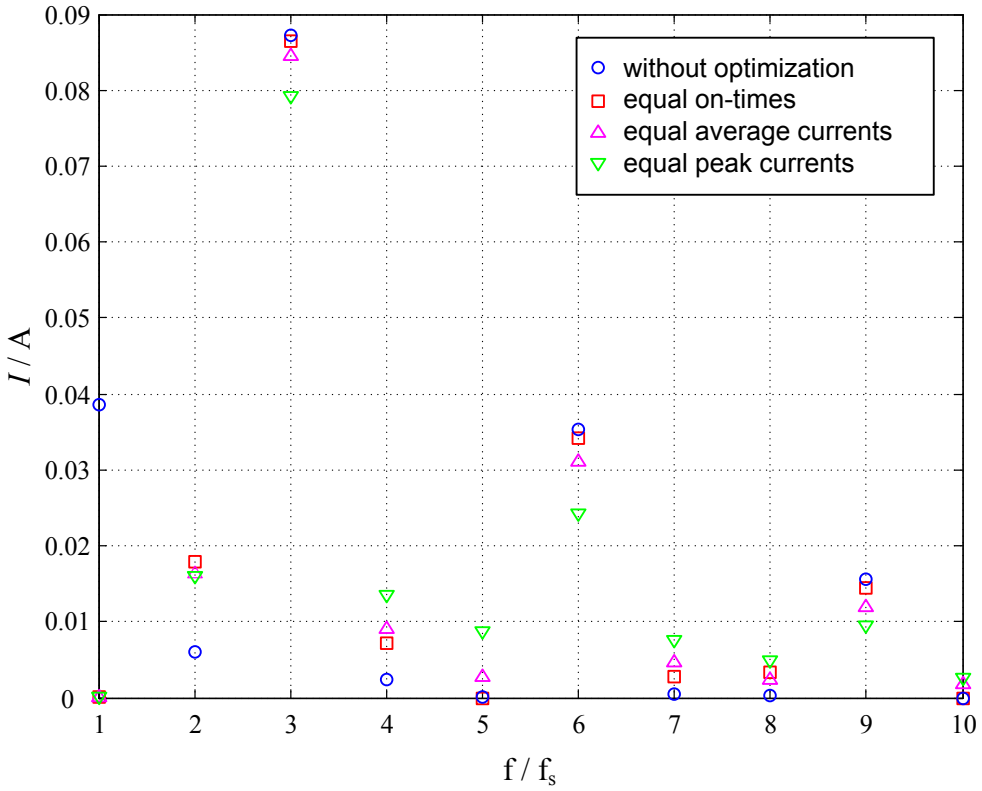

Figure 8.30: Harmonic components at $D = 0.6$ without optimization, with equal on-times, with equal average currents and with equal peak currents

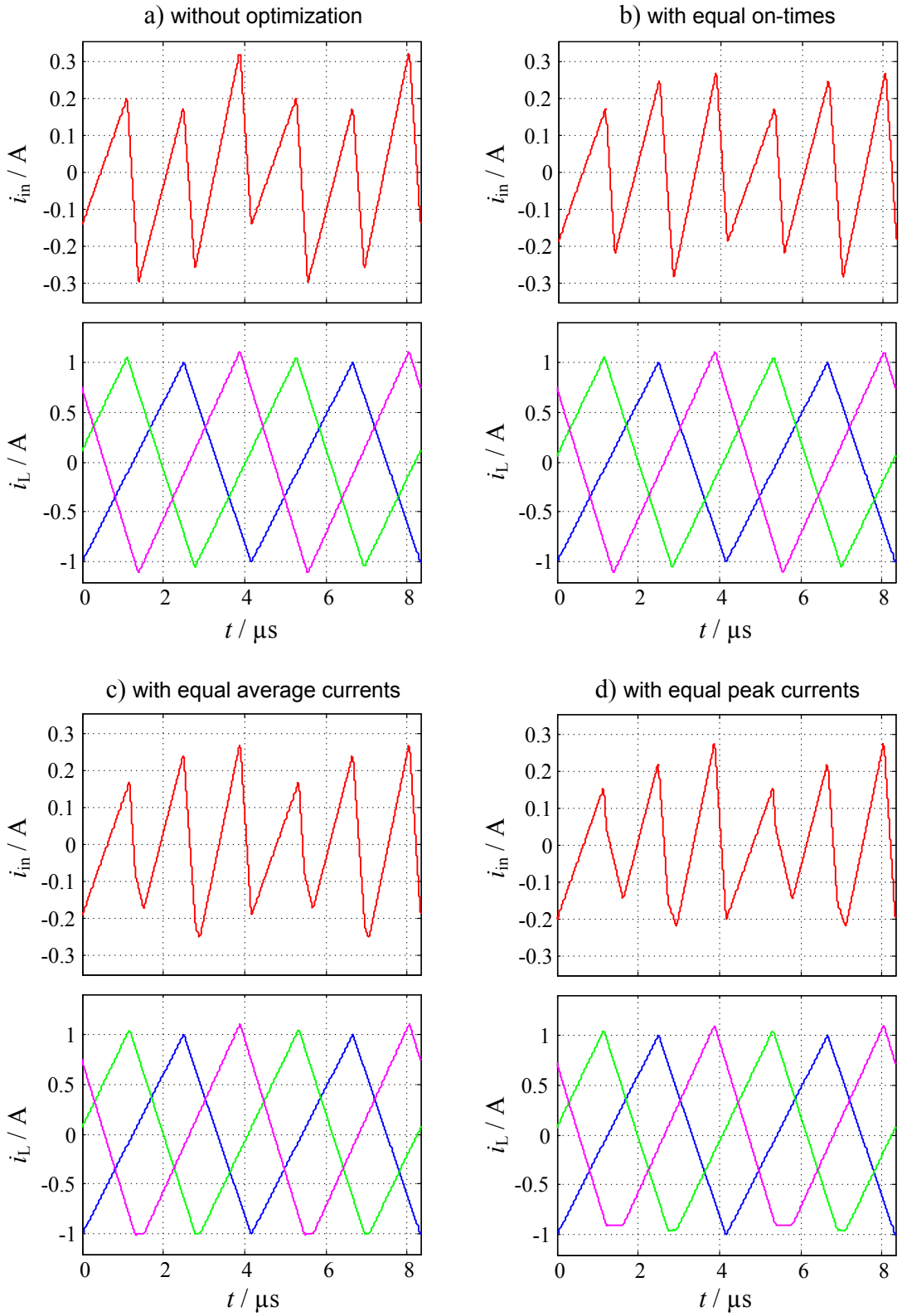

Figure 8.31: Inductor currents and resulting input current at $D = 0.6$
a) without optimization *b) with equal on-times*
c) with equal average currents *d) with equal peak currents*

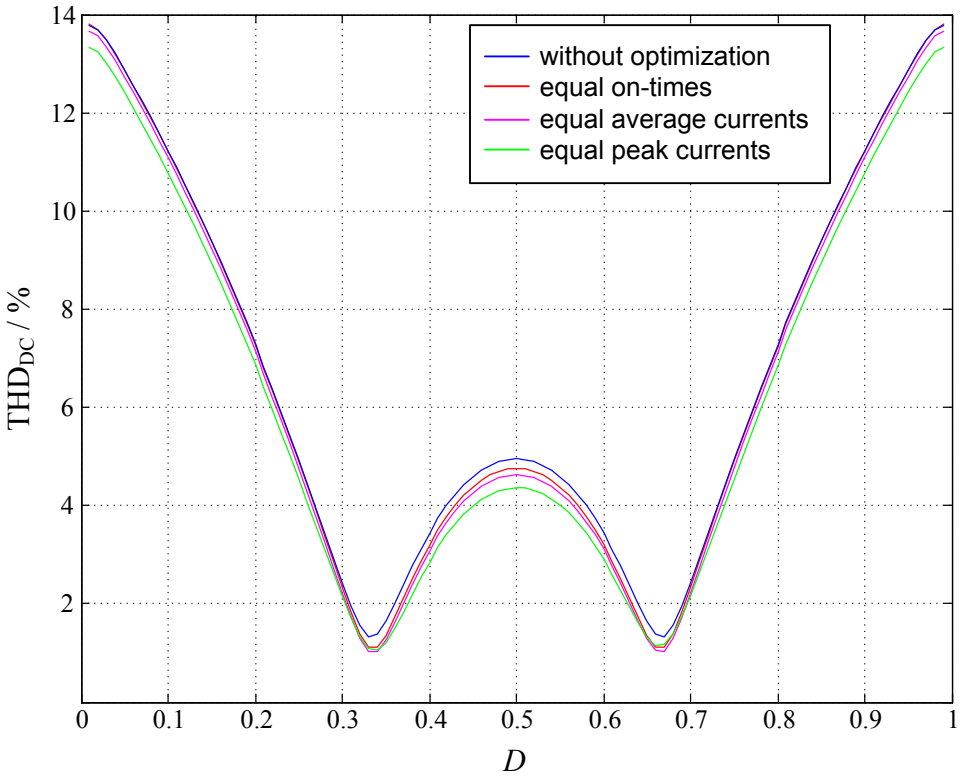

Figure 8.32: THD_{DC} versus duty-ratio without optimization and with optimization at equal on-times, equal average currents and equal peak currents

8.6.2.3 Minimization of the THD_{DC} by applying a master DCM ratio

So far the elimination of harmonic components was done with the master rail operating in BCM ($K_{lag} = 1$). A reduction in the THD_{DC} was already attained with this practice. However, in Section 8.6.1 it is shown, that with adjusting the DCM ratio the THD_{DC} can be further reduced.

For this purpose the DCM ratio of the master rail is varied in the range $K_{lag} = 1 \ldots 1.5$. This range represents the continuous phase shedding with $k = 2 \ldots 3$ active rails at equal inductance values. Examined is the situation without restriction of current balancing. Thus, for every particular value of K_{lag} the first and second harmonic are eliminated by solving the system of Eq.(8.42).

If there are restrictions to the current balancing, the procedure is very similar. Instead of Eq. (8.42) just the system of Eq. (8.43) needs to be applied.

By applying values for the DCM ratio $K_{lag} > 1$ it is no longer necessary to limit the values for the balancing factor to $0 < K_b \leq 1$. Now the range can be extended to $0 < K_b \leq K_{lag}$. This means that due to the optimization slave rails can be operated at smaller DCM ratios than the master rail.

For each particular fractional value of K_{lag} the entire duty-ratio range has to be examined. The resulting curves of the THD_{DC} are depicted in Figure 8.33. In the region of $0.4 < D < 0.6$ the THD_{DC} can be reduced even further due to applying the optimal DCM ratio for the master rail. From the curves of Figure 8.33 a control law can be deduced (cf. Figure 8.34 solid line). For comparison the control law for equal inductances is also depicted (dashed line). Since there are no discontinuities in the control law, it is well suited for practical usage including PFC applications. However, the illustrated control law is not valid in general. It depends on the deviation in the inductance values and therefore needs to be updated for every set of inductance ratios.

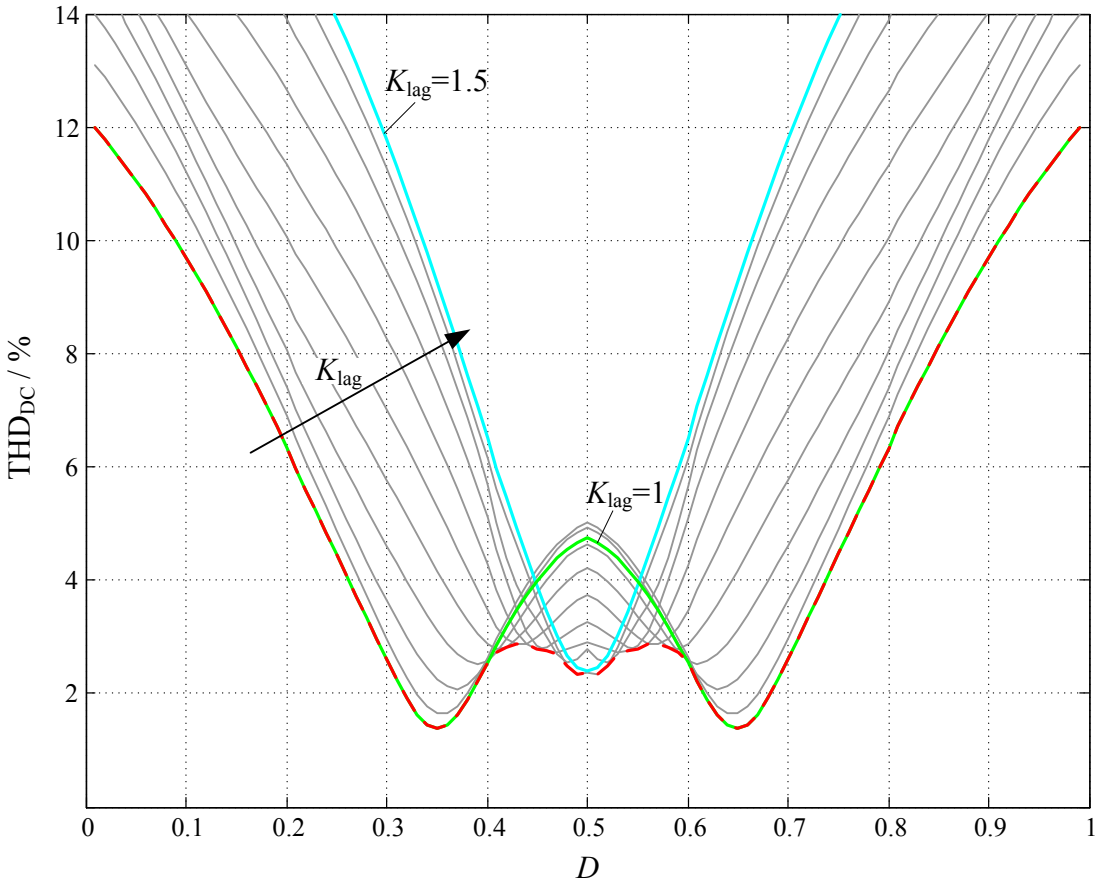

Figure 8.33: THD_{DC} of the input current vs. duty-ratio at unequal inductances under DCM ratio variation in the range of $K_{lag} = 1 \ldots 1.5$ and minimum THD_{DC} (dashed red)

8.6.2.4 Practical implementation

If there are significant mass production tolerances in the inductance values, an individual combination of inductance values will result for each power supply. Consequently, a generalized control law for minimizing the THD_{DC} cannot be defined. For which reason, an individual control law needs to be computed for each power supply. The required inductance ratios can be identified with the method described in Section 8.4.2.

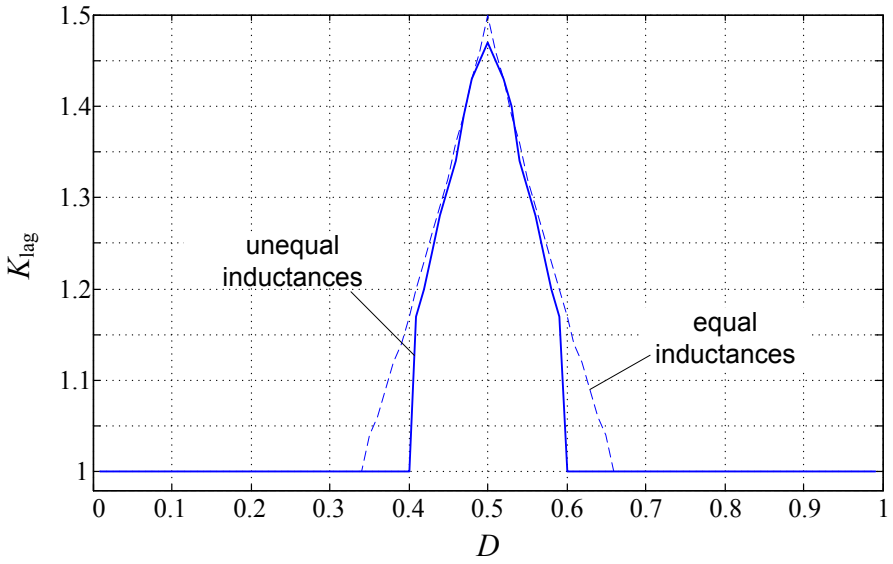

Figure 8.34: Control law for minimum THD_{DC} with unequal inductances (solid line) and equal inductances (dashed line)

Determining the optimal parameters for minimized THD_{DC} at unequal inductance values can be separated in two tasks. First the optimal phase shift values and if applicable, the optimal balancing factors need to be computed. If this is accomplished with the Newton method for the entire duty-ratio range, it becomes a time-consuming procedure. With an increasing number of variables the presetting of adequate start values becomes more difficult. In the curves for the optimal phase shift values, steps occur for $n > 2$ (cf. Figure 8.25). Such steps are not acceptable during operation. Hence, using the optimal phase shift values is limited. For example in a PFC application at low line voltage, where only duty-ratios $D > 0.5$ occur, the steps in Figure 8.25 are not relevant. In other applications restrictions must be accepted, i.e. the optimal values can only be utilized for parts of the operation range.

However, the optimal phase shift values and balancing factors need to be computed offline. The results can be stored in LUTs $(\varphi_2(D), K_{b2}(D), ...)$. If there is not enough processor performance to perform the offline optimization, this procedure can be outsourced. But finding adequate start values remains challenging for multiple converter rails.

The second task is to determine the optimal K_{lag} for the master rail. Therefore the first task needs to be executed for the relevant K_{lag} range. The computational effort increases, respectively. An additional LUT is generated and is utilized like in the method with equal inductance values. Figure 8.34 shows, that it seems also conceivable to apply the generalized control law for equal inductance values. The control laws are very similar for wide ranges of the duty-ratio. Consequently, the computational effort could be reduced significantly by this approximation.

8.7 Summary

Current control of PFC rectifier in BCM and DCM can be established by a simple algorithm that is best suited to be realized as full digital control even for high switching and sampling frequencies due to low computational effort. By utilizing pure feed-forward current control there is no need of any current measurement. For a closed-loop implementation an additional current controller for the average input current can be applied.

The control concept can handle multi-rail interleaving without additional computational effort. The possibility of specific control of the DCM ratio leads to a novel fractional phase shedding method in contrast to conventional phase shedding, where only an integer number of converter rails is turned off. This novel continuous degree of freedom can be used to minimize switching losses at light load and even within a line half-cycle or to keep the switching frequency within a narrow band. If the inductance values are unequal due to manufacturing tolerances, the DCM ratio can also be employed to balance the inductor currents to equal peak or average values.

With interleaving several converters the first harmonic components are eliminated and the THD and the input current ripple are significantly reduced. In DCM further reduction can be attained by adjusting the DCM ratio. A universal control law can be generated for every number of paralleled converter rails to operate the converter with minimum THD_{DC} and current ripple at any duty-ratio. The method is not limited to the presented application. It can be utilized for all paralleled converter operating in DCM.

The DCM feed-forward algorithm with continuous phase shedding is well suited to enable the THD_{DC} minimization. By utilizing LUTs the control law can be implemented with little computational effort.

If the inductance values are unequal, the first harmonics are not longer eliminated by applying equal phase shift values. The optimal phase shifts needs to be computed depending on the inductance ratios for the entire duty-ratio range. Additionally, the balancing factor which gives every single converter rail an individual DCM ratio can be utilized to eliminate further harmonic components. The optimal values for the phase shifts and balancing factors are computed numerically with the Newton method. The computed values are only valid for the given inductance ratios and therefore need to be updated for each set of inductors. A generalized control law cannot be generated. For three and more parallel converter rails the presetting of adequate start values for the Newton method becomes more and more complicated. Additionally, the values for the optimal phase shift changes with steps at particular duty-ratios. Accordingly, restrictions have to be accepted so that an optimal elimination of harmonic components is not realizable in every application.

To find the optimal DCM ratio of the master rail for minimum THD_{DC} further computation cycles need to be performed. However, utilizing the universal control law from equal inductances is a good compromise.

9 Conclusions

Alternative control concepts for interleaved boost PFC rectifiers have been introduced in this thesis. The requirements for those concepts are sophisticated due to the fact that three different control tasks must be achieved at the same time:

- The inner current control loop needs to achieve nearly unity power factor by forcing the input current to track the shape of the sinusoidal line voltage as close as possible.
- The outer voltage control loop has to provide a nearly constant DC output voltage.
- The current balancing control must ensure equal rail power for the paralleled converters.

In addition, it is in the nature of PFC applications that the operating point varies continuously within every line half-cycle. Thus, the operation mode of the boost converter can change frequently between CCM and DCM.

Like for all power converters also for PFC rectifiers there are further general demands, such as high efficiency, high power density, good noise rejection and low cost.

All requirements are also the indicators for evaluating the performance of the presented control concepts. However, some control concepts are suited only for particular operation modes, what makes an unrestricted comparison regarding all categories impossible.

Analog control has the advantage of high control bandwidth, which is important for the current loop. With digital control the drawback of the limited bandwidth can be overcome in particular by applying feed-forward loops, adaptive control or non-linear algorithms. The semi-digital control concept shows, that it is not essential to implement a full digital control in order to achieve high flexibility. Almost the same performance can be achieved when only realizing the low bandwidth voltage control in digital. Fast control functions are retained in analog, for which reason only low computing power is required, which reduces the costs of the digital controller significantly.

Highest bandwidth in the current loop can be achieved by applying peak current control. Available DSPs or μCs with analog on-chip comparators enables digital peak current control and consequently a further mixed-signal PFC control concept. Digital slope compensation has been developed in order to avoid subharmonic oscillations at duty-ratios above 50%. Adaptive algorithms can be utilized to adjust the compensation and to ensure sinusoidal shape of the average inductor current.

All these control concepts are suited for interleaved PFC rectifiers, which are operated in CCM and DCM with constant switching frequency. Since the concepts result in equal operation modes, there is no difference in the achievable efficiency. Power management features such as phase shedding and load dependent adjustment of the switching frequency can contribute to higher efficiency at partial load. Also the THD in the input current and the power density of the power path are expected to be equal. Due to differences in

required analog circuitry and computational effort only little differences in the required printed circuit board (PCB) space and the costs for the control result for the different control concepts.

With operating the converter rails in BCM or DCM only, the realizable power level per rail is reduced. An applicable interleaving method is essential to reach higher power levels and to reduce the THD in the input current. But the varying switching frequency in these operation modes makes interleaving challenging. Two control concepts were presented, which provide multi-rail interleaving by applying digital control.

The already popular BCM control achieves a high power factor by applying a constant switch on-time for the boost switch during the whole line half-cycle. By turning on the switch in the first valley of the drain-source voltage after the ZCD signal, the switching losses are minimized. A digital phase shift control has been presented, which enables multi-rail interleaving. With the flexibility of the digital implementation it is possible to apply phase shedding and limit the switching frequency by maintaining optimal interleaving.

Current control of interleaved PFC rectifier operated in BCM and DCM can also be realized by a simple feed-forward algorithm. Only little computational effort is required for the presented control concept even for high switching frequencies and multi-rail interleaving. Current balancing is possible even in the case of inductance variations due to manufacturing tolerances. The DCM ratio can be controlled while still retaining the desired current average value. The adjustable DCM ratio establishes a novel scheme of fractional phase shedding in contrast to conventional phase shedding, where only an integer number of converter rails can be turned off. With this novel continuous degree of freedom the performance can be enhanced in different ways. The switching losses can be reduced at light load and even within a line half-cycle or the switching frequency can be kept within a narrow band. A promising method is introduced, which tracks the DCM ratio and the phase shift between the converter rails for every operating point in order to minimize the THD_{DC} in the input current.

The effort for interleaved operation of the presented PFC control concepts are briefly summarized in Table 9.1.

The introduction of digital control provides additional functionality for interleaved PFC rectifiers to improve the performance in different categories. Furthermore, with digital control it is possible to realize the PFC control in many ways. This study of different control concepts has shown that digital control is not a general solution for improved performance. It often makes sense to combine digital control with suitable analog parts such as analog comparators.

There is no control concept which is the best solution for all application. It is still up to the design engineer to choose the suitable control for each power converter according to the specifications.

Control concept	Control hardware effort for an additional rail	Computational effort for an additional rail	Effort for current balancing
Analog control	Additional current measurement, current compensator and clock signal (--)		Additional analog PWM circuit for each rail (-)
Full digital average current control	Additional current measurement (+)	Additional current control loop (-)	Inherent with separate current control loop for each rail (+)
Semi-digital control	Additional current measurement and current compensator (-)	None (++)	Additional analog PWM circuit for each rail (-)
Digital peak current mode control	Additional current measurement (+)	Additional slope compensation (o)	None (inherent) (++)
Digital BCM control	Additional ZCD signal Additional phase shift controller (on FPGA or with discrete components) (-)	None (regarding DSP or µC) (++)	Not mandatory in BCM Not implemented (+)
Feed-forward control for BCM and DCM	None (++)	None (++)	Not mandatory in BCM/DCM Only one additional multiplication for each rail (+)

Table 9.1: Properties of the PFC control concepts regarding the effort for multi-rail interleaving. Rating: (++): very good, (+): good, (o): reasonable, (-): poor, (--): very poor

A Appendix

A.1 Definition of Power Factor (PF) and Total Harmonic Distortion (THD)

The total harmonic distortion (THD) is defined as the ratio of the geometric sum of the harmonic components to the fundamental component. The THD of a current signal is computed as

$$\mathrm{THD}_i = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \cdots + I_n^2}}{I_1} \tag{A.1}$$

and of a voltage signal as

$$\mathrm{THD}_v = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots + V_n^2}}{V_1}. \tag{A.2}$$

Where I_k and V_k $(k = 1,2, \ldots, n)$ are the fundamental and the harmonic components of the current and the voltage signal.

The total harmonic distortion with respect to the average value of the input current $\bar{i}_{in}$ is defined as the ratio of the geometric sum of the harmonic components to the DC component:

$$\mathrm{THD}_{DC} = \frac{\sqrt{\sum_{n=1}^{\infty} I_n^2}}{\bar{i}_{in}} = \frac{\sqrt{I_1^2 + I_2^2 + I_3^2 + \cdots + I_n^2}}{\bar{i}_{in}} \tag{A.3}$$

In general the power factor (PF) is defined as ratio of real power to apparent power:

$$\mathrm{PF} = \frac{\text{real power}}{\text{apparent power}} = \frac{|P|}{V_{\mathrm{RMS}} I_{\mathrm{RMS}}} \tag{A.4}$$

Where the real power is the average over one cycle of the instantaneous product of current and voltage, and the apparent power is product of the current RMS value times the voltage RMS value.

For purely sinusoidal signals, it follows:

$$\mathrm{PF} = \frac{|P|}{S} = \frac{V_1 I_1 \cdot \cos\varphi}{V_1 I_1} = \cos\varphi \tag{A.5}$$

If the voltage and current contain harmonics, these need to be considered and the power factor results as

$$\mathrm{PF} = \frac{|P|}{V_1 I_1} \cdot \frac{1}{\sqrt{1 + \mathrm{THD}_v{}^2} \cdot \sqrt{1 + \mathrm{THD}_i{}^2}}. \tag{A.6}$$

In many cases the voltage is nearly pure sinusoidal and only the current contains significant harmonics. Thus, the THD_v is zero and the power factor can be computed with

$$\mathrm{PF} = \frac{|P|}{V_1 I_1} \cdot \frac{1}{\sqrt{1 + \mathrm{THD}_i{}^2}}. \tag{A.7}$$

A.2 Fourier Coefficient Calculation of DCM Inductor Current

The calculation of the Fourier coefficients Q_ν of the periodic DCM inductor current signal $i(t)$, which is shown in Figure A.1, is derived in the following. Because only the harmonic components should be analyzed, the DC component is set to zero.

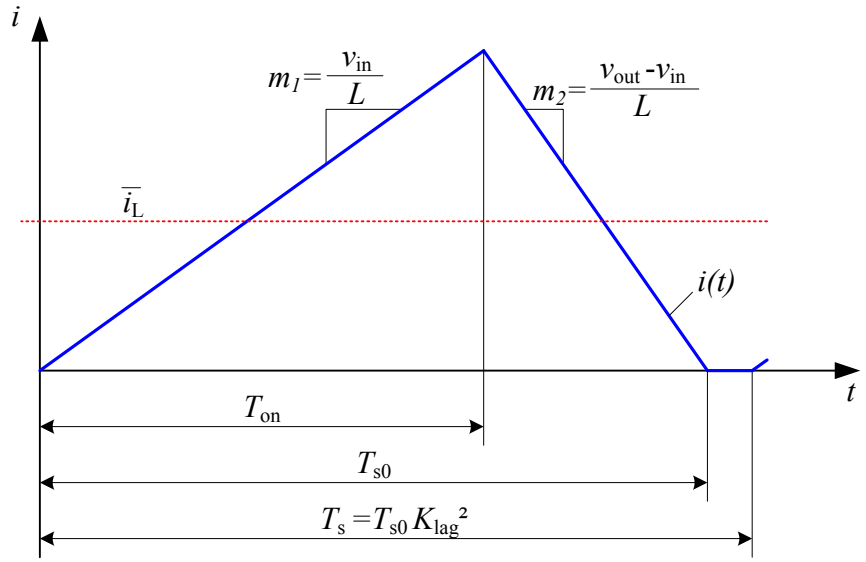

Figure A.1: Single cycle of the periodic inductor current in DCM

The Fourier coefficients of a periodic signal are calculated with

$$Q_\nu = \frac{1}{T} \int_0^T i(t) \cdot e^{-j\nu\omega t} dt. \tag{A.8}$$

If the signal is a continuous function, the integration by parts

$$\int_a^b f'(x) \cdot g(x)dx = [f(x) \cdot g(x)]_a^b - \int_a^b f(x) \cdot g'(x)dx \tag{A.9}$$

can be utilized. In this case

$$f'(t) = e^{-j\nu\omega t} \tag{A.10}$$

and

$$g(t) = i(t) \tag{A.11}$$

are applied.

For the calculation of the Fourier coefficients it follows

$$Q_\nu = \frac{1}{T}\int_0^T i(t) \cdot e^{-j\nu\omega t}dt = \left[\frac{i(t) \cdot e^{-j\nu\omega t}}{-j\nu\omega T}\right]_0^T + \frac{1}{j\nu\omega T}\int_0^T i'(t) \cdot e^{-j\nu\omega t}dt. \tag{A.12}$$

Since the DC component of the signal $i(t)$ is zero and due to the periodicity $i(0) = i(T)$, the first term on the right side of Eq. A.11 is zero. For solving the second term the time derivative $i'(t)$ is required:

$$i'(t) = \begin{cases} m_1 & \text{for } 0 < t \leq T_{on} \\ -m_2 & \text{for } T_{on} < t \leq T_{s0} \\ 0 & \text{for } T_{s0} < t \leq T \end{cases} \tag{A.13}$$

Thus, it follows

$$Q_\nu = \frac{1}{j\nu\omega T}\left[\int_0^{T_{on}} m_1 \cdot e^{-j\nu\omega t}dt - \int_{T_{on}}^{T_{s0}} m_2 \cdot e^{-j\nu\omega t}dt\right]. \tag{A.14}$$

Solving this equation we get

$$Q_\nu = \frac{1}{(\omega\nu)^2 T}\left[(m_1 + m_2)e^{-j\nu\omega T_{on}} - m_1 - m_2\, e^{-j\nu\omega T_{s0}}\right]. \tag{A.15}$$

For the given application the Fourier coefficients need to be computed depending on the average inductor current $\bar{i}_L$, the voltage ratio $D = (v_{out} - v_{in})/v_{out}$ and the DCM ratio K_{lag}. Therefore the unknown values ω, m_1, m_2, T_{on}, T_{s0} and T must be eliminated with:

$$\omega = 2\pi/T \tag{A.16}$$

$$m_1 = \frac{v_{in}}{L} \tag{A.17}$$

$$m_2 = \frac{v_{out} - v_{in}}{L} \tag{A.18}$$

$$T_{on} = \frac{2\bar{i}_L L}{v_{in}} K_{lag} \tag{A.19}$$

$$T_{s0} = \frac{2\bar{i}_L L}{D v_{in}} K_{lag} \tag{A.20}$$

$$T = \frac{T_{on}}{D} K_{lag} \tag{A.21}$$

After substitution of these values the required equation for the Fourier coefficient results as

$$Q_\nu = \frac{\bar{i}_L \, K_{lag}^2}{2\pi^2 \nu^2 D(1-D)} \left[e^{-j\nu D \frac{2\pi}{K_{lag}}} - 1 + D - D \, e^{-j\nu \frac{2\pi}{K_{lag}}} \right]. \tag{A.22}$$

In Figure A.2 the reconstruction of a given signal is illustrated with $n = 3$ and $n = 15$ Fourier coefficients.

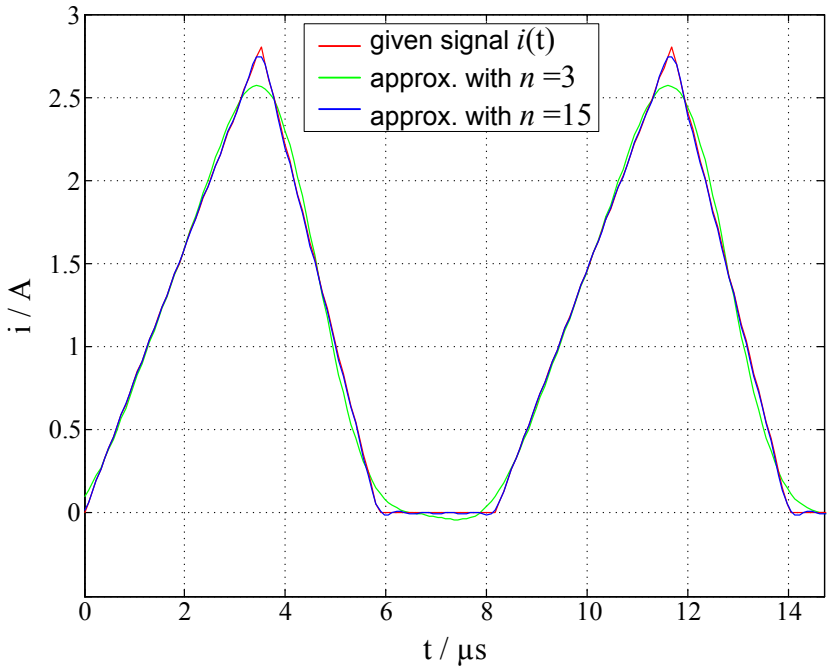

Figure A.2: Replication of DCM current signal with Fourier series of length n ($\bar{i}_L = 1\text{A}; D = 0.6; K_{lag} = 1.4$)

A.3 Harmonic Elimination Utilizing Newton Algorithm

In order to solve the nonlinear system of equation

$$\begin{aligned} F_1 &= Re\{Q_{1,1}\} + Re\{Q_{2,1}\} + Re\{Q_{3,1}\} = 0 \\ F_2 &= Im\{Q_{1,1}\} + Im\{Q_{2,1}\} + Im\{Q_{3,1}\} = 0 \\ F_3 &= Re\{Q_{1,2}\} + Re\{Q_{2,2}\} + Re\{Q_{3,2}\} = 0 \\ F_4 &= Im\{Q_{1,2}\} + Im\{Q_{2,2}\} + Im\{Q_{3,2}\} = 0 \end{aligned} \tag{A.23}$$

the numeric Newton method is employed. Where $Q_{i,\nu}$ represents the equation to compute the Fourier coefficient ν of the rail i.

The system of equation is merged to the multidimensional function vector

$$F(x) = \begin{bmatrix} F_1 \\ F_2 \\ F_3 \\ F_4 \end{bmatrix}. \tag{A.24}$$

For the initial step of the iterative calculation the start values

$$x_0 = \begin{bmatrix} \varphi_{2,0} \\ K_{b2,0} \\ \varphi_{3,0} \\ K_{b3,0} \end{bmatrix} \tag{A.25}$$

needs to be defined, which should be ideally already near the final solution.

In iterative steps the calculation of

$$J(x_k)\Delta x_k = -F(x_k) \tag{A.26}$$

is repeated. Where

$$J(x) = \begin{pmatrix} \frac{\partial F_1}{\partial x_1} & \frac{\partial F_1}{\partial x_2} & \frac{\partial F_1}{\partial x_3} & \frac{\partial F_1}{\partial x_4} \\ \frac{\partial F_2}{\partial x_1} & \frac{\partial F_2}{\partial x_2} & \frac{\partial F_2}{\partial x_3} & \frac{\partial F_2}{\partial x_4} \\ \frac{\partial F_3}{\partial x_1} & \frac{\partial F_3}{\partial x_2} & \frac{\partial F_3}{\partial x_3} & \frac{\partial F_3}{\partial x_4} \\ \frac{\partial F_4}{\partial x_1} & \frac{\partial F_4}{\partial x_2} & \frac{\partial F_4}{\partial x_3} & \frac{\partial F_4}{\partial x_4} \end{pmatrix} \tag{A.27}$$

is the Jacobian matrix.

The next iterative step is performed with new start values, determined by

$$x_{k+1} = x_k + \Delta x_k. \tag{A.28}$$

As terminating condition a lower boundary

$$\|F(x_k)\| < \varepsilon \tag{A.29}$$

can be defined.

Short Forms

ADC	analog to digital converter
BCM	boundary conduction mode
CCM	continuous conduction mode
DCM	discontinuous conduction mode
DPS	distributed power system
DSP	digital signal processor
EMI	electromagnetic interferences
LFF	load feed-forward
LSB	least significant bit
PCB	printed circuit board
PF	power factor
PFC	power factor correction
POL	point of load
PSFB	phase shift full bridge
PSU	power supply unit
PWM	pulse width modulation
RMS	root mean square
SMPS	switched mode power supply
THD	total harmonic distortion
THD_{DC}	total harmonic distortion with respect to the DC component
VFC	voltage feed-forward control
VRM	voltage regulator module
ZCD	zero current detection
µC	microcontroller

Definition of Symbols

C	converter output capacitance
d	duty ratio
$d_{ff,CCM}$	feed-forward duty ratio in CCM
$d_{ff,DCM}$	feed-forward duty ratio in DCM
D	boost converter voltage ratio ($1 - v_{in}/v_{out}$); in CCM it follows: $D = d$
f_c	control loop crossover frequency
f_{clk}	DPWM counter clock frequency
f_s	switching frequency
$f_{s,total}$	total switching frequency seen by the EMI filter
$G_{cc}(s)$	current controller transfer function
G_{in}	input conductance of the converter
$G_I(s)$	transfer function of I-type controler
$G_{ic}(s)$	control-to-inductor current transfer function at peak current control
G_{id}(s)	control-to-inductor current transfer function of the boost converter in CCM
$G_{id,DCM}(s)$	control-to-inductor current transfer function of the boost converter in DCM
$G_{i,BCM}(s)$	control-to-inductor current transfer function of the boost converter in BCM
$G_{load}(s)$	transfer function of the voltage loop control path
$G_o(s)$	open-loop transfer function
$G_{PWM}(s)$	transfer function of the PWM unit
$G_{vc}(s)$	voltage loop compensator transfer function
I_0	steady state valley inductor current
i_{ac}	line current
I_{ac}	RMS value of the line current
$I_{ac,ref}$	RMS reference value of the line current
i_{cmp}	current threshold for comparator at peak current control
$i_{cmp,DCM}$	current threshold for comparator at peak current control in DCM

i_{in}	input current after rectification
$\overline{i}_{in}$	average value of the input current during one switching cycle
Δi_{in}	input current ripple
i_L	inductor current
$\overline{i}_L$	average value of the inductor current during one switching cycle
$i_{L,min}$	valley inductor current
$\hat{\imath}_L$	inductor current peak value within one switching cycle
i_n	sampled valley inductor current in cycle n
$\hat{\imath}_{ref}$	input current reference value within one line half-cycle
i_{ref}	reference current
$i_{ref,ff}$	feed-forward reference current for peak current control
$i_{ref,ff,DCM}$	feed-forward reference current for peak current control in DCM
$\Delta\overline{i}_L$	deviation in the average inductor current
$\Delta i_{L,CCM}$	inductor current ripple in CCM
$\Delta i_{L,DCM}$	inductor current ripple in DCM
Δi_{sc}	deviation in the inductor current caused by slope compensation
Δi_{sd}	deviation in the inductor current caused by delayed sampling
K_b	balancing factor
k_{sc}	compensation factor for digital slope compensation
K_{lag}	DCM ratio
k_r	factor for digital slope compensation to emulate constant compensation ramp
L	inductance value
M	conversion ratio of the boost converter in CCM
M_{DCM}	conversion ratio of the boost converter in DCM
m_1	rising current slope
m_2	falling current slope
m_{sc}	equivalent current slope of the slope compensation ramp
P_{out}	output power
P_{ref}	output power reference value
Q_v	Fourier coefficient

R	load resistance
T_{adj}	Time offset to adjust phase shift error in BCM
T_{clk}	DPWM counter clock period
T_d	dead time
T_{on}	switch-on duration
$T_{on,adj}$	switch-on duration determined by current controller
$T_{on,ff}$	switch-on duration determined by feed-forward algorithm
$T_{on,PS}$	switch-on duration for phase shedding case
T_{off}	switch-off duration
T_s	switching period
$T_{s,min}$	minimum valid period time
T_{sd}	sample delay
$T_{shift,PS}$	phase shift delay for phase shedding case
v_{ac}	line voltage
V_{ac}	RMS value of the line voltage
v_C	output capacitor voltage ($v_C = v_{out}$)
v_{clk}	clock signal
v_{DS}	drain-source voltage of MOSFET
v_g	gate-source voltage of MOSFET
v_{in}	input voltage after rectification
$\hat{v}_{in}$	input voltage peak value
V_{in}	RMS value of the inputvoltage ($V_{in} = V_{ac}$)
v_{out}	output voltage
κ	correction factor for sample correction in DCM
σ_k	phase shift offset for rail k of the phase shift controller in BCM
γ	compensation gain for digital slope compensation
ω_c	crossover angular frequency

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