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Master Thesis

Integration of Electrostatic Simulation in FEM Magnetics Toolbox for Capacitance Optimization in Magnetic Components

by

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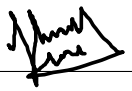
Paderborn, 28.04.2025 

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Abstract

Inductors and transformers are fundamental components in power electronic converters, playing critical roles in energy storage, and power conversion. However, parasitic capacitance, an inherent and often undesirable effect in these components, can significantly impact their performance, especially in fast-switching applications, where the high voltage slew rates ($\mathrm{d}v/\mathrm{d}t$) generated by modern semiconductor devices such as GaN and SiC lead to substantial capacitive currents [1] [2]. Parasitic capacitance arises from the capacitive coupling between winding turns, layers, and the core, leading to resonant behavior, over voltage, and reduced efficiency. Addressing this challenge requires accurate modeling and optimization of parasitic capacitance during the design phase.

This thesis focuses on integrating electrostatic simulation capabilities into the FEM Magnetics Toolbox (FEMMT), an open-source tool developed by the Department of Power Electronics and Electrical Drives (LEA) at Paderborn University. By extending FEMMT to include electrostatic simulation, this work enables a comprehensive analysis of both magnetic and capacitive effects in inductors and transformers.

After implementing the electrostatic simulation into the FEM Magnetics Toolbox (FEMMT), the thesis further focuses on the extraction of parasitic capacitances for the capacitive equivalent circuits of inductors and transformers, followed by an optimization study aimed at minimizing the parasitic capacitances in inductors.

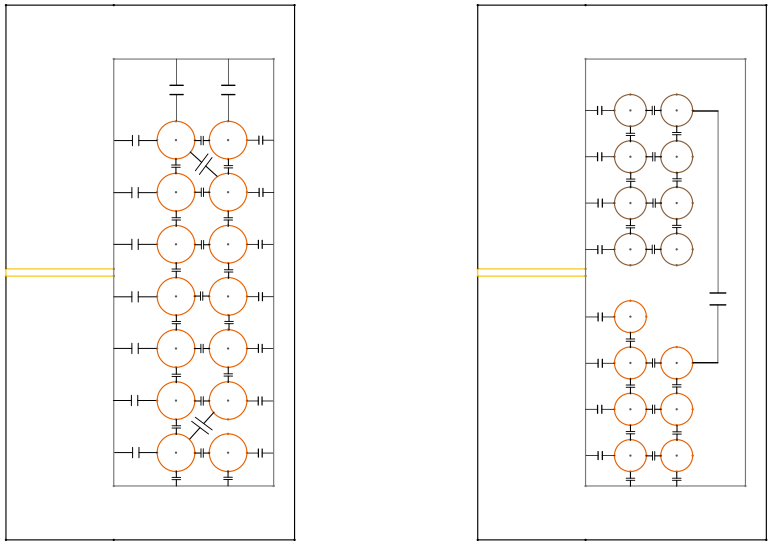
Contents

1 Introduction

Inductors and transformers are essential components in power electronics, performing key functions such as energy storage, power conversion, and electrical isolation. In DC-DC converters, inductors efficiently store and transfer energy, while transformers provide galvanic isolation between input and output stages [3]. However, with the advent of fast-switching semiconductor technologies such as GaN and SiC, the resulting high voltage slew rates lead to significant capacitive currents. As a result, parasitic capacitance within magnetic components has become a critical factor that affects performance, especially in high-speed switching applications [4].

Parasitic capacitance refers to unintended capacitance arising from the proximity of conductive elements within magnetic components. The presence of parasitic capacitance in inductors and transformers is illustrated in Fig. 1.1. In inductors, this capacitance typically arises between adjacent winding turns, as depicted in Fig. 1.1a. Similarly, in transformers, parasitic capacitance occurs due to coupling between winding layers, individual turns, and the core, as shown in Fig. 1.1b. These parasitic effects can adversely affect the performance of magnetic components by inducing resonant behavior, and overvoltage. Parasitic capacitance interacts primarily with the fast voltage transients that occur during the switching events of modern power semiconductors. The resulting capacitive current can contribute to undesirable effects such as common-mode noise and increased electromagnetic interference [4]. Common-mode currents, in particular, represent a major challenge associated with parasitic capacitance. They can lead to EMC test failures and may necessitate the use of over-sized and costly common-mode filters to achieve compliance [4]. As a consequence, careful modeling and mitigation of parasitic capacitance have become essential in ensuring reliable and compliant converter operation.

However, due to the complexity of the field distribution in magnetic components, certain approximations are applied to simplify the problem. These approximations are based on the fact that regions with low electric field strength have minimal influence on the overall capacitance and can therefore be neglected. In transformers, a simplified model is used in which each winding and the core are treated as nodes with electrostatic potentials. The capacitances between these nodes form a capacitive network, as shown in Fig. 1.2.



(a) Simplified model of parasitic capacitance in an inductor

(b) Simplified model of parasitic capacitance in a transformer

Fig. 1.1: Simplified models of parasitic capacitance in an inductor and a transformer

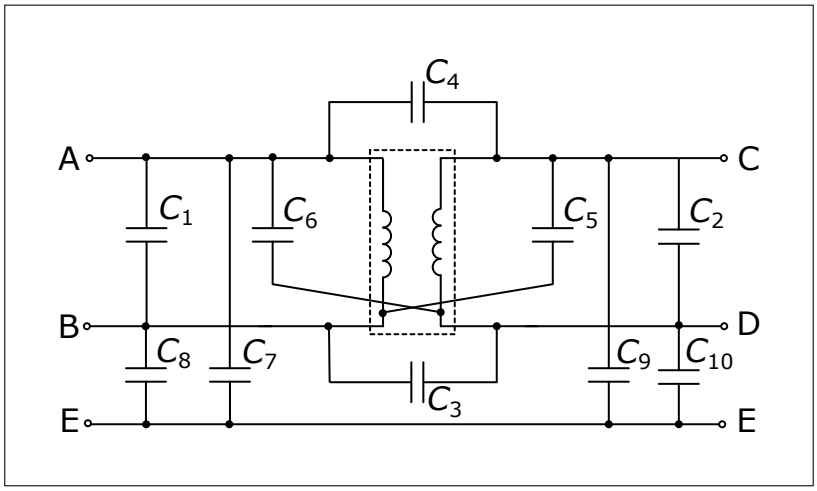


Fig. 1.2: Simplified equivalent circuit of parasitic capacitance in a transformer

In order to determine and analyze the parasitic capacitance in inductors and transformers, it is necessary to model both magnetic and electrostatic effects. While magnetic simulations capture essential properties such as inductance and losses, they do not account for the capacitive coupling between conductive elements. Therefore, this master's thesis focuses primarily on integrating electrostatic simulation capabilities into the FEM Magnetics Toolbox (FEMMT)[5]. FEMMT, developed by the Department of Power Electronics and Electrical Drives (LEA) at Paderborn University, is designed to simulate magnetic properties, including core and winding geometries. The extended version used in this work additionally supports electrostatic simulations, enabling the analysis of parasitic capacitance within magnetic components.

To validate the accuracy of the integrated electrostatic simulation, example simulations are performed using FEMMT. The simulation results are first cross-verified with established tools such as ANSYS [6] to ensure consistency and reliability. Following this, the results are compared with measurements obtained from an impedance analyzer.

However, a key objective of this thesis is to study the effect of parasitic capacitance on LLC converter performance. Special attention is given to the comparison of two transformer prototypes, each with different spatial separation between the windings, to evaluate their impact on the converter behavior. In addition, an optimization study on the inductor is conducted, focusing on minimizing parasitic capacitances through various winding arrangements, while maintaining the same inductance and loss characteristics.

2 Basic Electrostatics

The integration of electrostatic simulations into the FEM Magnetics Toolbox (FEMMT) require a fundamental understanding of the principles governing electrostatics. These principles, described by Maxwell's equations, explain how electric fields and potentials behave in linear, homogeneous, and isotropic media.

Gauss's law relates the electric flux density $\boldsymbol{D}$ to the volume charge density ρ_v. The integral form is given by [7]

$$\oint_S \boldsymbol{D} \cdot \mathrm{d}\boldsymbol{S} = \int_v \rho_\mathrm{v} \, \mathrm{d}v = Q \tag{2.1}$$

where Q is the total charge enclosed by the surface S. By applying the divergence theorem, the differential form of Gauss's law is obtained as [7]

$$\nabla \cdot \boldsymbol{D} = \rho_\mathrm{v}. \tag{2.2}$$

Furthermore, electrostatic fields are conservative, meaning they exhibit no circulation. This is expressed by [7]

$$\oint_C \boldsymbol{E} \cdot \mathrm{d}\boldsymbol{l} = 0 \tag{2.3}$$

which indicates that the line integral of the electric field $\boldsymbol{E}$ around any closed path C is zero. Applying Stokes's theorem leads to the differential expression [7]

$$\nabla \times \boldsymbol{E} = 0. \tag{2.4}$$

However, the electric flux density $\boldsymbol{D}$ is proportional to the electric field $\boldsymbol{E}$, with the proportionality constant depending on the permittivity of the medium $\varepsilon_0 \varepsilon_r$. the relationship is written as [7]

$$\boldsymbol{D} = \varepsilon_0 \varepsilon_\mathrm{r} \boldsymbol{E}. \tag{2.5}$$

Since the curl of the gradient of any scalar function is always zero $\nabla \times \nabla\varphi = 0$, it follows that $\boldsymbol{E}$ must be the gradient of a scalar function. This confirms the relationship between electric field intensity $\boldsymbol{E}$ and the potential φ, as shown in equation (2.6). The negative

sign indicates that the electric field intensity $\boldsymbol{E}$ points from higher potential to lower potential [7].

$$\boldsymbol{E} = -\nabla\varphi. \tag{2.6}$$

By applying Gauss's law in equation (2.2) and the relationship between the electric field $\boldsymbol{E}$ and potential φ, the most important equation for solving electrostatic problem, know as Poisson's equation, is obtained, as shown in equation (2.7). Poisson's equation establishes a direct relationship between the scalar potential φ and the charge distribution ρ_v within a general medium [7].

$$\nabla \cdot (-\varepsilon\nabla\varphi) = \rho_\mathrm{v}. \tag{2.7}$$

For homogeneous medium, equation (2.7) becomes as follows

$$\nabla^2\varphi = \rho_\mathrm{v}. \tag{2.8}$$

Furthermore, one important quantity of interest in electrostatics is the stored energy density in electrostatic fields. The stored energy density is crucial for calculating other parameters, such as the capacitance of a system, which depends on the ability of the electric field to store energy between conductors. For a system with an electric field $\boldsymbol{E}$ and electric displacement $\boldsymbol{D}$, the electrostatic energy W is expressed as [7]

$$W = \frac{1}{2}\int_v \boldsymbol{D}\cdot\boldsymbol{E}\,\mathrm{d}v = \frac{1}{2}\int_v \varepsilon_0\varepsilon_r E^2\,\mathrm{d}v. \tag{2.9}$$

With the energy stored in the system now established, the capacitance parameter, which is central to our goal of implementing electrostatic simulation in FEMMT, can now be calculated. Capacitance can be defined either by the ratio of the charge stored on a conductor to the voltage applied across the conductors [7]

$$C = \frac{Q}{\varphi} = \frac{\varepsilon \oint \boldsymbol{E}\cdot\mathrm{d}\boldsymbol{S}}{\int \boldsymbol{E}\cdot\mathrm{d}\boldsymbol{l}} = \frac{2W}{\varphi^2} \tag{2.10}$$

or through its relationship with the stored electrostatic energy [7]

$$C = \frac{2W}{\varphi^2}\,. \tag{2.11}$$

In conclusion, these fundamental principles of electrostatics are used for integrating electrostatic simulation capabilities into the FEM Magnetics Toolbox (FEMMT). The electrostatic field equations, along with material properties and boundary conditions, are directly applied in FEMMT to compute potential distributions and calculate parasitic capacitance in magnetic components.

3 Advancements in FEMMT: Incorporating Electrostatic Simulation

Extending FEMMT's capabilities to include electrostatic simulations marks an important step in its development. Initially designed to simulate magnetic components in both frequency and time domain [8], FEMMT is now evolving into more versatile simulation tool capable of analyzing electrostatic phenomena. This section discusses the integration of electrostatic simulation, key structural adaptions, and enhancement to FEMMT's codebase to accommodate these new functionalities.

3.1 Electrostatic Simulation Workflow in FEMMT

The structure of FEMMT consists of a combination of Python files and non-Python text files that define simulation parameters, material properties, and solver instructions. FEMMT leverages the GetDP finite element solver, interfacing with GMSH mesh generator through the ONELAB API [9]. ONELAB's Python module acts as a bridge, coordinating the transfer of mesh and solver data between Python scripts and sub-clients that run the simulations. Furthermore; the GetDP solver files are identified by the ".pro" extension, while mesh files use the ".msh" extension. The result files have the ".pos" extension for field solutions and ".dat" for global quantities [10].

To enable electrostatic simulations in FEMMT, specific solver scripts such as "electrostatic_solver.pro", "electrostatic_fields.pro", "electrostatic_values.pro" and "ind_axi_python_controlled_electrostatic.pro" were introduced.

The "ind_axi_python_controlled_electrostatic.pro" file forms a core component of the GetDP script, defining essential elements such as geometry, physical parameters, boundary conditions, resolution methods, equations, and related objects. The "electrostatic_solver.pro" file is responsible for solving these equations, handling the mathematical operations required to compute the electrostatic potential, field distributions, and other related quantities.

In essence, the inclusion of these electrostatic-specific files has enhanced FEMMT's capabilities, transforming it from a tool primarily focused on magnetic simulations to a versatile platform capable of both magnetic and electrostatic analyses. This marks a significant advancement in FEMMT's ongoing development, including the modeling of parasitic capacitance and electric field behavior in magnetic components. Notably, the internal structure and computational flow used for electrostatic simulation in FEMMT, as illustrated in Fig. 3.1, follow the same architecture as that used for electromagnetic simulation [11].

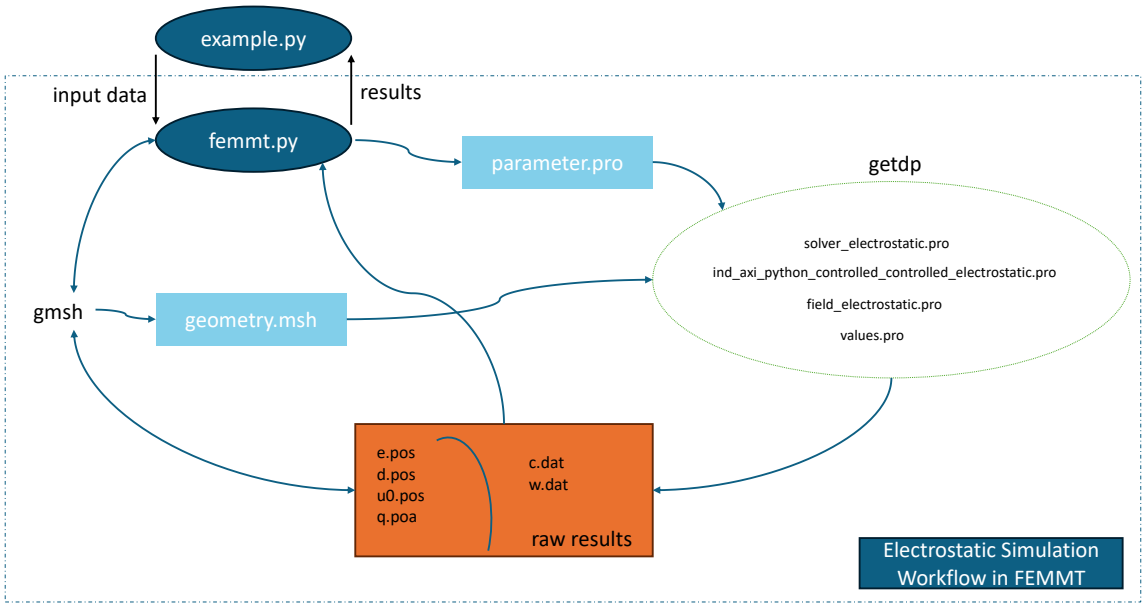


Fig. 3.1: Electrostatic simulation workflow in FEMMT

3.2 Constructing Objects for Electrostatic Simulation Analysis

FEM simulations require precise definitions of materials, boundary conditions, and excitation methods. Properly defining these elements ensures that the computed electric fields and parasitic capacitances closely reflect real-world behavior. This section details the key steps involved in constructing objects for electrostatic simulation analysis, including the definition of geometry, material properties, winding schemes, and excitation strategies.

3.2.1 Geometry

In electrostatic simulations, the geometry is crucial in determining how electric fields interact within and around magnetic components. This interaction is influenced by both the physical layout and the material properties of various components, such as the core, conductor insulation, bobbin insulation, and surrounding air. The definition of material properties, particularly the relative permittivity ε_r, directly affects the electric field distribution and the calculation of parasitic capacitance. Materials with different dielectric properties can alter the electric field intensity and displacement, thereby influencing energy storage and field coupling.

Furthermore, the winding scheme, including the number of turns, turn-to-turn spacing, and layer arrangement, plays a critical role in electrostatic simulations. Variations in the winding scheme can lead to different capacitive couplings between turns, layers, and the core.

In this section two key aspects are discussed in detail, namely material properties and the winding scheme, highlighting their roles in accurately modeling electrostatic phenomena and improving simulation reliability.

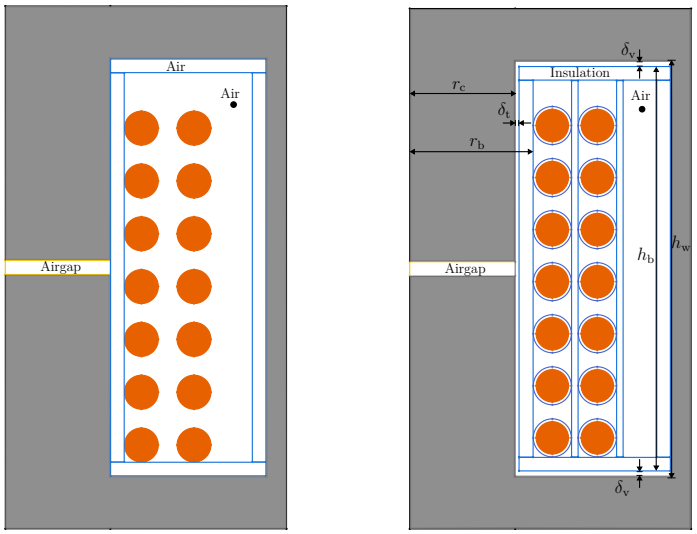
3.2.1.1 Material Properties

In order to conduct reliable electrostatic simulations, precise definitions of geometry and material properties are crucial. While the geometry in previous magnetic simulations primarily focused on core and winding configurations, electrostatic simulations require additional details to accurately capture capacitive effects. This includes defining the insulation layers around each winding turn and assigning materials to components such as the bobbin (core insulation), conductor insulation, layer insulation, and the surrounding air.

In the inductor geometry setup, shown in Fig. 3.2a, all insulation regions, including the conductor insulation, bobbin insulation, and surrounding space, were assigned as air by default. This simplified approximation did not account for the influence of different material properties on the electric field distribution. In the modified geometry, depicted in Fig. 3.2b, these regions are now accurately defined with their respective materials. The conductor insulation, bobbin insulation, layer insulation, and core insulation are assigned appropriate permittivity values to reflect their physical properties.

Additionally, a small gap is observed between the core and the core insulation (bobbin) in Fig. 3.2b. This gap arises due to a dimensional mismatch between the bobbin and the core. Specifically, this gap results from a slight difference between the inner diameter of the core and the inner diameter of the bobbin, as well as minor discrepancies in the top and bottom clearances. The radial gap δ_t between the bobbin and the core can be calculated as:

$$\delta_\mathrm{t} = r_b - r_c \tag{3.1}$$



(a) Inductor geometry with only air insulation

(b) Inductor geometry with different insulation materials

Fig. 3.2: Inductor geometry in FEMMT: (a) with only air insulation, (b) with core, layer, and conductor insulation materials

where r_b and r_c represent half of the inner diameters of the bobbin and core, respectively. Similarly, the vertical gap δ_v accounts for the gap at the top and bottom of the bobbin, arising from differences in height between the core window and the bobbin. It is defined as:

$$\delta_v = \frac{h_w - h_b}{2} \tag{3.2}$$

In Tab. 3.1, the material properties for different regions in the electrostatic simulation are defined, with relative permittivity values assigned based on the dielectric properties of each material. The air region is assigned a relative permittivity of 1, representing a free-space environment. The core has a high permittivity value of 100 k, accounting for both its magnetic and dielectric properties. The bobbin insulation is characterized by a relative permittivity of 2.7 [12]. The Polyester film, serving as the conductor insulation, exhibits temperature-dependent permittivity, ranging from 3.0 to 3.6 over a temperature range of $-40\,°C$ to $160\,°C$, across frequencies from 50 Hz to 1 MHz . The influence of frequency on polyester's permittivity is minimal, particularly at higher temperatures, where thermal effects dominate [13]. According to room-temperature data sheet, kapton insulation, which serves as the layer insulation between each layer of turns, has a relative permittivity of 3.4 [14]. These assignments ensure that the electric field distribution and parasitic capacitance are calculated more accurately by incorporating the correct material properties.

Tab. 3.1: Material permittivity assignment in electrostatic simulation.

Type	Relative permittivity
Air	1
Core	100 k
Bobbin	2.7
Kapton	3.4
Polyester	3 - 3.6

To investigate the influence of geometric modifications on the stored electrostatic energy, four different inductor configurations were simulated using FEMMT. The baseline model consists of a standard geometry using only air insulation. Subsequent configurations introduce insulation materials around the core, between winding layers, and finally around each conductor.

Fig. 3.3 presents the evolution of stored electrostatic energy with each geometry refinement. It can be observed that the introduction of a dielectric insulation material around the core yields the most significant increase (72.5 %). The effect of layer insulation is minimal due to the relatively small change in field distribution, while the conductor insulation provides an additional 32.2 % increase. Overall, the optimized inductor geometry results in a 130.2 % increase in stored electrostatic energy compared to the initial configuration. This demonstrates the importance of considering dielectric materials in magnetic designs for accurate electrostatic modeling.

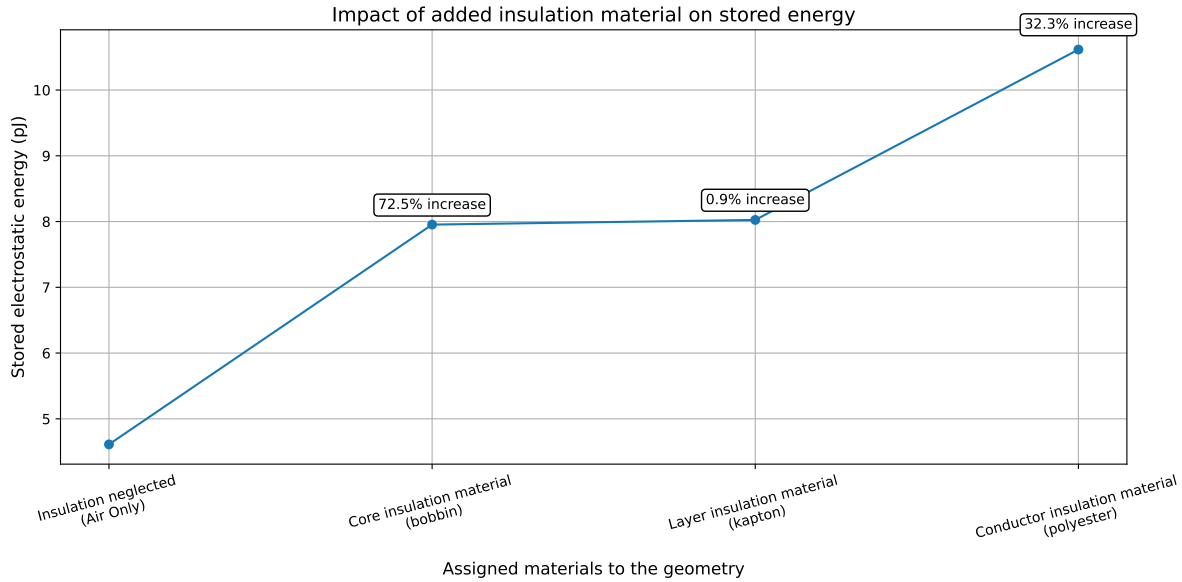


Fig. 3.3: Stored electrostatic energy of an inductor with different added insulation

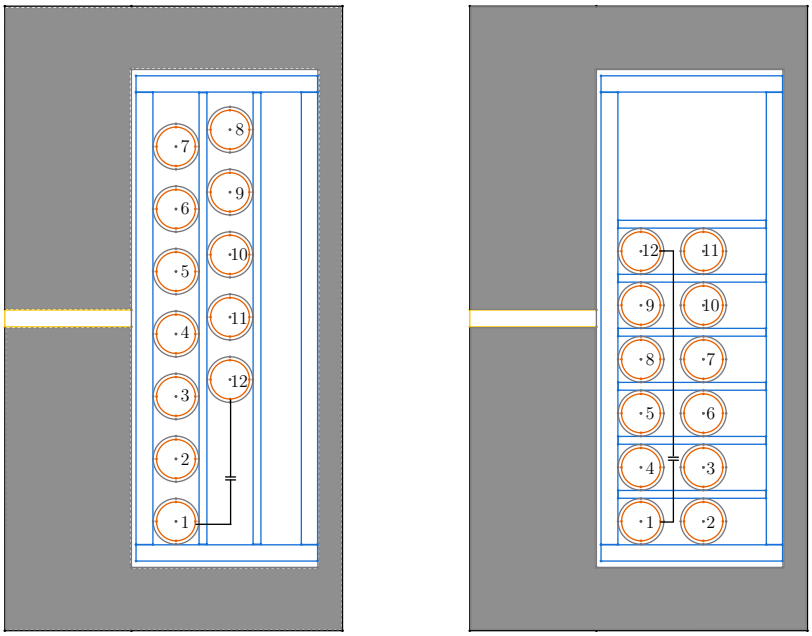
3.2.1.2 Winding Scheme

The winding scheme significantly influences parasitic capacitance by affecting the spatial arrangement and proximity of the winding turns. In Fig. 3.4, two different winding schemes show that selecting a proper winding schemes is essential to control parasitic capacitance, each with a distinct arrangement of turns. In the vertical movement scheme, shown in Fig. 3.4a, the turns are wound sequentially from the bottom to the top within each column. Turn 1 is placed at the bottom, followed by turn 2 directly above it, and so forth, with subsequent turns continuing in the next column after the first column is completed. This arrangement minimizes the physical separation between the first and last turns, resulting in a higher capacitance due to the reduced distance between them. Additionally, because the turns are vertically aligned, the overlapping surface area between adjacent turns is maximized, further increasing the capacitive coupling between them.

On the other hand, the horizontal movement scheme, depicted in Fig. 3.4b, arranges the turns in a horizontal sequence across the layer. Instead of stacking turns vertically, they are positioned side-by-side, and the winding continues horizontally before moving to the next row. This configuration shifts the primary capacitive coupling to adjacent turns within the same layer, altering the capacitance distribution compared to the vertical scheme. However, the introduction of layer insulation between stacked layers introduces materials with higher permittivity, which can increase the overall capacitance due to the dielectric properties of the insulation.

There are multiple winding configurations, each influencing parasitic capacitance in different ways. While the current discussion presents these two arrangements, further analysis will focus on identifying optimal designs that minimize capacitance, and enhance electrostatic performance. A deeper exploration of alternative configurations will be discussed later, aiming to determine the most effective approach based on specific design requirements. For now, these presented configurations offer insight into how different winding schemes impact capacitance, providing a basis for selecting the most suitable design.

The implementation of the distances between turns within each layer and between the layers themselves has also been incorporated. This is necessary because the number of turns in each layer can vary due to design constraints and manufacturing tolerances. It is important to note that both inter-turn and inter-layer capacitances contribute significantly to the overall measured capacitance [15] [16]. In practice, the number of turns per layer is often not consistent, which can lead to variations in the electric field distribution within the component and, consequently, in these capacitances. Fig. 3.5 illustrates the spacing between winding turns in an inductor, with labeled distances representing both horizontal and vertical separations between adjacent turns.



(a) Vertical movement **(b)** Horizontal movement

Fig. 3.4: Winding scheme order in FEMMT

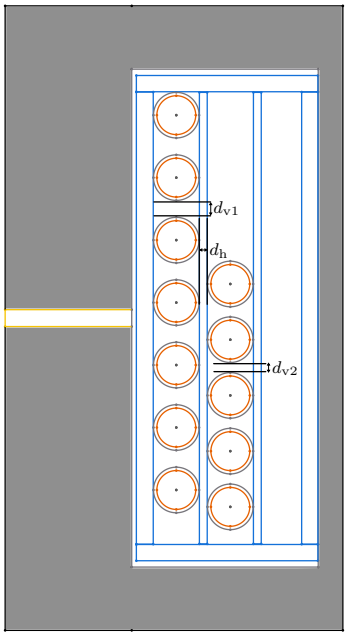


Fig. 3.5: Different distances between layers and adjacent turns

3.2.2 Excitation

In FEMMT, the excitation for electrostatic simulation is implemented by assigning a Dirichlet boundary condition, where a fixed voltage is applied to each turn of the winding, as shown in Listing 3.1. By prescribing a specific potential to each turn, the simulation accurately captures localized potential differences that drive electric field interactions between adjacent conductors. This approach enables precise modeling of capacitive coupling effects, allowing for a comprehensive analysis of how parasitic capacitance influences the overall electrical behavior of the component. Alternatively, instead of applying a fixed voltage, it is also possible to assign charges to each turn as seen in 3.2, which provides another method for defining the electrostatic excitation. This charge-based approach can be useful in cases where the total charge distribution needs to be controlled or analyzed separately from voltage-driven excitations.

```
// Assign a voltage to each turn of each winding
For n In {1:n_windings}
 nbturns~{n} = NbrCond~{n} / SymFactor;
    For turn In {1:nbturns~{n}}
      Val_Potential_Turn~{n}~{turn} = Voltage~{n}~{turn};
    EndFor
EndFor
```

Listing 3.1: Voltage assignment to winding turns in FEMMT

```
// Assign a charge to each turn of each winding
For n In {1:n_windings}
  nbturns~{n} = NbrCond~{n} / SymFactor;
    For turn In {1:nbturns~{n}}
      Cha_Potential_Turn~{n}~{turn} = Charge~{n}~{turn};
    EndFor
EndFor
```

Listing 3.2: Charge assignment to winding turns in FEMMT

However, the entire core region can be assigned a specific voltage, including the possibility of grounding the whole core. This means that rather than grounding only specific points or surfaces, the entire volume of the core can be set to a uniform potential. This configuration ensures that all regions within the core maintain the same voltage, which can significantly influence the electric field distribution and capacitive coupling within the simulation. Additionally, depending on the simulation requirements, the core can also be left floating or assigned a different potential value to accurately reflect real-world operating conditions. However, the outer boundary of the simulation domain can also be configured to be grounded or floated. These choices are based on the fact that the core's electrical state is crucial for capturing realistic operating scenarios in the simulation.

Consequently, Fig. 3.6 illustrates the core and outer boundary configuration used in electrostatic simulations, where appropriate boundary conditions are applied. A homogeneous Neumann boundary condition is imposed on the left boundary of the domain. This condition specifies that there is zero normal flux of the electric displacement field across the

left boundary, expressed mathematically as $\boldsymbol{n} \cdot \boldsymbol{D} = 0$, reflecting the symmetry of the problem [17].

On the other hand, homogeneous Dirichlet boundary conditions are applied to the outer boundaries on the top, bottom and right sides of the domain in case of grounding the outer boundary. These conditions set the potential φ_{Out} to zero, effectively grounding the outer boundary and providing a reference point for the potential distribution within the simulation [17]. However, if the core is grounded, the potential throughout the core is fixed at zero, serving as the primary reference point for the simulation. In this case, assigning a floating or grounded condition to the outer boundary would not influence the overall voltage reference in the simulation since the core itself dictates the primary equipotential surface. If neither the core nor the outer boundary is grounded, Neumann boundary conditions are also applied to the whole boundary, to simulate open space or symmetry, implying that the electric field does not cross the boundary but can still vary within the solution domain.

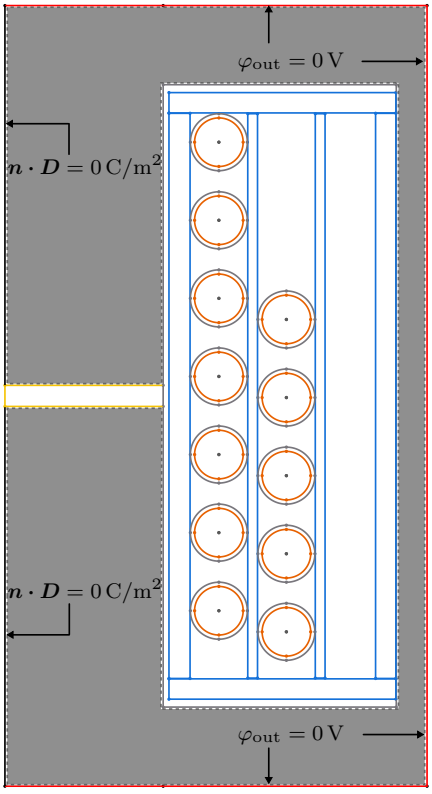


Fig. 3.6: Core and outer boundary representation

3.2.3 Solver

The electrostatic solver in FEMMT is designed to compute the electrostatic potential distribution across the geometry of magnetic components based on user-defined excitations. These excitations can be expressed either by assigning electric potentials or by specifying charges, depending on the simulation setup as illustrated in Fig. 3.7.

Fig. 3.7 provides an overview of the solver architecture in FEMMT. At the core of the simulation framework are two essential components which are function spaces and the formulation. Function spaces define all quantities involved in the simulation, whether they are known, or unknown. These quantities are then used within the formulation, which specifies the system of equations to be solved [17].

The function space in FEMMT introduces three key quantities `Phi`, `U`, and `Q`. The variable `Phi` represents the local electrostatic potential defined throughout the entire domain and is used to evaluate the resulting electric field distribution. The quantity `U` is a global potential applied to selected parts of the geometry, such as windings or the core. When a region is assigned a fixed voltage, `U` ensures that this condition is correctly enforced by overriding any floating behavior. Finally, `Q` denotes the global electric charge applied to a conductor in charge-excitation simulations. In such cases, the solver interprets the region as floating and calculates its potential `U` based on the specified charge constraint.

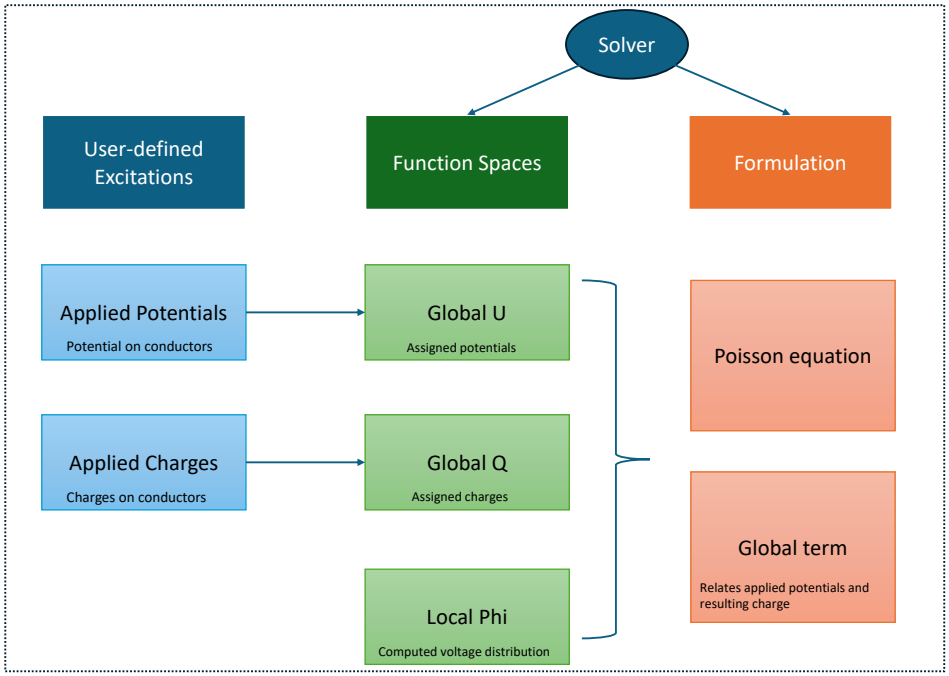


Fig. 3.7: Electrostatic solver workflow in FEMMT

The way these quantities are defined in the solver is shown in Listing 3.3, where each is associated with a specific function space. The variable `Phi` belongs to the local function space for solving differential equations, while `U` and `Q` are global quantities used in the definition of boundary and excitation constraints.

```
    { Name Electrostatic_Potential ; Type FemEquation ;
    Quantity {
       { Name Phi  ; Type Local  ;
            NameOfSpace Hgrad_v_Ele_floating ; }
       { Name U ; Type Global ;
            NameOfSpace Hgrad_v_Ele_floating [GlobalPotential]; }
       { Name Q   ; Type Global;
            NameOfSpace Hgrad_v_Ele_floating [GlobalCharge]; }
     }
    }
```

Listing 3.3: Definition of electrostatic potential and charge in FEMMT

The Poisson equation was previously discussed in Ch. 2, and the solver in FEMMT relies on solving this equation to determine the electrostatic potential distribution within the simulation domain, as shown in 3.4. The global quantities, `phi` and `Q`, are explicitly defined, allowing them to be used in the corresponding "GlobalTerm" in the Formulation. These global terms serve as the equivalent of an "Integral" term, but no numerical integration is required since they directly impose charge-voltage relations on the solver [9].

```
    Equation {
        Integral { [ epsilon[] * Dof{d phi} , {d phi} ];
                In Domain; Jacobian Vol; Integration II; }
        For n In {1:n_windings}
          GlobalTerm { [ -Dof{Q} , {U} ]; In Winding~{n}; }
        EndFor
    }
```

Listing 3.4: Implementation of Poisson's equation in FEMMT

3.2.4 Post-Processing

After the electrostatic simulation is completed, FEMMT performs a post-processing step to extract various physical quantities such that the electrostatic potential, the charges, the electric field, the electric displacement field, and the energy stored in the magnetic component. Based on these quantities, capacitance can be calculated either between individual turns, between windings, or between windings and the core. The capacitance values can be directly obtained from the files generated after each simulation.

4 Capacitance Modeling in Magnetic Components

The determination of capacitances in inductors and transformers is crucial for accurate modeling of their electrical behavior. The discussion begins with the inter-turn capacitances in inductors, exploring how they can be calculated and their significance in electrostatic coupling. A matrix-based formulation is presented to describe the capacitive interaction between turns and the core, and the resulting capacitance values are obtained through electrostatic simulations in FEMMT. The results of the inter-turn capacitance are validated through comparisons with both analytical estimations and simulations performed in commercial tools like ANSYS.

In addition, while the influence of cores on capacitances is often neglected, it is important to recognize conditions where this simplification is insufficient. Particularly, in scenarios with very small winding capacitances, such as single-layer windings, or when the spacing between the winding and the core is minimal, the core's effect on winding capacitance becomes significant [15]. Therefore, this chapter also provides estimations that describe the core's impact on the capacitance model.

Following this, the analysis extends to the equivalent circuit representations of both inductors and transformers, incorporating capacitance effects to achieve a more precise electrical model. To validate the accuracy of our electrostatic simulation implementation, the extracted capacitances from FEMMT are compared with those obtained from ANSYS simulations and experimental measurements.

4.1 Inter-turn Capacitance

The inter-turn capacitance in an inductor can be analyzed by examining the charge distribution on each turn and its interaction with adjacent turns. Fig. 4.1 illustrates the electrostatic coupling between three winding turns in an inductor, where the core is grounded, influencing the capacitance network within the system.

The capacitances between these turns and between each turn and the core are explicitly labeled in Fig. 4.1. The inter-turn capacitances, denoted as C_{ij}, represent the capacitive

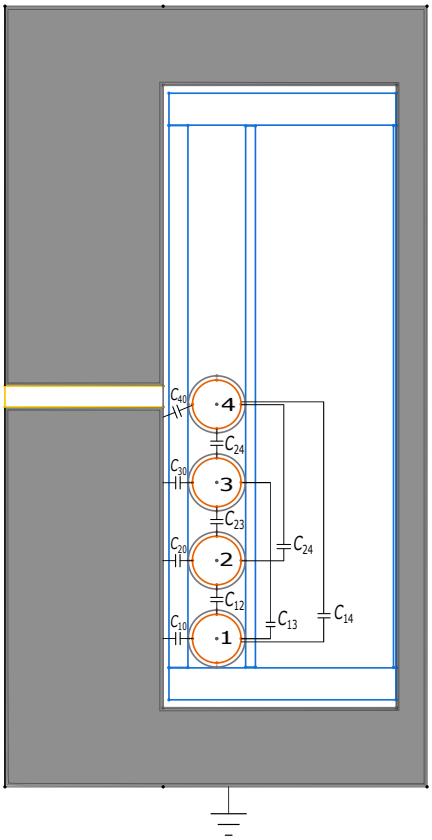


Fig. 4.1: Inter-turn capacitances in an inductor

coupling between different turns (mutual capacitance), while C_{i0} represents the capacitance between each turn and the grounded core. These capacitances can be represented in a matrix, which defines the relationship between the charge Q_i stored on each turn and the corresponding voltage V_i. The general form of this capacitance matrix for n_t turns is given by [6]

$$\begin{bmatrix} Q_1 \\ Q_2 \\ \vdots \\ Q_{n_\mathrm{t}} \end{bmatrix} = \begin{bmatrix} C_{10} + \sum\limits_{j\neq 1} C_{1j} & -C_{12} & \cdots & -C_{1n_\mathrm{t}} \\ -C_{21} & C_{20} + \sum\limits_{j\neq 2} C_{2j} & \cdots & -C_{2n_\mathrm{t}} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{n_\mathrm{t}1} & -C_{n_\mathrm{t}2} & \cdots & C_{n_\mathrm{t}0} + \sum\limits_{j\neq n_\mathrm{t}} C_{n_\mathrm{t}j} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_{n_\mathrm{t}} \end{bmatrix}. \tag{4.1}$$

The diagonal elements C_{ii} in the matrix represent the self-capacitance of each turn, which is the sum of all capacitances connecting that turn to other turns and to the grounded core. This means that each self-capacitance C_{ii} accounts for the total electrostatic influence experienced by that particular turn due to its surroundings. The off-diagonal elements C_{ij} denote the mutual capacitance between two turns. The negative sign indicates that this capacitance corresponds to the charge induced on one turn when the other turn is held

at zero potential. In addition, the capacitance matrix exhibits symmetry, meaning that the mutual capacitance between any two turns satisfies the condition $C_{ij} = C_{ji}$ [6].

However, to extract the inter-turn capacitance for n_t, where n_t is the number of turns, n_t separate simulations in FEMMT are required. In each of the n_t simulations, a voltage of 1 V is applied individually to one turn, while 0 V is applied to the remaining turns and the core is always grounded [6].

For example, in the case of three turns ($n_\mathrm{t} = 3$), the first simulation, where the first turn is excited by 1 V and the others are set to zero, yields the following matrix

$$\begin{bmatrix} Q_1 \end{bmatrix} = \begin{bmatrix} C_{10} + C_{12} + C_{13} \\ -C_{12} \\ -C_{13} \end{bmatrix} \begin{bmatrix} V_1 \end{bmatrix}. \tag{4.2}$$

The simulation determines these capacitances by calculating the charges induced on the turns set to 0 V and on the core, and dividing by the voltage difference between the excited turn and these zero-voltage conductors [7]. Specifically, the capacitances in equation (4.2) are defined as

$$C_{10} = -\frac{Q_\mathrm{core}}{V_1 - V_\mathrm{core}} \tag{4.3a}$$

$$C_{12} = -\frac{Q_2}{V_1 - V_2} \tag{4.3b}$$

$$C_{13} = -\frac{Q_3}{V_1 - V_3} \tag{4.3c}$$

$$C_{11} = \frac{Q_1}{V_1} = |C_{10}| + |C_{12}| + |C_{13}|. \tag{4.3d}$$

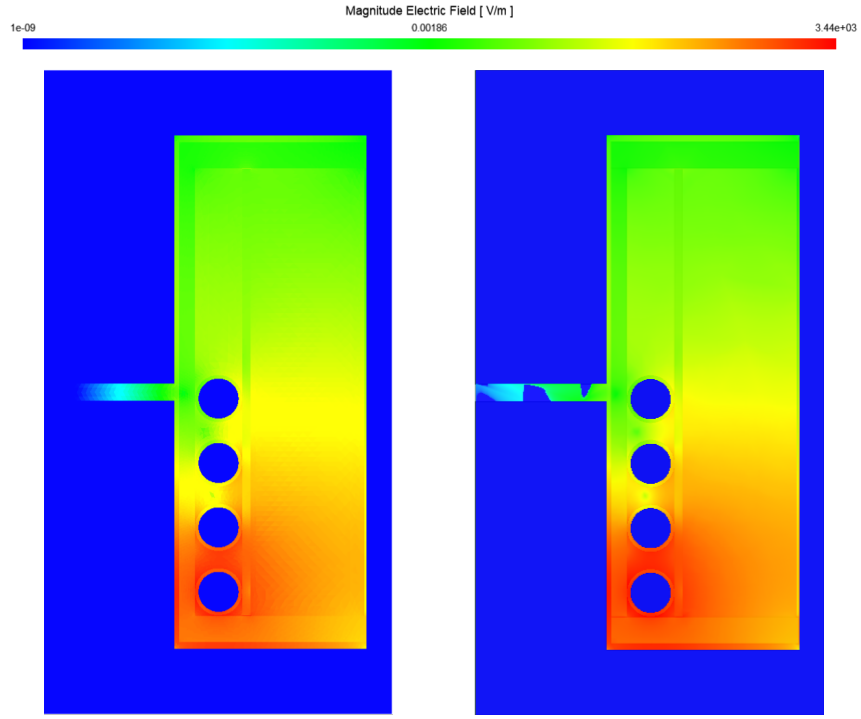
From equation (4.3), it can be observed that the self-capacitance is equal to the sum of the mutual capacitances. This relationship arises from the fundamental principle of charge conservation. Initially, before applying any voltage, the total net charge within the system is zero. Consequently, after applying a voltage of 1 V to the first turn, the charges induced on the other conductors and the grounded core must balance the charge on the excited turn, ensuring the total net charge remains zero. Therefore, (4.3d) can be written as

$$C_{11} = \frac{Q_1}{V_1} = |C_{10}| + |C_{12}| + |C_{13}| = \frac{|Q_\mathrm{core} + Q_2 + Q_3|}{V_1}. \tag{4.4}$$

Furthermore, Fig. 4.2 illustrates the magnitude of the electric field resulting from the first simulation for an inductor with $n_\mathrm{t} = 4$, where only turn 1 is excited at 1 V. Fig. 4.11b presents the electric field distribution obtained from the simulation in ANSYS,

while Fig. 4.11a shows the the electric field distribution from the simulation obtained in FEMMT. The comparison between these two figures provides validation for the accuracy of our FEMMT implementation, demonstrating strong agreement with the established ANSYS simulation.

However, the highest magnitude of the electric field is concentrated around the excited turn and gradually decreases with increasing distance. Additionally, there is no electric field inside the conductors (turns and core). This is because conductors are equipotential bodies, meaning that the electric potential is constant throughout each conductor, leading to zero internal electric field. Consequently, according to Gauss's law, the charge density ρ_v must be zero if $\boldsymbol{E}$ is zero. Hence, This implies that charges cannot reside inside the volume of a conductor; instead, any net charge accumulates only on its surface [7].



(a) Electric field distribution simulated in FEMMT

(b) Electric field distribution simulated in ANSYS

Fig. 4.2: Electric field distribution in the first simulation, where $V_1 = 1\,\mathrm{V}$

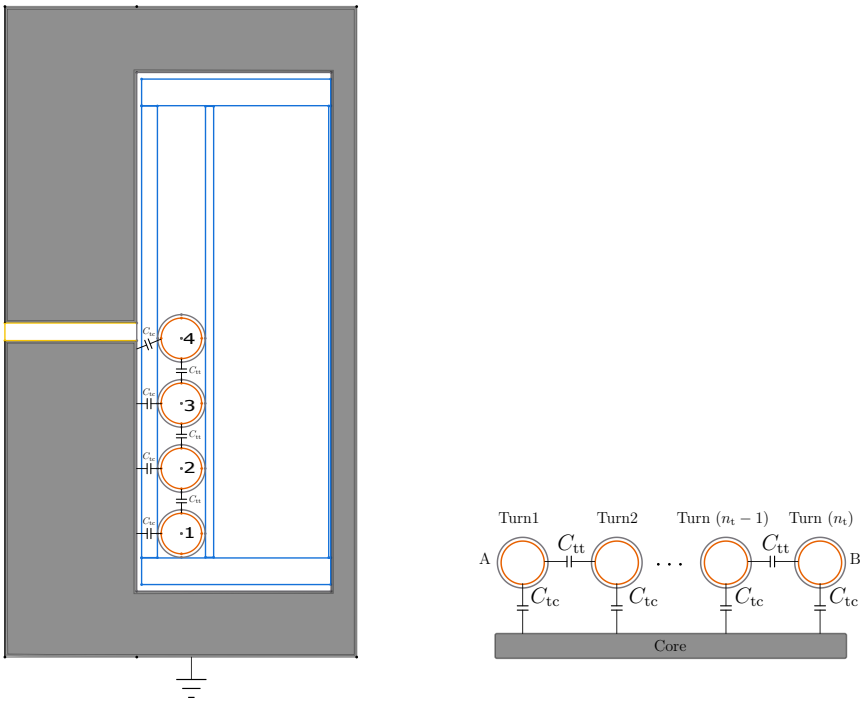
Tab. 4.1 shows the results from all needed simulations for the inductor with 4 turns. It can be observed that the capacitances obtained from FEMMT closely match those computed by ANSYS, with errors generally below 10 %. The highest discrepancies, such as those seen in C_{13} and C_{31}, can be attributed to their significantly smaller magnitudes, where small numerical variations have a proportionally larger impact. Overall, these results validate the accuracy of the FEMMT simulations for capacitance extraction.

Moreover, it can be seen that the capacitance between adjacent turns is approximately the same, i.e, $C_{12} = C_{23} = C_{34}$, and the capacitances between each turn and the edge of the core, such as C_{10} and C_{40} are also nearly equal. Interestingly, the capacitances C_{20} and C_{30} are approximately half the value of C_{10} and C_{40}, respectively. This behavior can be explained by the geometric symmetry of the inductor. The turns located in the middle (e.g., turns 2 and 3) are equally influenced by the surrounding turns and the core. When the structure is symmetric with respect to the inductor's central axis, the turn-to-core electric field is balanced, leading to an effective capacitance that is roughly halved for inner turns compared to edge turns [18].

As shown in Tab. 4.1, the capacitances between non-adjacent turns are significantly smaller than those between adjacent turns. Therefore, these smaller inter-turn capacitances can be neglected to simplify the equivalent capacitance model of the inductor. Consequently, the inter-turn capacitance model illustrated in Fig. 4.1 can be reduced to the simplified model presented in Fig. 4.3. Fig. 4.3a depicts this simplified representation for an inductor with $n_\mathrm{t} = 4$. In this model, the capacitance between adjacent turns is assumed to be equal and denoted as $C_{12} \approx C_{23} \approx C_{34} = C_\mathrm{tt}$, while the capacitance between each turn and the core is represented as $C_{10} \approx C_{20} \approx C_{30} \approx C_{40} = C_\mathrm{tc}$. In addition, the turn-gound capacitance can also be approximated as $C_\mathrm{tc} = 2 \cdot C_\mathrm{tt}$ [19]. Fig. 4.3b shows the equivalent capacitance circuit for an inductor with n_t turns.

Tab. 4.1: Comparison of Capacitances from FEMMT and ANSYS simulations

Capacitance (pF)	FEMMT				ANSYS	Error (%)
	Sim. 1	**Sim. 2**	**Sim. 3**	**Sim. 4**	**Reference**	
C_{11}	7.123	—	—	—	6.910	3.08
C_{12}	-1.558	—	—	—	-1.435	8.56
C_{13}	-0.052	—	—	—	-0.042	23.81
C_{14}	-0.007	—	—	—	-0.006	16.67
C_{10}	-5.506	—	—	—	-5.426	1.47
C_{21}	—	-1.558	—	—	-1.435	8.56
C_{22}	—	6.021	—	—	5.745	4.80
C_{23}	—	-1.575	—	—	-1.453	8.40
C_{24}	—	-0.058	—	—	-0.048	20.83
C_{20}	—	-2.829	—	—	-2.808	0.75
C_{31}	—	—	-0.052	—	-0.042	23.81
C_{32}	—	—	-1.575	—	-1.453	8.40
C_{33}	—	—	6.013	—	5.739	4.77
C_{34}	—	—	-1.605	—	-1.477	8.66
C_{30}	—	—	-2.780	—	-2.766	0.51
C_{41}	—	—	—	-0.007	-0.006	16.67
C_{42}	—	—	—	-0.058	-0.048	20.83
C_{43}	—	—	—	-1.605	-1.477	8.66
C_{44}	—	—	—	5.216	5.027	3.76
C_{40}	—	—	—	-3.545	-3.495	1.43



(a) Simplified model of inter-turn capacitance for $n_t = 4$

(b) Generalized inter-turn capacitance model with n_t turns

Fig. 4.3: Simplified model of inter-turn capacitance in an inductor

4.2 Winding capacitance

The total stray capacitance $C_{AB}(n_t)$ of a single-layer inductor with n_t turns can be approximated using the inter-turn capacitance. The core can be treated as a single common node to which all turn-to-core capacitances C_{tc} are connected. This step makes it easier to simplify the circuit by using its symmetry [19] [20]. Consider an even number of turns, such as two turns located at the center of the coil as shown in Fig. 4.4a. In this case, the turn-to-core capacitances C_{tc} are connected in series with each other and in parallel to the inter-turn capacitance C_{tt} between the two turns. Thus, the total stray capacitance for two turns $C_{AB}(2)$ can be written as [19]

$$C_{AB}(2) = \frac{C_{tc} \cdot C_{tc}}{C_{tc} + C_{tc}} + C_{tt} = \frac{2C_{tt} \cdot 2C_{tt}}{4C_{tt}} + C_{tt} = 2C_{tt}. \tag{4.5}$$

Similarly, consider an odd number of turns, such as two turns located at the center of the coil as shown in Fig. 4.4b. It is shown that the capacitance C_{tc} in the middle can be split into two halves and applying Δ/Y transformation. Thus, the total stray capacitance for three turns $C_{AB}(3)$ can be written as [19]

$$C_{AB}(3) = \frac{C_{tt}}{2} + \frac{C_{tc}}{2} = \frac{C_{tt}}{2} + \frac{2C_{tt}}{2} = \frac{3}{2}C_{tt}. \tag{4.6}$$

To calculate the total stray capacitance for $n_t = 4$ or $n_t = 5$, an additional turn is added to each side of the previous configuration. The resulting total capacitance is then given by the series connection of the previous network with two additional turn-to-turn capacitances, combined in parallel with the series combination of two additional turn-to-core capacitances. Thus, the total stray capacitance for $n_t = 4$ is [19]

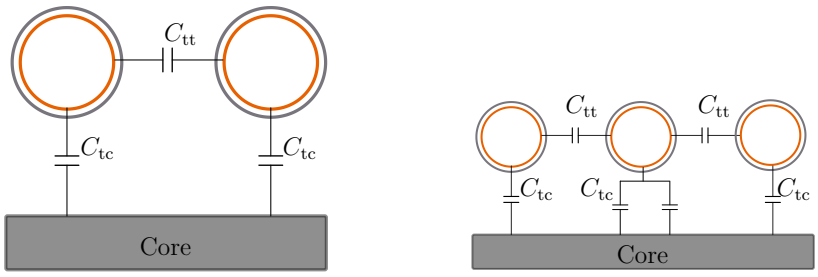
$$C_{AB}(4) = \frac{C_{tt}C_{AB}(2)}{2C_{AB}(2) + C_{tt}} + C_{tt} = \frac{C_{tt} \cdot 2C_{tt}}{2 \cdot 2C_{tt} + C_{tt}} + C_{tt} = \frac{7}{5}C_{tt}. \tag{4.7}$$

Similarly, the total stray capacitance for $n_t = 5$ can be calculated as [19]:

$$C_{AB}(5) = \frac{C_{tt}C_{AB}(3)}{2C_{AB}(3) + C_{tt}} + C_{tt} = \frac{C_{tt} \cdot \frac{3}{2}}{\frac{3}{2} \cdot 2C_{tt} + C_{tt}} + C_{tt} = \frac{11}{8}C_{tt}. \tag{4.8}$$

However, the inter-turn capacitance C_{tt} for $n_t = 4$, depicted from Tab. 4.1 in section 4.1 is approximately 1.759 pF. Thus, the total stray capacitance $C_{AB}(4)$ is calculated as

$$C_{AB}(4) = \frac{7}{5}C_{tt} = \frac{7}{5} \cdot 1.759 \approx 2.211\,\text{pF}. \tag{4.9}$$



(a) Two turns in the middle of a coil

(b) Three turns in the middle of a coil

Fig. 4.4: Representation of two different cases of inter-turn capacitance

Overall, the total stray capacitance C_{AB} can be calculated in general as [19]

$$C_{AB}(n_t) = \frac{C_{tt}}{2 + \dfrac{C_{tt}}{C_{AB}(n-2)}} + C_{tt}. \tag{4.10}$$

Equation (4.10) describes the relationship used to calculate the total stray capacitance $C_{AB}(n_t)$ of a single-layer inductor with n_t turns. As the number of turns increases, the computed values of $C_{AB}(n_t)$ form a sequence that converges rapidly. It can be observed

that this sequence stabilizes around a limiting value, and for sufficiently large n_t, the total stray capacitance converges to approximately $C_{AB}(n_t) \approx 1.366 \cdot C_{tt}$. However, for a two-layer coil, the total stray capacitance converges to $C_{AB}(n_t) \approx 1.83 \cdot C_{tt}$, indicating that the stray capacitance is higher compared to that of a single-layer inductor [19].

Furthermore, the total stray capacitance can be directly obtained from simulation. Assuming a linear voltage distribution along the inductor [15], from 1V at the first turn to 0V at the last turn, and with the core kept floating as shown in Fig. 4.5, the total stray capacitance can be calculated accordingly from the stored energy in the inductor as

$$C_{AB}(4) = \frac{2 \cdot W_e}{V^2} = 2.839\,\text{pF} \tag{4.11}$$

where W_e is the total energy stored in the component and V is the voltage between the first and last turns. It can be seen that the value of $C_{AB}(4)$ calculated from the asymptotic expression in (4.9) closely matches the result obtained from the simulation in (4.11).

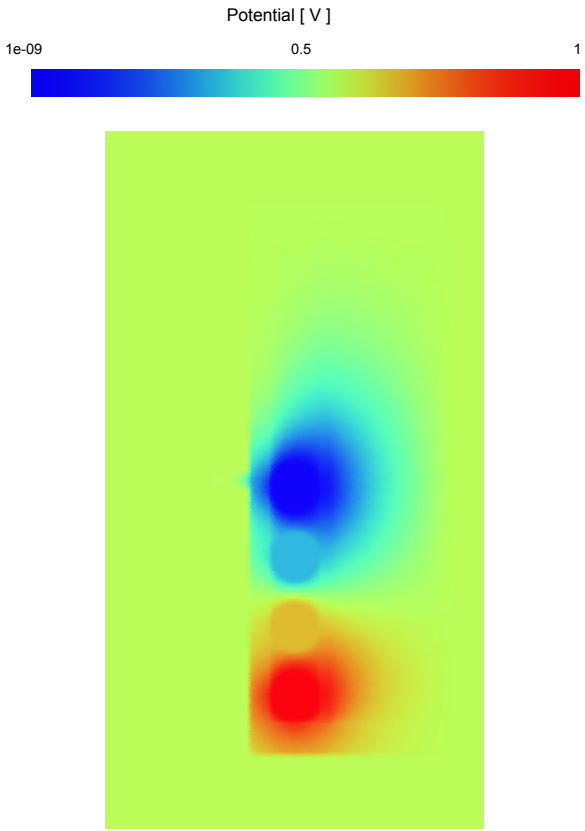


Fig. 4.5: Linear voltage drop across turns in an inductor

However, the assumption that the stray capacitance $C_{\mathrm{AB}}(n_{\mathrm{t}})$ depends only on the inter-turn capacitance C_{tt} between adjacent turns holds primarily when the number of turns is small and the turns are well spaced. As the number of turns increases and the spacing between them decreases, the electrostatic interactions between non-adjacent turns become stronger, complicating the approximation of the capacitance calculations [21]. To illustrate the limitations of this approximation for inductors with a large number of turns and closely spaced windings, consider an inductor with $n_{\mathrm{t}} = 84$ turns as shown in Fig. 4.6. The horizontal distance between adjacent turns is $d_{\mathrm{h}} = 0.133\,37\,\mathrm{mm}$, and the turn-to-turn spacing is $d_{\mathrm{t}} = 0.12\,\mathrm{mm}$, resulting in strong electrostatic interactions that go beyond adjacent-turn coupling. Using the asymptotic estimation for two layers, the total stray capacitance is approximated as

$$C_{\mathrm{AB}}(84) \approx 1.366 \cdot C_{\mathrm{tt}} \approx 1.366 \cdot 1.74\,\mathrm{pF} = 3.18\,\mathrm{pF}. \tag{4.12}$$

However, an electrostatic simulation with a linear voltage distribution from 1 V at the first turn to 0 V at the last turn, and with the core kept floating, yields a total energy stored in the structure corresponding to a capacitance of

$$C_{\mathrm{AB}}(84) = \frac{2 \cdot W_{\mathrm{e}}}{V^2} = 36.7\,\mathrm{pF}. \tag{4.13}$$

It can be seen that the value of $C_{\mathrm{AB}}(84)$ calculated in (4.12) does not match the result obtained from the simulation in (4.13). This discrepancy arises because the interactions between non-adjacent turns become increasingly significant in compact, high-turn inductors, contributing to the total capacitance in a way that the simplified model does not capture.

Therefore, a capacitive equivalent circuit is necessary to accurately represent inductors and transformers within mathematical models. This modeling approach enables better prediction of inductor and transformer behaviors. The capacitive equivalent circuit consists of mathematical parameters that characterize the electrostatic energy distribution in inductors and transformers. Indeed, achieving an accurate representation of electrostatic energy sometimes requires these capacitive parameters to be positive or even negative. The discussion begins by exploring the equivalent capacitance representation of inductors with conductive cores, detailing the calculations necessary to determine these capacitances through simulation, and validating them against measurements. Following this, the focus shifts to transformers, where the capacitive equivalent circuit becomes more complex due to the presence of a second winding.

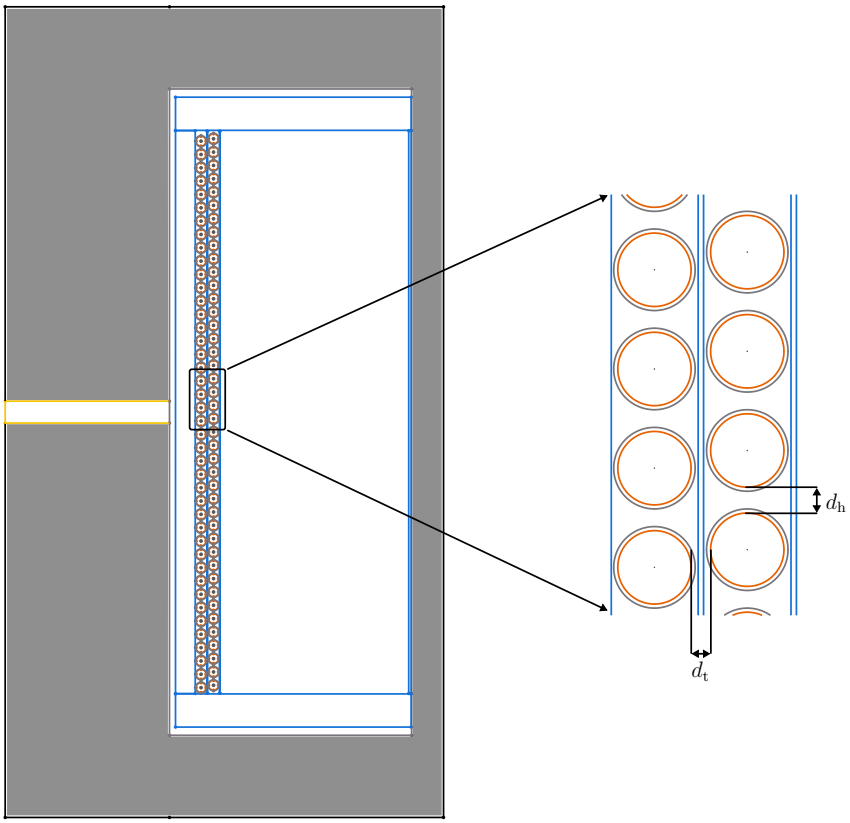


Fig. 4.6: Geometric representation of an inductor with $n_\mathrm{t} = 84$ turns

4.3 Capacitive Equivalent Circuit of an Inductor with a Conductive Core

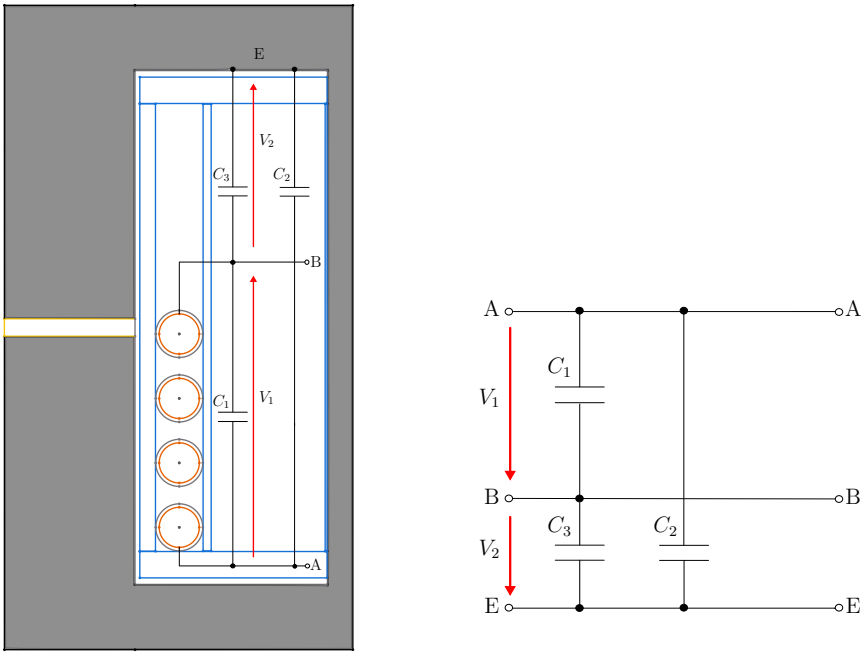
The capacitive equivalent circuit of an inductor with a conductive core is shown in Fig. 4.7. Terminal A corresponds to the first turn of the inductor, while terminal B corresponds to the last turn. Terminal E represents the conductive core. As a result, three capacitances exist between three terminals as shown in Fig. 4.7a. Consequently, C_1 denotes the capacitance between terminals A and B, C_2 represents the capacitance between terminal A and the core, and C_3 is the capacitance between terminal B and the core. For simplicity, the inductor symbol itself has been omitted from the capacitive equivalent circuit diagram shown in Fig. 4.7b.

To determine the electric energy stored within the geometry and, consequently, calculate the capacitances between the three terminals A, B, and C, the potential distribution must be known. Therefore, it is assumed that all turns experience essentially the same flux, resulting in a linear potential distribution along the winding. However, in practice, due to varying magnetic coupling between individual turns and displacement currents caused

by capacitive effects, particularly at higher frequencies, the voltage distribution along the winding is not strictly linear [15].

The capacitance C_1 is determined from the voltage drop V_1 shown in Fig. 4.7b between terminal A and B. Similarly, the capacitances C_2 and C_3 are determined from the voltage drops between A and B, respectively, and the core. The voltage across C_2 is the total voltage between terminal A and the core, which corresponds to the sum $V_1 + V_2$, while C_3 experiences the voltage drop V_2. Therefore, the total electrostatic energy W_e stored in the inductor component is given by

$$W_\mathrm{e} = \frac{C_1 V_1^2}{2} + \frac{C_2 (V_1 + V_2)^2}{2} + \frac{C_3 V_2^2}{2}. \tag{4.14}$$



(a) Simplified view of inductor with conductive core illustrating capacitances

(b) Simplified capacitive equivalent circuit diagram of inductor

Fig. 4.7: Capacitive equivalent circuit representation of inductor with conductive core

However, in simulation environments, it is not feasible to directly assign a voltage drop. Instead, potentials must be assigned individually to each terminal. As there are three capacitances, three separate simulations are required, each assigning distinct potentials to the terminals, to determine the stored electrostatic energy. The resulting energies from these simulations are then used to solve a system of equations, enabling the accurate

determination of each capacitance. The potentials can be chosen arbitrarily; but it is important to note that the potentials assigned in the simulations should be linearly independent. This ensures that the system of equations formed from the energy expressions has a unique solution.

Hence, assuming the potential assigned to the first turn (terminal A) is denoted by V_{A}, the potential at the last turn (terminal B) by V_{B}, and the potential at the core (terminal E) by V_{E}, the voltage drops between the terminals are defined as follows

$$V_1 = V_{\mathrm{A}} - V_{\mathrm{B}}, \quad V_2 = V_{\mathrm{B}} - V_{\mathrm{E}}. \tag{4.15}$$

As the potential assigned to each terminal in every simulation defines the corresponding voltage drop, the voltage drop across each capacitor in simulation i can be represented using the symbol $V_{1,i}$, $V_{2,i}$, and $V_{3,i}$, where the subscript i indicates the simulation number. Similarly, the stored electrostatic energy obtained from each simulation can be denoted as $W_{e,i}$. Therefore, to calculate the three unknown capacitances, three independent simulations are required. The results from these simulations can be expressed in matrix form as follows

$$\begin{bmatrix} W_{e,1} \\ W_{e,2} \\ W_{e,3} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} V_{1,1}^2 & (V_{2,1} + V_{3,1})^2 & V_{2,1}^2 \\ V_{1,2}^2 & (V_{2,2} + V_{3,2})^2 & V_{2,2}^2 \\ V_{1,3}^2 & (V_{2,3} + V_{3,3})^2 & V_{2,3}^2 \end{bmatrix} \begin{bmatrix} C_1 \\ C_2 \\ C_3 \end{bmatrix}. \tag{4.16}$$

To simplify the matrix formulation and make it more user-friendly in FEMMT, the potential at each terminal is defined using binary values—either 0 or 1. This approach leads to a well-defined and structured matrix. In the first simulation, the potentials assigned to the terminals are $(V_{\mathrm{A}}, V_{\mathrm{B}}, V_{\mathrm{E}}) = (1\,\mathrm{V}, 0\,\mathrm{V}, 0\,\mathrm{V})$. As a result, the voltage drops between the terminals are

$$V_1 = V_{\mathrm{A}} - V_{\mathrm{B}} = 1\,\mathrm{V}, \quad V_2 = V_{\mathrm{B}} - V_{\mathrm{E}} = 0\,\mathrm{V}.$$

In this simulation setup, since the potential at terminal A is set to 1 and terminals B and E are set to 0, a voltage drop of $V_1 = 1$ occurs across capacitor C_1, while $V_2 = 0$ implies that there is no voltage drop across capacitor C_3. As a result, the equivalent circuit shown in Fig. 4.7b can be simplified as in Fig. 4.10.

In the second simulation, the potentials assigned to the terminals are $(V_{\mathrm{A}}, V_{\mathrm{B}}, V_{\mathrm{E}}) = (1\,\mathrm{V}, 1\,\mathrm{V}, 0\,\mathrm{V})$. As a result, the voltage drops between the terminals are

$$V_1 = V_{\mathrm{A}} - V_{\mathrm{B}} = 0\,\mathrm{V}, \quad V_2 = V_{\mathrm{B}} - V_{\mathrm{E}} = 1\,\mathrm{V}$$

In this configuration, both terminals A and B are set to 1 V, and terminal E is set to 0 V. This results in a voltage drop of $V_1 = 0\,\mathrm{V}$ across capacitor C_1, indicating no energy storage in that component. However, since $V_2 = 1\,\mathrm{V}$, capacitors C_2 and C_3 now both experience the full potential difference and thus contribute to the stored energy. Therefore, the

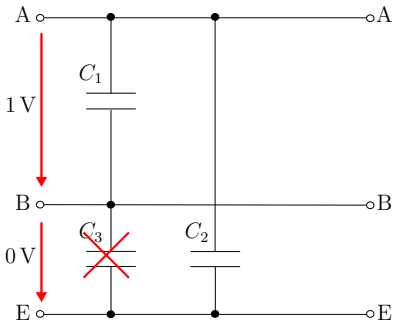


Fig. 4.8: Capacitive equivalent circuit of the inductor obtained from simulation 1

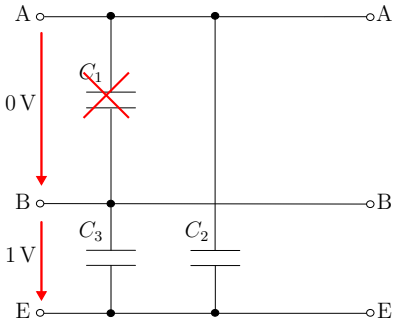


Fig. 4.9: Capacitive equivalent circuit of the inductor obtained from simulation 2

equivalent circuit simplifies by excluding C_1, and only C_2 and C_3 remain active in the model as shown in Fig. 4.9.

In the third simulation, the potentials assigned to the terminals are $(V_\mathrm{A}, V_\mathrm{B}, V_\mathrm{E}) = (1\,\mathrm{V}, 0\,\mathrm{V}, 1\,\mathrm{V})$. As a result, the voltage drops between the terminals are

$$V_1 = V_\mathrm{A} - V_\mathrm{B} = 1\,\mathrm{V}, \quad V_2 = V_\mathrm{B} - V_\mathrm{E} = -1\,\mathrm{V}$$

In this configuration, the voltage drop $V_1 = 1\,\mathrm{V}$ causes capacitor C_1 to store energy, and $V_2 = -1\,\mathrm{V}$ results in energy storage in capacitor C_3. However, the voltage drop across capacitor C_2, given by $V_1 + V_2 = 1 - 1 = 0\,\mathrm{V}$, is zero. Therefore, only C_1 and C_3 are active in the equivalent circuit, and C_2 can be excluded.

After defining the three simulations, the matrix shown in equation (4.16) can take specific values based on the previous assigned potentials and resulting voltage drops. This yields the following system:

$$\begin{bmatrix} W_{e,1} \\ W_{e,2} \\ W_{e,3} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} C_1 \\ C_2 \\ C_3 \end{bmatrix}. \tag{4.17}$$

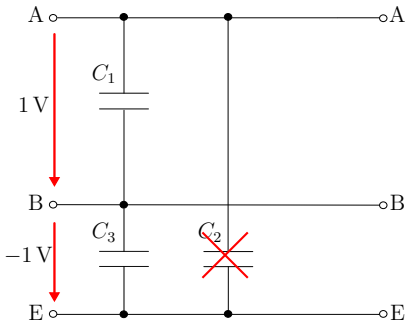


Fig. 4.10: Capacitive equivalent circuit of the inductor obtained from simulation 3

With the form of the matrix established, the system is now ready for validation. To verify the accuracy of the simulation results, an inductor was physically constructed and measured. The test inductor consists of 42 turns of copper wire with a diameter of 0.50 mm, wound in a single layer. It is built around a PQ40/40 ferrite core and measured using a `Wayne Kerr 6515B` impedance analyzer to extract the capacitance results. The results from these experimental measurements are then compared with those obtained from the electrostatic simulation to evaluate the reliability of the proposed method.

To extract the values of the unknown capacitances C_1, C_2, and C_3 in the simulation using FEMMT, the three defined simulations are executed sequentially. The resulting matrix system, shown in equation (4.17), is solved by substituting the computed electrostatic energy values from each simulation. The system of equations becomes

$$\begin{bmatrix} 5.2395 \times 10^{-12} \\ 1.4200 \times 10^{-11} \\ 5.0554 \times 10^{-12} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} C_1 \\ C_2 \\ C_3 \end{bmatrix}. \tag{4.18}$$

To further validate the accuracy of the electrostatic simulation performed using FEMMT, the same inductor geometry and simulation conditions were replicated in ANSYS. This comparison allows to assess the reliability and precision of FEMMT in computing electrostatic energy. Tab. 4.2 below presents the electrostatic energy values obtained from both FEMMT and ANSYS for the three simulation scenarios. The relative error between the electrostatic energy obtained from FEMMT and ANSYS is calculated using the following expression

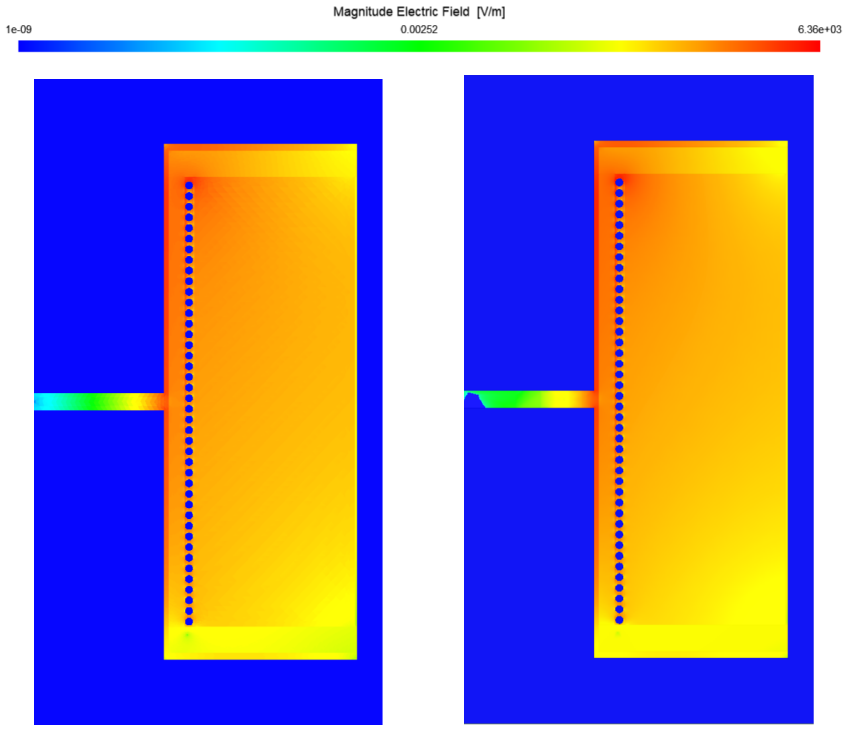
$$\text{Error } (\%) = \left(\frac{W_{e,i}^{\text{ANSYS}} - W_{e,i}^{\text{FEMMT}}}{W_{e,i}^{\text{ANSYS}}} \right) \times 100. \tag{4.19}$$

In addition, Fig. 4.11 shows the electric field distribution resulting from the third simulation, visualized in both FEMMT and ANSYS. In this simulation scenario, the potential configuration was set to $V_{\text{A}} = 1\,\text{V}$, $V_{\text{B}} = 0\,\text{V}$, and $V_{\text{E}} = 1\,\text{V}$. The visualization highlights the spatial distribution and magnitude of the electric field in the inductor geometry. Overall, a qualitative comparison between the two tools shows a strong similarity in the field

Tab. 4.2: Comparison of electrostatic energy results between FEMMT and ANSYS

$W_{e,i}$ **(J)**	**FEMMT**	**ANSYS**	**Error (%)**
$W_{e,1}$	5.2395×10^{-12}	5.2326×10^{-12}	0.132
$W_{e,2}$	1.4200×10^{-11}	1.4152×10^{-11}	0.340
$W_{e,3}$	5.0554×10^{-12}	5.0451×10^{-12}	0.203

patterns, which further supports the accuracy of the electrostatic model implemented in FEMMT.



(a) Electric field distribution simulated in FEMMT

(b) Electric field distribution simulated in ANSYS

Fig. 4.11: Electric field distribution in the third simulation

By solving the matrix system in equation (4.18), the values of the three capacitances C_1, C_2, and C_3 can be determined. The matrix was solved numerically using the electrostatic energy results obtained from the three simulations. The computed capacitance values are listed in Tab. 4.3. As previously discussed, the appearance of a negative capacitance value (in this case, C_1) can result from the mathematical nature of the energy decomposition and the assumptions made in the equivalent circuit representation.

Tab. 4.3: Capacitance values of the 42-turn inductor

Capacitance (pF)	
C_1	-3.905
C_2	14.384
C_3	14.016

To experimentally validate the proposed capacitive equivalent circuit model, physical measurements were performed by configuring the terminals of the inductor in three specific ways: terminal A versus the combined terminals B and E (A vs BE), terminal B versus terminals A and E (B vs AE), and terminals A and B versus the core terminal E (AB vs E). These configurations are designed to correspond to the terminal relationships represented by the equivalent capacitances C_1, C_2, and C_3 in the mathematical model.

It is important to note that the capacitances C_1, C_2, and C_3 themselves are not directly measurable physical quantities. They are mathematical parameters derived from energy relationships within the system and are valid only within the context of the assumed model. For this reason, physical measurements do not attempt to isolate and directly measure these capacitances. Instead, the physical capacitances measured between the above-mentioned terminal groupings are used to calculate the model-based parameters, and ultimately to validate the consistency of the mathematical representation against experimental results.

Fig. 4.12 presents the impedance magnitude and phase angle versus frequency for the three measured terminal configurations of the 42-turn inductor: A vs BE, B vs AE, and AB vs E.

The results clearly show that the A vs BE and B vs AE configurations exhibit an inductive behavior over the frequency range of interest. For these two inductive configurations, the inductance L is first determined from the impedance slope in the lower frequency range as

$$L = \frac{\mathrm{Im}(Z)}{2\pi f} = \frac{Z \cdot \sin\theta_z}{2\pi f} \tag{4.20}$$

where f is the frequency at which the impedance Z and its phase angle θ_z are evaluated. Then, the capacitance C is extracted based on the observed resonance frequency, where the impedance peaks and the phase angle rapidly shifts toward 0°. The resonance frequency f_{res} is used in the relation

$$C = \frac{1}{(2\pi f_{\mathrm{res}})^2 L} \tag{4.21}$$

On the other hand, the AB vs E configuration exhibits a capacitive behavior across the entire frequency range. Thus, capacitance C can be calculated directly as

$$C = -\frac{1}{2\pi f\,\mathrm{Im}(Z)} = -\frac{1}{2\pi f Z \cdot \sin\theta_z} \tag{4.22}$$

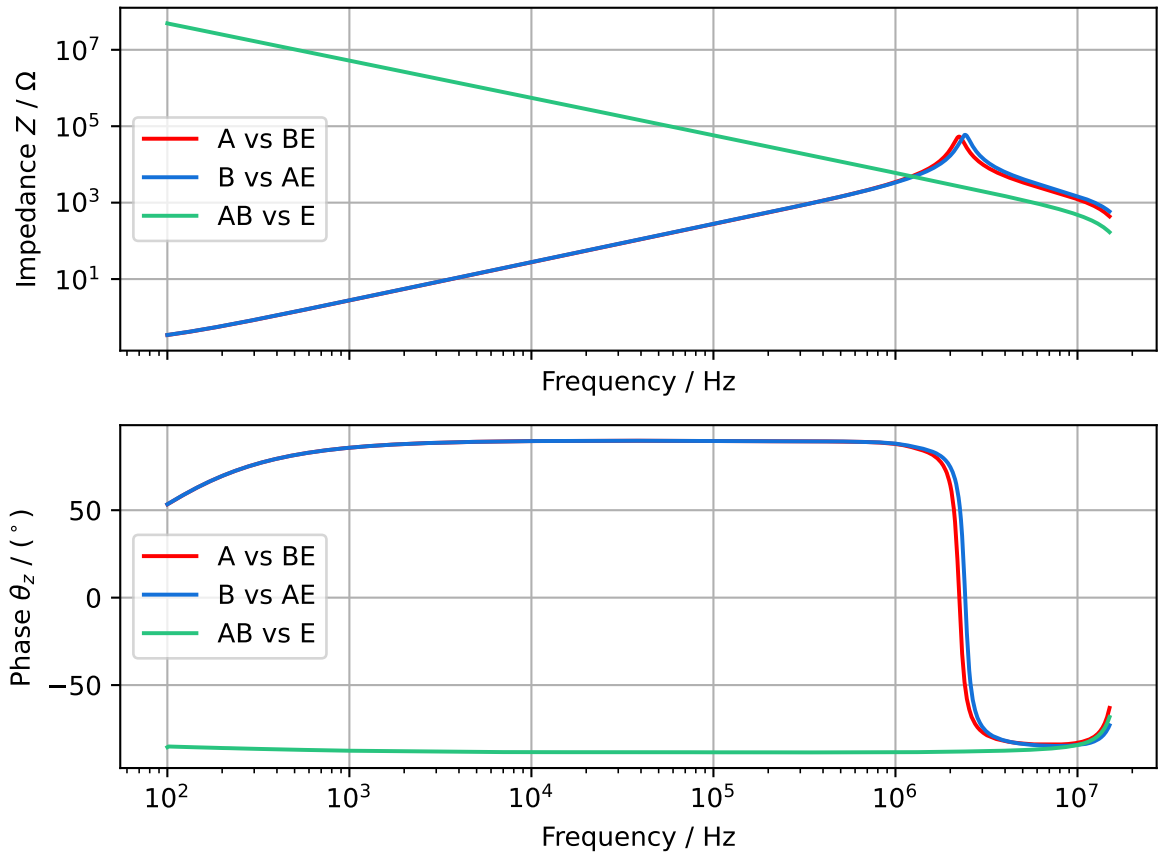


Fig. 4.12: Measured impedance and phase angle versus frequency for three terminal configurations of the 42-turn inductor: A vs BE, B vs A, and AB vs E

Tab. 4.4 compares the measured capacitances with the values obtained from FEMMT simulations. The absolute error ranges approximately from 0.4% to 11% due to geometry tolerances and modeling assumptions.

However, the stray capacitance $C_{\mathrm{AB}}(42)$ can be determined in two ways. First, it can be estimated using the assumption of a linear voltage distribution across the winding with floating the core, as discussed in Section 4.2. Alternatively, it can be calculated directly from the three extracted capacitances using the following relation

$$C_{\mathrm{AB}}(42) = C_1 + \frac{C_2 C_3}{C_2 + C_3} \tag{4.23}$$

This expression results from the series-parallel combination of the capacitances in the mathematical model between terminals A, B, and the core (E). However, if the core is left floating and the the inductor is geometrically symmetric, then the potential on the core will be approximately half of V_1 [22]. Thus, the stray capacitance $C_{\mathrm{AB}}(42)$ can also be calculated as shown in Tab. 4.4.

Tab. 4.4: FEMMT validation with measurements on the 42-turn inductor

Connection	**Measurement**	V_1	V_2	**Behaviour of EC**	**FEMMT**
A vs BE	11.72 pF	1 V	0 V	$C_1 + C_2$	10.47 pF
B vs AE	10.04 pF	−1 V	1 V	$C_1 + C_3$	10.09 pF
AB vs E	27.46 pF	0 V	1 V	$C_2 + C_3$	28.40 pF
A vs B (core floating)	2.80 pF	1 V	−0.5 V	$C_1 + \frac{1}{4}C_2 + \frac{1}{4}C_3$	3.18 pF

$$C_{\mathrm{AB}}(42) = C_1 + \frac{1}{4}C_2 + \frac{1}{4}C_3. \tag{4.24}$$

In addition, Fig. 4.13 illustrates the comparison between simulated and experimentally measured capacitance values for four terminal configurations of the 42-turn inductor. Each configuration's error ratio, defined as the ratio of simulated to measured capacitance, is annotated above the respective simulated value. The close agreement between simulation and measurement, with most error ratios near unity, demonstrates the reliability of the implemented mathematical modeling approach for inductor geometries.

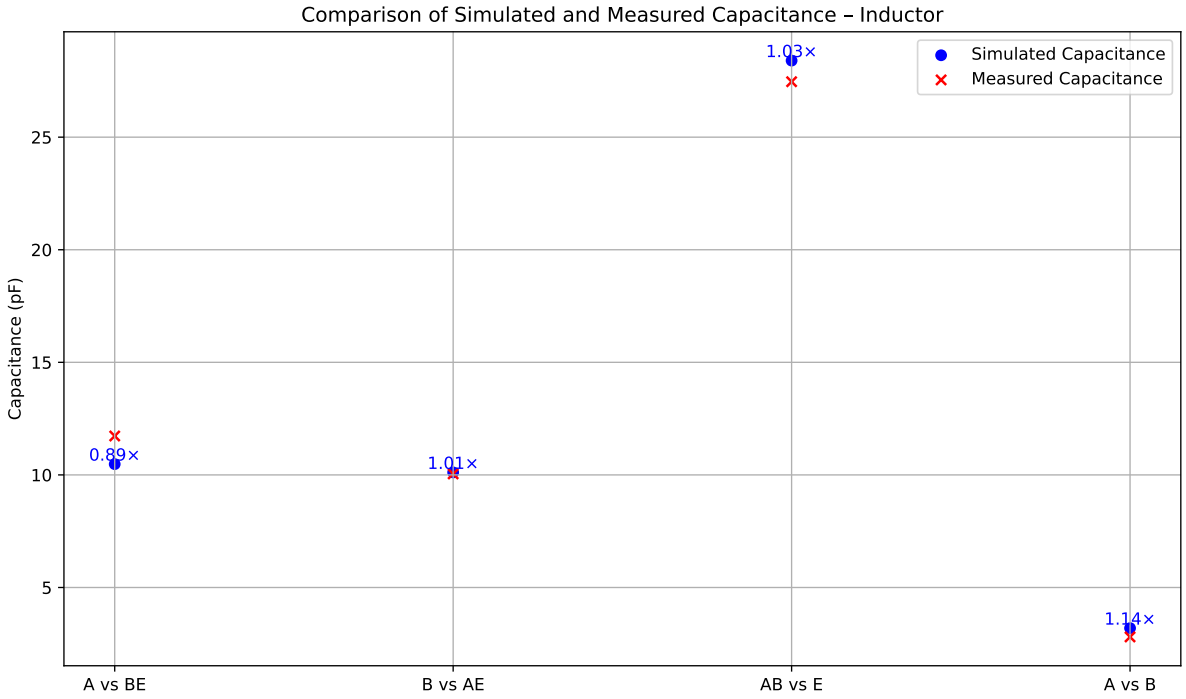


Fig. 4.13: Comparison between simulated and measured capacitance for various terminal configurations of the 42 inductor

Furthermore, since the capacitive equivalent circuit of the inductor includes only three unknown capacitances, it is feasible to determine their values by solving a system of linear equations derived from the measured capacitances of specific terminal configurations [23] [24]. In contrast, for more complex components such as transformers, which involve a larger number of capacitances, this approach becomes impractical, meaning that even small measurement errors can lead to large deviations in the computed capacitance values [22]. For that reason, the validation is kept on the connections described in Tab. 4.4.

However, in the case of a single-layer winding, the influence of the core cannot be neglected, as a significant portion of the electrostatic energy is stored between the winding and the core. This is clearly demonstrated in Fig. 4.14, which shows the energy distribution in the same measured inductor with $n_\mathrm{t} = 42$ turns arranged in a single layer. The highest concentrations of stored energy are observed in the regions between the first and last turns and the core. However, when the winding capacitance is small, as in single-layer winding, or when the windings are positioned very close to the core, the core must be included in the electrostatic model to ensure accurate prediction of parasitic capacitance [15].

In contrast, Fig. 4.15 shows the electrostatic energy distribution for an 84-turn inductor wound in two layers. In this case, inter-layer coupling dominates the energy distribution, and the core influence becomes negligible. The conductors are more tightly packed, and the electric field tends to stay confined between the layers themselves. Consequently, many analytical models approximate the total winding capacitance using only the inter-layer contribution [15] [16] [25]. This is further supported by the capacitance values in Tab. 4.5, where the stray capacitance $C_\mathrm{AB}(84)$ closely matches the dominant inter-layer capacitance C_1.

Tab. 4.5: Capacitance values of the 84-turn inductor

Capacitance (pF)	
C_1	30.28
C_2	20.03
C_3	9.57
$C_\mathrm{AB}(84)$	36.67

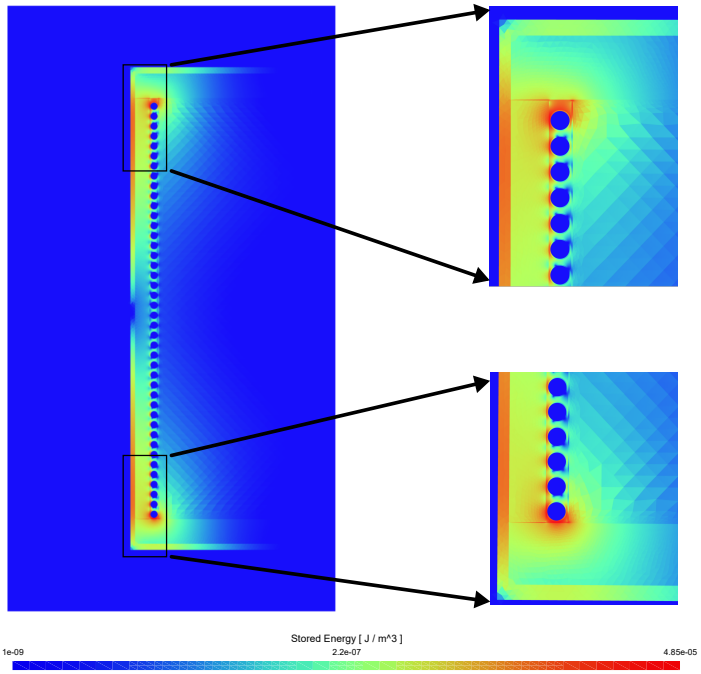


Fig. 4.14: Stored energy is concentrated between the winding and the core for single-

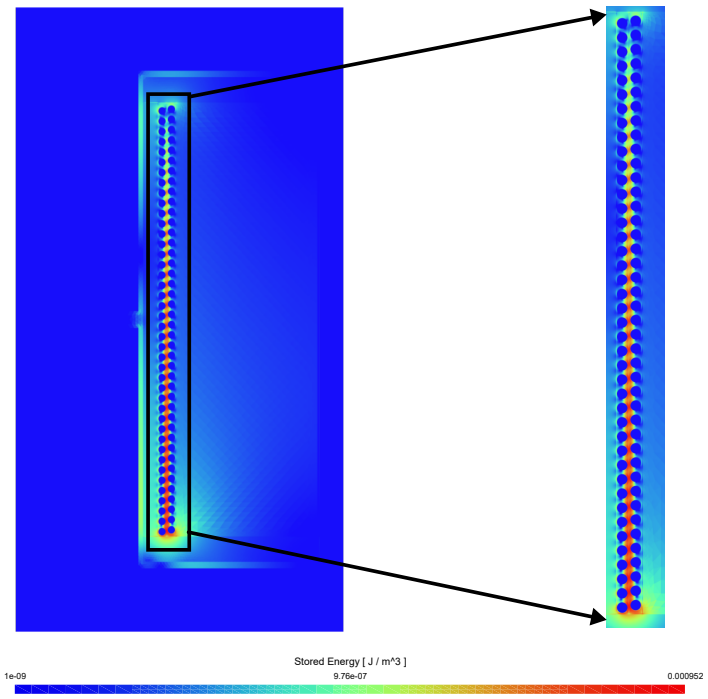
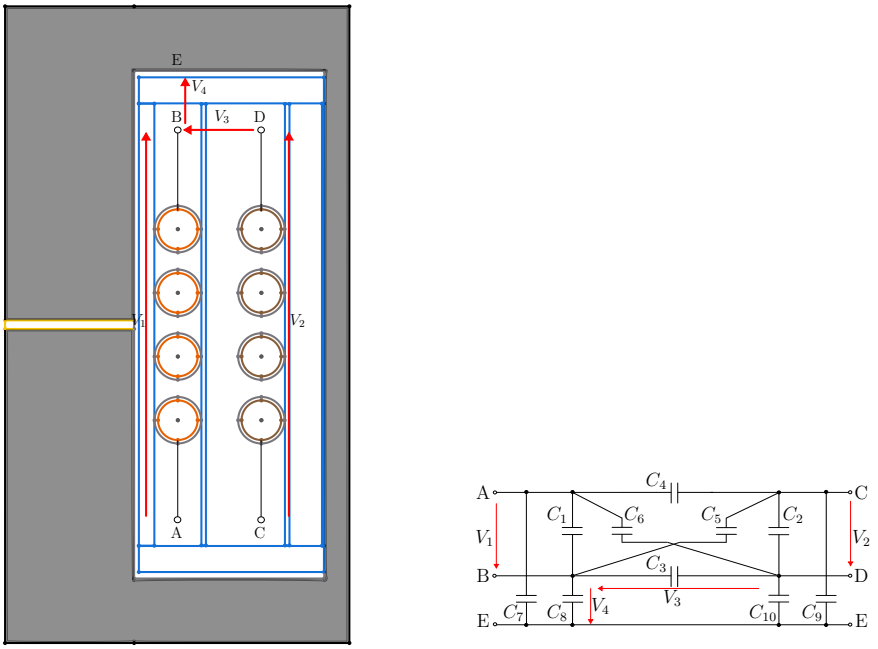


Fig. 4.15: Stored energy is concentrated between the inter-layer of turns for two-layers

4.4 Capacitive Equivalent Circuit of a Transformer

The capacitive equivalent circuit of a transformer follows the same fundamental concept as that used in the inductor analysis presented earlier in section 4.3, but extended to account for two windings. However, the addition of just one extra winding significantly increases the complexity of the equivalent circuit. This is due to the need to model the capacitances between five terminals. As a result, the number of capacitances required to accurately describe the electrostatic behavior increases substantially. The transformer configuration with two windings is illustrated in Fig. 4.16, where terminal A corresponds to the input of the first winding, and terminal B is its output. In general, terminal C corresponds to the input of the second winding, and terminal D is its output. Terminal E represents the potential of the core. This configuration introduces five distinct electrical potentials: V_A, V_B, V_C, V_D, and V_E. In a general case, all five terminals are considered to have independent potentials [22].



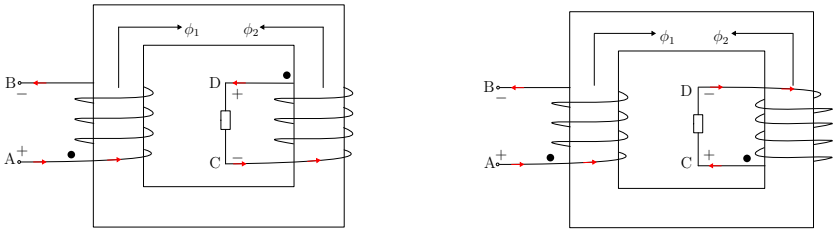
(a) Terminals configuration of a transformer in FEMMT

(b) Simplified capacitive equivalent circuit diagram of transformer

Fig. 4.16: Capacitive equivalent circuit representation of transformer

However, the determination of the voltage polarity across transformer windings is directly influenced by the winding sense, as illustrated in Fig. 4.17. If terminal A is defined as the positive terminal, where the current enters the primary winding, then a terminal is assigned as the positive terminal on the secondary side, where the current exits the winding. Hence, according to Lenz's law, the direction of the induced current in the

secondary winding is such that the magnetic field generated by this current opposes the change in the magnetic flux that caused it [7]. In Fig. 4.17a, the induced voltage in the secondary will be opposite to the induced voltage in the primary, which changes the definition of terminal C and D in the equivalent circuit shown in Fig. 4.16b. Conversely, in Fig. 4.17b, the induced voltage in the primary and the secondary has the same polarity, which align to the definition of the terminal C and D in the equivalent circuit. Therefore, the correct assignment of terminals C and D depends on the polarity of the induced voltage in the secondary winding, which is determined by the winding sense and its relation to the primary voltage.



(a) Different polarity **(b)** Same polarity

Fig. 4.17: Winding sense of a transformer

Furthermore, the total electrostatic energy stored within the transformer can be expressed as the sum of the energy stored in each individual capacitance. For ten independent capacitances between all pairs of the five terminals (A, B, C, D, and E), the total energy W_e is given by [15]

$$\begin{aligned} W_\mathrm{e} = &\frac{1}{2}C_1V_\mathrm{AB}^2 + \frac{1}{2}C_2V_\mathrm{CD}^2 + \frac{1}{2}C_3V_\mathrm{DB}^2 + \frac{1}{2}C_4V_\mathrm{AC}^2 + \frac{1}{2}C_5V_\mathrm{BC}^2 \\ &+\frac{1}{2}C_6V_\mathrm{AD}^2 + \frac{1}{2}C_7V_\mathrm{AE}^2 + \frac{1}{2}C_8V_\mathrm{BE}^2 + \frac{1}{2}C_9V_\mathrm{CE}^2 + \frac{1}{2}C_{10}V_\mathrm{DE}^2. \end{aligned} \tag{4.25}$$

To simplify the representation of the stored electrostatic energy, all potential differences in the capacitive equivalent circuit are referred to a set of four independent potential differences: V_1, V_2, V_3, and V_4, where the definition of these voltages are as follow

$$\begin{aligned} &V_\mathrm{AB} = V_1, && V_\mathrm{CD} = V_2, && V_\mathrm{DB} = V_3, && V_\mathrm{BE} = V_4, \\ &V_\mathrm{AC} = V_1 - V_3 - V_2, && V_\mathrm{BC} = V_2 + V_3, && V_\mathrm{AD} = V_1 - V_3, \\ &V_\mathrm{AE} = V_1 + V_4, && V_\mathrm{CE} = V_2 + V_3 + V_4, && V_\mathrm{DE} = V_3 + V_4. \end{aligned} \tag{4.26}$$

By substituting the voltage terms from equation (4.26) into the general energy expression given in equation (4.25), the total electrostatic energy can be fully expressed in terms of the four independent voltage differences V_1, V_2, V_3, and V_4. This yields the following reformulated expression [22]

$$\begin{aligned} W_\mathrm{e} =& \frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2 + \frac{1}{2}C_3V_3^2 + \frac{1}{2}C_4(V_1 - V_3 - V_2)^2 + \frac{1}{2}C_5(V_2 + V_3)^2 \\ &+ \frac{1}{2}C_6(V_1 - V_3)^2 + \frac{1}{2}C_7(V_1 + V_4)^2 + \frac{1}{2}C_8V_4^2 + \frac{1}{2}C_9(V_2 + V_3 + V_4)^2 \\ &+ \frac{1}{2}C_{10}(V_3 + V_4)^2. \end{aligned} \tag{4.27}$$

However, this implies that a total of ten independent electrostatic simulations are required in order to determine all ten capacitances. Similar to the approach used in the inductor case, each simulation yields one energy value, and together they provide a system of ten linear equations as illustrated in (4.28). Solving this system enables the unique identification of all capacitances in the equivalent circuit.

$$\underbrace{\begin{bmatrix} W_{e,1} \\ W_{e,2} \\ \vdots \\ W_{e,10} \end{bmatrix}}_{10\times1} = \frac{1}{2}\underbrace{\begin{bmatrix} V_1^2 & V_2^2 & V_3^2 & (V_1 - V_3 - V_2)^2 & (V_2 + V_3)^2 & (V_1 - V_3)^2 & (V_1 + V_4)^2 & V_4^2 & (V_2 + V_3 + V_4)^2 & (V_3 + V_4)^2 \\ V_{1,2}^2 & V_{2,2}^2 & V_{3,2}^2 & (V_{1,2} - V_{3,2} - V_{2,2})^2 & (V_{2,2} + V_{3,2})^2 & (V_{1,2} - V_{3,2})^2 & (V_{1,2} + V_{4,2})^2 & V_{4,2}^2 & (V_{2,2} + V_{3,2} + V_{4,2})^2 & (V_{3,2} + V_{4,2})^2 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ V_{1,10}^2 & V_{2,10}^2 & V_{3,10}^2 & (V_{1,10} - V_{3,10} - V_{2,10})^2 & (V_{2,10} + V_{3,10})^2 & (V_{1,10} - V_{3,10})^2 & (V_{1,10} + V_{4,10})^2 & V_{4,10}^2 & (V_{2,10} + V_{3,10} + V_{4,10})^2 & (V_{3,10} + V_{4,10})^2 \end{bmatrix}}_{10\times10} \underbrace{\begin{bmatrix} C_1 \\ C_2 \\ \vdots \\ C_{10} \end{bmatrix}}_{10\times1} \tag{4.28}$$

To apply the same simulation strategy used in the inductor case, the four independent potential differences in the transformer model V_1, V_2, V_3, and V_4 are defined using binary values, i.e., either 0 V or 1 V. This can be achieved by varying the terminal potentials $V_\mathrm{A}, V_\mathrm{B}, V_\mathrm{C}$, and V_D as shown in Tab. 4.6. For simplicity, the potential of the core V_E is kept constant at 0 V. These voltage differences are then used to evaluate the electrostatic energy stored in the system during each simulation. Following that, it is now possible to construct the full excitation matrix shown in equation (4.28). Each row of the matrix corresponds to one simulation, with the squared voltage differences serving as the coefficients of the unknown capacitances. This system of ten equations can then be solved using the electrostatic energy results obtained from each simulation, yielding all ten capacitances of the transformer's equivalent circuit.

Tab. 4.6: Terminal potentials and resulting voltage differences for transformer simulations

Simulation	V_A	V_B	V_C	V_D	V_E	$V_1 = V_\mathrm{AB}$	$V_2 = V_\mathrm{CD}$	$V_3 = V_\mathrm{DB}$	$V_4 = V_\mathrm{BE}$
1	1	0	0	0	0	1	0	0	0
2	0	0	1	0	0	0	1	0	0
3	0	0	1	1	0	0	0	1	0
4	1	1	1	1	0	0	0	0	1
5	1	0	1	0	0	1	1	0	0
6	1	0	1	1	0	1	0	1	0
7	2	1	1	1	0	1	0	0	1
8	0	0	2	1	0	0	1	1	0
9	1	1	2	1	0	0	1	0	1
10	1	1	2	2	0	0	0	1	1

However, the first simulation yields the capacitive configuration shown in Fig. 4.18. In this case, terminal A is held at 1 V, while all other terminals, including the core, are zeros. As a result, the voltage drop occurs exclusively across the capacitors connected to terminal A, which are C_1, C_4, C_6, and C_7. These are the only capacitors that contribute to the capacitive equivalent circuit in this simulation. Conversely, the remaining capacitors C_2, C_3, C_5, C_8, C_9, and C_{10} experience no potential difference and therefore can be removed from the capacitive equivalent circuit. These inactive elements are visually marked with a red "X" in the diagram to indicate their exclusion from energy calculations in this simulation.

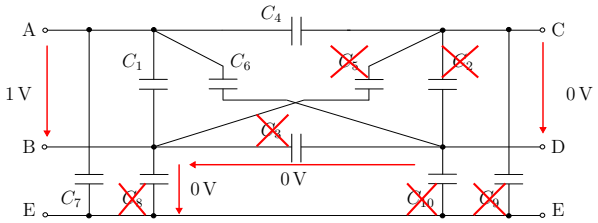


Fig. 4.18: Capacitive equivalent circuit of the transformer obtained from simulation 1

As another example, in simulation 8 as shown in Fig. 4.19, the goal is to excite the capacitances associated with the voltage differences $V_2 = V_{\mathrm{CD}}$ and $V_3 = V_{\mathrm{BD}}$, both of which are set to 1 V. To achieve this, the terminal potentials are assigned as follows: $V_{\mathrm{A}} = 0$ V, $V_{\mathrm{B}} = 0$ V, $V_{\mathrm{C}} = 2$ V, and $V_{\mathrm{D}} = 1$ V, while the core terminal V_{E} remains at 0 V.

With these values, the resulting voltage differences become

$$V_2 = V_{\mathrm{C}} - V_{\mathrm{D}} = 2\ \mathrm{V} - 1\ \mathrm{V} = 1\ \mathrm{V}, \quad V_3 = V_{\mathrm{D}} - V_{\mathrm{B}} = 1\ \mathrm{V} - 0\ \mathrm{V} = 1\ \mathrm{V}$$

and both $V_1 = V_{\mathrm{AB}} = V_{\mathrm{A}} - V_{\mathrm{B}} = 0$ and $V_4 = V_{\mathrm{BE}} = 0$. This configuration ensures that only capacitances dependent on V_2 and V_3 contribute to the capacitive equivalent circuit.

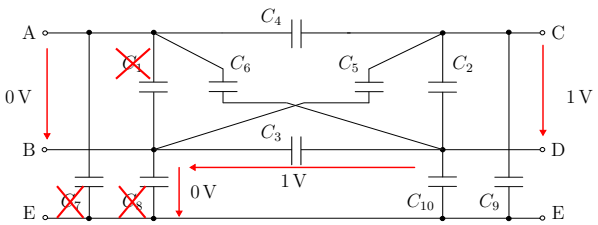


Fig. 4.19: Capacitive equivalent circuit of the transformer obtained simulation 8

However, the detailed equivalent circuit diagrams corresponding to each of the ten simulation cases are provided in the Appendix A.1 for completeness. These visual representations clearly illustrate which capacitances are active in each scenario based on the assigned

terminal potentials and resulting voltage differences. This allows for intuitive understanding of how each simulation contributes to the excitation matrix used for extracting the capacitance values.

After running the ten distinct electrostatic simulations defined by different combinations of terminal potentials, the resulting electrostatic energies $W_{e,i}$ for each case can be related to the ten unknown capacitances C_1 through C_{10} using the voltage expressions derived in equation (4.27). Since each energy term is a quadratic function of the relevant voltage differences, squaring the corresponding coefficients yields a system of ten linear equations in matrix form. The resulting excitation matrix, shown below in equation (4.29), is used to solve for the ten capacitance values in the equivalent circuit

$$\underbrace{\begin{bmatrix} W_{e,1} \\ W_{e,2} \\ W_{e,3} \\ W_{e,4} \\ W_{e,5} \\ W_{e,6} \\ W_{e,7} \\ W_{e,8} \\ W_{e,9} \\ W_{e,10} \end{bmatrix}}_{10\times1} = \frac{1}{2} \underbrace{\begin{bmatrix} 1&0&0&1&0&1&1&0&0&0 \\ 0&1&0&1&1&0&0&0&1&0 \\ 0&0&1&1&1&1&0&0&1&1 \\ 0&0&0&0&0&0&1&1&1&1 \\ 1&1&0&0&1&1&1&0&1&0 \\ 1&0&1&0&1&0&1&0&1&1 \\ 1&0&0&1&0&1&4&1&1&1 \\ 0&1&1&4&4&1&0&0&4&1 \\ 0&1&0&1&1&0&1&1&4&1 \\ 0&0&1&1&1&1&1&1&4&4 \end{bmatrix}}_{10\times10} \underbrace{\begin{bmatrix} C_1 \\ C_2 \\ C_3 \\ C_4 \\ C_5 \\ C_6 \\ C_7 \\ C_8 \\ C_9 \\ C_{10} \end{bmatrix}}_{10\times1} \tag{4.29}$$

However, to validate the accuracy of the electrostatic simulation results, a transformer was physically constructed and experimentally measured. The test transformer consists of a primary winding with 58 turns and a secondary winding with 50 turns, each made of wire with a diameter of 0.50 mm. The transformer is wound on a PQ40/40 ferrite core, and its geometry is illustrated in Fig. 4.20. Capacitance measurements were carried out using a `Wayne Kerr 6515B` impedance analyzer. The experimentally obtained results are compared with those from the electrostatic simulation to assess the reliability and accuracy of the proposed modeling approach.

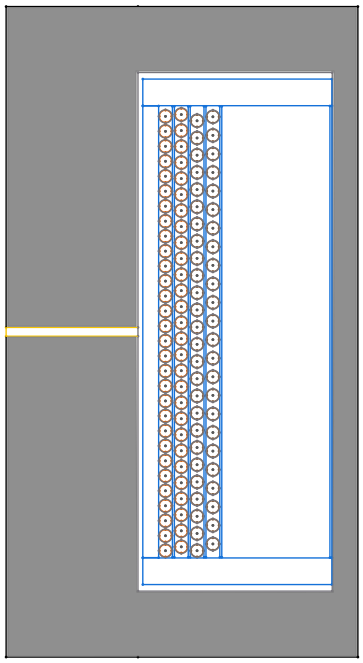


Fig. 4.20: Geometry of the constructed transformer

To extract the ten capacitances in the capacitive equivalent circuit, ten electrostatic simulations were performed, each with a distinct set of voltage excitations applied to the five terminals (A, B, C, D, E), as detailed previously in Table 4.6. The resulting stored electrostatic energy values $W_{e,i}$ from each scenario are then substituted into the system of equations given in equation (4.29). The system of equations becomes

$$\overbrace{\begin{bmatrix} 24.30 \\ 39.64 \\ 46.28 \\ 17.06 \\ 50.84 \\ 50.61 \\ 60.41 \\ 152.19 \\ 59.94 \\ 71.28 \end{bmatrix}}^{W_{e,i}\,[\mathrm{pJ}]}_{10\times1} = \frac{1}{2} \overbrace{\begin{bmatrix} 1&0&0&1&0&1&1&0&0&0 \\ 0&1&0&1&1&0&0&0&1&0 \\ 0&0&1&1&1&1&0&0&1&1 \\ 0&0&0&0&0&0&1&1&1&1 \\ 1&1&0&0&1&1&1&0&1&0 \\ 1&0&1&0&1&0&1&0&1&1 \\ 1&0&0&1&0&1&4&1&1&1 \\ 0&1&1&4&4&1&0&0&4&1 \\ 0&1&0&1&1&0&1&1&4&1 \\ 0&0&1&1&1&1&1&1&4&4 \end{bmatrix}}^{\mathrm{V}^2\,[\mathrm{V}]}_{10\times10} \overbrace{\begin{bmatrix} C_1 \\ C_2 \\ C_3 \\ C_4 \\ C_5 \\ C_6 \\ C_7 \\ C_8 \\ C_9 \\ C_{10} \end{bmatrix}}^{C_i\,[\mathrm{pF}]}_{10\times1} \tag{4.30}$$

The capacitance values listed in Tab. 4.7 were obtained by solving the system of equations defined in equation (4.30), using the stored electrostatic energy results from the ten simulated voltage excitation scenarios. These capacitances correspond to the individual coupling paths in the capacitive equivalent circuit of the transformer. Notably, the highest capacitance value is observed between terminals B and C ($C_5 = 49.922$ pF), indicating strong coupling between the primary and secondary windings. Meanwhile, other capacitances such as C_9 and C_{10}, which represent coupling between winding terminals and the core, are relatively smaller.

Tab. 4.7: Capacitance values extracted from electrostatic simulation

Capacitance (pF)	
C_1	9.582
C_2	13.009
C_3	14.737
C_4	13.098
C_5	49.922
C_6	6.873
C_7	19.051
C_8	7.132
C_9	3.247
C_{10}	4.688

To experimentally validate the proposed capacitive equivalent circuit model for the transformer, impedance measurements were performed using ten distinct terminal configurations. Each configuration corresponds to a specific connection between the transformer terminals A, B, C, D, and E. Fig. 4.21 presents the impedance magnitude and phase angle versus frequency for the ten measured terminal configurations of the 58-50 transformer.

The same methodology described in the inductor section 4.3 for extracting capacitances is applied here. These expressions allow for the determination of either the inductance or the capacitance based on the observed impedance magnitude and phase at specific frequencies. For configurations exhibiting inductive behavior, the capacitance is derived via the resonance frequency and extracted inductance using (4.21). For configurations that exhibit purely capacitive behavior, the capacitance is computed directly from the imaginary part of the impedance using (4.22).

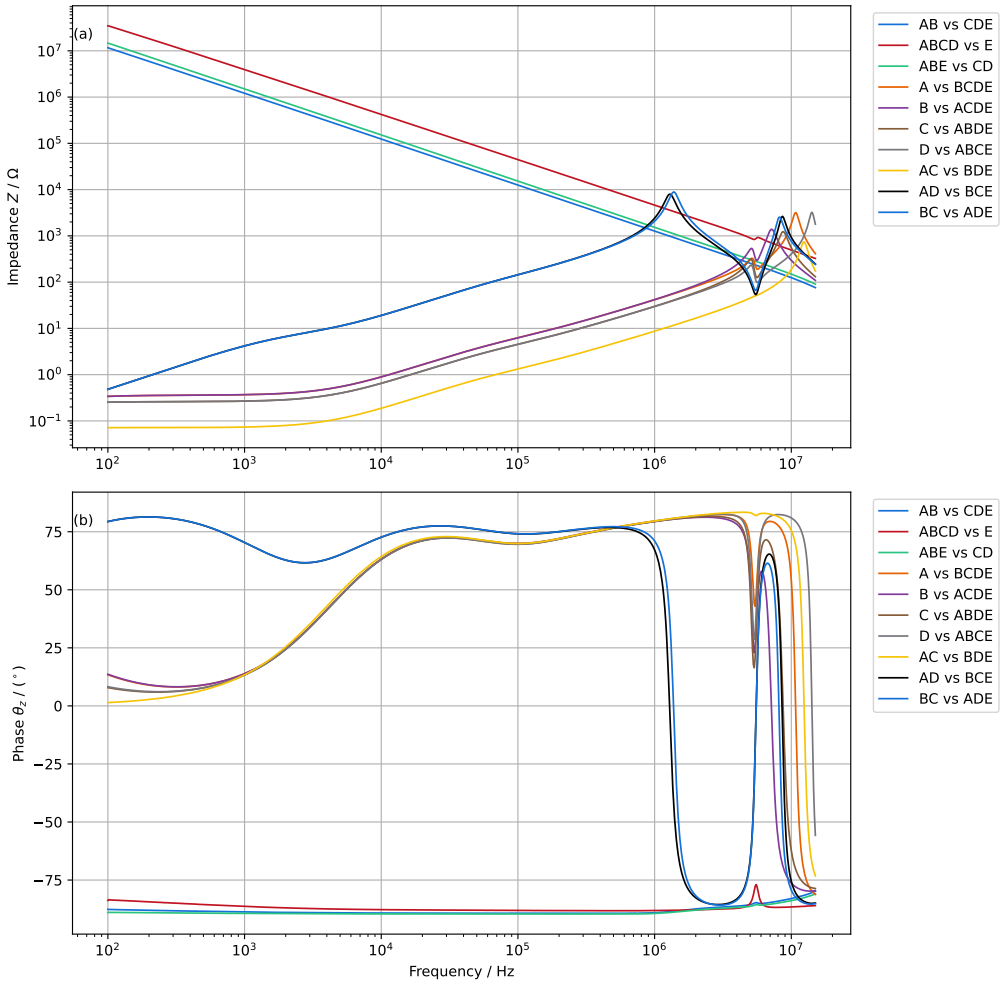


Fig. 4.21: Measured impedance magnitude (a) and phase (b) for ten different terminal configurations of the transformer. Each configuration corresponds to a specific capacitive coupling path in the equivalent circuit.

However, the extracted capacitances from measurements and simulations are compared for each of the ten terminal configurations. Table 4.8 provides a detailed comparison between the experimentally measured capacitance values and those obtained from the FEMMT simulation for the corresponding terminal excitations. Each configuration is characterized by a distinct set of voltage conditions and an associated equivalent capacitance expression based on the coupling paths in the capacitive model. The close agreement between the measured and simulated values across most configurations validates the applicability of the electrostatic modeling approach to transformer structures with complex winding arrangements.

Tab. 4.8: Comparison between measurements and FEMMT simulation results for the transformer

Connection	**Measurement**	V_1	V_2	V_3	V_4	**Behaviour of EC**	**FEMMT**
AB vs CDE	125.72 pF	0	0	-1	1	$C_3 + C_4 + C_5 + C_6 + C_7 + C_8$	110.81 pF
ABCD vs E	358.15 pF	0	0	0	1	$C_7 + C_8 + C_9 + C_{10}$	34.11 pF
ABE vs CD	103.66 pF	0	0	-1	1	$C_3 + C_4 + C_5 + C_6 + C_9 + C_{10}$	92.56 pF
A vs BCDE	35.15 pF	1	0	0	0	$C_1 + C_4 + C_6 + C_7$	48.60 pF
B vs ACDE	76.39 pF	-1	0	-1	1	$C_1 + C_3 + C_5 + C_8$	81.37 pF
C vs ABDE	72.49 pF	0	1	0	0	$C_2 + C_4 + C_5 + C_9$	79.28 pF
D vs ABCE	28.56 pF	0	-1	1	0	$C_2 + C_3 + C_6 + C_{10}$	39.31 pF
AC vs BDE	122.07 pF	1	1	0	0	$C_1 + C_2 + C_5 + C_6 + C_7 + C_9$	101.08 pF
AD vs BCE	81.12 pF	1	-1	1	0	$C_1 + C_2 + C_3 + C_4 + C_7 + C_{10}$	74.17 pF
BC vs ADE	62.37 pF	-1	1	-1	1	$C_1 + C_2 + C_3 + C_4 + C_8 + C_9$	60.81 pF
A vs B (CD Open)	56.63 pF	V_m	nV_m	(4.32a)	(4.32b)	(4.33)	80.28 pF
A vs B (CD short)	24.23 pF	V_m	0	(4.34a)	(4.34b)	(4.35)	31.40 pF

In addition, although it might seem reasonable to determine the individual capacitances of the equivalent circuit $C_1, C_2, \ldots, C_{10}$ by solving the system of equations derived from measured connection capacitances, this approach is not feasible for the transformer structure. The excitation matrix involved in such a computation is ill-conditioned, meaning that even small perturbations in the measurement data can result in large deviations in the computed capacitances. Consequently, the inversion of the excitation matrix under these conditions would produce highly unreliable results [22]. Therefore, the equivalent circuit capacitances cannot be directly validated through measurements in this case. A direct extraction would only be possible if the equivalent circuit were reduced to a smaller number of parameters, such as six capacitances when the core is neglected, proposed in [23] [24]. For that reason, the validation is kept on the connections described in Tab. 4.8.

Fig. 4.22 visualizes the comparison between the simulated and measured capacitance sums for each of the ten terminal configurations listed in Tab. 4.8. The measured values, obtained through impedance analysis, are shown alongside the simulated results. To quantify the agreement, the ratio of simulated to measured capacitance is annotated above each data point. A ratio close to unity indicates strong correlation between the two methods. In addition, the majority of the configurations demonstrate excellent consistency, further supporting the accuracy and reliability of the proposed electrostatic modeling approach.

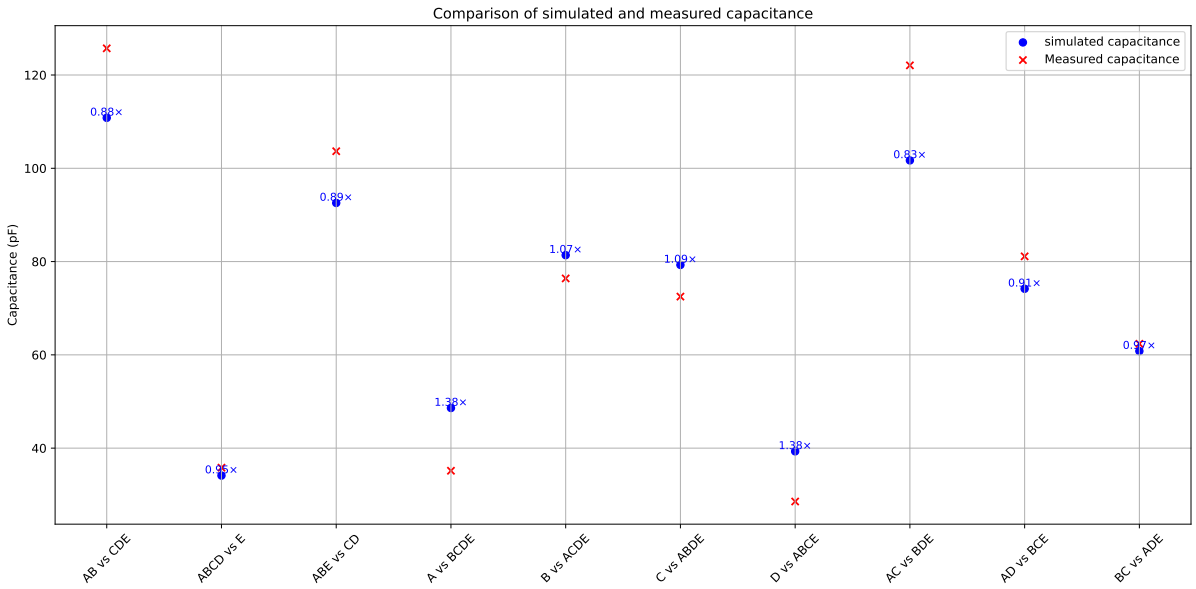


Fig. 4.22: Comparison between simulated and measured capacitance for various terminal configurations of the 58-50 transformer. Error ratios are annotated for each configuration, representing the ratio of simulated to measured capacitance.

In addition, for the cases of the connections A vs B with CD open and A vs B with CD shorted, the voltages V_1 and V_2 in Tab. 4.8 correspond to the applied voltages at the input and output terminals of the transformer, respectively. In the measurement setup, $V_1 = 1\,\mathrm{V}$ and $V_2 = n \times 1\,\mathrm{V}$, where n is the turns ratio of the transformer. In contrast, the voltages V_3 and V_4 depend on the electrostatic potential differences between nodes D and B, and between node B and the core potential E. Notably, V_3 can assume a finite value even when nodes B and D are electrically disconnected, such as when terminal D is floating. In such scenarios, the floating potential adjusts itself to minimize the total electrostatic energy. A similar principle applies to V_4 when the core is floating. Therefore, from equation (4.25), The voltages V_3 and V_4 can be determined as the values that minimize the electrostatic energy W_e [22].

$$V_{3,\,\mathrm{float-D}} = \frac{(C_4 + C_6)V_1 - (C_4 + C_5 + C_9)V_4 - (C_9 + C_{10})V_4}{C_3 + C_4 + C_5 + C_6 + C_9 + C_{10}} \tag{4.31a}$$

$$V_{4,\,\mathrm{float-E}} = \frac{-C_7V_1 - C_9V_2 - (C_9 + C_{10})V_3}{C_7 + C_8 + C_9 + C_{10}} \tag{4.31b}$$

Therefore, the expressions for V_3 and V_4 under these conditions, when C and D are open, can be derived by minimizing W_e, and are given as follows [22]

$$V_3 = \frac{V_\mathrm{m}(C_4 + C_6 + C_7(C_9 + C_{10}))}{C_7 + C_8 + C_9 + C_{10}} - \frac{V_\mathrm{m} n(C_4 + C_5 + C_9 - C_9(C_9 + C_{10}))}{C_7 + C_8 + C_9 + C_{10}} \cdot \left(\frac{1}{C_3 + C_4 + C_5 + C_6 + C_9 + C_{10} - \frac{(C_9 + C_{10})^2}{C_7 + C_8 + C_9 + C_{10}}} \right) \tag{4.32a}$$

$$V_4 = -\frac{V_\mathrm{m}(C_7 + (C_4 + C_6)(C_9 + C_{10}))}{C_3 + C_4 + C_5 + C_6 + C_9 + C_{10}} + \frac{V_\mathrm{m} n(C_9 - (C_9 + C_{10})(C_4 + C_5 + C_9))}{C_3 + C_4 + C_5 + C_6 + C_9 + C_{10}} \cdot \left(\frac{1}{C_7 + C_8 + C_9 + C_{10} - \frac{(C_9 + C_{10})^2}{C_3 + C_4 + C_5 + C_6 + C_9 + C_{10}}} \right). \tag{4.32b}$$

Due to the complexity involved in deriving the behavior of the equivalent circuit when terminals C and D are open, the equation for C_open is decomposed into four parts, which are three numerators and a denominator. λ_1, λ_2, and λ_3 are the numerators and λ_4 is the denominator. The derivations of λ_1, λ_2, λ_3 and λ_4 is shown in A.2.1. Thus, the behavior of the equivalent circuit when terminals C and D are open can be written as [22]

$$C_\mathrm{open} = \frac{n^2 \cdot \lambda_1 - n \cdot \lambda_2 + \lambda_3}{\lambda_4}. \tag{4.33}$$

In the case where terminals C and D are shorted, the electrostatic behavior of the system changes due to the direct electrical connection between these two nodes. Consequently, under these conditions, the resulting expressions for V_3 and V_4 can be derived as follows [22]

$$V_3 = \frac{V_\mathrm{m}(C_4 + C_6 + C_7(C_9 + C_{10}))}{C_7 + C_8 + C_9 + C_{10}} \cdot \left(\frac{1}{C_3 + C_4 + C_5 + C_6 + C_9 + C_{10} - \frac{(C_9 + C_{10})^2}{C_7 + C_8 + C_9 + C_{10}}} \right) \tag{4.34a}$$

$$V_4 = -\frac{V_\mathrm{m}\,(C_7 + (C_4 + C_6)(C_9 + C_{10}))}{C_3 + C_4 + C_5 + C_6 + C_9 + C_{10}} \cdot \left(\frac{1}{C_7 + C_8 + C_9 + C_{10} - \frac{(C_9 + C_{10})^2}{C_3 + C_4 + C_5 + C_6 + C_9 + C_{10}}} \right). \tag{4.34b}$$

However, in the case of the measurement configuration labeled “A vs B (CD short)” in Tab. 4.8, the equivalent circuit behavior can still be represented in a structured form involving a numerator and a denominator as shown in A.2.2. Thus, the behavior of the equivalent circuit, when C and D are short, can be written as:

$$C_\mathrm{short} = \frac{C_1 + \lambda_1}{\lambda_2} \tag{4.35}$$

Furthermore, as shown in Fig. 4.23, the simulated results are derived based on the analytical expressions developed previously in (4.33) and (A.2.2), while the measured values are obtained experimentally. For both configurations, the simulated values show agreement with measurements. The ratio of simulated to measured capacitance is annotated on each bar, with values of 1.42 and 1.30 for the CD open and CD short cases, respectively. These deviations can be attributed to slight inaccuracies in the material parameters, or geometry tolerances.

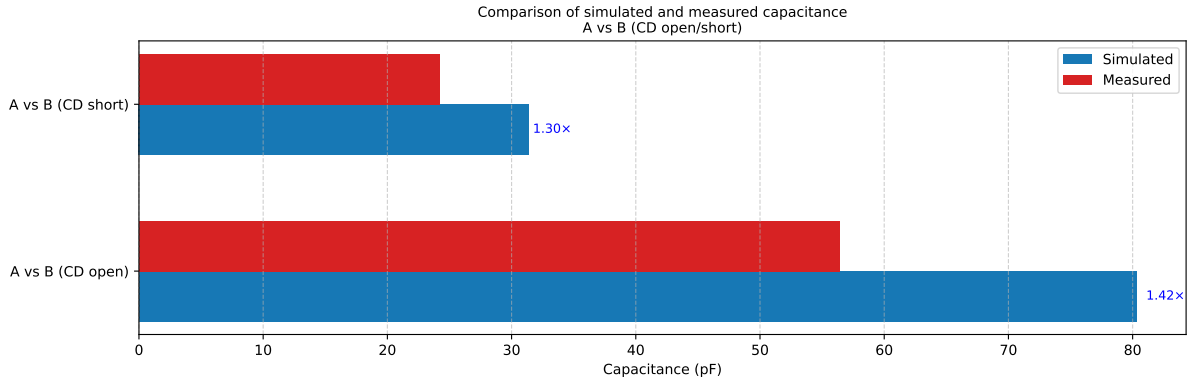


Fig. 4.23: Comparison between simulated and measured capacitance for the connection A vs B with terminals C and D either open or shorted

However, in FEMMT, two functions are implemented to extract the capacitive equivalent circuit based on the simulated electrostatic field distribution. These functions are `get_inductor_capacitance()` for extracting the capacitances in the equivalent circuit of inductors and `get_transformer_capacitance()` for extracting the capacitances in the equivalent circuit of transformers. Each function can be executed after defining the winding geometry, and assigning material properties. This capability of FEMMT provides a distinct advantage over commercial tools such as ANSYS, where the extraction of equivalent capacitances typically requires manual post-processing or complex scripting.

```
1    geo.get_inductor_capacitance()
2    geo.get_transformer_capacitance()
```

Listing 4.1: Implemented functions for extracting the capacitances in FEMMT

An interesting direction for future work is the extension of the presented methodology to multi-winding transformers, where the number of windings exceeds two windings. In such cases, the capacitive equivalent circuit becomes increasingly complex, with a significantly higher number of coupling capacitances.

5 Application Example: LLC Converter

To demonstrate the practical relevance of the developed electrostatic capacitance extraction methodology, an LLC resonant converter is used as a case study. The goal is to investigate how variations in transformer design, specifically the spatial separation between primary and secondary windings, influence the common mode (CM) behavior in DC-DC converters.

The LLC resonant converter shown in Fig. 5.1 consists of three main functional stages, which are the bridge driver, the LC resonant tank, and the rectification stage. At the input side, a full-bridge inverter formed by four switching devices (S_1 to S_4) converts the DC input voltage V_i into an AC waveform. This excitation is then applied to the LC resonant tank, which comprises a resonant capacitor C_r, a series inductor L_r, and the magnetizing inductance L_m of the transformer. The resonant tank enables soft switching conditions over a wide frequency range and shapes the voltage and current waveforms to achieve high efficiency. The transformer provides galvanic isolation between the primary and secondary sides and also scales the voltage according to the turns ratio n. On the secondary side, the AC voltage is rectified using a diode bridge to produce a DC output voltage V_o [3].

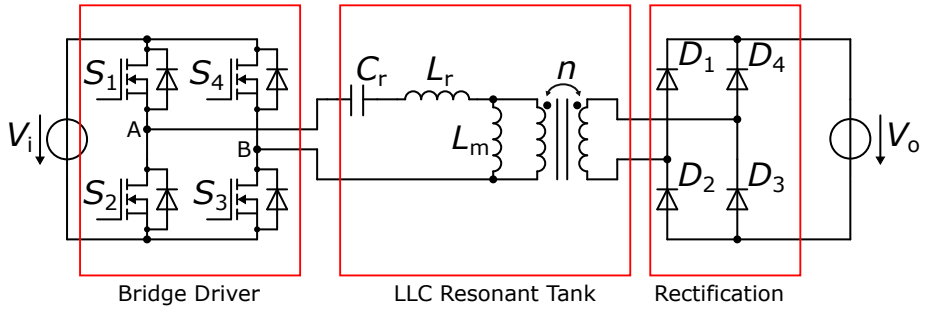
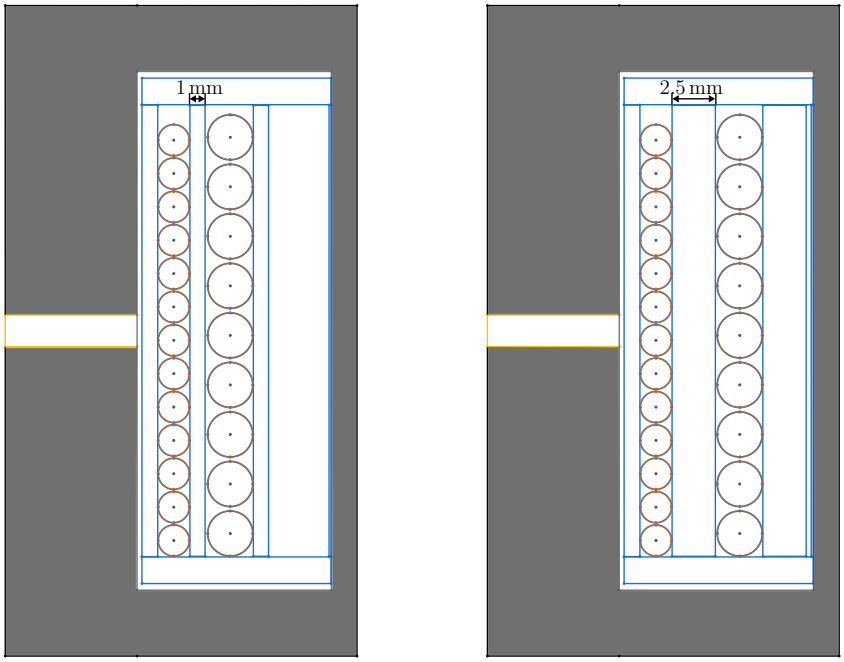


Fig. 5.1: LLC Converter

However, two transformer prototypes A and B are designed and implemented within the same LLC converter topology as shown in Fig. 5.2. The first transformer shown in Fig. 5.2a features a compact winding arrangement with minimal separation between the primary and secondary windings. The second transformer shown in Fig. 5.2b, in contrast, was constructed with a larger spatial distance between the windings to reduce capacitive coupling. The primary winding consists of $N_\mathrm{p} = 13$ turns wound from a litz bundle of 405 strands, each with a radius of 35.5 µm, and a fill factor $k_\mathrm{fill} = 0.67$; the secondary winding comprises $N_\mathrm{s} = 9$ turns made from 1200 strands of 30 µm radius, using the same fill factor.

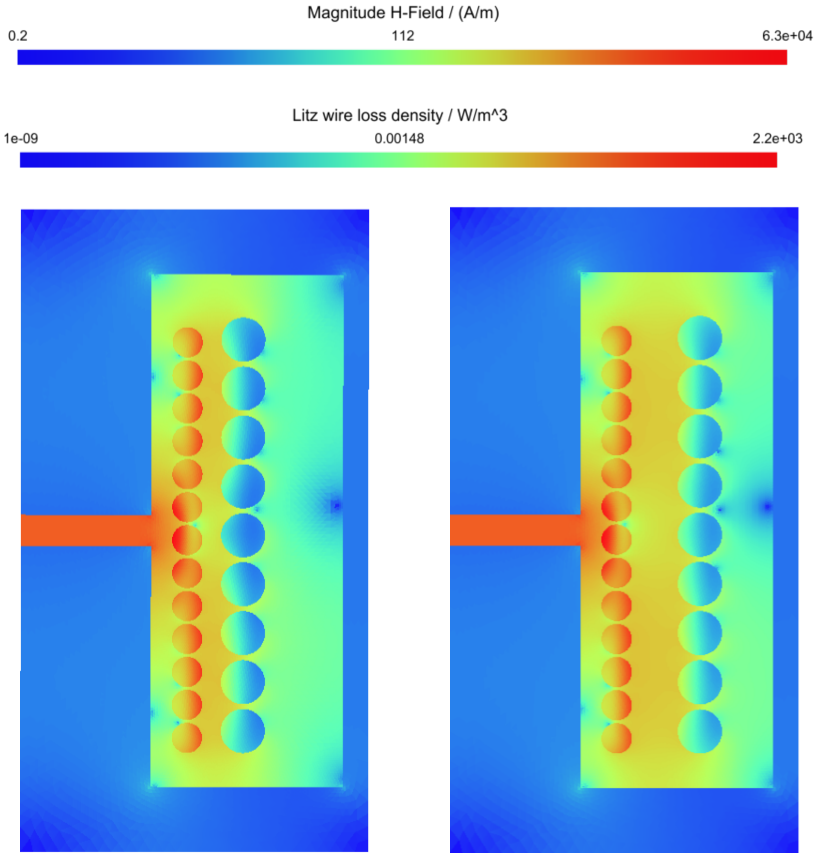


(a) Geometry of transformer A with 1 mm between the primary and secondary

(b) Geometry of transformer B with 2.5 mm between the primary and secondary

Fig. 5.2: Transformer geometry used in LLC converter

Consequently, Fig. 5.3 illustrates the simulated steady-state magnetic-field magnitude together with the volumetric loss density in the litz conductors for the two transformer layouts shown in Fig. 5.2. With an inter-winding gap of 1 mm, as depicted in Fig. 5.3a, the primary and secondary conductors are tightly coupled, and only a small fraction of the magnetic flux returns through the air; the resulting leakage inductance is therefore low. When the spacing is increased to 2.5 mm, as depicted in Fig. 5.3b, the return path widens, allowing a larger portion of the flux to bypass the core and travel through the air region between the windings. The longer, less-tightly-coupled flux path yields a higher leakage inductance [26].

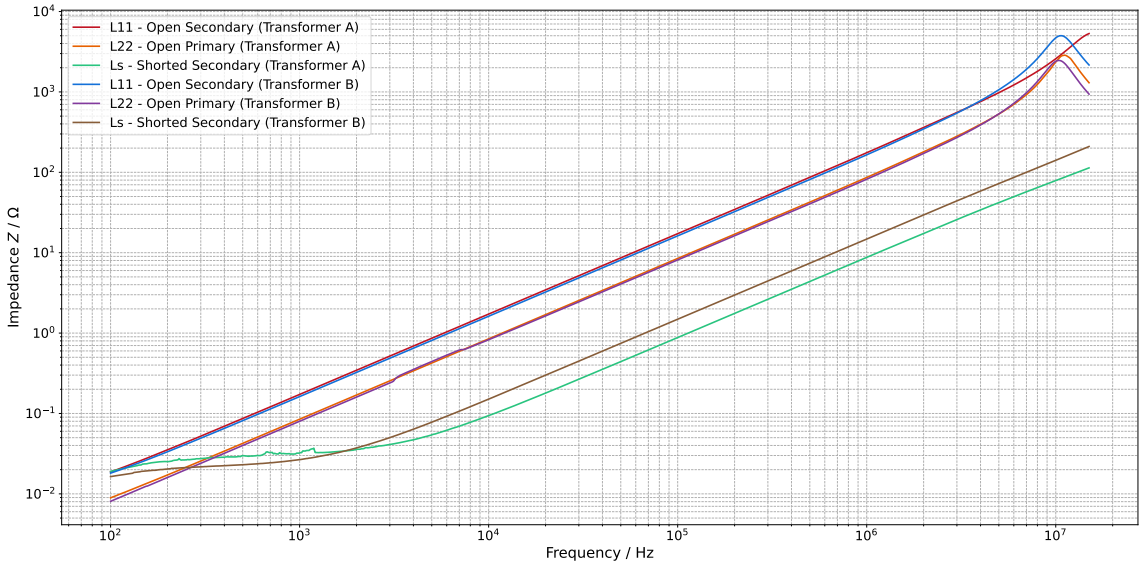


(a) Magnetic simulation for transformer A with 1 mm inter-winding gap

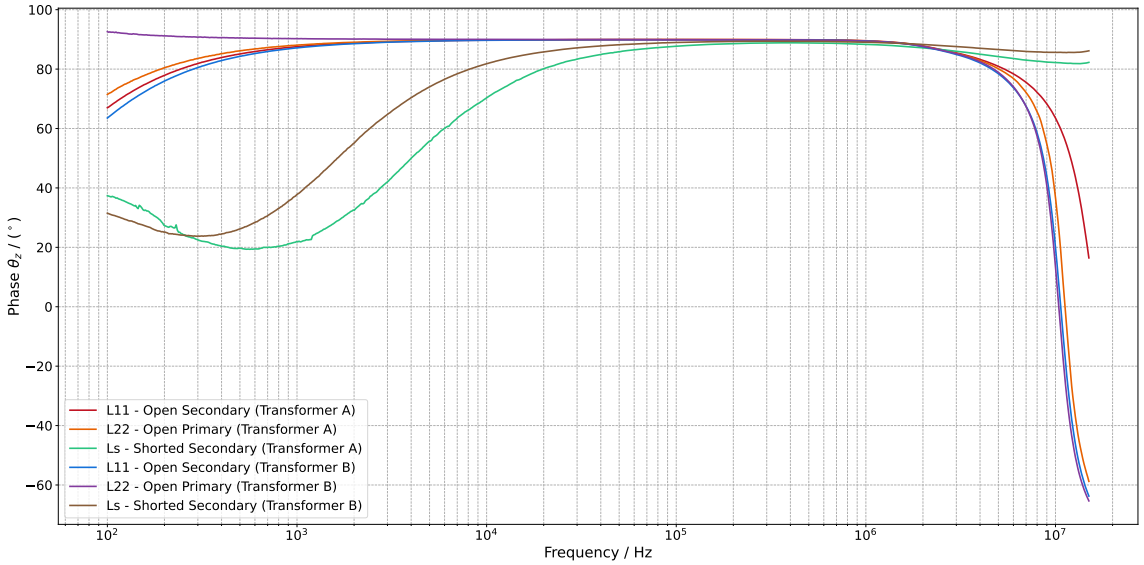
(b) Magnetic simulation fortransformer B with 2.5 mm inter-winding gap

Fig. 5.3: Magnetic field and winding loss density for both transformers

To quantify the impact of the inter-winding distance on the magnetic coupling behavior, both transformer prototypes are characterized through simulation and experimental measurement. However, the impedance measurements for both transformer prototypes under various terminal conditions are presented in Fig. 5.4. In the top subplot, the impedance magnitude $|Z|$ is plotted over a logarithmic frequency axis. The open-circuit configurations corresponding to L_{11} and L_{22} primarily capture the self-inductance of the respective windings. The short-circuit configuration, used to extract the leakage inductance L_{s}, shows a significantly lower impedance magnitude, especially for transformer A. This is consistent with the reduced inter-winding distance of 1 mm, which leads to tighter magnetic coupling and reduced leakage flux. In addition, it is important to note that within the frequency range covered in the measurements using `Wayne Kerr 6515B` impedance analyzer, no distinct resonance peak is observed in most configurations.



(a) Impedance magnitude



(b) Impedance phase

Fig. 5.4: Measured impedance magnitude (a) and phase (b) for open-circuit and short-circuit configurations of both transformer prototypes.

Tab. 5.1 presents the extracted values for the self-inductance of the primary L_{11} and secondary L_{22} , as well as the leakage inductance L_{s}. The simulation results are obtained using FEMMT, while the measured values are derived from an impedance analyzer. For both prototypes, the simulated and measured values show good agreement, validating the accuracy of the modeling approach. However, as expected, transformer B, which is with

a larger spacing of 2.5 mm, exhibits a significantly higher leakage inductance compared to transformer A, consistent with the magnetic field simulations discussed earlier.

Tab. 5.1: Simulated and measured inductance values for the two transformer prototypes

Inductance	Transformer A (1 mm gap)		Transformer B (2.5 mm gap)	
	Simulation	Measurement	Simulation	Measurement
L_{11}	26.68 µH	27.43 µH	26.68 µH	27.77 µH
L_{22}	13.43 µH	13.49 µH	13.87 µH	13.93 µH
L_{s}	1.357 µH	1.399 µH	2.201 µH	2.368 µH

Furthermore, the capacitances of both transformers are extracted using the electrostatic simulation methodology described in Section 4.4. However, the implementation of electrostatic simulation in femmt currently supports only solid conductors. Since the transformer prototypes in this work employ litz wire, an approximation is made by modeling the conductors as solid in the electrostatic simulations. This simplification allows for an estimation of the winding capacitances, although it may introduce a minor deviation from the actual physical behavior due to the distributed nature of the litz structure.

Tab. 5.2 lists the capacitance values obtained from electrostatic simulations for both transformer prototypes, corresponding to the capacitive equivalent circuit of the transformer. It can be observed that with the increase in spatial separation between the primary and secondary windings, from 1 mm in transformer A to 2.5 mm in transformer B, the values of common-mode capacitances, such as C_3, C_4, C_5 and C_6, are reduced. The increased gap introduces greater electric field fringing and reduces the effective plate area overlap, resulting in weaker capacitive coupling. The negative capacitance C_1, and C_2 appear due to the mathematical modeling approach described in section 4.3, which explains that achieving an accurate representation of electrostatic energy distribution in inductors and transformers may require certain capacitances to be represented by negative values.

Meanwhile, some capacitances involving ground (e.g., C_7 to C_{10}) show a smaller variation or even an increase, which may be attributed to the redistribution of electric field lines due to the wider physical layout. When the distance between the windings is increased, the electrostatic energy becomes more concentrated in the region between the windings and the magnetic core. However, Despite these individual differences, the total open-circuit terminal capacitance C_{open}, calculated using the symbolic expression described in section 4.4 using equation (4.33), remains relatively similar for both prototypes, with only a slight reduction in transformer B. However, it is important to note that the terminal configurations described earlier in Tab. 4.8 cannot be fully validated based on the measurement results for both transformers, as the resonance frequencies associated with many of the capacitive coupling paths lie beyond the upper frequency limit of the Wayne Kerr 6515B impedance analyzer.

Tab. 5.2: Simulated capacitance values for the two transformer prototypes

Capacitance	Transformer A (1 mm gap)	Transformer B (2.5 mm gap)
C_1	−6.65 pF	−5.60 pF
C_2	−4.27 pF	−6.07 pF
C_3	4.27 pF	6.89 pF
C_4	3.97 pF	7.05 pF
C_5	9.48 pF	3.61 pF
C_6	9.82 pF	3.04 pF
C_7	12.14 pF	12.63 pF
C_8	11.11 pF	11.57 pF
C_9	7.12 pF	17.79 pF
C_{10}	6.03 pF	16.56 pF
$C_{\text{open, sim}}$	24.37 pF	23.55 pF

Nevertheless, an exception is observed for transformer B in the configuration where terminals A and B are excited and terminals C and D are left open. In this case, a noticeable resonance peak appears around 10.5 MHz, which can serve as an approximate validation point for the capacitive model. The open-circuit capacitance was determined using both simulation and measurement for transformer B. The measurement was performed following the procedure described in equation (4.21). The results of both approaches are summarized in the following equations

$$\begin{gathered} C_{\text{open, meas}} = 9.77\,\text{pF}, \quad C_{\text{open, sim}} = 23.55\,\text{pF} \\ \text{Error Ratio} = \frac{C_{\text{open, sim}}}{C_{\text{open, meas}}} = 2.27. \end{gathered} \tag{5.1}$$

However, if the validation is based solely on the resonance frequency observed near the upper limit of the measured spectrum, the resulting error becomes more significant. This indicates that the approximation made in the electrostatic simulation for these transformers, specifically, modeling the litz wire as a solid conductor, may no longer be sufficient to accurately capture the true capacitive behavior of the winding structure. Another important remark is that geometry tolerances can significantly influence the measured capacitance. In particular, the physical arrangement of the transformer during measurement, such as the additional length of the connection cables required to be connected to the converter, can introduce parasitic capacitances that are not accounted for in the simulation model. These additional effects may further contribute to the discrepancy between simulated and measured values. However, as this resonance corresponds only to the C_{open} configuration, it does not provide validation for the other terminal configurations

or coupling paths represented in the full capacitive equivalent circuit. Therefore, relying on this single resonance for verification may lead to misleading conclusions.

Meanwhile, due to the relatively low number of turns in both transformer prototypes, the resonance frequency could not be captured within the available measurement bandwidth. However, it should be note that existing studies focus on medium-voltage applications [4] [27], where also a higher number of turns is typically used in inductors and transformers, resulting in lower resonance frequencies that are easier to observe experimentally. In addition, parasitic capacitance plays more important role in medium-voltage applications, as higher voltage levels result in more electric field energy being stored in parasitic capacitors. This is especially relevant for medium-voltage SiC MOSFETs, where converter efficiencies exceeding 99 % have been reported for kVA-rated systems operating at switching frequencies of 5-10 kHz under hard-switching conditions [28][4][27]. In such scenarios, parasitic resistance effects are relatively less dominant, whereas parasitic capacitance becomes more significant due to the ultrafast switching transients, with voltage slew rates $\mathrm{d}v/\mathrm{d}t$ reaching up to 250 V/ns [1][4][27].

Due to the low number of turns in the transformer prototypes ($N_\mathrm{p} = 13$, $N_\mathrm{s} = 9$), there is limited flexibility to optimize the winding arrangement for minimizing parasitic capacitance. With such a small number of turns, options such as multi-layer structuring, advanced interleaving, or more distributed layouts are not feasible. Therefore, the impact of winding scheme optimization is less pronounced in this case compared to transformers with a higher number of turns.

In addition, another measurements of LLC converter with both transformers A and B are performed using a Teledyne LeCroy HDO4104 High Definition Oscilloscope (1 GHz, 2.5 GS/s) to capture the current flowing through the common-mode capacitances. Fig. 5.5 presents the measured waveforms for transformer prototypes A and B operating under identical conditions in an LLC resonant converter delivering 2 kW of output power. The top subplot presents the common-mode current. It is observable that transformer B, which has a larger spatial separation between windings, exhibits reduced common-mode current compared to transformer A. This supports the simulation results discussed earlier, indicating that increased distance between windings weakens the capacitive coupling and hence reduces the current through the parasitic capacitance. The middle subplot displays the primary-side current for both transformers. Despite the same excitation, differences in leakage and magnetizing inductance lead to slight waveform deviations. The bottom subplot shows the voltage at node A (see Fig. 5.1), referenced to ground.

In addition, a complementary EMC test was carried out on the same hardware, where the results of the measurement are summarised in Appendix A.3.

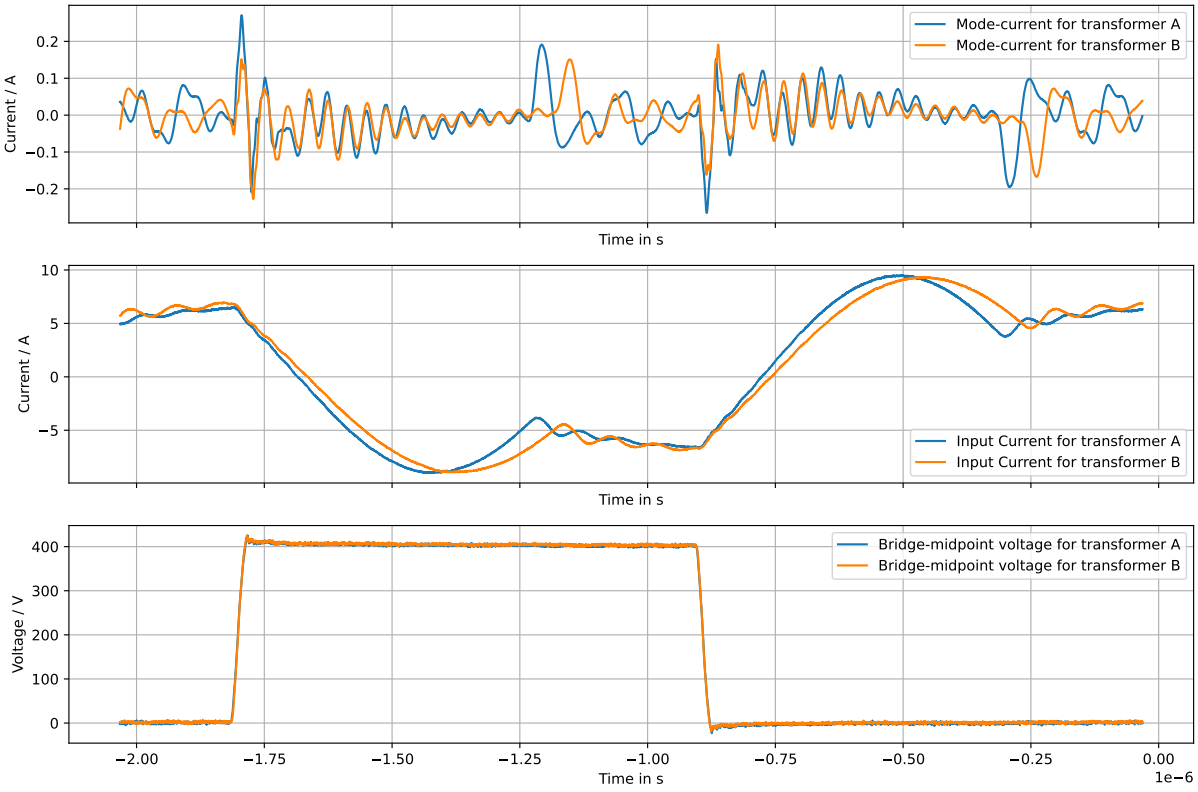


Fig. 5.5: Measured currents and voltages of the LLC converter using transformer prototypes A and B

6 Inductor Optimization

In this chapter, the focus shifts to the winding scheme of a single-winding inductor, investigating how turn ordering and spacing affect its parasitic capacitances and overall performance. The discussion begins by examining multi-layer winding configurations and the geometric parameters that govern the parasitic capacitance of the inductor. The objective is to assess the influence of different winding schemes while maintaining a fixed number of turns and an initially defined spacing between them. It should be noted, however, that this approach does not represent a full optimization. When the number of turns is modified, the airgap height and other geometric parameters should be adjusted to approximately maintain a constant inductance.

However, Fig. 6.1 illustrates one possible detailed turn arrangement within the inductor window. The left side of Fig. 6.1 shows the overall magnetic component geometry, highlighting the compact placement of the winding structure inside the core window. The right side of Fig. 6.1 depicts a winding configuration in which the turns are placed from bottom to top with a zigzag movement.

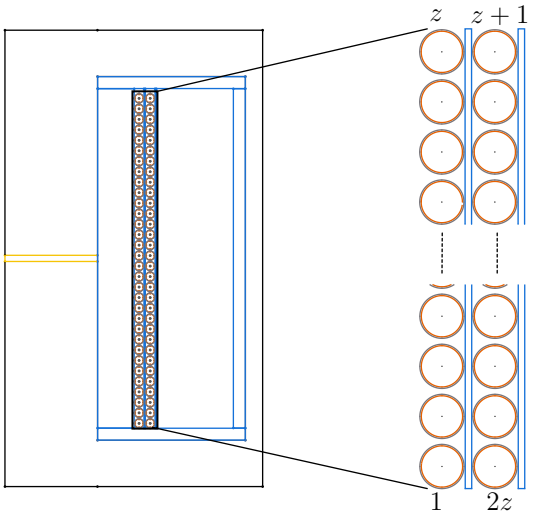


Fig. 6.1: Vertical winding arrangement with zigzag movement

In contrast, Fig. 6.2 illustrates an alternative winding arrangement where the turns are placed horizontally across the window before stacking vertically after completing a row. A zigzag movement is also applied in this case; after reaching the end of a row, the winding direction reverses for the next row, forming an alternating pattern. However, the horizontal arrangement alters the spatial distribution of the turns, which influence the parasitic capacitance and the magnetic coupling differently compared to the vertical arrangement configuration.

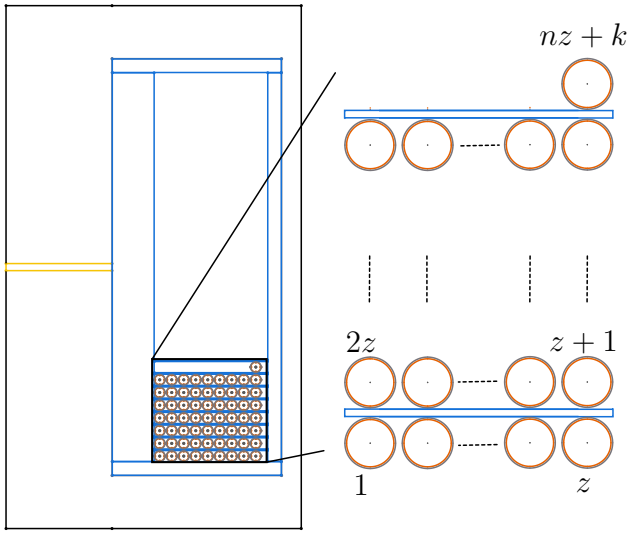


Fig. 6.2: Horizontal winding arrangement with zigzag movement

However, magnetic and electrostatic simulations for both winding arrangements are performed using FEMMT. The simulated inductor comprised 64 turns of solid conductor, each with a radius of 0.35 mm, whereas the spacing between adjacent turns is uniform, with $d_v = 0.1$ mm. Tab. 6.2 summarizes the simulation results for the two investigated winding configurations. The vertical zigzag arrangement achieves a lower inductance compared to the horizontal zigzag layout, as reflected in the inductance values. However, the vertical arrangement also leads to significantly higher parasitic capacitance, particularly C_1 and $C_{\mathrm{AB}(64)}$, due to the closer proximity and stronger coupling between adjacent turns. In terms of winding losses, the horizontal zigzag configuration exhibits higher total losses, which can be attributed to a less distribution of the magnetic field and increased leakage flux. Overall, the results highlight a trade-off between minimizing parasitic capacitance and controlling leakage inductance and losses when selecting the winding scheme.

Tab. 6.1: Comparison of losses, inductance, and capacitance for vertical and horizontal winding arrangements

Parameter	**Vertical Arrangement**	**Horizontal Arrangement**
Losses (W)	28.709	35.15
Inductance (mH)	2.012	2.257
C_1 (pF)	32.35	2.287
C_2 (pF)	22.49	31.25
C_3 (pF)	13.65	14.38
$C_{\mathrm{AB}}(64)$ (pF)	40.85	12.13

However, the vertical winding arrangement can be modified in order to have the same inductance and same losses while trying to minimize the parasitic capacitance of the inductor. Fig. 6.3 illustrates an alternative winding scheme that preserves the same total turns $n_{\mathrm{t}} = 64$ and uniform inter-turn spacing, but the second layer of turns is shifted farther away from the core's top, and the third layer of turns is shifted even more distally. Moreover, it is not expected to minimize the capacitance significantly using this arrangement of the conductors as just one layer is shifted farther away from the core.

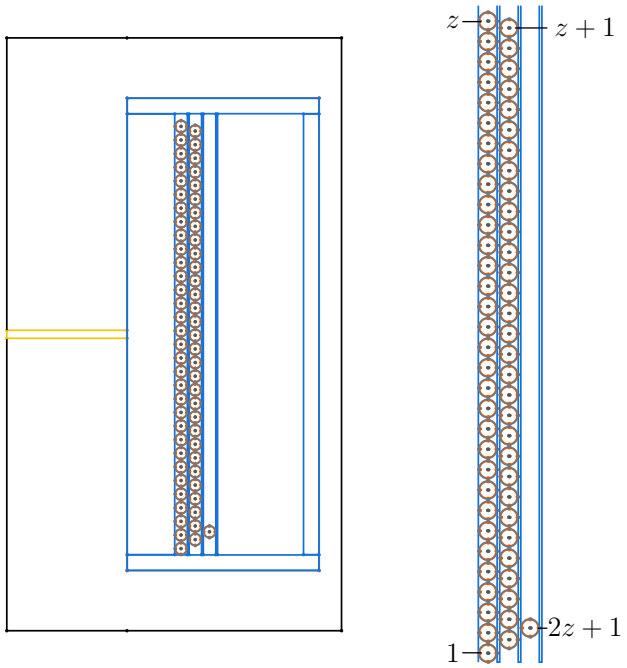


Fig. 6.3: Vertical winding arrangement with zigzag movement and different distances of layers to the core

Similarly, the horizontal winding arrangement can be modified in order to have the same inductance and same losses compared the the horizontal movement depicted previously in Fig. 6.2, while reducing the parasitic capacitance of the inductor. Fig. 6.4 illustrates an alternative winding scheme that preserves the same total turns $n_t = 64$ and uniform inter-turn spacing. Here, z denotes the number of complete turns per layer, and k is the number of additional turns that do not fill an entire layer (in this case $k = 4$). However, in this arrangement all even-numbered layers of turns is shifted farther away from the sides of the core.

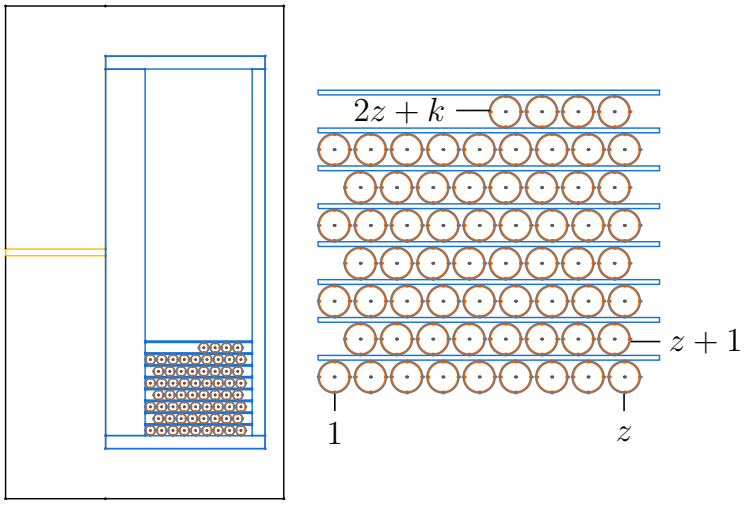


Fig. 6.4: Horizontal winding arrangement with zigzag movement and different distances of layers to the core

Tab. 6.2 summarizes the impact of the optimized winding schemes on key performance metrics. The vertical I represents the winding scheme for vertical movement shown previously in Fig. 6.1, whereas vertical II represents the optimized winding scheme for vertical movement as shown in Fig. 6.3. Similarly, horizontal I represents the winding scheme for horizontal movement shown previously in Fig. 6.1, whereas horizontal II represents the optimized winding scheme for horizontal movement as shown in Fig. 6.3.

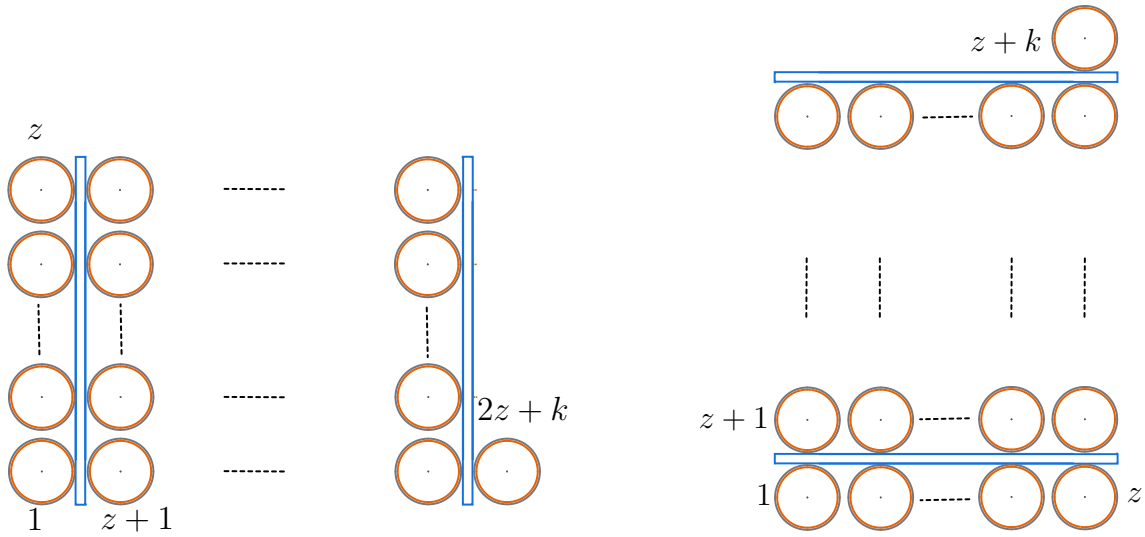
However, both optimized winding scheme for vertical and horizontal movements have a reduction of the stray capacitance of the inductor with 8.27 % and 14.83 %, receptively. The inductance and loss values of both optimized winding schemes remain essentially unchanged compared to those of the original winding schemes. The capacitance C_1, which represents the capacitance of the terminals A-B, as defined previously in chapter 4.3 in Fig. 4.7b is reduced in both optimized winding schemes, with the optimized horizontal scheme producing the most reduction. The capacitance C_3 which represents the capacitance of the terminals B-E, as defined previously in chapter 4.3 in Fig. 4.7b is decreased in the optimized schemes, where C_2 remains essentially unchanged, exhibiting a slight increase in the optimized vertical scheme.

Tab. 6.2: Comparison of losses, inductance, and capacitance for different winding arrangements with different distances of layers of turns to the core

Parameter	**Vertical I**	**Vertical II**	**Reduction**
Losses (W)	28.709	28.756	–
Inductance (mH)	2.012	2.012	–
C_1 (pF)	32.35	29.74	8.06 %
C_2 (pF)	22.49	23.02	−2.3 %
C_3 (pF)	13.65	11.63	14.79 %
$C_{\mathrm{AB}}(64)$ (pF)	40.85	37.47	8.27 %
Parameter	**Horizontal I**	**Horizontal II**	**Reduction**
Losses (W)	35.15	34.95	–
Inductance (mH)	2.257	2.257	–
C_1 (pF)	2.287	1.269	44.51 %
C_2 (pF)	31.25	30.96	0.928 %
C_3 (pF)	14.38	12.82	10.84 %
$C_{\mathrm{AB}}(64)$ (pF)	12.13	10.33	14.83 %

Furthermore, an alternative winding scheme is introduced as shown Fig. 6.5. Fig. 6.5a shows that all layers are wound in the same direction, such that from bottom to top. Similarity, Fig. 6.5b shows that all layers are wound in the same direction, such that from left to right. However, irrespective of how the connection is made between turn z at the right end of the first layer and turn $z + 1$ at the left end of the second layer, the focus here is solely on the effect of this scheme on the winding capacitance [15].

In this winding scheme, because all turns across successive layers follow the same winding direction, the potential difference between vertically adjacent layers in the vertical scheme remains nearly constant along the entire winding width. Similarly, the potential difference between horizontally adjacent layers in the vertical scheme remains nearly constant along the entire winding height. Specifically, in the vertical winding scheme, the voltage difference between a turn on the left layer and its adjacent turn to the right is minimized, tending toward a value close to $U_0/2$, where U_0 is the total voltage applied across the coil. Likewise, in the horizontal winding scheme, the voltage difference between a turn in the lower layer and the corresponding turn directly above it tends toward $U_0/2$. As a result, the electric field between adjacent layers or adjacent turns is reduced compared to conventional alternating-layer schemes, where larger potential differences typically occur. Consequently, this arrangement significantly decreases the inter-layer and inter-turn capacitance, leading to a lower overall parasitic capacitance for the inductor. [15]



(a) bottom to top **(b)** left to right

Fig. 6.5: Vertical and horizontal schemes without zigzag movement

The different winding schemes described previously are now compared in terms of their influence on the key electrical parameters of the inductor, while maintaining a fixed inductance and loss level. Tab. 6.3 summarizes the losses, inductance, and extracted capacitances for all investigated winding schemes.

It can be observed that, by optimizing the winding arrangement, a significant reduction in the parasitic capacitances, particularly C_1 and $C_{\mathrm{AB}}(64)$, can be achieved without compromising the inductance or increasing the losses. The vertical III and horizontal III configurations, where all turns are wound consistently in the same direction across the layers, show the highest reduction in parasitic capacitance compared to the original zigzag-based winding schemes. However, For the vertical winding schemes, the Vertical III configuration achieves the greatest reduction in stray capacitance, with a decrease of 24.79 %. Similarly, for the horizontal winding schemes, the Horizontal II configuration exhibits the most significant reduction in stray capacitance, amounting to 14.83 %.

It is worth noting that the stray capacitances in the inductor can be further minimized by adjusting structural parameters, while keeping the same inductance and decreasing the losses through changing some parameters such as the height of the air gap and the number of turns. In addition, by increasing or decreasing the spacing between the turns or between certain winding layers, the electric field distribution can be changed, thereby reducing the capacitive coupling between adjacent turns or layers. Furthermore, Parasitic capacitance can also be minimized by maximizing the distance between the winding and the core [15].

Tab. 6.3: Comparison of losses, inductance, and capacitance for all described winding arrangements

Parameter	**Vertical I**	**Vertical II**	**Reduction I**	**Vertical III**	**Reduction I**
Losses (W)	28.709	28.756	–	28.709	–
Inductance (mH)	2.012	2.012	–	2.012	–
C_1 (pF)	32.35	29.74	8.06 %	22.45	30.60 %
C_2 (pF)	22.49	23.02	-2.3 %	23.32	-3.69 %
C_3 (pF)	13.65	11.63	14.79 %	12.82	-68.64 %
$C_{\mathrm{AB}}(64)$ (pF)	40.85	37.47	8.27 %	30.72	24.79 %
Parameter	**Horizontal I**	**Horizontal II**	**Reduction I**	**Horizontal III**	**Reduction I**
Losses (W)	35.15	34.95	–	32.35	–
Inductance (mH)	2.257	2.257	–	32.35	–
C_1 (pF)	2.287	1.269	44.51 %	0.905	60.42 %
C_2 (pF)	31.25	30.96	0.928 %	30.85	1.280 %
C_3 (pF)	14.38	12.82	10.84 %	14.08	2.086 %
$C_{\mathrm{AB}}(64)$ (pF)	12.13	10.33	14.83 %	10.57	12.86 %

However, without considering the inductance and the losses, the most effective approach for minimizing the parasitic capacitance of an inductor is to implement a single-layer winding configuration. If a single-layer winding is not feasible, the parasitic capacitance can be minimized by avoiding two-layer windings and instead using a large number of thinner layers [15] [21], as it has already seen in the horizontal movement shown in Fig. 6.2. Tab. 6.4 shows the results from magnetic and electrostatic simulations with different number of layers, where the number of turns in every layer is $n_t = 32$. It is observable that that the capacitances for three-layers of turns are smaller than the capacitance for two-layers of turns. Moreover, a single-layer of turns has the smallest capacitances compared to others.

Tab. 6.4: Comparison of multi-layers of turns of an inductor

Parameter	**Single-layer**	**Two-layers**	**Three-layers**
Losses (W)	6.74	28.756	67.33
Inductance (mH)	0.503	2.012	4.27
C_1 (pF)	-3.84	32.35	28.83
C_2 (pF)	16.94	22.49	26.16
C_3 (pF)	15.24	13.65	14.82
C_{AB} (pF)	4.18	40.85	38.07

7 Conclusion

This work aimed to investigate and minimize the parasitic capacitance in magnetic components, with a particular focus on inductors and transformers used in DC-DC converters. To achieve this, the FEM Magnetics Toolbox (FEMMT) was successfully extended to include electrostatic simulation capabilities, enabling the combined analysis of magnetic and capacitive effects within a unified framework. The integration involved the development of a dedicated electrostatic solver, including new modules for geometry definition, excitation assignment, solving the Poisson equation, and post-processing of results.

The electrostatic simulation feature was validated through cross-comparison with results obtained from the commercial tool ANSYS and experimental measurements, demonstrating good agreement and confirming the reliability of the developed method. Using FEM Magnetics Toolbox (FEMMT), detailed capacitance models for inductors and transformers were established, accounting for inter-turn, inter-layer, and turn-to-core coupling mechanisms.

To demonstrate the practical relevance of the developed methodology, an application example involving an LLC resonant converter was presented. Two transformer prototypes with different spatial separations between the primary and secondary windings were designed and characterized. The electrostatic simulations and experimental measurements confirmed that increasing the winding separation reduces the parasitic capacitance and, consequently, the common-mode current, thereby improving the electromagnetic compatibility (EMC) performance of the converter.

In addition, a dedicated optimization study was performed on inductors to investigate the impact of different winding schemes and insulation strategies on the total parasitic capacitance. The results highlighted that material selection, geometric layout, and winding arrangement have a significant influence on electrostatic energy storage and parasitic capacitance, offering valuable design guidelines for minimizing capacitive effects in magnetic components.

Overall, the contributions of this thesis provide an effective simulation and design methodology for accurately predicting and studying the methodology of minimizing parasitic capacitance, particularly in inductors.

7.1 Future Work

During the course of this thesis, several perspectives emerged for future investigations.

First, the current electrostatic simulation capability integrated into the FEM Magnetics Toolbox (FEMMT) supports only solid conductors. However, as demonstrated during the experimental validation phase, especially when modeling transformers wound with litz wire, this simplification introduces a noticeable deviation between simulated and measured capacitances. Therefore, a valuable extension of the FEM Magnetics Toolbox (FEMMT) would be the development of electrostatic simulation capabilities that accurately model litz wire structures. This enhancement would allow for more precise predictions of parasitic capacitance in practical applications where litz wire is commonly used.

Second, while this work primarily focused on inductors and transformers with two windings, future studies should extend the investigation to components featuring more than two windings. In multi-winding magnetic components, the complexity of capacitive coupling paths increases significantly, necessitating a more detailed equivalent circuit modeling and extraction methodology.

Finally, a more comprehensive optimization study should be conducted to systematically minimize parasitic capacitances in inductors and transformers. This would involve not only adjusting the winding scheme but also adjusting geometric parameters such as core material, air gap dimensions, and conductor placement, while maintaining required magnetic performance. Such a multi-objective optimization approach could lead to more robust designs with improved electromagnetic compatibility and overall system efficiency.

Appendix

In this chapter, all relevant supplementary plots are presented.

A.1 Behavior of the Equivalent Circuit

In this section, the behavior of the equivalent circuit of transformer for all ten electrostatic simulation are illustrated. Each configuration corresponds to a unique set of terminal voltage assignments used to activate different subsets of the equivalent capacitances in the transformer model. These setups are crucial for generating the linear system used to solve for the unknown capacitance values, as discussed in Section 4.4. Each figure shows which capacitors are active (i.e., contribute to energy storage) and which are not, with inactive capacitors marked using red crosses.

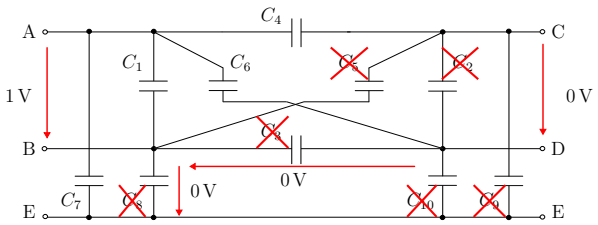


Fig. A.1: Capacitive equivalent circuit of the transformer obtained from simulation 1

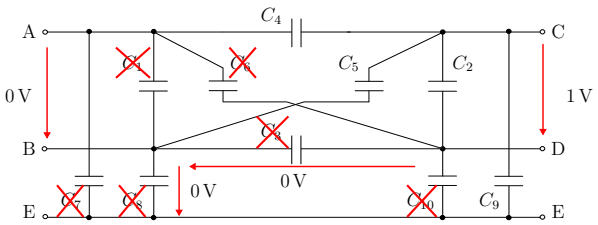


Fig. A.2: Capacitive equivalent circuit of the transformer obtained from simulation 2

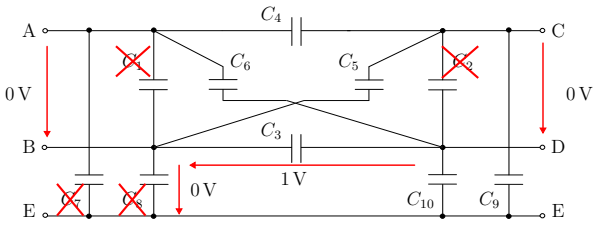


Fig. A.3: Capacitive equivalent circuit of the transformer obtained from simulation 3

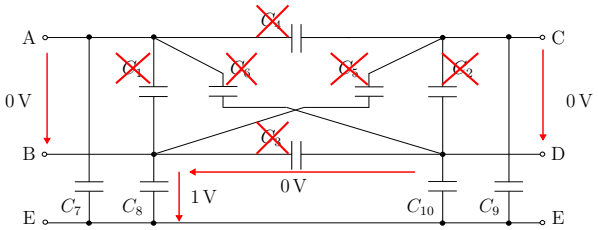


Fig. A.4: Capacitive equivalent circuit of the transformer obtained from simulation 4

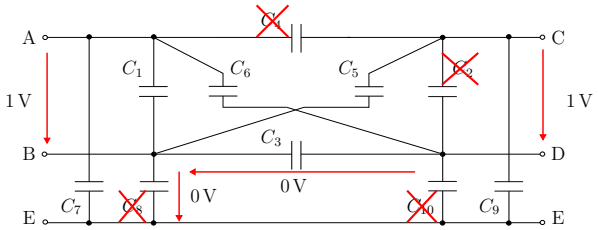


Fig. A.5: Capacitive equivalent circuit of the transformer obtained from simulation 5

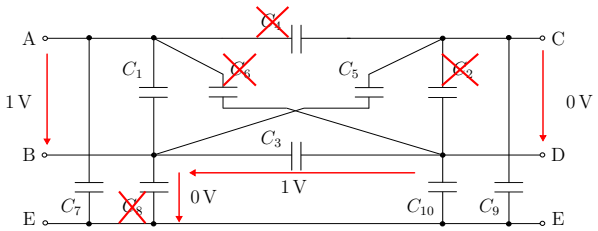


Fig. A.6: Capacitive equivalent circuit of the transformer obtained from simulation 6

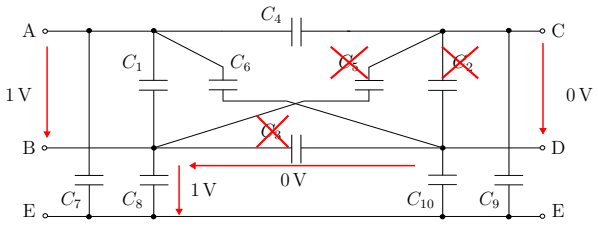


Fig. A.7: Capacitive equivalent circuit of the transformer obtained from simulation 7

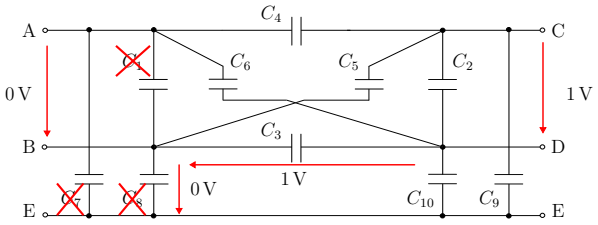


Fig. A.8: Capacitive equivalent circuit of the transformer obtained from simulation 8

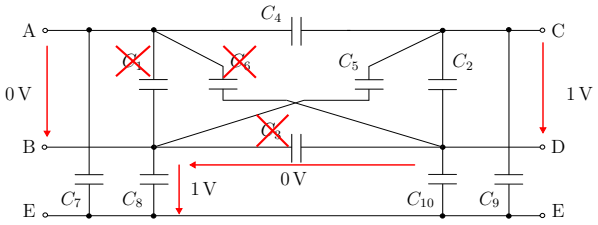


Fig. A.9: Capacitive equivalent circuit of the transformer obtained from simulation 9

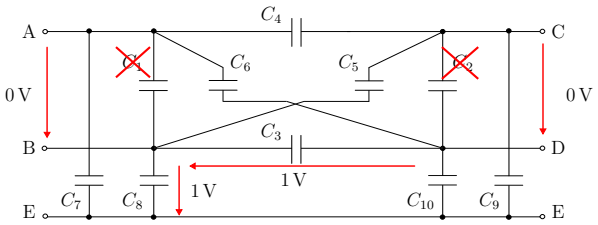


Fig. A.10: Capacitive equivalent circuit of the transformer obtained from simulation 10

A.2 Behavior of EC for Open and Short Circuit

A.2.1 A vs B (CD open)

$$\begin{aligned}\lambda_1 = {} & C_2C_3C_7 + C_2C_3C_8 + C_2C_4C_7 + C_2C_3C_9 + C_2C_4C_8 + C_2C_5C_7 + C_3C_4C_7 + C_2C_3C_{10} \\ & + C_2C_4C_9 + C_2C_5C_8 + C_2C_6C_7 + C_3C_4C_8 + C_3C_5C_7 + C_2C_4C_{10} + C_2C_5C_9 \\ & + C_2C_6C_8 + C_3C_4C_9 + C_3C_5C_8 + C_2C_5C_{10} + C_2C_6C_9 + C_3C_4C_{10} + C_3C_5C_9 \\ & + C_4C_6C_7 + C_2C_6C_{10} + C_2C_7C_9 + C_3C_5C_{10} + C_4C_6C_8 + C_5C_6C_7 + C_2C_7C_{10} \\ & + C_2C_8C_9 + C_3C_7C_9 + C_4C_6C_9 + C_5C_6C_8 + C_2C_8C_{10} + C_3C_8C_9 + C_4C_6C_{10} \\ & + C_5C_6C_9 + C_4C_7C_{10} + C_5C_6C_{10} + C_3C_9C_{10} + C_4C_8C_{10} + C_5C_7C_{10} + C_6C_7C_9 \\ & + C_4C_9C_{10} + C_5C_8C_{10} + C_6C_8C_9 + C_5C_9C_{10} + C_6C_9C_{10} + C_7C_9C_{10} + C_8C_9C_{10}\end{aligned}$$

$$\begin{aligned}\lambda_2 = {} & 2C_3C_4C_7 + 2C_3C_4C_8 + 2C_3C_4C_9 + 2C_3C_4C_{10} - 2C_5C_6C_7 + 2C_3C_7C_9 \\ & - 2C_5C_6C_8 - 2C_5C_6C_9 - 2C_5C_6C_{10} + 2C_4C_8C_{10} - 2C_5C_7C_{10} - 2C_6C_8C_9\end{aligned}$$

$$\begin{aligned}\lambda_3 = {} & C_1C_3C_7 + C_1C_3C_8 + C_1C_4C_7 + C_1C_3C_9 + C_1C_4C_8 + C_1C_5C_7 + C_1C_3C_{10} \\ & + C_1C_4C_9 + C_1C_5C_8 + C_1C_6C_7 + C_3C_4C_7 + C_1C_4C_{10} + C_1C_5C_9 + C_1C_6C_8 \\ & + C_3C_4C_8 + C_1C_5C_{10} + C_1C_6C_9 + C_3C_4C_9 + C_3C_6C_7 + C_4C_5C_7 + C_1C_6C_{10} \\ & + C_1C_7C_9 + C_3C_4C_{10} + C_3C_6C_8 + C_4C_5C_8 + C_1C_7C_{10} + C_1C_8C_9 + C_3C_6C_9 \\ & + C_3C_7C_8 + C_4C_5C_9 + C_5C_6C_7 + C_1C_8C_{10} + C_3C_6C_{10} + C_3C_7C_9 + C_4C_5C_{10} \\ & + C_4C_7C_8 + C_5C_6C_8 + C_3C_7C_{10} + C_5C_6C_9 + C_5C_7C_8 + C_4C_8C_9 + C_5C_6C_{10} \\ & + C_5C_7C_9 + C_6C_7C_8 + C_4C_8C_{10} + C_5C_7C_{10} + C_6C_8C_9 + C_6C_8C_{10} \\ & + C_7C_8C_9 + C_7C_8C_{10}\end{aligned}$$

$$\begin{aligned}\lambda_4 = {} & C_3C_7 + C_3C_8 + C_4C_7 + C_3C_9 + C_4C_8 + C_5C_7 + C_3C_{10} + C_4C_9 + C_5C_8 + C_6C_7 \\ & + C_4C_{10} + C_5C_9 + C_6C_8 + C_5C_{10} + C_6C_9 + C_6C_{10} + C_7C_9 + C_7C_{10} \\ & + C_8C_9 + C_8C_{10}\end{aligned}$$

A.2.2 A vs B (CD short)

$$\begin{aligned}\lambda_1 = {} & C_3C_4C_7 + C_3C_4C_8 + C_3C_4C_9 + C_3C_6C_7 + C_4C_5C_7 + C_3C_6C_8 + C_4C_5C_8 \\ & + C_3C_6C_9 + C_3C_7C_8 + C_4C_5C_9 + C_5C_6C_7 + C_3C_6C_{10} + C_3C_7C_9 + C_4C_7C_8 \\ & + C_5C_6C_9 + C_5C_7C_8 + C_4C_8C_9 + C_5C_6C_{10} + C_5C_7C_9 + C_6C_7C_8 + C_4C_8C_{10} \\ & + C_5C_7C_{10} + C_6C_8C_9 + C_6C_8C_{10} + C_7C_8C_9 + C_7C_8C_{10}\end{aligned}$$

$$\begin{aligned}\lambda_2 = {} & C_3C_7 + C_3C_8 + C_4C_7 + C_3C_9 + C_4C_8 + C_5C_7 + C_3C_{10} + C_4C_9 + C_5C_8 + C_6C_7 \\ & + C_4C_{10} + C_5C_9 + C_6C_8 + C_5C_{10} + C_6C_9 + C_6C_{10} + C_7C_9 + C_7C_{10} \\ & + C_8C_9 + C_8C_{10}\end{aligned}$$

A.3 EMC Measurements

To characterize the EMC performance of the LLC converter, a pre-compliance measurement was carried out, as schematized in Fig. A.11. The EMC test consists of a line impedance stabilization network (LISN), which is inserted between the 400 V DC link and the converter under test, and its RF output was routed via a 10 dB pulse limiter to a Rohde & Schwarz ESRP EMI test receiver. However, as the receiver supports different standard detection modes, such as peak detection (PK), quasi-peak detection (QP), and average detection (AV) [29], all spectra shown here were recorded using the peak detection (PK) mode. The converter used in the EMC test is shown in Fig. A.13. Figure A.12 compares the conducted-EMI spectra of transformer A (inter-winding gap 1 mm) and transformer B (2.5 mm gap)

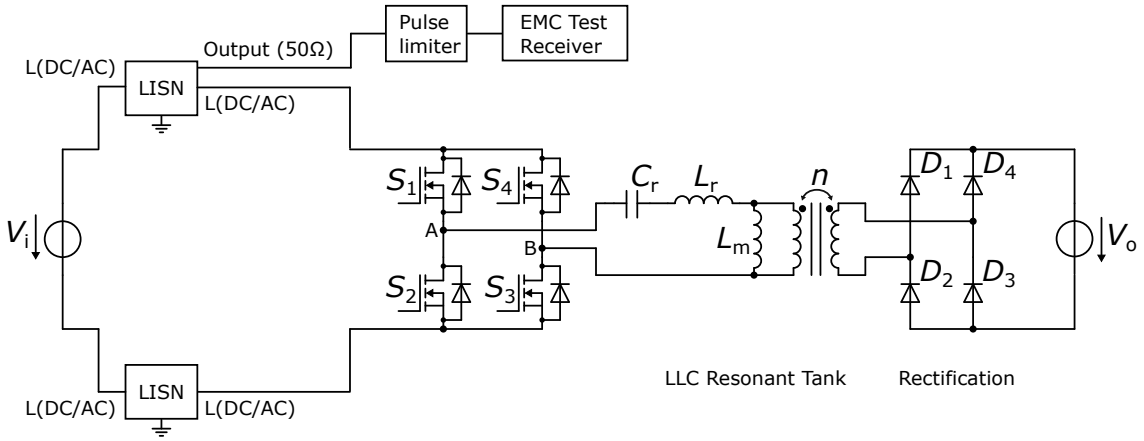


Fig. A.11: Electromagnetic-compatibility (EMC) measurement setup for the LLC converter

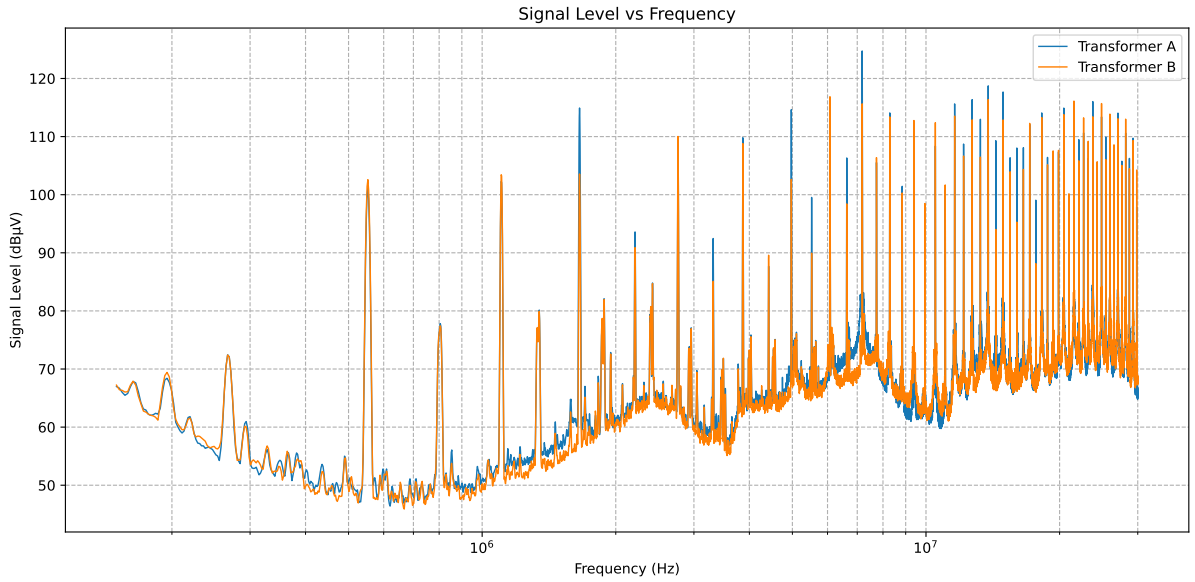


Fig. A.12: Conducted-emission spectrum of the LLC converter measured with the peak detector (comparison of transformers A and B)

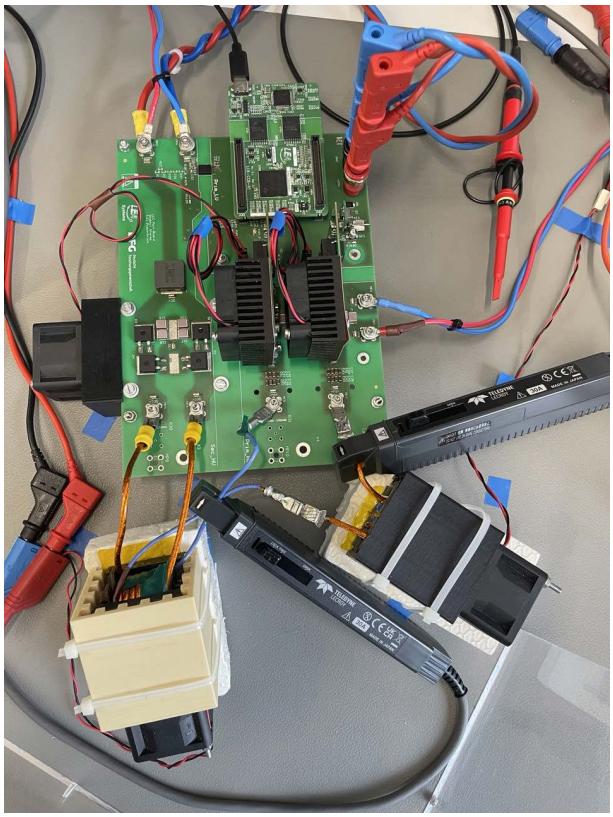


Fig. A.13: Prototype system in LEA lab

List of Figures

List of Tables

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