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# Half-Cycle-Sampled Discrete Model of Series-Parallel Resonant Converter with Optimized Modulation and its Control Design

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# Abstract

In the development of isolated DC-DC converters, series-parallel-resonant converter (SPRC) demonstrates its advantages with regard to wide operation range, high efficiency and highly dynamic performance. Compared to phase-shifted full bridge converter (PSFB), SPRC topology presents a limited utilization, because of its nonlinear gain and dynamic characteristics. The complexity of its model and further difficulties of its control design are the bottle-necks of this problem.

Due to the nonlinear characteristics of the SPRC, the primary objective of this work is to find a balanced modelling method for the SPRC between its complexity and accuracy. In the research of optimized modulation strategy (OM), it is interesting to find out the control signals in the OM modulator are sampled every half cycle of resonant oscillation with varying the switching frequency. From this point, this varying-step sampling can be applied in the modelling approach and also in the control design. This discrete system, with synchronized sampling steps in converter, modulator and controller, is called "half-cycle-sampled discrete (HSD) system". It is proved to be the best balanced modelling approach for describing the SPRC. It efficiently utilizes the calculation resources and has sufficient accuracy for the SPRC. This HSD modelling approach takes the dynamic behaviour of the modulator into consideration.

The second objective of this work is to design the appropriate controller in order to improve the dynamic performance of the SPRC. With the accurate dynamic model of the SPRC, the discrete controller with the varying sampling step is considered an optional improvement. The other improvement is to utilize the width of pulses as the control signal instead of the duty ratio. A novel control algorithm, HSD-PW control, is proposed combining these two improvements. It demonstrates that HSD-PW control clearly reduces the control settling time of output voltage in the experiment.

Subsequently, the calculation system of the entire controlled SPRC is implemented in the computer, in order to simulate the dynamic behaviour of SPRC. All the design options are added to the calculation system as the modules. The calculation system has a simple algorithm and can be performed rapidly. It is a helpful tool for computer-aided design in the future.

# Zusammenfassung

Bei der Entwicklung von isolierten DC-DC-Wandlern zeichnet sich die Topologie des Serien-Parallel-Resonanzkonverters (SPRC) durch einen breiten Betriebsbereich, einen hohen Wirkungsgrad sowie durch eine hohe Dynamik aus. Im Gegensatz zur phasenverschobenen Vollbrücke (PSFB) weist die Topologie des SPRC eine nichtlineare Charakteristik auf, weshalb diese auf dem Anwendungsfeld von Gleichstromwandlern bislang nur in eingeschränkter Weise zum Einsatz kommt. Eine aufwändige Modellierung sowie der Entwurf einer geeigneten Regelung sind die wesentlichen Herausforderungen, die der Einsatz eines Serien-Parallel-Resonanzkonverters aufgrund seiner Komplexität mit sich bringt.

Das primäre Ziel dieser Arbeit war es, eine ausgewogene Modellierungsmethode für den SPRC zu finden, die einen Kompromiss zwischen Komplexität und Genauigkeit bezüglich der nichtlinearen Charakteristik erlaubt. Bei der Erforschung von optimierten Modulationsstrategien wurde festgestellt, dass der Modulator in jeder Halbperiode der Resonanzschwingung abgetastet und die Schaltfrequenz zu diesen Zeitpunkten angepasst werden kann. Aus dieser Erkenntnis heraus erscheint es sinnvoll, das Verfahren der Abtastung mit variabler Schrittweite in die Modellierung und den Reglerentwurf mit einzubeziehen. Das zeitdiskretisierte System mit synchronisierten Abtastschritten für Konverter, Modulator und Regelung wird „Halbperioden-abgetastetes diskretes (HSD) System“ genannt. Es hat sich als ausgewogenster Modellansatz zur Beschreibung des SPRC herausgestellt. Dieser nutzt die zur Verfügung stehenden Rechenressourcen in effizienter Weise und garantiert dabei gleichzeitig eine ausreichende Genauigkeit für den SPRC.

Ein weiteres Ziel dieser Arbeit war es, den entsprechenden Regler auszulegen, um die Dynamik des SPRC zu verbessern. Mit dem akkuraten, dynamischen Modell des SPRC kann auch der diskrete Regler mit variabler Abtastzeit als eine zusätzliche Verbesserung angesehen werden. Zu einer weiteren Verbesserung führte die Verwendung der Pulsbreite anstatt des Tastverhältnisses als Stellsignal. Mit einem neuartigen Regelalgorithmus, der HSD-PW-Regelung, können diese beiden Verbesserungen erzielt werden. Die HSD-PW-Regelung führte in praktischen Versuchsdurchführungen zu einer reduzierten Ausregelzeit der Ausgangsspannung.

Anschließend wurde das Modell des geregelten SPRC auf einem Rechner implementiert, um das dynamische Verhalten der SPRC zu simulieren. Zusätzliche Module, die in das Berechnungsverfahren integriert wurden, erlauben die Ausführung alle relevanten Entwurfsoptionen. Das Berechnungsverfahren selbst besteht aus einem einfachen Algorithmus, der nur relativ kurze Ausführungszeiten erfordert. Dieses Verfahren leistet in Form eines hilfreichen Werkzeugs einen wertvollen Beitrag im Bereich des Computer-aided Design.

# Notation

## Symbols

| Symbol | Explanation | Unity |
|---|---|---|
| $\alpha, \beta, \theta$ | Auxiliary angle values describing the waveform | rad |
| $\boldsymbol{A, B, C, D}$ | Transfer system matrix of small-signal model | |
| $\boldsymbol{A_d, B_d}$ | System matrix of discrete linear model | |
| $\boldsymbol{A_{pw}, B_{pw}}$ | System matrixes of continuous model for pulse-width-regulated SPRC | |
| $\boldsymbol{A_{d,pw}, B_{d,pw}}$ | System matrixes of discrete model for pulse-width-regulated SPRC | |
| $A, A_n$ | The amplitude of saw-tooth signal in modulator | |
| $C_f$ | Capacitor in output filter | F |
| $C_p$ | Parallel capacitor | F |
| $C_s$ | Series capacitor | F |
| $D, D_p$ | Duty ratio, extra duty ratio for time compensation | |
| $D_{nom}$ | Normalized duty ratio | |
| $D_{real}$ | Real effective duty ratio in the modulation | |
| $D_1, D_2, D_3, D_4$ | Reverse parallel diodes of full bridge circuit of SPRC-LC | |
| $D_5, D_6, D_7, D_8$ | Rectifier diodes in secondary side of SPRC-LC | |
| $\boldsymbol{E}$ | Identity matrix | |
| $F_{uCp,a}$ | Average coefficient of parallel-capacitor voltage | |
| $F_{uCp,s}$ | Sine coefficient of parallel-capacitor voltage | |
| $F_{uCp,c}$ | Cosine coefficient of parallel-capacitor voltage | |
| $f_s$ | Switching frequency | Hz |
| $i_{Lf}, I_{Lf}$ | Current through output filter inductor | A |
| $i_{Ls}, I_{Ls}$ | Current through series inductor, amplitude of series inductor current | A |
| $\Delta i_{Ls}$ | Unbalanced part of resonant current | A |
| $i_{out}$ | Output current | A |
| $i_R$ | Rectifier current | A |
| $K_{p,d}, K_{i,d}$ | Discrete control parameters | |
| $L_s$ | Series inductor in resonant tank | H |
| $L_f$ | Inductor in output filter | H |
| $P_w$ | Pulse-width signal | s |
| $r$ | Current ratio, $I_{Lf}/I_{Ls}$ | |
| $R_L$ | Load resistance | Ω |
| $s, s_n$ | Slope of saw-tooth signal in the modulator | 1/s |
| $t_h, t_{h,n}$ | length of half cycle | s |
| $T_1, T_2, T_3, T_4$ $(T_n)$ | Gate signals of transistors or the transistors | |
| $U_{out}, u_{out}$ | Output voltage | V |
| $U_{dc}, u_{dc}$ | Input voltage, direct current (DC) voltage | V |

| | | |
|---|---|---|
| $u_{Cs}$, $U_{Cs}$ | Voltage on series capacitor, amplitude of series capacitor voltage | V |
| $u_{Cp}$ | Voltage on parallel capacitor | V |
| $u_{Cf}$ ,$U_{Cf}$ | Voltage on output filter capacitor | V |
| $u_{ref}$ | Reference of output voltage | V |
| $\omega$ | Angular switching frequency | rad/s |
| $\boldsymbol{x}$, $\boldsymbol{y}$, $\boldsymbol{u}$ | State variables of linear models | |
| $Z_{ac}$ , $Z_{equ}$ | AC equivalent impedance of secondary side | Ω |

# Contents

**Contents**

# 1 Introduction

DC-DC converters with isolation are becoming more and more popular due to the rapid development of their present applications in electric power applications. At the same time, new fields of DC-DC applications appear in renewable energy harvesting, fuel-cell application and power management. In isolated DC-DC converter topologies, the phase-shifted full bridge (PSFB) is still the first choice in medium and high power application. Because of the potentially smaller switching losses, resonant converters are becoming more and more attractive beside the PSFB. Because resonant converters enable soft-switching conditions for the transistors, the switching frequencies are normally higher than the PSFB with the same efficiency requirements. Due to their higher switching frequencies, resonant converters achieve advantages in output filter volume and dynamic performance. Thus, resonant converters show the potential to replace the PSFB in medium and high power DC-DC isolated applications, for their smaller switching losses, higher power density and faster dynamics. [Cao14]

Series-resonant converters (SRC), parallel-resonant converters (PRC) and series-parallel-resonant converters (SPRC) are the most common circuits among the resonant converter topologies. The SPRC unites advantages of SRC and PRC, and abolishes their main disadvantages. The SPRC is allowed to be operated in a wide load range from full load to no load, whereas PRC regulation is lost at full load and SRC regulation is lost at light load. When wide operating ranges are required, the SPRC offers the best efficiency performance in the medium and high power range. Compared to the PSFB under the same efficiency and operation range requirement, higher power density and better dynamic performance can be achieved in SPRC [Bha90][Cao14][Fro91].

Until now, the SPRC has not yet been widely utilized in real isolated DC-DC applications. The major reason is its nonlinear gain and dynamic characteristics and its modelling complexity. The PSFB performs a linear characteristic in its continuous current mode, which is easy to understand and predict. Because of this linear characteristic, the control algorithm of the PSFB is simple and robust. Even in spite of its relative high switching losses, PSFB is still the preferred choice for many industry applications.

Compared to PSFB, the modelling techniques and controller design for the SPRC pose a series of challenges. The state-of-the-art modelling techniques of the SPRC can be divided into two categories. One category of modelling techniques, including fundamental AC analysis [Ste88] and extended describing function model [YLJ92], is simple but has a poor accuracy, especially at heavy load condition. The other category, including sampled-data analysis and time-domain analysis [VEK86], is accurate but complex to derive and calculate. The SPRC is suitable for being operated in a wide load range, but modelling techniques do not show sufficient accuracy at heavy load condition [FWM03]. If high accuracy in wide load range and output-voltage range is required, the modelling techniques for the SPRC normally become too complicated to calculate and implement. These modelling approaches involve groups of numerical solutions and consume a lot of computation resources. The complexity of SPRC modelling approaches also impedes the development of its controller algorithm. The major state-of-the-art control algorithm is gain-scheduling proportional-integral control. The application of an advanced control structure depends on further development of simple and accurate modelling techniques.

Due to the development of digital devices, e.g. field programmable gate array (FPGA) and complex programmable logic device (CPLD), appropriately designed algorithms with certain complexity can be implemented in these devices, calculating the model in real-time. This technique is mainly used in hardware-in-the-loop (HIL) simulation, as an objective for

verifying the controller. The development of these real-time algorithms also spurs some complex control ideas, like model-predictive controls. State-of-the-art modelling techniques with sufficient accuracy in wide range (sampled-data or time-domain method) are too complex to be implemented in these digital devices. This is mainly because several transcendental differential equations are substance of these SPRC models. Until now, these modelling approaches are used for computer-aided analysis and computer-aided design in practice, which are calculated by numerical solution methods in high-end computers with practically infinite calculation capabilities. The calculation requirements of these modelling approaches are clearly beyond the capability of present digital devices. This is another motivation for developing novel modelling and control algorithms for the SPRC. By reducing the complexity of algorithms, the SPRC model can be transplanted to FPGAs for real-time simulation.

Due to these problems, this dissertation focuses on the discussion of modelling and control algorithms for the SPRC. Finding an appropriate algorithm with relatively low computation complexity and sufficient accuracy for the SPRC is the main objective of this dissertation. Main questions about modelling and control algorithm for SPRC are listed below:

- Is it possible to model the SPRC without involving numerical solutions?
- What is the best compromise between model complexity and accuracy?
- How does the novel modelling algorithm support the control design?
- How can the dynamic performance of SPRC be improved with the advanced control design?

In order to answer these questions, a new idea about modelling techniques for resonant converter is proposed, called the half-cycle-sampled discrete (HSD) system. In Chapter 2, the principle idea of the HSD system is introduced. Improved steady-state analysis of the SPRC

considering the voltage distortion is proposed in Chapter 3. The modelling algorithm cleverly avoids numerical solutions in the calculation process and simplifies the calculation procedure. By combining Forsyth's steady-state model [FWM03] and HSD model, a novel discrete dynamic model for the SPRC with optimized modulation is presented in Chapter 4. The modulation and control strategies of SPRC are discussed utilizing the novel HSD idea to answer the third question. These modulation strategies are introduced and implemented in Chapter 5. These strategies are also modelled in the discrete system to describe their dynamic behaviour. The HSD principle is also applied in the controller design, using synchronized varying-step controller instead of the fixed-step controller. In Chapter 6, these novel controllers are introduced and implemented to improve the dynamic performance of the system. In Chapter 7, a calculation system of the SPRC is introduced based on the HSD system. The novel calculation system simulates the dynamic process of SPRC system. The experimental setup of SPRC hardware is also presented in Chapter 7. Finally, a conclusion and outlook are given in Chapter 8.

# 2 The principal idea of half-cycle sampled system

In order to find a low-calculation-cost modelling algorithm for the SPRC, a novel modelling technique for the SPRC is proposed in this chapter. Due to the sampling characteristic of the modulation strategy, the general idea of novel system, called half-cycle sampling, is generated. As the SPRC has a similar waveform in each half period of the switching cycle, the sampling step is selected as the same as the length of each half cycle. Utilizing this varying-step sampling, the entire system of the SPRC is converted to a half-cycle-sampled discrete system (HSD system). This novel sampling leads to a novel varying-step sampled model of SPRC, called HSD model. This discrete model will be briefly introduced in this chapter and introduced in detail in chapter 4.

This chapter includes 5 sections. First, the entire system of the SPRC is designed and introduced, including SPRC topology and its control circuit. The circuit design and operation modes of the SPRC are presented in Section 2.1. SPRC has a number of options in its design process, including the selection of switching frequency, filter topology and modulation strategies. There are three major modulation strategies for the SPRC, which are introduced and selected in Section 2.2. The principal idea of HSD method is proposed and introduced in Section 2.3. As a varying-step sampled system, the general modelling procedures from electrical circuits to the HSD models are introduced in Section 2.4. Finally, a short summary of the novel HSD idea is given in Section 2.5.

## 2.1 Designing choices of series-parallel-resonant converter

As the growth of series-parallel-resonant converters (SPRC) utilization, the design of SPRC system becomes mature during time. The SPRC has three major options in its design process, including the selection of switching frequency, filter topology and modulation strategies. Compared to PSFB and other resonant converters, SPRC shows its advantage in efficiency and operation range. Thus, the SPRC is mainly designed for two specifications in this dissertation: wide operation range and fast dynamic performance. Following this specifications, SPRC is designed with two options below.

First, the category of SPRC topologies can be separated by the type of its output filter, as with capacitive filter (SPRC-C) and with inductor-capacitive filter (SPRC-LC). SPRC-C has better output performance when high quality of output voltage is required [Cav06]. In order to achieve high control dynamics while retaining small output voltage and current ripples, inductor-capacitive filter as a higher-order filter performs better than single capacitive filter. [Cao14]

Second, SPRC can also be operated at sub-resonant mode or super-resonant mode, with the switching frequency below or above the resonant point. A super-resonant converter is selected because of its elimination of the reverse-recovery losses on the freewheeling diodes [Cao14].

Therefore, a super-resonant SPRC-LC is selected in this dissertation because it performs the better efficiency (no reverse-recovery losses) and potential high dynamics (LC filter) [Cao14]. The circuit diagram of the super-resonant SPRC-LC is illustrated in Figure 2.1. The SPRC circuit is composed of full-bridge inverter, resonant components, transformer, rectifier and output filter. Considering it as a black box in the control system, the four gate signals for the

transistors are the input Boolean signals ($T_n$, $n$ = 1, 2, 3, 4) while the output voltage ($U_{out,r}$) is the output signal of this converter.

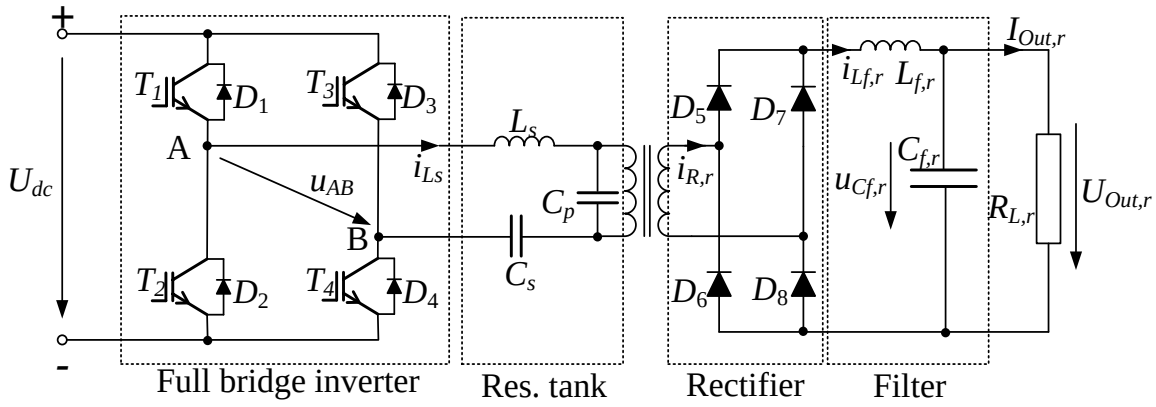



Figure 2.1: Schematics and major components of a series-parallel-resonant converter

To regulate the output voltage, the control structure of SPRC is normally divided into the controller, the modulator and the converter. An example of SPRC control structure is illustrated in Figure 2.2. In this dissertation, the output voltage is the only control objective for the different control algorithms. The reference value $u_{ref}$ is given, while the output voltage $u_{out}$ is the feedback signal from the converter. The controller determines the control signals with its control algorithm, as duty ratio $D$ in the figure. The modulator converts the control signals into corresponding gate signals ($T_n$, $n$ =1, 2, 3, 4) and sends them to the transistors.

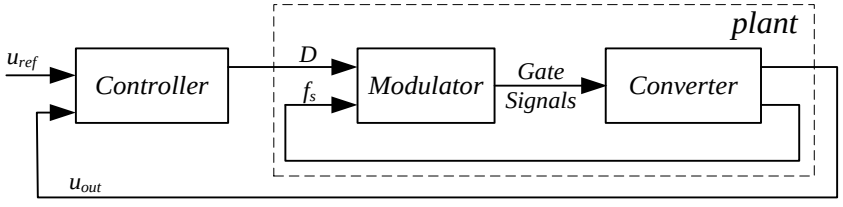



Figure 2.2: Basic block structure of SPRC system

## 2.2 Introduction of three different modulation strategies

According to previously published works [YP04+], there are several optional modulation and control strategies for the SPRC-LC topology. Because of the conduction condition of full-bridge inverter, the modulation behaviour can be simplified as generating a square waveform ($u_{AB}$) with positive, negative and zero values of input DC voltage ($U_{dc}$).

Normally, the switching frequency is the only controlled variable in the system, while the duty ratio is constant to unity. This modulation strategy is called pulse frequency modulation (PFM), as illustrated in Figure 2.3(a). At different switching frequencies, the phase difference between $i_{Ls}$ and $u_{AB}$ varies. It is the most widely applied modulation strategy for resonant converters. However, the converter operated with PFM has two hard switching-off transients in every switching cycle. If a wide operation range is required, the switching frequency also varies in a wide range. Because the design of transistors and magnetic cores are depending on the highest frequency, it introduces some additional challenges in design process. Thus, PFM is not suitable for wide operation range application.

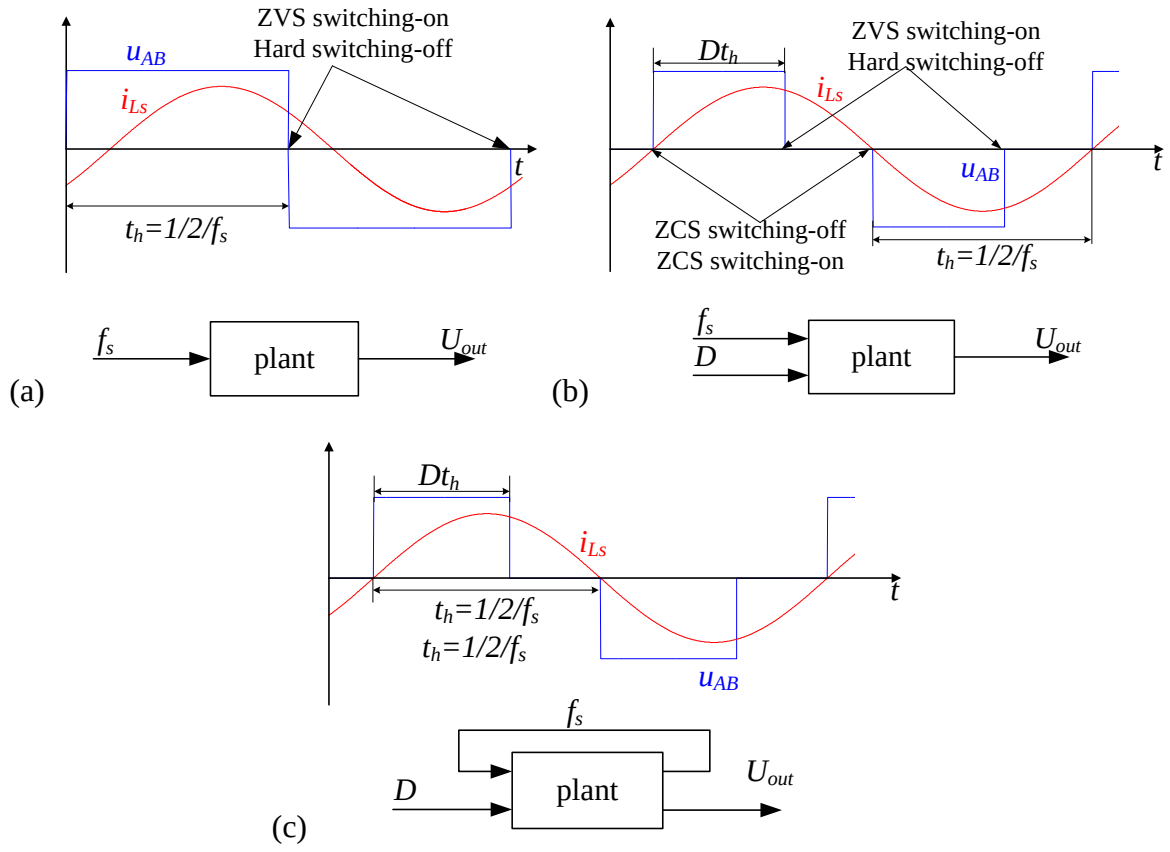



Figure 2.3: Comparison of modulation strategies, (a) PFM (b) PFWM (c) OM

In order to avoid this problem, the duty ratio can also be controlled in the system [Aig05]. As illustrated in Figure 2.3(b), the modulation strategy acting on both switching frequency and duty ratio is called pulse frequency and width modulation (PFWM). PFWM reduces the switching frequency variation in a wide operating range due to the additional duty-ratio regulation. It can achieve zero-voltage switching (ZVS) in one leg and zero current switching-off and switching-on (ZCS) in the other, if the load condition is appropriate. PFWM is suitable for wide operation range because of the relatively small frequency variation.

If the ZCS condition needs to be guaranteed in PFWM, the switching frequency has a nonlinear relationship with the duty ratio. Each switching frequency has a corresponding duty ratio at certain operating point. This relationship mainly depends on the circuit parameters of

the resonant tank and is sensitive to the parasitic components. In practice, the controller does not have the capability to predict the relationship because complicated calculation is required.

In order to avoid these complex calculations in the control algorithm, Pinheiro proposed a novel modulation strategy in 1999, called self-sustained oscillating control (SSOC) [PJJ99]. Instead of directly controlling switching frequency, SSOC measures and utilizes the resonant current as the synchronizing signal in modulation. The modulator is operated and reset synchronously by the resonant current, which contains the information of switching frequency. The control structure of this modulation can be approximately considered as an internal feedback of switching frequency.

Although in [PJJ99] SSOC modulation is mainly designed for PFM, it can also be applied to the PFWM strategy. In this dissertation, the modulation strategy combined with PFWM and SSOC is called optimized modulation (OM). Once the duty ratio is adjusted in OM, the switching frequency is automatically adapted by the feedback loop, as illustrated in Figure 2.3(c). ZVS and ZCS conditions are automatically guaranteed even in a wide operation range. OM inherits the high efficiency and narrow frequency variation from PFWM and the modulation is more convenient to implement. It is obviously the best modulation strategy for the SPRC with wide operation range requirement

## 2.3 General thoughts about half-cycle sampled discrete system

The details and the implementations of a real OM strategy will be introduced in Chapter 4. In order to explain the half-cycle sampled thoughts in this section, Figure 2.4 gives the major waveforms of SPRC-LC operated by OM (SPRC-LC-OM).

From top to bottom, the waveforms depict resonant current $i_{Ls}$, saw-tooth signal with duty ratio and output voltage of full-bridge inverter $u_{AB}$. The modulation strategy can simply be expressed by three steps. First, the modulator generates the synchronized saw-tooth

waveform. The saw-tooth signals are reset at the zero-crossing point of resonant current $i_{Ls}$. Second, the duty-ratio signal is compared to the saw-tooth waveform to decide the pulse width of $u_{AB}$. Third, voltage $u_{AB}$ is generated with the desired pulse width and the direction of $i_{Ls}$.

In Figure 2.4, the switching frequency is increasing It is observed that the waveforms $i_{Ls}$ , $u_{AB}$ and saw-tooth signals have similar shapes in different half cycles, even with different switching frequencies. The waveforms $i_{Ls}$ and $u_{AB}$ in odd half cycles are inversely symmetrical to the waveforms in the even half cycles. Considering this symmetric characteristic, the waveforms $|i_{Ls}|$ , $|u_{AB}|$ and saw-tooth signals are periodic waveforms in the half cycle. Half-cycle periods can be considered as the minimum analysis unit in the time-domain. It is also interesting to point out that only one value of duty ratio is active in every time unit, as shown in the figure. It can be considered as sampling with varying step in every half cycle.

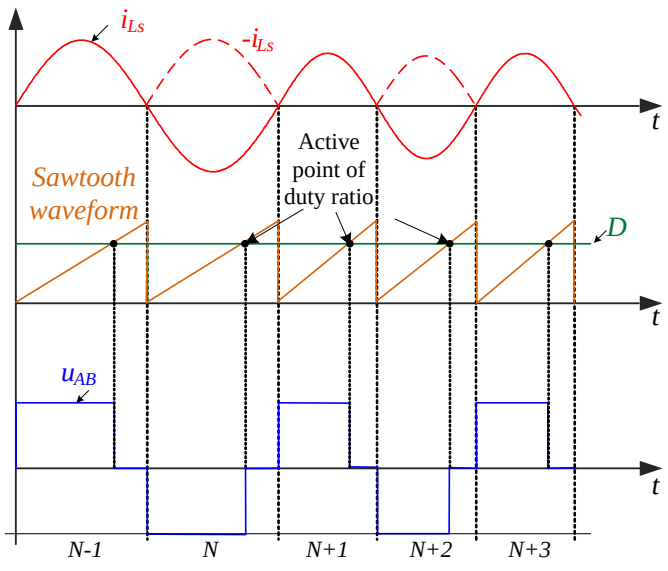
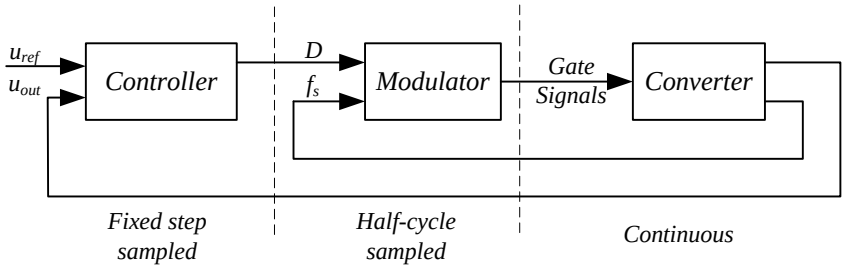


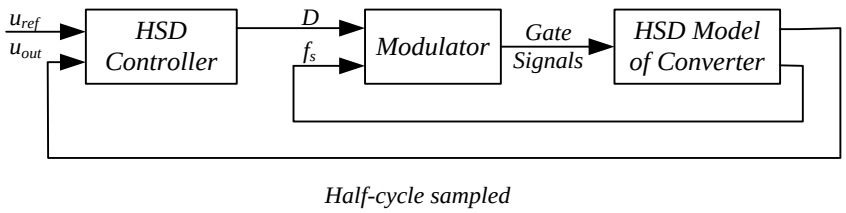

Figure 2.4: Synchronicity of major waveforms and half cycle sampling characteristic in optimized modulation

In state-of-the-art control systems of SPRC, there are normally three different sampling times. Although some of these modelling techniques [YLJ92] [CNT+12] analyse the model with half-cycle sampling period in derivation, almost all the published works [Ste88] [PJJ99] [YLJ92] [CNT+12] [YPJ04] of modelling techniques assume that the SPRC converter is a continuous system. Second, the modulator samples the control signals synchronously with the resonant current $i_{Ls}$ as the analysis mentioned above. The control signal in OM and SSOC is sampled with half cycle. Third, the controller, normally digital and discrete, has another fixed sampling step, e.g. 20 kHz in the control system. Figure 2.5(a) illustrates the different sampling steps in the SPRC-LC-OM system.

The characteristic of the modulator leads to a novel thought for modelling technique and control algorithm. Instead of the system with different sampling steps, the whole system should be created based on the same sampling step. The sampling step of SPRC system depends on the length of half-cycle. The entire system can be called "half-cycle-sampled discrete system" (HSD system). The structure of HSD system is illustrated in Figure 2.5 (b).




(a)




(b)

Figure 2.5: Three different sampling steps in original control system (a) and half-cycle sampled control system (b)

As illustrated in Figure 2.5, the HSD system comprises of the novel half-cycle-sampling discrete controller (HSD controller), the modulator and the novel half-cycle-sampling discrete model of SPRC-LC (HSD model). This dissertation will be organized with these three blocks. The HSD model will be introduced in Chapter 3 and Chapter 4. The modulator will be introduced and implemented in Chapter 5. The HSD controller will be designed and implemented in Chapter 6.

Generally speaking, HSD model with half-cycle sampling eliminates the frequency higher than switching frequency. This is a conclusion of Nyquist–Shannon sampling theorem. In real converter, the output filter is designed as a low-pass filter for eliminating the voltage and current ripples. High-frequency signals are blocked in the output filter and have almost no effect at the output side in real converter. Therefore, a HSD model of SPRC can perform an accurate average result and an inaccurate ripple result in theory.

Beside the accuracy of average result, there are some obvious advantages of the HSD system. First, the HSD system makes the controller, modulator and converter to be operated synchronously. It brings some convience in control and protection, as well as the exception handling. The control structure of the SPRC system will be simplified because of its synchronicity. Second, in the aspect of variable expression, the HSD system gives the most compact expression of the SPRC system. It constricts the deduction process, simplifies the algorithm and reduces the cost of computation resources. Obviously, the HSD system gives a potential modelling technique with a good compromise between complexity and accuracy.

## 2.4 General method of half-cycle sampled discrete model

Among the three blocks of SPRC structure, the HSD modelling approach of SPRC is the most significant part in the HSD system. The converters comprise of electrical components in real hardware. The modelling approach from these components to a mathematical model is one of the emphases of this dissertation. The design of synchronized controller and modulator are dependent on this HSD model. A general method of HSD model is proposed in this section.

In control theory, the HSD model can be considered as a discrete system with varying sampling steps. There is complete knowledge and research about the analysis of a discrete system. The discrete domain control is also fully developed. Thus, the focus will be on the generation of HSD model with varying sampling steps. A general method for creating a HSD model is introduced in the following.

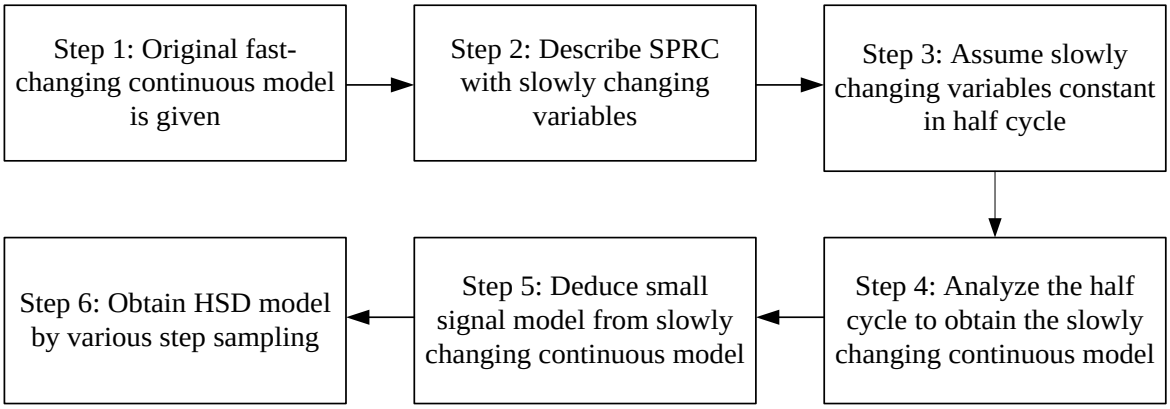



Figure 2.6: The modelling process of general HSD model method

There are six steps to derive the HSD model from the electrical circuit. First, the original fast-changing continuous model is given based on the characteristics of the passive components in the converter. The second step is describing the resonant state variables with slowly changing variables. Using the resonant current as an instance, it rapidly changes during the half cycle, from positive to negative. In order to assume this variable is constant in the third step, the

amplitude of resonant current $I_{Ls}$ is taken as the modelling variable instead. The amplitude of resonant current $I_{Ls}$ is relatively steady and changes slowly during several half cycles.

Third, assume these slowly changing variables as being constant in every half cycle. AC analysis can now be applied with this assumption. The slowly changing continuous model, also the large-signal model, can be derived in the fourth step, based on the analysis of the model. In the fifth step, the small-signal, or linear model is deduced from the slowly changing large-signal model by perturbation and linearization. In the sixth step, varying step sampling is applied in the large- and small-signal model, generating the linear and nonlinear HSD model.

An example of the sixth step is illustrated in the following. For a certain operating point, the linear or small-signal model of the SPRC-LC can be expressed by its system matrixes as

$$\frac{d\boldsymbol{x}}{dt} = \boldsymbol{Ax} + \boldsymbol{Bu} \tag{2.1}$$

$$\boldsymbol{y} = \boldsymbol{Cx} + \boldsymbol{Du} \tag{2.2}$$

The varying step sampling is applied on this model. The sampling step can be expressed as

$$t_s = t_h = \frac{1}{2f_s} = \frac{\pi}{\omega}$$

where $t_s$ and $t_h$ represent the sampling step and the time length of half cycle. $f_s$ represents the switching frequency and $\omega$ the angular switching frequency. If the Forward Euler Method is applied, the discrete model can be expressed by the discrete system matrixes as

$$\boldsymbol{x_{n+1}} = (\boldsymbol{E} + \frac{\boldsymbol{A}}{2f_{s,n}})\boldsymbol{x_n} + \frac{\boldsymbol{B}}{2f_{s,n}}\boldsymbol{u_n} \tag{2.3}$$

$$\boldsymbol{y_n} = \boldsymbol{Cx_n} + \boldsymbol{Du_n} \tag{2.4}$$

where $f_{s,n}$ is the varying switching frequency in the dynamic process and $\boldsymbol{E}$ represents the identity matrix. In state-of-the-art modelling techniques, the switching frequency $f_{s,n}$ is

considered as an input variable or a state variable in matrixes already. The HSD model does not introduce extra intermediate parameters into the system.

For the nonlinear model, the process of HSD modelling is similar. With different operation points, the nonlinear model can be linearized and can be described by an approximate linear model. Thus, the corresponding nonlinear discrete model can also be generated from the continuous large-signal model.

The HSD model is a general method for any modelling approach or any discretization methods. Different modelling techniques have different assumptions and calculation procedures in the fourth step. Different discretization methods lead to different expressions in the sixth step. Many published modelling approaches, e.g. [Ste88] [PJJ99] [YLJ92] [CNT+12] [YPJ04] have their corresponding discrete modelling approaches for the SPRC-LC topology. In these discrete approaches, the best compromise in regards of simplicity and accuracy will be discussed in the following two chapters.

## 2.5 Summary

In this chapter, the principal idea of the HSD system is introduced. The basic thoughts of HSD systems come from the investigation of modulation strategies. For a modulator applying SSOC and OM strategies, the sampling step of control signal is synchronized with the resonant current. In order to achieve synchronicity in the entire SPRC system, the same sampling step is applied for the converter model and the controller. Therefore, the whole SPRC system is expressed using the HSD system, including HSD model and HSD control. In this chapter, the advantages of this HSD system are analysed briefly. HSD system describes the dynamic behaviour of the SPRC and is relatively concise in the mathematical expression. HSD modelling method is considered as a potential balanced method between complexity and accuracy.

The general method of the HSD model is also introduced in this chapter. It involves the varying-step sampling of a continuous model. The stability of this discrete model is also addressed. The general method of the HSD model can be applied for any modelling approach for the SPRC with any discretization method. As there are many developed modelling approaches for SPRC topology, those offering the best compromise are discussed in the next two chapters.

# 3 Improved steady-state model of SPRC-LC considering the voltage distortion

The model of the resonant converter, as a nonlinear gain system, normally contains transcendental equations. The attempt to solve these equations costs many computation resources. These complex models have limited benefits because only high-performance computers can offer sufficient calculation capability and can thus be employed in analysis. In order to reduce the calculation complexity of the SPRC model to the digital devices level, a novel steady-state modelling technique will be proposed in this chapter.

In this chapter, the state-of-the-art modelling techniques for the SPRC-LC are first investigated in Section 3.1. Within the four state-of-the-art modelling categories, extended fundamental AC analysis, proposed by Forsyth, give a good balance between complexity and accuracy. It is selected as the basis for further development. To highlight the derivation, SPRC-LC circuit is simplified based on some assumptions, which will be presented in Section 3.2. Extended fundamental AC analysis will be introduced step by step in Section 3.3. Because of its drawbacks, improved steady-state analysis considering the voltage distortion is introduced in Section 3.4. Simulation and experimental validation of the novel steady-state analysis with PFWM are performed in Section 3.5. Finally, a short summary is given in section 3.6.

## 3.1 State-of-the-art modelling techniques of SPRC-LC

Resonant converters are characterized in general nonlinear gain and dynamic systems. The nonlinear gain characteristics cause the major difficulties when starting the design of its operation points. Treating this nonlinear gain characteristic, many contributions have been

published on the steady-state modelling techniques for the SPRC-LC, from the 1980s until now.

There are mainly four major categories of the modelling techniques: fundamental AC analysis, extended describing function model, extended fundamental AC analysis and sampled-data or time-domain analysis.

The fundamental AC analysis method was proposed in 1988 [Ste88]. It is widely utilized for operation range decision and first-step circuit design of resonant converters. The analysis method assumes all the voltage and current waveforms in the resonant tank to be ideally sinusoidal, including resonant current $i_{Ls}$, series-capacitor voltage $u_{Cs}$, and parallel-capacitor voltage $u_{Cp}$. The rectifier diodes ($D_n$, $n$ =5, 6, 7, 8) are considered as ideal switches, which transform the sinusoidal waveform of the parallel-capacitor voltage $u_{Cp}$ into its absolute value$|u_{Cp}|$. The output filter is considered sufficiently large, such that the average value of $|u_{Cp}|$ equals the output voltage $u_{out}$ in steady state. Hence, the load DC resistance is converted to an equivalent AC resistance, so that AC circuit analysis can be applied in the resonant tank. The DC voltage transfer ratio and the steady-state model are derived in [Ste88]. The small-signal model of fundamental AC analysis method is derived in [PJJ99].

Fundamental AC analysis is an approximate but simple method. It does not involve complicated mathematical calculations. One of the major problems of fundamental AC analysis is its accuracy at heavy-load condition. The parallel-capacitor voltage $u_{Cp}$ is distorted from sinusoidal waveform, which brings the deviation into the model.

Another modelling approach for resonant converters was proposed by Yang in [YLJ92] and [YLJ92+], called extended describing function model. The major method is to describe the resonant behaviour with slowly time-varying values. Again, it assumes that all the voltage and current waveforms of the resonant tank are ideally sinusoidal. Instead of the real state

variables, fundamental Fourier coefficients of resonant current $i_{Ls}$ and resonant voltages ($u_{Cs}$ and $u_{Cp}$), are utilized to describe the waveforms of the resonant-tank components. This approach yields an accurate small-signal model in the high-frequency range. At heavy load, this approach also leads to large deviations due to the distorted waveforms.

In order to solve the insufficiency at heavy load, Forsyth proposed another steady-state model for the SPRC-LC topology in [FWM03], called extended fundamental AC analysis. This analysis considers the distorted parallel-capacitor voltage $u_{Cp}$ as the integration result of its current. The resonant current $i_{Ls}$ and the series-capacitor voltage $u_{Cs}$ are still assumed as ideally sinusoidal waveforms. Due to the accurate description of parallel capacitor voltage $u_{Cp}$, extended fundamental AC analysis performs much better at heavy load. The corresponding small-signal model of extended fundamental AC analysis is first mentioned in [CNT+12]. The approach is easy to understand but mathematically relatively complex to be solved. It involves a series of transcendental equations each half cycle, for which numerical solutions are required and high calculation costs have to be paid.

Another modelling approach of SPRC-LC is sampled-data or time-domain analysis. Though with different expressions, the essence of time-domain analysis is the same as sampled-data analysis. Many impressing works have been published in this category, such as [VEK86], [YPJ04], [CTF+13], etc. Sampled-data analysis considers the resonant converter as a "switched control system". This comprises of several subsystems and switches between them depending on the switching strategies. The mathematical research in this field towards investigation of stability is still developing nowadays [DK01], [Mic06]. In practice, this method requires an explicit solution of differential equations, because the deviation will be cumulative during the calculation procedure. Due to the third-order resonant tank of the SPRC, sampled-data analysis needs 14 switching transients in SPRC-LC-OM [CTF+13].

Sampled-data analysis is calculated iteratively in dynamic processes, so large calculation resources are required.

The basic ideas of modelling techniques with their steady-state model and small-signal model are summarized in the following table. From top to bottom, model complexity is increasing, while accuracy of approach is also improved.

Table 3.1: The major modelling methods of SPRC

| Name | Major assumptions | Steady-state model | Small-signal model | Drawbacks |
|---|---|---|---|---|
| Fundamental AC analysis method | Ideally sinusoidal waveform in resonant tank | [Ste88] | [PJJ99] | Inaccuracy under heavy load |
| Extended describing model | Ideally sinusoidal waveform in resonant tank described by their amplitudes | [YLJ92] [YLJ92+] | | Inaccuracy under heavy load |
| Extended fundamental AC analysis | Distorted parallel capacitor voltage | [FWM03] | [CNT+12] | Transcendental equations in the model |
| Sampled-data analysis | Switched control system | [VEK86] [YPJ04] | | Requires an explicit numerical solution of differential equations |

There are also some other intuitive approaches to derive SPRC steady-state and small-signal model. The approximate method of Vorperian [Vor89] assumes that the dynamic behaviour of the SPRC is dominated by a single-pole transfer function in the middle frequency range. It is a good combination of accuracy and simplicity. However, this approach is an intuitive idea rather than a formal approximation.

The modelling techniques for different modulation strategies have also been developed during the progress of modulation strategies. Modelling approaches for PFM and PFWM have already been widely analysed in published works, e.g. [YLJ92+] and [FWM03]. For OM, however, only a time-domain modelling approach is presented in [CTF+13]. The major

difficulty encountered in SPRC-LC-OM modelling is the variation of switching frequency. Without constant switching frequency, AC analysis is not allowed to be applied in resonant-tank. Thus, the time-domain analysis is the only method available for SPRC-LC-OM. Because of the complexity of time-domain analysis, simpler modelling approaches with sufficient accuracy are required for further development of OM.

Among all these modelling techniques, the sampled-data or time-domain method is the most complex and the most accurate method, but extended fundamental AC analysis is relatively balanced between its complexity and accuracy. Considering the possibility of implementation in digital devices, extended fundamental AC analysis is selected as the basic analysis method in this chapter. In Section 3.3, the modelling details of extended fundamental AC analysis are introduced.

## 3.2 Major assumptions and simplification of SPRC-LC topology

Before establishment of the SPRC model, some major assumptions are made in order to simplify the modelling process. First, all components, including the transistors, diodes, capacitors and inductors, are assumed ideal without any losses. The input DC voltage $u_{dc}$ is considered constant without voltage ripples. The internal resistance is neglected. The transformer is regarded as ideal and the windings are perfectly coupled.

The topology of converter is simplified as Figure 3.1. All quantities in the secondary side of transformer are referred to the primary side. In this dissertation, the primary side equivalent quantities are dominantly mentioned. In order to make the expression clear, the real parameters of the secondary side components are expressed with the subscript ‘r’. The

parameters of the primary side equivalent component are expressed directly.

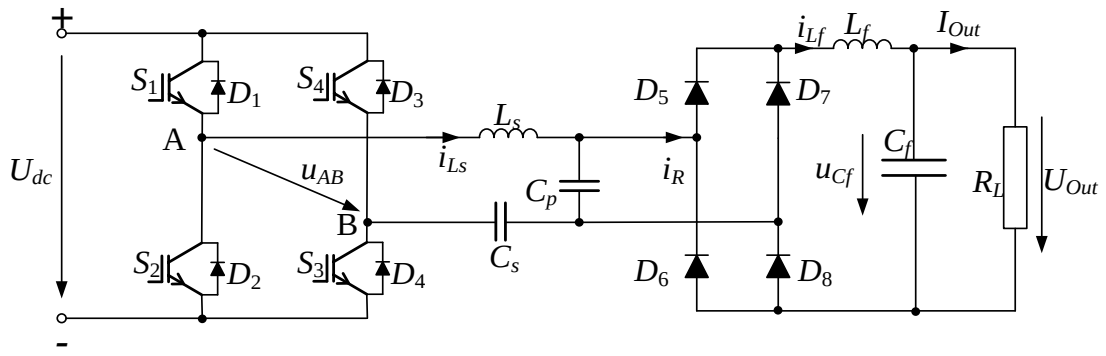



Figure 3.1: Simplified topology of SPRC-LC

In order to clarify the modelling method and its features, several small-value components in the power circuit are ignored. The parasitic resistance and inductance of the filter capacitor, the series resistance of filter inductor and resonant inductor and the equivalent conduction resistance of transistors and diodes are examples in the SPRC circuit. Part of these small-value components are the source of power losses in the circuit. Though they have certain effects on the output voltage, small-value and parasitic components are ignored in order to pursue the most simplified system in the analytical study. For further development of practical modelling techniques, these components can be taken into consideration in the future.

## 3.3 Extended fundamental AC analysis

As the basic method of novel modelling technique, Forsyth's extended fundamental AC analysis [FWM03] is introduced first. Extended fundamental AC analysis is suitable for the SPRC with constant switching frequency, taking the distorted parallel capacitor voltage into consideration.

The basic principle of extended fundamental AC analysis is converting the SPRC-LC topology into a simplified equivalent AC circuit, as illustrated in Figure 3.2. There are two

steps in the circuit conversion. The first step converts the full-bridge inverter circuit and the DC voltage source into an equivalent AC voltage source. Due to the band-pass characteristic of the resonant tank, the fundamental-frequency harmonic $u_{AB[1]}$ approximates the output voltage of the full-bridge inverter $u_{AB}$. The second step converts parallel capacitor, rectifier, filter and the load into an equivalent impedance $Z_{ac}(R_L)$, which is dependent on the load resistance.

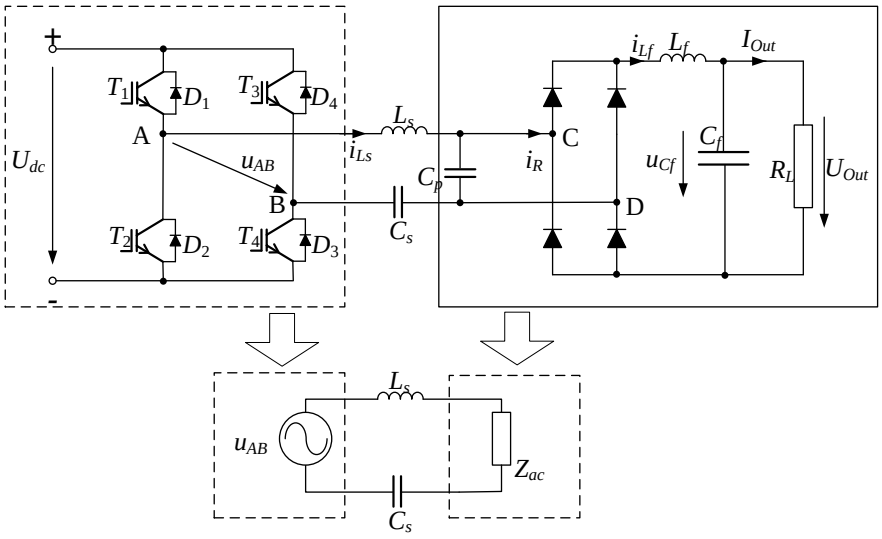



Figure 3.2: Circuit conversion of SPRC in extended fundamental AC analysis

In the equivalent circuit, AC circuit analysis can be applied. Series capacitor and series inductor are considered as a corresponding impedance. The resonant current $i_{Ls}$ can be expressed as

$$I_{Ls} = \frac{U_{AB[1]}}{\left| j\omega L_s + \frac{1}{j\omega C_s} + Z_{ac} \right|} \tag{3.1}$$

With the explicit value of the resonant current $i_{Ls}$, all the related voltage values ($u_{Ls}$, $u_{Cs}$ and $u_{Zac}$) in the resonant tank can be calculated. Therefore, the significant point of this model lies in the estimation of equivalent impedance $Z_{ac}$. In order to derive a correct equivalent impedance $Z_{ac}$, circuit analysis is applied to the rectifier and the parallel capacitor.

### 3.3.1 Circuit analysis of rectifier

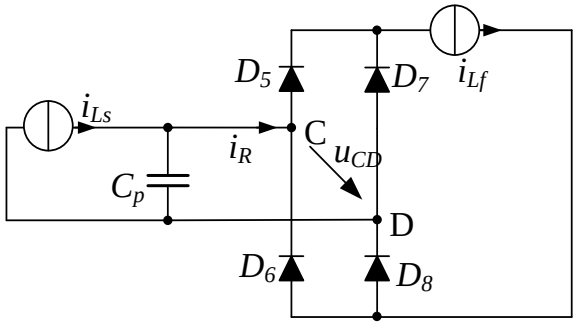



Figure 3.3: Equivalent circuit of rectifier in SPRC

Figure 3.3 illustrates the equivalent circuit of rectifier and parallel capacitor in the SPRC. In steady state, the resonant current and the filter-inductor current are modelled as a corresponding current source. Assuming the resonant current is sinusoidal, $i_{Ls}(t) = I_{Ls}sin(\omega t)$, and output inductor current has no ripple $i_{Lf}(t) = I_{Lf}$, the conduction states of diodes are decided by the value of both currents. In order to avoid the series connection of two unequal current sources, the DC current source is sometimes considered as an inductor.

Because of the symmetry of the resonant waveform, the circuit analysis in half switching cycle is sufficient. The half cycle with positive resonant current( $i_{Ls} > 0$ ) is analysed for the instance. The conduction conditions of the rectifier are listed in the table below and are illustrated in Figure 3.4.

Table 3.2: Conduction conditions of rectifier ($\boldsymbol{i_{Ls} > 0}$)

| **Condition No.** | $\boldsymbol{u_{Cp}}$ | $\boldsymbol{\lvert i_{Ls}\rvert - i_{Lf}}$ | **Diode action** | $\boldsymbol{i_R}$ |
|---|---|---|---|---|
| 1 | >0 | >0 | $D_5$, $D_8$ ON, $D_6$,$D_7$ OFF | $i_{Lf}$ |
| 2 | <0 | >0 | $D_6$,$D_7$ ON, $D_5$,$D_8$ OFF | $-i_{Lf}$ |
| 3 | >0 | <0 | $D_5$, $D_6$,$D_7$,$D_8$ ON | $i_{Ls}$ |
| 4 | <0 | <0 | $D_6$,$D_7$ ON $D_5$,$D_8$ OFF | $-i_{Lf}$ |

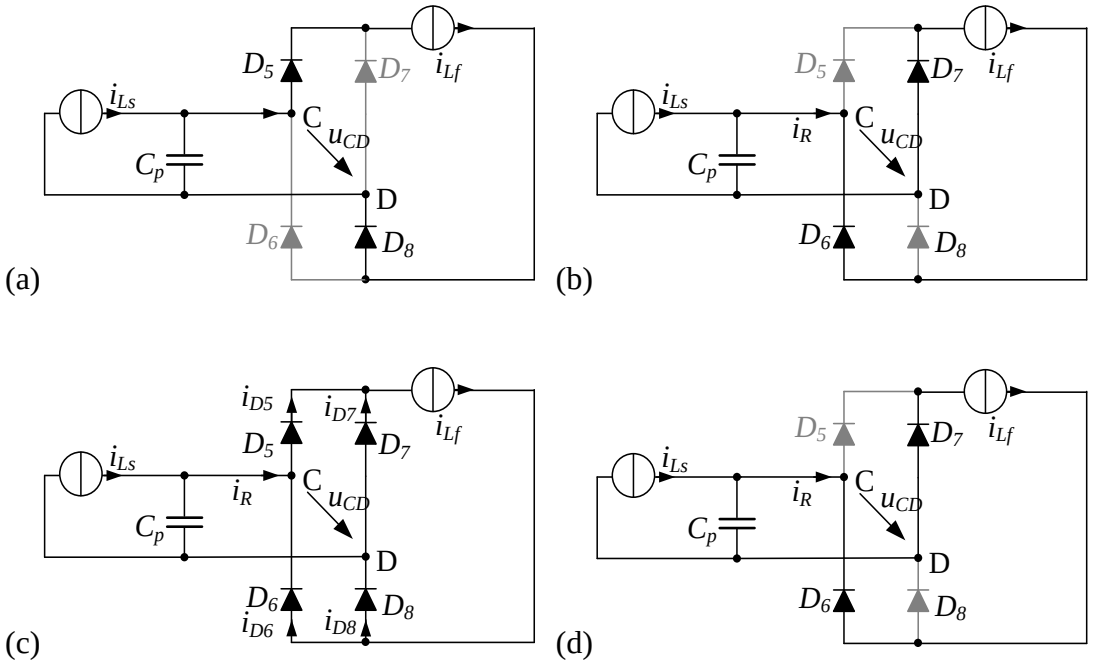



Figure 3.4: Rectifier in different conduction conditions, (a) condition 1 (b) condition 2 (c) condition 3 (d) condition 4

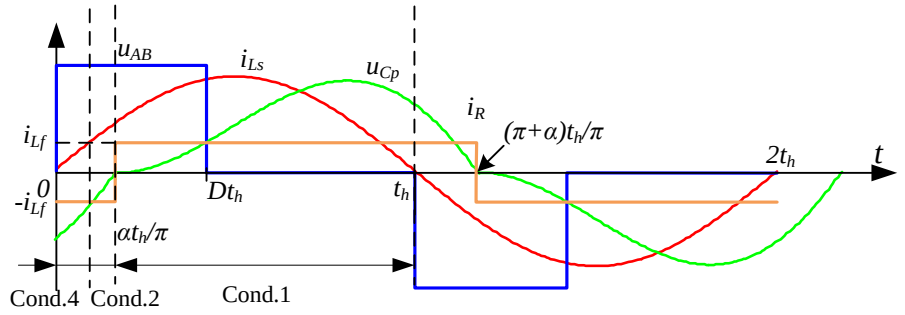
Three conduction conditions of the rectifier, condition 1, 2 and 4, are common with two conducting diodes and the other two blocking diodes. Only in condition 3, the currents are distributed over all four diodes. Because the resonant current is smaller than the filter inductor current $|i_{Ls}| - i_{Lf}$<0, part of the diode current comes from the resonant current ($|i_{Ls}|$), and part is straight free-wheeling through the rectifier ($i_{Lf} - |i_{Ls}|$). The current in each diode is expressed as,

$$i_{D5} = i_{D8} = \frac{\left(|i_{Ls}| + i_{Lf}\right)}{2} \tag{3.2}$$

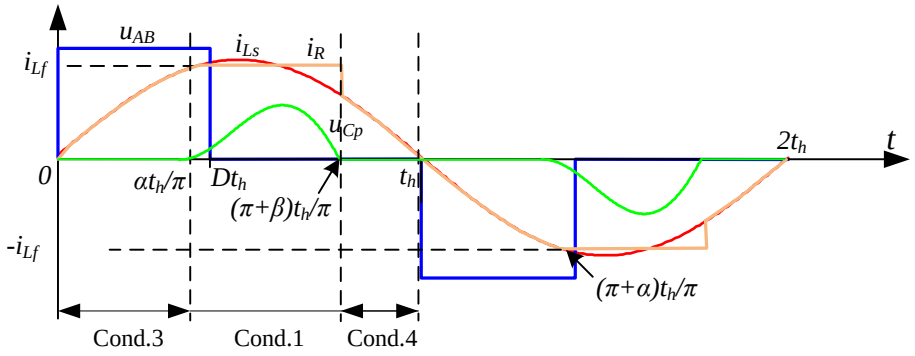
$$i_{D6} = i_{D7} = \frac{\left(-|i_{Ls}| + i_{Lf}\right)}{2} \tag{3.3}$$

The rectifier sink current $i_R$ equals the resonant current $|i_{Ls}|$ in condition 3.

### 3.3.2 Steady-state analysis of extended fundamental AC model




(a)




(b)

Figure 3.5: Typical waveform of $u_{AB}$, $u_{Cp}$, $i_R$ and $i_{Ls}$ in SPRC-OM

Based on the circuit analysis, the steady-state waveform of the SPRC converter can be drawn, as illustrated in Figure 3.5. There are two important instants in the SPRC waveforms: the instant when $|i_{Ls}(t)|$ equals $i_{Lf}(t)$ and the instant when $u_{Cp}(t)$ equals 0. If $u_{Cp}(t) = 0$ occurs after $|i_{Ls}(t)| = i_{Lf}(t)$, the waveform is illustrated as Figure 3.5 (a). If $u_{Cp}(t) = 0$ occurs before $|i_{Ls}(t)| = i_{Lf}(t)$, the waveform is illustrated as Figure 3.5 (b). In these waveforms, the four different rectifier conditions appear as mentioned in the previous section. Based on the continuity of the $u_{Cp}$ waveform or the appearance of condition 3 or condition 2, the operation mode can be divided into continuous voltage mode (CVM) and discontinuous voltage mode (DVM). In DVM, condition 3 appears in circuit analysis, which changes the shape of rectifier current $i_R$. In Figure 3.5 (b), the changed waveform of rectifier current $i_R$ is clearly illustrated.

Both CVM and DVM waveforms can be described by mathematical functions depending on time in a half cycle. Assuming sinusoidal waveform, the resonant current is expressed as

$$i_{Ls}(t) = I_{Ls} sin(\omega t) \tag{3.4}$$

The parallel-capacitor voltage $u_{Cp}$ in half cycle is the result of the integration of the current difference, which can be expressed as

$$u_{Cp}(t) = u_{Cp}(0) + \int_0^t (I_{Ls} sin(\omega\tau) - i_R) d\tau \tag{3.5}$$

Because of the waveform symmetry, the description of waveform in a half cycle is sufficient. In the phase range $0 < \omega t < \pi$, the diode current $i_R$ can be described in CVM as

$$i_R(t) = \begin{cases} -I_{Lf}, & 0 < \omega t < \alpha \\ I_{Lf}, & \alpha < \omega t < \pi \end{cases} \tag{3.6}$$

and in DVM as

$$i_R(t) = \begin{cases} -I_{Lf}, 0 < \omega t < \beta \\ I_{Ls}, \beta < \omega t < \alpha \\ I_{Lf}, \alpha < \omega t < \pi \end{cases} \tag{3.7}$$

In this dissertation, the definition of $\alpha$ and $\beta$ is different from the original paper [FWM03], because there is some further development of large-signal model in Chapter 4. The angle $\alpha$ is defined as the angle when the voltage $u_{Cp}(t)$ leaves the zero point and becomes positive in the first half cycle. Due to the symmetric characteristic of the waveform, the voltage $u_{Cp}(t)$ becomes negative at the angle $\pi + \alpha$ in second half cycle in steady state. The angle is given the name "leaving angle", marking the instant when $u_{Cp}(t)$ leaves the x-axis. The angle $\beta$ is defined as the angle when the voltage $u_{Cp}(t)$ returns to zero, called "returning angle". In CVM mode, $\beta = \alpha$. In order to simplify the expression, the calculation phase window is moved from time range $0 < \omega t < \pi$ to $\alpha < \omega$. In the novel phase windows, the expressions of rectifier current $i_R$ are expressed as

$$i_R(t) = I_{Lf} = I_{out}, \qquad \alpha < \omega t < \pi + \alpha \tag{3.8}$$

in CVM and

$$i_R(t) = \begin{cases} I_{Lf}, & \alpha < \omega t < \pi + \beta \\ -I_{Ls}, & \pi + \beta < \omega t < \pi + \alpha \end{cases} \tag{3.9}$$

in DVM. Inserting (3.8) and (3.9) into (3.5) gives

$$u_{Cp}(t) = \frac{I_{Ls}}{\omega C_p}(-cos(\omega t) - \omega t r + \alpha r + \cos(\alpha)), \qquad CVM \tag{3.10}$$

$$u_{Cp}(t) = \begin{cases} \frac{I_{Ls}}{\omega C_p}(-cos(\omega t) - \omega t r + \alpha r + \cos(\alpha)), & \alpha < \omega t < \pi + \beta \\ 0, & \pi + \beta < \omega t < \pi + \alpha \end{cases}, \qquad DVM \tag{3.11}$$

The ratio $r$ is defined as the quotient of the filter-inductor current divided by the amplitude of the resonant current.

$$r = \frac{I_{Lf}}{I_{Ls}} \tag{3.12}$$

**Continuous voltage mode (CVM)**

For the continuous voltage mode, $u_{Cp}$ falls to zero at the end of every half cycle $t = \pi + \alpha$. The expression for $\alpha$ is obtained by setting $u_{Cp}\left(\frac{\alpha+\pi}{\omega}\right) = 0$ and $u_{Cp}\left(\frac{\alpha}{\omega}\right) = 0$.

$$\alpha = \text{acos}\left(\frac{\pi r}{2}\right) \tag{3.13}$$

Although even with the correct expression in their text, the figures in [FWM03] and [Cao14] are somehow misleading. In CVM, the angle $\alpha$ does not equal to the value $asin(r)$. This means the waveform of $i_R(t)$ and $i_{Ls}(t)$ is not affected in the figure. As illustrated in Figure 3.5(a), there is a short period of rectifier conduction condition 2 in CVM mode.

An expression for the converter output voltage may be obtained by calculating the average value of the rectified parallel capacitor voltage $\overline{|u_{Cp}|}$. Integrating the equation (3.10) over half cycle gives the following

$$u_{out} = \overline{|u_{Cp}|} = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} u_{Cp}(t)d\omega t = \frac{2I_{Ls}sin(\alpha)}{\pi\omega C_p} \tag{3.14}$$

Set $u_{out} = i_{out}R_L$ in (3.14) where $R_L$ is the load resistance. It gives the fundamental frequency impedance $Z_{ac}$ in CVM. The expression gives,

$$Z_{ac} = \frac{1 - \frac{4}{\pi^2}(1 + cos2\alpha) + j\frac{4}{\pi^2}sin2\alpha}{j\omega C_p} \tag{3.15}$$

**Discontinuous voltage mode (DVM)**

For the discontinuous voltage mode, the first setting is $u_{Cp}\left(\frac{\pi+\beta}{\omega}\right) = 0$, giving

$$-cos(\pi + \beta) - \pi r - \beta r + \alpha r + \cos(\alpha) = 0 \tag{3.16}$$

Second, the average rectified voltage $\overline{|u_{Cp}|}$ is expressed as

$$\overline{|u_{Cp}|} = u_{out} = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} u_{Cp}(t)d\omega t = \frac{1}{\pi}\int_{\alpha}^{\pi+\beta} u_{Cp}(t)d\omega t \tag{3.17}$$

Rearranging this equation, it gives

$$u_{out} = \frac{I_{Ls}}{\pi\omega C_p}\left(sin\alpha + sin\beta + \frac{\alpha^2}{2} - \frac{(\pi+\beta)^2}{2} + (\alpha r + \cos(\alpha))(\pi + \beta - \alpha)\right) \tag{3.18}$$

Inserting $u_{out} = i_{out}R_L$ and $sin\alpha = r$ into the equation yields

$$sin\alpha + sin\beta + \frac{\alpha^2}{2} - \frac{(\pi+\beta)^2}{2} + (\alpha r + \cos(\alpha))(\pi + \beta - \alpha) = \pi R_L r\omega C_p \tag{3.19}$$

The fundamental-frequency impedance $Z_{ac}$ is expressed as

$$Z_{ac} = \frac{1 - \frac{1}{2\pi}\left[2(\alpha - \beta) + je^{-2j\beta} - je^{-2j\alpha}\right] - \frac{2r}{\pi}(1 + e^{-j\alpha})}{j\omega C_p} \tag{3.20}$$

The solving procedure of extended fundamental AC analysis can be divided into four steps. The first step is to solve angles $\alpha$ and $\beta$ from the equations (3.13) in CVM, or (3.16) and (3.19) in DVM. With the explicit angle values, the fundamental-frequency impedance $Z_{ac}$ is calculated by (3.15) in CVM or (3.20) in DVM. Then, an AC analysis is applied to the

resonant tank to estimate the resonant current by (3.1). Finally, the output voltage is calculated with impedance $Z_{ac}$, resonant current, current ratio $r$ and load $R_L$ by (3.17).

Extended fundamental AC analysis is an accurate approach because of considering the distorted parallel-capacitor voltage. In CVM, the modelling calculation is simple. A major drawback of this approach is its dependence on the explicit numerical solution in DCM. Because equations (3.16) and (3.19) are transcendental functions, the only way to solve these equations is to calculate their numerical solutions. As the output voltage is sensitive to the angles $\alpha$ and $\beta$, explicit numerical solutions are required and thus large calculation resources are needed.

Because the load $R_L$ is also contained in the function of the equivalent AC impedance $Z_{ac}$, the output filter has to be ignored in the extended fundamental AC analysis. It is not a big problem for the steady-state analysis, but it brings some difficulty to extend the steady-state model towards a corresponding large-signal model.

## 3.4 Improved steady-state analysis for SPRC-LC

### 3.4.1 Equivalent circuit of SPRC-LC

Forsyth's analysis takes frequency analysis of the distorted parallel-capacitor voltage into consideration in SPRC-LC models firstly. However, the major problem of Forsyth's modelling technique is that numerical solutions are required and the output filter is eliminated. In order to deduce a more flexible and feasible steady-state model, an improved steady-state analysis is proposed.

Improved steady-state analysis does not focus on the equivalent fundamental-frequency impedance $Z_{ac}$ depending on the load resistance. Instead, the parallel-capacitor voltage $u_{Cp}$ is the most significant waveform in the converter. The distorted voltage $u_{Cp}$ performs as AC

voltage in the resonant tank, while its absolute value $|u_{Cp}|$ is considered as the DC voltage source for the filter circuit. The equivalent circuit of the SPRC is considered as two separated circuits, an AC circuit and a DC filter circuit, as illustrated in Figure 3.6.

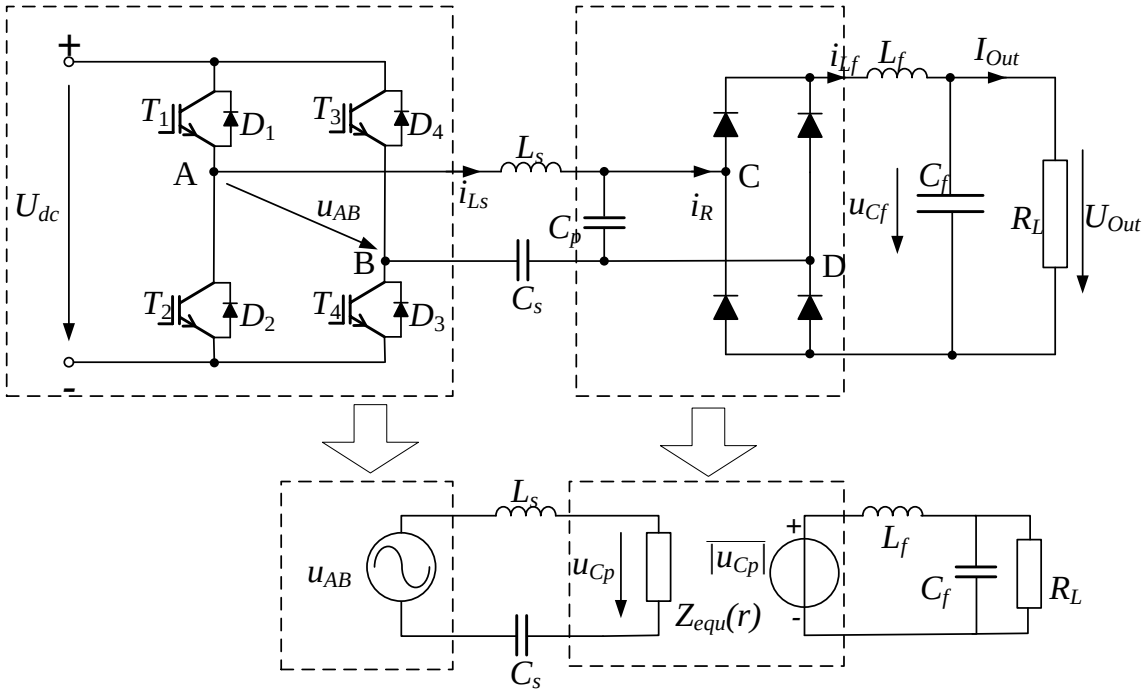



Figure 3.6: Circuit conversion of SPRC in improved steady-state analysis

The DC input source and full bridge are considered as an equivalent AC source $u_{AB}$. The parallel capacitor and diodes are replaced by an equivalent impedance $Z_{equ}\,(r)$ and corresponding DC source $\overline{|u_{Cp}|}$. These two equivalent components depend on the current ratio $r$. In the output filter and load circuit, the steady-state equation is described as

$$\overline{|u_{Cp}|} = u_{out} \tag{3.21}$$

Because of the band-pass characteristic of the resonant tank, the fundamental frequency waveform plays the significant role in the circuit. Similar to Extended Fundamental AC analysis, an AC analysis can be applied as,

$$I_{Ls} = \frac{U_{AB[1]}}{\left| j\omega L_s + \frac{1}{j\omega\, C_s} + Z_{equ} \right|} \tag{3.22}$$

The analysis of the distorted $u_{Cp}$ waveform, including its average value, is the most significant point for the improved steady-state model. In the mathematical expression, it is described by these two components, equivalent impedance $Z_{equ}(r)$ and corresponding DC source $\overline{|u_{Cp}|}$.

### 3.4.2 Description of parallel capacitor voltage

As illustrated in equation (3.10) and (3.11), the time-domain waveform of $u_{Cp}$ is expressed in the phase range $\alpha < \omega t < \pi + \alpha$ as following,

$$u_{Cp}(t) = \frac{I_{Ls}}{\omega C_p}(-cos(\omega t) - \omega t r + \alpha r + \cos(\alpha)), \qquad CVM \tag{3.23}$$

$$u_{Cp}(t) = \begin{cases} \frac{I_{Ls}}{\omega C_p}(-cos(\omega t) - \omega t r + \alpha r + \cos(\alpha)), & \alpha < \omega t < \pi + \beta \\ 0, & \pi + \beta < \omega t < \pi + \alpha \end{cases}, \qquad DVM \tag{3.24}$$

In order to analyse the shape of the waveform, the novel function $f(\theta, \alpha, r)$ is defined as the expression in the bracket in (3.23) and (3.24). The normalized function $f(\theta, \alpha, r)$ depends on only three independent parameters, $\theta$, $\alpha$ and $r$.

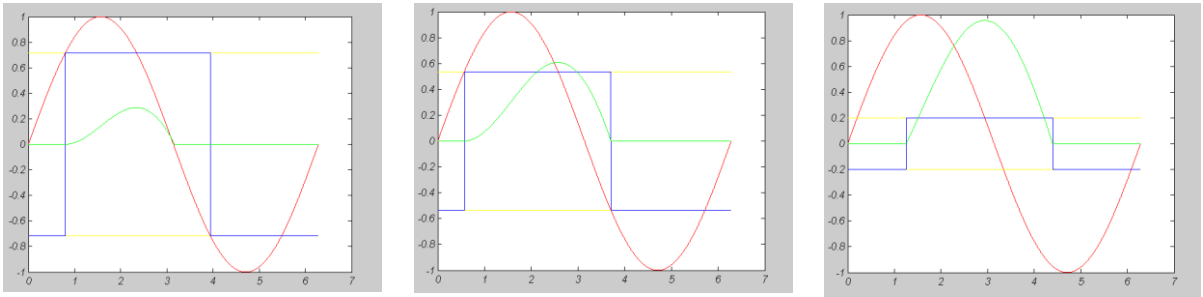
$$f(\theta, \alpha, r) = -\cos(\theta) - \theta r + \alpha r + \cos(\alpha), \ \alpha < \omega t < \pi + \alpha, \ CVM$$
$$f(\theta, \alpha, r) = \begin{cases} -cos(\omega t) - \omega t r + \alpha r + \cos(\alpha), & \alpha < \omega t < \pi + \beta \\ 0, & \pi + \beta < \omega t < \pi + \alpha \end{cases}, \qquad DVM \tag{3.25}$$

where $\theta$ is the variable representing the time $\omega t$. The waveform of the parallel-capacitor voltage $u_{Cp}$ can be considered as a horizontally and vertically stretched figure from this newly defined function $f(\theta, \alpha, r)$. Parallel-capacitor voltage $u_{Cp}$ can be decided by three describing factors: the shape of the waveform described by $f(\theta, \alpha, r)$, the amplitude and the switching frequency. In other words, the shape of parallel-capacitor voltage $u_{Cp}$ in SPRC is the same as the function $f(\theta, \alpha, r)$, expressed as

$$u_{Cp}(t) = \frac{I_{Ls}}{\omega C_s} f(\omega t, \alpha, r) \tag{3.26}$$

Afterwards, this newly defined function can be analysed independently. As the angle $\theta$ represents $\omega t$, the shape of the waveform $f(\theta, \alpha, r)$ actually depends on the other two inner

parameters, angle $\alpha$ and current ratio $r$. In Figure 3.6, three examples of waveform with different $\alpha$ and $r$ are illustrated.



$\alpha = 0.8, r = 0.7174$ $\alpha = 0.5370, r = 0.5669$ $\alpha = 1.2534, r = 0.2290$

(a. DVM) (b. Critical point) (c. CVM)

Figure 3.7: Waveform examples of $f(\theta, \alpha, r)$ depending on $\alpha$ and $r$

The operation mode can be divided into CVM and DVM. The definition of these two operation modes are the same as extended fundamental AC analysis.

If $(\theta, \pi + \alpha, r) = 0$, the waveform returns to zero exactly at the end of the half cycle $\omega t = \pi + \alpha$, as the third figure in Figure 3.7 (c) illustrates. It is operated in CVM. The expression of the angle $\alpha$ is obtained by two equations.

$$f(\theta, \alpha, r) = 0, \qquad f(\theta, \pi + \alpha, r) = 0 \tag{3.27}$$

If $f(\theta - \Delta\theta, \pi + \alpha, r) = 0$, the dependent variable returns to zero before the end of the half cycle, as illustrated in Figure 3.7 (a), it is operated in DVM. Here, $\Delta\theta$ represents a small positive angle difference. The expression of the angle $\alpha$ is obtained from time point $\theta = \alpha$,

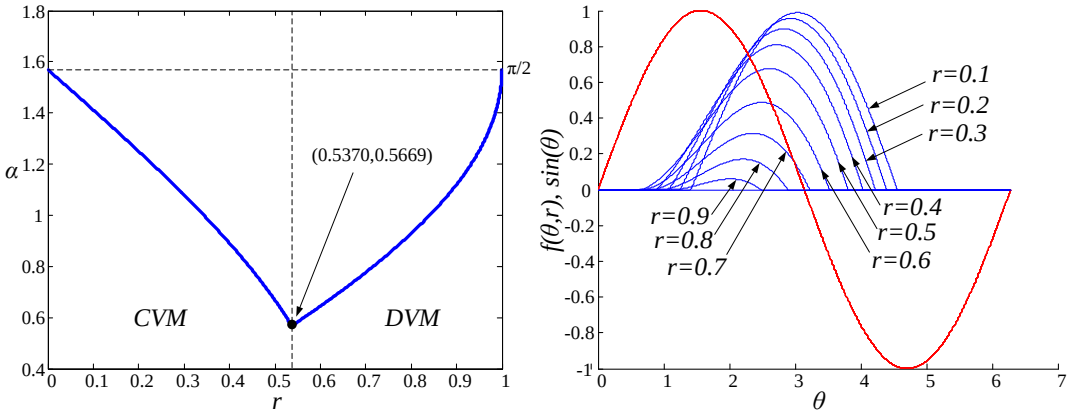
$$f(\theta, \alpha, r) = 0 \tag{3.28}$$

The transition between CVM and DVM mentioned in [FWM03] and [Cao14] is also correct, but the transition condition can be given more strictly as

$$r_c = \frac{2}{\sqrt{\pi^2 + 4}} \approx 0.5370, \quad \alpha_c = \text{asin}\left(\frac{2}{\sqrt{\pi^2 + 4}}\right) \approx 0.5669 \tag{3.29}$$

Combining these two modes, the relationship of angle $\alpha$ and current ratio $r$ is given in formula (3.30) and illustrated in Figure 3.8(a). With this relationship of $\alpha$ and $r$, the shape of function waveform has only one freedom degree. It can be described by one parameter, e.g. by the current ratio $r$.

$$\alpha(r) = \begin{cases} \text{asin}(r), & if\, r \geq r_c\,, DVM \\ \text{acos}\left(\frac{\pi r}{2}\right), & if\, r < r_c\,, CVM \end{cases} \tag{3.30}$$




(a) (b)

Figure 3.8: (a) Relationship between angle $\alpha$ and current ratio $r$ and (b) series of curves depending on current ratio $r$

Figure 3.8(b) gives a series of curves with different current ratio $r$.In Figure 3.8(a), the trajectory of the angle $\alpha$ decreases from $\pi/2$ to $asin(r_c)$ in CVM, in the range $0 < r < r_c$. Then it increases from $asin(r_c)$ to $\pi/2$ in DVM in the range $r_c < r < 1$, which can also be observed in Figure 3.8(b). Those shapes of curves vary from an approximate sinusoidal waveform ($r = 0.1$) to a severely distorted waveform ($r = 0.9$) when current ratio $r$ varies.

After all analysis above, the shape of parallel-capacitor voltage $u_{Cp}$ can be described by the function $f(\theta, r) = f(\theta, \alpha(r), r)$. There is only one parameter deciding the shape, which makes the following AC analysis possible.

### 3.4.3 Three coefficients and expression of improved steady state model

Because the parallel-capacitor voltage $u_{Cp}$ shares the same shape as these series of curves, the application of frequency analysis and Fourier transforms are possible. With a group of curves depending on different current ratios $r$, the Fourier transforms give a series of coefficients for describing the curves. Considering simplicity of the steady-state model, only the fundamental-frequency Fourier coefficients are used in improved steady state model.

The fundamental frequency Fourier coefficients, $F_{uCp,s}(r)$ and $F_{uCp,c}(r)$, and average coefficient $F_{uCp,a}(r)$ are given by the following equations. The subscript, 's' denotes the sine part of the fundamental-frequency coefficients, 'c' denotes the cosine part of the fundamental-frequency coefficients and 'a' denotes the average coefficients. These three coefficients are the zero-order and first-order coefficients in a Fourier series.

$$F_{uCp,a}(r) = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} f(\theta,\alpha,r)d\theta \tag{3.31}$$

$$F_{uCp,s}(r) = \frac{2}{\pi}\int_{\alpha}^{\pi+\alpha} f(\theta,\alpha,r)\sin(\theta)d\theta \tag{3.32}$$

$$F_{uCp,c}(r) = \frac{2}{\pi}\int_{\alpha}^{\pi+\alpha} f(\theta,\alpha,r)\cos(\theta)d\theta \tag{3.33}$$

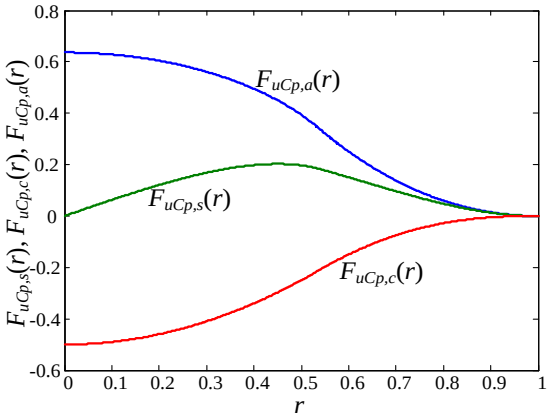



Figure 3.9: Three coefficients depending on current ratio $r$

As the curves is decided by the only parameter $r$, these coefficients are depending on this parameter, current ratio $r$. The coefficients can be considered as three functions of the current ratio $r$, as illustrated in Figure 3.9. With three coefficients, the formulas (3.34) and (3.35) approximately describe the parallel-capacitor voltage $u_{Cp}$ and its rectified value $|u_{Cp}|$.

$$u_{Cp} = \frac{I_{Ls}}{\omega C_p}\left(F_{uCp,s}(r)\, sin(\omega t) + F_{uCp,c}(r)\, cos(\omega t)\right) \tag{3.34}$$

$$\overline{|u_{Cp}|} = \frac{I_{Ls}}{\omega C_p} F_{uCp,a}(r) \tag{3.35}$$

Here, the coefficients $F_{uCp,s}(r)$ and $F_{uCp,c}(r)$ describe the fundamental harmonic of the parallel-capacitor voltage $u_{Cp}$. The coefficient $F_{uCp,a}(r)$ describes the equivalent DC voltage of the distorted voltage $u_{Cp}$. Because $F_{uCp,s}(r)$ is always positive and $F_{uCp,c}(r)$ is always negative, the equivalent impedance $Z_{equ}(r)$ can be considered as a connection of resistor and capacitor in the real circuit.

Therefore, the AC equivalent impedance $Z_{equ}(r)$ is a complex function depending on the real value $r$. It can be expressed as

$$Z_{equ}(r) = \frac{1}{\omega C_p}\left(F_{uCp,s}(r) + jF_{uCp,c}(r)\right) \tag{3.36}$$

These coefficients are functions depending on only one variable, the current ratio. They are not directly related to the components' parameters of the electrical circuit. These coefficients are common method for the SPRC-LC topology with different parameters and operation points.

By inserting (3.35) and (3.36) to the model of SPRC, the improved steady state analysis of SPRC-LC is proposed. The equivalent circuit of the SPRC is illustrated in Figure 3.10. As the functions of current ratio $r$, the impedance $Z_{equ}$ and DC voltage $\overline{|u_{Cp}|}$ is the mathematical approach for distorted voltage $u_{Cp}$.

The circuit clearly illustrates the difference between extended fundamental AC analysis and improved steady-state analysis. Instead of impedance $Z_{ac}$, which is related to the load resistance $R_L$, the novel impedance $Z_{equ}\,(r)$ depends on the current ratio $r$. Besides the resonant components, the DC equivalent circuit of the output filter also appears, including the equivalent DC source $\overline{|u_{Cp}|}$. The DC voltage $\overline{|u_{Cp}|}$ depends on the resonant current and the current ratio $r$. All the passive components except the parallel-capacitor $C_p$ are included in the novel steady-state model.

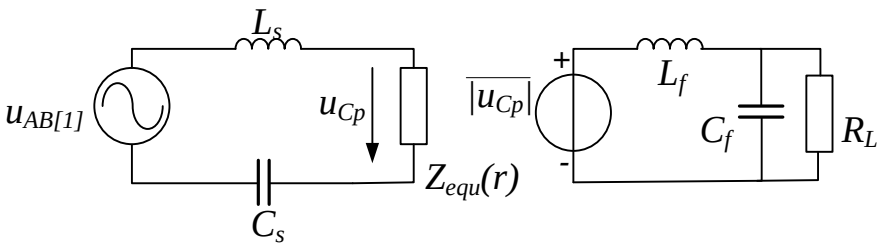



Figure 3.10: Equivalent circuit of SPRC with improved steady-state analysis

The estimation procedure with PFWM or PFM modulation has four steps in a novel analysis approach. By inserting $u_{out} = i_{out} R_L$ into (3.35), it gives

$$\frac{F_{uCp,a}(r)}{r} = \omega C_p R_L \tag{3.37}$$

First, solve the steady-state ratio $r$ from equation (3.37). Second, the impedance $Z_{equ}\,(r)$ can be calculated with (3.36). Third, the resonant current $I_{Ls}$ can be calculated with (3.22). The values of the entire circuit, including resonant-tank part and filter part, can be calculated finally.

When using OM modulation, both steady-state analyses (Forsyth's and the improved) have two or more unknown intermediate variables. There are angles $\alpha$, $\beta$ and switching frequency $\omega$ in extended fundamental AC analysis, and ratio $r$ and switching frequency $\omega$ in improved steady-state analysis. For both analysis methods, the explicit values can only be obtained

from two or more transcendental equations. In this case, the steady-state analysis can be calculated from the large-signal model or HSD model in the following chapter.

### 3.4.4 Advantages of improved steady-state analysis

The improved steady-state analysis is mathematically equivalent to extended fundamental AC analysis with PFWM or PFM modulation. The major difference between these two analysis approaches lies on the expressions of distorted parallel-capacitor voltage. Extended fundamental AC analysis utilizes the impedance $Z_{ac}$ which is equivalent to the whole secondary side of SPRC-LC circuit, including the load resistance. Thus, the dynamic process of changing load resistance is hard to describe in extended fundamental AC analysis. However, it is not a problem in improved steady-state analysis. Because the filter is included in the equivalent circuit, the changing of the load can be described correctly.

Another advantage of improved steady-state analysis is its possibility for implementing to digital devices. In extended fundamental AC analysis, the distortion of $u_{Cp}$ is described by the load resistance. Numerical solutions are the only method for the extended fundamental AC model. In improved model, the current ratio $r$ can be approximately calculated by the look-up table in practice, using three coefficients. The distortion is described only by current ratio and the shape of distorted waveform is already decided by a group of curves.

The angle $\alpha$ and $\beta$ are sensitive parameters in extended fundamental AC analysis. They are also relatively difficult to obtain explicit value through numerical solution. In digital devices, the calculation resources are not enough to solve these complex equations. However, the improved steady-state analysis can be implemented as a look-up table like Figure 3.9. The numerical solution of (3.37) can also be realized in linear interpolated look-up table. The complexity of modelling approach is reduced dramatically from extended fundamental AC

analysis. Thus, the calculation algorithm of improved steady-state analysis can be described by the following five steps.

Step 1: Calculate the expression $\omega C_p R_L$ with circuit parameters, with (3.37)

Step 2: Obtain the value $r$ from the look-up table calculated in advance

Step 3: Utilize the value $r$ to estimate the equivalent impedance $Z_{equ}$, by two corresponding look-up tables $F_{uCp,s}(r)$ and $F_{uCp,c}(r)$, with (3.32) and (3.33)

Step 4: Calculate the amplitude of resonant current with equivalent impedance $Z_{equ}$ with (3.22).

Step 5: Estimate the output voltage as the average voltage $\overline{|u_{Cp}|}$ by a look-up tables, with (3.26)

## 3.5 Simulation and experimental verification

The accuracy verification of improved steady-state analysis utilizes an existing SPRC-LC prototype with a rated power of 32 kW. The details of the hardware setup will be introduced in Chapter 7.

Experimental measurements, circuit simulation results and model calculation results are compared with given load resistance, switching frequency and duty ratio. The load resistance varies from 0.61 Ω to 15.9 Ω, in order to verify the accuracy of the novel model in a wide operation range. PFWM is selected as the modulation strategy in this verification.

The circuit simulation is operated in Matlab®/Simulink® platform with PLECS® plugin software. The experimental prototype is operated with 0.5μs dead time and with real energy losses, because these factors are inevitable in a real experimental device. There is also 0.5μs dead time in simulation. In order to compare the result fairly, dead time is compensated in simulation and experiment.

Output voltage, output current and amplitude of resonant current are compared at the same operate point, as given in Table **3.3**. The relative error is given in the right volumes. In the table, it is illustrated that the improved steady-state analysis has consistent performance with the measurement and simulation results. There are less than 11% calculation deviation vs. the measured variables, except for the very heavy load condition $R_L$ = 0.61 Ω. In the measured four points, improved model shows better accuracy in three points than circuit simulation, except the point at load condition $R_L$ = 2.59 Ω. Improved steady-state analysis shows an acceptable accuracy in wide operating range, when compared to the circuit simulation.

Table 3.3: Verification of improved steady-state analysis with PFWM modulation

| | $R_L$/ Ω | $f_s$ / kHz | $D$ / 1 | $U_{out}$ / V | $I_{out}$ / A | $I_{Ls}/A$ | $\Delta U_{out}$ | $\Delta I_{out}$ | $\Delta I_{Ls}$ |
|---|---|---|---|---|---|---|---|---|---|
| Measurement | 0.61 | 39.8 | 0.2873 | 47.62 | 77.9 | 83.7 | | | |
| Simulation | | | | 68.65 | 113.6 | 118 | 44.16% | 45.83% | 40.98% |
| Calculation | | | | 58.61 | 96.53 | 101.7 | 23.08% | 23.92% | 21.51% |
| Measurement | 2.59 | 44.97 | 0.505 | 194.6 | 75.9 | 100.5 | | | |
| Simulation | | | | 206 | 79.67 | 107.1 | 5.86% | 4.97% | 6.57% |
| Calculation | | | | 216 | 83.77 | 100.2 | 11.00% | 10.37% | -0.30% |
| Measurement | 7.89 | 55.036 | 0.6649 | 381.7 | 48.3 | 78.4 | | | |
| Simulation | | | | 401.7 | 51.76 | 84.2 | 5.24% | 7.16% | 7.40% |
| Calculation | | | | 393.2 | 49.84 | 81.04 | 3.01% | 3.19% | 3.37% |
| Measurement | 15.9 | 65.865 | 0.5767 | 480.4 | 30.4 | 74 | | | |
| Simulation | | | | 503.6 | 32.58 | 78.8 | 4.83% | 7.17% | 6.49% |
| Calculation | | | | 482.3 | 29.9 | 72.08 | 0.40% | -1.64% | -2.59% |

## 3.6 Summary

The gain characteristic of the SPRC-LC model is investigated in this chapter, along with the search for the appropriate modelling algorithm, which balances between complexity and accuracy. Sampled-data method and time-domain analysis are not suitable because of their complicated algorithms and extensive utilization of numerical solutions.

Extended fundamental AC analysis, proposed by Forsyth, is selected for further development in this chapter. Considering the distorted parallel-capacitor voltage, the extended fundamental AC analysis has a good accuracy in heavy-load condition. Extended fundamental AC analysis, however, has two major disadvantages. First, it cannot take the output filter into consideration because of its assumptions. Second, extended fundamental AC analysis suffers from high requirements of large calculation resources when implementing its algorithm.

Because of those problems, an improved steady-state analysis is proposed. This novel analysis method sets an intermediate parameter, current ratio $r$, in the modelling process. It shows that the parallel-capacitor voltage waveform has only one degree of freedom, which can be described by this parameter $r$. By defining a new function describing the shape of the voltage, three coefficients of the waveform are calculated, dependent only on the current ratio $r$. Thus, the modelling approach is largely simplified in derivation and calculation.

Improved steady-state analysis has two advantages as following. First, improved steady-state analysis is suitable to be implemented in devices with low calculation abilities. The algorithm is calculated without numerical solutions. The coefficients can be implemented in look-up tables, which are calculated in advance, so that the calculation requirement of improved steady-state analysis is extremely low in practice. Second, the load resistance is not involved in the equivalent AC impedance, which makes dynamic analysis more convenient when the load is changing. Improved steady-state model can be easily extended to the corresponding large-signal model. It will be introduced in the following chapter.

# 4 Continuous models and half-cycle-sampled discrete models of SPRC with OM

Steady-state models mainly serve for the first-step design for power converters, such as prediction of output range and design of operating points. However, for the dynamic performance prediction, an appropriately designed controller is necessary. Effective controller design depends on the accurate small-signal model of the converter. As pursuing the best dynamic performance of SPRC, a continuous small-signal model of SPRC is normally required. There are already many dynamic analysis methods for resonant converters, as mentioned in Section 3.1. These methods usually assume that the switching frequency is constant. They can be utilized to analyse the dynamic behaviour of the SPRC modulated by PFM and PFWM. But problems arise when OM is implemented in SPRC-LC, with self-adaptive switching frequency.

Improved steady-state analysis, proposed in the last chapter, considers four passive components in the equivalent circuit. The corresponding derivation of large- and small-signal models for SPRC-LC-OM will be introduced in detail in this chapter. After that, the half-cycle-sampled discrete model (HSD model) is also derived employing the method mentioned in Chapter 2. The process of HSD modelling is introduced step by step in this chapter.

The derivation of the large-signal model for the SPRC-LC-OM is introduced in Section 4.1. By adding perturbations and linearizing to the steady-state operation point, the small-signal model is derived in Section 4.2. As the novel modelling method, the HSD model is

introduced in detail in Section 4.3. The simulation and the experimental verifications are illustrated in Section 4.4. Finally, a short conclusion is given in Section 4.5.

## 4.1 Large-signal and nonlinear model

In the previous chapter, the extended fundamental AC analysis [FWM03] has been introduced, considering the distortion of the parallel-capacitor voltage. Because of the complex mathematical approach with transcendental equations, it is difficult to be extended to a large-signal model. There were one large-signal model trial of this method in [CNT+12], using a series of numerical solutions to realize the large-signal model. This model is based on iterative algorithms along the operating time. In order to solve the transcendental equations, Newton-Raphson numerical method is applied in this model, which requires a lot of calculation resources. Therefore, it is normally utilized only for computer-aided analysis.

In other modelling techniques [BYR96] [YLJ92], the switching frequency is always assumed constant. SPRC-LC-OM is not covered in these modelling techniques because of its varying switching frequency. The only small-signal modelling method including varying switching frequency is mentioned in [CTF+13]. The basic idea of this modelling technique is time-domain analysis. The time-dependent waveforms are separated into three periods in each half cycle. The calculation has to keep strict boundary conditions and needs a high level of explicit numerical solutions. Complicated algorithms make the time-domain analysis difficult to be implemented on low-cost devices in practice.

In order to overcome these drawbacks, the extended dynamic model from improved steady-state analysis is introduced in this chapter. As mentioned in Chapter 3, the performance of parallel capacitor and rectifier is described by equivalent impedance and controlled DC voltage source in the improved steady-state analysis. Four passive components, except the parallel capacitor, are included in the simplified equivalent circuit. Thus, the fourth-order

large- and small- signal model can be deduced from the simplified equivalent circuit as shown in Figure 3.10.

The half cycle sampling, as mentioned in Chapter 2, can be utilized in the dynamic model of SPRC. It creates the novel HSD model with one sampling at each half cycle. The process is given with following steps.

Step 1: Formulate the original continuous model

Step 2: Describe the model with slowly changing variables instead of fast changing variables.

Step 3: Assume the variables to be constant in half cycle period.

Step 4: Analyse the half cycle interval. Give the novel continuous model.

Step 5: Deduce small-signal model by linearization and perturbation of the continuous model.

Step 6: Obtain linear and nonlinear HSD models by varying step sampling.

### 4.1.1 Original continuous model

**Step 1: Original continuous model is given.**

Similar as in the previous chapter, the model of SPRC is simplified in order to focus on the derivation. The major assumptions and simplifications of SPRC circuit are the same as in Chapter 3. The detailed assumptions can be found in Section 3.2.

Based on Kirchhoff's circuit laws and the characteristics of inductors and capacitors, the continuous model of the SPRC-LC is expressed by formulae (4.1) to (4.5).

$$L_s \frac{di_{Ls}}{dt} = u_{AB} - u_{Cs} - u_{Cp} \tag{4.1}$$

$$C_s \frac{du_{Cs}}{dt} = i_{Ls} \tag{4.2}$$

$$C_p \frac{du_{Cp}}{dt} = i_{Ls} - i_R \tag{4.3}$$

$$L_f \frac{di_{Lf}}{dt} = |u_{Cp}| - u_{Cf} \tag{4.4}$$

$$C_f \frac{du_{Cf}}{dt} = i_{Lf} - \frac{u_{Cf}}{R_L} \tag{4.5}$$

Here, $i_R$ represent the current on rectifier, a square waveform depending on the ON/OFF statues of rectifier. In order to give the simplest description, SPRC converter can be considered as two-input-one-output black box in this system. The input variable vector is $[D, u_{dc}]^T$ and the output vector is $[u_{Cf}]$. The vector of state variables is $[i_{Ls}, u_{Cs}, u_{Cp}, i_{Lf}, u_{Cf}]^T$ in this original continuous model.

### 4.1.2 Major assumptions of HSD model

**Step 2: Describing the model with slowly changing variables.**

In the original continuous model, the AC variables of resonant components, $u_{AB}$, $u_{Cs}$, $u_{Cp}$ and $i_{Ls}$ are fast-varying time-dependent variables. They change from positive to negative or from negative to positive within each half cycle. The resonant current $i_{Ls}$ is assumed as an ideally sinusoidal waveform, as the same as Chapter 3. Parallel capacitor voltage is integrated by resonant current from equation (4.3).The conclusion of Chapter 3 proves $u_{Cp}$ can be described with three coefficients. Using the amplitude of resonant current $I_{Ls}$ as the parameter, these variables are expressed as

$$i_{Ls}(t) = I_{Ls} sin(\omega t) \tag{4.6}$$

$$u_{Cp} = U_{Cp,s}\, sin(\omega t) + U_{Cp,c}\, cos(\omega t) = \frac{I_{Ls}}{\omega C_p} F_{uCp,s}(r)\, sin(\omega t) + \frac{I_{Ls}}{\omega C_p} F_{uCp,c}(r)\, cos(\omega t) \tag{4.7}$$

$$|u_{Cp}| = \frac{I_{Ls}}{\omega C_p} F_{uCp,a}(r) \tag{4.8}$$

The definitions of current ratio $r$ and the three coefficients ($F_{uCp,a}(r)$, $F_{uCp,s}(r)$, $F_{uCp,c}(r)$) are the same as Chapter 3. Current ratio $r$ equals to the value that output filter current divides

by the amplitude of resonant current, $r = I_{Lf}/I_{Ls}$. For the series capacitor voltage, the expression yields by inserting (4.6) into (4.2).

$$u_{Cs}(t) = U_{Cs,c}cos(\omega t) = -\frac{I_{Ls}}{\omega C_s}cos(\omega t) \tag{4.9}$$

Here, the series-capacitor voltage $u_{Cs}$ is also considered as an ideally sinusoidal waveform.

The AC variables $u_{AB}$ are also replaced by similar expressions: the fundamental-frequency component of its Fourier series. The voltage $u_{AB}$ is expressed as,

$$U_{AB,s} = U_{dc}\frac{2-2cos(\pi D)}{\pi}, \qquad U_{AB,c} = U_{dc}\frac{2sin(\pi D)}{\pi} \tag{4.10}$$

$$u_{AB}(t) = U_{AB,c}\,cos(\omega t) + U_{AB,s}\,sin(\omega t) \tag{4.11}$$

Here, capital letters represent amplitude variables of fundamental frequency. Using fundamental harmonics representing the AC variables, the system is described by slowly-changing variables ($U_{AB,s}$, $U_{AB,c}$, $U_{Cs,c}$, $U_{Cp,s}$, $U_{Cp,c}$ and $I_{Ls}$) instead of fast changing variables ($u_{AB}$, $u_{Cs}$, $u_{Cp}$ and $i_{Ls}$). These variables are almost stable during time, changing slowly within nearby half cycles. This is a significant precondition for the next assumption.

The DC-filter variables ($u_{Cf}$ and $i_{Lf}$) can also be represented with similar slowly-changing variables. Real DC-filter variables contain some switching frequency ripples. In the slowly-changing expression, its averaged values in half cycle ($U_{Cf}$ and $I_{Lf}$) is utilized, ignoring high-frequency ripples.

By introducing these variable conversions, SPRC model is described by slowly-changing variables. All the high-order harmonics and ripples are ignored in this conversion, except the distortion of voltage $u_{Cp}$. The distortion of voltage $u_{Cp}$ is assumed as the major reason of nonlinear behaviour of SPRC and is the only distortion considered in slowly-changing model. The small error of the slowly-changing approximations can be proved by the conclusion of Chapter 3 in most operation range.

**Step 3: Assume the variables to be constant or interpolated in half cycle**

There are two different expressions of these slowly-changing variables in the dynamic model. On one hand, variables are assumed constant in each half cycle, when they are described by steady-state equation (4.6) (4.7) (4.9) and (4.11). On the other hand, the changing value in each half-cycle interval is significant for describing the dynamic behaviour of SPRC. Thus, the major assumption of this step is to divide these variables into basic values and the changing values in each half-cycle interval. Using the switching frequency as the example, the actual value ω can be sampled when the resonant current goes though zero, while it can be approximately described by its basic value $\omega_n$ and changing value $\Delta\omega_n$ in each half-cycle interval (n=0,1,2,3...). Because these variables are slowly-changing, the basic value $\omega_n$ is much larger than changing value $\Delta\omega_n$.

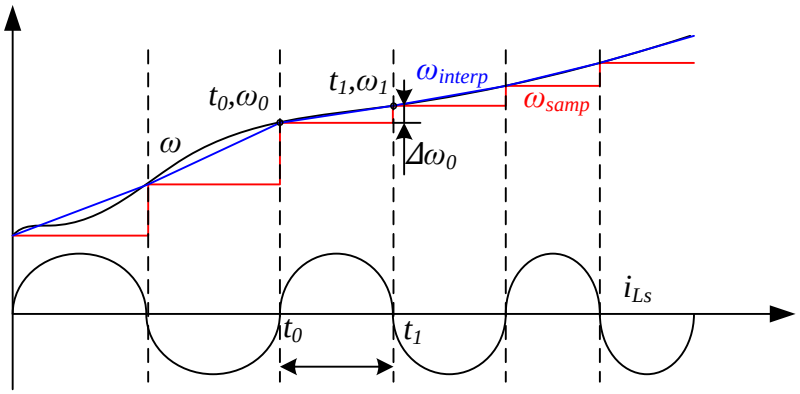



Figure 4.1: Approximation of slowly-changing variables

The slowly-changing variables can be approximately described by two different ways in each half-cycle interval. The first one is to directly use the basic value $\omega_n$ in the current half-cycle interval and to add the changing values $\Delta\omega_n$ at the end of current half-cycle interval. It can be called as sampling-like approximation. The other one is to assume that the variable is ramp-like in current half cycle. At the end of current half-cycle, the variable reaches the value

$\omega_n + \Delta\omega_n$. It can be called as interpolation-like approximation. These two approximations, shown by the red and the blue lines in the Figure 4.1, will introduce more deviation into the system but will give simple mathematical expression.

To achieve the simplest form of a dynamic model, slowly-changing voltage and current values are described by sampling-like approximation. The switching frequency is firstly described by interpolation-like approximation. In the deduction process, switching frequency will be secondly approximated as sampling-like. For the first step, the switching frequency in interval $t_0 < t < t_1$ can be expressed as

$$\omega(t) = \omega(t_0) + \frac{\omega(t_1) - \omega(t_0)}{t_1 - t_0}(t - t_0), \qquad t_0 < t < t_1 \tag{4.12}$$

or with a simpler form as

$$\omega(t) = a + b(t - t_0)\,, \qquad t_0 < t < t_1 \tag{4.13}$$

Here, $a$ and $b$ are the parameters depending on two points in the waveform $(t_0, \omega(t_0))$, $(t_1, \omega(t_1))$.

$$a = \omega(t_0) \tag{4.14}$$

$$b = \frac{\omega(t_1) - \omega(t_0)}{t_1 - t_0} \tag{4.15}$$

### 4.1.3 Slowly-changing continuous model

**Step 4: Obtain slowly-changing continuous model.**

After first-level approximation, the slowly-changing model can be deduced from the original continuous model. In the interval $t_0 < t < t_1$, the resonant current can be described with the interpolated-like approximated switching frequency as

$$i_{Ls}(t) = I_{Ls}(t)sin(\omega(t)(t - t_0)) = I_{Ls}(t)sin(a(t - t_0) + b(t - t_0)^2) \tag{4.16}$$

The differential of resonant current yields,

$$\frac{di_{Ls}(t)}{dt} = \frac{d(I_{Ls}(t)sin(a(t-t_0)+b(t-t_0)^2))}{dt} \tag{4.17}$$
$$= sin(a(t-t_0)+b(t-t_0)^2)\frac{dI_{Ls}(t)}{dt}$$
$$+ I_{Ls}(t)cos(a(t-t_0)+b(t-t_0)^2)(a+2b(t-t_0))$$

The voltages $u_{Cs}$, $u_{Cp}$, and $u_{AB}$ can be expressed by the integration of the resonant current. Use the series capacitor voltage as the example, it gives,

$$u_{Cs}(\mathrm{t}) = \frac{1}{C_s}\int_{t_0}^{\mathrm{t}} i_{Ls}(\tau)\mathrm{d}\tau = \frac{1}{C_s}\int_{t_0}^{\mathrm{t}} I_{Ls}(\tau)sin(a(\tau-t_0)+b(\tau-t_0)^2)\,\mathrm{d}\tau \tag{4.18}$$

Because of sampling-like approximation, $I_{Ls}(\tau)$ can be replaced with the $I_{Ls}(t_0)$. For the same reason, $\omega(\tau) = a + b(\tau - t_0)$ can also be simplified by sampling-like approximation in the integration term $\omega(t_0)$. The voltage can approximately be expressed by the value depending on starting time $t_0$. It gives,

$$I_{Ls}(\tau) \approx I_{Ls}(t_0), \quad t_0 < \tau < t_1 \tag{4.19}$$

$$\omega(\tau) \approx \omega(t_0), \quad t_0 < \tau < t_1 \tag{4.20}$$

$$u_{Cs}(\mathrm{t}) \approx \frac{1}{C_s}\int_{t_0}^{\mathrm{t}} I_{Ls}(t_0)sin(\omega(t_0)(\tau-t_0))\,\mathrm{d}\tau = -\frac{I_{Ls}(t_0)}{\omega(t_0)C_s}cos(\omega(t_0)(t-t_0)) \tag{4.21}$$

The other voltages $u_{Cp}$, and $u_{AB}$, are using the same approximation. Here directly gives the approximation results.

$$u_{Cp}(t) \approx \frac{I_{Ls}(t_0)}{\omega(t_0)C_p}\left(F_{uCp,s}(r)\,sin(\omega(t_0)(t-t_0)) + F_{uCp,c}(r)\,cos\,\omega(t_0)(t-t_0)\right) \tag{4.22}$$

$$u_{AB}(t) \approx U_{AB,c}\,cos(\omega(t_0)(t-t_0)) + U_{AB,s}\,sin(\omega(t_0)(t-t_0)) \tag{4.23}$$

Here, the voltages are expressed with the help of steady-state factors $F_{uCp,s}(r)$, $F_{uCp,c}(r)$ from (3.31) and (3.32). In the actual dynamic process of SPRC, the voltages are slightly different from its steady-state waveform, as the resonant current $I_{Ls}(\tau)$ is changing in this half-cycle. It is approximately expressed by these factors, because the major distortions of waveforms are still on the voltage $u_{Cp}(t)$. Inserting (4.21), (4.22) and (4.23), the equation (4.1) is replaced with the following equation.

$$
\begin{aligned}
L_s sin(a(t-t_0)+b(t-t_0)^2)\frac{dI_{Ls}(t)}{dt} + L_s I_{Ls}(t) cos(a(t-t_0)+b(t-t_0)^2)(a \\
+ 2b(t-t_0)) \\
= U_{AB,s}\, sin\big(\omega(t_0)(t-t_0)\big) + U_{AB,c}\, cos\big(\omega(t_0)(t-t_0)\big) \\
+ \frac{I_{Ls}(t_0)}{\omega(t_0)C_s} cos\big(\omega(t_0)(t-t_0)\big) \\
- \frac{I_{Ls}(t_0)}{\omega(t_0)C_p}\big(F_{uCp,s}(r)\, sin\big(\omega(t_0)(t-t_0)\big) \\
+ F_{uCp,c}(r)\, cos\big(\omega(t_0)(t-t_0)\big)\big)
\end{aligned}
\tag{4.24}
$$

Here, $a(t-t_0)+b(t-t_0)^2 = \omega(t_0)(t-t_0)$. The equation can be divided into two parts. The sine terms can be simplified as

$$
L_s \frac{dI_{Ls}(t)}{dt} = U_{AB,s} - \frac{I_{Ls}(t_0)}{\omega(t_0)C_p} F_{uCp,s}(r) \tag{4.25}
$$

The equation above is the differential equation for the function of $I_{Ls}(t)$. Eliminate the common factors in cosine equation, dividing $L_s I_{Ls}(t_0) cos\big(\omega(t_0)(t-t_0)\big)$ in both sides, at the time point $t_1$,

$$
a + 2b(t_1 - t_0) = \frac{U_{AB,c}}{L_s I_{Ls}(t_0)} + \frac{1}{\omega(t_0)L_s(t_0)C_s} - \frac{F_{uCp,c}(r)}{\omega(t_0)L_s C_p} \tag{4.26}
$$

Reorganize (4.26), it gives

$$
b = \frac{1}{2(t_1-t_0)}\left(\frac{U_{AB,c}}{L_s I_{Ls}(t_0)} + \frac{1}{\omega(t_0)L_s(t_0)C_s} - \frac{F_{uCp,c}(r)}{\omega(t_0)L_s C_p} - a\right) \tag{4.27}
$$

Inserting the definition of $a$ and $b$ first. Because of sampling-like approximation, the length of interval can be given as $t_1 - t_0 \approx \pi/\omega(t_0)$.

$$
\begin{aligned}
\frac{d\omega(t)}{dt} \approx \frac{\omega(t_1)-\omega(t_0)}{t_1-t_0} = b \\
= \frac{\omega(t_0)}{2\pi}\left(\frac{U_{AB,c}}{L_s I_{Ls}(t_0)} + \frac{1}{\omega(t_0)L_s C_s} - \frac{F_{uCp,c}(r)}{\omega(t_0)L_s C_p} - \omega(t_0)\right)
\end{aligned}
\tag{4.28}
$$

Here, the differentiation of switching frequency is replaced with its slope in interpolation-like approximation. Of course, more deviation is introduced into the system. This is a trade-off between the calculation complexity and the precision.

Equations (4.25) and (4.28) are both depending on the values at the instant $t = t_0$. The state

of resonant tank can be decided by two variables: $I_{Ls}(t_0)$ and $\omega(t_0)$. The differential of $I_{Ls}$ and $\omega$ can be calculated by the (4.25) and (4.28) approximately. These two equations can be simplified as following.

$$\frac{dI_{Ls}(t)}{dt} = \frac{U_{AB,s}}{L_s} - \frac{I_{Ls}(t)}{\omega(t)C_pL_s}F_{uCp,s}(r) \tag{4.29}$$

$$\frac{d\omega(t)}{dt} = \frac{\omega(t)U_{AB,c}}{\pi L_s I_{Ls}(t)} + \frac{1}{\pi C_s L_s} - \frac{F_{uCp,c}(r)}{\pi L_s C_p} - \frac{\omega(t)^2}{\pi} \tag{4.30}$$

DC analysis is applied to the output filter circuit of the SPRC. By inserting equation (4.8) into (4.4) and (4.5), it gives

$$\frac{dI_{Lf}(t)}{dt} = \frac{I_{Ls}(t)}{\omega(t)C_pL_f}F_{uCp,a}(r) - \frac{U_{Cf}(t)}{L_f} \tag{4.31}$$

$$\frac{dU_{Cf}(t)}{dt} = \frac{I_{Lf}(t)}{C_f} - \frac{U_{Cf}(t)}{C_fR_L} \tag{4.32}$$

Thus, the original fast-changing model expressed by small letters is replaced by the slowly-changing model expressed by capital letters. Equations (4.29), (4.30), (4.31) and (4.32) give the fourth-order continuous large-signal model of the SPRC. The state variables in this model are $\left[I_{Ls},\ \omega,\ I_{Lf},\ U_{Cf}\right]^T$. Here, the slowly-changing model is an approximate model, because of these approximations in step 2 and step 3. As the slowly-changing characteristics of SPRC system, the approximate error is relative negligible.

In the model, equations (4.31) and (4.32) describe the dynamic behaviour of the output filter. Equation (4.29) describes the changing amplitude of resonant current and equation (4.30) describes the changing of switching frequency. As the switching frequency varies in this novel model, the large-signal model is suitable for describing SPRC-LC-OM system. Just like the process of OM modulation, the switching frequency is calculated and adjusted every half cycle.

## 4.2 Small-signal and linear model

**Step 5: Deduce small-signal model from slowly-changing continuous model.**

Steady-state model and small-signal model can be derived from the large-signal model, describing the dynamic behaviour around a stable operation point. Supposing the differential parts equal to zero in (4.29), (4.30), (4.31) and (4.32), the steady-state model is obtained as,

$$0 = \frac{U_{AB,s}}{L_s} - \frac{I_{Ls}}{\omega C_p L_s} F_{uCp,s}(r) \tag{4.33}$$

$$0 = \frac{\omega U_{AB,c}}{\pi L_s I_{Ls}} + \frac{1}{\pi C_s L_s} - \frac{F_{uCp,c}(r)}{\pi L_s C_p} - \frac{\omega^2}{\pi} \tag{4.34}$$

$$0 = \frac{I_{Ls}}{\omega C_p L_f} F_{uCp,a}(r) - \frac{U_{Cf}}{L_f} \tag{4.35}$$

$$0 = \frac{I_{Lf}}{C_f} - \frac{U_{Cf}}{C_f R_L} \tag{4.36}$$

Because the equations still contains transcendental functions, the easy approach of steady-state analysis is still a problem in the SPRC-LC-OM model temporarily. Here, a numerical solution, which is complex mathematically, is still needed for the derivation of the steady-state model. The operation points can be calculated by solving transcendental functions.

After calculation the operation point of the steady-state model, small perturbations are added to the state variables and input variables. The model is linearized around the stable operation point in order to obtain its small-signal model. In the small-signal model, $\hat{\boldsymbol{x}}$ represents the state vector. $\hat{\boldsymbol{u}}$ represents the input vector. $\hat{\boldsymbol{y}}$ represents the output vector. The symbol hat above the variable means the small perturbation. **A** $\boldsymbol{B}$ $\boldsymbol{C}$ $\boldsymbol{D}$ are the matrixes describing the state system.

$$\hat{\boldsymbol{x}} = [\widehat{I_{Ls}} \quad \hat{\omega} \quad \widehat{I_{Lf}} \quad \widehat{U_{Cf}}]^T \tag{4.37}$$

$$\hat{\boldsymbol{u}} = [\hat{D} \quad \widehat{U_{dc}}]^T \tag{4.38}$$

$$\hat{\boldsymbol{y}} = [\widehat{U_{Cf}}] \tag{4.39}$$

After linearization, the small-signal model can be expressed as the following

$$\frac{d\hat{\boldsymbol{x}}}{dt} = \boldsymbol{A}\hat{\boldsymbol{x}} + \boldsymbol{B}\hat{\boldsymbol{u}} \tag{4.40}$$

$$\hat{\boldsymbol{y}} = \boldsymbol{C}\hat{\boldsymbol{x}} + \boldsymbol{D}\hat{\boldsymbol{u}} \tag{4.41}$$

$$\boldsymbol{A} = \begin{bmatrix} -\frac{1}{\omega C_p L_s}\left(F_{uCp,s}(r) - rF_{uCp,s}{}'(r)\right) & \frac{1}{\omega^2 C_p L_s}F_{uCp,s}(r) & -\frac{1}{\omega C_p L_s}F_{uCp,s}{}'(r) & 0 \\ -\frac{2\omega sin(\pi D)U_{dc}}{\pi^2 L_s {I_{Ls}}^2} + \frac{r}{\pi C_p L_s I_{Ls}}F_{uCp,c}{}'(r) & \frac{2sin(\pi D)U_{dc}}{\pi^2 L_s I_{Ls}} - \frac{2\omega}{\pi} & -\frac{1}{\pi C_p L_s I_{Ls}}F_{uCp,c}{}'(r) & 0 \\ \frac{1}{\omega C_p L_f}\left(F_{uCp,a}(r) - rF_{uCp,a}{}'(r)\right) & -\frac{1}{\omega^2 C_p L_f}F_{uCp,a}(r) & \frac{1}{\omega C_p L_f}F_{uCp,a}{}'(r) & -\frac{1}{L_f} \\ 0 & 0 & \frac{1}{C_f} & -\frac{1}{R_L C_f} \end{bmatrix} \tag{4.42}$$

$$\boldsymbol{B} = \begin{bmatrix} \frac{2U_{dc}sin(\pi D)}{\pi L_s} & \frac{2(1-cos(\pi D))}{\pi L_s} \\ \frac{2\omega U_{dc}cos(\pi D)}{\pi^2 I_{Ls} L_s} & \frac{2\omega sin(\pi D)}{\pi^2 L_s I_{Ls}} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{4.43}$$

$$\boldsymbol{C} = [0 \quad 0 \quad 0 \quad 1] \tag{4.44}$$

$$\boldsymbol{D} = [0 \quad 0] \tag{4.45}$$

The small-signal model of the SPRC-LC-OM is deduced from the large-signal model and has the normal expression form of the small-signal model. If the steady-state operation point is already known, the small-signal model is simple to calculate because the current ratio $r$ is already decided by stable operation point calculation. For a certain steady-state operation point, all coefficients can be calculated in advance with the current ratio $r$.

The small-signal model also considers the small perturbations on switching frequency. This is not mentioned in any other modelling techniques, except [CTF+13]. Small-signal model of SPRC is calculated with time-domain analysis in [CTF+13]. A long operation time will be calculated in time-domain and the amplitude and phase is analysed on the frequency domain. It is the reason why a large amount of calculation resources is needed. In this novel small-signal model, the dynamic behaviour of switching frequency is described by only one matrix with three coefficients. With the desired accuracy, these coefficients are calculated and interpolated in advance. Instead of a series of transcendental functions solution, this novel

small-signal model largely compresses the complexity. It is possible to calculate such a simple small-signal model in digital devices.

## 4.3 Half-cycle-sampled discrete model

**Step 6: Convert continuous mode into HSD model by varying step sampling**

The varying-step sampling is finally applied and converts the continuous model into the HSD model. Corresponding to the large-signal model and small-signal model, the nonlinear and the linear HSD models are derived in this section. Figure 4.2 illustrates the discrete description of variables in the resonant tank.

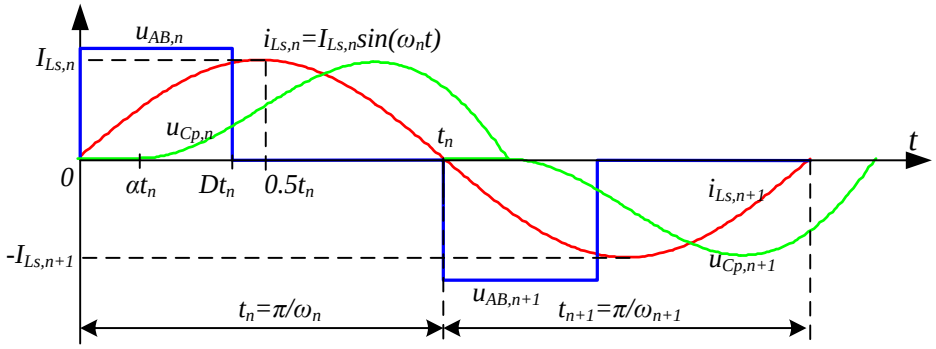



Figure 4.2: Waveform of HSD model at varying frequency

Instead of the continuous variable $I_{Ls}$, the discrete variable $I_{Ls,n}$ is utilized to describe the waveform in the half cycle. The signal $I_{Ls,n}$ is the varying-step sampling result at the starting instant of each half cycle. $I_{Ls,n+1} = I_{Ls}(t_n)$. As discussed in Chapter 2, the HSD model, as well as average model, has enough accuracy to describe the dynamic performance of the SPRC-LC-OM. By sampling the equations (4.29), (4.30), (4.31) and (4.32) in each half-cycle, a nonlinear HSD model is obtained as,

$$I_{Ls,n+1} = \frac{\pi}{\omega_n}\left(\frac{2U_{dc}(1-cos(\pi D_n))}{\pi L_s} - \frac{I_{Ls,n}}{\omega_n C_p L_s} F_{uCp,s}(r_n)\right) + I_{Ls,n} \tag{4.46}$$

$$\omega_{n+1} = \frac{2U_{dc}\ sin(\pi D_n)}{L_s I_{Ls,n}} + \frac{1}{\omega_n C_s L_s} - \frac{F_{uCp,c}(r_n)}{\omega_n L_s C_p} \tag{4.47}$$

$$I_{Lf,n+1} = \frac{\pi}{\omega_n}\left(\frac{I_{Ls,n}}{\omega_n C_s L_f} F_{uCp,a}(r_n) - \frac{U_{Cf,n}}{L_f}\right) + I_{Lf,n} \tag{4.48}$$

$$U_{Cf,n+1} = \frac{\pi}{\omega_n}\left(\frac{I_{Lf,n}}{C_f} - \frac{U_{Cf,n}}{C_f R_L}\right) + U_{Cf,n} \tag{4.49}$$

where $r_n = I_{Lf,n}/I_{Ls,n}$. It is important to point out that the discrete characteristic of the variables already appears in step 3 of the continuous deducing procedure. Some variables are assumed to be constant in each half cycle in deducing. The continuous model of the SPRC is actually sampled each half cycle in theory, though it is considered as continuous model in the mathematical expression.

Corresponding the large- and small- signal model, the nonlinear and linear HSD model is deduced. By the discretization of the small-signal model, the discrete system can be expressed as

$$\boldsymbol{x}_{n+1} = \boldsymbol{A_d}\boldsymbol{x}_n + \boldsymbol{B_d}\boldsymbol{u}_n \tag{4.50}$$

$$\boldsymbol{y}_n = \boldsymbol{C_d}\boldsymbol{x}_n + \boldsymbol{D_d}\boldsymbol{u}_n \tag{4.51}$$

The linear HSD model can also be considered as the linearization result of the nonlinear HSD model. Similar to small-signal model, linear HSD model represent small perturbations around an steady state operation point. The difference of the next half-cycle variables with the perturbation is approximated to parameters in the linear model matrixes. In the discrete system employing Forward Euler method, the matrixes are expressed as

$$\boldsymbol{A_d} = \boldsymbol{E} + \frac{\boldsymbol{A}}{2f_{s,n}} = \boldsymbol{E} + \frac{\pi \boldsymbol{A}}{\omega_n}$$

$$= \begin{bmatrix} 1 - \frac{\pi}{{\omega_n}^2 C_p L_s}\left(F_{uCp,s}(r_n) - r_n F_{uCp,s}{}'(r_n)\right) & \frac{\pi}{{\omega_n}^3 C_p L_s} F_{uCp,s}(r_n) & -\frac{\pi}{{\omega_n}^2 C_p L_s} F_{uCp,s}{}'(r_n) & 0 \\ -\frac{2sin(\pi D)U_{dc}}{\pi L_s {I_{Ls,n}}^2} + \frac{r}{\omega_n C_p L_s I_{Ls}} F_{uCp,c}{}'(r_n) & \frac{2sin(\pi D)U_{dc}}{\pi \omega_n L_s I_{Ls,n}} - 1 & -\frac{1}{C_p L_s I_{Ls,n}} F_{uCp,c}{}'(r_n) & 0 \\ \frac{\pi}{{\omega_n}^2 C_p L_f}\left(F_{uCp,a}(r_n) - r F_{uCp,a}{}'(r_n)\right) & -\frac{\pi}{{\omega_n}^3 C_p L_f} F_{uCp,a}(r_n) & 1 + \frac{\pi}{{\omega_n}^2 C_p L_f} F_{uCp,a}{}'(r_n) & -\frac{\pi}{\omega_n L_f} \\ 0 & 0 & \frac{\pi}{\omega_n C_f} & 1 - \frac{\pi}{\omega_n R_L C_f} \end{bmatrix}$$

$$\boldsymbol{B_d} = \frac{\boldsymbol{B}}{2f_{s,n}} = \frac{\pi \boldsymbol{B}}{\omega_n} = \begin{bmatrix} \frac{2U_{dc}\sin(\pi D)}{L_s} & \frac{2(1-\cos(\pi D))}{\omega_n L_s} \\ \frac{2U_{dc}\cos(\pi D)}{\omega_n I_{Ls} L_s} & \frac{2\sin(\pi D)}{\omega_n L_s I_{Ls}} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

$$\boldsymbol{C_d} = \boldsymbol{C} = [0 \quad 0 \quad 0 \quad 1]$$

$$\boldsymbol{D_d} = \boldsymbol{D} = [0 \quad 0]$$

The nonlinear model can be utilized to calculate the steady-state operation point of SPRC-LC-OM by iteration. It gives the answer of steady-state operation point calculation problem in Section 4.2. The equations (4.46) (4.47) (4.48) and (4.49) can be considered as an iteration algorithm. Under the aspect of numerical analysis, the iterative process generates a sequence of improving approximate solutions during hundreds of cycles. The numerical calculation deviation is gradually reduced in the iterative process. The linear model can be utilized to calculate the discrete transfer function and prove the stability at a certain operation point.

In order to estimate the complexity of the different modelling approaches, time-complexity analysis method in computer science is utilized. Time-complexity estimation is an algorithm quantifying the amount of time needed when the modelling approach is running in the Von Neumann architecture. The complexity of different modelling techniques is estimated in the following table.

Table 4.1: Calculation complexities of different dynamic modelling methods

| Modelling method | Modulation strategy | Reference | Including transcendental equations or not | Calculation time |
|---|---|---|---|---|
| Fundamental AC analysis | PFWM | [BYR96] | No | O($f_s$) |
| Extended describing model | PFWM | [YLJ92+] | No | O($f_s$) |
| Extended fundamental AC analysis | PFWM | [CNT+12] | Yes | O($kf_s$) |
| Time-domain analysis | OM | [CTF+13] | Yes | O($kf_s$) |
| HSD model | OM | | No | O($f_s$) |

In the table, parameter $k$ represents the number of iterations in the calculation procedure. In a group of modelling approach for SPRC, switching frequency variation is normally ignored. Compared to time-domain analysis [CTF+13] which contains numerical solutions, the HSD model requires a lower calculation capability because the iterative calculation is performed from half cycle to half cycle. The numerical solution requires finishing the iteration calculation in half cycle and uses the results for the next step calculation. Without the explicit values in half cycle, the deviations may be accumulated and the system may have problems in stability. As explicit solution is required at every calculation step, high calculation capability is needed. In HSD model, the stability of discrete model can be proved in advance by using its linear HSD model. The calculation deviation of nonlinear HSD algorithm is reduced on calculation duration when the system is proved stable. At each step, the result contains calculation deviations and explicit solution is not required. Because of this, the nonlinear HSD can estimate the operation point with a simple and clear iteration algorithm.

HSD model can also be utilized as a calculation system cooperating with OM modulator. The major usage of this system is to predict the dynamic behaviour of SPRC-OM on the hardware. SSOC modulation and OM detect the zero-crossing points of the resonant current, which is the trigger signal for the HSD model. The calculation system is triggered and executes the iteration algorithm for one step. As the HSD model is deduced for the simplest mathematical expression and lowest calculation cost, it is easy to transplant nonlinear HSD model into fast digital devices and achieve the prediction in hardware. It will be an interesting idea that a model predict control with HSD model is designed for SPRC-OM.

## 4.4 Simulation and experimental verification

The verification of HSD models is implemented in two parts, steady-state verification and small-signal-model verification.

First, the iterative algorithm of the nonlinear HSD model is verified by simulation and experiment. Four state variables are measured and simulated in different steady-state operation points. The iterative approach is used to predict the steady-state results. These state variables are obtained by iterating nonlinear HSD model until it is stable. The stable condition is set that the error between nearby period is smaller than 1 V, 0.5 A and 100 Hz. In order to prove the accuracy of model in a wide load range, the load resistance varies from 2.2 Ω to 16.3 Ω. The duty ratio varies from 0.05 to 0.95 in simulation and calculation. Some operation points are impossible to be realized and be measured in real hardware. In addition, the resonant current is not measured in experiment because current sensor is not installed in hardware.

The results of steady-state verification are illustrated in Figure 4.3. The iterative approach of the nonlinear HSD model shows a good accuracy in a wide load range. In the duty-ratio range, there shows some error in very high duty-ratio range (D>0.9) and low duty-ratio range (D<0.3). Only in the middle range (0.3<D<0.9) HSD model shows good estimate results.

In the high duty-ratio range (D>0.9), HSD model shows some error because the current on output filter inductor becomes discontinuous. This discontinuous current problem is not included in HSD model. The error is increasing when duty ratio is increasing and the load resistor is reducing. At the worst point (D=0.95, R=2.2 Ω), the voltage $u_{Cp}$ is severely distorted and has the highest peak value. The current on filter inductor has the largest ripple and become discontinuous.

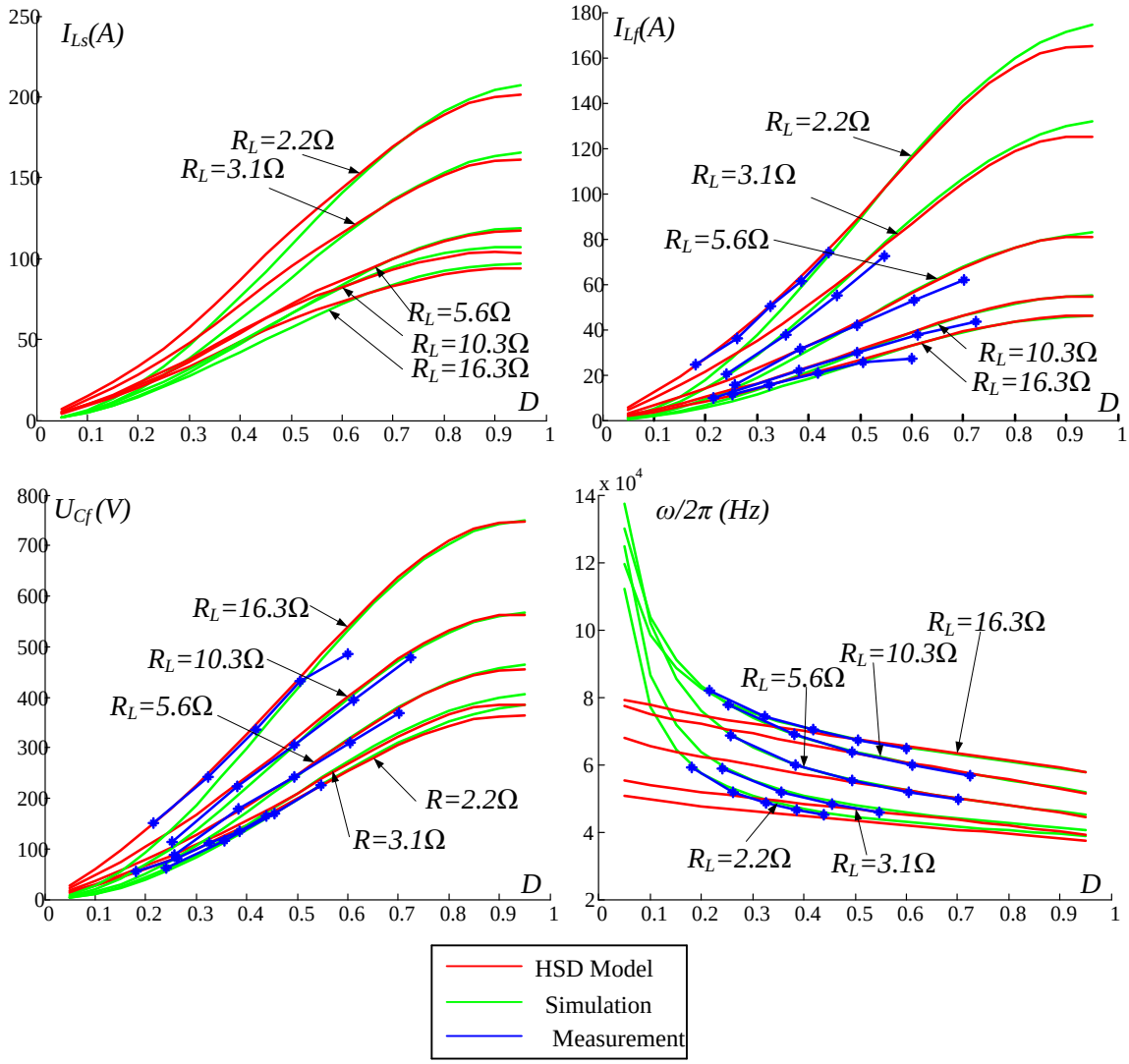



Figure 4.3: Verification of nonlinear HSD steady-state approach (red) with simulation (green) and experiment (blue)

The other kind of error occurs on low-duty-ratio range (D<0.3). With a relative small duty ratio, the voltage $u_{AB}$ contains more harmonics. And the resonant current becomes distorted, as the high-order harmonics plays a more important role in the low-duty-ratio range. The assumption of HSD model, ideal sinusoidal resonant current, is no longer true in this range. Even worse, the distortion of resonant current will be more complex in experiment, because of some parasitic components in resonant tank. Some oscillation between parasitic and resonant components occurs in this range. The resonant current is observed with not negligibly distorted in the experiment as illustrated in Figure 4.4.

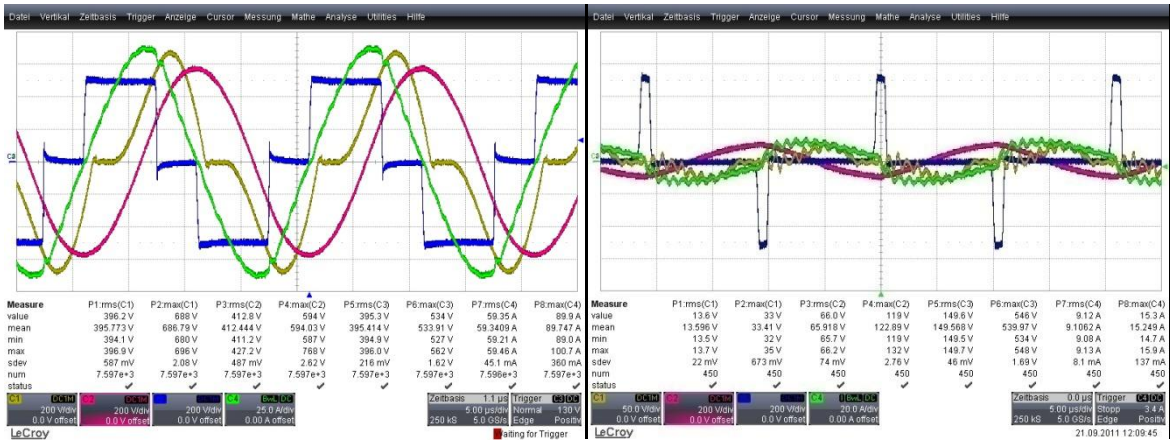


Figure 4.4: The distortion of resonant current at low-duty-ratio, $u_{AB}$ (blue), $i_{Ls}$ (green), $u_{Cs}$ (red) and $u_{Cp}$ (yellow)

The second part of verification is focusing on the small-signal model. The continuous small-signal model in Section 4.2 is used to calculate the transform function at operating point. For simulation and experiment, an extra AC voltage source is added into the input signal, generating the small perturbation. By measuring the same AC frequency components of output voltage, one point of the Bode diagram is drawn. As the frequency of the input voltage varies, the magnitude and the phase of the AC output voltage vary, too. By connecting these points, a Bode diagram is illustrated as the Figure 4.6.

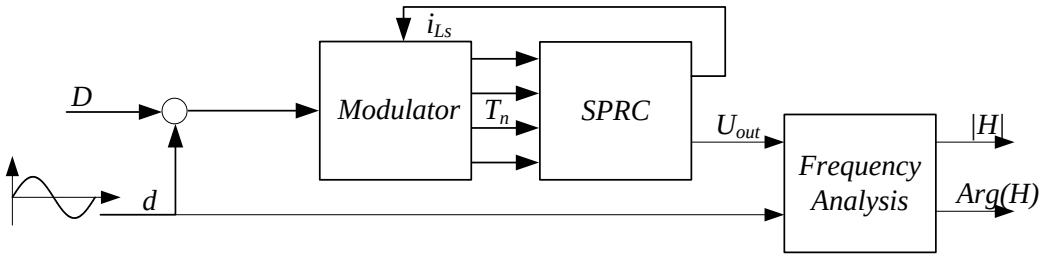



Figure 4.5: Structure of small-signal model measurement in simulation and experiment

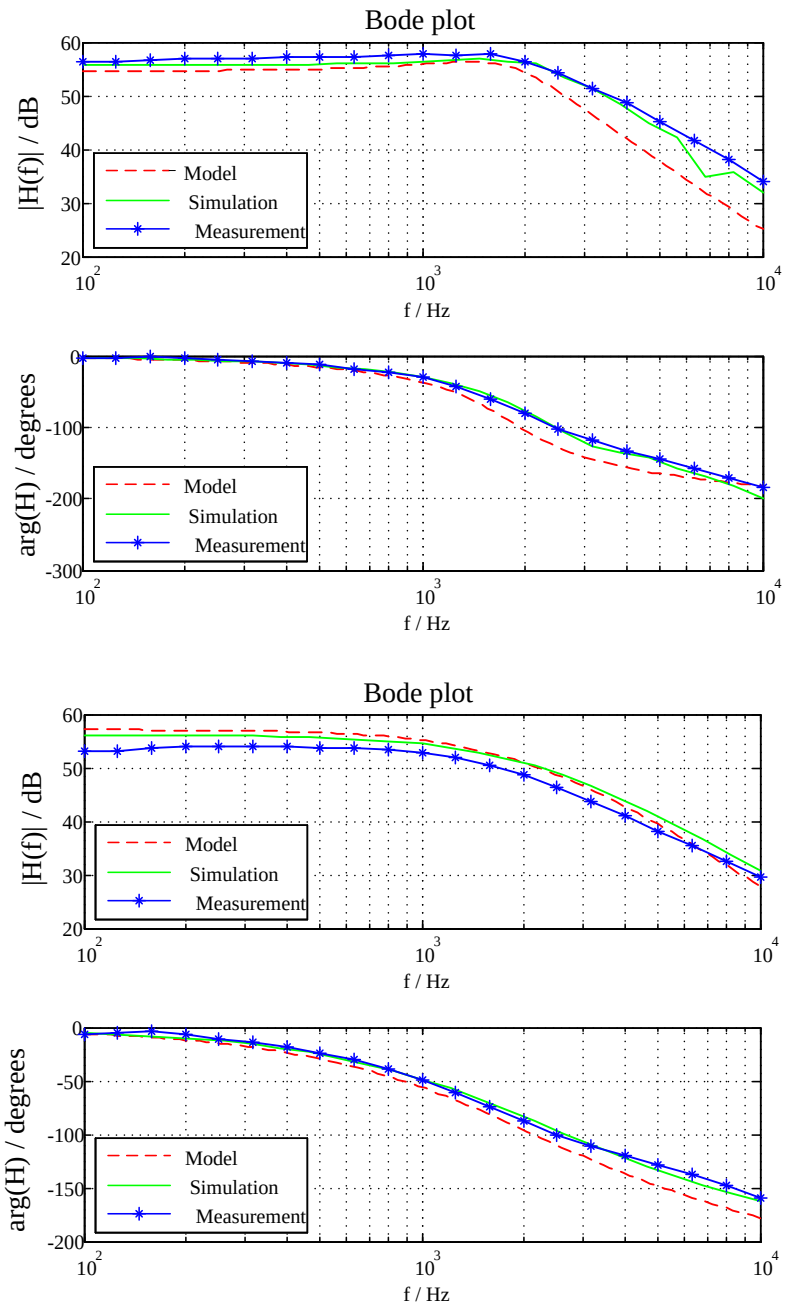



Figure 4.6: Verification of small-signal model in simulation and experiment:

The experiment measurement of SPRC-OM uses the frequency analyser. It generates the extra AC source and analyse the output voltage, directly give the Bode plot in frequency domain. The simulation uses the same essence. Only the AC source are designed in Simulink and the frequency analysis are held in Matlab®. The Bode plot of small-signal model is directly deduced from the matrix, using the Control Toolbox in Matlab®.

Figure 4.6 gives the result of small-signal model verification. The transfer function of this measurement is from the duty ratio to output voltage. The top two figures are measured at the operating point $R_L = 3.87\Omega$, $D = 0.5482$, which is in DVM mode. The lower two figures are measured at the operating point $R_L = 8.99\Omega$, $D = 0.4761$, which is in CVM mode. As a simplified fourth-order small-signal model, the HSD model is accurate in the low-frequency range and has some error in the high-frequency range. The small-signal model of SPRC-LC-OM still has room for further improvement.

## 4.5 Summary

In this chapter, novel modelling approaches of SPRC-LC-OM are proposed, including the continuous models and half-cycle sampling discrete (HSD) models. The derivation process starts with some basic assumptions and a continuous model with fast-changing state quantities. The half cycle is utilized as the base period for analysis. By assuming constant or interpolated state variables in the half cycle, a slowly-changing continuous model is derived. By linearizing and perturbing the nonlinear model, a small-signal model is obtained.

Afterwards, the novel HSD model for SPRC-LC-OM is derived as mentioned in Chapter 2. Nonlinear and linear HSD models are given, corresponding to the continuous large- and small- signal models. In practice, the nonlinear model is iterated to predict the steady-state operation points. Linear HSD model are used to give the stability and transfer function of the SPRC-LC-OM. The essence of the continuous model is mathematically the same as the HSD models. HSD model gives the simplest expression of SPRC-LC-OM, considering the variation of switching frequency.

Circuit simulations and experimental measurements are undertaken to validate these models. HSD model has good steady-state accuracy in a wide load and in middle voltage range. The small-signal model also gives an accurate approach with low calculation complexity. Because

the three coefficients of the parallel-capacitor voltage $u_{Cp}$ can be realized in look-up tables, these models do not contain transcendental functions and do not need numerical solutions. By analysing these models by time-complexity algorithm from computer science, HSD models are proved to have the balanced performance with complexity and accuracy.

Some assumptions have to be made in order to simplify the derivation procedure. Similar as improved steady-state model, the first-order Fourier coefficients are used to describe the distorted waveform. Furthermore, the state variables are assumed as being constant in the half cycle. These two assumptions lead to some errors of the HSD model, especially in low-duty-cycle range. In future research, it might be interesting to analyze the effects of high-order harmonics in the resonant-tank quantities. In the chapter, high-order harmonics have to be ignored because a model of low complexity is required.

# 5 Modelling and implementations of optimized modulation strategy

As the second block of the controlled SPRC system, the function of the modulator is to receive the control signals from the controller and to generate and to send the gate signals to the converter, as illustrated in Figure 2.2. There are three major modulation strategies in SPRC control: PFM, PFWM and OM. There are two different implementations of OM: analog-digital hybrid implementation and full-digital implementation. Full-digital implementation is first proposed in my publication [TCS12]. Both implementations will be introduced in this chapter.

The dynamic behaviour of the modulators is normally ignored in state-of-the-art modelling approaches, because switching frequency is supposed to be adjusted much faster than output voltage in real circuit. However, the real switching frequency has a transient adjusting process, which is an factor and should be modelled in SPRC system. The dynamic modelling of modulators will also be introduced in this chapter.

The operation principle of OM is introduced first with an ideal modulator in Section 5.1. After that, two different implementations of OM are introduced. The most significant part of the modulator, the saw-tooth generator, is introduced with its hybrid and digital implementations. In Section 5.2, the state machine is introduced as the common component of both implementations. With the help of HSD modelling techniques, the dynamic behaviour of modulators is appropriately modelled and concisely expressed in Section 5.3. Finally, a short summary about the modulators is given in Section 5.4.

## 5.1 Optimized modulation strategies of SPRC

Among three major modulation strategies, PFM and PFWM are regulated according to the external switching frequency signals given by the controller. They normally use the clock signal of digital device to generate time periods with desired length. As the crystal oscillator of micro-controller is stable and has very high frequency, it has no problem for accurate pulse width in PFM and PFWM.

The core algorithm of OM is to generate a synchronized square waveform with desired duty-ratio value. This is the major challenge encountered in the implementing OM strategy. In OM, three major blocks and the signals of SPRC system are illustrated in Figure 5.1. The signal of switching frequency is feed back to the modulator when resonant current is measured. For the modulator, the input signals are duty ratio from the controller and the resonant current value from the converter.

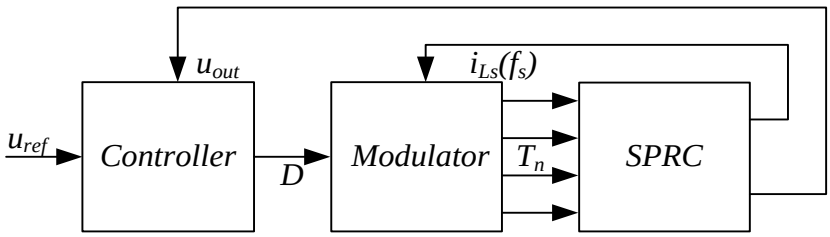



Figure 5.1: Control structure of SPRC-LC-OM

As mentioned in chapter 2, the direct idea for OM implementation is to generate the synchronized saw-tooth waveform. By comparing the duty ratio with this synchronized saw-tooth waveform, the desired pulse length square waveform will be generated. In order to generate the synchronized saw-tooth signal, three different modulation strategies are mentioned in the following, from ideal modulator to real modulators.

### 5.1.1 Ideal modulator and the operation principle of optimized modulation

The ideal modulator is operated fully synchronized with the resonant current as illustrated in Figure 5.2. In the period $t_{h,n}$, the saw-tooth signal rises with the slope $s_n$ and is reset when the resonant current is crossing zero. At the peak point of the saw-tooth signal, the amplitude exactly reaches the expected value where $A_n = A_O$. With this saw-tooth signal compared to the denormalized duty ratio $DA_O$, the modulator signal will be generated ideally.

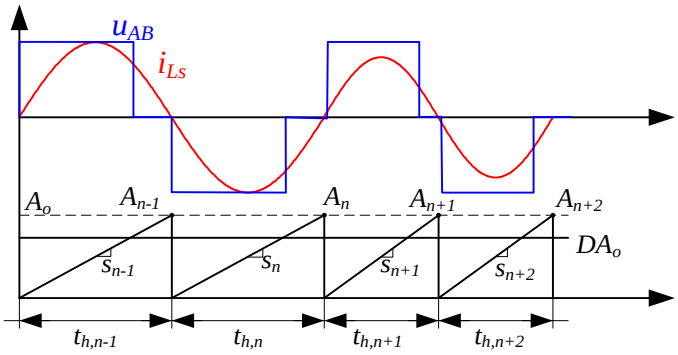



Figure 5.2: The ideal OM modulation strategy

There are four function blocks in the modulator structure, zero-crossing detection (ZCD), saw-tooth generator (STG), comparator and state machine, as illustrated in Figure 5.3. In this section, ZCD, STG and comparator are introduced. The state machine will be introduced in section 5.2.

The basic operation principle is introduced first. The zero-crossing instants of resonant current are detected from the feedback of resonant current. A narrow pulse signal, called reset pulse (RP), is generated each time the zero-crossing of resonant current occurs. The reset pulse is used to reset the saw-tooth signal in STG. STG employs the slope to generate the desired saw-tooth signal. The modulator adjusts the slope of saw-tooth signal in order to make sure that the amplitude of the saw-tooth signal is constant ($A_n = A_O$) not only in steady

state but also in transition. In ideal modulator, the amplitude can be perfectly controlled, so there is no distortion and deviation in the modulator.

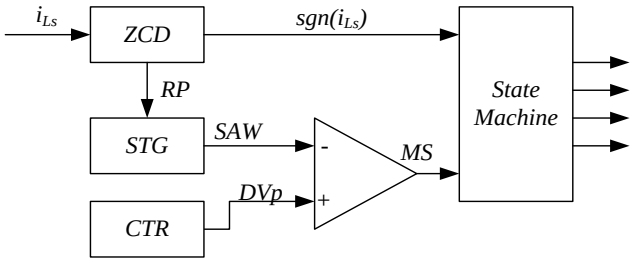



Figure 5.3: Block diagram of ideal OM modulation

It is clear that the ideal modulation cannot be achieved physically. The reason is that the modulator must predict the length of the half cycle $t_{h,n}$ at the beginning of every half cycle. If the exactly predicted half cycle length $t_{h,n}$ is obtained, the slope of saw-tooth can be calculated as $s_n = \mathrm{A}_0 / t_{h,n}$ to ensure the expected amplitude $\mathrm{A}_0$ at the end of each half cycle. However, the external conditions, e.g. the load resistance or the input voltage, have affects to the SPRC resonant tank. Half cycle length $t_{h,n}$ might be changed in its own half cycle period. Therefore, the length of half cycle $t_{h,n}$ is not a determined value and cannot be predicted at the beginning point as presumed.

As an ideal modulator is not achievable in practice, real implementations of OM are these two different methods: hybrid modulator and digital modulator. The operation principle of OM modulator is similar to ideal modulator. These two implementations differ slightly in the saw-tooth generation from the ideal modulation strategy.

### 5.1.2 Hybrid implementation of optimized modulator

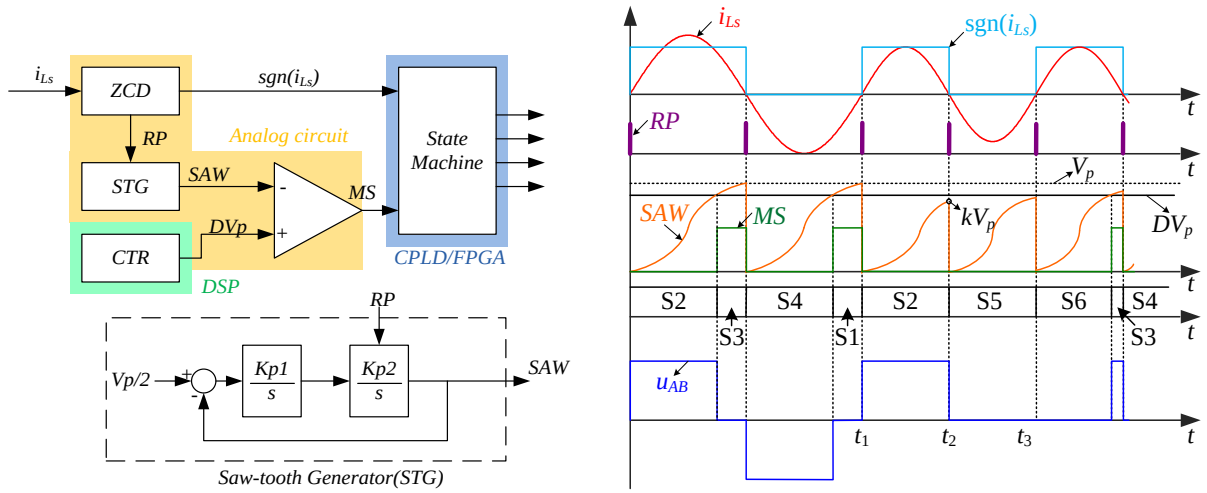
In an analog-digital hybrid modulator, ZCD, STG and comparator are implemented in analog circuits. The state machine is designed using a FPGA or CPLD as its hardware. The control structure and the analog-digital implementation of the hybrid modulator are illustrated in

Figure 5.4(a). Instead of the abstract expected amplitude ($A_0$), the analog circuit utilizes the voltage value ($A_0 = Vp$) as the real amplitude of saw-tooth signal. The duty ratio *D* is also denormalized to the corresponding voltage value $DVp$.

If the switching frequency step occurs at the time instant $t_1$ as illustrated in Figure 5.4, the saw-tooth signal is reset before it reaches the expected amplitude at the time instant $t_2$ . The slope of the saw-tooth is adjusted by an integral controller, which is illustrated in the bottom of Figure 5.4(a). The measured amplitude of the saw-tooth signal is compared with the reference voltage ($Vp/2$) and the integrator accumulates the compared result. The slope of the saw-tooth increases during several cycles until the amplitude reaches the expected value again.

In control theory, there is an inner control loop in the slope adjusting process. In the hybrid modulator, the adjusting function is realized by two integrators. The structure of its saw-tooth signal generator is illustrated at the bottom of Figure 5.4 (a). The first integrator $K_{p1}$ compares the reference voltage ($Vp/2$) with the feedback of the saw-tooth signal, giving the slope value. The second integrator $K_{p2}$ generates the saw-tooth signal until it is reset by the RP signal.

In the hybrid modulator, the saw-tooth signal is a clipping of the sine waveform, as it is generated by two integrators. These saw-tooth waveforms might be distorted when the integral parameters are large. There is a trade-off between this distortion of the saw-tooth waveform and the adjusting dynamics of the STG. The distortion is illustrated exaggeratedly in Figure 5.4(b). In addition, the hybrid modulator also requires highly reliable RP signals. If the RP signal is missing or repeated at the zero-crossing point, the integrator will receive a false amplitude signal with a big deviation, leading to a wrong slope signal in several half cycles.




(a) (b)

Figure 5.4: Block diagram and waveform of the hybrid OM modulator

### 5.1.3 Digital implementation of optimized modulator

In a full-digital implementation, ZCD, STG and comparator are all implemented in the FPGA. The current direction signal $sgn(i_{Ls})$ and the $RP$ signal are generated directly by a digital comparator in the ZCD block. The structure of the digital modulator is illustrated in Figure 5.5(a). The saw-tooth signal is generated by a digital counter and reset by digital reset signal RP. Hence, it has a constant slope and a variable amplitude when switching frequency varies. At the beginning of period $t_{h,n}$, the duty ratio $D$ ($0 < D < 1$) is multiplied with the amplitude of the saw-tooth signal in the last period, as illustrated in Figure 5.5 (b).

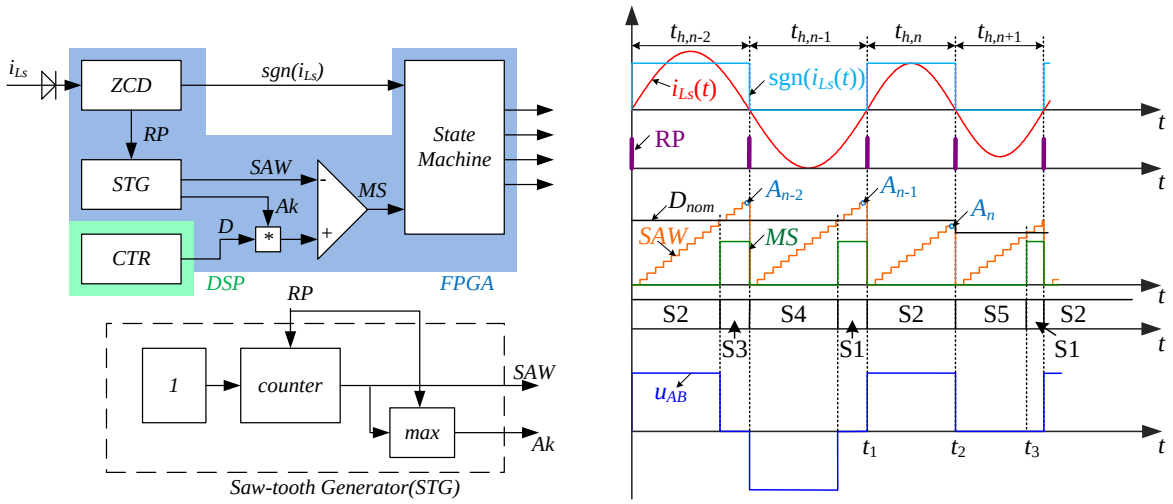
$$D_{Nom,n} = DA_{n-1} \tag{5.1}$$

The transformed duty ratio contains the information of the delayed saw-tooth amplitude. In control theory, it can be considered as one half-cycle delay in control loop. When switching frequency is changing at time instant $t_1$, the normalized duty ratio is the same as it contains the amplitude of last period $A_{n-1}$. In the next half-cycle period, the normalized duty ratio is reduced at time instant $t_2$.

Both hybrid and digital modulator produce slight errors in modulation process. The adjusting process of slope or the transformation of duty ratio is a factor that influences the dynamic

performance. In steady state condition, a hybrid or digital STG do not show problems because the amplitude of nearby periods is almost the same. But when the switching frequency varies in transition, the real STG leads to some deviations. In Figure 5.4 and Figure 5.5, the waveform of $u_{AB}$ is clearly not desired after time instant $t_1$.

In addition, the missing or repeated RP signal is also a problem in digital modulation. The counter will obtain a double amplitude value if one RP signal is missing. However, because most FPGA boards offer a lot of unoccupied designable digital units, the modulation algorithm will be further modified and optimized in the following sections.




(a) (b)

Figure 5.5: Block diagram and waveform of full-digital OM modulator

### 5.1.4 Time compensation in digital implementation

In the design process of the OM, three major time delays shall be considered: time delay of the measurement circuit ($T_{d1}$), dead time of the inverter ($T_{d2}$) and rise time of the transistor gate-emitter voltage ($T_{d3}$), as illustrated in Figure 5.6 (a). The total time delay is the sum of these three and is represented by the symbol $T_d$. The total time delay can be compensated by introducing an additional duty ratio $D_p$ ($0 < D_p < 1$). The duty ratio is slightly reduced from the amplitude of saw-tooth signal in the last period.

$$D_{p,n} = A_{n-1} - sT_d$$

where the parameter *s* represents the slope of saw-tooth. The normalized duty ratio is also slightly smaller as expressed below.

$$D_{nom,n} = D_n A_{n-1} - sT_d$$

Instead of the modulation strategy that is mentioned below, the modulated signal is generated between the time instants $s = D_1$ and $s = D$. As illustrated in Figure 5.6(b), the gate signal $T_1$ is reset at the time instant $s = D_1$. After the dead time $T_{d2}$, the gate signal $T_2$ is set. The gate signals are generated before the zero-crossing instant. Hence, the transistor begins to conduct exactly at the time instant of current zero-crossing, as illustrated in Figure 5.6(b). [TCS12]

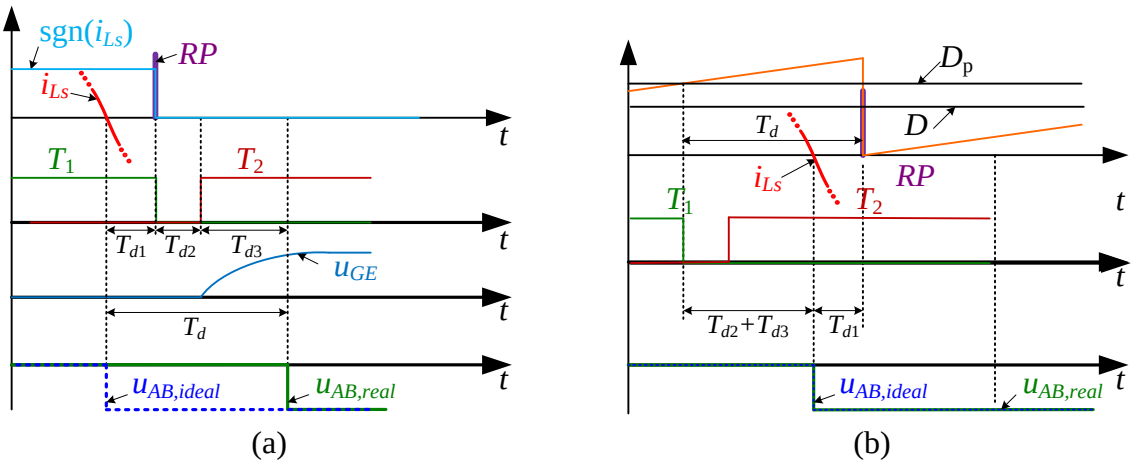



Figure 5.6: Work principles of the time delays compensation

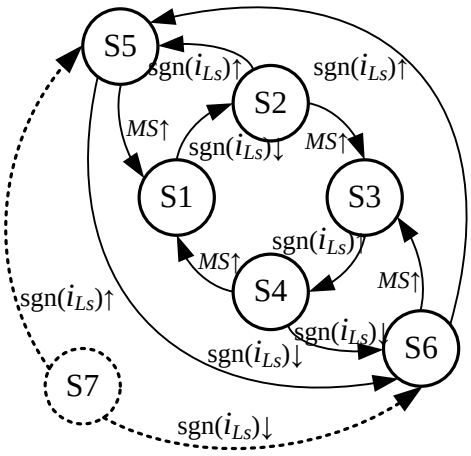
## 5.2 State machine

### 5.2.1 Design of state machine

In the OM modulator, ZCD, STG and comparator generate the modulated signal $MS$ and the current-direction signal $sgn(i_{Ls})$. These signals are sent towards the state-machine to generate the transistor gate signals ($T_n$, $n$ =1, 2, 3, 4). The state machine is mainly designed

for proper switching sequences in order to prevent a short circuit or any other damage to the transistors. The states and conditions of the state machine are illustrated in Figure 5.7. [TCS12]

The operation modes of the state machine are normal condition, protection condition and start-up condition. In normal condition, the operating state circulates in the loop of the normal states S1, S2, S3, and S4. The waveform of normal condition is illustrated before $t_2$ in Figure 5.4(b) and before $t_1$ in Figure 5.5(b). Normal states generate width-modulation signals $MS$ synchronized with the resonant current in steady state. If the resonant frequency has a sudden and substantial change, such as $t_2$ in Figure 5.4 (b) and $t_1$ in Figure 5.5 (b), the state-machine goes into the protection states (S5, S6), turns off the ZVS leg and keeps the ZCS leg freewheeling, until the next rising edge of the $MS$ signal appears. During the protection period, the full-bridge output voltage is kept at zero while the filter output voltage falls. The operating state of the state-machine is highlighted with red lines in Figure 5.8. [TCS12]




| State | T1 | T2 | T3 | T4 |
|---|---|---|---|---|
| S1 | ON | OFF | OFF | ON |
| S2 | OFF | ON | OFF | ON |
| S3 | OFF | ON | ON | OFF |
| S4 | ON | OFF | ON | OFF |
| S5 | ON | OFF | OFF | OFF |
| S6 | OFF | ON | OFF | OFF |
| S7 | OFF | OFF | OFF | OFF |

Figure 5.7: State machine of the OM control unit

It is important to point out that in protection mode the system is not controllable. The protection mode occurs frequently with a large value of duty ratio input, as the trigger

condition is $A_n < DA_{n-1}$. In a close-loop controlled system with controller and modulator, the protective intervention occurs as a big step up of the reference voltage. When the state machine changes to the protection mode, the output voltage becomes uncontrolled and continues to reduce. The controller will give an even larger duty ratio to adjust the output voltage. Hence, the close-loop system will be locked in the protection mode. The solution of this problem will be given in Chapter 6.

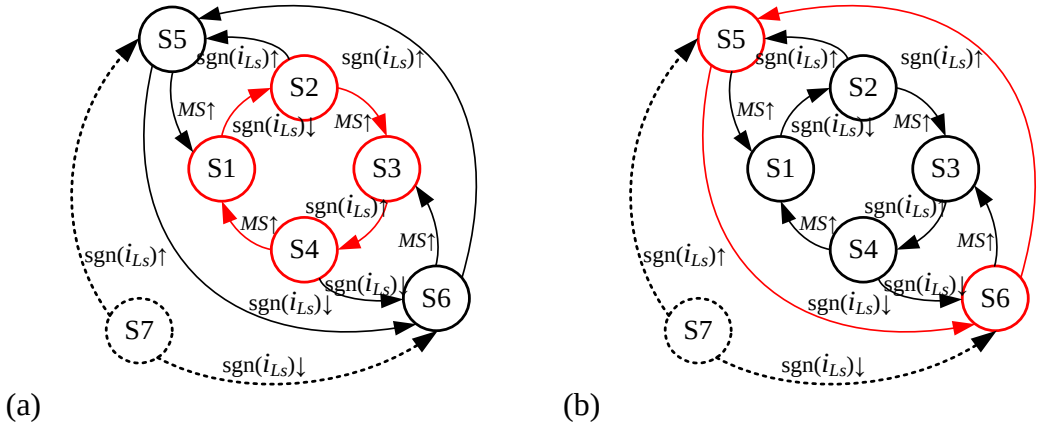



Figure 5.8: Circulating loop of normal condition (a) and protection condition (b)

### 5.2.2 Special operation mode for start-up phase

In order to further reduce the turn-off losses of the transistors in the ZVS-leg, capacitive snubber is usually desired. However, the capacitive snubber can only be applied if the ZVS condition is guaranteed in all operation modes. Since the snubber capacitors are pre-charged by the DC-link voltage to the value $U_{dc}/2$, a special operation mode of the state machine is required. An additional state S7 is added in the state machine as the dashed lines in Figure 5.7. [TCS12]

An example of the start-up operation mode is illustrated in Figure 5.9. Before start time $t_0$, the converter is disabled and the state machine keeps its state at S7. All transistors are off and

the voltage on the snubber capacitors is half of DC-link voltage $U_{dc}/2$. When the enable signal is set at time $t_0$, the converter starts working. Due to the measurement error of the current sensor, the direction signal $sgn(i_{Ls})$ oscillates even though there is no resonant current in power circuit. Once the zero-crossing occurs, $sgn(i_{Ls})$ begins to fall at the time instance $t_1$. The falling edge of $sgn(i_{Ls})$ changes the converter state from S7 to S6 and turns on the transistor $T_2$. During the time interval $t_1 < t < t_2$ the upper snubber capacitor $C_U$ is charged and the lower snubber capacitor $C_D$ is discharged. Because of the charging process, a small voltage pulse with the voltage $U_{dc}/2$ is given to resonant tank, which generates the first measurable resonant current during $t_1 < t < t_3$. At the end of this half cycle, the resonant current is reversed and the state changes from S6 to S5. During the time interval $t_3 < t < t_4$, $C_U$ is discharged and $C_D$ is charged. This generates more small voltage pulses with the value of the DC-link voltage $U_{dc}$. At time instance $t_4$ the charging and the discharging are completed. With the length information of the last half cycle, the transformed duty ratio $DA_{n-1}$ is given. The modulated signal MS rises at time $t_5$ and the state converts to S1. The start-up phase is completed and the state machine is cycling in normal condition after time $t_5$. [TCS12]

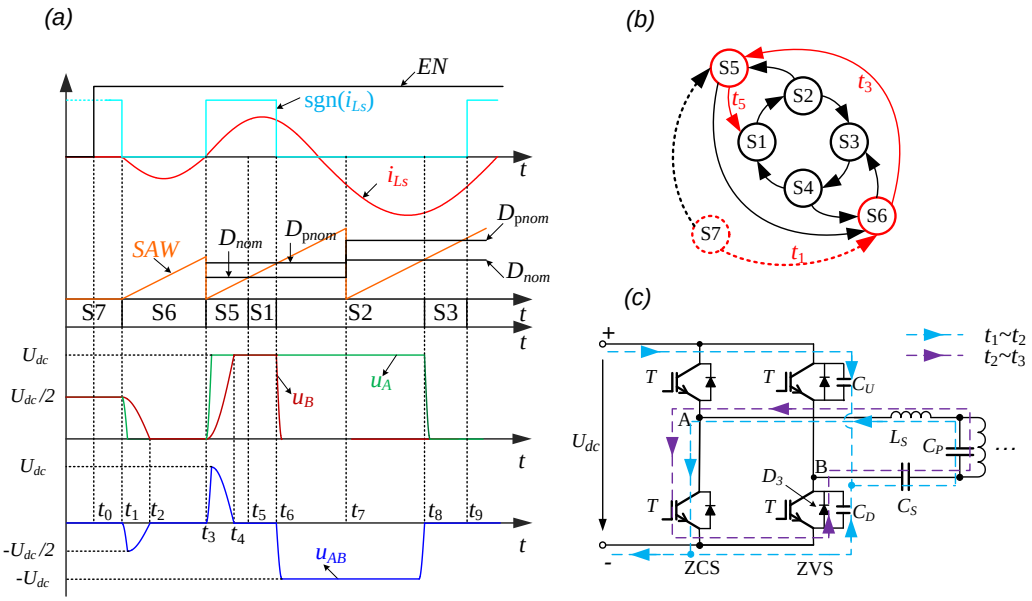


Figure 5.9: Waveforms of hybrid and digital modulator at start-up operation

### 5.2.3 Experimental results of digital OM modulation

The digital OM modulator is implemented on a dSPACE® rapid prototyping control system (RCP), which includes a processor board and a FPGA board. Briefly, the processor board measures the output voltage, performs the control algorithm and outputs the duty ratio *D*. The full-digital OM modulator is implemented on the FPGA board, which reads the duty ratio value from the processor and generates the gate signals. The detail information of hardware setup will be given in Chapter 7. [TCS12]

Measured waveforms in start-up phase and in steady-state operation are given in Figure 5.10. Resonant current $i_{Ls}$ and inverter output voltage $u_{AB}$ are directly measured in the power circuit. Enable signal and converter states are output from the dSPACE RCP via a digital-analog converter within the FPGA card. There is a slight delay of these signals due to the digital-analog conversion. Measurement results show that all functional blocks of the OM control unit are successfully implemented. As illustrated in Figure 5.10, the start-up process agrees positively with the theoretical analysis in Section 5.2.2. [TCS12]

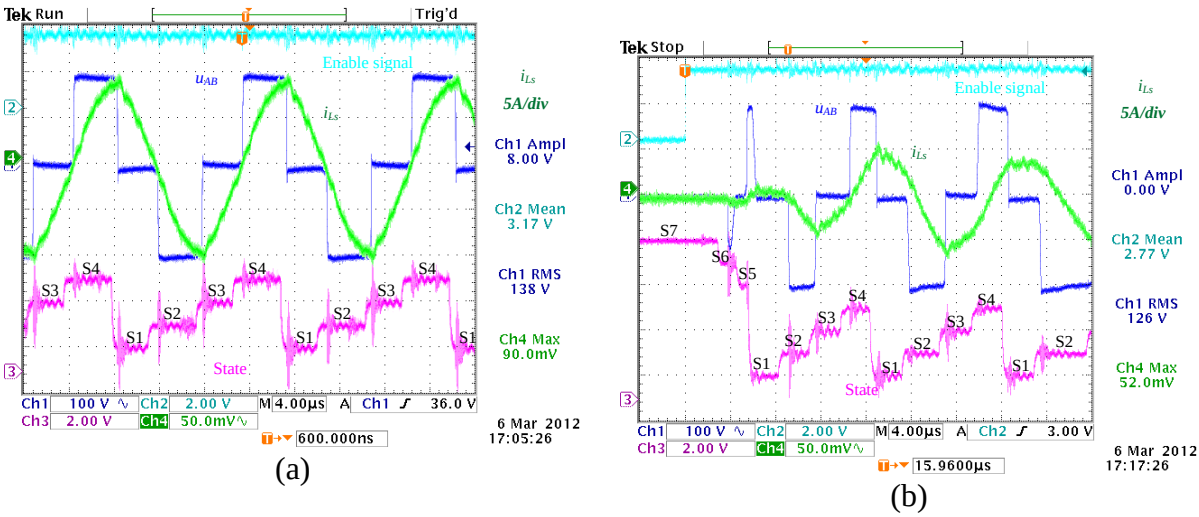



Figure 5.10: Experiment results under steady-state operation (a) and in starting phase (b)

## 5.3 Modelling of modulators' dynamic behaviour

As mentioned in Section 5.1, the hybrid and the digital implementation of OM has different dynamic behaviour during transitions. The real effective value of the duty ratio is different from given duty ratio, if the real amplitude does not equal the expected value $A_O$. There is a conversion between the effective duty ratio and the given duty ratio. In SPRC-LC-OM system, the modulator is also a significant part of the dynamic model.

Until now, one published work [CTF+13] takes the modulator dynamic behaviour into consideration, using time-domain analysis to deduce the model. It is clearly an accurate approach, but it is really complicated and time-consuming. With the help of the HSD system, the modelling of modulation can be expressed briefly.

All three implementations of OM are considered in this modelling approach, including ideal, hybrid and digital modulator. First, the ideal OM modulator is modelled. The real effective duty ratio equals the given duty ratio in any condition.

$$D_{real,n} = D_n \tag{5.2}$$

For hybrid implementation of OM, the slope of the saw-tooth signal is adjusted by the integral controller. Assuming the integral gain of the inner loop is $K_{p1}$ and the expected amplitude is $A_O$, the slope is expressed discretely as

$$s_n = s_{n-1} + K_{p1}(A_O - A_{n-1}) \tag{5.3}$$

The normalized or active duty ratio is expressed as

$$D_{real,n} = \frac{\pi}{\omega_n} D_n s_n \quad (0 < D_{nom,n} < 1) \tag{5.4}$$

The amplitude $A_n$ is given as

$$A_n = \frac{\pi}{\omega_n} s_n \tag{5.5}$$

Suppose the transition starts at one steady-state operating point when $s_0 = A_O\omega_0/\pi$. Then insert (5.5) into (5.3) and it gives

$$s_n = (1 - K_{p1}A_O\frac{\pi}{\omega_n})s_{n-1} + K_{p1}A_O \tag{5.6}$$

The digital implementation of OM also adjusts the saw-tooth waveform in dynamics. The duty ratio $D$ is multiplied with the former amplitude of saw-tooth waveform.

$$D_{real,n} = \frac{A_{n-1}}{A_n}D_n \ \ (0 < D_{real,n} < 1) \tag{5.7}$$

For the digital modulator, the amplitude is inversely proportional to the switching frequency $\omega_n$. The real duty ratio then gives

$$D_{real,n} = \frac{\omega_n}{\omega_{n-1}}D_n \ \ (0 < D_{real,n} < 1) \tag{5.8}$$

Utilizing the nonlinear HSD model as an example, SPRC-LC-OM with the hybrid implementation is actually a fifth-order nonlinear system. The iterative equations do not include only the HSD model of the SPRC-LC-OM, (4.46) to (4.49), but also the adjusting process of the hybrid modulator, (5.6). As there is a controlled slope signal in the modulator, it should be considered as an extra state in the system.

In the modelling process, it also shows that the dynamic of the modulator is an important factor in the SPRC system. If the modulator is designed inappropriately, the dynamic behaviour of the SPRC-LC-OM would be deteriorated. In the control design of the SPRC-LC-OM, the fourth-order model is extended to the fifth-order model by the integral slope controller, as the plant in discrete domain.

## 5.4 Summary

In this chapter, the modulator in the SPRC-LC-OM system is discussed. With the development of digital devices, the OM modulator can be implemented in a fully digital

manner in FPGA. In this chapter, three different implementations of OM are introduced, ideal, hybrid and digital implementation. The latter two differ slightly from the ideal modulator, especially in the STG. By analyzing the adjusting process of the STGs, the three implementations are modeled in HSD system. The influence of slope adjustment has been ignored in previous literature. The exact modeling of the modulator helps the precise control design.

With the designable calculation capability of FPGA board, some further development of OM modulator, e.g. the time compensation and start-up-phase control, are realized in digital implementation. The experimental results validate the successful modulation of the SPRC.

# 6 Pulse-width regulation and half-cycle-sampled discrete control

Due to the rapid development of digital devices, a high-performance FPGA boards have sufficient calculation capability for complex control algorithms and modulation strategies. State-of-the-art digital OM control, however, is mainly developed from digital OM control. Digital OM control normally uses the digital OM modulator and proportional-integral controller with fixed sampling step. The modulation strategy and the control algorithm can be discussed and improved in order to achieve a higher dynamic performance of SPRC-LC-OM system. In addition, digital OM control has some drawbacks in the control process. With these reasons, a novel control algorithm is proposed, designed and verified in this chapter. The novel controller is designed partly to overcome the drawbacks of OM control and partly to improve the dynamic performance. The experimental result validates the improvement of SPRC-LC-OM.

First, three major drawbacks of the original digital OM modulator are given in Section 6.1. Two different improvements of the digital OM modulator are mentioned separately in Section 6.2 and Section 6.3. The HSD-PW control is implemented and modelled with HSD modelling techniques in Section 6.4. The close-loop control parameters are designed in Section 6.6 and validated in Section 6.7. Finally, a summary is given in Section 6.7.

## 6.1 Drawbacks of digital OM control

There are three major drawbacks of state-of-the-art digital OM modulator and controller. First, the output voltage is actually regulated by both duty ratio and switching frequency. In order to guarantee ZCS and ZVS in operating, the switching frequency is directly measured

from resonant-current feedback. This generates an uncontrollable inner loop in the control structure. The response speed of the inner loop affects the dynamic performance of the system as mentioned in chapter 5. In circuit simulation, this problem is not that obvious because the measurement of the resonant current is reliable and considered ideal. In practice, it is difficult to ensure the perfect waveform of resonant current.

This problem is even worse when the switching frequency is measured from the length of the half cycle. In the resonant converter with OM modulation, the feedback of resonant current is the weak point in regard of interference. This is because the measuring of switching frequency is dependent on the zero-crossing points of the resonant current. Small interferences in the current waveform will change the zero-crossing points. As mentioned in the chapter 5, the real duty ratio is recalculated with the switching frequency in digital OM modulator. Considering the switching frequency measurement with interference, the real duty ratio has some noise near its stable value. This is the reason why the output voltage is not stable at some operating points. The interference of the switching frequency, which brings some deviations in duty ratio and output voltage, should be added into consideration for control design.

Second, the controller cannot regulate the output voltage when the state machine is circulating in the protection states (S5, S6). In this protection period, the input duty ratio is not utilized in the modulator and the output voltage is not controlled by the controller. The feedback, however, still misleads the controller while the control algorithm furthermore gives the meaningless duty ratio. The problem has already been mentioned in Section 5.2.1. When the SPRC-LC-OM is operated with the duty ratio near the upper limit, the system will be locked in protection mode in transition.

Third, in all OM modulators, duty ratio and switching frequency are assumed to change slowly in transition. In the modulator, it is assumed that the control signals are almost steady in a half cycle. With rapidly-changing control signals, it is hard to point out the real effective value of the duty ratio, which is compared to the saw-tooth signal in the dynamic process. This leads to some difficulties in precise designing and debugging of the controller in hardware.

Because modulator and controller are designed to be implemented in the high-performance FPGA, complex controls can be realized with the sufficient calculation capability. Hence, a discussion about control and modulation methods is held to solve these problems.

## 6.2 Half-cycle-sampled discrete control (HSD control)

In order to perform with better dynamic in the SPRC-LC-OM system, the first attempt of the novel controller tries to increase the sampling frequency of the controller. Due to the basic concept of HSD, the package of modulator and converter can be considered as a HSD plant instead of a continuous system. Hence, the controller can also be designed on half-cycle sampling, which is called half-cycle-sampled discrete control (HSD control) in this dissertation. Because the OM modulator performs the half-cycle sampling behaviour, the highest and most effective sampling step of the controller is half-cycle period.

In order to fairly compare the different control algorithms, the output voltage is selected as the common control objective in this chapter. The proportional-integral (PI) controller is designed for different sampling steps and different control signals. The control structure of HSD control and original digital OM control is illustrated in Figure 6.1.

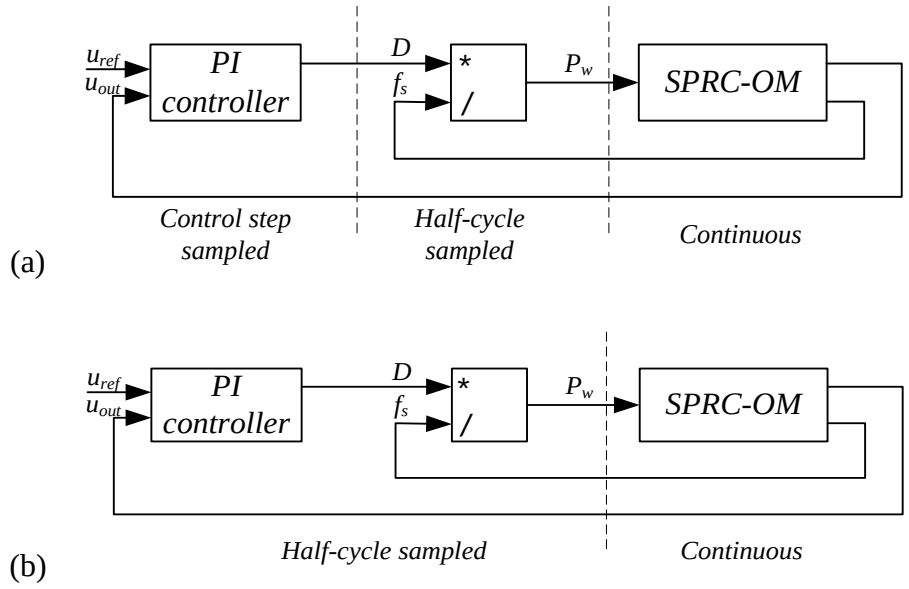



Figure 6.1: Sampling steps of OM control (a) and HSD control (b)

As illustrated in Figure 6.1, the HSD control contains a discrete PI controller in the system. Instead of a fixed-step control algorithm, the control algorithm is calculated once each half cycle. In practice, the control algorithm can be triggered by the RP signal from the modulation.

HSD control has two expected advantages compared to the fixed-step control algorithm. One is that the protection statue can be fed back to the controller, to eliminate the protection locking problem. The other advantage is the expected improvement in dynamic performance. The control algorithm is operated at twice switching frequency, which is normally higher than the sampling step in original digital OM control. The HSD controller is designed with HSD model of SPRC-LC-OM in Section 4.3. The design process of different controllers will be given in Section 6.6.

In the control theory, HSD control gives a simpler structure because the sampling delays are eliminated. The control algorithm is synchronized, so the control signals will be definite and clear. It solves the third problem of digital OM controller. Considering the calculation resources, HSD control algorithm asks for a higher requirement of hardware, but also

improves the dynamic performance. The implementation of HSD control is achieved in FPGA board, which will be introduced in Chapter 7.

By analysed in theory, HSD control can be one of the solution for digital OM control problems.

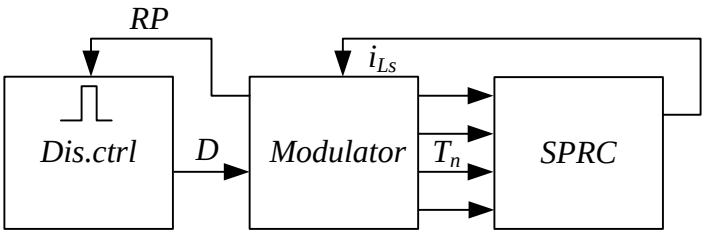



Figure 6.2: The structure of HSD control

## 6.3 Pulse-width regulation

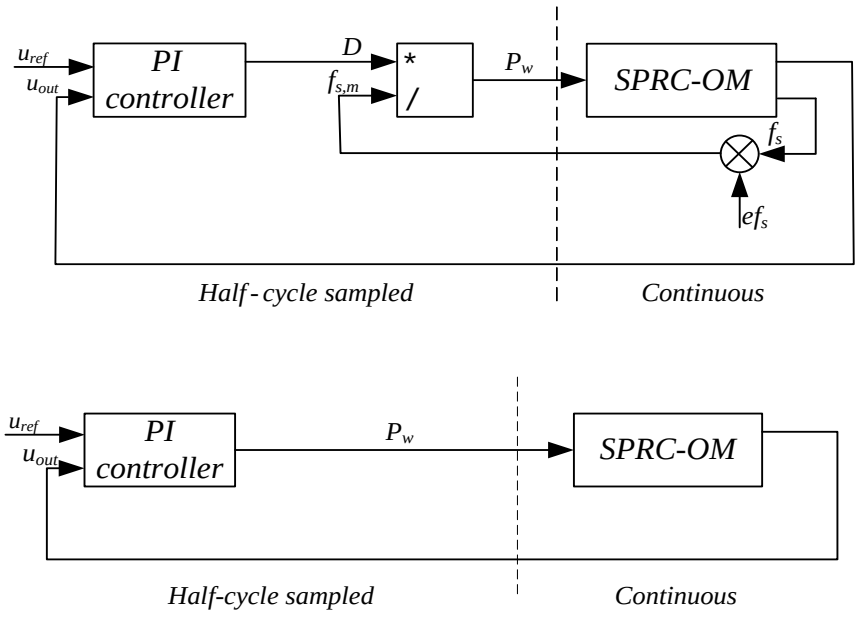



Figure 6.3: The basic structure of pulse-width regulation

In order to eliminate the inner loop of switching frequency, another attempt to modify the controller is called pulse-width regulation. In original digital OM control, the saw-tooth

generator and the comparator in the OM modulator are considered as generating a pulse with desired width. The width of the pulse is calculated as

$$P_w = Dt_h = \frac{D}{2f_s} = \pi\frac{D}{\omega} \tag{6.1}$$

where the parameter $P_w$ represents the pulse width signal. In pulse-width regulation, however, the width of the pulse is directly given by the controller. The structure of pulse width regulation is illustrated and compared to duty ratio regulation in Figure 6.3. The control signal is the pulse width, instead of the duty ratio.

Pulse-width regulation avoids introducing the measurement deviation of switching frequency into the control systems. As mentioned before, switching frequency is the signal most sensitive to interference, while the effective duty ratio is calculated with the switching frequency. There are actually two parts of the modulation strategy that are dependent on the zero-crossing measurement of resonant current. First, the reset pulse signal is created according to the zero-crossing instants, which decides the start and the end of each half cycle. Second, the length of a half cycle is measured from two adjacent zero-crossing points. The duty ratio signal is multiplied with the length of half cycle as the transformed duty ratio in modulation.

Pulse-width regulation obviously eliminates the deviation of period length measurement by directly giving the pulse width directly from the controller. The deviation from the first part is the reason of ZCS switching condition. If ZCS is to be guaranteed in the operation process, the first rule is not allowed to be broken. In the aspect of control structure, pulse-width regulation avoids the multiplication in the intermediate process. It obviously simplifies the control structure of the SPRC-LC-OM system. The digital OM utilizing duty ratio as the control signal is illustrated in Figure 6.4(a). The control strategy utilizing pulse-width regulation is illustrated in Figure 6.4(b).

The control structure of pulse-width regulation is illustrated in Figure 6.5. Pulse-width regulation mainly avoids the first drawback of digital OM controller.

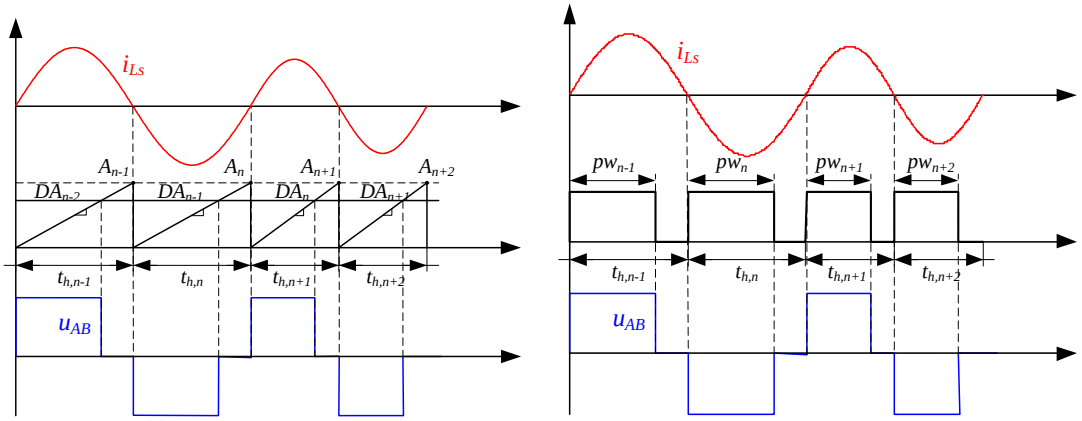



Figure 6.4: Comparison of two modulation signals: duty ratio (a) and pulse width (b)

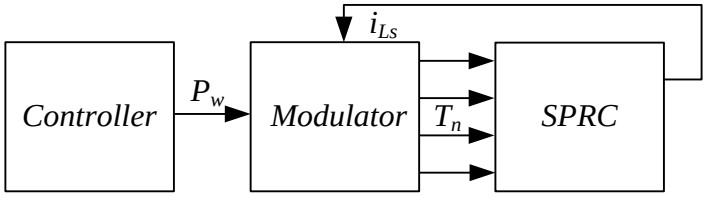



Figure 6.5: Structure of pulse-width regulation

## 6.4 HSD pulse-width control (HSD-PW)

Combining HSD control and pulse width regulation, a novel control algorithm is created, called HSD pulse-width (HSD-PW) control. The entire HSD-PW control structure consists of five blocks, including zero-crossing detection (*ZCD*), pulse-width generator (*PWG*), state machine, discrete controller and converter. The zero-crossing detection has the same function as the original block, generating reset pulse signal (*RP*) and resonant current direction signal ($sgn(i_{Ls})$).

In the HSD-PW control algorithm, the RP signal is utilized not only in the PWG but also to trigger the discrete control algorithm. Instead of duty ratio, the pulse-width signal ($P_w$) is

utilized as the control signal, generated from the controller and sent to the PWG. The discrete controller is synchronized with pulse-width generator and state machine. Based on the synchronization, an extra protection signal (*Prot.*) is fed to the controller to lock it when the state-machine is operating in the protection states. The structure of HSD-PW control is illustrated in Figure 6.6.

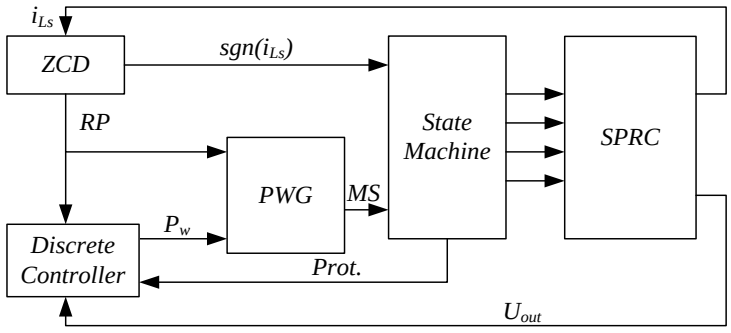
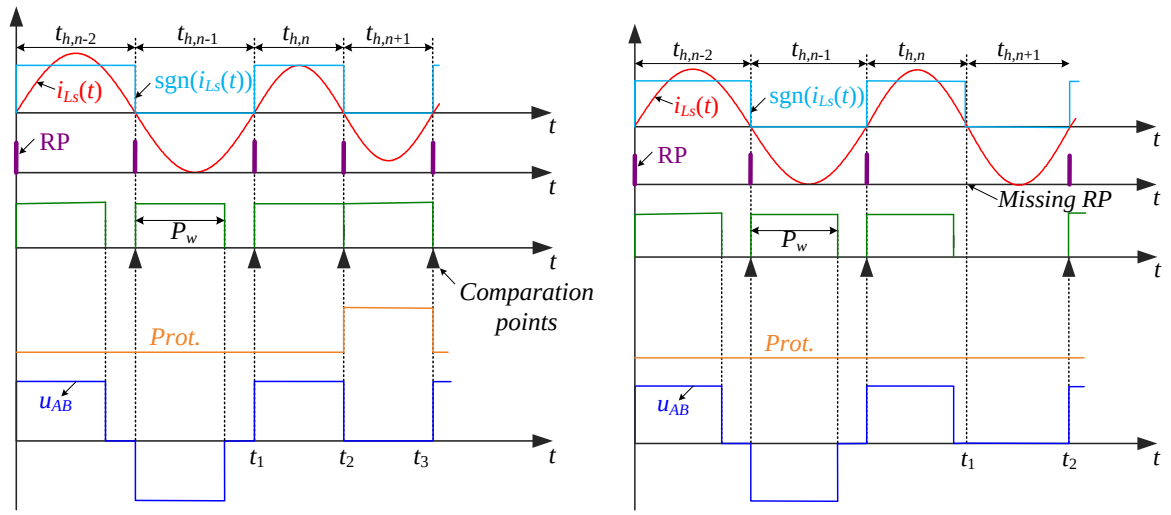



Figure 6.6: Structure of novel HSD control

The detection of the protection states in HSD-PW control also shows the differences from the original digital OM control. In digital OM control, the protection instant is detected when the rising modulated signal is missing in half cycle. At that time instant, the state machine makes the decision and the operating state is changed to the protection states. And the following several cycles will be influence until the state machine goes back to normal states. This detection and state transition has been introduced in detail in Section 5.2.

In HSD-PW control, the length of every half cycle is measured and compared to the desired pulse length. The protection is detected when the measured length is smaller than the desired pulse length. If protection is detected, the operating state goes into the protection states and the protection signal (*Prot.*) is set. In normal and protection conditions, the comparison is performed at the zero-crossing instants. If the length of the half cycle is longer than desired pulse width, the state machine will turn back to normal condition.




(a) (b)

Figure 6.7: Special control conditions of HSD-PW: (a) protection condition (b) RP-signal-missing condition

HSD-PW control has more tolerance to signal faults. If the *RP* signal is lost in the measurement, HSD-PW control ignores the missing half cycle and stops generating the voltage pulse in this period ($t_1 < t < t_2$ in Figure 6.7(b)). Because the length of the half cycle is measured between RP signals in digital OM, a missing RP causes an extremely large half cycle length measurement and then the control system is protected. HSD-PW is obviously a more robust control structure than digital OM.

Therefore, HSD-PW control shows some improvements in control structure and protection detection. First, deviations of the past periods have no effect on the modulation in the present period. It makes the controller more stable in transition and eliminates the interference of measurements. HSD-PW control is less dependent upon the accuracy of the zero-crossing measurement of the resonant current. Second, HSD-PW control makes the protection states robust and has more tolerance to signal faults. Third, three drawbacks of digital OM control is solved in HSD-PW control.

## 6.5 Modelling of pulse-width regulation

The transfer function of different control signals, including duty ratio and pulse width, can be analysed with HSD modelling techniques. The duty-ratio-regulated dynamic model has already been deduced in Chapter 4. The pulse-width-regulated model is deduced briefly in this section from the dynamic model of duty-ratio regulation.

The relationship of duty ratio and pulse width in large signal model is expressed as following,

$$D = \frac{\omega P_w}{\pi} \tag{6.2}$$

The differential of duty ratio can be expressed as,

$$dD = \frac{P_w}{\pi} d\omega + \frac{\omega}{\pi} dP_w \tag{6.3}$$

In the small-signal model, the small perturbation of the state variables is approximated by its differential. Hence, the perturbation of the duty ratio can be expressed approximately as

$$\widehat{D} = \frac{P_w}{\pi} \widehat{\omega} + \frac{\omega}{\pi} \widehat{P_w} \tag{6.4}$$

Inserting (6.4) into the small-signal model of duty ratio (4.40) and (4.41), the system matrix of the pulse-width-regulated dynamic model is obtained as

$$\boldsymbol{A}_{pw} = \boldsymbol{A} + \frac{P_w}{\pi} \boldsymbol{B} \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{6.5}$$

$$\boldsymbol{B}_{pw} = \frac{\omega}{\pi} \boldsymbol{B} \tag{6.6}$$

The system matrixes $\boldsymbol{C}$ and $\boldsymbol{D}$ are the same in the linear model with duty-ratio regulation. HSD model can also be applied to the pulse-width-regulated model. It can be utilized to design the closed-loop parameters of HSD-PW control. Here gives the expression.

$$\boldsymbol{A}_{d,pw} = \boldsymbol{E} + \frac{\pi \boldsymbol{A}_{pw}}{\omega} \tag{6.7}$$

$$\boldsymbol{B}_{d,pw} = \frac{\pi}{\omega} \boldsymbol{B}_{pw} \tag{6.8}$$

The transfer functions of pulse-width-regulated SPRC can be calculated with this linear model. Figure 6.8 illustrates the Bode plots with different control signals at one operating

point ($R_L$ = 3.87 Ω, D= 0.505). In order to compare the Bode plots, the transfer functions are normalized to give the same magnitude at the frequency point 1 Hz.

$$|H(f)|_{nom,pw} = \frac{\omega}{\pi} |H(f)|_{pw}$$

In the figure, it is clearly illustrated that pulse-width regulation qualifies with a wider bandwidth than duty-ratio regulation. In other words, pulse-width regulation clearly should have better dynamic performance than duty ratio regulation.

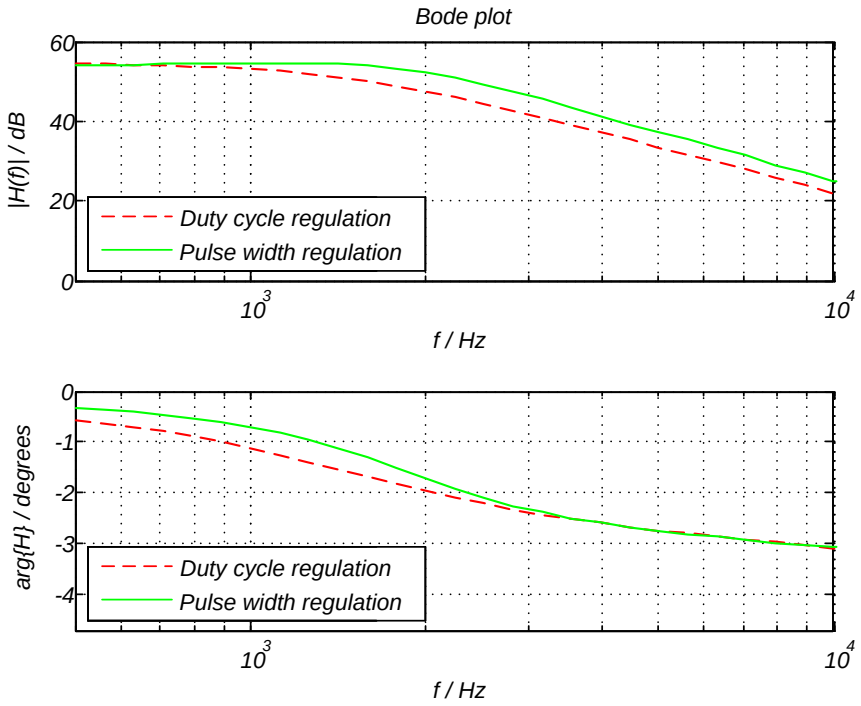



Figure 6.8: Bode plot with different control objectives: duty ratio regulation (red) and pulse width regulation (green)

## 6.6 Closed-loop design of duty-ratio regulation and pulse-width regulation

In order to make a fair comparison of the results, both digital OM control and HSD-PW control are designed with the same control structure, with a gain-scheduling proportional-

integral controller. The dynamic performance of closed-looped control depends on the parameters of the gain-scheduling controller. For both control algorithms, the design of the control parameters is calculated with the following principles.

**OM control**

For one operation point, the control parameters are designed as following. [Cao14]

First, the nonlinear system is linearized around the selected operation points. The small-signal models are given as in Section 4.3. With these small-signal models, the transfer function from output voltage to duty ratio is dependent on the operation point and the state variables. Second, the control parameters $K_{p,c}$ and $K_{i,c}$ are designed by means of standard frequency-domain design methods. The crossover frequency is selected as 4 kHz (about 10% of the minimum switching frequency). The phase margin is set to $30^{\circ}$. [Cao14]

All gain-scheduling parameters in the entire operation range are calculated with the linear approximation. The operation range is represented by some typical operation points. At each operation point, the design method mentioned below is applied and is calculated the continuous control parameters. In order to utilize the control parameters $K_{p,c}, K_{i,c}$ in the fixed-step discrete system, the forward differential conversion is applied to calculate the discrete control parameters $K_{p,d}$, $K_{i,d}$. The discrete control parameters on typical operating points are calculated and saved in a look-up table. The control parameters of certain points in the operation range are calculated by interpolation. [Cao14]

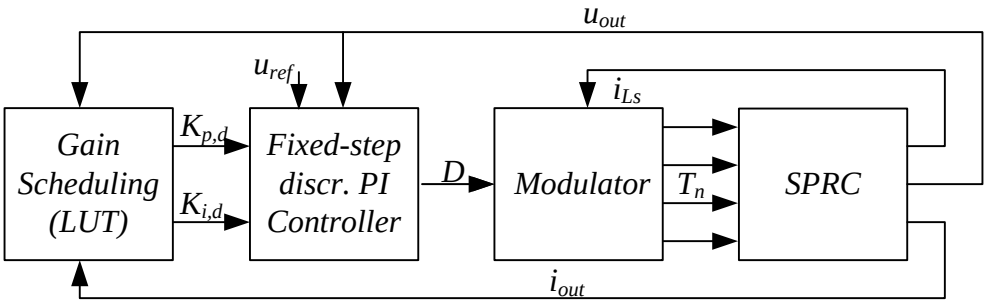



Figure 6.9: The control structure of gain-scheduling control with duty-ratio regulation

The structure of gain scheduling control is illustrated in Figure 6.9. There are some operation points with low dynamic performance, e.g. operation points with extremely large load resistance. The parameter design at these points is based on a smaller crossover frequency.

**HSD-PW control**

The design of the varying-step discrete controller has a similar process. Instead of a continuous model, the discrete control design is based on the linear HSD model deduce in last section. The structure of the plant is illustrated in Figure 6.10.

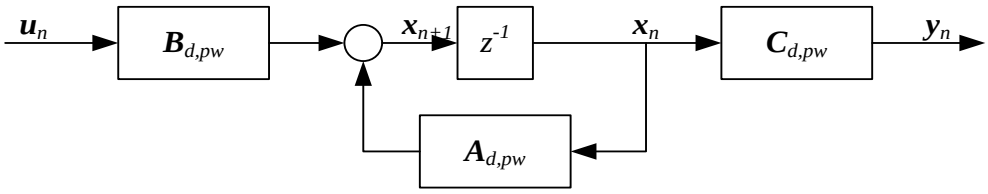



Figure 6.10: The control structure of linear HSD model

With the z-function, the discrete system is expressed by

$$H(z) = \frac{Y(z)}{U(z)} = \boldsymbol{C_{d,pw}}(z\boldsymbol{E} - \boldsymbol{A_{d,pw}})^{-1}\boldsymbol{B_{d,pw}}$$

For a certain operation point, the transfer function is directly calculated from the discrete plant. The parameters of the PI controller are designed as OM control in every typical operating point. The discrete control parameters are also calculated with the frequency-

domain analysis method. The control parameters at several operation points are shown in the following table.

Table 6.1: Controller parameters of different control algorithms: OM control and HSD-PW control

| **Operation point** | | **Duty ratio** | **OM control** | | **HSD-PW control** | |
|---|---|---|---|---|---|---|
| $u_{out}$ (V) | $i_{out}$ (A) | $D$ | $K_{p,d}$ (*$10^{-3}$ 1/V) | $K_{i,d}$ (*$10^{-3}$ s/V) | $K_{p,d}$ (*$10^{-3}$ 1/V) | $K_{i,d}$ (*$10^{-3}$ s/V) |
| 200 | 80 | 0.4824 | 1.21 | 0.392 | 3.80 | 2.52 |
| 400 | 80 | 0.7457 | 1.09 | 0.385 | 3.21 | 1.53 |
| 500 | 32 | 0.6155 | 0.562 | 0.235 | 2.53 | 1.30 |
| 500 | 64 | 0.8956 | 0.894 | 0.349 | 2.94 | 1.42 |

## 6.7 Simulation and experimental validation

The simulation is performed on a Simulink® platform with the Xilinx® FPGA toolbox as the first step of validation. Digital OM control and HSD-PW control algorithms are implemented to compare the simulation results. The switching frequency of HSD-PW control varies from 40 kHz to 70 kHz, depending on the operation point. The original OM control has the designed fixed-sampling frequency of 40 kHz.

Figure 6.11 illustrates the simulation results of HSD-PW control compared with original OM control. The reference voltage steps up from 50 V to 150 V with the load resistance 3.87 Ω. Because the two controllers have different control signals, the pulse-width signal is converted to the corresponding duty ratio by multiplying with the switching frequency in order to draw both control process in one figure. As illustrated in Figure 6.11, HSD-PW control (blue line) has an improved dynamic performance and yields shorter control settle-down time than the original OM control (green line). In order to show the dynamic improvement more clearly, HSD control utilizing duty-ratio regulation (red line) is also taken into the comparison. The HSD control has better dynamics than fixed-step control, because the sampling step is

obviously smaller. Pulse-width regulation has better performance because its bandwidth is higher than that of duty ratio regulation.

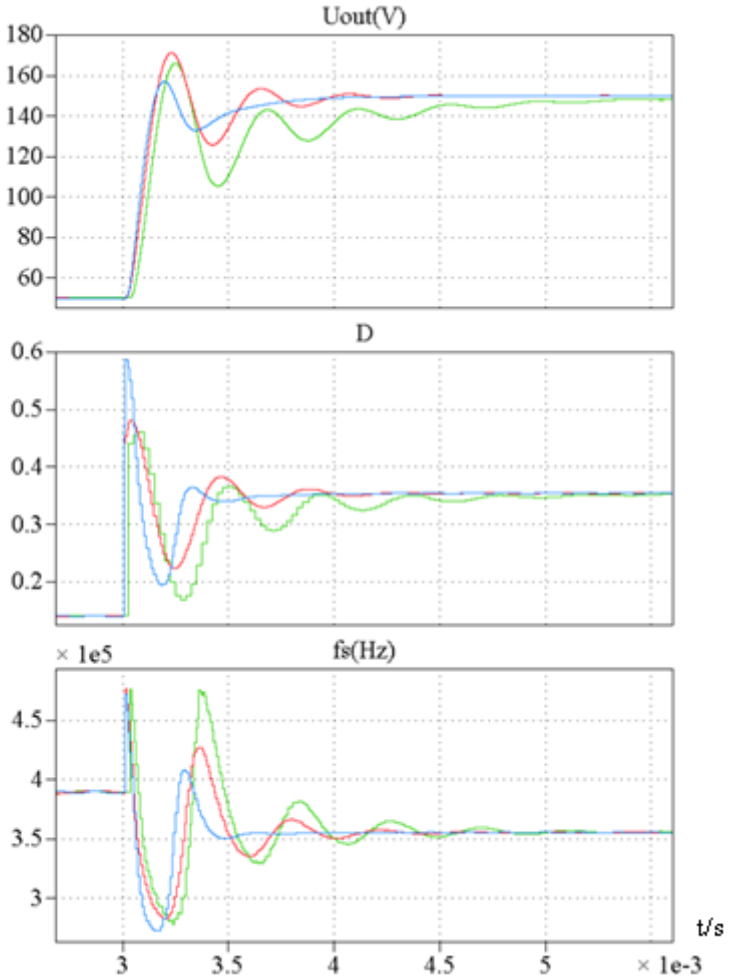



Figure 6.11: Dynamic response of reference step with different control algorithms: HSD-PW control (blue), HSD control (red), OM control (green), simulation ($R_L$ = 3.87 Ω)

The experimental measurement has been taken on the existing 32kW prototype. The reference voltage step is from 52V to 91 V with the designed gain-scheduling controller. In the real hardware, the control signals cannot directly be compared because of interferences of the measured switching frequency. The output voltage transient of both control algorithms is illustrated in Figure 6.12. HSD-PW control (red line) clearly has a faster dynamic response than OM control (green line). The settle-down time is reduced from 0.53 ms to 0.43 ms in the figure.

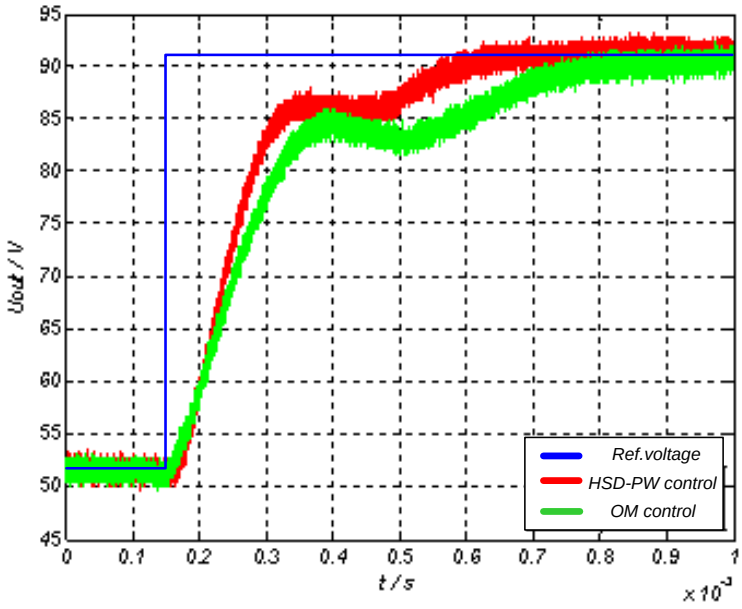



Figure 6.12: Dynamic response of reference step with different control algorithms: HSD-PW (red) and digital OM control (green), experiment

## 6.8 Summary

The main subject of this chapter is the further development of modulator and controller for digital OM. The discussion is based on two reasons. First, the FPGA board offers sufficient calculation capability for more complex control algorithms. Second, the state-of-the-art digital OM control has a series of problems because it is mainly designed for analog-digital hybrid implementation.

In order to overcome the three major drawbacks of digital OM, HSD-PW control is proposed. The novel control algorithm combines the ideas of HSD control and pulse-width regulation. By developing the dynamic HSD model, pulse-width-regulated HSD model is deduced and utilized for the design of controller parameters. Compared to the original OM control, the structure of the modulator is simplified and adapted to FPGA calculation. The simulations and the experimental results validate that HSD-PW control results in better dynamics than digital OM control.

# 7 Half-cycle-sampled calculation system and hardware implementation of SPRC

In this chapter, some more details of HSD system are introduced. It includes two parts for SPRC-LC-OM system. The first part gives the entire calculation system for SPRC-LC-OM and implements it in computer. Some calculation results are given in order to show the dynamic behaviour of SPRC-LC-OM system with different components. The second part gives the experiment platform of SPRC hardware, which is used in verification in previous chapters. The design requirement and the parameters of this prototype are introduced.

The calculation results and the estimation of calculation resources are given in section 7.1. The hardware setup of SPRC is described in Section 7.2.

## 7.1 Calculation system for SPRC-LC-OM

In the field of computer-aided design and computer-aided analysis, the HSD system for the SPRC-LC-OM can be utilized as calculation tools for simulation and dynamic process prediction, instead of the usual time-domain analysis and circuit simulation. Compared to the time-domain analysis, the HSD model for SPRC-LC-OM is easier to understand and deduce. The calculation cost of the HSD model is largely reduced, so the model can be implemented easily in different hardware platforms, even as a real-time calculation model.

Every components of HSD system for SPRC-LC-OM has been analysed and modelled separately in the previous chapters. The entire HSD system of SPRC–LC-OM is pieced together as a calculation system in the computer. The entire system, including converter, modulator, and controller are calculated with their corresponding HSD model in this

calculation system. Different control algorithms can be implemented and verified in the calculation system as the first step of validation.

In order to cover different modelling techniques and different modulations, the calculation system is designed with three modules. Every module has a series of options. Different HSD models for the SPRC are potential options in the converter module. In the modulation module, ideal OM, hybrid OM and digital OM can be selected. In the controller module, different control strategies can be designed with varying sampling steps. Pulse-width regulation and duty-ratio regulation are also covered in this calculation system. The structure of the calculation system is illustrated in Figure 7.1.

The present calculation system is based on the nonlinear HSD model in chapter 4 and the HSD controllers with duty-ratio/pulse-width regulation in chapter 6. It can be extended further for different modelling techniques and more complex control algorithms.

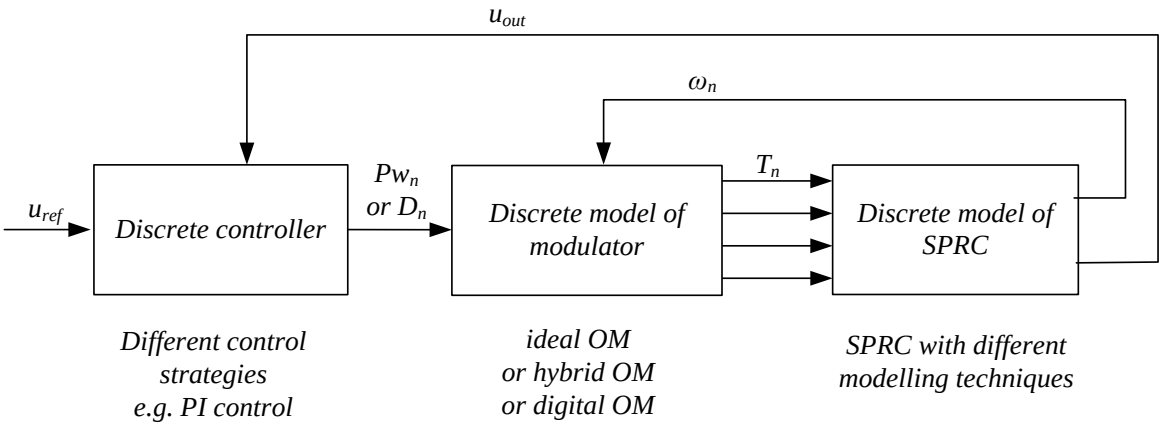
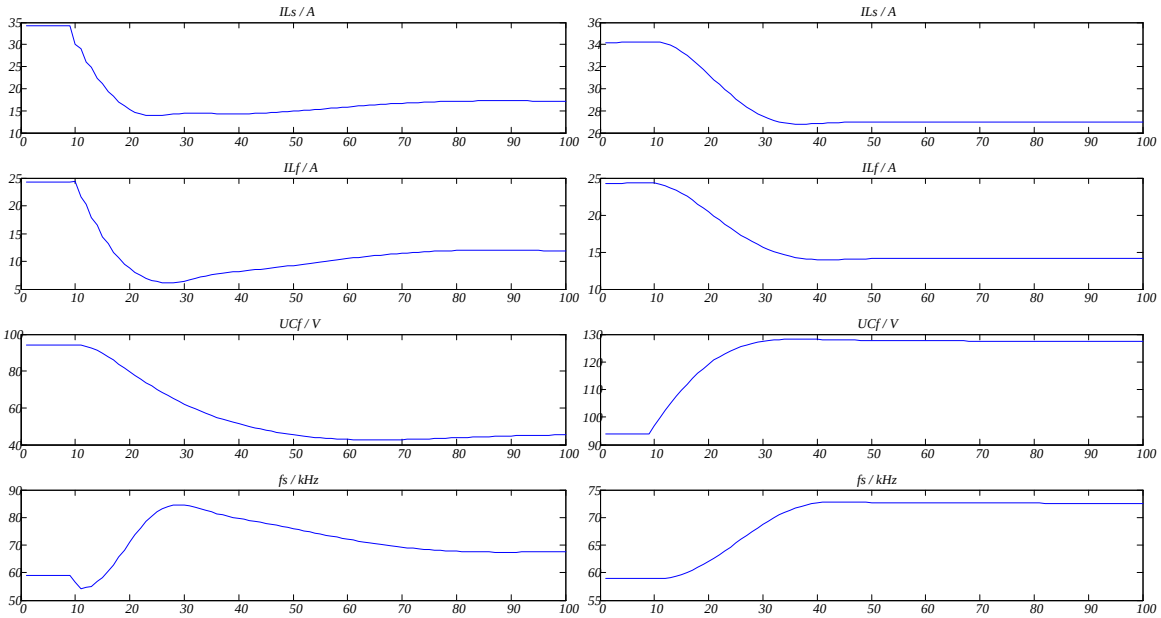



Figure 7.1: The structure of calculations system

With relatively small calculation costs, the SPRC system can be calculated and simulate the behaviour of SPRC-LC-OM system with different modulation strategy and different control methods. The entire system can be calculated synchronously, with the same sampling steps. The feedback of switching frequency in OM can be analysed directly. The discrete algorithm

executes once to represent the half-cycle period in time domain. The calculation system is implemented by programming in the Matlab® software. The coefficients are calculated in advance and are realized in look-up table in SPRC-LC-OM calculation system. The look-up table gives 500 points of current ratio, from 0.002 to 1. The calculation of a exact coefficients is given by linear interpolation.

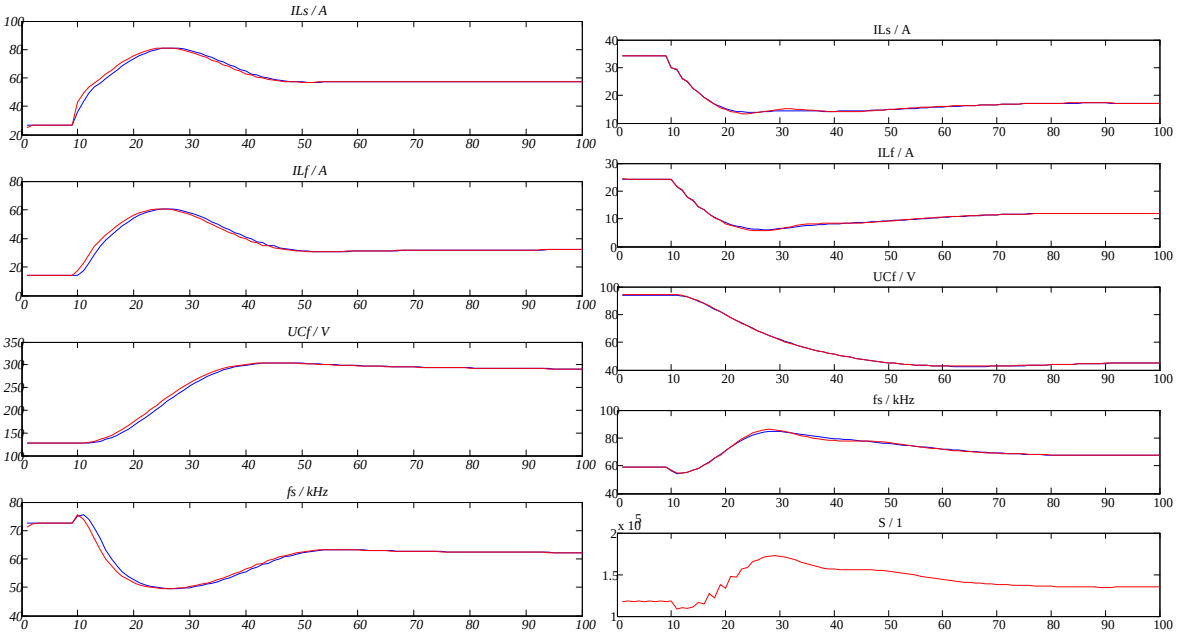
Some result of this calculation system is given in the following. Figure 7.2(a) illustrates a reducing step of the duty ratio of the SPRC-LC-OM with ideal modulator. From the top to the bottom, four state variables are depicted, as amplitude of resonant current $I_{Ls}$, filter current $I_{Lf}$, filter output voltage $U_{Cf}$ and switching frequency $f_s$. The load resistance is 3.87 Ω and the duty ratio steps down from 0.3 to 0.2. Figure 7.2(b) illustrates the changing of the load resistance from 3.87 Ω to 8.99 Ω, while the duty ratio is kept at 0.3. The x-axis of the figures represents the number of half cycles.




(a) (b)

Figure 7.2: Calculation system simulation with varied duty ratio (a) and load resistance (b), x-axis representing the number of half cycles

The system can also be used to observe and predict the behaviour of the modulator. Ideal modulation (blue) and digital modulation (red) are compared in Figure 7.3(a). The operation points load resistance is 8.99 Ω and the duty ratio is steping from 0.3 to 0.5. Ideal modulation (blue) and hybrid modulation (red) are compared in Figure 7.3(b). The operation points load resistance is 3.87 Ω and the duty ratio is stepped from 0.3 to 0.2. In the hybrid modulation strategy, the slope of saw-tooth is added in the figure, as it is an extra state value in the system. The integral parameter in the hybrid modulator is $K_{p1}A_o = 2.35 \times 10^5$.



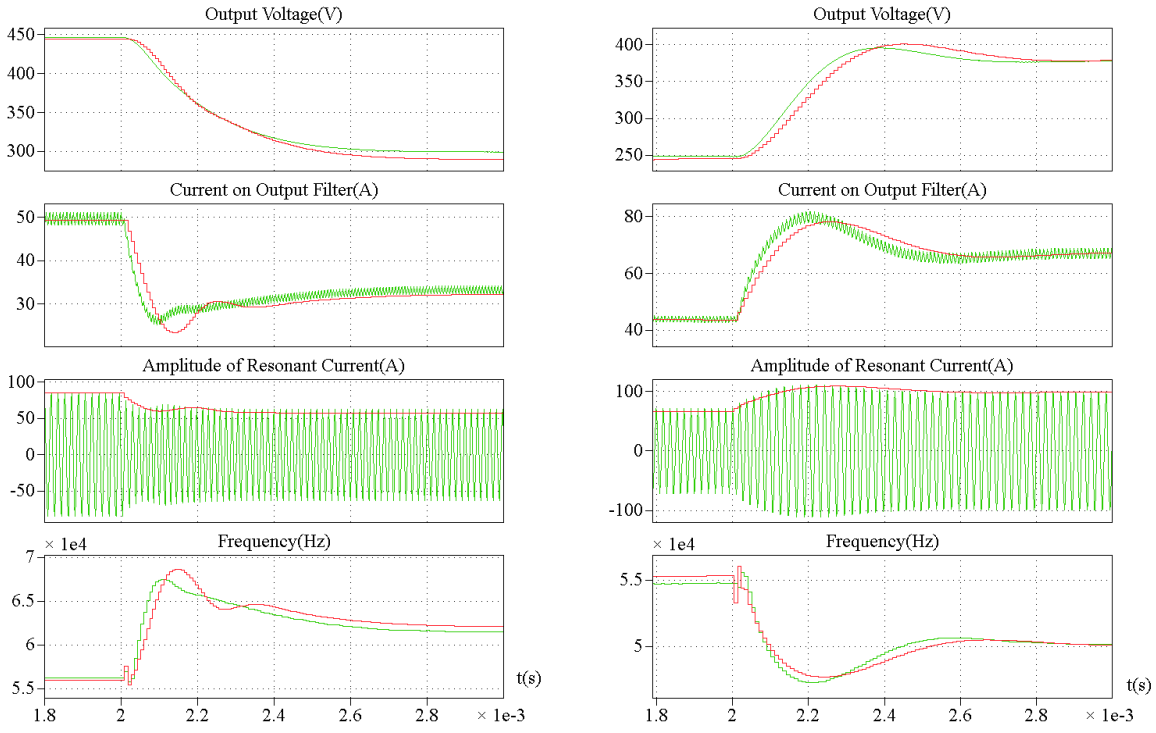

(a) (b)

Figure 7.3: Calculation system with different modulator strategies: (a) ideal modulation (blue) and digital modulation (red), (b) ideal modulation (blue) and hybrid modulation (red), abscissa representing the number of half cycles

Figure 7.4 gives the comparison of the circuit simulation and the result of calculation system. The SPRC-LC-OM system, with ideal OM modulator and open-loop duty-ratio controller is simulated with the PLECS® toolbox in Simulink® and is calculated with HSD calculation system. The red line represents the result of calculation system and the green line represents

the output results of circuit simulation in dynamic. The left figure is operated with 8.99 Ω load resistance and the duty ratio is stepping from 0.7 to 0.5. The right figure is operated with 5.66 Ω load resistance and the duty ratio is stepping from 0.5 to 0.7.

It proves that the calculation system gives a very similar dynamic performance of circuit simulation. The calculation system can roughly predict the behaviour of SPRC-LC-OM in micro-second scaling. However, it also shows some steady state error and dynamic differences.




(a) (b)

Figure 7.4: Dynamic process of calculations system (red) and simulation results (green), x-axis representing the time

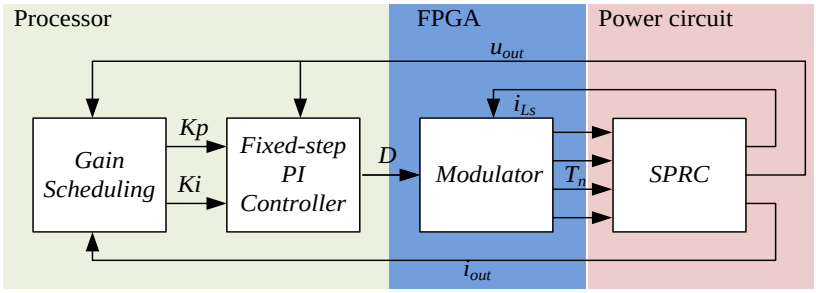
## 7.2 Experimental setup of SPRC in hardware

The previous experiments are all measured at a 32-kW SPRC-LC-OM prototype. The design parameters of the constructed prototype are given in Table 7.1. The device is mainly designed for working in a wide operation range and fast dynamics.

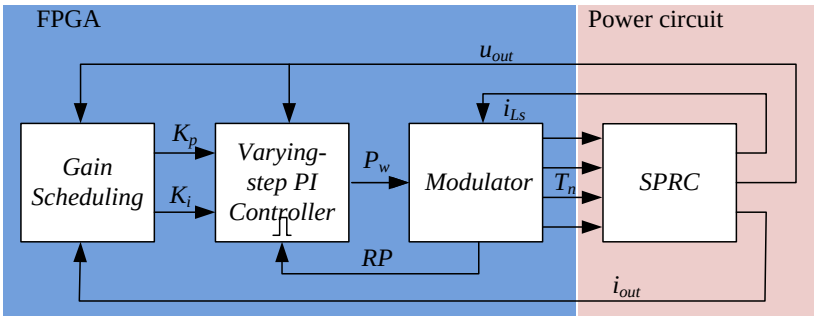
Table 7.1: Design parameters of the SPRC converter

| Name of components | Symbol | Value |
|---|---|---|
| Resonant inductor | $L_s$ | 46 μH |
| Resonant series capacitor | $C_s$ | 484 nF |
| Resonant parallel capacitor | $C_p$ | 178 nF |
| Filter inductor | $L_{out,r}$ | 150 μH |
| Filter capacitor | $C_{out,r}$ | 33 μF |
| Transformer ratio | $n$ | 0.9 |
| Input voltage | $U_{dc}$ | 540 V |

The modulation strategy and the control algorithm for SPRC-LC-OM are implemented in dSPACE® rapid prototype (RCP) system, which comprises a FPGA board "DS-5203" and a process board "DS-1005". The "DS-1005" process board features a Power PC 750GX processor running at 1 GHz. The "DS-5203 FPGA" board contains a Virtex-5 Xilinx FPGA as its core chip. The Virtex-5 Xilinx FPGA chip has the calculation step as 10 ns [Dspa12]. At the large digital operation capability of dSPACE® RCP system, especially the FPGA board, the entire control system can be implemented. The digital OM control is realized in two separate parts on the process and the FPGA board. The gain-scheduling controller is realized in the processer board, while the modulator is realized in the FPGA board, as illustrated in Figure 7.5(a). The HSD-PW control is entirely realized in the FPGA board, as illustrated in Figure 7.5(b). The varying-step controller is triggered by reset pulse (RP) signal from the modulator.




(a)




(b)

Figure 7.5: Hardware implementation of (a) OM control and (b) HSD-PW control

Due to the high dynamic requirement, the measurement of the resonant current direction is realized by an analog circuit outside the FPGA board. A digital input pin is connected to the analog circuit as show in Figure 7.6. An amplifier is used to handle the measured low-voltage resonant-current signal. The pin $u_{in}$ is connected to the voltage output of current sensor. And the pin $u_{out}$ is connected to the digital input pin of FPGA board.

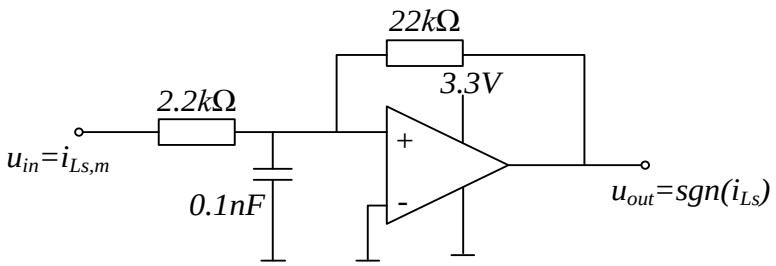



Figure 7.6: The amplifier of resonant current direction measurement

Figure 7.7 gives a general view of the SPRC test bench. The SPRC converter is connected to the programmable DC voltage source, which is a product of the company Regatron AG. The low-voltage circuits are supplied by another 15 V DC voltage source. The dSPACE RCP is operated and has real-time communications with the computer. The 15 V DC source and the computer is isolated with a 50-Hz transformer. The planform has been designed and assembled with the help of Regatron AG.

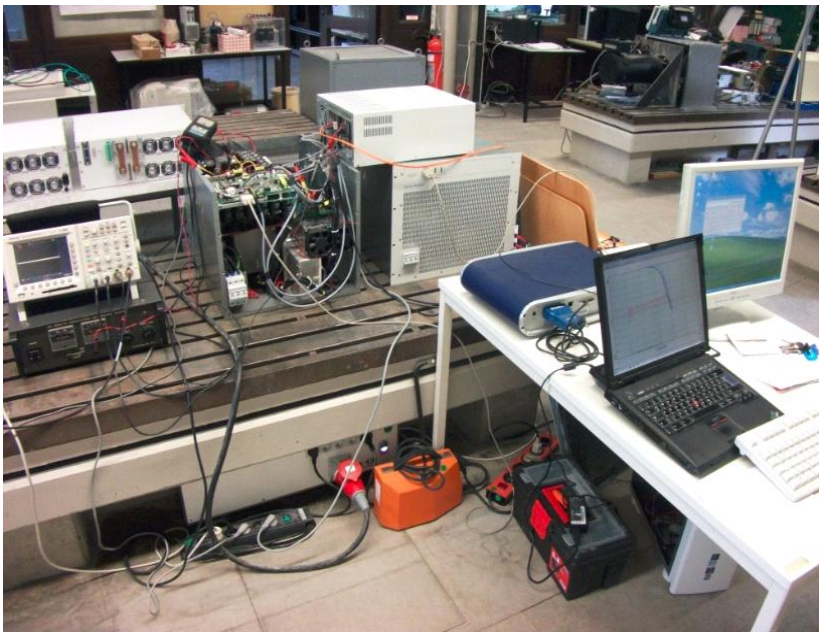


Figure 7.7: The photograph of SPRC test bench

# 8 Conclusion and outlook

## 8.1 Conclusion

The SPRC excels in efficient performance in a wide operation range, but modelling and control algorithms are relatively difficult to derive and calculate. Thus, the primary objective of this dissertation is to find a balanced modelling and control technique for SPRC system. The expected mathematical algorithms should require low calculation costs and has sufficient accuracy.

From this requirement, the HSD idea is proposed from the research of modulation strategies. The half cycle of the resonant oscillation is considered as analyse time unit and sampling step for the entire SPRC system. The continuous system is converted into a discrete system with half-cycle sampling. This sampling method is applied in the modelling approach of the converter, as well as the analysis of modulation and in the control design.

In the research of the HSD model, the SPRC-LC-OM circuit is analysed and represents by an equivalent simplified circuit. The amplitudes of the fundamental AC quantities are utilized to represent the half-cycle waveform in the converter. In order to derive a balanced modelling approach, the steady-state model is derived from Forsyth's approach. Instead of its original expression, a novel clear and compact definition, called improved steady-state analysis is given. It retains four passive components of the SPRC-LC circuit and is convenient to be implemented in digital devices.

The large- and small-signal models are extended from the improved steady-state analysis. After that, nonlinear and linear HSD models are derived step by step from the continuous models. These discrete models are mathematically equivalent to the continuous models, but

economize the calculation capability. The novel large- and small-signal models cover the changing of switching frequency in transitions, which gives a good prediction of the dynamic behaviour of the SPRC-LC-OM system.

The half-cycle-sampling principle is also considered in the modulator. The design of the modulator strategy does not only consider the implementation in hardware, but also its dynamic characteristics. With the design freedom of the FPGA board, the hybrid analog-digital modulator is abandoned. The novel fully digital modulator is implemented in the FPGA board with some extra functions like time-delay compensation and start-up modulation. For both implementations of modulators, the dynamic behaviour is analysed and modelled in the HSD system. Both implementations differ slightly from the ideal modulator, which have some effects on the SPRC system and are considered in the entire model of the SPRC system.

HSD-PW control is developed in order to eliminate the problems of digital OM. HSD-PW control eliminates the effect of measuring error of switching frequency and has a better dynamic performance than digital OM control. The ZVS and ZCS condition is still effective with HSD-PW control. Its control parameters are designed from the linear HSD model of the SPRC-LC-OM. The simulation and the experimental results prove a smaller overshoot voltage and faster settle-down time of HSD-PW control.

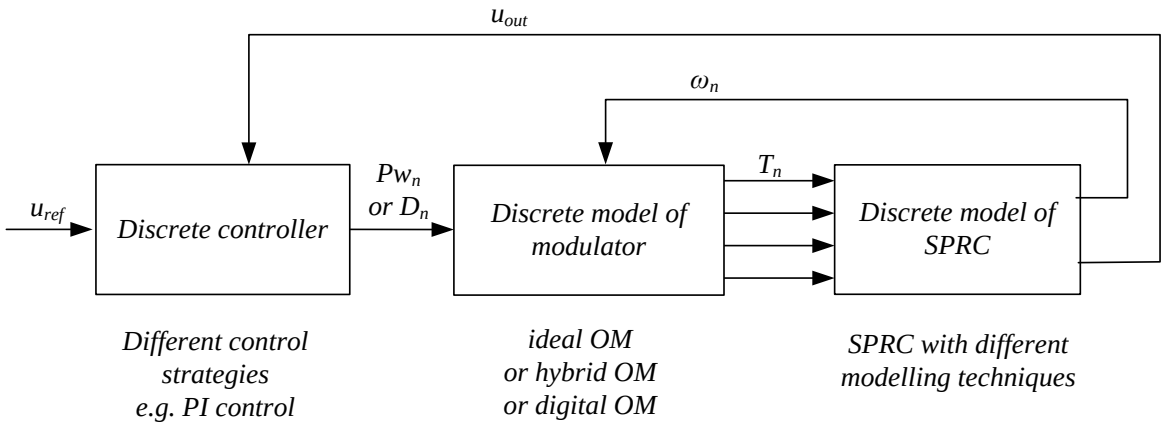
Finally, the SPRC system including models of converter, modulator and controller is implemented on the computer as a calculation system. Compared to time-domain analysis, the calculation system predicts the dynamic behaviours of SPRC-LC-OM accurately while demanding much less calculation resources. A circuit simulation is performed to validate the accuracy of calculation system. The system can be utilized for further development of the SPRC-LC-OM system, e.g. for a more advanced control design.

## 8.2 Outlook

There is still some room for improvement in the modelling approach of SPRC-LC-OM system. It is observed that the small-signal model and the steady-state model still have some deviations. In the steady-state model, the distortion of the resonant current is the major reason of deviation. High-order harmonics can be taken into consideration to construct a more precise model with HSD model. For the small-signal model, the precise approach should be a fifth-order state system. The dynamic of the parallel-capacitor voltage is ignored In the HSD approach. The fourth-order state system has a relatively good accuracy in the low-frequency range, but shows some error in the high-frequency range.

With the HSD model of SPRC-LC-OM, further development of controller, e.g. model-predictive control, can be utilized and designed. HSD model converts the complex SPRC converter into a discrete system. Due to the developed research methods in discrete domain, the control algorithms can be developed with this simplified fourth-order discrete system. The HSD model can also be utilized as an observer to predict state variables in the resonant converter. HSD model has a clear stability criterion, which offers great convenience in future applications.

# List of figures



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**Publikationen**


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