PADERBORN UNIVERSITY

DOCTORAL THESIS

Single-Stage DC-DC Converters for a Wide Input & Output Voltage Range

Author:
Philipp Ernst REHLAENDER

Doctoral supervisor:
Prof. Dr.-Ing. Joachim BÖCKER
Second examiner:
Prof. Dr.-Ing. Regine MALLWITZ

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For Katja, William and Sophie

"Science can amuse and fascinate us all, but it is engineering that changes the world.."

Isaac Asimov

Abstract

On-board DC-DC converters are the connecting link between the traction battery and the auxiliary battery and supply energy to the crucial components of an electrical vehicle. This work addresses DC-DC converters of a wide conversion range necessary to cover the voltage-transfer ratio resulting from the varying state of charge of the traction and auxiliary battery and investigates three topologies for this application: the *LLC resonant converter*, the *active-clamp forward converter* and the *isolated full-bridge converter*.

At first, the LLC resonant converter is analyzed and several operating modes are investigated and proposed to better cover the wide transfer ratio. The operating modes are benchmarked showing that the alternating-asymmetrical phase shift modulation and the frequency-doubler modulations can significantly reduce the MOSFET temperature. To switch from full-bridge mode to half-bridge mode, an improved morphing modulation is proposed that reduces the flux overshoot by about 70 % compared to the conventional concept. For an increased output power, multiple rails are operated in parallel while the balancing is achieved by phase-shift and asymmetrical operation and a balanced topology morphing control is proposed. Finally, an integrated planar transformer is proposed to increase the power density of the LLC.

The active-clamp forward converter is investigated to propose an accurate steady-state model. A snubber circuitry is presented to limit the voltage overshoot of the synchronous rectifier.

The isolated full-bridge converter is investigated in its hard- and soft-switching operation. A hard-switched frequency-doubler modulation is proposed to reduce the maximum temperature significantly. Additionally, a steady-state model is derived to accurately calculate the current shape of the converter and a topology morphing concept is proposed to limit the blocking voltage of the secondary-side semiconductors while switching between half and full-bridge mode.

To adapt the aforementioned analysis to 800 V systems, flying-capacitor inverter circuitry is analyzed to employ MOSFETs of 600 V blocking voltage alongside a balancing concept to regulate the flying capacitor voltage. Additionally, a flying-capacitor phase-shift and an active-clamp forward converter are proposed where the latter features extended zero-voltage switching capability and reduced freewheeling current.

Finally, a topology comparison and design methodology is proposed that enables a fair topology comparison without choosing a switching or resonant frequency. The three aforementioned topologies are compared and experimentally evaluated. The hard-switched full bridge strikes with a good performance over the entire operating region and an easy control. However, for low loads, a clear drop in efficiency is evident. If very light load is the design criteria, the LLC performs better. However, for low gains, a clear drop in efficiency is a drawback. Finally, the ACFC performs well over the entire load range and also at light load coupled with an easy control method. However, the peak efficiency is slightly lower compared to the hard-switched full bridge and LLC resonant converter.

Zusammenfassung

On-bord DC-DC-Konverter sind das Bindeglied zwischen der Traktionsbatterie und der Hilfsbatterie und versorgen wichtige Komponenten des Elektrofahrzeugs. Diese Arbeit adressiert den weiten Spannungsbereich des Wandlers, der eine Folge der variierenden Spannungen der Batterien ist. Als potentielle Topologien werden der LLC Resonanzwandler, der aktiv geklemmte Flusswandler und der isolierte Vollbrücken-Konverter untersucht.

Zunächst wird hierbei der LLC untersucht und verschiedene Modulationstechniken zur Abdeckung des weiten Spannungsbereichs gegenübergestellt, um zu zeigen, dass die Frequenzverdoppler-Modulation und die alternierende Phasenverschiebungsmodulation die maximale Temperatur der Halbleiter deutlich senken. Zum Wechsel zwischen Voll- und Halbbrückenmodulation wird eine Modulationstechnik vorgeschlagen, welche den transienten Überschwinger des Magnetisierungsflusses um über 70 % respektive des konventionellen Konzept senkt.

Für den aktiv geklemmten Flusswandler wird ein verbessertes Modell vorgestellt, das die Blockierspannung im lückenden und nichtlückenden Betrieb sehr genau modelliert. Zudem wird eine Snubber-Schaltung vorgeschlagen, welche die sekundärseitige transiente Blockierspannung deutlich reduziert

Für den isolierten Vollbrücken-Konverter werden hart- und weichschaltende Modulationstechniken analysiert und eine hartschaltende Frequenz-Verdoppler-Modulationstechnik vorgeschlagen, welche die maximale Schaltertemperatur deutlich reduziert. Zudem wird ein erweitertes Modell für den stationären Zustand vorgestellt und eine Modulationstechnik sowie Beschaltung vorgeschlagen, um zwischen dem Voll- und Halbbrückenmodus zu wechseln.

Die Anwendbarkeit für 800 V-Systeme wird unter Ausnutzung von Drei-Level-Topologien untersucht und eine Modulationstechnik zur Regelung der Kondensatorspannung vorgeschlagen. Zusätzlich wird ein Drei-Level aktiv geklemmter Flusswandler vorgestellt, welcher den weichschaltenden Betriebsbereich erweitert und den Freilauf-Strom reduziert.

Die zuvor erarbeiteten Konverter werden unter Anwendung einer vorgestellten Designmethodik verglichen. Durch Normierung der Bauteilparameter wird ein fairer Vergleich ohne Vorauswahl der Schalt- oder Resonanzfrequenz ermöglicht. Zuletzt werden die Schaltungen evaluiert und es wird gezeigt, dass die hartgeschaltete Vollbrücke einen hohen und stabilen Wirkungsgrad über einen weiten Spannungsbereich erzielt, bei Schwachlast allerdings deutlich Wirkungsgradverlust aufzeigt. Sind sehr hohe Wirkungsgrade bei Schwachlast das Designkriterium, dann zeigt der LLC in diesem Betrieb einen besseren Wirkungsgrad. Allerdings muss damit ein schlechterer Wirkungsgrad bei einem geringen Übertragungsverhältnis in Kauf genommen werden. Der aktiv geklemmte Flusswandler liefert dagegen einen relativ konstanten Wirkungsgrad über den gesamten Betriebsbereich gekoppelt mit einer einfachen Ansteuerung. Er fällt gegenüber den anderen Topologien allerdings beim Maximalwirkungsgrad zurück.

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Author's Contributions

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Contents

Chapter 1

Introduction

The anthropogenic climate change is one of the primary threats to the human existence. In 2022 the IPCC assessed that 3.3 to 3.6 billion people were living in countries that are global climate hot spots with a particularly high risk [Kix22]. While speaking at the climate conference COP23 in November 2017, Angela Merkel called the climate change *a question of fate* as it determines the well being of everyone [Ang15] and Stephen Hawking emphasized "*climate change is one of the great dangers we face, and it's one we can prevent if we act now*" [Gho17]. A united global response to revolutionize all sectors contributing to carbon emission is imperative to achieve the goal of limiting global warming well below 2 °C above pre-industrial levels, which was defined by the Paris Climate Accords.

With an emission of about 8.26 billion tons carbon dioxide in 2018, transportation is responsible for about 25 % of the carbon emission worldwide [Kor20a] and, thus, one of the primary carbon-intensive sectors. About 6.09 billion tons of emission are caused by road traffic [Kor20a]. Therefore, the electrification of the drive train is key to the reduction of global emission. Fueled by massive subsidies, there were about 10 million electric vehicles registered in 2020 worldwide. That is an increase of more than 900 % in six years compared to less than one million in 2014. Despite the influence of the Covid 19 pandemic, registrations increased by as much as 41 % in 2020 [Bib+21]. While these developments are a promising indicator of the transformation, the process is still in its early stages, noting that Germany alone had about 59 million registered vehicles in 2020 [Kra21] and even in 2020 there were more registrations of traditional internal combustion engine (ICE) vehicles than electric vehicles in Germany[1]. These developments emphasize the necessity of new and better technologies to reduce vehicle costs and increase the range to enable them to penetrate further into the markets traditionally covered by conventional ICE vehicles. Technological progress is required on all fronts.

A typical drive train of an all-electric vehicle is depicted in Figure 1.1 [Adl+18; Cha+20; Dop20; KMN15; Tha21]. The battery can be charged using the on-board or off-board charger and is connected using an optional DC-DC converter to the inverter feeding the electric motor. While the DC link voltage is usually at a level of 400 or 800 V, low-voltage electric loads (usually supplied with a voltage of about 12 V)

[1] about 1 million more vehicles have been registered in Germany in 2020 [Kra21] and only 172 thousand more registered electric vehicles [Kor22]

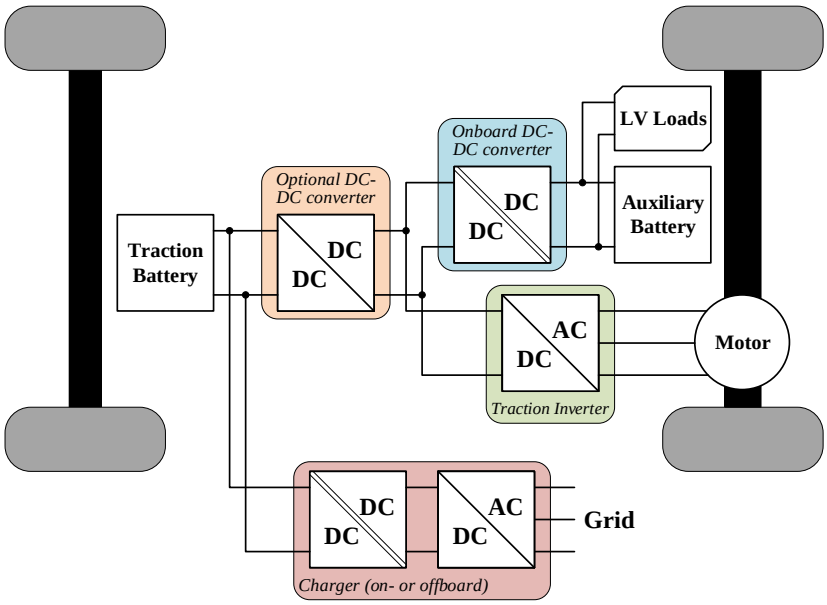


FIGURE 1.1: Typical drivetrain structure of a battery-electric vehicle [Adl+18; Cha+20; Dop20; KMN15; Tha21]

require an interface to the traction battery. The low-voltage energy storage is commonly a traditional lead-acid battery and supplies loads such as windshield wipers, light, radio and electric window openers [Dop20]. The commonly unidirectional energy transfer between the traction battery and the auxiliary battery is commonly achieved with an on-board DC-DC converter, which will be the focus of this thesis.

Due to the varying state of charge of the traction battery and the auxiliary battery, the converter is required to cover a wide voltage-transfer ratio (VTR). The voltage of the traction battery (from hereon referred to as the input voltage V_{in}) may vary within 200 to 420 V whereas the voltage of the auxiliary battery (from hereon referred to as the output voltage V_{out}) may vary within 8 to 16 V. The maximum output power of the converter investigated in this thesis is $P_{\text{out}} = 1.82\,\text{kW}$ with a maximum output current of $I_{\text{out}} = 130\,\text{A}$. Furthermore, it is specified that for any output voltage smaller $V_{\text{out}} = 11\,\text{V}$, the maximum output current is to be supplied. The converter must supply the output between the maximum gain ($\check{V}_{\text{in}} = 200\,\text{V}$, $\hat{V}_{\text{out}} = 16\,\text{V}$) and the minimum gain ($\hat{V}_{\text{in}} = 420\,\text{V}$, $\check{V}_{\text{out}} = 8\,\text{V}$) – a very wide VTR range is, thus, required. A measure of the required VTR range is the normalized conversion range factor G_{norm}, which is the ratio of the products of the maximum output and input voltages ($\hat{V}_{\text{out}}$, $\hat{V}_{\text{in}}$) and minimum output and input voltages ($\check{V}_{\text{out}}$, $\check{V}_{\text{in}}$):

$$G_{\text{norm}} = \frac{\hat{V}_{\text{out}}\hat{V}_{\text{in}}}{\check{V}_{\text{out}}\check{V}_{\text{in}}}. \tag{1.1}$$

The application requires a normalized conversion range factor of $G_{\text{norm}} = 4.2$. Conventional topologies suffer at this wide conversion range, which leads to higher losses and a reduced power density. Common solutions employ a two-stage approach: a first-stage galvanically-coupled converter supplies a second-stage galvanically-isolated converter. The two-stage setup, however, is detrimental to the efficiency, the power density and the costs. It is evident that a single-stage solution can be beneficial regarding all three aspects. The purpose of this thesis is to find a

well suitable single-stage topology that can be operated in the specified wide input and output voltage range.

This thesis investigates three different converter topologies, the ***LLC resonant converter***, the ***active-clamp forward converter*** and the ***isolated full-bridge converter*** in its most common modulations – the *phase-shift modulation* and the *hard-switched operation*. The ***LLC resonant converter*** is selected as it is one of the most common industrial converters, which is preferred for its capability to operate the primary-side switches at zero-voltage switching and the secondary switches at zero-current switching, which can substantially reduce the switching losses. However, it is mostly only operated at a narrow input and output voltage range. The feasibility of this converter for a wide transfer ratio is investigated in this thesis by employing various operating modes. The ***active-clamp forward converter*** is chosen as it only employs two primary inverter switches compared to the other topologies that employ four. Further, it employs only one main switch as the other only has a auxiliary function which is subjected to a much smaller effective current. While the voltage rating of those switches is higher compared to the other topologies and the effective transformer usage is smaller compared to the other topologies, the overall costs of the semiconductors may be smaller and - with wide bandgap semiconductors - this topology may be operated at higher switching frequencies to overall reduce the size of the magnetic components. Finally, the ***isolated full-bridge converter*** in its *hard-switched operation* is investigated for its simplicity of operation and its potential to reduce the switching losses by using wide-bandgap semiconductors. As this topology is also commonly employed at a narrow operation range due to its drawbacks on the secondary-side blocking voltage, this thesis investigates its efficacy for wide-voltage range applications by operating it in different operation modes.

The converters are investigated in Chapter 2. This chapter presents modeling approaches, analyzes modulation strategies, concepts for magnetic integration and clamping techniques. Finally, characteristic operating points are chosen for the design process. Section 2.1 describes the analysis of the LLC resonant converter, the active-clamp converter is investigated in Section 2.2 and the isolated full-bridge converter in Section 2.3. The efficacy of the analysis of the three topologies to vehicles with a traction battery with a nominal voltage of 800 V is performed in Section 2.4 where the full-bridge or half-bridge inverter is subsequently replaced by a flying capacitor inverter that allows the designer to employ the same inverter switches, and magnetic components compared to the 400 V design showing that the aforementioned analysis can be transferred to the design of an on-board charger coupling 800 V to 12 V systems.

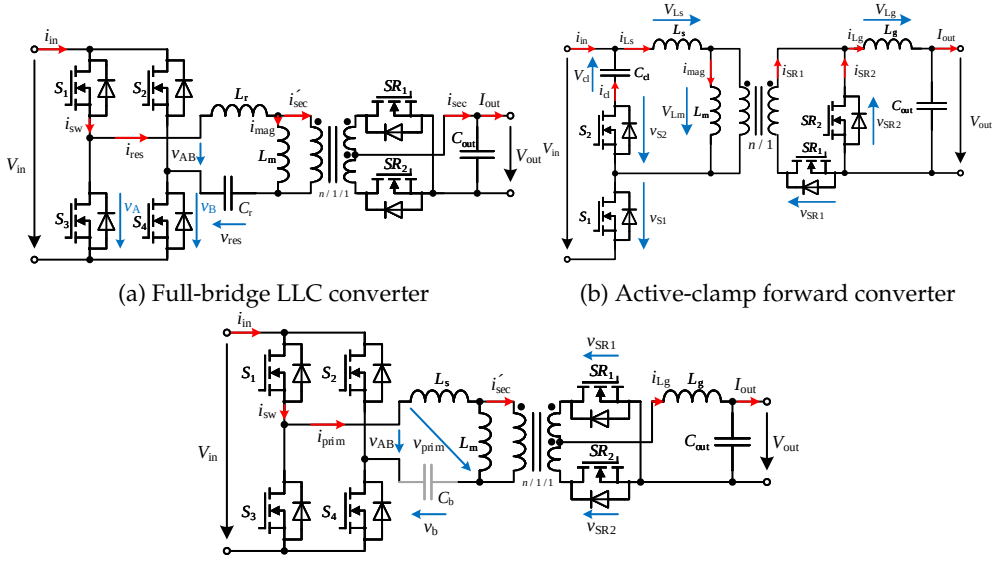
The topologies are subsequently compared in Chapter 3. The chapter reviews topology comparison methodologies in Section 3.1 to propose a normalized comparison and design methodology in Section 3.2. The presented frequency-independent methodology allows the designer to compare converter stress values such as RMS currents, turn-off currents, charges and flux densities frequency-independently to allow a fair non-biased benchmark of the topologies. This methodology is employed to compare the three investigated topologies in Section 3.3. Finally, the topologies are benchmarked experimentally in Section 3.4 before the thesis is concluded in Chapter 4.

Chapter 2

Topology Analysis

To accurately compare and design the DC-DC converters for the application of a wide input and output voltage range, this chapter describes the analysis of the three selected topologies:

- ***the LLC resonant converter***,
- ***the active-clamp forward converter***, and the
- ***isolated full-bridge converter*** in its operating modes
  - *hard-switched operation* as a hard-switched full-bridge converter (HSFB) and
  - *phase-shift operation* as a phase-shifted full bridge converter (PSFB).



(a) Full-bridge LLC converter

(b) Active-clamp forward converter

(c) Isolated full-bridge converter

FIGURE 2.1: Circuit diagrams of the three compared topologies.

All analyzed topologies are depicted in Figure 2.1.

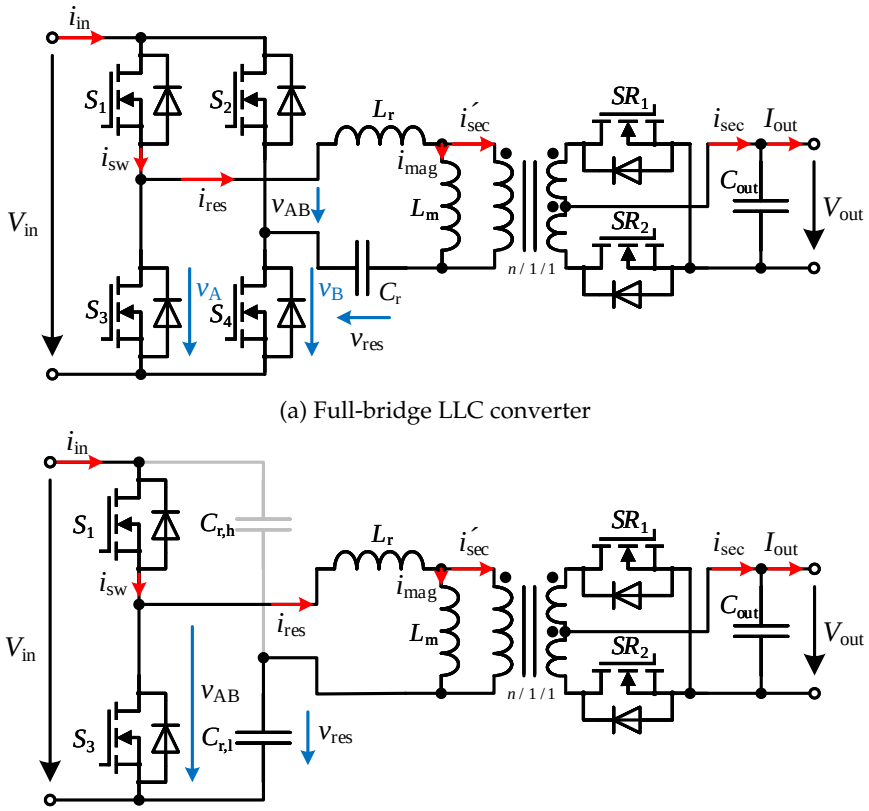
The LLC resonant converter of Figure 2.1a is analyzed in Section 2.1. To cover the wide input and output voltage range, the operating modes of the converter are

analyzed in Section 2.1.1. By utilizing further operating modes aside from the conventional switching-frequency control, the converter can be much better employed for these demanding requirements. However, to switch from one operating mode to the other, an on-the-fly morphing modulation is required, which is described and analyzed in Section 2.1.2. Since the conventional concept results in an undesired magnetizing flux offset, an improved variant is proposed in Section 2.1.3. An analysis of the LLC operation in these operating modes is further provided in Section 2.1.4. Since a single-rail design may not be sufficient to meet the light-load efficiency requirements, a multi-rail concept may be required. To balance the power transfer of the rails, Section 2.1.5 analyzes the interleaving of two LLC resonant converters in full-bridge and half-bridge mode. Finally, a method to integrate the resonant inductor and transformer into one single magnetic component is described in Section 2.1.6. By employing the proposed method, the costs of the magnetic components can be reduced and the power density can be increased.

The active-clamp forward converter depicted in Figure 2.1b is analyzed in Section 2.2. To accurately analyze and design the converter, the operating principle is described for CCM in Section 2.2.1 and for DCM in Section 2.2.2 to derive a highly-accurate operating model. Section 2.2.3 describes the model extension for an extended interleaved converter type suitable for large output loads. The zero-voltage switching concepts are investigated in Section 2.2.4. Due to the inductive termination and the small conversion ratio of the active-clamp converter, the topology results in large overshoots in the secondary-side rectifier blocking voltage. Section 2.2.5 proposes an active snubber to reduce these over voltages to successfully enable its operation. Finally, characteristic design operating points are derived in Section 2.2.6.

The isolated full-bridge converter with inductive termination that is depicted in Figure 2.1c is described in Section 2.3. The operating modes of this converter are investigated in Section 2.3.1 to derive loss balancing frequency-doubler operation in Section 2.3.1C. Section 2.3.2 describes the operating principle to derive a highly-accurate model that includes the influence of both the series inductance and magnetizing inductance. To successfully switch from one operating mode to the other during operation, an on-the-fly morphing concept is proposed in Section 2.3.3, which avoids excessive over voltages at the rectifier semiconductors and an increased magnetizing flux. Finally, characteristic operating points are derived for the phase-shift and hard-switched operation in Section 2.3.4 and Section 2.3.5 respectively.

The efficacy of the described concepts are investigated for 800 V systems in Section 2.4 by employing flying-capacitor inverter stages. After a brief introduction to these types of inverters in Section 2.4.1, flying-capacitor quasi full-bridge converters are investigated in Section 2.4.2 and a flying-capacitor active-clamp forward converter is proposed in Section 2.4.3.



(a) Full-bridge LLC converter

(b) Half-bridge LLC converter

FIGURE 2.2: Circuit diagram of the LLC resonant converter (LLC) in a configuration with a full-bridge inverter and center-tapped rectifier with a full-bridge inverter (a) and a half-bridge inverter (b). For the half-bridge inverter, the resonant capacitor may be connected to ground, V_{in} or both.

2.1 LLC Converter

For decades the LLC resonant converter (cf. Figure 2.2) has been a dominant topology in power electronics as it provides zero-voltage switching (ZVS) of the primary switches and zero-current switching (ZCS) of the secondary semiconductors to increase the efficiency and power density [LM01; SXZ21; YCL02; Yan+02]. The topology has been employed in a number of different applications including photovoltaic applications, electric vehicle charging, and server power supply [WLM20b] to raise the efficiency and power density. To control the output, the frequency is usually adjusted. For VTRs the LLC is operated with a switching frequency larger than the resonant frequency in buck configuration while for large VTRs the converter is operated with a switching frequency below the resonant frequency in boost configuration. In contrast to pulse-width modulation (PWM)-modulated (buck) converters such as the phase-shifted full bridge, the LLC converter, therefore, is a buck-boost topology.

The inverter stage of the LLC can hereby be realized as a full bridge or half bridge. If a full-bridge configuration is used, the voltage applied to the resonant tank is $v_{AB} = \pm V_{in}$. For a half bridge configuration, the inverter voltage is $v_{AB} = \{0, V_{in}\}$. The resonant capacitor acts partly as a blocking capacitor, which is pre-charged to $\frac{1}{2}V_{in}$. The input voltage of the resonant tank is thereby effectively reduced by a factor

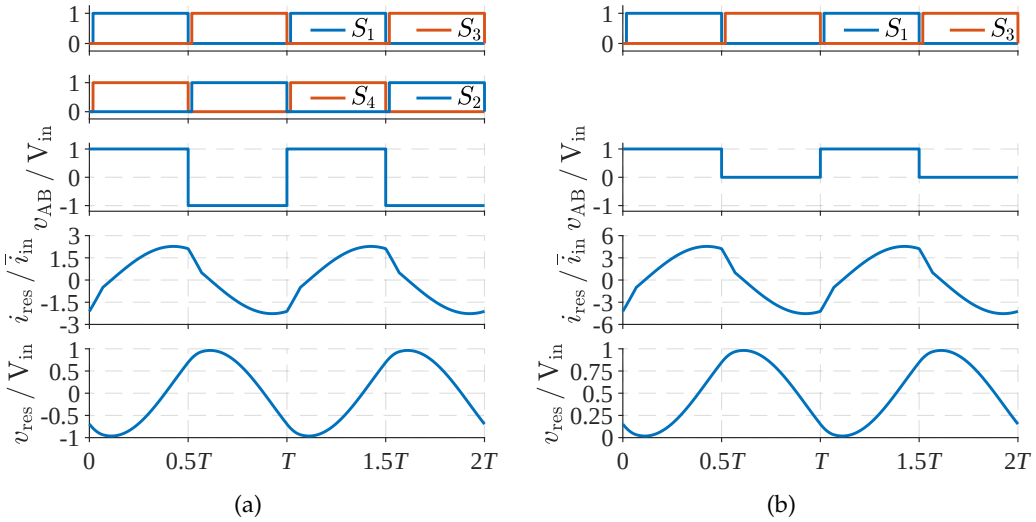


FIGURE 2.3: (a) Full-bridge and (b) half-bridge LLC converter in the CCMA scheme. Note the much higher normalized resonant current for the operation in half-bridge modulation.

of two yielding a halved VTR. Figure 2.3 shows the simulated resonant currents and voltages of a resonant converter in full-bridge configuration (Figure 2.3a) and half-bridge configuration (Figure 2.3b). For the half-bridge simulation, the input voltage is doubled. It is evident that the shape of the resonant current and voltage is the same with the only difference being the offset in the resonant voltage of Figure 2.3b. The normalized input current $i_{res}/\bar{i}_{in}$ is increased for the half-bridge configuration through the increased input voltage. The absolute resonant current amplitude is the same. This comparison emphasizes that the combination of a full-bridge configuration and half-bridge configuration can be beneficial for applications of wide VTR applications.

This section analyzes this topology to investigate different operating modes to increase the VTR range of the converter. Section 2.1.1 describes a selection of those that are particularly useful to achieve low conduction and switching losses. In Section 2.1.1A full-bridge modulations are discussed that can be employed for high and intermediate VTRs while Section 2.1.1B discusses modulation techniques suitable for low VTRs. To switch from a half-bridge modulation to a full-bridge modulation and reverse while continuously supplying the load, Section 2.1.2 discusses morphing techniques. A design methodology for wide VTR application is proposed in Section 2.1.4.

For higher output powers, it may be beneficial to occupy two parallel resonant converters. They can be advantageously operated with an equal switching frequency to reduce the output capacitor current ripple. However, a balancing control is necessary. The balancing of those rails is analyzed in Section 2.1.5A. A balanced morphing strategy is proposed in Section 2.1.5C.

Finally, Section 2.1.6 proposes a high-current transformer to integrate the resonant inductance and the transformer into one single magnetic component to increase the power density and reduce the converter costs.

2.1.1 Operating modes

Conventionally, the LLC is best employed for applications with a VTR that is relatively static [FML13; Kim+10; LJH11; Lee+11; Ryu+12; SL14; Vin06; ZH09; USB20a]. As the gain is adjusted with the switching frequency, a wide VTR application inevitably results in a wide switching frequency range. This is undesirable as the high switching frequencies that are required for a low gain operation may result in high switching losses and high eddy-current losses[1] in the inductive components. Additionally, the low switching frequencies that are required for the large-gain operation increase the filter size. To limit the switching frequency, the LLC can be designed for a large VTR by reducing the magnetizing inductance L_m to increase the inductance ratio $\lambda = \frac{L_\mathrm{r}}{L_\mathrm{m}}$, which is causing a steeper gain function [Den+15]. However, this results in increased resonant currents inevitably causing higher conduction and turn-off losses.

Due to the typical LLC transfer behavior, low VTRs can - in the conventional operation - only be achieved by increasing the switching frequency. For light load, this is even more problematic as the necessary switching frequency increases with decreasing load. Furthermore, the parasitic output capacitance of the synchronous rectifiers/diodes prevents an operation for very light loads as the charging interval of those capacitances, which participates in the energy transfer, becomes increasingly more significant such that ultra low loads cannot always be achieved with any switching frequency in the conventional mode of operation. To reduce the VTR at a constant switching frequency, the *phase-shift modulation (PSM)* has been analyzed in several publications [Che+14; Yan+16; MW14; Lo+11; Kim+14; Kim+15; Liu+14; Sha+16; RSB21; Reh+20a]. This modulation, however, results in unbalanced inverter losses. Section 2.1.1A discusses different modulation techniques that result in the same inverter voltage by employing increased modulation lengths to investigate modulations that result in balanced inverter losses.

In full-bridge configuration, the LLC can also be operated as a quasi half-bridge configuration by permanently turning on one switch and turning off the other switch of the same respective bridge leg. This mode shall be referred to as *half-bridge modulation (HBM)* while *conventional full-bridge modulation (FBM)* refers to an operation where S_1/S_4 and S_2/S_3 are operated complementary with a duty cycle of 0.5. A problem of the half-bridge modulation (HBM) is that one switch conducts the full resonant current, while the other bridge leg is operated complementary with a duty cycle of 50 %. The modulation, thus, results in unbalanced inverter losses. For that purpose, Section 2.1.1B2 benchmarks the HBM versus the frequency-doubler half-bridge modulation (FD-HBM) that results in the same inverter voltage. In Section 2.1.1B4 the asymmetrical half-bridge modulation is discussed as a modulation technique for very low VTRs and output loads. It is compared to the proposed asymmetrical frequency-doubler modulation in Section 2.1.1B5

A Full-bridge modulation schemes

A1 Phase-shift modulation To avoid the very high switching frequencies in full-bridge configuration and, therefore, increase the conversion efficiency, phase-shift modulation (PSM) is used [Kim+14; Kim+15; Lo+11; MW14]. Furthermore, it is employed for start-up purposes [Che+14; Yan+16], interleaving [MK16; Fig+08; Fig16]

[1] for increased switching frequencies, the hysteresis losses usually reduce as a result of the lower flux ripple

and wide VTR applications [Liu+14; Sha+16; Liu+16b; WLM20b].

In PSM, the two converter legs - the leading leg S_1/S_3 and lagging leg S_2/S_4 - are operated with a small phase shift such that freewheeling intervals are inserted through the switches S_1/S_2 and S_3/S_4 (see Figure 2.4a) in which no voltage is applied to the resonant tank. While this can work very well, one problem of this modulation is that ZVS cannot always be achieved for the lagging leg. As a voltage is applied to the resonant inductor L_r by the resonant capacitor voltage, resistive voltage drops and, in some instances, the transformed output voltage, the resonant current reduces during the freewheeling interval such that the energy in the resonant inductor may not be large enough to ensure ZVS for the primary switches or for some modes even lead to hard switching (positive turn-on current) [Liu+16b]. While hard switching should normally be prevented, a switching with a residual voltage may in some cases be acceptable. However, it inevitably leads to increased switching losses that can be calculated using [Kas+16]. Another effect of the reduction of the resonant current in the freewheeling interval is that the turn-off current of the leading leg is always larger than the turn-off current of the lagging leg resulting in imbalanced turn-off losses. The imbalance of the turn-off losses and the loss of zero-voltage switching cause an imbalance in the losses of the leading and lagging leg such that the thermal stress on the switches may be severe.

A2 Asymmetrical phase-shift modulation In phase-shift modulation, the inverter voltage is achieved through two freewheeling intervals: the conducting switches are S_1, S_2 and S_3, S_4. In contrast, the modulation depicted in Figure 2.4b achieves an equal inverter voltage. The operating mode is described in [She+16; WG18; KD21]. While in PSM, the freewheeling path is S_1/S_2 and S_3/S_4, in the asymmetrical modulation it is only S_1/S_2 or only S_3/S_4. This has the probable advantage that the leg with high conduction losses has low switching losses and the reverse. Furthermore, it is possible to switch from a freewheeling path of S_1/S_2 to a freewheeling path S_3/S_4 from one period to the next such that equal thermal stress can be guaranteed [LC14; LSC15].

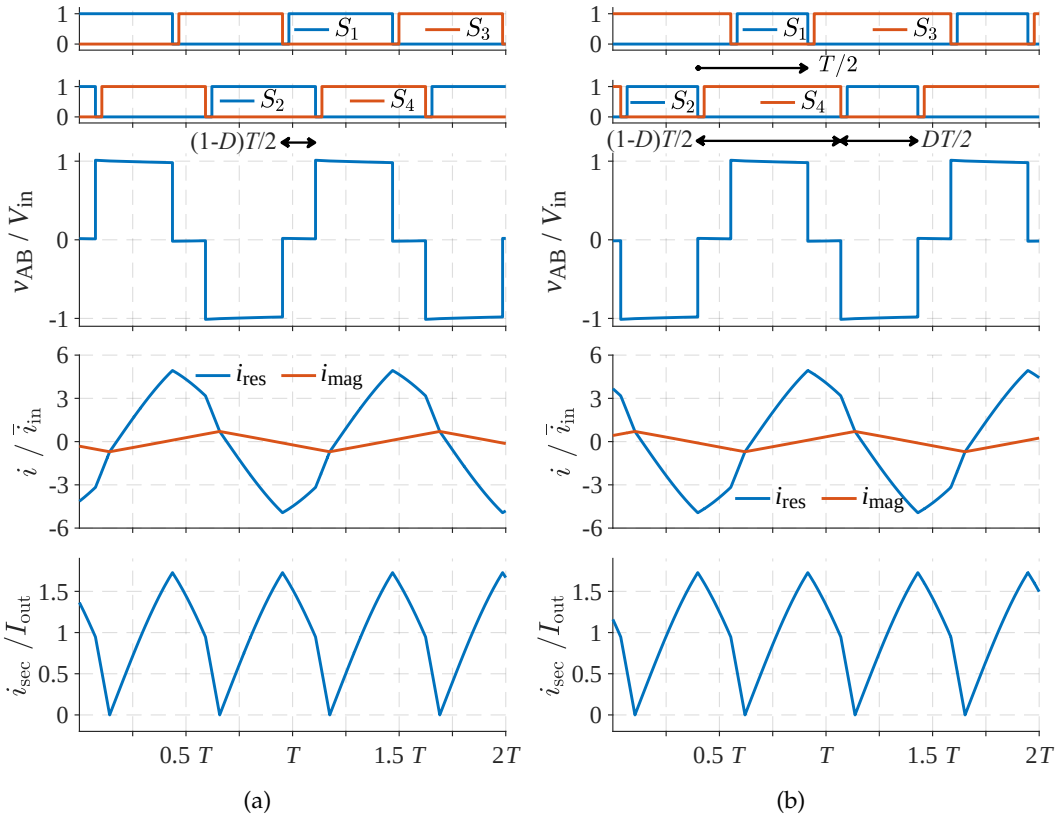


FIGURE 2.4: Phase-shift modulation (PSM) (a) and asymmetrical phase-shift modulation (aPSM) (b) of the LLC converter. Both operated with $D = 0.35$[1]. (parameters: Config$_{2.1a}$).

A3 Phase-shift modulation analysis

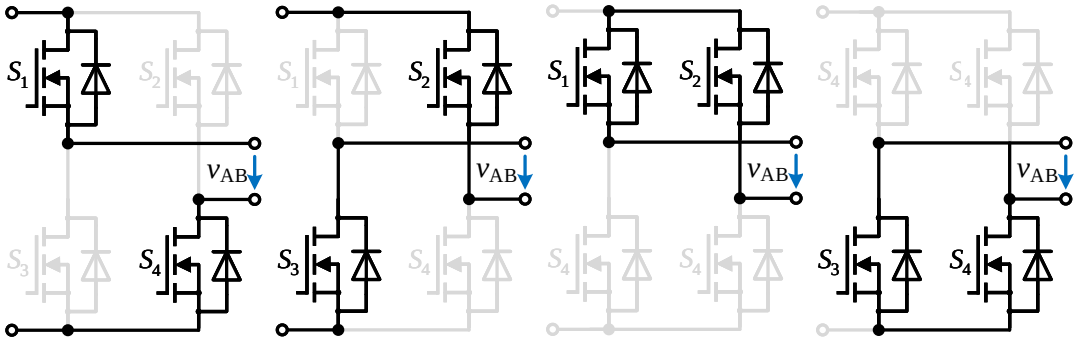
this section has been previously published in parts in [Reh+21d].

The following analysis is valid for every full-bridge converter operated in phase-shift modulation. Thus, it is also valid for the isolated full-bridge converter operated in phase-shift modulation, which is covered in Section 2.3.1A.

The switching states of the inverter can be divided into two basic intervals: the *energy-transfer* (ET) interval, in which power is drawn from the input and transmitted to the output and the *freewheeling* (FW) interval in which no power is drawn from the input but power may still be transmitted to the output. In the ET interval, the switches S_1 and S_4 can be activated for a positive inverter voltage ($v_{AB} = V_{in}$) while the switches S_2 and S_3 can be activated for a negative inverter voltage ($v_{AB} = -V_{in}$). These states are denoted as ET$^+$ and ET$^-$ respectively. For $v_{AB} \approx 0\,\mathrm{V}$ the two high-side switches S_1 and S_2 or the two low-side switches S_3 and S_4 can be activated. These states will be referred to as FW$^+$ and FW$^-$ respectively. In the conventional phase-shift modulation the intervals repeat in the order

$$\begin{aligned} &\mathbf{ET^+}(S_1, S_4) \rightarrow \mathbf{FW^-}(S_3, S_4) \rightarrow \\ &\mathbf{ET^-}(S_3, S_2) \rightarrow \mathbf{FW^+}(S_1, S_2) \end{aligned} \tag{2.1}$$

if the switches S_2 and S_4 are operated as the leading leg (see Figure 2.6, left). If the



(a) **ET**$^+$ ($v_{AB} \approx V_{in}$) (b) **ET**$^-$ ($v_{AB} \approx -V_{in}$) (c) **FW**$^+$ ($v_{AB} \approx 0\,V$) (d) **FW**$^-$ ($v_{AB} \approx 0\,V$)

FIGURE 2.5: Switching states of the inverter

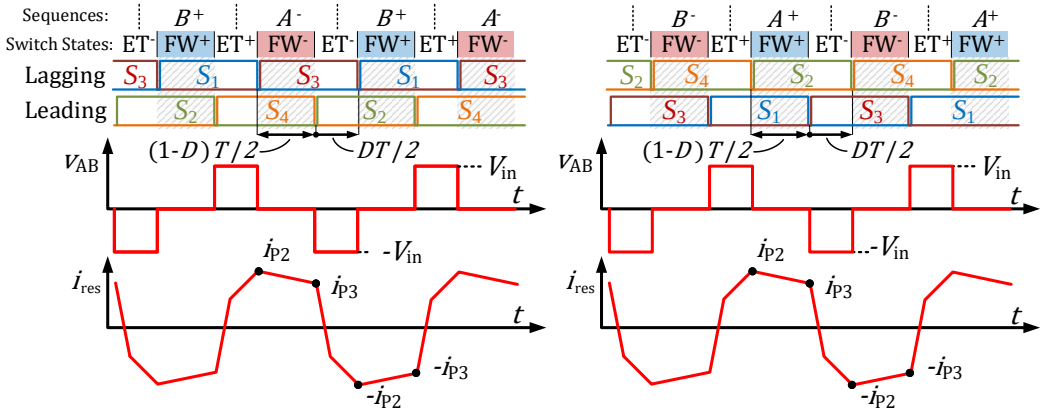


FIGURE 2.6: Phase-shift modulation (PSM) with inverter voltages and transformer current. Left: leading leg: S_2 and S_4; lagging leg S_1 and S_3. Right: leading leg: S_1 and S_3; lagging leg S_2 and S_4.

switches S_1 and S_3 are operated as the leading leg, the intervals repeat in the reverse order (see Figure 2.6, right):

$$\begin{aligned} &\mathbf{ET}^+(S_1, S_4) \rightarrow \mathbf{FW}^+(S_1, S_2) \rightarrow \\ &\mathbf{ET}^-(S_3, S_2) \rightarrow \mathbf{FW}^-(S_3, S_4). \end{aligned} \tag{2.2}$$

In an FW-ET transition, the transistors are switched at i_{P3}. Table 2.1a lists the switches that are turned off in an FW-ET transition. In an ET-FW transition, the switches commutate the current i_{P3}. Table 2.1b lists the four switches that are turned in the four potential transitions. It is evident that the lagging-leg switches are turned-off at i_{P2} while the leading-leg switches are commutated at i_{P3}. As the current i_{P3} may not be large enough to achieve ZVS, the leading-leg switches may be subject to incomplete ZVS losses $E_{on,iZVS}(i_{P3})$. Assuming ZVS for the lagging leg, the switching losses of the lagging-leg switches can be described as

$$P_{sw,PSM,lagg} = f_{sw} E_{off}(i_{P2}) \tag{2.3}$$

[1] the interval lengths last from one turn-off moment to the other because the current directly commutates to the switch's diode such that the voltage v_{AB} changes instantaneously. The length of the commutation interval is neglected in the figure.

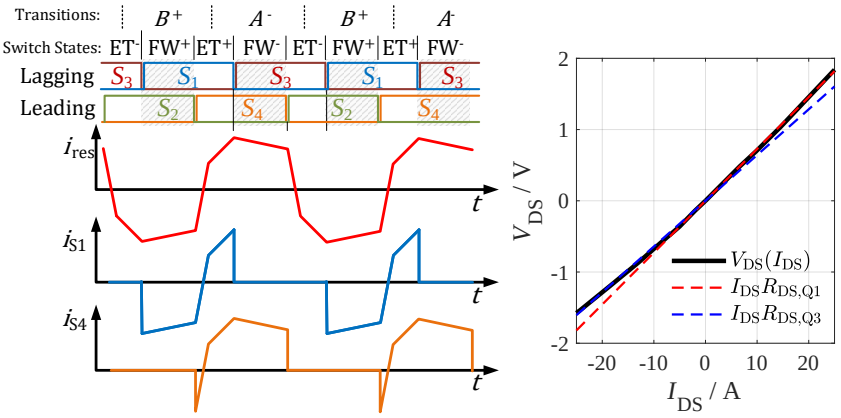
TABLE 2.1: The eight fundamental transitions in the phase-shift operation

Start \ End	ET^+	ET^-
FW^+	S_2	S_1
FW^-	S_3	S_4

(a) Switches that are turned off in a transition from a freewheeling interval to an energy-transfer interval (i_{P3}-Transition)

Start \ End	FW^+	FW^-
ET^+	S_4	S_1
ET^-	S_3	S_2

(b) Switches that are turned off in a transition from an energy-transfer interval to a freewheeling interval (i_{P2}-Transition)



(a) (b)

FIGURE 2.7: (a) Depiction of the switch currents i_{S1} and i_{S4}. While i_{S1} is negative the majority of time, i_{S4} is mostly positive. (b) transfer behavior of the silicon-carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) *C3M0075120J* [Cre19b]. For negative (3rd quadrant, Q3) currents, the on-state resistance is about 13 % compared to positive currents (1st quadrant, Q1) resulting in smaller conduction losses for the lagging leg.

while the switching losses of the leading-leg transistor can be calculated as[1]

$$P_{\text{sw,PSM,lead}} = f_{\text{sw}}[E_{\text{off}}(i_{\text{P3}}) + E_{\text{on,iZVS}}(i_{\text{P3}})]. \tag{2.4}$$

When analyzing the switch currents, it becomes evident that the lagging-leg switches conduct a negative freewheeling current while the freewheeling current of the leading-leg switches are positive.

The analysis of Table 2.1 shows that eight elementary sequences exist. However, the inverter must naturally transit from an ET^+ interval through any FW interval into an ET^- interval and from an ET^- interval through any FW interval into an ET^+

[1] in reality, the switching behavior of the transistors is influenced by a range of parameters (the current i_{P3}, the inductance L_s and L_m, the inductor current i_{Lg} and i_{mag} as well as the output capacitance of the primary ***and*** secondary switches). If i_{P3} is not large enough to achieve ZVS of the leading leg, a residual voltage, Δv, remains at the turn-on. The incomplete ZVS turn-on results in additional switching losses, which can be calculated using the formula derived in [Kas+16]. While for galvanically coupled converters, it is possible to calculate the voltage using data sheet parameters, this is not analytically possible for galvanically isolated converters that involve a magnetizing inductance L_m and the output capacitance of the secondary switches because the switching action influences the voltage of the output capacitance of the primary and secondary semiconductors as well as the magnetizing current. This stands in contrast to the derivation of the aforementioned paper where the energy formula can be solely solved for the voltage of the output capacitance of the primary semiconductor.

interval. This is a constraint such that four elementary sequences exist: the two elementary transitions an ET^{+} interval to a ET^{-} interval (labeled as type-A sequence)

$$\boldsymbol{A^{+}}: \ \mathbf{ET^{+}}(S_1, S_4) \rightarrow \mathbf{FW^{+}}(S_1, S_2) \rightarrow \mathbf{ET^{-}}(S_2, S_3) \tag{2.5}$$

$$\boldsymbol{A^{-}}: \ \mathbf{ET^{+}}(S_1, S_4) \rightarrow \mathbf{FW^{-}}(S_3, S_4) \rightarrow \mathbf{ET^{-}}(S_2, S_3) \tag{2.6}$$

and the two possible transitions from ET^{-} to ET^{+} (labeled type-B sequence):

$$\boldsymbol{B^{+}}: \ \mathbf{ET^{-}}(S_2, S_3) \rightarrow \mathbf{FW^{+}}(S_1, S_2) \rightarrow \mathbf{ET^{+}}(S_1, S_4) \tag{2.7}$$

$$\boldsymbol{B^{-}}: \ \mathbf{ET^{-}}(S_2, S_3) \rightarrow \mathbf{FW^{-}}(S_3, S_4) \rightarrow \mathbf{ET^{+}}(S_1, S_4). \tag{2.8}$$

Assuming that these sequences start in the middle of the ET intervals, they are half a period in length. Table 2.2 shows in which sequence the polarity of the switch current is positive or negative[1]. The analysis shows that an A-type and B-type sequence is necessary, to achieve equal conduction behavior for all switches.

TABLE 2.2: Polarity of the switch current in the freewheeling interval i_{Si}^{FW} for all four elementary sequences

	Sequence	
Switch \ Polarity	$i_{Si}^{\mathrm{FW}} > 0$	$i_{Si}^{\mathrm{FW}} < 0$
S_1	A^{+}	B^{+}
S_2	B^{+}	A^{+}
S_3	B^{-}	A^{-}
S_4	A^{-}	B^{+}

[1] for the PSFB, the polarity of the switch current does not change in the freewheeling interval (assuming steady state). When employing the LLC converter, however, the resonant current may change polarity during this interval due to the resonant voltage [Liu+16b]. This behavior results in a loss of ZVS, which in turn leads to a hard turn-on. Therefore, this mode of operation should be avoided.

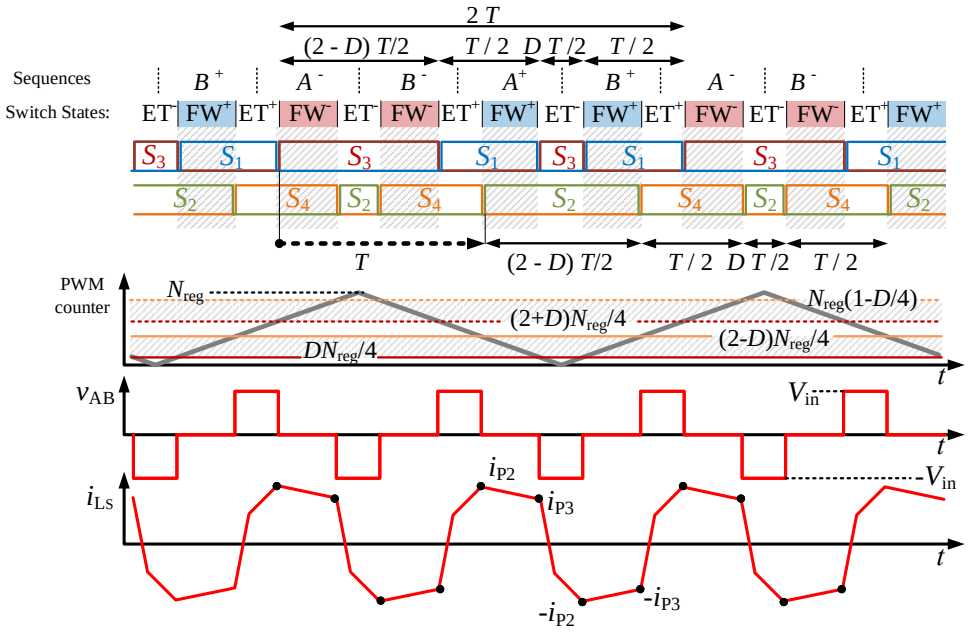


FIGURE 2.8: Alternating asymmetrical phase-shift modulation (a²PSM) of the LLC converter operated with $D = 0.35$. The modulation consists of intervals of the length $(1-D)T$, $T/2$, DT and $T/2$, which is phase shifted for the half bridges by T. The pulses of the switches thus repeat their pattern every $2T$ ($T_{mod} = 2T$).

A4 2-period alternating asymmetrical phase-shift modulation

this section has been previously published in parts in [Reh+21d] *and the presented method has been applied for patent in* [Reh+21b].

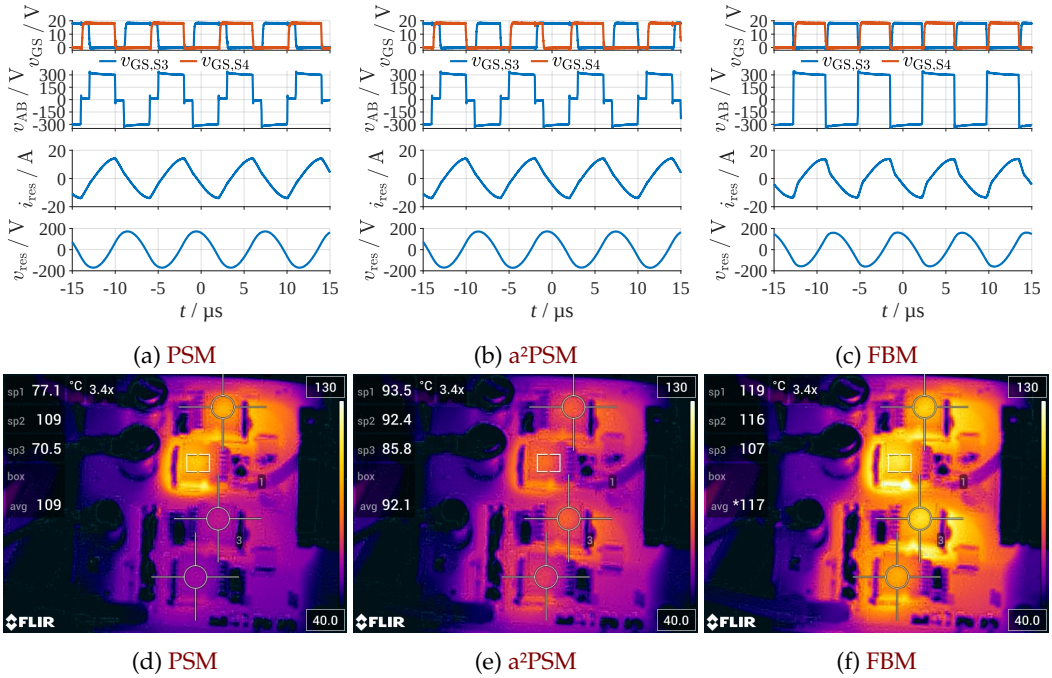
To achieve equal losses for all switches to avoid thermal hotspots, it is necessary to utilize a modulation that results in equal switching and conduction conditions for all switches. A modulation achieving equal losses for all switches is proposed in [Mih04]. This section provides a comprehensive analysis of this pulse pattern to propose additional modulations of increased lengths in 2.1.1A5 that result in a special common-mode behavior.

To achieve equal conduction and switching losses for all switches, the sequences of (2.5)-(2.8) must appear equally often in a given sequence. Since the conventional phase-shift modulation consists of the sequence $A^- - B^+$ (as in Figure 2.6, left) or of the sequence $A^+ - B^-$ (as in Figure 2.6, right), the modulation leads to an imbalanced loss distribution.

The alternating asymmetrical phase-shift modulation (a²PSM)[1] visualized in Figure 2.8 repeats every two periods ($T_{mod} = 2T$) and consists of the sequence

$$\begin{aligned} &\mathbf{ET^+}(S_1,S_4) \rightarrow \mathbf{FW^+}(S_1,S_2) \rightarrow \\ &\mathbf{ET^-}(S_3,S_2) \rightarrow \mathbf{FW^+}(S_1,S_2) \rightarrow \\ &\mathbf{ET^+}(S_1,S_4) \rightarrow \mathbf{FW^-}(S_3,S_4) \rightarrow \\ &\mathbf{ET^-}(S_3,S_2) \rightarrow \mathbf{FW^-}(S_3,S_4), \end{aligned} \tag{2.9}$$

[1] in [Mih04] the modulation is named "*uniform-loss modulation*". However, as [LC14; LSC15] proposed a control method to interchange the leading leg with the lagging leg, which achieved the same, this modulation will be referred to as alternating asymmetrical phase-shift modulation (a²PSM).



(a) PSM (b) a²PSM (c) FBM

(d) PSM (e) a²PSM (f) FBM

FIGURE 2.9: Experimental measurement results for a low VTR operating point: PSM (a,d), a²PSM (b,e) and FBM (c,f) for a gate resistance of $R_g = 19.5\,\Omega$. By employing phase-shift modulation, the maximum switch temperature is reduced from 119 ° to 109 °C whereas the a²PSM reduced the maximum switch temperature to 93.5 °C by another 16 K (parameters: $\text{Config}_{2.1b}$, $\text{Config}_{2.1c}$).

which translates into the $A^+ - B^+ - A^- - B^-$-sequence. In this modulation, every switch is once switched at the large current value (i_{P2}) and once at the smaller current value (i_{P3}) while every elementary sequence of (2.5)-(2.8) appears once for all switches in the modulation period, T_{mod}. Conduction intervals of the lengths $(2-D)T/2$, $T/2$, $DT/2$ and $T/2$ result, which can be implemented using one PWM up-down counter with two comparative values leading to gate signals that are phase-shifted for one leg by T. Referring to Figure 2.8[1], in leg S_1-S_3 the switch S_3 is turned off at a counter level of $DT_{reg}/4$ on up-count while being turned on at the same level on down-count (the maximum value of the counter is T_{reg}). On up-count S_3 is turned on at $(2+D)T_{reg}/4$ while being turned off at the same level on down-count. Generally, this type of modulation can be easily implemented on a digital signal processor (DSP)/microcontroller (e.g. in TI C2000 controllers[2]). Over the modulation period T_{mod} every switch is switched once at i_{P3} and once at i_{P2} such that the switching losses of each switch can be calculated as

$$P_{sw,a2PSM} = \frac{f_{sw}}{2}[E_{off}(i_{P2}) + E_{off}(i_{P3}) + E_{on,iZVS}(i_{P3})]. \tag{2.10}$$

[1] the modulation of (2.9) is operated to result in turn-on interval lengths of $T/2$ for the switches S_1 and S_4. It is also possible to apply the a²PSM with the reversed order of the intervals $ET^+ \to FW^+ \to ET^- \to FW^- \to ET^+ \to FW^- \to ET^- \to FW^+$ ($A^+ - B^- - A^- - B^+$-sequence), which results in turn-on interval lengths of $T/2$ for the switches S_2 and S_3. The described derivations are valid for both modulation schemes; both modulations result in an equal turn-off and conduction stress. Therefore, Figure 2.8 shows the modulation of (2.9) only.

[2] by using the action-qualifier control registers, AQCTL.

To prove that the root mean square (RMS) currents are equal for all MOSFETs , ξ shall be introduced as the integrated squared current. During the ET$^-$ intervals it applies

$$\xi_{\mathrm{ET}}^{-} = \int\limits_{\Delta t_{\mathrm{ET}^-}} i_{\mathrm{ET}^-}^2 \mathrm{d}t = \int\limits_{DT/2} i_{\mathrm{ET}^-}^2 \mathrm{d}t. \tag{2.11}$$

For symmetry reasons ($i_{\mathrm{ET}^-}(t) = -i_{\mathrm{ET}^+}(t)$, $\Delta t_{\mathrm{ET}^-} = \Delta t_{\mathrm{ET}^+} = DT/2$), the integral of the squared current in the ET$^+$-interval, $\xi_{\mathrm{ET}^-}^{+}$, is equal to (2.11) ($\xi_{\mathrm{ET}}^{+} = \xi_{\mathrm{ET}}^{-} = \xi_{\mathrm{ET}}$). The same applies for the freewheeling intervals:

$$\xi_{\mathrm{FW}}^{-} = \int\limits_{\Delta t_{\mathrm{FW}^-}} i_{\mathrm{FW}^-}^2 \mathrm{d}t = \int\limits_{(1-D)T/2} i_{\mathrm{FW}^-}^2 \mathrm{d}t \tag{2.12}$$

with $\xi_{\mathrm{FW}}^{-} = \xi_{\mathrm{FW}}^{+} = \xi_{\mathrm{FW}}$. Through (2.11) and (2.12), the RMS currents $I_{\mathrm{S},k}$ of all switches S_k ($k \in \{1,2,3,4\}$) can be calculated as

$$I_{\mathrm{S},k} = \sqrt{\frac{1}{2T}(2\xi_{\mathrm{FW}} + 2\xi_{\mathrm{ET}})} = \sqrt{\frac{1}{T}(\xi_{\mathrm{FW}} + \xi_{\mathrm{ET}})} \tag{2.13}$$

whereas the RMS transformer current is calculated as

$$I_{\mathrm{Ls}} = \sqrt{\frac{1}{T}(2\xi_{\mathrm{FW}} + 2\xi_{\mathrm{ET}})}. \tag{2.14}$$

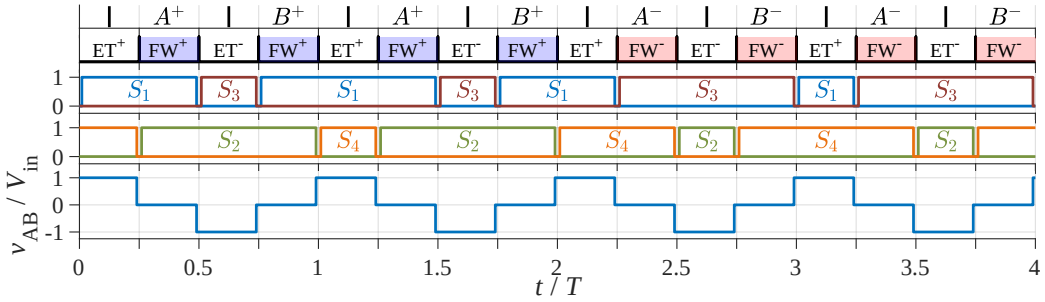
Substituting (2.14) in (2.13) results in

$$I_{\mathrm{S},k} = \frac{1}{\sqrt{2}} I_{\mathrm{Ls}} \tag{2.15}$$

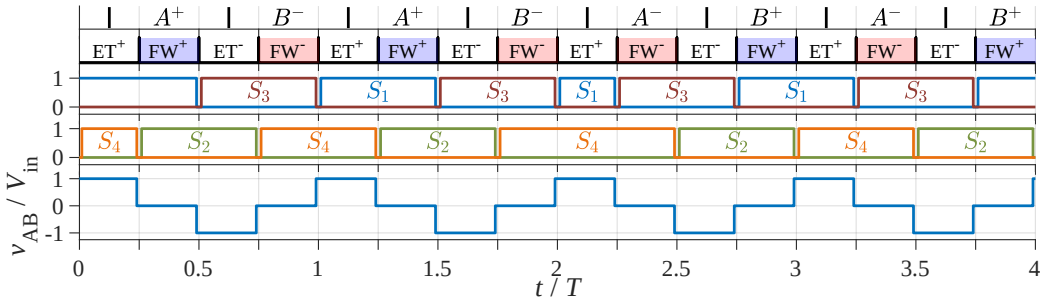
proving that all switches are stressed by equal RMS currents. Furthermore, every switch conducts two consecutive freewheeling intervals such that the conduction losses are equally distributed even for a nonlinear transfer behavior. While for the conventional PSM, a difference in conduction losses results from the unequal transfer behavior of the MOSFETs (cf. Figure 2.7), this effect is suppressed by the equal conduction behavior for the a²PSM. Every switch performs an A-type and B-type sequence such that the switches conduct the freewheeling current once in the positive and once in the negative direction.

An experimental comparison of the PSM, the a²PSM and the FBM is provided in Figure 2.9 for a gate resistance of $R_g = 19.5\,\Omega$. The MOSFETs are bottom-cooled through the printed circuit board (PCB) (*see* Section 3.4.2) such that the case temperature can be very well measured by an IR-camera. Figure 2.9 (a-c) depicts measurement results of the low-side MOSFETs ($v_{\mathrm{GS,S3}}$, $v_{\mathrm{GS,S4}}$), the resonant current i_{res}, the resonant voltage v_{res} and inverter voltage v_{AB}. Considering the inverter voltage and the resonant current and voltage shown in Figure 2.9 (a-c), both modulations result in equal shapes of the currents and voltages in the resonant circuit. Figure 2.9 (d-f) show a thermal analysis of the MOSFET temperature. For the conventional phase-shift modulation, the case temperature of the lagging leg Figure 2.9d (top) is about 32 K higher than the temperature of the leading leg (Figure 2.9d (bottom)). Employing the a²PSM that is visualized in Figure 2.9e, the case temperatures are approximately equal with a deviation of only about 1.3 K[1]. The average temperature is hereby approximately equal to the mean temperature of the PSM visualized in Figure 2.9d. By using this modulation, the maximum temperature is reduced by about 16 K. Comparing these results to the FBM shows that the maximum switch temperature is significantly larger than both the PSM and the a²PSM. The measurement results in Figure 2.9f show a maximum temperature of about 119 °C, which is

[1] the bottom switch of the depicted measurements hereby shows a better connection to the heatsink, which is likely caused by the fact that it is closer to the fan. It is hereby a clear outlier.



(a) $A^+ - B^+ - A^+ - B^+ - A^- - B^- - A^- - B^-$-sequence



(b) $A^+ - B^- - A^+ - B^- - A^- - B^+ - A^- - B^+$-sequence

FIGURE 2.10: Two examples of a four-period a²PSM modulation. (a) $4T$ a²PSM (1); (b): $4T$ a²PSM (2).

about 10 K higher than the PSM and about 26 K larger than the a²PSM.

A5 Alternating asymmetrical phase-shift modulation of increased lengths

this section has been previously published in parts in [Reh+21d].

While the smallest possible modulation length to achieve equal losses for all switches is $2T$ (two periods of the resonant current), it is also possible to construct modulation sequences of longer lengths that achieve this goal. In the modulation of (2.9), every fundamental sequence of (2.5)-(2.8) appears once. For longer sequences, the fundamental sequences again need to appear equally often. While this increases the modulation complexity, the fundamental frequency of the voltages v_A and v_B is reduced and the common-mode noise, thus, altered. It is possible to construct a multiple of pulse patterns with longer pulse lengths ($T_{mod} > 2T$) that achieve equal losses for all MOSFETs . There are two potential sequences A and B, which can be placed individually and need to occur equally often. Thus, in an a²PSM of length T_{mod}, there are T_{mod}/T sequences of type A (and B) and $T_{mod}/(2T)$ sequences of type A^+/A^- (and B^+/B^-). Therefore, there are $\binom{\frac{T_{mod}}{T}}{\frac{T_{mod}}{2T}}$ possibilities of A^+/A^- placements and an equal number of B^+/B^- placements. Considering that the modulation starts with a defined sequence (resulting in a division with two), the number of pulse patterns of length T_{mod} can be calculated as

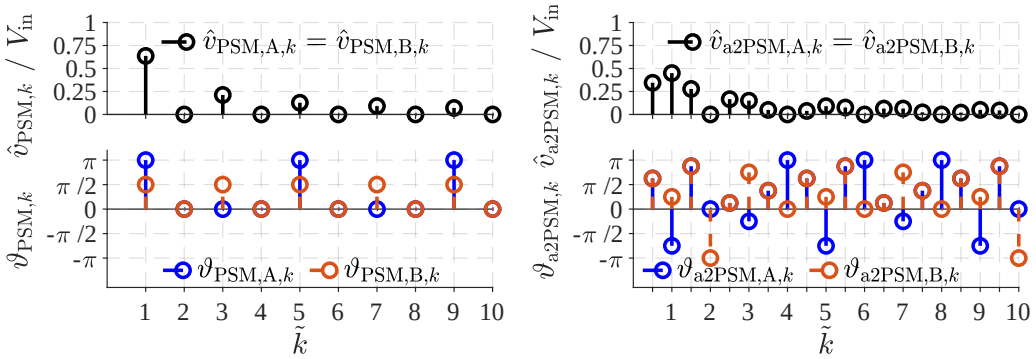
$$N = \frac{1}{2}\binom{\frac{T_{mod}}{T}}{\frac{T_{mod}}{2T}}^2. \tag{2.16}$$

This number includes sequences that repeat within the modulation period T_{mod} also. The number of unique pulse patterns is calculated numerically and is displayed in Table 2.3.

TABLE 2.3: Number N of unique a²PSM patterns for various pulse lengths

T_{mod} / T	2	4	6	8
N	2	8	66	606

Two potential four-period long sequences are displayed in Figure 2.10. Figure 2.10a shows a modulation where for one half of the modulation length, only FW^{+} intervals are used whereas for the rest of the modulation, only FW^{-} intervals are employed. Figure 2.10b shows a modulation where the leading and lagging leg are interchanged every $2T$.



(a) PSM (b) a²PSM

FIGURE 2.11: Harmonics of the voltages v_{A} and v_{B} for PSM (a) and a²PSM (b). The modulation changes the harmonics of the switched potentials to improve the EMC.

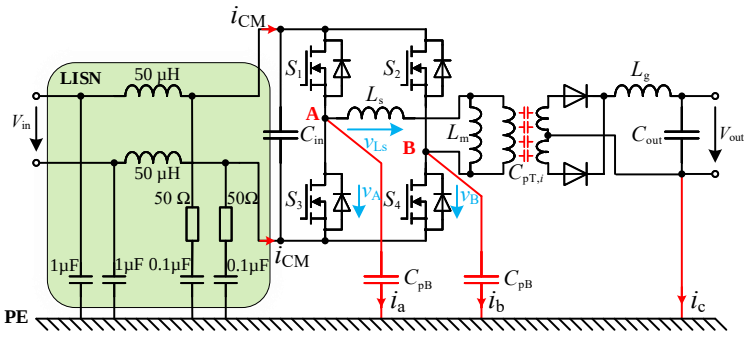


FIGURE 2.12: Common-mode model of the PSFB [CCB03; XRY18; Cha+14; CW15].

A6 Common-mode implications of the a²PSM With the described modulation, the half-bridge voltages v_{A} and v_{B} (cf. Figure 2.12) are altered. While the differential-mode noise is affected by the input current of the converter [RNK10; Fre+20] that remains unaltered by the modulation, the pulse pattern results in a different common mode (CM) noise compared to the original PSM. Most notably, the fundamental frequency of the CM noise is halved. CM noise is caused by voltages with large $\mathrm{d}v/\mathrm{d}t$ that are linked through a parasitic capacitance to protective earth (PE) as well as through the inter winding capacitance of the isolation transformer if the secondary ground is connected to PE [CCB03; XRY18; Cha+14; CW15]. Areas with large $\mathrm{d}v/\mathrm{d}t$ generate a common-mode current that flows through the protected ground to the source. In a full-bridge converter[1], the two voltages v_{A} and v_{B} as well as the inductor voltage v_{Ls} (cf. Figure 2.12) exhibit large $\mathrm{d}v/\mathrm{d}t$ that generate common-mode noise leading to common-mode currents i_{CM} propagating through the circuit.

Using Fourier series analysis, the frequency spectrum of the voltages v_{a} and v_{b} can been calculated with

$$v_{\mathrm{A}}(t) = \sum_{k=0}^{\infty} \hat{v}_{\mathrm{A},k} \cos(2\pi k f_{\mathrm{mod}} t + \vartheta_k). \tag{2.17}$$

[1] the following analysis shows the derivation for a PSFB. However, it is equally valid for an LLC converter if the resonant capacitor is evenly distributed to both sides of the transformer.

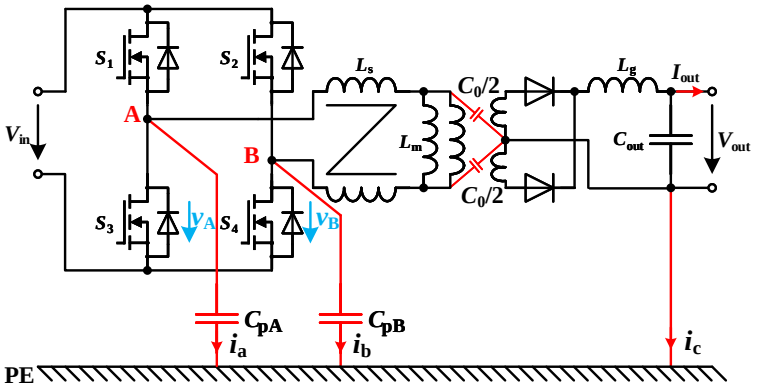
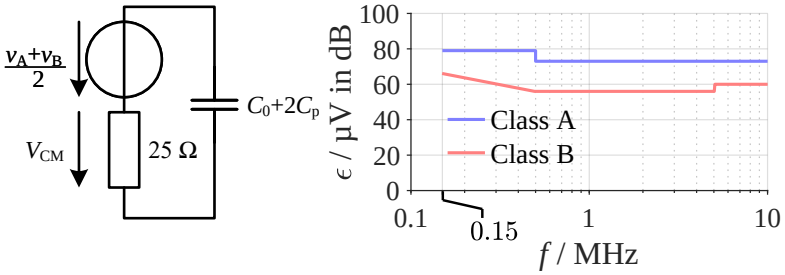


FIGURE 2.13: Simplified common-mode model of the PSFB considering a symmetrical series inductance L_s and a symmetrical transformer as derived in [XRY18].



(a) (b)

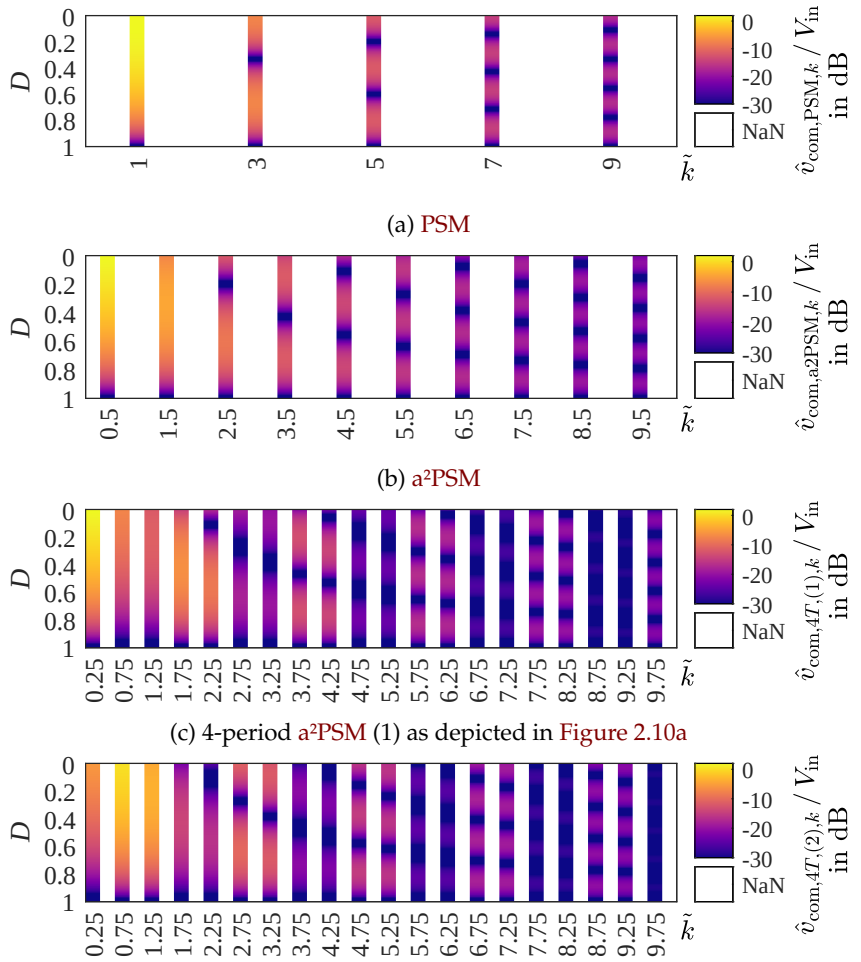
FIGURE 2.14: (a) Equivalent circuit model of the PSFB with a symmetrical series inductor and transformer as derived in [XRY18]. (b) EN55032 conducted emission (ϵ) limits (quasi-peak). Below 150 kHz no limit is defined for this norm. By placing the fundamental frequency below 150 kHz employing the a²PSM, the largest noise amplitude is placed outside the norm while the converter is actually operated above 150 kHz.

The frequency spectrum of v_A and v_B is depicted for $D = 0.5$ in Figure 2.11. To compare equal frequencies $\tilde{k}$ is introduced as

$$\tilde{k} = \frac{T}{T_{\text{mod}}} k. \tag{2.18}$$

The analysis shows that the amplitude of the harmonics of the fundamental oscillation frequency are substantially reduced for the a²PSM. Furthermore, it is evident that for $\tilde{k} = \{0.5, 1.5, 2.5...\}$ $V_{\text{a2PSM,A}}$ and $V_{\text{a2PSM,B}}$ are in phase while for $\tilde{k} = \{1, 2, 3...\}$ they are opposite in phase ($\Delta\varphi = |\varphi_{\text{a2PSM,A},k} - \varphi_{\text{a2PSM,B},k}| = \pi$).

The circuit can be modeled with the line impedance stabilization network (LISN) as depicted in Figure 2.12 [XRY18; XRY16; ZMA17] (model of an LLC converter is equivalent). With a symmetrical series inductance L_s and a symmetrical transformer, the model simplifies to the circuit depicted in Figure 2.13 such that the effect of the series inductance on the common-mode noise is mitigated [XRY18] leading to a load-independent behavior. The equivalent circuit model of this structure has been derived in [XRY18] and is depicted in Figure 2.14 assuming $C_{\text{pA}} = C_{\text{pB}} = C_{\text{p}}$. The two nodal voltages v_A and v_B generate a collective common-mode noise



(a) PSM

(b) a²PSM

(c) 4-period a²PSM (1) as depicted in Figure 2.10a

(d) 4-period a²PSM (2) as depicted in Figure 2.10b

FIGURE 2.15: Collective common-mode noise source voltage v_{com} plotted over the duty cycle. Utilizing the a²PSM, the electromagnetic spectrum can be altered.

$$v_{\mathrm{com}} = \frac{v_{\mathrm{A}} + v_{\mathrm{B}}}{2} \tag{2.19}$$

Referring to Figure 2.11 frequencies of $\tilde{k} = \{1, 2, 3...\}$ cancel each other out, substantially reducing the induced common-mode noise for the a²PSM at these frequencies. Since the differential-mode noise has its harmonics at $\tilde{k} = \{1, 2, 3...\}$, this implies that the differential-mode and common-mode noise are now emitting at ***different*** frequencies. To evaluate the noise voltage for all duty cycles, the spectrum is displayed in Figure 2.15 with the duty cycle displayed on the ordinate and the frequency displayed on the abscissa. The noise amplitude is displayed as a color value.

The collective CM noise source voltage is visualized in Figure 2.16 for $D = 0.5$. The analysis shows that the CM noise amplitude of the a²PSM does not exceed the amplitude of the PSM. As the fundamental frequency of the a²PSM is moved to smaller frequencies (potentially below the electromagnetic interference (EMI) frequency of 150 kHz, cf. Figure 2.14,b), higher-order a²PSMs may prove to be especially beneficial as these reduce the CM noise at low frequencies significantly. An

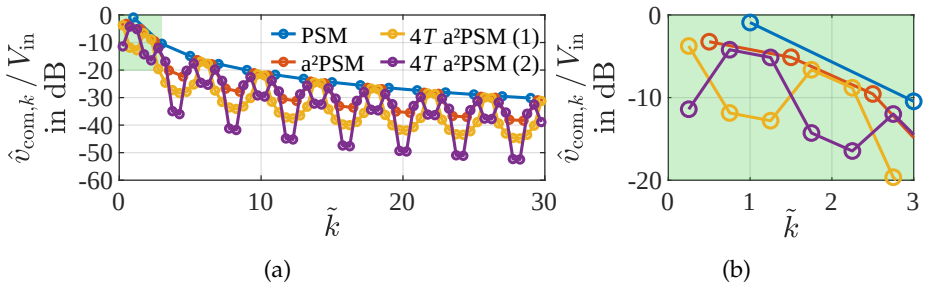


FIGURE 2.16: Collective common-mode noise source voltage v_{com} for the PSM and various a²PSMs at $D = 0.5$. (a) spectrum over the first 30 fundamental frequencies, (b) zoom to the first three fundamental frequencies.

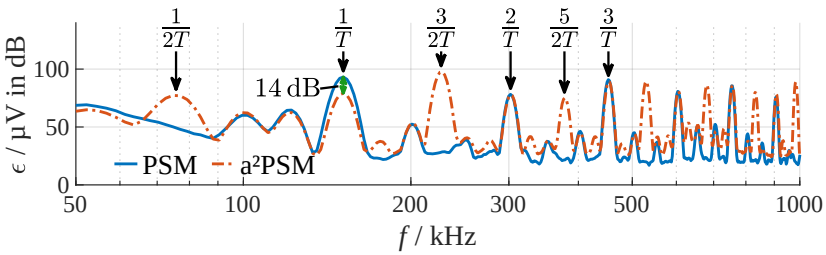
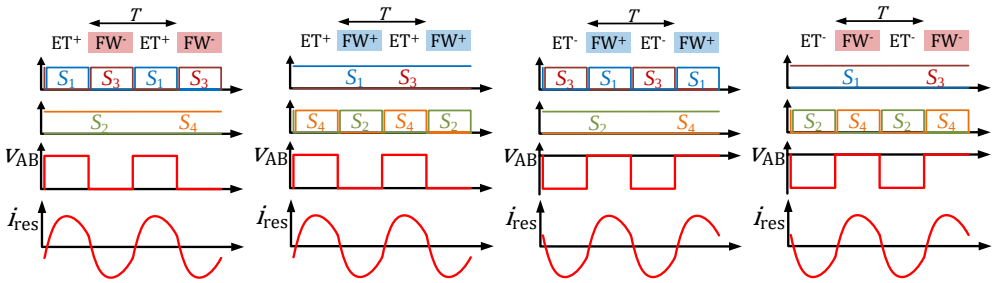


FIGURE 2.17: Electromagnetic emission (CM and differential mode (DM)) of the PSM and 2-period a²PSM measured on an LLC resonant converter operated at $f = \frac{1}{T} = 151\,\mathrm{kHz}$ and $D = 0.24$. The a²PSM reduces the CM emission at the operating frequency by 14 dB (parameters: Config$_{2.1d}$).

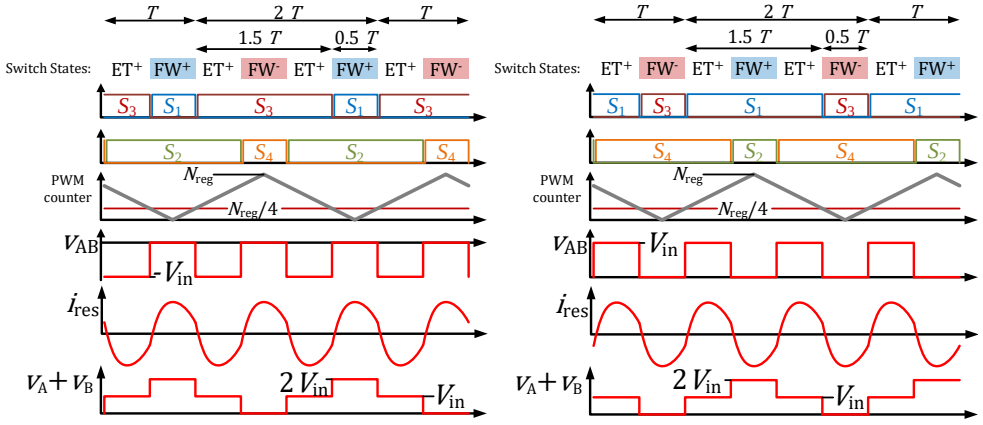
example is that close to the fundamental oscillation frequency ($\tilde{k} = 1$), the $4T$ a²PSM (1) modulation reduces the noise source amplitude by about 10 dB compared to the standard PSM if the fundamental frequency of v_{A} and v_{B} is placed below 150 kHz.

The a²PSM and PSM are employed on the LLC converter of Table 3.2(a) that is depicted in Figure 3.23a (non-symmetrical design, rudimentary EMI filter). The electromagnetic emission (CM and DM emission combined) is depicted for $f = 151\,\mathrm{kHz}$ and $D = 0.24$ in Figure 2.17. For the operating frequency, the electromagnetic emission is reduced by 14 dB. Emissions at half the operating frequency and 1.5 times the operating frequency are clearly visible for the a²PSM. However, as the emissions at half the operating frequency are outside the norm spectrum, they are considered irrelevant.



(a) HBM (switch S_4 on) (b) HBM (switch S_1 on) (c) HBM (switch S_2 on) (d) HBM (switch S_3 on)

FIGURE 2.18: All four possible HBM applied to an LLC resonant converter.



(a) FD-HBM ($v_{AB} \in \{0, V_{in}\}$) (b) FD-HBM ($v_{AB} \in \{-V_{in}, 0\}$)

FIGURE 2.19: FD-HBM employed on the LLC converter. The modulation consists of intervals of the length $3T/2$ and $T/2$, which are phase shifted for one bridge leg by T. The pulses of the switches thus repeat their pattern every $2T$.

B Half-bridge modulation schemes

To cover the wide voltage-transfer ratio, it has been suggested to operate an LLC full-bridge converter in half-bridge mode [Lia+10; JI15a; JI16; Sun+18; Reh+20a; Reh+20b; RSB21]. One MOSFET is hereby turned on continuously whereas the other MOSFET of the respective bridge leg is permanently turned off. While in the conventional full-bridge operation, the inverter voltage is pulsed between the two voltage levels $v_{AB} \in \{-V_{in}, V_{in}\}$, in half-bridge mode the inverter voltage is pulsed between the two voltage levels $v_{AB} \in \{-V_{in}, 0\}$ or $v_{AB} \in \{0, V_{in}\}$. The resonant capacitor hereby acts as a blocking capacitor as the average voltage is half the input voltage. This reduces the gain by a factor of two making this mode of operation especially useful for small VTRs, whereas for large voltage-transfer ratios the conventional full-bridge operation should be employed. For intermediate gains and loads, phase-shift operation may be beneficial to reduce the switching frequency and increase the efficiency. To change the operating mode from full-bridge to half-bridge operation and reverse, an on-the-fly topology morphing mode is proposed in [JI15a; JI16].

B1 Conventional half-bridge modulation

this section has been previously published in parts in [Reh+21e].

When employing the conventional HBM, one leg of the inverter is not pulsed – one switch is permanently turned on while the other is turned off. All potential half-bridge modulation schemes are depicted in Figure 2.18. Intervals with $v_{AB} = 0$ are depicted in blue for FW$^+$-intervals and in red for FW$^-$-intervals. Figure 2.18a and Figure 2.18b show modulations that result in a positive (or zero) inverter voltage (the average resonant capacitor voltage is $\bar{v}_{res} = \frac{1}{2}V_{in}$) whereas Figure 2.18c and Figure 2.18d show the modulations that result in only negative (or zero) inverter voltages (the average resonant capacitor voltage is $\bar{v}_{res} = -\frac{1}{2}V_{in}$). Note that the modulations in Figure 2.18b and Figure 2.18c cannot be achieved with bootstrap drivers since the high-side switches cannot be permanently turned on with this driver supply. It is evident that the modulations in Figure 2.18a and Figure 2.18b as well as the modulations in Figure 2.18c and Figure 2.18d result in an equal inverter output voltage v_{AB} and, thus, in equal resonant currents.

Assuming that MOSFETs are employed as the inverter switches, the losses of the individual switches that are pulsed complementary (*compl*) can be calculated as

$$P^{\mathrm{HBM}}_{\mathrm{compl}} = \overbrace{\frac{1}{2} I^2_{\mathrm{res}} R_{\mathrm{ds,on}}(\vartheta_{\mathrm{j}})}^{P^{\mathrm{HBM}}_{\mathrm{cond,compl}}} + \overbrace{f_{\mathrm{sw}} E_{\mathrm{off}}(i_{\mathrm{off}})}^{P^{\mathrm{HBM}}_{\mathrm{sw,compl}}} \tag{2.20}$$

where ϑ_{j} is the junction temperature of the MOSFETs , E_{off} are the losses of a turn-off at the current i_{off}, f_{sw} is the switching frequency and I_{res} is the RMS value of the resonant current i_{res}. In stationary operation i_{off} and ϑ_{j} can be considered constant.

To evaluate the loss distribution, the losses of these MOSFETs are divided into the conduction losses $P^{\mathrm{HBM}}_{\mathrm{cond,compl}}$ and the switching losses $P^{\mathrm{HBM}}_{\mathrm{sw,compl}}$. The MOSFET that is permanently turned (*p-on*) on is stressed with the full resonant current such that the losses can be calculated as

$$P^{\mathrm{HBM}}_{\mathrm{p-on}} = I^2_{\mathrm{res}} R_{\mathrm{ds,on}}(\vartheta_{\mathrm{j}}). \tag{2.21}$$

Assuming that the same MOSFET type is employed for all switches and neglecting temperature dependencies of the on-state resistance $R_{\mathrm{ds,on}}$, the overall inverter losses can be calculated as $P_{\mathrm{inv}} = 2I^2_{\mathrm{res}} R_{\mathrm{ds,on}} + 2 f_{\mathrm{sw}} E_{\mathrm{off}}(i_{\mathrm{off}})$. The conduction losses of the MOSFET that is permanently turned on are about twice as large as the conduction losses of the pulsed switches ($P^{\mathrm{HBM}}_{\mathrm{p-on}} = 2P^{\mathrm{HBM}}_{\mathrm{cond,compl}}$). This may be a problem for converters that employ switches where conduction losses are the dominant loss contributor – the switches have to be designed for a lower on-state resistance, which results in larger converter costs.

B2 Frequency-doubler modulation

this section has been previously published in parts in [Reh+21e].

If an LLC full-bridge converter is operated in half-bridge mode, one switch conducts the full resonant current while exhibiting no switching losses. The respective other switch of this half-bridge is permanently turned off such that this switch is not stressed at all. The switches of the pulsing half bridge conduct the resonant current for one half of a period such that they are stressed with half the conduction losses compared to the switch that is permanently turned on. However, they exhibit turn-off losses. This leads to imbalanced inverter losses. For dominant conduction losses, the switch that is permanently turned on is stressed with much larger losses than the pulsing switches. If the switching losses are dominant, the pulsing switches exhibit larger losses compared to the switch that is permanently turned on.

In comparison to the half-bridge modulation, the frequency-doubler modulation achieves the same inverter voltage. The modulation is proposed for a stacked-bridge inverter in [IAP16] and has since then be applied for the conventional full-bridge LLC converter in [Lin+16; Wei+20c; WM20; WLM20b]. As this modulation emulates the half-bridge modulation, it will be referred to as *frequency-doubler half-bridge modulation* (FD-HBM) in this thesis. This modulation has previously been discussed as an alternative to the conventional half-bridge modulation. However, to the author's best knowledge, the benefit of the FD-HBM with respect to individual switch losses and, thus, to the maximum junction temperature has not yet been analyzed and the loss distribution has not been investigated for different setups.

By considering Figure 2.18, it is evident that two modulations achieve exactly the same inverter voltage. Therefore, it is possible to interchange the freewheeling intervals FW^{+} and FW^{-} as depicted in Figure 2.19 without modifying the inverter voltage v_{AB}. By employing this concept, asymmetrical pulse patterns result for both half bridges, which are phase-shifted by T. Considering Figure 2.19, the modulation utilizes an up-down counter to achieve the pulse pattern where the compare values are $N_{\mathrm{reg}}/4$ for one bridge leg and $3N_{\mathrm{reg}}/4$ for the other bridge leg. This results in the necessary turn-on times of $T/2$ and $3T/2$. It is equally possible to employ any other counter. However, an up-down counter is beneficial in the on-the-fly morphing process (*see* Section 2.1.2A), and can also be employed to achieve balanced losses for an operation in PSM (*see* Section 2.1.1A4). This avoids the necessity of a PWM reconfiguration [LC14; LSC15].

Referring to Figure 2.19, two types of MOSFETs can be distinguished:
the MOSFETs that are turned on 75 % of the time, resulting in high losses and the MOSFETs that are turned on for the remaining 25 % of the time, resulting in lower losses. The high losses $P_{\mathrm{high}}^{\text{FD-HBM}}$ of the switches that are turned on 75 % of the time can be calculated as

$$P_{\mathrm{high}}^{\mathrm{FD-HBM}} = \overbrace{\frac{3}{4} I_{\mathrm{res}}^{2} R_{\mathrm{ds,on}}(\vartheta_{\mathrm{j}})}^{1.5\, P_{\mathrm{cond,compl}}^{\mathrm{HBM}} = 0.75\, P_{\mathrm{p-on}}^{\mathrm{HBM}}} + \overbrace{\frac{1}{2} f_{\mathrm{sw}} E_{\mathrm{off}}(i_{\mathrm{off}})}^{0.5\, P_{\mathrm{sw,compl}}^{\mathrm{HBM}}} . \tag{2.22}$$

The overbrace puts these losses in relation to the conventional HBM while neglecting temperature dependencies of the on-state resistance. The switches are turned off every two periods T of the resonant current while the switches conduct for three quarters of a period. The lower losses $P_{\mathrm{low}}^{\mathrm{FD-HBM}}$ of the switches that are only turned

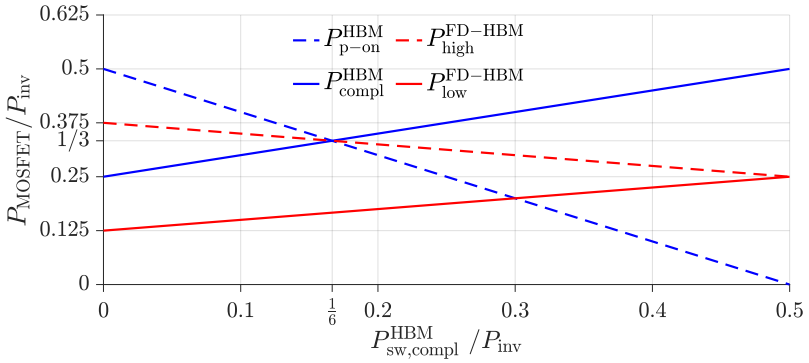


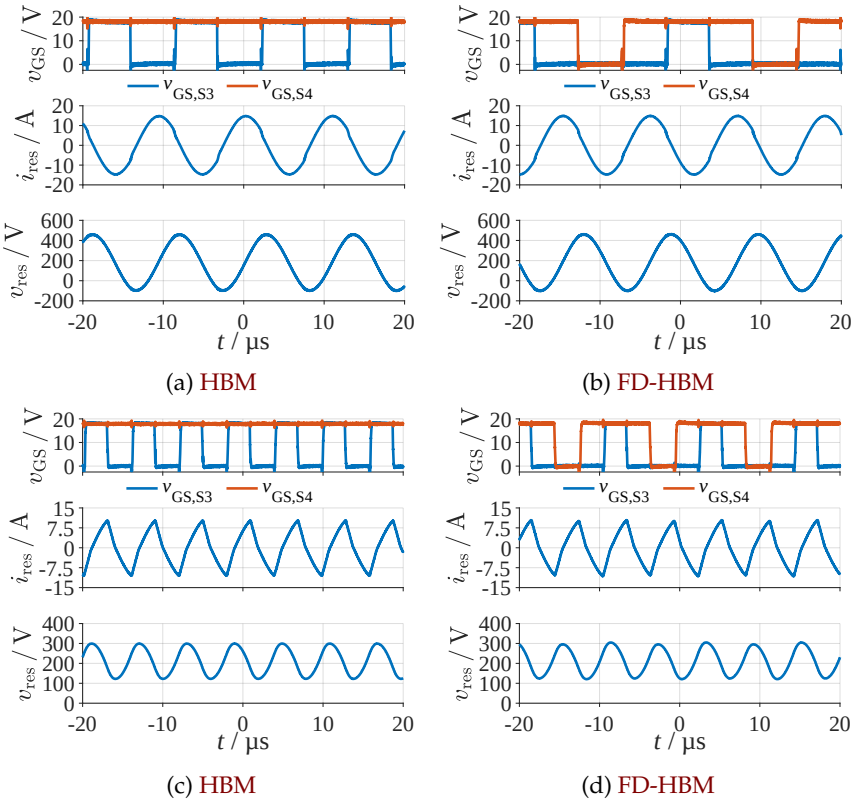
FIGURE 2.20: Loss analysis of the HBM and the FD-HBM assuming a constant on-state resistance $R_{\mathrm{ds,on}}$.

on for 25 % of the time on the other hand can be calculated as

$$P^{\mathrm{FD-HBM}}_{\mathrm{low}} = \overbrace{\frac{1}{4} I^2_{\mathrm{res}} R_{\mathrm{ds,on}}(\vartheta_{\mathrm{j}})}^{0.5\, P^{\mathrm{HBM}}_{\mathrm{cond,compl}} = 0.25\, P^{\mathrm{HBM}}_{\mathrm{p-on}}} + \overbrace{\frac{1}{2} f_{\mathrm{sw}} E_{\mathrm{off}}(i_{\mathrm{off}})}^{0.5\, P^{\mathrm{HBM}}_{\mathrm{sw,compl}}} . \tag{2.23}$$

Thus, the overall losses P_{inv} of this modulation are the same as in the conventional half-bridge modulation. To evaluate the performance of this modulation, the HBM and the FD-HBM shall be evaluated for different loss distributions of the conduction losses and the switching losses. The reference is the conventional HBM. Figure 2.20 shows a loss analysis assuming a constant on-state resistance $R_{\mathrm{ds,on}}$. The losses of the MOSFETs are depicted over the ratio of the switching losses $P^{\mathrm{HBM}}_{\mathrm{sw,compl}}$ to the overall losses of the operation P_{inv}. An abscissa value of $P^{\mathrm{HBM}}_{\mathrm{sw,compl}}/P_{\mathrm{inv}} = 0$ indicates that there are negligible switching losses in the overall loss breakdown of the inverter, whereas a value of $P^{\mathrm{HBM}}_{\mathrm{sw,compl}}/P_{\mathrm{inv}} = 0.5$ implies that there are negligible conduction losses in the overall inverter losses P_{inv}. The actual loss distribution hereby depends on the choice of MOSFETs and the operating point. For low turn-off currents, low switching frequencies, and wide-bandgap switches, the conduction losses may be more dominant than the switching losses whereas for higher switching frequencies, high turn-off currents, and (silicon) MOSFETs with more turn-off losses, the switching losses may be the dominant loss contributor.

Obviously, the FD-HBM distributes the losses more equally among all MOSFETs compared to the conventional HBM. While for $P^{\mathrm{HBM}}_{\mathrm{sw,compl}}/\ P_{\mathrm{inv}} < \frac{1}{6}$ (dominant conduction losses in $P^{\mathrm{HBM}}_{\mathrm{compl}}$), the switch that is permanently turned on experiences the largest losses, for $P^{\mathrm{HBM}}_{\mathrm{sw,compl}}/P_{\mathrm{inv}} > \frac{1}{6}$ (dominant switching losses in $P^{\mathrm{HBM}}_{\mathrm{compl}}$), the switches that are pulsed face the largest losses. The MOSFET being subject to the largest losses of the FD-HBM ($P^{\mathrm{FD-HBM}}_{\mathrm{high}}$) always shows lower or identical overall losses than the most-stressed MOSFET of the conventional HBM.
Only for $P^{\mathrm{HBM}}_{\mathrm{sw,compl}}/P_{\mathrm{inv}} = \frac{1}{6}$ where the overall conduction and switching losses are equal in $P^{\mathrm{HBM}}_{\mathrm{compl}}$ ($P^{\mathrm{HBM}}_{\mathrm{sw,compl}} = P^{\mathrm{HBM}}_{\mathrm{cond,compl}}$), the losses of the maximum stressed switches in the HBM are the same as the maximum stressed switches in the FD-HBM. However, considering the temperature-dependent on-state resistance, the FD-HBM is also likely to perform better at this point.



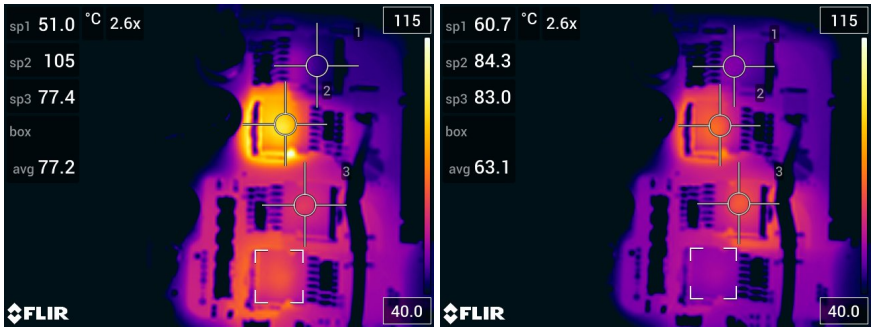
(a) HBM (b) FD-HBM

(c) HBM (d) FD-HBM

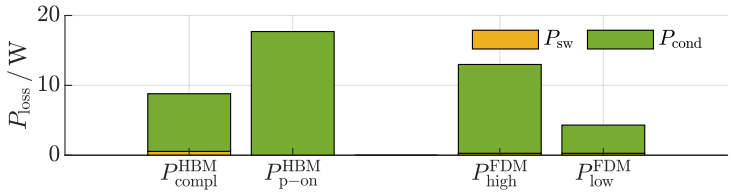
FIGURE 2.21: Experimental measurement results of the FD-HBM and HBM for two different operating points and setups. Depicted are the low-side gate voltages $v_{GS,S3}$ and $v_{GS,S4}$, the resonant current i_{res} and the inverter voltage v_{AB}. It is evident that both modulations result in about equal inverter voltages and resonant currents (parameters (a,b): $\text{Config}_{2.1e}$, (c,d): $\text{Config}_{2.1f}$).

B3 Exemplary comparison based on a laboratory prototype

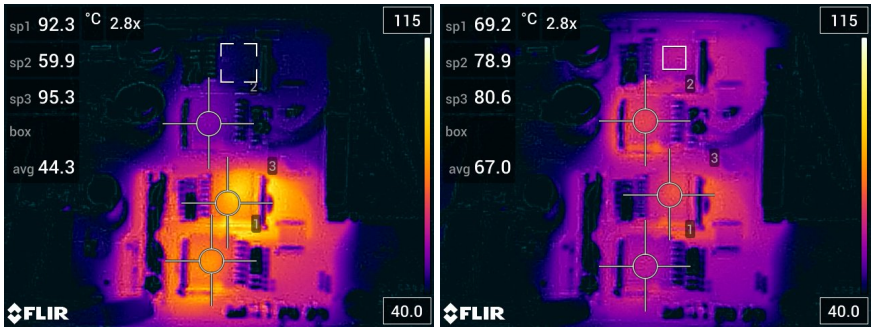
The HBM and FD-HBM were both employed on the LLC converter, which is displayed in Figure 3.23b. The prototype utilizes SiC MOSFETs of type SCT3120AW7 (Rohm, 650 V, 120 mΩ @ 25 °C, [ROH20]). Measurement results are depicted for the operating point $V_{in} = 350\,V$, $V_{out} = 11\,V$ and $I_{out} = 130\,A$ and a gate resistance of 2.2 Ω in Figure 2.21 (a,b) and Figure 2.22 (a,b). The resonant current i_{res}, resonant-capacitor voltage v_{res}, and gate voltages v_{GS} of the low-side switches S_3 and S_4 are depicted in Figure 2.21. It is evident that both modulation schemes result in equal resonant voltages and resonant currents. A thermal analysis of both operating modes is depicted in Figure 2.22(a,b). From top to bottom the switches are: S_1, S_3, S_2, S_4. By employing the FD-HBM, the maximum MOSFET temperature is reduced by about 20 K. The experiments were performed at thermal steady state at the same operating conditions. The measured efficiency is 93.15 % for half-bridge modulation and 93.27 % for the FD-HBM. The higher efficiency in FD-HBM is caused by the lower average junction temperatures of the switches. A modeled loss distribution of the MOSFETs is depicted in Figure 2.22c. The conduction losses have been modeled using datasheet parameters of the temperature-dependent on-state resistance $R_{ds,on}(\vartheta_j)$ while the switching losses have been modeled using double-pulse measurements.



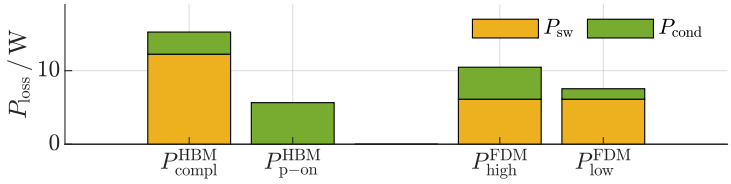
(a) HBM (b) FD-HBM



(c) Modeled loss distribution for an operating point with dominant conduction losses



(d) HBM (e) FD-HBM



(f) Modeled loss distribution for an operating point with dominant switching losses

FIGURE 2.22: LLC half-bridge mode with HBM (d,c) and FD-HBM (b,e) for dominant conduction losses (a,b) and dominant switching losses (d,e). (a) depicts the modulation of Figure 2.18b while (b) depicts the modulation of Figure 2.19a. From top to bottom the switches (shown by the markers) are: S_1, S_3, S_2, S_4. The FD-HBM reduces the maximum temperature by about 20 K for the operation with dominant conduction losses. For dominant switching losses, the junction temperature is reduced by about 15 K (parameters (a,b): $\text{Config}_{2.1e}$, (d,e): $\text{Config}_{2.1f}$).

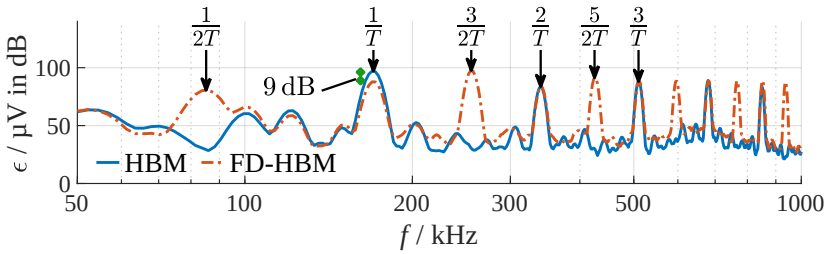


FIGURE 2.23: Electromagnetic emission spectrum of the conventional HBM and the FD-HBM applied to an LLC operated at 170 kHz. The FD-HBM reduces the EMI emission at the operating frequency by about 9 dB. However, additional emissions can be recognized at odd multiples of half the operating frequency. The EMI filter must, thus, be designed accordingly (parameters: $\text{Config}_{2.1g}$).

An operating point with dominant switching losses in half-bridge mode is depicted in Figure 2.21 (c,d) and Figure 2.22(d,e). The inverter is operated at a switching frequency of about 168 kHz and a gate resistance of 24 Ω[1]. The measured efficiency is 83.41 % for HBM and 83.58 % for FD-HBM. The input voltage is $V_{\text{in}} = 420\,\text{V}$, the output voltage is $V_{\text{out}} = 5\,\text{V}$ at an output current of $I_{\text{out}} = 80\,\text{A}$. The modeled loss distribution of the MOSFETs is depicted in Figure 2.22f. The thermal measurement results of Figure 2.22(d,e) show that for this setup, the maximum MOSFET temperature is reduced by about 15 K.

The aforementioned results prove the analysis of Figure 2.20 and show that the FD-HBM is the superior choice over the conventional half-bridge modulation. For both cases of dominant conduction losses and dominant switching losses, the maximum MOSFET temperature is reduced significantly.

The FD-HBM also influences the common-mode behavior of the circuit. As stated in Section 2.1.1A6, the common-mode emission largely depends on the sum of the voltages v_{A} and v_{B} ($v_{\text{com}} = v_{\text{A}} + v_{\text{B}}$), especially if a symmetrical circuit is employed [ZMA17; XRY18; Reh+21e]. Therefore, the FD-HBM has a direct influence on the common-mode behavior of the circuit. The sum of the voltages of the FD-HBM is depicted in Figure 2.19. For the conventional HBM, this voltage is $v_{\text{com}} = |v_{\text{AB}}|$. While for the conventional HBM, the fundamental frequency is equal to the operating frequency, for the FD-HBM, the fundamental frequency is reduced by a factor of two. Therefore, additional emissions ϵ can be measured for frequencies equal to an odd integer of half the operating frequency. At even integers of half the operating frequency, the phase difference of v_{A} and v_{B} is 180° such that a destructive interference results, which is similar to the alternating-asymmetrical phase-shift modulation [Reh+21e]. Measurements of the EMI behavior for the conventional HBM and the FD-HBM are depicted in Figure 2.23, which shows this behavior. For the operating frequency (170 kHz), the EMI emission is reduced by 9 dB. However, the additional emissions can clearly be recognized for odd multiples of half the operating frequency and must be taken into account.

[1] this value is chosen deliberately large to achieve dominant switching losses.

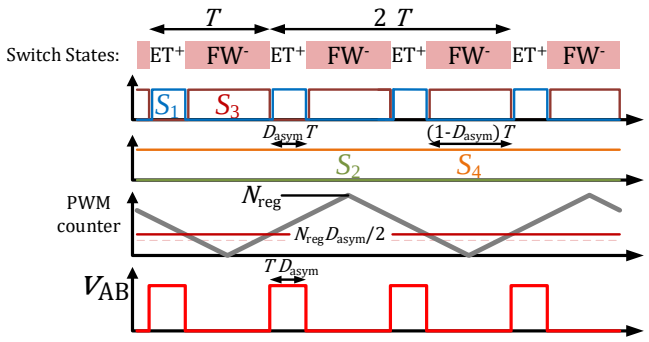
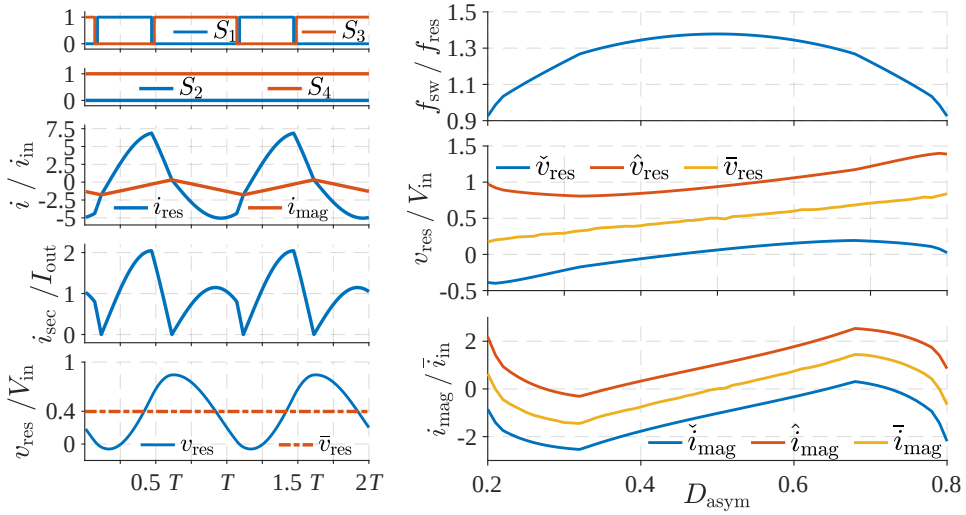


FIGURE 2.24: Asymmetrical half-bridge modulation. The modulation consists of intervals of the lengths $D_{\text{asym}}T$ and $(1 - D_{\text{asym}})T$



(a) Current and voltage shapes ($D_{\text{asym}} = 0.4$)

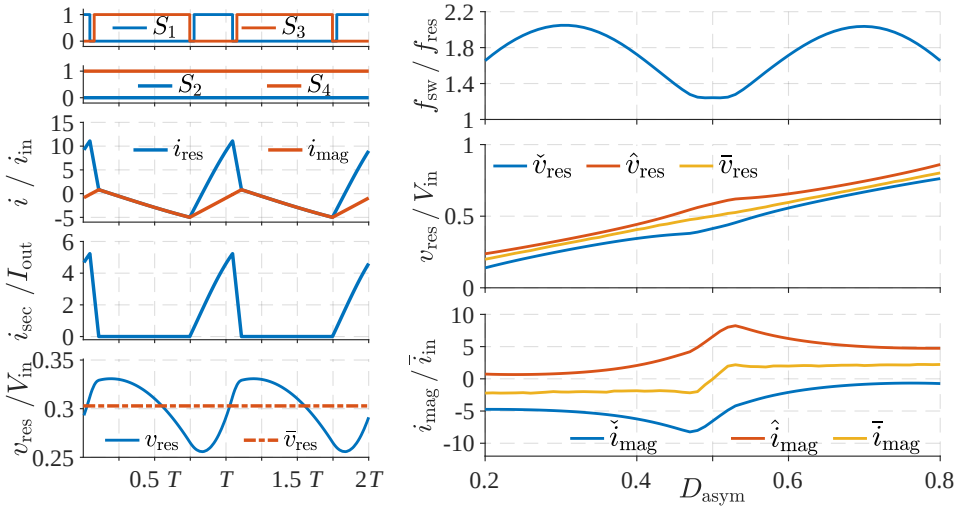
(b) Transfer characteristics

FIGURE 2.25: Asymmetrical pulse-width modulation (aPWM). (a) typical current shapes; (b) resonant capacitor voltage and magnetizing current dependency on the duty cycle (parameters: Config$_{2.1h}$).

B4 Asymmetrical pulse-width modulation

Conventionally, the voltage-transfer ratio of half-bridge LLC resonant converters is adjusted through the switching frequency. However, it is also possible to adjust the voltage-transfer ratio or regulate the output current by operating the converter with an asymmetrical duty cycle (cf. Figure 2.26). This operation is conventionally referred to as aPWM. While commonly employed on a half-bridge LLC converter (Figure 2.2b), it can also be employed on a full-bridge LLC converter (Figure 2.2a). The inverter voltage can be achieved by turning one switch permanently on while the two MOSFETs of the other respective bridge leg are operated with asymmetrical duty cycles (cf. 2.25a). This operation will be referred to as asymmetrical half-bridge modulation (aHBM). Typical current and voltage shapes of this operation are shown in Figure 2.25a.

The operation has been introduced for the LLC converter in [IM93]. The half-bridge configuration with an aPWM leads to an imbalance in the rectifier currents, which generally is unsatisfactory as it leads to higher losses. However, to limit the



(a) Current and voltage shapes (boost operation, $D_{asym} = 0.35$)

(b) Transfer characteristics

FIGURE 2.26: aPWM with boost characteristics. (a) typical current shapes; (b) resonant capacitor voltage and magnetizing current dependency on the duty cycle at constant output voltage (parameters: Config$_{2.1i}$).

switching frequency, the mode is still frequently applied to reduce the conversion losses for low loads and small voltage-transfer ratios in [IM93; SZL17; Rue+20]. However, as it is also possible to increase the output current with an asymmetrical duty cycle, this modulation scheme is also applied as a hold-up modulation for data-center applications in [KPM11]. This boost characteristic can be problematic when the modulation scheme is intended for buck purposes only. An analysis on this behavior has been published in [Rue+20] . The behavior is depicted in Figure 2.26.

In half-bridge configuration the resonant capacitor voltage v_{res} has a voltage offset of $\bar{v}_{res} = \pm\frac{V_{in}}{2}$[1] when operated with a symmetrical duty cycle. However, if an asymmetrical duty cycle is applied, the offset changes. If the low-side switch is operated with a larger duty cycle ($D_{asym} > 0.5$), the offset reduces ($\bar{v}_{res} < \frac{V_{in}}{2}$) and increases for $D_{asym} < 0.5$. Similarly, this mode also leads to an average magnetizing current i_{mag} unequal to zero, which has to be accounted for in the design process. This behavior is visualized in Figure 2.25b and Figure 2.26b. To avoid over voltages in the resonant capacitor, in the following, it is assumed that the low-side switch is always operated with a duty cycle larger than 0.5 such the voltage pulse width reduces ($D_{asym} < 0.5$, cf. Figure 2.24).

[1] the sign of the voltage depends on the type of the employed modulation (see Section 2.1.1B1).

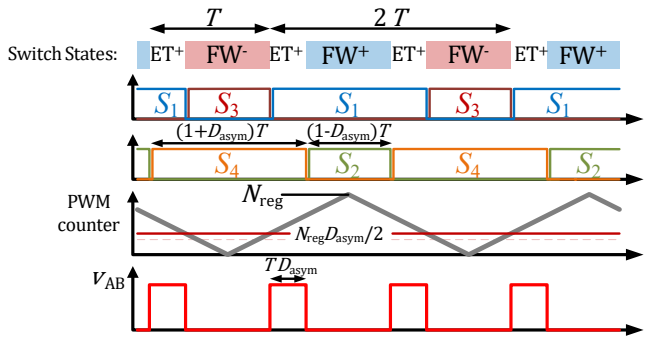


FIGURE 2.27: Asymmetrical frequency-doubler modulation (aFDM). The modulation consists of intervals of the lengths $(1 + D_{\text{asym}})T$ and $(1 - D_{\text{asym}})T$, which are phase shifted for one half bridge by T. The pulses of the switches thus repeat their pattern every $2T$.

B5 Asymmetrical frequency-doubler modulation

The aHBM also suffers from the unbalanced loss distribution similar to the conventional HBM. It is, however, equally possible to generate the asymmetrical inverter voltage with the concept of the FD-HBM by extending the freewheeling intervals. This concept of the proposed aFDM is depicted in Figure 2.27. The solid lines at the counter shows the compare value to generate the asymmetrical inverter voltage while the dashed line shows the reference value that is used for the conventional FD-HBM. By employing this aFDM, the peak inverter switch losses can be reduced significantly – for dominant conduction losses and dominant switching losses. For the conventional aHBM three types of switches can be distinguished:

1. the switch that is turned on for $D_{\text{asym}}T$ with the switch current $I_{\text{sw},1}$ and the turn-off current $i_{\text{off},1}$,
2. the switch that is turned on for $(1 - D_{\text{asym}})T$ with the switch current $I_{\text{sw},2}$ and the turn-off current $i_{\text{off},2}$,
3. the permanently turned-on switch being stressed with the resonant current $I_{\text{res}} = \sqrt{I_{\text{sw},1}^2 + I_{\text{sw},2}^2}$.

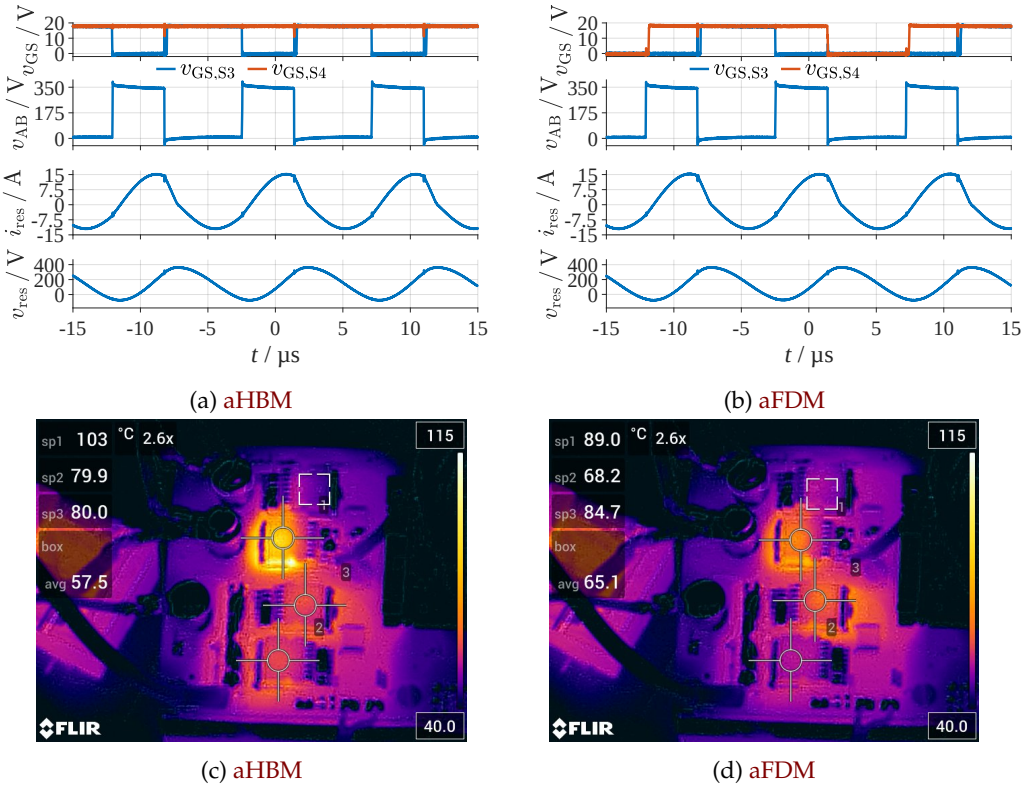
Usually, the turn-off current of the switch being turned on for $D_{\text{asym}}T$ is larger than the one of the other pulsing switch ($i_{\text{off},1} > i_{\text{off},2}$) such that the switching losses of that switch are the highest. The losses of the two pulsing switches are calculated as

$$P_{\text{compl}}^{\text{aHBM}} = I_{\text{sw},k}^2 R_{\text{ds,on}}(\vartheta_{\text{j}}) + f_{\text{sw}} E_{\text{off}}(i_{\text{off},k}) \tag{2.24}$$

where $k \in \{1, 2\}$. Similar to the analysis of the HBM, the losses of the switch that is permanently turned on can be calculated with (2.21).

If the aFDM is employed, only two types of switches are distinguishable:

1. the switch that is turned on for $(1 + D_{\text{asym}})T$ being stressed with the RMS current $I_{\text{high}} = \sqrt{\frac{2I_{\text{sw},1}^2 + I_{\text{sw},2}^2}{2}}$ and the turn-off current $i_{\text{off},1}$,
2. the switch that is turned on for $(1 - D_{\text{asym}})T$ being stressed with the RMS current $I_{\text{low}} = \sqrt{\frac{I_{\text{sw},2}^2}{2}}$ and the turn-off current $i_{\text{off},2}$.



(a) aHBM (b) aFDM

(c) aHBM (d) aFDM

FIGURE 2.28: Experimental measurement results of the aHBM (a,c) and aFDM (b,d) for a case of dominant conduction losses at the configuration $\text{Config}_{2.1j}$ at a gate resistance of $R_g = 2\,\Omega$ at the configuration $\text{Config}_{2.1k}$. The maximum MOSFET temperature is reduced by 14 K.

Referring to the analysis of (2.24), the losses of the switch that is turned on for $(1 + D_{asym})T$ are calculated as

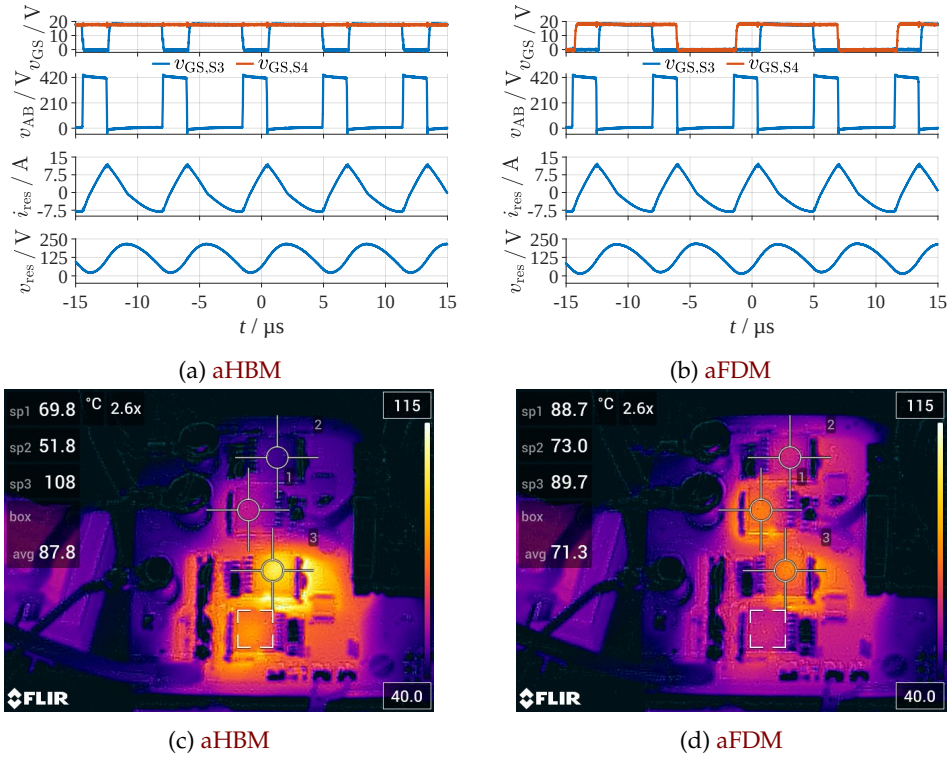
$$P_{high}^{aFDM} = (2I_{sw,1}^2 + I_{sw,2}^2)R_{ds,on}(\vartheta_j) + \frac{f_{sw}}{2}E_{off}(i_{off,1}), \tag{2.25}$$

whereas the losses of the other switch type are calculated as

$$P_{low}^{aFDM} = I_{sw,2}^2 R_{ds,on}(\vartheta_j) + \frac{f_{sw}}{2}E_{off}(i_{off,2}). \tag{2.26}$$

Due to the large number of variables ($i_{off,1}$, $i_{off,2}$, $I_{sw,1}$, $I_{sw,2}$), it is not possible to visualize the loss distribution as it is done in Figure 2.20. However, it is evident that this modulation may result in a better loss distribution than the conventional aHBM. The maximum RMS current is reduced from $\sqrt{\frac{2I_{sw,1}^2+2I_{sw,2}^2}{2}}$ to $\sqrt{\frac{2I_{sw,1}^2+I_{sw,2}^2}{2}}$ and the maximum switching losses are reduced from $f_{sw}E_{off}(i_{off,1})$ to $\frac{f_{sw}}{2}E_{off}(i_{off,1})$.

Experimental measurements are provided for dominant conduction losses at a gate resistance of $R_g = 2\,\Omega$ and the configuration $\text{Config}_{2.1j}$ in Figure 2.28 (the hottest switch is the one that is permanently turned on). For dominant switching losses at a gate resistance of $R_g = 19.5\,\Omega$ and the configuration $\text{Config}_{2.1k}$. Measurement results are provided in Figure 2.29 (the hottest switch is the one being turned on for the duration of $D_{asym}T$ and turned off at $i_{off,1}$). For both experiments the maximum switch temperature is significantly reduced. For dominant conduction losses the



(a) aHBM (b) aFDM

(c) aHBM (d) aFDM

FIGURE 2.29: Experimental measurement results of the aHBM (a,c) and aFDM (b,d) for a case of dominant switching losses at a gate resistance of $R_g = 19.5\,\Omega$ at the configuration $\text{Config}_{2.1k}$. The maximum MOSFET temperature is reduced by 18 K.

maximum switch temperature is reduced by 14 K from $\vartheta = 103\,°\text{C}$ to $\vartheta = 89\,°\text{C}$ whereas for dominant switching losses the maximum switch temperature is reduced by 18.3 K from $\vartheta = 108\,°\text{C}$ to $\vartheta = 89.7\,°\text{C}$. For both cases the resonant voltage and current look completely similar.

From the measurement results of Figure 2.28 and Figure 2.29, it is evident that through the exploitation of the aFDM, the maximum switch losses can be significantly reduced resulting in a more balanced inverter temperature. Due to the reduced MOSFET temperature, the efficiency can be marginally increased. For the case of dominant conduction losses, for instance, it is increased from $\eta = 90.83\,\%$ (aHBM) to $\eta = 90.88\,\%$ (aFDM). Due to the more balanced junction temperature and the increased efficiency, the aFDM should be the preferred mode of operation favored over the aHBM.

2.1.2 On-the-fly topology morphing

To switch from full-bridge modulation to half-bridge mode, the resonant capacitor voltage needs to be changed from $\bar{v}_{\text{res}} = 0$ to $\bar{v}_{\text{res}} = V_{\text{in}}/2$ (or to $\bar{v}_{\text{res}} = -V_{\text{in}}/2$ if the other half-bridge mode is employed). The sudden change from half-bridge modulation to full-bridge modulation was attempted in [Lia+10] for a converter for photovoltaic applications. Considering the necessary change of the switching frequency and resonant capacitor voltage, this resulted in a large overshoot/undershoot of the photovoltaic voltage and current.

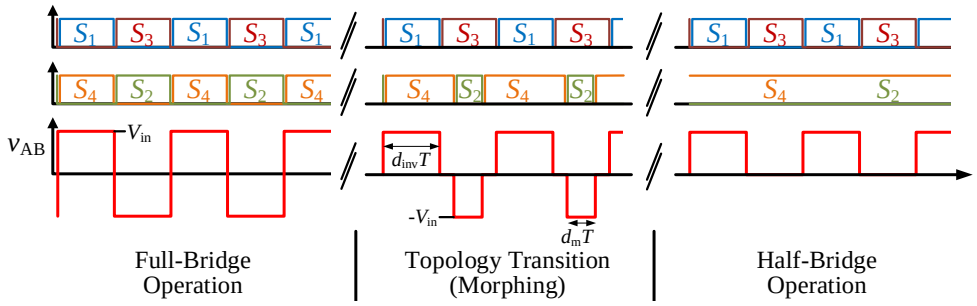
While the duty cycle of all switches changes by only 25 % when transitioning between the full-bridge modulation and the FD-HBM, the average resonant capacitor voltage needs to be adjusted similarly to the change between full-bridge modulation and half-bridge modulation from $\bar{v}_{\text{res}} = 0$ to $\bar{v}_{\text{res}} = V_{\text{in}}/2$. A sudden transition from full-bridge to FD-HBM and back was tested in [Wei+20c] leading to an output voltage overshoot of 44 % when transitioning from FD-HBM to full-bridge modulation and to an undershoot of 36 % in the reverse direction. A feed-forward control adjusting the switching frequency was able to substantially reduce this over-/undershoot [Wei+20c; WM21]. However, since the switching frequency largely depends on the components of the resonant tank, component deviations considerably affect the system behavior [Bin+14; Keu23] such that this type of control may be problematic if the exact component values are not matched. The work of [Keu23] showed that a feed-forward control similar to the control method of [Wei+20c; WM21] could not be successfully employed as component deviations resulted in extensive switching frequency deviations. The work of [Wei+20c; WM21] did not analyze the influence of component deviations and the depicted measurement results appear to show steady-state deviations. Additionally, only a very large time base is depicted such that the instantaneous influence over several switching periods of the transition cannot be evaluated. Furthermore, the switching frequency largely depends on the output load, which requires that the load must be known at the instance of the transition. However, the influence of load variations was also not analyzed in [Wei+20c; WM21].

To change the operating mode from full-bridge to half-bridge operation and reverse, a slower continuous method labeled *on-the-fly topology morphing* was proposed in [JI15b; JI15a; JI16]. The duty cycle of one switch is hereby continuously increased from 50 % to 100 % while the other duty cycle of the same respective half-bridge is switched complementary. The modulation, however, resulted in a substantial increase of the magnetizing current by over 70 %, which must be considered in the design of the transformer. To the authors' best knowledge no on-the-fly morphing modulation to transition from full-bridge modulation to FD-HBM and reverse has yet been described.

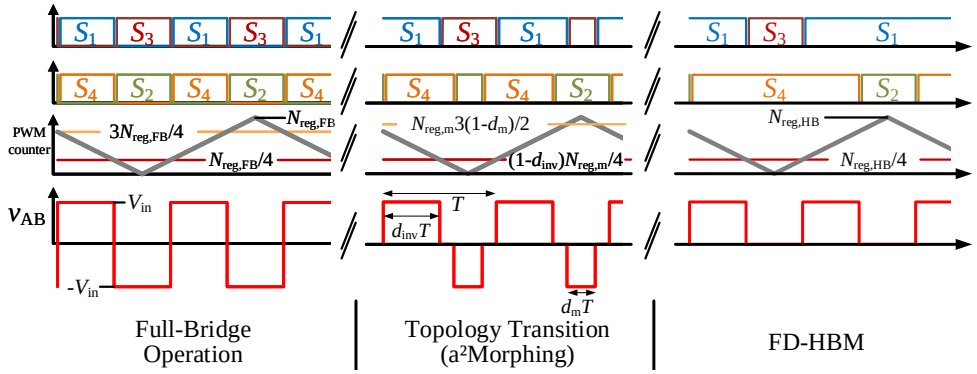
A Morphing between full-bridge operation and FD-HBM and reverse

this section has been previously published in parts in [Reh+21e]
and the presented method has been applied for patent in [Reh+21c].

To change the operating mode from full-bridge to half-bridge mode and back, an on-the-fly topology morphing method was proposed in [JI16]. For this transition, the duty cycle of one low-side switch of a half-bridge is slowly increased from 50 % to 100 % whereas the high-side switch of the other respective half bridge is pulsed complementary. This results in a reduction of the negative inverter voltage pulse



(a) Full-bridge to HBM transition



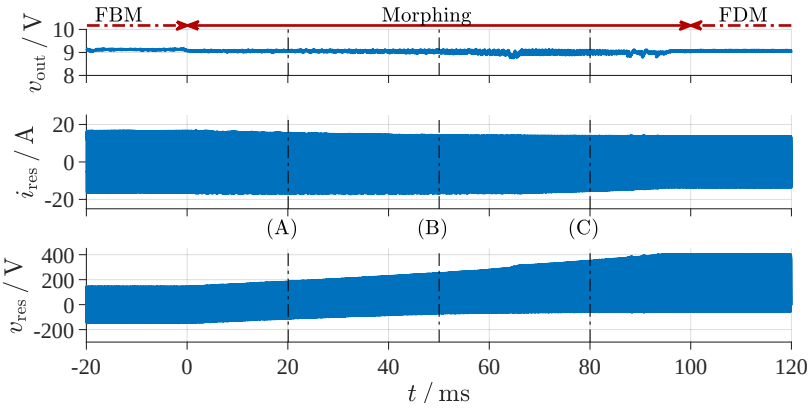
(b) Full-bridge to FD-HBM transition

FIGURE 2.30: On-the-fly morphing from full-bridge modulation to half-bridge mode. (a) transition to the conventional HBM, (b) transition to the FD-HBM. For (b), one compare value is shifted to achieve the morphing modulation.

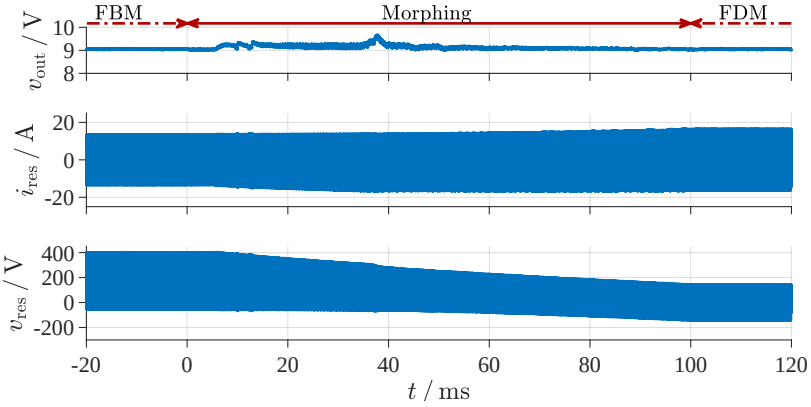
length $d_m T$. This is visualized in Figure 2.30a. For a transition from half-bridge to full-bridge operation, this method is reversed. For this section, it will be assumed that the negative inverter voltage pulse is centered between two positive-inverter voltage pulses. However, other pulse positions are also possible [JI16].

By employing the FD-HBM, it is equally possible to control the morphing from full-bridge to FD-HBM modulation and back (cf. Figure 2.30b). The operation is hereby achieved also with an up-down counter. During the morphing process one of the reference values is slowly adjusted to achieve the morphing modulation whereas the frequency is adjusted to achieve a steady output voltage/current. Since the modulation does not alter the shape of the inverter voltage, the traits of the morphing modulation remain the same: the magnetizing current still needs to be addressed in the design process and may increase during the morphing modulation (see Section 2.1.2C). Furthermore, similar to the conventional morphing method, this modulation also results in a hard turn-on of the MOSFETs close to the FD-HBM.

The alternating asymmetrical morphing is depicted in Figure 2.30b. It has been employed in a prototype and is displayed for the operating point $V_{in} = 350\,V$, $V_{out} = 9\,V$ and $I_{out} = 130\,A$ in Figure 2.31. The frequency-doubler half-bridge modulation in this and all following figures is abbreviated as *FDM*. The gain of this operating point has been chosen as it results in a slightly over-resonant operation in half-bridge mode. For the following analysis of the morphing, the synchronous rectifier has been disabled such that the forward voltage of the rectifier MOSFETs increases the necessary gain to almost resonant operation in half-bridge mode. This is

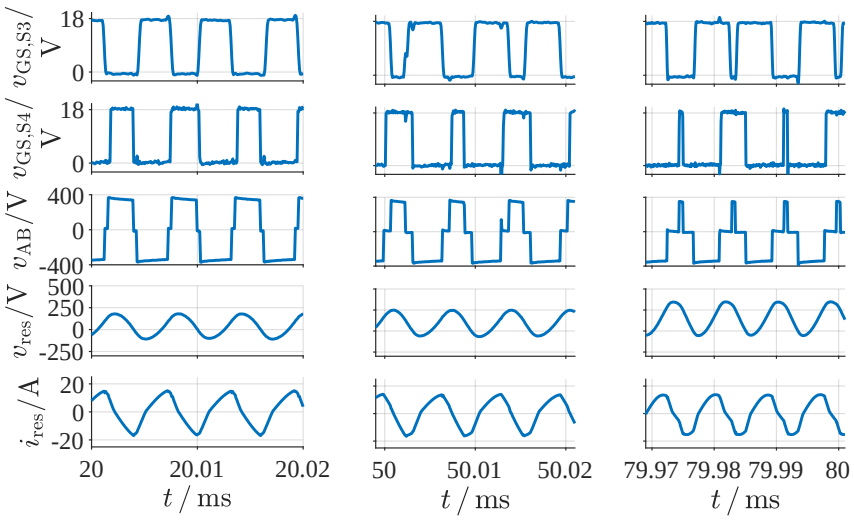


(a) FBM to FD-HBM transition



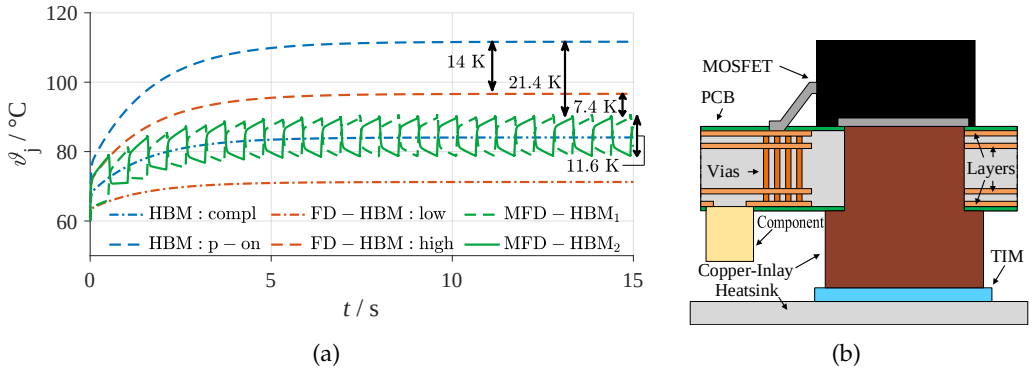
(b) FD-HBM to FBM transition

FIGURE 2.31: Experimental measurement results of the alternating asymmetrical (a^2) morphing transition. (a) transition from FBM to FD-HBM, the intersections (A)-(C) show the intervals that are depicted in Figure 2.32 (a)-(c); (b) transition from FD-HBM to FBM (parameters: $\text{Config}_{2.1l}$).



(a) (b) (c)

FIGURE 2.32: Experimental measurement results for different time instances in the transition depicted in Figure 2.31b of the FD-HBM to full-bridge transition. Visualization of the gate voltages v_{S3} and v_{S4}, the inverter voltage v_{AB} and the resonant voltage v_{res} and current i_{res}.



(a) (b)

FIGURE 2.33: (a) Simulated junction temperatures for the three different modes of operation: HBM, FD-HBM and alternating morphing (MFD-HBM). While the FD-HBM results in a reduction of the junction temperature by about 14 K, the alternating morphing between FD-HBM1 and FD-HBM2 reduces the maximum junction temperature even further by about 7.4 K. However, this modulation leads to a continuously jumping junction temperature by about 11.6 K. (b) Copper inlay used to improve the heat transfer between the MOSFET and the heat sink. The copper inlay acts as a large thermal capacitance that can be utilized to reduce the junction temperature by morphing from one FD-HBM to the other (parameters: Config$_{2.1m}$).

necessary as the following analysis also examines the operation for a large magnetizing inductance L_m (a small inductance ratio λ) where the under-resonant operation is limited. During the transition the output voltage (v_out) could be well controlled. Different time intervals of the transition process in Figure 2.31a are depicted in Figure 2.32.

B Alternating morphing for reduced junction temperatures

The FD-HBM still results in a largely different junction temperature for the MOSFETs stressed with $P_{\text{high}}^{\text{FD-HBM}}$ and the MOSFETs stressed with $P_{\text{low}}^{\text{FD-HBM}}$. While it is possible to change the operation from FD-HBM1 ($v_{\text{AB}} \in \{0, V_{\text{in}}\}$) depicted in Figure 2.19a to FD-HBM2 ($v_{\text{AB}} \in \{-V_{\text{in}}, 0\}$) (cf. Figure 2.19b) and reverse, the average resonant capacitor voltage needs to be changed from V_{in} / 2 to $-V_{\text{in}}$ / 2. This requires a morphing transition similar to the one depicted in Figure 2.30b. But, since this transition results in additional losses from partial hard turn-on, continuous morphing from one configuration to the other should not be performed. Therefore, it is beneficial to remain in either configuration for several hundreds of milliseconds. The thermal time constants of the semiconductors, however, are much smaller. If a copper inlay is employed (as depicted in Figure 2.33b) to improve the heat transfer between the semiconductor and the heat sink, an additional large thermal capacitance is introduced. This inlay can be utilized to force the inlay temperature to a steady value by alternating morphing from one mode to the other. Due to the comparably large thermal capacitance of the copper, the inlay temperature does not significantly change while remaining in either FD-HBM mode.

Figure 2.33a shows a simulation of the different MOSFET temperatures based on simulated currents for the HBM, FD-HBM and the alternating morphing mode (M-FD-HBM). Simulation results are depicted in Figure 2.33a. Turn-on and turn-off losses have been calculated with the loss characteristics provided in the datasheet [ROH20]; the conduction losses were calculated with the temperature-dependent on-state resistance. The temperatures were simulated with the provided equivalent thermal circuit from junction to case provided in the datasheet [ROH20], the calculated thermal capacitance for the thermal inlay (0.73 Ws/K) and the assumed thermal resistance of the thermal interface material is 2 K/W. The results show that the utilization of the FD-HBM results in a reduction of the junction temperature by about 14 K. The alternating morphing reduces the maximum junction temperature even further by about 7.4 K.

This benefit largely depends on the thermal connection of the employed switches. The larger the thermal resistance of the thermal-interface material (TIM), the larger is the benefit. However, due to the small thermal time constants of the semiconductor, the MOSFETs are continuously stressed with a temperature ripple of about 11.6 K, which may reduce the lifetime of the semiconductors. This temperature ripple largely depends on the thermal resistance of the junction-to-case connection. For the depicted analysis, the three equivalent thermal resistors of the junction-to-case connection sum up to a total thermal resistance of 1.1 K/W. The smaller this thermal resistance, the smaller is the resulting temperature ripple.

C Analysis of the magnetizing current offset

One of the problems of the on-the-fly morphing transition is that the magnetizing current increases over the transition time. The increase of the magnetizing current was described in [JI15a; JI16] where it was stated that the maximum magnetizing current increases during the morphing by up to 70 % compared to half-bridge modulation. The maximum (positive) magnetizing current morphing value compared to the maximum magnetizing current in half-bridge modulation will, in the following, be labeled *magnetizing current morphing ratio* $\hat{p}_{\mathrm{mag,m}}$ and is defined as

$$\hat{p}_{\mathrm{mag,m}} = \frac{\hat{\hat{i}}_{\mathrm{mag,m}}}{\hat{\hat{i}}_{\mathrm{mag,HB}}}. \tag{2.27}$$

Additionally, the minimum magnetizing current morphing value compared to the minimum magnetizing current in half-bridge modulation will be labeled as

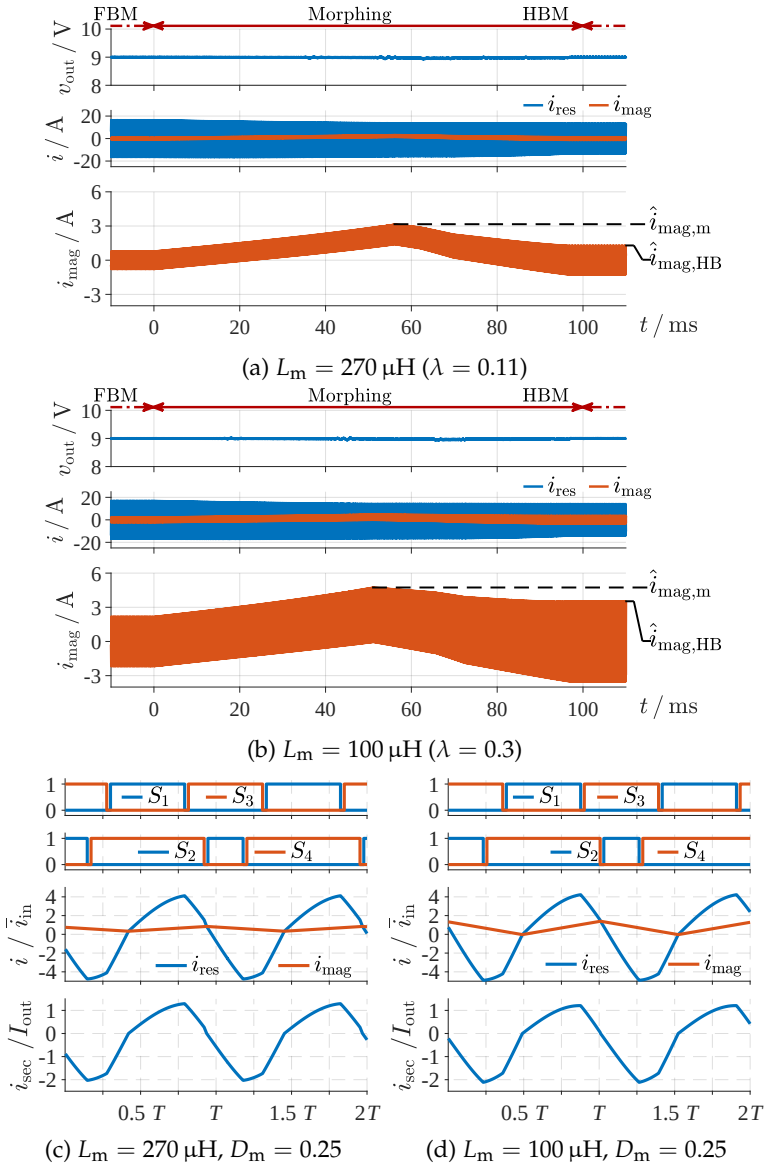
$$\check{p}_{\mathrm{mag,m}} = \frac{\check{\check{i}}_{\mathrm{mag,m}}}{\check{\check{i}}_{\mathrm{mag,HB}}}. \tag{2.28}$$

In [JI15a; JI16], it was identified that the longer the morphing duration t_{morph} is chosen, the easier the output control can be designed. Considering the case of slowly changing input and output voltages (i.e., in an electrical vehicle charger or on-board DC-DC converter), an operating mode change is required to optimize the conversion efficiency or to cover future voltage transfer ratios where the previous operating mode cannot be employed. Thus, at the voltage-transfer ratio where the operating mode is switched must obviously be reachable by either operating mode such that the morphing time duration can be chosen long. For that purpose, the following analysis will focus on long morphing durations (in this case of 100 ms) where the introduced dynamics are small. Figure 2.34a shows simulation results for a configuration with $\lambda = \frac{L_{\mathrm{r}}}{L_{\mathrm{m}}} = 0.11$ ($L_{\mathrm{r}} = 30\,\mu\mathrm{H}$, $L_{\mathrm{m}} = 270\,\mu\mathrm{H}$, $C_{\mathrm{r}} = 90\,\mathrm{nF}$, $n = 14.7$, $V_{\mathrm{in}} = 350\,\mathrm{V}$, $V_{\mathrm{out}} = 9\,\mathrm{V}$, $I_{\mathrm{out}} = 130\,\mathrm{A}$). The morphing increase can be well identified resulting in a maximum morphing magnetizing current value at $t = 55\,\mathrm{ms}$ (corresponding to $d_{\mathrm{m}} = 0.275$, cf. Figure 2.30a).

Considering the on-the-fly morphing transition from full-bridge to half-bridge mode, the resonant capacitor is charged from an average capacitor voltage of zero to an average capacitor voltage of half the input voltage. While it may at first glance appear plausible that this charging process is the root cause of the magnetizing current offset, at closer inspection, it becomes easily apparent that this is not the case. To charge the resonant capacitor, the circuit needs to deliver the charge $\Delta Q_{\mathrm{res}} = C_{\mathrm{res}} \frac{V_{\mathrm{in}}}{2}$. Assuming a constant overlying charging current over the morphing time t_{morph}, the resonant current offset $\bar{i}_{\mathrm{res}}$ is

$$\bar{i}_{\mathrm{res}} = \frac{\Delta Q_{\mathrm{res}}}{t_{\mathrm{morph}}} = \frac{C_{\mathrm{res}} V_{\mathrm{in}}}{2 t_{\mathrm{morph}}}. \tag{2.29}$$

In steady state, the average resonant current i_{res} must be the average charging current $\bar{i}_{\mathrm{res}}$ considering a linearly increasing resonant capacitor voltage. The relationship between the average charging current $\bar{i}_{\mathrm{res}}$, the average magnetizing current $\bar{i}_{\mathrm{mag}}$ and the transformed secondary currents i'_{sec} can be expressed as



(a) $L_m = 270\,\mu H$ ($\lambda = 0.11$)

(b) $L_m = 100\,\mu H$ ($\lambda = 0.3$)

(c) $L_m = 270\,\mu H$, $D_m = 0.25$

(d) $L_m = 100\,\mu H$, $D_m = 0.25$

FIGURE 2.34: Simulation of a conventional morph transition for small (a) and large λ-values (b). Morphing transition (a,b), steady-state simulation for $D_{morph} = 0.25$ (c,d). While small λ-values (a large magnetizing inductance L_m) result in a large magnetizing current morphing ratio $\hat{i}_{mag,m}/\hat{i}_{mag,HB}$ (cf. (a)), for larger λ-values, the ratio may be much smaller (cf. (b)). The imbalance of the secondary current i_{sec} is hereby similar (c,d) (parameters: Config$_{2.1n}$).

$$\begin{aligned} \frac{1}{T}\int_T i_{res}\mathrm{d}t &= \frac{1}{T}\int_T (i_{mag} + i'_{sec})\mathrm{d}t \\ &= \frac{1}{T}\int_T i'_{sec}\mathrm{d}t + \bar{i}_{mag} \overset{!}{=} \bar{i}_{res}. \end{aligned} \tag{2.30}$$

Considering a transition time of $t_{morph} = 100\,ms$, an input voltage of $V_{in} = 420\,V$ and a resonant capacitance of $C_{res} = 90\,nF$, the average DC current amounts to $\bar{i}_{res} = 157.5\,\mu A$, which is negligible compared to the magnetizing current offset (cf.

Figure 2.37a).

During the morphing transition, the secondary currents i_{SR1} and i_{SR2} are unbalanced such that

$$\int_T i_{SR1} \mathrm{d}t \neq \int_T i_{SR2} \mathrm{d}t \tag{2.31}$$

resulting in

$$\bar{i}_{sec} = n\bar{i}'_{sec} = \frac{1}{T}\left(\int_T i_{SR1}\mathrm{d}t - \int_T i_{SR2}\mathrm{d}t\right) \neq 0 \tag{2.32}$$

where n is the transformation ratio of the transformer.

This imbalance of the rectifier currents must be compensated by an average magnetizing current $\bar{i}_{mag}$ such that

$$\begin{aligned} \bar{i}_{mag} &\overset{!}{=} \bar{i}_{res} - \frac{1}{T}\int_T i'_{sec}\mathrm{d}t \\ &= \bar{i}_{res} - \frac{1}{nT}\left(\int_T i_{SR1}\mathrm{d}t - \int_T i_{SR2}\mathrm{d}t\right). \end{aligned} \tag{2.33}$$

As mentioned above, for a long morphing time t_{morph} the average charging current $\bar{i}_{res}$ is negligible such that (2.33) can be simplified to

$$\bar{i}_{mag} = -\frac{1}{nT}\left(\int_T i_{SR1}\mathrm{d}t - \int_T i_{SR2}\mathrm{d}t\right) = -\bar{i}'_{sec}. \tag{2.34}$$

Figure 2.34c shows the resonant, magnetizing and secondary current for the morphing state $D_m = 0.25$ indicating the largely unsymmetrical secondary currents that are the cause of the magnetizing current offset.

It shall be emphasized that the offset in the magnetizing current is dominantly caused by the employed morphing modulation and ***not*** by the dynamic transition itself. If the transition would be stopped at any given time, the magnetizing current offset would, therefore, not settle. Similarly, an increased morphing time would have no effect on the magnetizing current offset.

The magnetizing current directly corresponds with the flux density in the core. For a conventional transformer the time-varying flux density $b(t)$ can be calculated with the time varying magnetizing current $i_{mag}(t)$, the transformer stray inductance L_σ, the magnetizing inductance L_m, the primary turn number N_p and the transformer core cross section A_c[Alb17][1] as

[1] this equation is only valid for a conventional transformer where no stray path is implemented (as was done in [Har+13; ADF20; Li+15; LOA19; SAS08; Keu+19; KSB19]) and where secondary-side stray inductance is negligible. If the secondary stray inductance is non-negligible, this influence must be considered in the calculation of the flux density. The method presented in this section, however, is still valid for such transformers as it suppresses a morphing overlying DC current.

$$b_{\mathrm{mag}}(t) = \frac{(L_\sigma + L_\mathrm{m}) i_{\mathrm{mag}}(t)}{N_\mathrm{p} A_\mathrm{c}}. \tag{2.35}$$

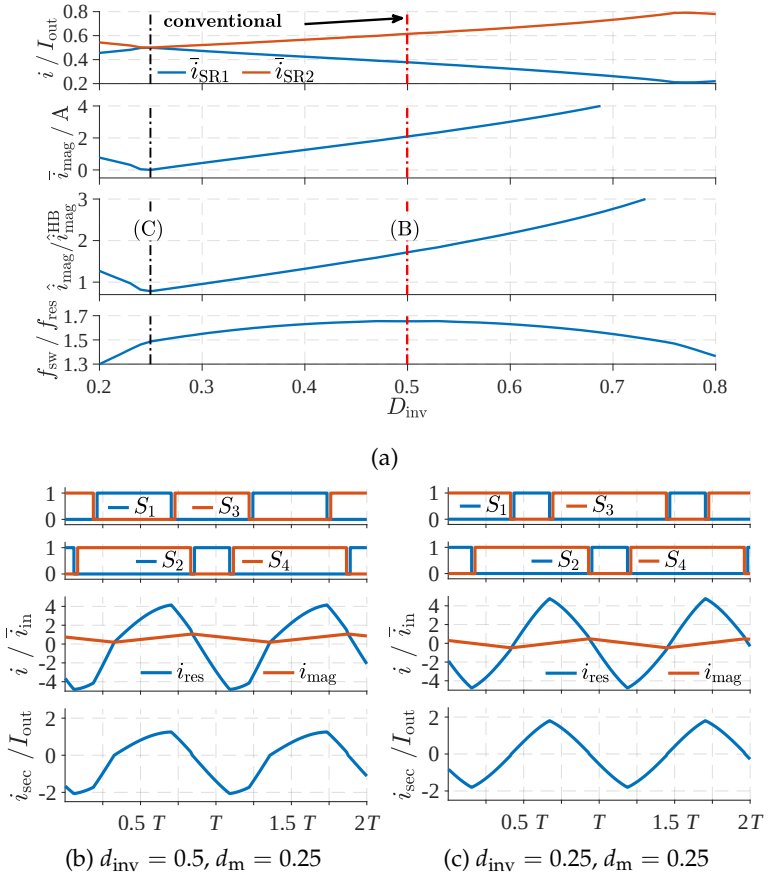
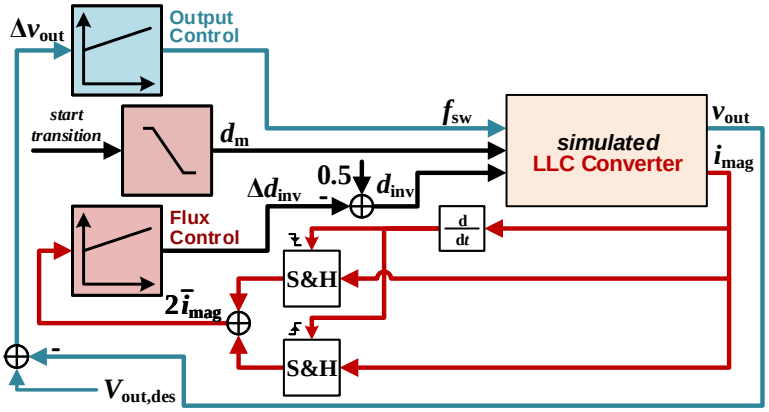


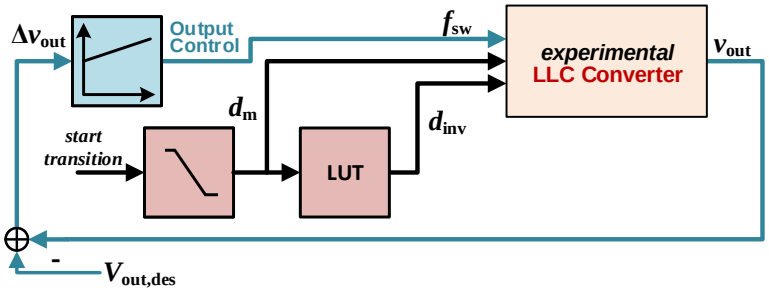
FIGURE 2.35: (a) Stationary dependency of the average secondary synchronous rectifier currents $\bar{i}_{\mathrm{SR1}}$, $\bar{i}_{\mathrm{SR2}}$, the magnetizing current $\bar{i}_{\mathrm{mag}}$ and the normalized switching frequency $f_{\mathrm{sw}}/f_{\mathrm{res}}$ on the positive inverter voltage pulse length D_{inv} for $d_\mathrm{m} = 0.25$. The conventional inverter voltage pulse length is $d_{\mathrm{inv}} = 0.5$ resulting in a substantial difference in the rectifier currents and a magnetizing current offset. By changing d_{inv} to 0.25, the imbalance and offset can be prevented. (b,c) stationary current shapes for the values depicted in (a) (parameters: Config$_{2.1o}$).

A temporary increase in the magnetizing current may, therefore, lead to a saturation of the transformer core. To avoid this, it has been stated that the transformer core must be designed for a larger saturation flux density [JI15a; JI16]. However, when analyzing (2.30) and (2.35) and looking at Figure 2.34a, the magnetizing flux density b_{mag} can be separated into an AC and a DC component. While the AC component of the magnetizing current relates to the design of the magnetizing inductance L_m and the applied voltage, the DC component depends on the secondary current offset $\bar{i}'_{\mathrm{sec}}$ only. Therefore, by choosing a smaller magnetizing inductance L_m, the magnetizing current ripple can be increased and the magnetizing current morphing ratio $\hat{p}_{\mathrm{mag,m}}$ (2.27) and magnetizing flux ratio can be reduced. However, the smaller magnetizing inductance directly influences the inductance ratio $\lambda = \frac{L_\mathrm{r}}{L_\mathrm{m}}$, which is an important design parameter of the resonant tank.

Figure 2.34b shows the morphing transition for the same operating point and



(a) Control structure used to derive the look-up table (LUT)

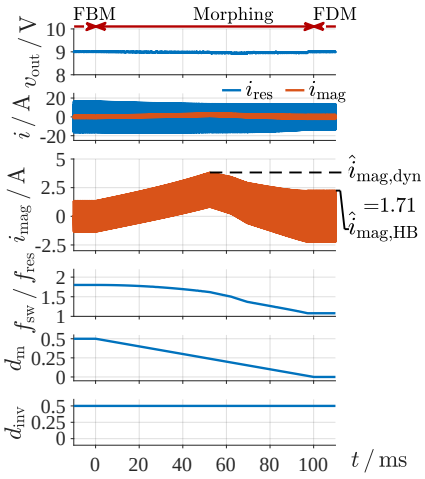


(b) Control structure for the actual experimental application

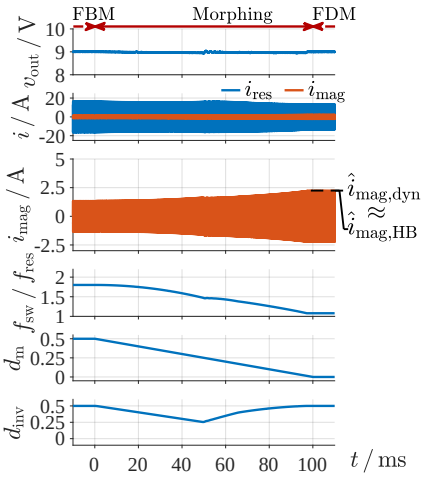
FIGURE 2.36: (a) Control of the simulation to derive the look-up-table for the on-the-fly morphing transition, (b) control of the experimental prototype in the transition from full-bridge modulation to half-bridge mode. The negative inverter voltage-pulse length $d_m T$ is a ramp from 0.5 to 0.

resonant tank parameters as in Figure 2.34a with the exception of a larger inductance ratio $\lambda = 0.3$ instead of $\lambda = 0.11$ ($L_m = 100\,\mu H$ instead of $L_m = 270\,\mu H$). Figure 2.34d shows the steady-state simulation for $d_m = 0.25$. While the imbalance in the secondary currents i_{SR1} and i_{SR2} is very similar (cf. Figure 2.34d), the magnetizing current ripple is larger such that the magnetizing current morphing ratio $\hat{p}_{mag,m}$ is much smaller (35 % for 100 µH, Figure 2.34b vs. 140 % for 270 µH, Figure 2.34a). While the maximum magnetizing current value is larger for the case of $L_m = 100\,\mu H$, $\hat{p}_{mag,m}$ is much more severe for $L_m = 270\,\mu H$. For the effects on the magnetizing flux density b_{mag}, however, only $\hat{p}_{mag,m}$ is relevant since the calculation of b_{mag} (2.35) includes a multiplication with the magnetizing inductance L_m.

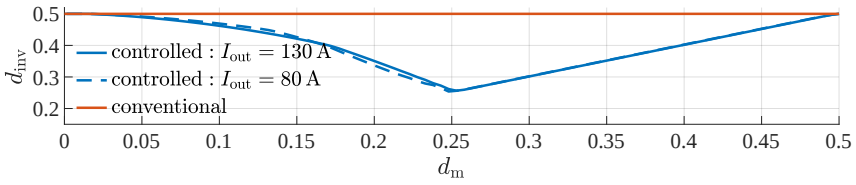
Therefore, the resonant tank can be designed to reduce $\hat{p}_{mag,m}$ and, thus, a saturation of the transformer core can be prevented. While a large inductance ratio λ is typically used for applications with a wide voltage-transfer ratio (where morphed LLC resonant converter excel), the designer is faced with the dilemma that one design freedom parameter must be sacrificed. It must, therefore, be concluded that this is a detrimental factor when using morphed LLC resonant converters. For that purpose Section 2.1.3 presents an improved morphing transition where the morphing offset can be largely reduced for any modulation.



(a) Conventional morphing (L_m = 160 µH) with a fixed positive inverter voltage pulse length of $d_{inv}T = 0.5T$



(b) Proposed morphing (L_m = 160 µH) with an adjusted positive inverter voltage pulse length $d_{inv}T$



(c) Optimal trajectory of the positive inverter voltage pulse length d_{inv} used for the simulation in (b) and derived by the control model in Figure 2.36a.

FIGURE 2.37: Simulation of a conventional morph transition (a) and proposed asymmetrical duty cycle morphing (b). The proposed transition does not results in a significant morphing offset of the magnetizing current i_{mag}; (c) Optimal trajectory to avoid a morphing increase of the magnetizing current (parameters: $\text{Config}_{2.1o}$).

2.1.3 Improved morphing using double-asymmetrical voltage pulses

this section has been previously published in parts in [Reh+22d] *and the presented method has been applied for patent in* [Reh+21c].

When transitioning from full-bridge to half-bridge mode and reverse, the switching period T is modified to control the output. The negative inverter voltage pulse length d_mT (cf. Figure 2.30) is adjusted to achieve the charging of the resonant capacitor and, thus, the transition itself. In the morphing transition described in [JI15a; JI16] it was assumed that the converter operates with a positive inverter voltage pulse length of $d_{inv} = 0.5$ (cf. Figure 2.30), which means that in the half-bridge modulation transition (cf. Figure 2.30a), S_1 and S_3 are operated complementary. However, the modification of this pulse length offers an additional degree of freedom during the transition.

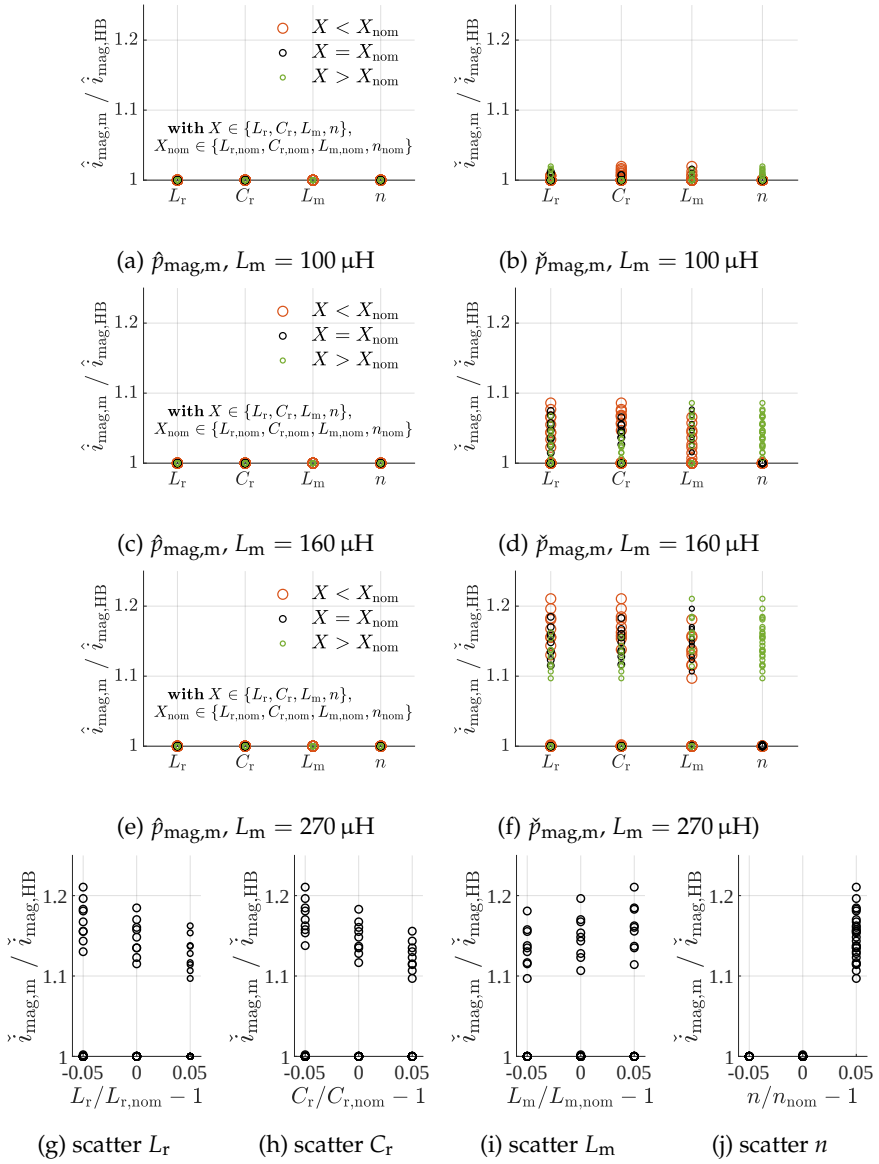
This section demonstrates that it is possible to suppress the magnetizing current offset by dynamically adjusting the positive inverter voltage pulse length $d_{inv}T$. It is hereby irrelevant whether the converter is transiting from full-bridge modulation to half-bridge or frequency-doubler modulation as the currents of the resonant tank (i_{mag} and i_{res}) are only influenced by the inverter voltage pulses and not by the

method how these pulses are generated. This enables a better design of the transformer as the saturation flux density of this component does not need to be designed for such large values. Furthermore, the magnetizing inductance L_m and, therefore, the inductance ratio λ can be freely designed such that this method offers an additional degree of freedom when designing the LLC resonant tank.

A Influence of the positive inverter voltage pulse length

If the inverter is operated such that $d_{\mathrm{inv}} \neq 0.5$, the transfer behavior of the LLC resonant converter is altered, which can potentially be used to suppress the morphing magnetizing current offset. Figure 2.35a shows the stationary transfer behavior (at steady state) for $D_{\mathrm{morph}} = 0.25$ ($L_{\mathrm{r}} = 30\,\mu\mathrm{H}$, $L_{\mathrm{m}} = 160\,\mu\mathrm{H}$, $C_{\mathrm{r}} = 90\,\mathrm{nF}$, $n = 14.7$, $V_{\mathrm{in}} = 350\,\mathrm{V}$, $V_{\mathrm{out}} = 9\,\mathrm{V}$, $I_{\mathrm{out}} = 130\,\mathrm{A}$). For the conventional operation at $D_{\mathrm{inv}} = 0.5$ (red dotted line), the imbalance is quite recognizable. While larger positive inverter voltage pulse lengths increase the imbalance of the rectifier currents and the average magnetizing current, smaller pulse lengths reduce this imbalance and can eventually fully compensate the imbalance at $D_{\mathrm{inv}} \approx 0.25$.

The magnetizing current, however, cannot be measured during the operation. While it may be possible to measure the fringing flux in the proximity of the transformer or the dynamic average secondary current (when employing a full-bridge rectifier), these methods require an additional sensor and increase the converter costs. Therefore, the following section presents an offline control of the magnetizing current to reduce the morphing offset of the transformer flux. The optimal trajectory for the positive inverter voltage pulse length is then implemented as a LUT in the prototype in Section 2.1.3D to verify the concept.



(a) $\hat{p}_{\text{mag,m}}$, $L_\text{m} = 100\,\mu\text{H}$ (b) $\check{p}_{\text{mag,m}}$, $L_\text{m} = 100\,\mu\text{H}$

(c) $\hat{p}_{\text{mag,m}}$, $L_\text{m} = 160\,\mu\text{H}$ (d) $\check{p}_{\text{mag,m}}$, $L_\text{m} = 160\,\mu\text{H}$

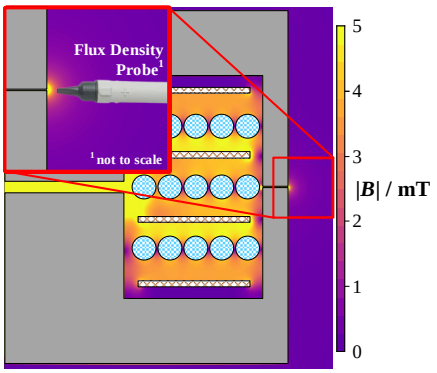
(e) $\hat{p}_{\text{mag,m}}$, $L_\text{m} = 270\,\mu\text{H}$ (f) $\check{p}_{\text{mag,m}}$, $L_\text{m} = 270\,\mu\text{H}$)

(g) scatter L_r (h) scatter C_r (i) scatter L_m (j) scatter n

FIGURE 2.38: (a-f) deviation analysis of the magnetizing morphing ratio $p_{\text{mag,m}}$ for different magnetizing inductances $L_\text{m} \in \{100, 160, 270\}\,\mu\text{H}$ current. Green: positive parameter deviation, black: no parameter deviation, red: negative parameter deviation. Every column in every sub figure shows all simulations where the color indicates, which parameter deviation is present for the column parameter. (g-j) scatter representation for the results displayed in (f) (parameters: $\text{Config}_{2.1p}$).

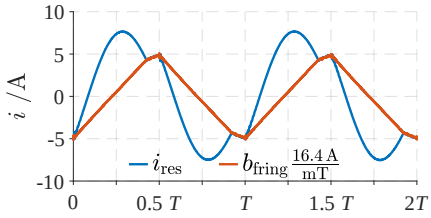
B Offline control of the magnetizing current

Section 2.1.3A showed that it is possible to suppress the undesired peak in the magnetizing current in a stationary operation by utilizing adjusted positive and negative inverter voltage pulses. To dynamically adjust the inverter voltage pulse length, the pulse length is controlled in the transition. This can be done in a switched-circuit simulation to derive a look-up table that can be implemented on a prototype. Figure 2.36a shows the control structure that is used to control the magnetizing current in the morphing transition and to obtain the LUT. Two sample-and-hold blocks are

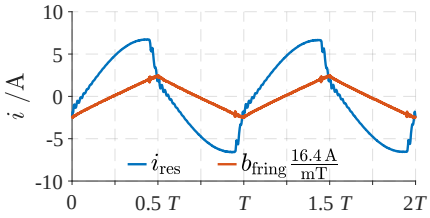


(a) FEM simulation (rotational-symmetrical) with 50 µm gap on the outer leg

(b) Laboratory sensor setup



(c) Measurement results for an LLC operation below resonance (DCMB-operation)



(d) Measurement results for an LLC operation above resonance (CCMA operation)

FIGURE 2.39: Experimental setup to evaluate the developed concept for avoiding significantly larger magnetizing flux densities during the morphing transition. (a) even small gaps at the glue spot (here FEM simulation for 50 µm) result in a small fringing field. (b) experimental sensor setup of the I-prober 520 by AIM TTi. (c,d) experimental measurements of the fringing field (at full bandwidth) scaled to the resonant current as a pseudo magnetizing current. The measurements conform with the conventional LLC magnetizing current shape.

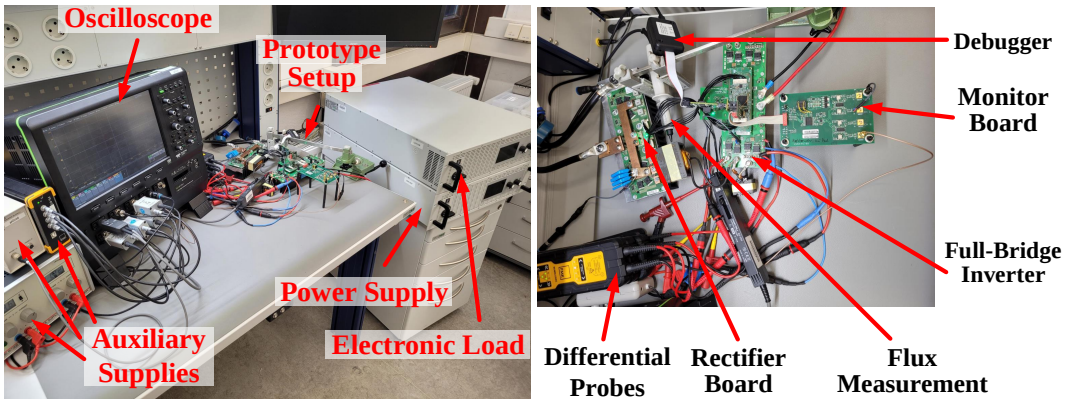
used to acquire the dynamic average of the magnetizing current, which is eventually fed to a flux controller (setup as a PI controller). An overlying output voltage controller sets the switching frequency to stabilize the output voltage. The LUT that is derived from this simulation can then be employed on an experimental prototype as shown in the control structure in Figure 2.36b. The start of the transition triggers a negative ramp for the negative inverter voltage pulse length $d_{\mathrm{m}}T$ from 0.5 to 0, which is then fed into the LUT to obtain the positive inverter voltage pulse length $d_{\mathrm{inv}}T$. A PI controller is again used to control the output voltage by altering the switching frequency.

Figure 2.37 shows simulation results for the conventional morphing transition (Figure 2.37a) and the morphing transition with double-asymmetrical duty cycles (Figure 2.37b). A morphing offset of the magnetizing current was prevented by the control of d_{inv}. While the conventional morphing transition results in the aforementioned increase of about 70 % compared to the steady state, the double-asymmetrical morphing transition can fully prevent an increased magnetizing current. The acquired LUT is depicted for two different loads in Figure 2.37c. From the visualization it is evident that the load dependency is very small.

C Parameter deviation analysis

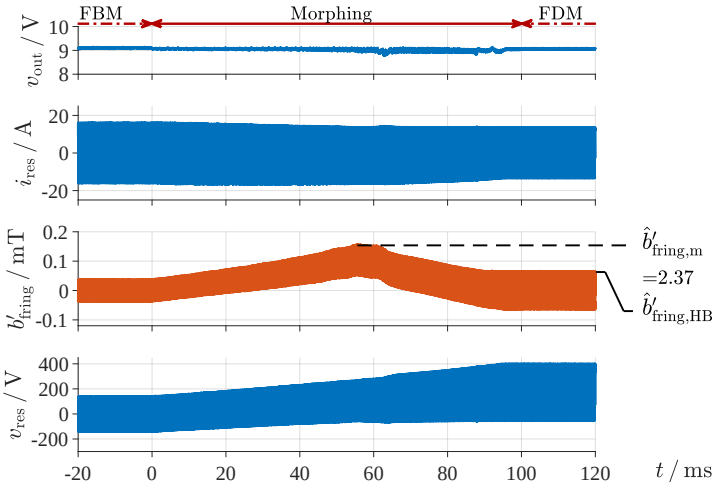
To analyze the impact of parameter deviations, the on-the-fly morphing transition was simulated for a fixed LUT derived for $L_{r,nom}$, $C_{r,nom}$, $L_{m,nom}$ and n_{nom} with the following parameters: $L_r \in \{0.95, 1, 1.05\}L_{r,nom}$, $C_r \in \{0.95, 1, 1.05\}C_{r,nom}$, $L_m \in \{0.95, 1, 1.05\}L_{m,nom}$ and $n \in \{0.95, 1, 1.05\}n_{nom}$ amounting to $3^4 = 81$ simulations. The base values for the parameter deviation analysis are as follows: $L_{r,nom} = 30\,\mu H$, $C_{r,nom} = 90\,nF$, $L_{m,nom} \in \{100\,\mu H, 160\,\mu H, 270\,\mu H\}$ and $n_{nom} = 14.7$. The impact on the morphing ratio $\hat{p}_{mag,m}$ and $\check{p}_{mag,m}$ (2.27,2.28) is displayed in Figure 2.38 (a-f). In each column all simulations are displayed simultaneously and the color of the dots display whether there is a positive deviation (green), no deviation (black) or negative deviation (red). The color of the dots displayed in each columns hereby indicates the type of component deviation labeled at the column. The largest value of $\check{i}_{mag,m}/\check{i}_{mag,HB}$ displayed in Figure 2.38f ($\check{i}_{mag,m}/\check{i}_{mag,HB} = 1.211$) is shown in all columns simultaneously and is caused by a negative deviation (red) for L_r and C_r and a positive (green) deviation for L_m and n. A more common visualization of the results is shown in the scatter representation depicted in Figure 2.38g-2.38j. Here the results displayed in Figure 2.38f are depicted in a different method to show the parameter influence.

The results show that a parameter deviation has almost no influence on the magnetizing current morphing ratio $\hat{p}_{mag,m}$ (2.27). However, $\check{p}_{mag,m}$ (2.28) is highly influenced. Especially if the transformation ratio n is estimated too large (displayed as green dots in the column of n), which is also an indicator that the resonant tank gain does not fit to the conversion gain of the LUT derivation, the pre-recorded LUT results in a substantial minimum magnetizing current value ratio of up to $\check{i}_{mag,m}/\check{i}_{mag,HB} = 21\,\%$ (cf. Figure 2.38f for $n = 1.05\,n_{nom}$, $L_r = 0.95\,L_{r,nom}$, $C_r = 0.95\,C_{r,nom}$, $L_m = 1.05\,L_{nom}$). Furthermore, an under-estimation of the resonant inductance L_r and resonant capacitance C_r has a minor impact on $\check{p}_{mag,m}$. These results are also emphasized by the representation of the results in Figure 2.38g-2.38j showing that the influence of L_r, C_r and L_m is minor compared to the influence of n.

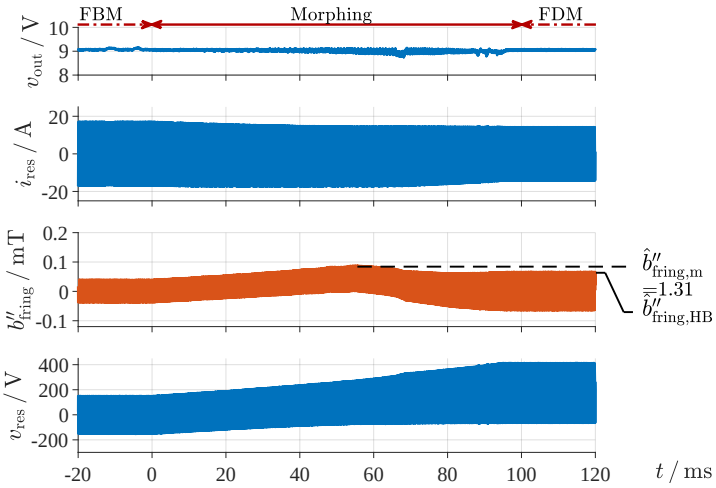


(a) Laboratory setup (b) Prototype setup

FIGURE 2.40: Photos of the laboratory (a) and prototype setup (b).



(a) Conventional morphing with $L_m = 270\,\mu H$



(b) Conventional morphing with $L_m = 100\,\mu H$

FIGURE 2.41: Experimental measurement results of the on-the-fly morphing transition (conventional) for two different magnetizing inductances (270 µH and 100 µH). The transitional magnetizing flux morphing ratio is much more severe for the large magnetizing inductance (parameters: $\text{Config}_{2.1q}$).

D Experimental verification

The LUT has been implemented on an experimental prototype. To evaluate the performance of the adjusted voltage pulses during the morphing transition, it is required to measure the transformer flux over a wide frequency range. On the one hand, it is necessary to measure the low-frequency impact to analyze the impact of a DC offset. On the other hand, it is necessary to analyze the switching frequency impact on the maximum transformer flux. Therefore, it is not possible to integrate the voltage signal of a test winding as the integration over several tens of milliseconds inevitably results in errors that aggravate the longer the morphing transition lasts. Instead the I-prober 520 by AIM TTi was employed as it offers a wide measurement range between DC and 5 MHz. Offering a maximum flux density measurement of 2.5 mT, the probe was employed to measure the fringing field in the glue spots of the transformer. The test transformer is made of two E-cores that are taped or glued together. At the glue spot, there is an inevitable small gap where the glue is applied. Figure 2.39a shows a finite element analysis for a gap of 50 µm. The simulation

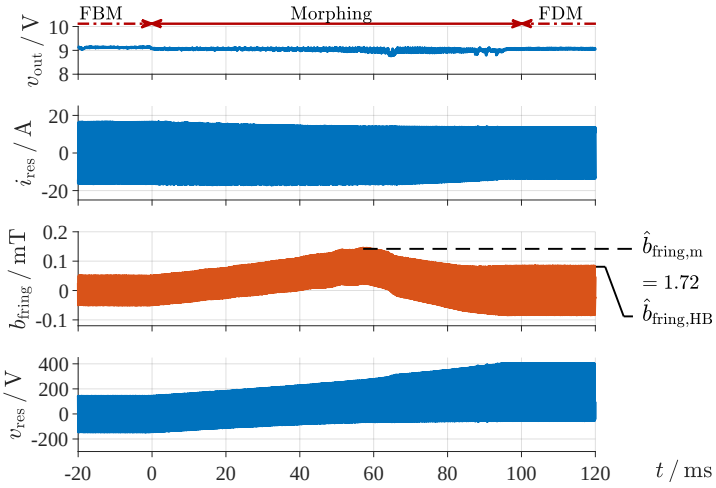
shows that the flux density in the transformer core can implicitly be measured at the fringing field of the glue spots. In the proximity of the glue spot, a field intensity of several millitesla can be measured. Figure 2.39b shows the experimental sensor setup. In Figure 2.39c and Figure 2.39d the shape of the field is depicted where it was scaled with 16.4 $\frac{\mathrm{A}}{\mathrm{mT}}$ to show it with the resonant current as a pseudo magnetizing current. The measurements show that the sensor acquires an accurate representation of the actual flux shape and can be used to evaluate the morphing transition. A visualization of the measurement setup is displayed in Figure 2.40.

To indicate the ratio of the maximum fringing field value during the morphing compared to the maximum fringing field value during half-bridge modulation and the respective ratio of the minimum fringing field value during the morphing to the minimum fringing field value in half-bridge modulation, two variables shall be defined as

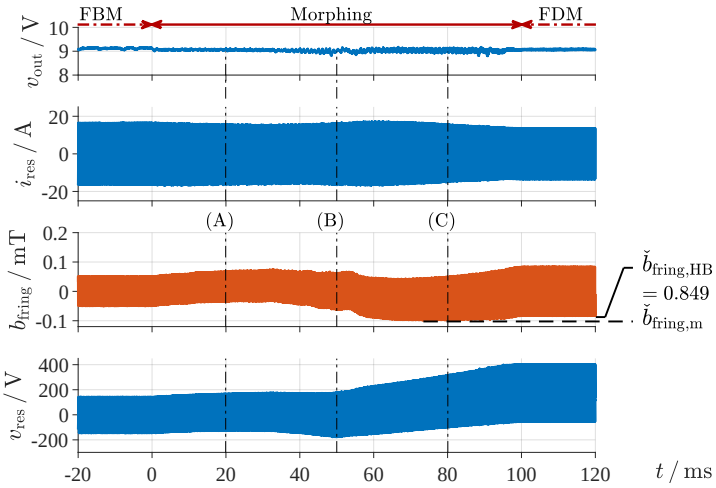
$$\begin{aligned} \hat{p}_{\mathrm{fring,m}} &= \frac{\hat{b}_{\mathrm{fring,m}}}{\hat{b}_{\mathrm{fring,HB}}}, \\ \check{p}_{\mathrm{fring,m}} &= \frac{\check{b}_{\mathrm{fring,m}}}{\check{b}_{\mathrm{fring,HB}}}. \end{aligned} \tag{2.36}$$

Figure 2.41 shows the conventional morphing transition for two different magnetizing inductances L_{m} for an input voltage of $V_{\mathrm{in}} = 350\,\mathrm{V}$, an output voltage of $V_{\mathrm{out}} = 9\,\mathrm{V}$ at an output current of $I_{\mathrm{out}} = 130\,\mathrm{A}$. As two different transformers were used, the flux sensor could not be positioned at exactly the same place. However, this is not a problem as only $\hat{p}_{\mathrm{fring,m}}$ (2.27) is of interest and not the amplitude. To indicate that the field was not measured at exactly the same position, the fringing field is labeled b'_{fring} and b''_{fring} respectively. While $\hat{p}_{\mathrm{fring,m}}$ for the large magnetizing inductance ($L_{\mathrm{m}} = 270\,\mu\mathrm{H}$) is very large (137 %, cf. Figure 2.41a), for a smaller magnetizing inductance ($L_{\mathrm{m}} = 100\,\mu\mathrm{H}$), $p_{\mathrm{fring,m}}$ is much smaller (31 %, cf. Figure 2.41b) proving the analysis of Section 2.1.2C.

An experimental comparison of the conventional and proposed transition is depicted in Figure 2.42 for a magnetizing inductance of $L_{\mathrm{m}} = 160\,\mu\mathrm{H}$, an input voltage of $V_{\mathrm{in}} = 350\,\mathrm{V}$, an output voltage of $V_{\mathrm{out}} = 9\,\mathrm{V}$ at an output current of $I_{\mathrm{out}} = 130\,\mathrm{A}$. Figure 2.42a shows the conventional transition with $d_{\mathrm{inv}} = 0.5$ whereas Figure 2.42b presents the transition with adjusted voltage pulses d_{inv}. In between both transitions, the experimental prototype was not moved or touched. Both transitions were measured within ≈10 minutes. Figure 2.44a - 2.44c show the intervals of the transition that are depicted in Figure 2.42b. The measurements were performed with a step width of 80 ns. The inverter voltage v_{AB}, the resonant capacitor voltage v_{res} and the gate voltages v_{S3} and v_{S4} were filtered with a moving average of four elements to mitigate EMI noise in the measurements that were performed with *Bumblebee* differential probes, which have a comparably large measurement loop. Furthermore, the fringing field b_{fring} was measured with a reduced measurement bandwidth of 500 kHz to mitigate the effects of switching transients, which were visible in the full-bandwidth measurements of Figure 2.39d. This allows a direct interpretation of the measurement results as the low-frequency components of the flux are of primary interest whereas the very-high-frequency components of the flux shape do not significantly influence the core utilization. During the transition, the LLC resonant converter was operated with switching frequencies between 100 kHz and 170 kHz.



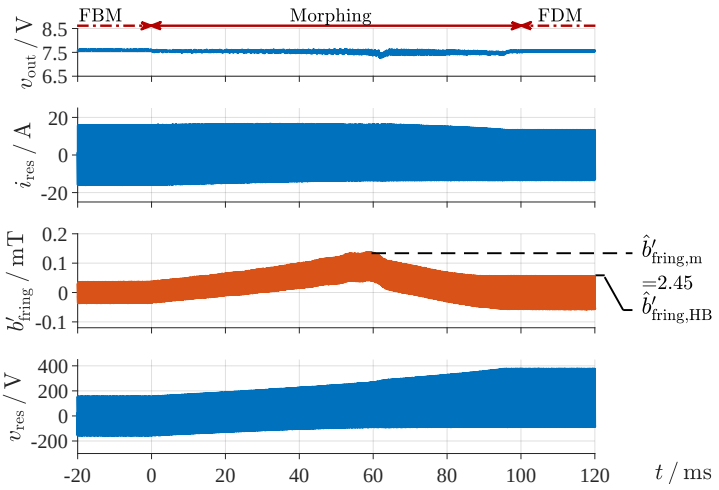
(a) Conventional morphing with $L_m = 160\,\mu H$



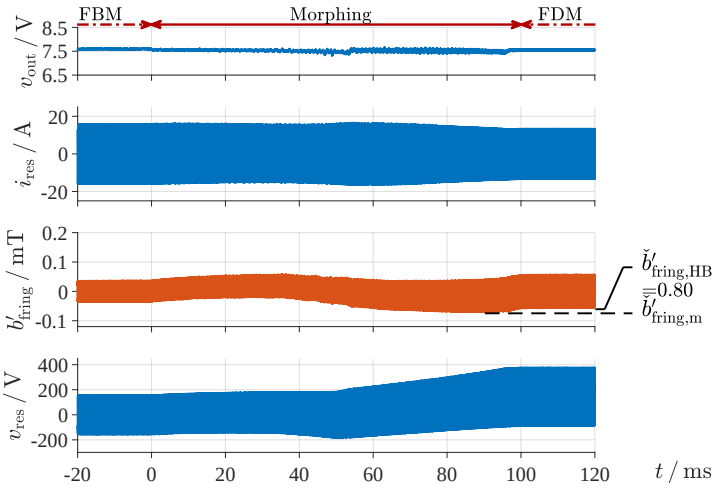
(b) Proposed morphing with $L_m = 160\,\mu H$

FIGURE 2.42: Experimental evaluation of the adjusted morphing transition. (a) full-bridge to frequency-doubler modulation with conventional voltage pulses. (b) proposed full-bridge modulation to frequency-doubler modulation with adjusted voltage pulses to reduce $\hat{p}_{fring,m}/\check{p}_{fring,m}$. With the proposed modulation, it was possible to reduce the maximum deviation from steady state from 66.5 % to $\frac{1}{0.849} - 1 = 18\,\%$ such that the absolute deviation was reduced by 75 % (parameters: $\text{Config}_{2.1r}$).

Another experimental transition is depicted in Figure 2.43 for a magnetizing inductance of $L_m = 270\,\mu H$, an input voltage of $V_{in} = 290\,V$, an output voltage of $V_{out} = 7.5\,V$ at an output current of $I_{out} = 130\,A$. The LUT for the positive inverter voltage-pulse length remained the same as for the transition in Figure 2.42. The modified magnetizing inductance was achieved by altering the center air gap of the transformer. This means that the flux sensor needed to be repositioned to the new transformer. To emphasize the new flux measurement, Figure 2.43 shows the altered fringing field measurement as b'_{fring} instead of b_{fring}. Figure 2.43a shows the conventional transition with $d_{inv} = 0.5$ whereas Figure 2.43b shows the transition with adjusted voltage pulses d_{inv}. Compared to the transition displayed in Figure 2.42, for the conventional case, $\hat{p}_{fring,m}$ is much more significant due to the larger magnetizing inductance. The ratio $\check{p}_{fring,m}$ of the proposed transition is also larger, however with $\check{p}_{fring,m} = 25\,\%$ it is much smaller than the conventional case with $\hat{p}_{fring,m} = 145\,\%$.



(a) Conventional morphing with $L_{\text{m}} = 270\,\mu\text{H}$



(b) Proposed morphing with $L_{\text{m}} = 270\,\mu\text{H}$

FIGURE 2.43: Experimental transition for a large magnetizing inductance. (a) full-bridge to frequency-doubler modulation with conventional voltage pulses. (b) proposed full-bridge to frequency-doubler modulation with adjusted voltage pulses to reduce the magnetizing flux offset. The absolute deviation was reduced by 83 % (parameters: Config$_{2.1s}$).

All depicted transitions of Figures 2.42 and 2.43 show a negative magnetizing flux offset for the proposed transition instead of a positive magnetizing flux offset for the conventional transition. An explanation of this phenomenon may be that in approximately the last third of the morphing modulation, hard switching results, which significantly reduces the converter efficiency before entering half-bridge mode[1]. Therefore, the negative magnetizing flux offset may be a result from these and other parasitics that were not considered in the PLECS simulation that was used to obtain the LUT.

A list of the conventional transition and the proposed transition is displayed in Table 2.4 for three different operating points and three different magnetizing inductances. The results show that the proposed approach is always significantly better

[1] the hard switching is a common trait of the morphing transition and was first reported for the conventional morphing modulation in [JI15a; JI16].

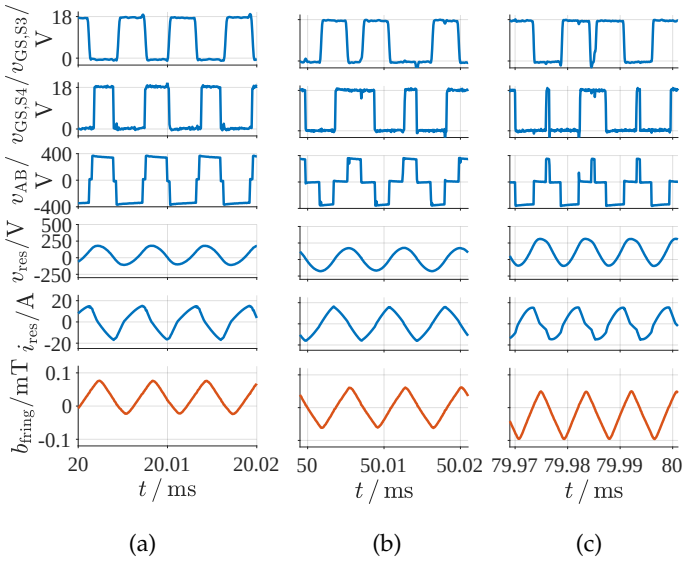


FIGURE 2.44: Measured close-ups of the intervals depicted in Figure 2.42b.

than the conventional transition for all evaluated operating points and magnetizing inductances. The results prove the developed concept. While the conventional transition results in large magnetizing flux morphing ratio, the adjusted transition is able to substantially reduce the core exploitation. In average, $\check{p}_{\text{fring,m}} / \hat{p}_{\text{fring,m}}$ was reduced by 78 % (cf. Table 2.4). This shows that the method can be successfully employed to avoid the use of much larger ferrite cross sections, which eventually reduces the transformer size.

TABLE 2.4: Measured values for $\hat{p}_{\text{fring,m}}/\check{p}_{\text{fring,m}}$ (2.36) for the on-the-fly morphing transition for three different magnetizing inductances and operating points for the conventional and proposed transition

operating point (V_{in},V_{out})		$\max(\hat{p}_{\text{fring,m}}, \check{p}_{\text{fring,m}})$		
	L_{m} / type	100 µH	160 µH	270 µH
290 V 7.5 V	conventional	32.2 %	69.8 %	**145.0 %**[1]
	proposed	1.64 %	11.8 %	**24.7 %**[2]
	reduction	94.9 %	83.1 %	83.0 %
350 V, 9 V	conventional	**35.3 %**[3]	**72.0 %**[4]	**139.9 %**[5]
	proposed	8.03 %	**17.8 %**[6]	35.7 %
	reduction	77.3 %	75.6 %	74.5 %
410 V, 10.5 V	conventional	29.8 %	68.6 %	140.1 %
	proposed	10.97 %	18.7 %	32.9 %
	reduction	63.2 %	72.7 %	76.5 %

[1] displayed in Figure 2.43a
[2] displayed in Figure 2.43b
[3] displayed in Figure 2.41b
[4] displayed in Figure 2.42a
[5] displayed in Figure 2.41a
[6] displayed in Figure 2.42b

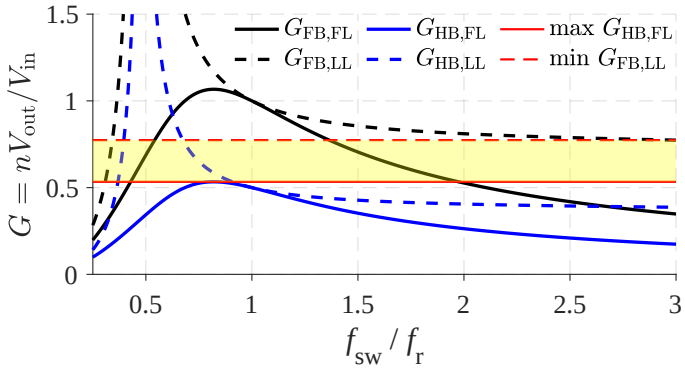


FIGURE 2.45: Gain behavior calculated using the fundamental-harmonic approximation (FHA) for $\lambda = 0.3$ and $Z = 19$ for full load ($R_0 = 0.107\,\Omega$) and light load ($R_0 = 1.07\,\Omega$, 10 % load). For full-bridge operation it is not possible to sufficiently reduce the gain for light-load operation ($\max(G_{HB,FL}) < \min(G_{FB,LL})$). Therefore, *phase-shift operation* will be utilized. The yellow area shows exemplary the phase-shift operating area at 10 % load.

2.1.4 LLC analysis operating in half- and full-bridge mode

this section has been previously published in parts in [Reh+20b; RSB21].

In the past, many methods have been proposed to utilize the LLC in wide VTR applications. A comprehensive analysis of these methods has been performed in [CLW18][1] where the methods were divided into four categories: *modification of the resonant tank*, *modification of the primary-side switch network*, *modifications on the secondary-side rectifier* and *control strategies*. The first three methods utilize additional components. On the contrary, the use of control strategies does not result in additional components and in a detrimental power density and increased costs. One of the control strategies suggests operating a full-bridge inverter in half-bridge configuration by permanently turning one low-side switch on and turning the other high-side switch of this half-bridge off [Lia+10]. This results in a gain reduction by a factor of two making it especially suitable for low VTR. However, sudden switching from a full-bridge to a half-bridge configuration during operation lead to transients in the resonant current and resonant voltage. *Jovanovic* [JI16; JI15a] introduced the on-the-fly topology morphing method, which has been described in Section 2.1.2A and which was improved in Section 2.1.3, to modify the inverter configuration during morphing while avoiding undesirable transients of the resonant current and voltage.

To cover the wide VTR of this application, this section presents a comprehensive design procedure for an LLC converter of operated in full-bridge configuration for large VTR while being operated in half-bridge configuration (see Section 2.1.1B) for VTRs such that the gain is reduced by two. The LLC and all following topologies are designed to run with an input voltage $V_{in} \in [200\,V, 420\,V]$ and an output voltage of $V_{out} \in [8\,V, 16\,V]$ at a maximum power of $P_{out} = 2.24\,kW$ and a maximum output current of $I_{out} = 130\,A$. For an input voltage smaller than $V_{in} = 240\,V$, the maximum output current is proportionally reduced from its maximum current at the operating

[1] this publication analyzed a wide range of methods to achieve wide-voltage transfer ratios. Therefore, this publication is considered sufficient as a literature review of existing methods.

output voltage to $I_{out} = 100\,A$ at $V_{in} = 200\,V$. This is the derated operating region. For the minimum gain operation, a minimum current of $I_{out} = 10\,A$ is considered.

The gain behavior of the LLC is visualized in Figure 2.45 for full load and light load in both configurations. The analysis reveals that not every operating point that may be achievable at partial load can also be achieved at full load, such that a determination of the operating regions based on the efficiency as was done in [JI16; JI15a] may be problematic as a transient load step in half-bridge may require a mode change to full-bridge configuration. However, the on-the-fly topology-morphing transition of [JI16; JI15a] lasts several milliseconds, which is too slow for most applications to react to load changes that require a controlled output voltage/current within hundreds of microseconds. Consequently, the half-bridge operating region needs to be determined based on the maximum achievable full-load gain.

Furthermore, the analysis of Figure 2.45 reveals that the maximum half-bridge full-load gain $G_{HB,FL}$ is much lower than the full-bridge light-load gain $G_{FB,LL}$ such that even an operation at large switching frequencies cannot sufficiently reduce the gain in light load. In [Kim+14; Kim+15] it was shown that phase-shift operation can increase the partial-load efficiency for full-bridge LLC converters. Consequently, for intermediate gains and loads, the LLC is operated in phase-shift modulation (see Section 2.1.1A1-2.1.1A6).

A further limitation of the half-bridge operation may be the resonant capacitor voltage. During half-bridge operation, the resonant capacitor voltage has an offset of half the input voltage adding to the AC value. To employ resonant capacitors of smaller blocking voltages, it may be beneficial to limit the half-bridge operating region and expand the full-bridge operating region. The two above factors limit the operating region where half-bridge configuration may be employed such that operating points at intermediate VTRs must be covered in full-bridge configuration at elevated switching frequencies. For large loads, minor changes in the switching frequency result in substantial changes in the converter gain because the gain curve is steep. For small loads, however, the converter gain is flat resulting in even larger switching frequencies. Furthermore, not all light-load operating points can be reached in the conventional-controlled operation as more power is transferred to the output than required resulting from charging the parasitic output capacitance of the rectifier semiconductors. For intermediate VTRs and low gains, it may be beneficial and necessary to operate the LLC in phase-shift operation [Kim+15; Kim+14; Lo+11;

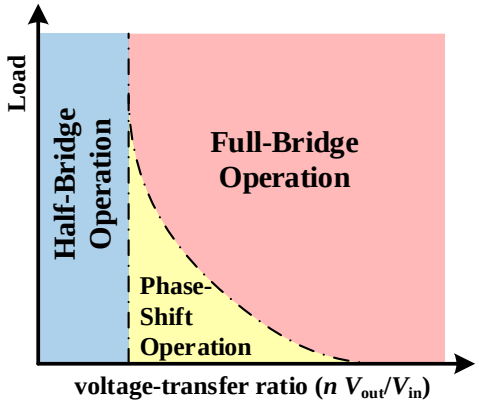


FIGURE 2.46: Qualitative representation of the different operating modes depending on the converter's voltage transfer ratio and load.

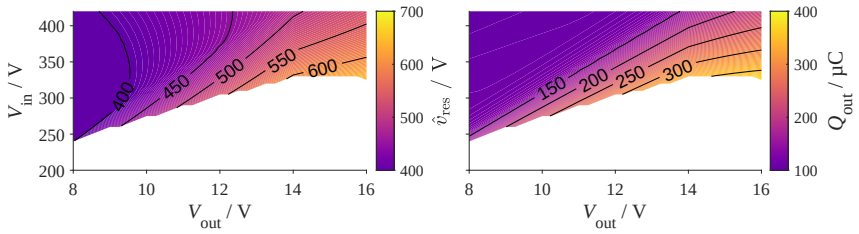


FIGURE 2.47: Dependency of the maximum resonant capacitor voltage $\hat{v}_{res}$ and output charge Q_{out} over the input and output voltage in half-bridge mode (parameters: $\text{Config}_{2.1t}$).

MW14; Sha+16; Liu+14]. The resulting operating concept is depicted in Figure 2.46.

To calculate the stressing values efficiently and accurately, time-domain analysis of the LLC converter was described for variable-frequency control in [Den+15; Hu+16b; Keu+17; LM01; Wei+20b; WLM20a; Wei+20a; Wei+21a; Yu+12; Fig16] and phase-shift control in [Liu+16b]. For this thesis, the tools developed by *Figge* [Fig16] and *Keuck* [Keu+17; Keu23] are adopted.

A Analysis of the half-bridge modulation

In a half-bridge configuration, the resonant voltage has an offset of half the input voltage. Large AC values resulting from an operation below resonance may destroy the resonant capacitors when the maximum peak voltage is surpassed. An operation below resonance also leads to large output charges translating into bulky output capacitors. Figure 2.47 shows the maximum resonant capacitor voltage and the output charge over the input and output voltage. White areas represent operating regions where half-bridge configuration cannot be applied as the maximum gain does not permit such a large VTR. It is evident that large input voltages in combination with large VTRs result in very large resonant voltages and – through the large output charge – in a large output capacitance. The magnetizing current is displayed together with the peak resonant current in Figure 2.48. The low switching frequency required for the large VTRs results in large peak resonant and magnetizing currents that define the inductor design. The regions with exceedingly large resonant voltages and currents should thus be avoided to avert large costs resulting from the large resonant currents and the large resonant capacitor blocking voltages. If ceramic capacitors are selected, the standard capacitors are of C0G-technology, which come with small component deviations making them feasible for a good resonant tank match. Common capacitors in the small 1206-package come with a typical breakdown voltage of $600 - 630\,\text{V}$. To retain a sufficient margin, the maximum resonant capacitor voltage is selected to be $\hat{v}_{res} = 500\,\text{V}$[1].

B Analysis of the conventional full-bridge modulation

Low loads cannot always be achieved by increasing the switching frequency. To achieve operating points at a low VTR in FBM, high switching frequencies become necessary resulting in increased switching losses. Furthermore, the output capacitance of the synchronous rectifiers/diodes may prevent an operation overall (section 2.1.1). Figure 2.49 shows exemplary the necessary switching frequency over the

[1] it is equally possible to employ resonant capacitors of larger blocking voltage to further increase the modulation region of the half-bridge configuration or to further reduce the operating region of the half-bridge modulation to retain a sufficient control margin. This can be subject to an iterative improvement of the resonant tank depending on the requirements of the application.

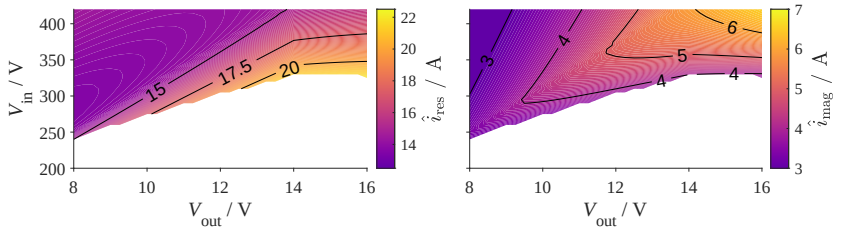


FIGURE 2.48: Dependency of the maximum resonant current $\hat{i}_{res}$ and magnetizing current $\hat{i}_{mag}$ over the input and output voltage in half-bridge mode (parameters: Config$_{2.1t}$).

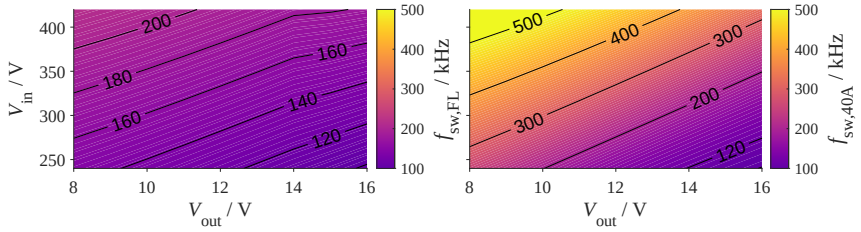


FIGURE 2.49: Switching frequency at full load $f_{sw,FL}$ and at an output current of 40 A $f_{sw,40A}$ at full-bridge mode (parameters: Config$_{2.1t}$).

operating region in FBM at $I_{out} = 130$ A and $I_{out} = 40$ A. Areas that permit HBM are greyed out. For full-bridge mode, they are depicted in Figure 2.50.

It is evident that for this set of parameters the necessary switching frequency for an output load of $I_{out} = 100$ A is quite high as a switching frequency of more than twice the resonant frequency is necessary. For a reduced load of $I_{out} = 50$ A the necessary normalized switching frequency of larger than three is unacceptable. For these operating points PSM is a suitable modulation scheme to achieve higher efficiencies. The exact switching frequency where the mode should be changed can be derived for each operating point individually through a loss analysis to maximize the efficiency[1]. For the first step, a maximum switching frequency of $f_{sw}/f_{res} = 2$ is assumed for the design procedure[2]. A first-step selection of a maximum switching frequency is necessary to analyze the rectifier current for the output load, at which the operation is shifted to PSM. This analysis is important because the secondary transformer current becomes discontinuous in PSM resulting in increased RMS currents.

[1] this analysis needs to be done for all sets of input voltages, output voltages and output loads, which makes the analysis very time consuming and hard to implement as a three-dimensional look-up table results.

[2] this is justified as the characteristic operating points are necessary for the thermal design only. With the selection of suitable magnetic components, semiconductors, etc. it is, however, possible to include the light-load operating points and analyze the losses through the switching frequency.

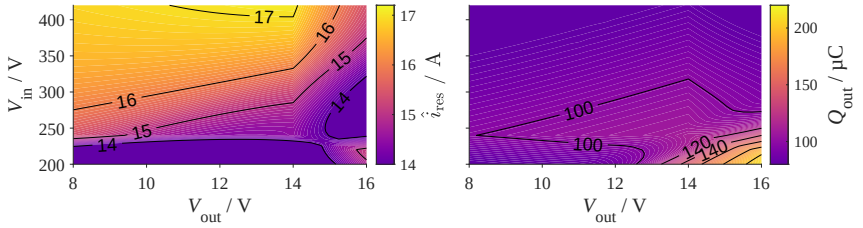


FIGURE 2.50: Maximum resonant current $\hat{i}_{res}$ and output charge Q_{out} in full-bridge mode (parameters: $\text{Config}_{2.1t}$).

C Analysis of phase-shift operation

Phase-shift operation is a suitable operating mode for low loads to avoid exceedingly large switching frequencies that are linked to large switching losses. By employing this operating mode, the LLC converter can be designed for a smaller inductance ratio $\lambda = \frac{L_r}{L_m}$ reducing the circulating currents in full load through a reduced magnetizing current. However, as the phase shift increases, the energy-transfer interval reduces (*see* Section 2.1.1A3). This implies that the turn-off current of the lagging leg reduces from the reduced ripple of the magnetizing current such that turn-off current of the switches is reduced. While typically, it is assumed that during the dead time the resonant inductor acts like a current source making ZVS always possible by adjusting the dead time [ASS09; Bei+11; KYS17; Lu+06; Wei+21b], it has been shown that this is not always the case [Keu+17; SXZ21]. For large switching frequencies the resonant inductor may not contain sufficient energy to deliver the necessary commutation charge Q_{com} for ZVS. In [SXZ21] an accurate ZVS model and condition was developed allowing an accurate ZVS design. *Keuck et al.* [Keu+17] used the commutation charge from the time-domain analysis (assuming instantaneous switching instances) as an indicator for whether the ZVS can be achieved. While this method generally calculates a commutation charge that is too small[1], it offers a rapid calculation method to estimate the commutation charge and predict whether ZVS can or cannot be achieved.

If the commutation charge is insufficient, the switches are turned-on with a residual voltage ΔV and the MOSFETs are subject to incomplete ZVS losses E_{iZVS}, which may be very large for silicon switches. In [Kas+16], the residual voltage is calculated for galvanically-coupled converters using datasheet parameters by solving the energy balance before and after the switching instant. However, this method cannot be applied for galvanically-coupled converters as the output capacitance of the primary *and* secondary semiconductors influences the switching behavior such that the residual voltage cannot be calculated analytically. A different concept was employed by [SXZ21] where a constant output capacitance was assumed to calculate the ZVS condition for one specific type of operation. In this work, the commutation charge of the time-domain analysis [Keu+17] shall be used to estimate the residual voltage ΔV and calculate the incomplete ZVS losses by employing the equations provided

[1] the charging and discharging of the output capacitances lasts for several nanoseconds. In this interval the resonant current changes only slowly such that a larger commutation charge results.

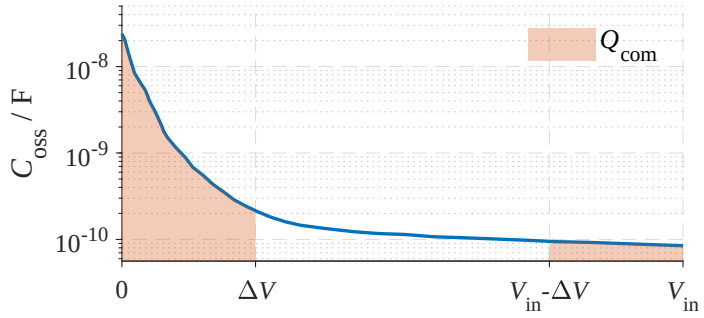


FIGURE 2.51: Visualization of the commutation charge.

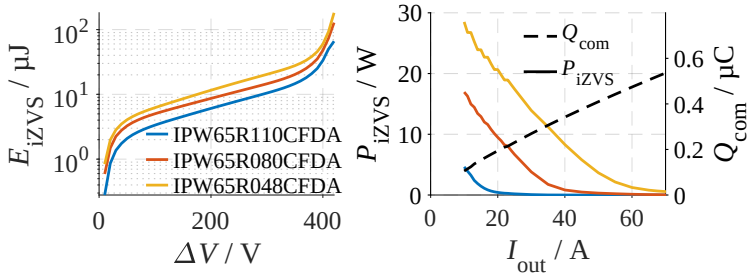


FIGURE 2.52: (Left) Incomplete ZVS losses E_{iZVS} plotted over the residual voltage ΔV, (right) incomplete ZVS losses P_{iZVS} for a resonant frequency of $f_{res} = 100\,\text{kHz}$ plotted with the commutation charge Q_{com} over the output current I_{out} (parameters: Config$_{2.1t}$).

in [Kas+16][1]. The residual voltage is calculated iteratively solving (2.37). The commutation charge and the residual voltage are displayed in Figure 2.51. The residual voltage can be derived by integrating the output capacitance based on

$$\int_0^{\Delta V} C_{oss}(v)\mathrm{d}v + \int_{V_{in}-\Delta V}^{V_{in}} C_{oss}(v)\mathrm{d}v \stackrel{!}{=} Q_{com}. \tag{2.37}$$

Equation (2.37) shows the incomplete ZVS losses E_{iZVS} for three MOSFETs of different on-state resistances plotted over the residual voltage ΔV and the calculated switching losses in $OP_{FB,edge}$ plotted with the calculated commutation charge Q_{com}. The losses are depicted in Figure 2.52. From the analysis, it is evident that a tradeoff needs to be found between the commutation charge and the on-state resistance of the employed MOSFETs . While a small on-state resistance results in low conduction losses at full load, it may lead to exceedingly large switching losses at light load that may potentially destroy the device if the converter is not designed properly. It is therefore necessary to investigate the commutation charge at light-load operation when designing the resonant tank and during selection of the semiconductors.

[1] this approximation results in overestimated incomplete ZVS losses. By calculating an overestimated commutation charge, the residual voltage is calculated too large also. Nevertheless, this approximation is a good approximation in the design procedure to avoid exceedingly large switching losses at light load and evaluate different MOSFETs types. This method avoids a numeric calculation, which is time-intensive and would need to be repeated for every MOSFET of interest.

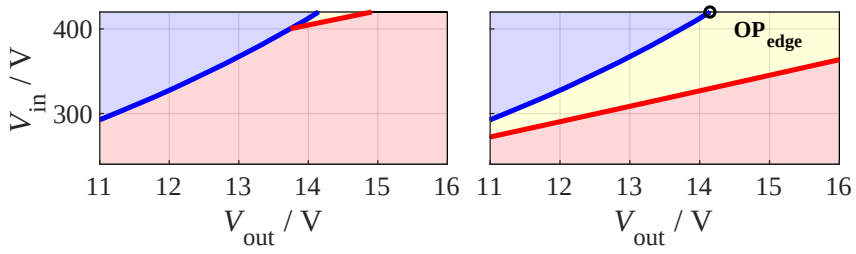


FIGURE 2.53: Visualization of the operating regions for $I_{out} = 100$ A (left) and $I_{out} = 50$ A (right) ($f_{max}/f_r = 2$) (parameters: $\text{Config}_{2.1t}$).

D Characteristic operating points

The combination of the three operating modes is depicted in Figure 2.53. For large loads, most of the operating region is covered with FBM and HBM. For smaller loads, the operating region for FBM decreases while the region with PSM increases. Based on the above analysis, it is possible to define characteristic operating points for the design procedure.

From the analysis, seven critical operating points can be defined: the operating point $\text{OP}_{\text{FB,Gmin,FC}}$ is critical to design the resonant inductor while $\text{OP}_{\text{FB,Gmax,FL}}$ is critical for the design of the output capacitor and to ensure that a sufficient gain can be achieved. The operating points $\text{OP}_{\text{HB,Gmin,FL}}$ and $\text{OP}_{\text{FB,edge,FL}}$ are the operating points with the smallest gain at full load. In these operating points, the conduction losses and the switching losses are large, as a high switching frequency is required to achieve the low gain. These operating points are critical to the design of the semiconductors and the magnetic elements thermal-wise. To avoid very large switching frequencies at light load in half-bridge operation, $\text{OP}_{\text{HB,Gmin,LL}}$ is investigated, while in $\text{OP}_{\text{FB,edge,LL}}$ the commutation charge is investigated to properly design the semiconductors and avoid high incomplete ZVS losses. To avoid large phase shifts in $\text{OP}_{\text{FB,edge}}$ at full load, the operating point is simulated with the maximum switching frequency ($f_{sw}/f_{res} = 2$) at no phase shift to investigate the resulting output current ($\text{OP}_{\text{FB,edge,PS}}$). A large output current hereby results in a large phase shift. All operating points are displayed in Table 2.5. A asterisk (*) at the parameters of OP_{edge} denotes that this value is subject to an iterative solution.

TABLE 2.5: Relevant operating points for the resonant tank design

Name	Abbreviation	V_{in}	V_{out}	I_{out}	Mode
$\text{OP}_{\text{HB,Gmin,FL}}$	OP_1	420	8	130	HB
$\text{OP}_{\text{FB,Gmax,FL}}$	OP_2	240	16	114	FB
$\text{OP}_{\text{FB,Gmin,FC}}$	OP_3	420	14	130	FB
$\text{OP}_{\text{FB,edge,FL}}$	OP_4	420	*	*	FB
$\text{OP}_{\text{FB,edge,LL}}$	OP_5	420	*	10	FB
$\text{OP}_{\text{FB,edge,PS}}$	OP_6	420	*	*	PS
$\text{OP}_{\text{HB,Gmin,LL}}$	OP_7	420	11	10	HB

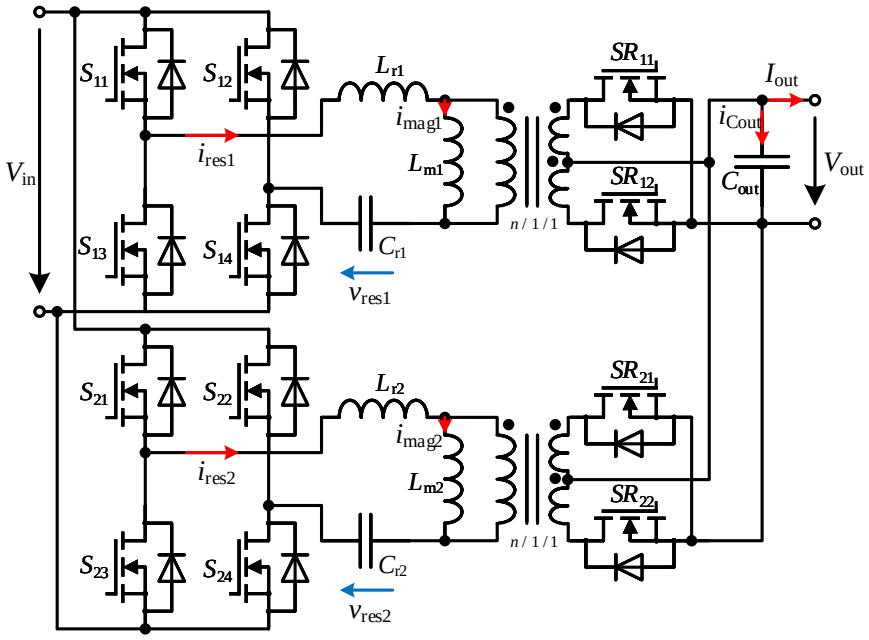


FIGURE 2.54: Interleaved LLC resonant converter.

2.1.5 Interleaving of LLC converters

this section has been previously published in parts in [RSB21; Reh+20b] *and the presented method has been applied for patent in* [RSB20].

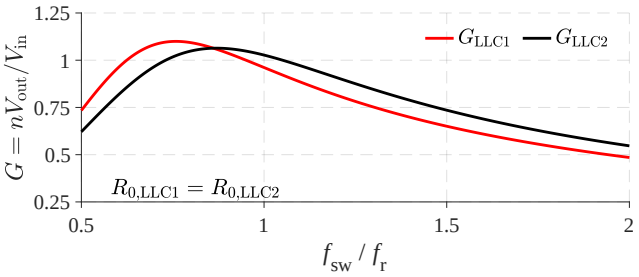
For larger output powers and/or increased light load efficiency, several LLCs (rails) can be connected in parallel (cf. Figure 2.54). This has the advantage that the transferred power is distributed between the converters and - for light load - converters can be switched off completely. This is called *phase-shedding*. If k converters are operated in parallel and the rails can be operated with a phase shift of $\varphi_{PS} = \frac{360}{2k}$ [1] to significantly reduce the current ripple in the input and – more importantly – the output capacitor. This is referred to as *ripple cancellation*. Ripple cancellation has the advantage that the frequency of the capacitors is increased by a factor of k whereas the current ripple is decreased by the same factor. In theory the capacitance can, therefore, be reduced by the factor k^2.

However, component deviances cause a slightly different system behavior preventing an equal operation. Employing the FHA, the gain behavior ($G = \frac{nV_{out}}{V_{in}}$) can be visualized for two LLC converters with a slight parameter mismatch with

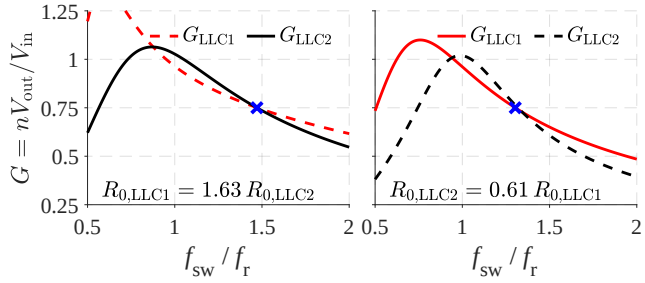
$$G(\lambda, Q, f_n) = \frac{1}{k\sqrt{(1+\lambda-\frac{\lambda}{f_n^2})^2 + Q^2(f_n - \frac{1}{f_n})^2}} \tag{2.38}$$

where

[1] the factor 2 results from the two-pulse topology – energy is transferred twice per period.



(a) Equal-load transfer functions



(b) Equal-gain transfer functions

FIGURE 2.55: LLC transfer functions with a 5 % resonant tank parameter mismatch. For equal output resistance, the mismatch results in a slight gain deviation (a). For both LLC converters the gain is fixed (constant input and output voltage). When operated with equal switching frequencies, different loads result. Exemplary loads are depicted for an equal gain of $G = 0.75$ in (b) for two switching frequencies where the solid lines correspond to the transfer functions of (a). In both cases LLC_2 transfers about 63 % more power than LLC_1.

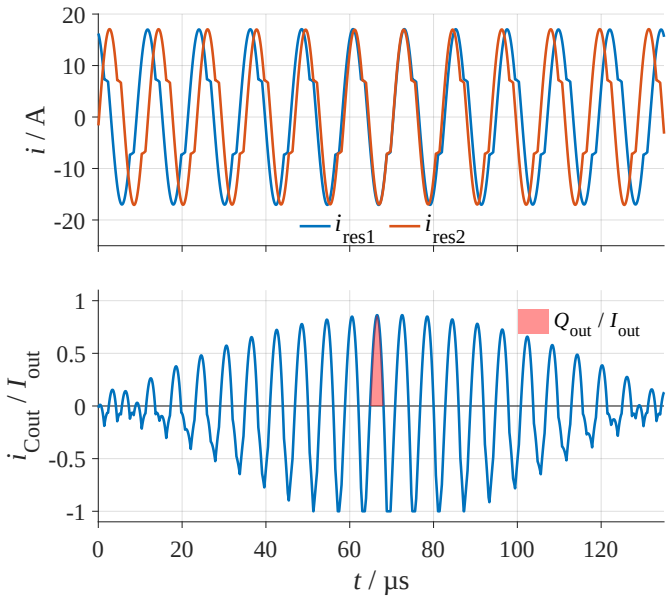
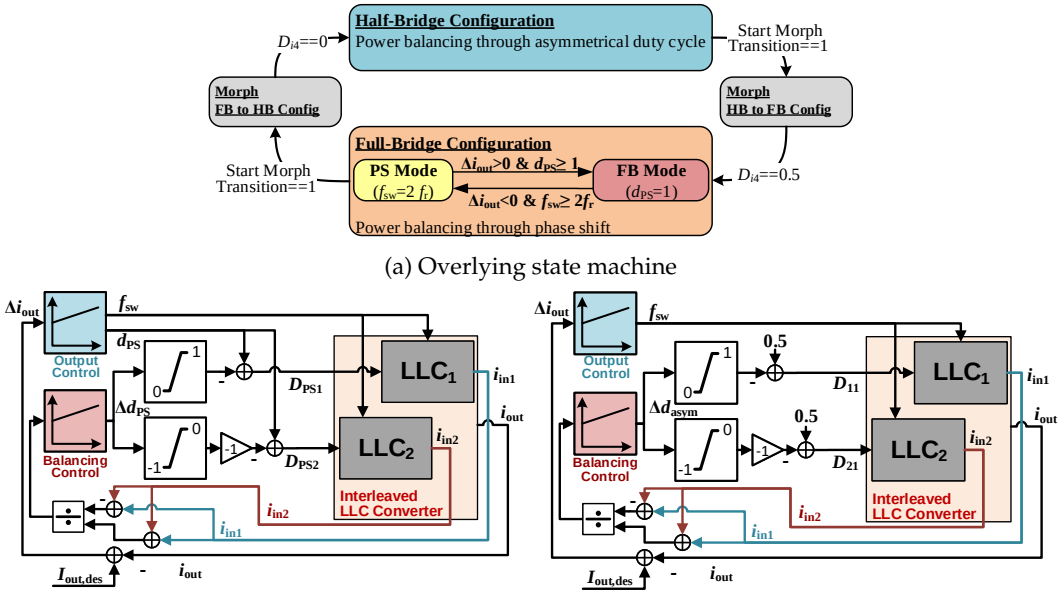


FIGURE 2.56: Two parallel LLC converters operated with unequal switching frequency to balance the transferred power. LLC_1 (i_{res1}) is operated with $f_1/f_r = 0.842$ whereas LLC_2 (i_{res2}) is operated at $f_2/f_r = 0.883$ (parameters: Config$_{2.1u}$).

$$\lambda = \frac{L_r}{L_m},\quad Z = \sqrt{\frac{L_r}{C_r}},\quad f_r = \frac{1}{2\pi\sqrt{L_r C_r}},\quad f_n = \frac{f_{sw}}{f_r}$$
$$Q = \frac{Z}{R_{AC}},\quad R_{AC} = \frac{8}{\pi^2} n^2 R_0,\quad R_0 = \frac{V_{out}}{I_{out}} \tag{2.39}$$

and $k = \{1,2\}$ is the configuration factor ($k = 1$: full-bridge inverter configuration, $k = 2$: half-bridge inverter configuration). Figure 2.55 (a) shows the gain of two LLC converters with worst-case 5 % parameter mismatch of the resonant tank components ($f_{r1} < f_r < f_{r2}$, $\lambda = 0.3$, $Z = 19$, f_r is the nominal resonant frequency). The parameter mismatch results in a gain deviation for equal switching frequencies. If the LLC converters are operated for a gain $G = 0.75$ as in Figure 2.55 (b), LLC_2 always transfers more power because its equivalent output resistance is smaller.

The converter rails must be balanced to ensure that every rail transfers the same power. PWM-based converters are operated at a constant switching frequency and the power transfer is adjusted with the duty cycle or phase shift. This results in an operation with an identical (constant) switching frequency allowing synchronized interleaving with an appropriate phase shift. For LLC converters, however, the transferred power is typically adjusted with the switching frequency such that in conventional operation, paralleled rails are operated at slightly different switching frequencies yielding in a low-frequency beat for the current of the input and output capacitor, which is depicted in Figure 2.56 such that the advantageous ripple cancellation is prevented. Especially for large output currents, this is a significant drawback since the output capacitor needs to be designed much larger. If a C-L-C filter is used, the same applies for the inductor (L), since the effective switching frequency is halved for two parallel converters compared to the 90°-interleaved variant. However, as it is an easy and robust method, it has been applied in [Yan14; YDS15; Mor+21].



(a) Overlying state machine

(b) Control concept in full-bridge configuration

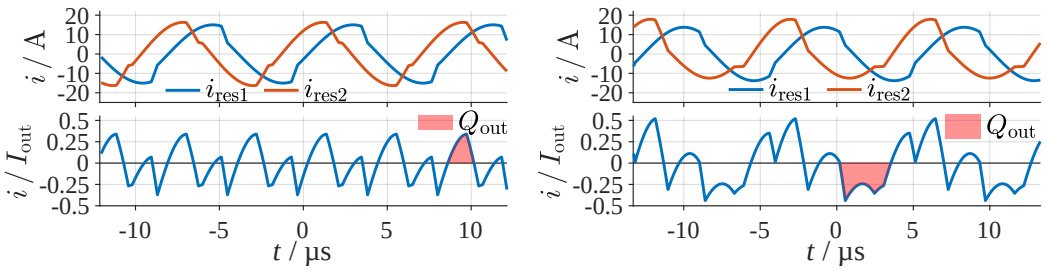
(c) Control concept in half-bridge configuration

FIGURE 2.57: Overlying state machine (a) where D_{i4} is the duty cycle of switch S_{i4}, detailed full-bridge (b) and half-bridge control concept (c) depicting the output and balancing controllers. As the two LLC converters are connected on a common output capacitor, the interleaved converter utilizes a common output current measurement. For small output loads it is also possible to employ phase shedding where one rail is turned off entirely.

A Conventional balancing of LLC converters

To operate paralleled LLCs with equal switching frequencies, many methods have been presented to achieve current ripple cancellation: in [LH14] an additional switched capacitor is described, which balances the resonant tank actively depending on the required operating point. This method requires at least two additional power MOSFETs . In [Xu+16; FSG14; YDS12; Kim+09] the balancing of the converters is achieved by connecting them in series on the input and parallel on the output. The transferred power is hereby inherently adjusted by their respective input voltage. However, this method relies on the series connection. Phase shedding (i.e. the selective shutdown of one leg/rail at low power transfer) is not an option and the converters need to be designed for a lower input voltage such that conduction losses increase. In [Fei+19] a shared power transfer is described for a three-times interleaved LLC by using a star or delta connection on the primary or secondary side. Three separate half bridges were employed as the primary inverters. This structure, however, can only be utilized for a three-phase structure and not for a dual-interleaved design. Furthermore, phase-shedding is problematic. A similar method is pursued in [Wan+16; Wan+17; Wan+18] where a common capacitor or common inductor were employed for a passive balanced power transfer. In [Yan+20], current sharing is achieved by grouping the secondary windings of the transformers requiring a full-bridge rectifier. The resonant currents are at equal phase such that ripple cancellation is not possible. In [KP18], the power transfer is achieved using a flying capacitor for one rail. This results in an automatic balanced power transfer at the cost of an additional component. The general structure of the introduced *two-phase interleaved flying-capacitor LLC*, however, does not allow ripple cancellation as the two converters are basically operated with a phase shift of 180°. In [Jan+15] the balancing is achieved by adjusting the delay time of the secondary low-side synchronous rectifiers of a full-bridge rectification circuit. With this control, a freewheeling interval is introduced on the secondary side, allowing the balancing of the two rails while the two converters can be operated with equal switching frequencies. As a drawback, however, this method can only be applied to full-bridge synchronous rectifier circuits, but not to center-tapped rectifiers. Furthermore, self-controlled synchronous rectification ICs, driving the rectifier MOSFETs locally, cannot be used since the latter have to be synchronized to the central LLC-controller. In [WZX17], an interleaved LLC is presented that utilized a hybrid rectifier. The power transfer is hereby adjusted with the phase-shift angle between the two LLC inverter modules. However, ripple cancellation cannot be achieved with this setup. Finally, in [Fig+08; Fig16; FSG14] a two-stage balancing concept is described. The system consists of two-stage rails. A first-stage, galvanically-coupled DC-DC converter generates the individual input voltage level for the second-stage LLC. By adjusting this input voltage level depending on the transferred power, the balancing of the two rails is achieved while operating them with equal switching frequencies allowing synchronized interleaving and, thus, the current ripple cancellation at the output. However, in principle, this method can only be applied to two-stage concepts but not to a single-stage design. In [FSG14; Fig16], it is shown that power-balancing is possible in full-bridge mode by applying a phase shift to that converter rail transferring more power. However, no implementation on a prototype is described and no design procedure is outlined. If two rails are considered, the LLC rail that transfers more power is operated with a phase shift. This results in a reduction of the VTR such that the transferred power of the rails can be balanced. However, this method can only be applied to full-bridge converters. To the author's knowledge, no method of balancing half-bridge

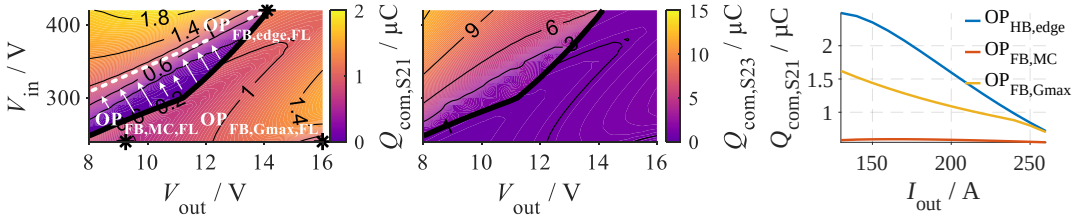
single-stage LLCs[1] without using additional components has yet been proposed.



(a) Phase-shift balancing

(b) Asymmetrical duty-cycle balancing

FIGURE 2.58: Simulation results for (a) phase-shift balancing and (b) asymmetrical balancing with the output charge Q_{out}. (a) parameters: $Config_{2.1v}$, (b) parameters: $Config_{2.1w}$.



(a) Commutation charge for the switches S_{21} and S_{23}

(b) Commutation charge over output load

FIGURE 2.59: (a) Commutation charge $Q_{com,S21}$ (left) and $Q_{com,S23}$ (right) of the switches S_{21} and S_{23} respectively. The LLC_2 is operated in phase-shift operation / in asymmetrical duty cycle modulation to balance the output currents. The operating regions are modified to achieve a larger commutation charge in half-bridge configuration. Upper left: *half-bridge configuration with asymmetrical duty cycle balancing*; lower right: *full-bridge configuration with phase-shift balancing*. All results for full load over the input and output voltage; (b) commutation charge of the critical operating points $OP_{HB,edge}$, $OP_{FB,MC}$ and $OP_{FB,Gmax}$ depicted over the output current.

[1] for an application with a center-tapped rectifier.

B LLC converters balancing using phase-shift and asymmetrical duty cycle operation

To guarantee equal switching frequencies and power transfer of the two interleaved rails, phase-shift balancing is applied for full-bridge configuration. For half-bridge configuration, this thesis proposes to apply an asymmetrical duty-cycle modulation to the rail transferring more power ensuring a balanced power transfer: the switches S_{i1} and S_{i3} of the same bridge-leg are not operated with an equal duty cycle, but complementary with a duty cycle unequal to 0.5.

The state machine for these modes is depicted in Figure 2.57a. As stated, the converter can be operated in half-bridge and full-bridge configuration. A balanced mode transition can be achieved through several special operating modes that are proposed in 2.1.5C. Mode changes are triggered in relation to the VTR at intermediate loads in single-rail operation. In full-bridge configuration, two modulation modes are utilized: for large loads and VTRs, the frequency-controlled *full-bridge mode* is used, whereas for low VTRs and loads, *phase-shift operation* is utilized. In half-bridge configuration, the output is controlled by the switching frequency. Figure 2.57b shows the full-bridge configuration control concept in more detail. A balanced power transfer is achieved by applying an (additional) phase shift to one of the rails. An exemplary simulated phase-shift balanced operation is displayed in Figure 2.58a. The phase shift is adjusted by a balancing controller that gets the deviation of the measured input currents as its input (the deviation is divided by the sum of the input currents to avoid a load-dependent behavior). Figure 2.57c shows the control concept of the half-bridge configuration. The control concept is very similar to the full-bridge concept. The balanced power transfer is achieved by adjusting the duty cycle of the high-side switch S_{i1}. An exemplary simulated asymmetrically-shift balanced operation is displayed in Figure 2.58b. To ensure a stable and robust system behavior, the balancing controller of both configurations needs to be designed of a different dynamic compared to the output control.

When balancing the power transfer of two interleaved rails, the resonant tank mismatch resulting from component deviations has a substantial influence on the system behavior of the LLC operation [KBD20]. In this analysis, it is assumed that the resonant capacitors are subject to a deviation of ± 1 % by utilizing capacitors matching this margin. It is assumed that inductances can be controlled within a margin of ± 5 %, which is supported by the comprehensive analysis given in [Bin+14] that explored the impact of deviations of the ferrite core on the final inductance of the coil. In [Fig16], different possibilities of imbalances were examined, which lead to the conclusion that the worst-case imbalance is apparent when the resonant inductance, resonant capacitance, and magnetizing inductance of the first LLC have a mismatch in the positive direction, whereas the resonant tank components of the second LLC have a mismatch in the negative direction. This leads to the worst-case deviation of the resulting resonant frequencies. The following analysis, therefore, assumes the condition: $L_{r1} = 1.05\,L_r$, $C_{r1} = 1.01\,C_r$, $L_{m1} = 1.05\,L_m$, $L_{r2} = 0.95\,L_r$, $C_{r2} = 0.99\,C_r$, $L_{m2} = 0.95\,L_r$.

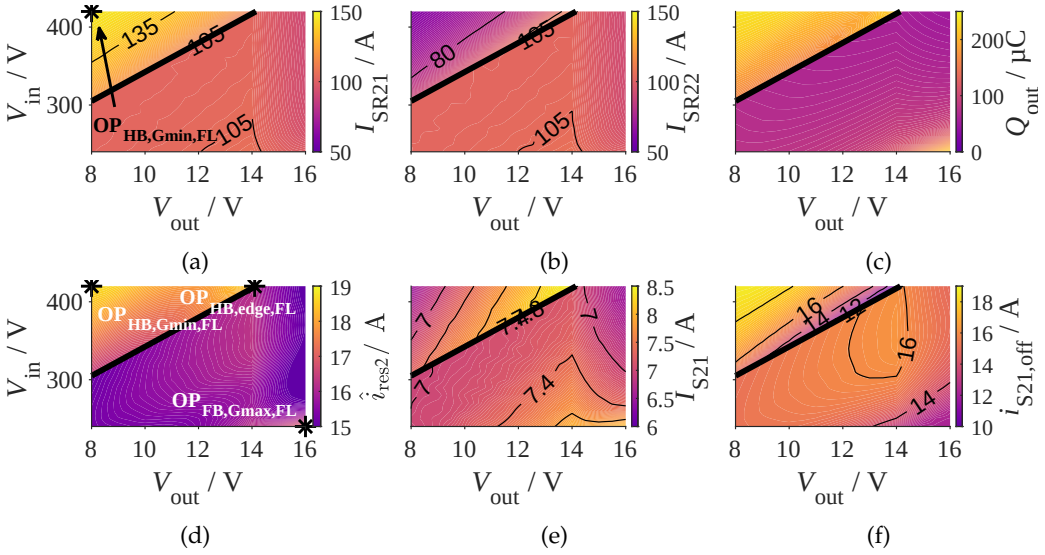


FIGURE 2.60: (a) Synchronous rectifier currents I_{SR21} and I_{SR22} (b); output charge of the common output capacitor Q_{out} (c) and maximum resonant current $\hat{i}_{res2}$ (d); switch RMS current I_{S21} (e) and its respective turn-off current $\hat{i}_{S21,off}$ (f). All results for full load over the input and output voltage. Upper left: half-bridge configuration; lower right: full-bridge configuration.

B1 System analysis The phase-shift balancing operation for full-bridge configuration and the asymmetrical duty cycle balancing for half-bridge configuration have a substantial impact on the system behavior. As the converter is operated in the operating modes at full load, the resonant voltage is relatively large. This leads to a decrease of the resonant current in the freewheeling interval (phase-shift operation) as well as in the asymmetrical pulse-width modulation resulting in a low turn-off current and, potentially, in a loss of ZVS at full load. Figure 2.59a shows the commutation charge assuming the above-defined operating regions at full load. This is motivated by the analysis of the commutation charge over the output load depicted in Figure 2.59b showing that the commutation charge decreases for all critical operating points with increasing load. From Figure 2.59a, it is evident that the balancing operation results in a fairly low commutation charge for the half-bridge configuration. However, this can be countered by reducing the operating region to achieve a larger commutation charge. Overall three critical operating points can be identified: $OP_{HB,edge,FL}$, $OP_{FB,MC,FL}$, and $OP_{FB,Gmax,FL}$. In $OP_{HB,edge,FL}$, the commutation charge may be critically low resulting from the low switching frequency. In $OP_{FB,MC,FL}$, the phase-shift operating modes changes from an ACD-sequence to a CDE-sequence (sequences named in accordance with [Liu+16b]). At large switching frequencies on the left of $OP_{FB,MC,FL}$, the resonant voltage is not large enough to force the resonant current during the freewheeling interval onto the magnetizing current. For $OP_{FB,MC,FL}$ and larger output voltages, the resonant current is forced onto the magnetizing current. However, the lower switching frequency on the right of $OP_{FB,MC,FL}$ leads to larger magnetizing currents and therewith to a larger commutation charge. Finally, for large gains at $OP_{FB,Gmax,FL}$, the phase-shift modulation may enter the CDF-sequence where the resonant current drops below the magnetizing current, which may even result in a hard turn-on.

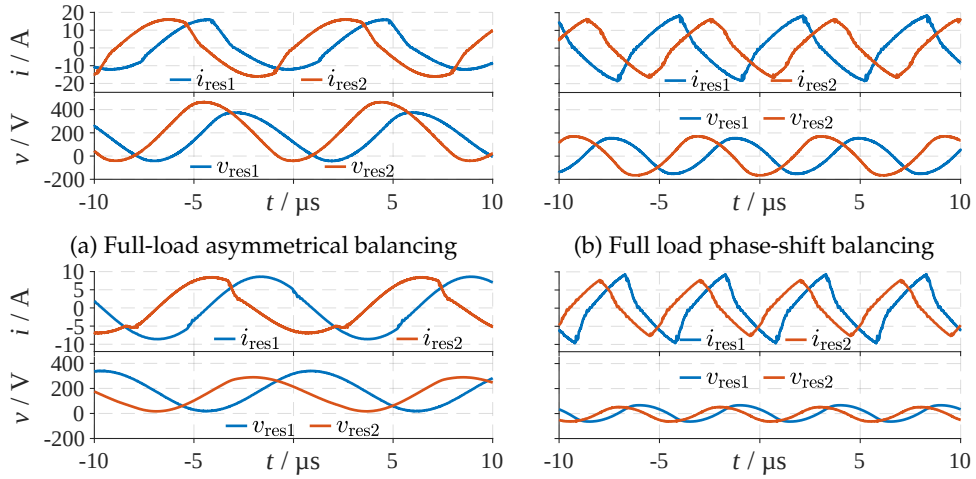
The following analysis assumes a reduced operating region for half-bridge configuration as indicated in Figure 2.59a to achieve a sufficient commutation charge for ZVS. Figures 2.60a and 2.60b show the rectifier currents of the rail operated

TABLE 2.6: Relevant operating points for the resonant tank design when employing phase-shift balancing in full-bridge configuration and asymmetrical PWM to balance the LLC in half-bridge configuration.

Name	Abbreviation	V_{in}	V_{out}	I_{out}	Mode
$OP_{HB,Gmin,FL}$	OP_1	420	8	260	HB
$OP_{HB,edge,FL}$	OP_2	420	*	*	HB
$OP_{FB,Gmax,FL}$	OP_3	420	16	228	FB
$OP_{FB,MC,FL}$	OP_4	240	*	260	FB
$OP_{FB,edge,FL}$	OP_5	420	*	*	FB
$OP_{FB,edge,LL}$	OP_6	420	*	20	FB
$OP_{FB,edge,PS}$	OP_7	420	*	*	PS
$OP_{HB,min,LL}$	OP_8	420	11	10	HB
$OP_{FB,max,DL}$	OP_9	200	16	100	FB

in phase-shift modulation / asymmetrical duty cycle modulation. As expected, in asymmetrical duty-cycle modulation the rectifier currents are very imbalanced. $OP_{HB,Gmin,FL}$ can be identified as the critical operating point to properly dimension the synchronous rectifier. Figures 2.60c and 2.60d show the output charge and maximum resonant current. The analysis shows that three operating points are critical to consider in the design procedure: $OP_{HB,Gmin,FL}$, $OP_{HB,edge,FL}$, and $OP_{FB,Gmax,FL}$.

The primary semiconductors need to be dimensioned for maximum losses. The RMS current is a measure of the conduction losses, whereas the combination of the switching frequency and the turn-off current is a measure of the switching losses. Figures 2.60e and 2.60f show the RMS current I_{S21} of the switch S_{21} with its respective turn-off current $i_{S21,off}$. The LLC shall employ silicon MOSFETs , which have comparably large switching losses. This means that $OP_{HB,Gmin,FL}$ or $OP_{FB,edge,FL}$ are most likely the operating points with the largest thermal stress of the semiconductors because the switching losses are dominant and there are large conduction losses. However, if semiconductors with low switching losses are employed (such as gallium-nitride (GaN) or SiC), $OP_{FB,Gmax,FL}$ or $OP_{HB,edge,FL}$ may be the operating points with the largest thermal stress as the conduction losses are maximum. All operating points are summarized in Table 2.6.



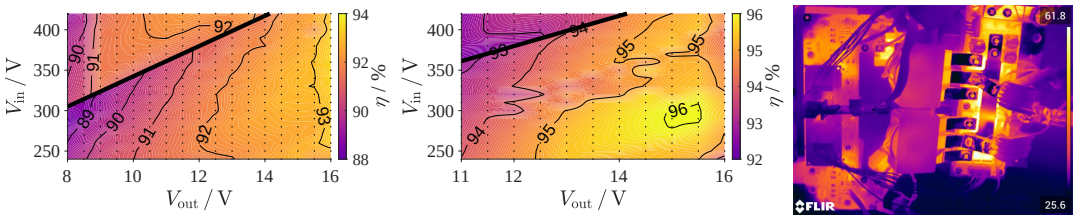
(a) Full-load asymmetrical balancing

(b) Full load phase-shift balancing

(c) Partial-load asymmetrical balancing

(d) Partial-load phase-shift balancing

FIGURE 2.61: Measurement results of the balanced LLC. (a) parameters: $\text{Config}_{2.1y}$, (b) parameters: $\text{Config}_{2.1z}$.



(a) $I_{out} = 260\,\text{A}$

(b) $P_{out} = 2.2\,\text{kW}$

(c) Thermal analysis in $\text{OP}_{\text{FB,FL}}$

FIGURE 2.62: (a,b): Measured dual-rail efficiency. Upper left: half-bridge configuration with asymmetrical duty cycle balancing, lower right: full-bridge configuration with phase-shift balancing. (c) thermal analysis of the converter in $\text{OP}_{\text{FB,FL}}$.

B2 Steady-state evaluation The interleaving method has been employed on an LLC, which is designed according to the design considerations proposed in [Reh+20b; RSB21]. The concept of the design is presented in Chapter 3. However, as this chapter describes a single-rail topology comparison method, the design of the dual-interleaved LLC will not be described in this thesis. For more information, please refer to [Reh+20b; RSB21].

Measurement results for the full-bridge configuration are depicted in Figure 2.61. For the full-load measurement results in Figure 2.61b, LLC_2 is operated with a phase shift of 55.4° for balancing the power transfer. Due to the full-bridge operation, there is no DC-component in the resonant capacitor voltage. Full load measurement results for the half-bridge configuration are shown in Figure 2.61a (left) where LLC_2 is the LLC that is operated with an asymmetrical duty cycle for balancing of the output currents. Due to the half-bridge operation, a DC-component offset of approximately $V_{in}/2$ in the resonant capacitor voltage is present, which is reduced for $v_{res,2}$ by the asymmetrical duty cycle operation by 45 V. The duty cycle is $D_{ls} = 0.6$ for the low-side switch and $D_{hs} = 0.4$ for the high-side switch.

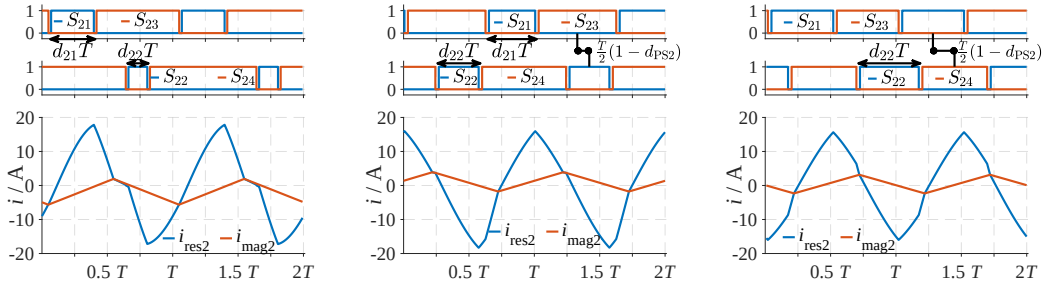
(a) Effective output capacitor current

(b) Normalized output capacitor charge

FIGURE 2.63: Comparison of (a) the effective output capacitor current I_{Cout} and (b) the normalized output capacitor charge $Q_{\mathrm{n,out}}$ for the presented balancing method and switching-frequency balancing (for optimized phase shift between the rails).

The converter efficiency is displayed in Figure 2.62. Figure 2.62a shows the full-load efficiency, while Figure 2.62b shows the light-load efficiency (both in balanced operation). During the balancing operation, the converter achieves a peak efficiency of approximately 96.5 %, while it reaches an efficiency above 90 % for almost all operating points. Only for output voltages below 10 V, the efficiency is below 90 %. The efficiencies were measured with a *HIOKI PW6001* power analyzer. A thermal analysis is depicted in Figure 2.62c. The measurement of the input and output current is conducted with the current probes *HIOKI CT6841* and *HIOKI CT6844* respectively. All losses include the EMI filter and the auxiliary power supply. The thermal limit of 90 °C is kept at all times. Neglecting the non-optimized input EMI-filter, the power density is 2.1 kW/l.

To evaluate the performance of the output ripple current cancellation, Figure 2.63a shows the simulated RMS current of the output capacitor I_{Cout} and Figure 2.63b shows the normalized output charge $Q_{\mathrm{n,out}}$ for the conventional power transfer balancing using the switching frequency (resulting in the described beat of i_{Cout}; cf. Figure 2.56) vs. phase-shift / asymmetrical duty cycle balancing (with optimized phase shift between rail 1 and 2). The utilized balancing operation reduces the worst-case RMS current by about 45 % and the output charge by about 60 %. The output ripple current cancellation is effective and small output capacitors can be selected.



(a) Asymmetrical morphing with asymmetrical duty cycles (used in *Morph-AsB*)

(b) Asymmetrical morphing with asymmetrical duty cycles and phase shift (used in *Morph-PSB-As* and *Morph-AsB-PS*)

(c) Morphing with phase shift (used in *Morph-PSB*)

FIGURE 2.64: Modulations used to achieve the balanced on-the-fly topology transition from full-bridge to half-bridge modulation and reverse.

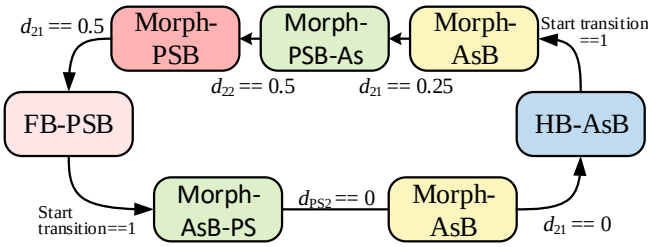


FIGURE 2.65: State diagram for the balanced morphing transition employing multiple LLC rails.

C Balanced topology morphing

In 2.1.5B it has been suggested to employ phase-shift balancing when operating in full-bridge configuration and asymmetrical balancing when employing half-bridge modulation. During operation, it is necessary to achieve a balanced morphing transition when switching from one operating mode to the other to avoid over voltages at the resonant capacitor or over currents in the resonant inductor. For that purpose, this section proposes a balanced on-the-fly morphing transition when switching between these balanced operating modes.

In Section 2.1.2C, it was shown that by employing LLC converters with a comparably large magnetizing inductance, the dynamic flux overshoot during the morphing process can be largely reduced. Therefore, it may not be necessary to utilize the modification of the positive inverter voltage pulse length, meaning that this pulse length is a degree of freedom when transitioning from full-bridge configuration to half-bridge configuration for such configurations. For the multi-rail transition, this parameter can, thus, be modified to achieve a balanced morphing transition.

To achieve the balanced transition, it is suggested to employ three further modes of operation, which are depicted in Figure 2.64. These are[1]:

[1] in the following analysis, it is assumed that without balancing, LLC_2 (S_{21}-S_{24}) transfers more power requiring a balancing modulation. LLC_1 is further operated with the conventional morphing modulation (see Section 2.1.2A). It is further assumed that the converter transitions from full-bridge modulation to half-bridge modulation and reverse. However, the description is equally valid when employing the frequency-doubler modulation since the same voltage levels can be achieved.

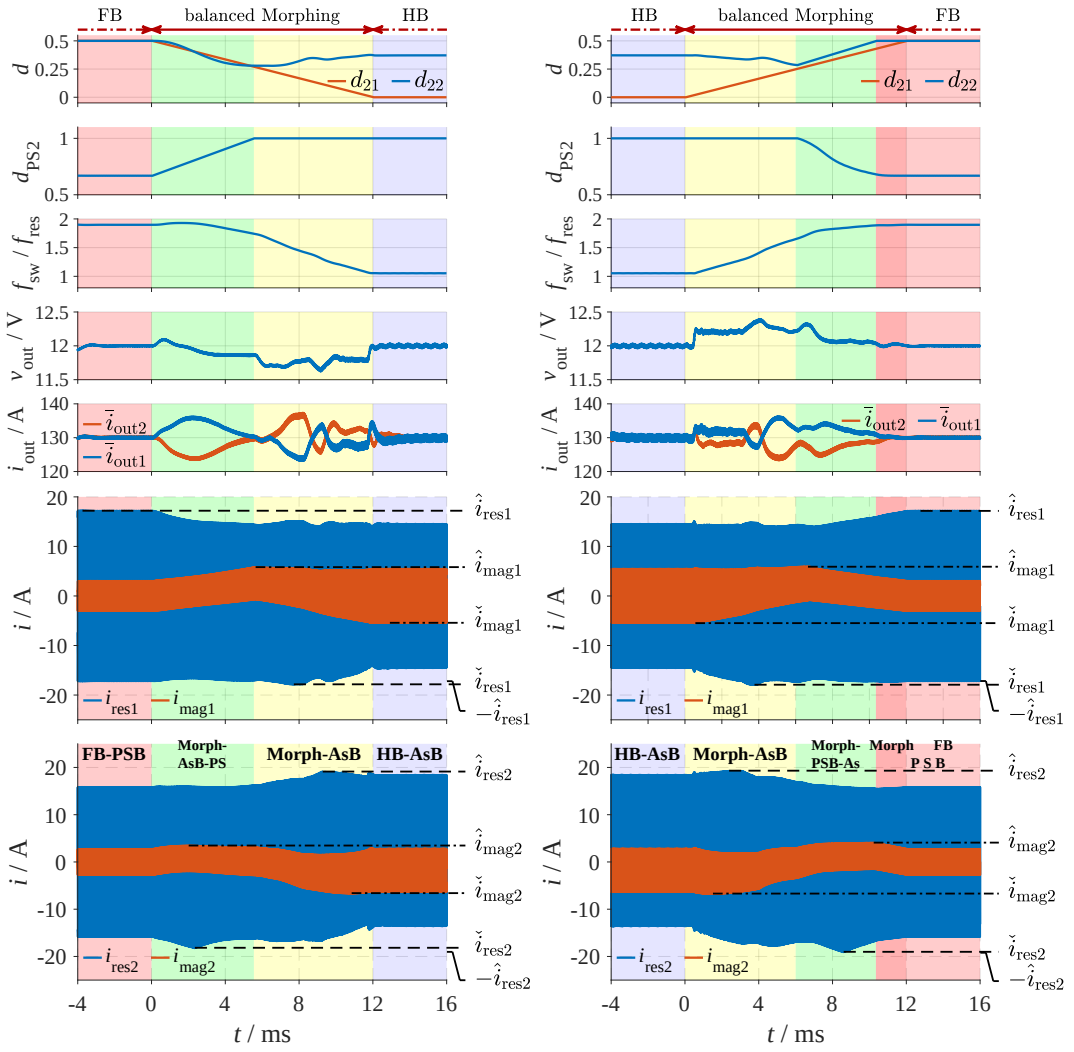
1. ***Asymmetrical morphing with asymmetrical duty cycles*** (cf. Figure 2.64a):
   The modulation has asymmetrical pulse widths for both bridge legs ($d_{21}, d_{22} < 0.5$). The turn-on of S_{21} is centered between the turn-on of switch S_{24}.
2. ***Asymmetrical morphing with asymmetrical duty cycles and phase shift*** (cf. Figure 2.64b):
   The modulation has asymmetrical pulse widths for both bridge legs ($d_{21}, d_{22} < 0.5$). In contrast to 1, the modulation also has a phase shift, such that the center of the turn-on pulse of S_{24} is phase-shifted to the center of the turn-on pulse of S_{21}.
3. ***Morphing with phase shift*** (cf. Figure 2.64c):
   The modulation has no asymmetrical duty cycles for the bridge leg S_{21}-S_{23}. However, there is an asymmetrical duty cycle for the morphing bridge leg (S_{22}-S_{24}). Furthermore, there is a phase shift between the center of the turn-on pulse of S_{24} and the center of the turn-on pulse of S_{21}.

During the transition, the LLCs can be balanced either using an asymmetrical duty cycle d_{21} (*asymmetrical balancing*, AsB) or through a phase-shift (*phase-shift balancing*, PSB). The balanced transition is achieved through four different states corresponding with the three different operating modes depicted in Figure 2.64. The state machine of the different operating modes during the transition from full-bridge configuration with phase-shift balancing to half-bridge configuration with asymmetrical balancing and reverse is depicted in Figure 2.65.

At the start of the transition from full-bridge configuration to half-bridge configuration, the duty cylce d_{21} is slowly reduced from 0.5 to 0. The converter at first enters the morphing state *asymmetrical balancing with phase shift* (Morph-AsB-PS, cf. Figure 2.65; modulation depicted in Figure 2.64b). The rails are immediately balanced with an asymmetrical duty cycle where the phase shift of the balanced rail is linearly reduced from its current state to zero. When the phase shift is zero, the converter enters the morphing state *asymmetrical balancing* (Morph-AsB, cf. Figure 2.65; modulation depicted in Figure 2.64a). The rails are further balanced with an asymmetrical duty cycle with no phase shift. When the duty cycle d_{21} finally reaches zero, the balanced converter operates in half-bridge configuration with asymmetrical balancing.

During the transition from half-bridge configuration to full-bridge configuration, the duty cycle d_{21} is slowly increased from 0 to 0.5. The converter at first enters the morphing state *asymmetrical balancing* (Morph-AsB, cf. Figure 2.65; modulation depicted in Figure 2.64a). When the duty cycle d_{21} reaches a certain threshold (here, $d_{21} = 0.25$), the converter enters the morphing state *phase-shift balancing with asymmetrical duty cycles* (Morph-PSB-As, cf. Figure 2.65; modulation depicted in Figure 2.64b). From the modulation perspective, this state is the same as the state *asymmetrical balancing with phase shift* (Morph-AsB-PS). However, the rails are now balanced with the phase shift of LLC_2. During this state, the asymmetrical duty cycle d_{22} is slowly increased. When this duty cycle finally reaches $d_{22} = 0.5$, the converter enters the morphing state *balancing with phase shift* (Morph-PSB, cf. Figure 2.65; modulation depicted in Figure 2.64c). Finally, when d_{21} reaches $d_{21} = 0.5$, the converter is operating in full-bridge configuration and the rails are balanced with the phase shift.

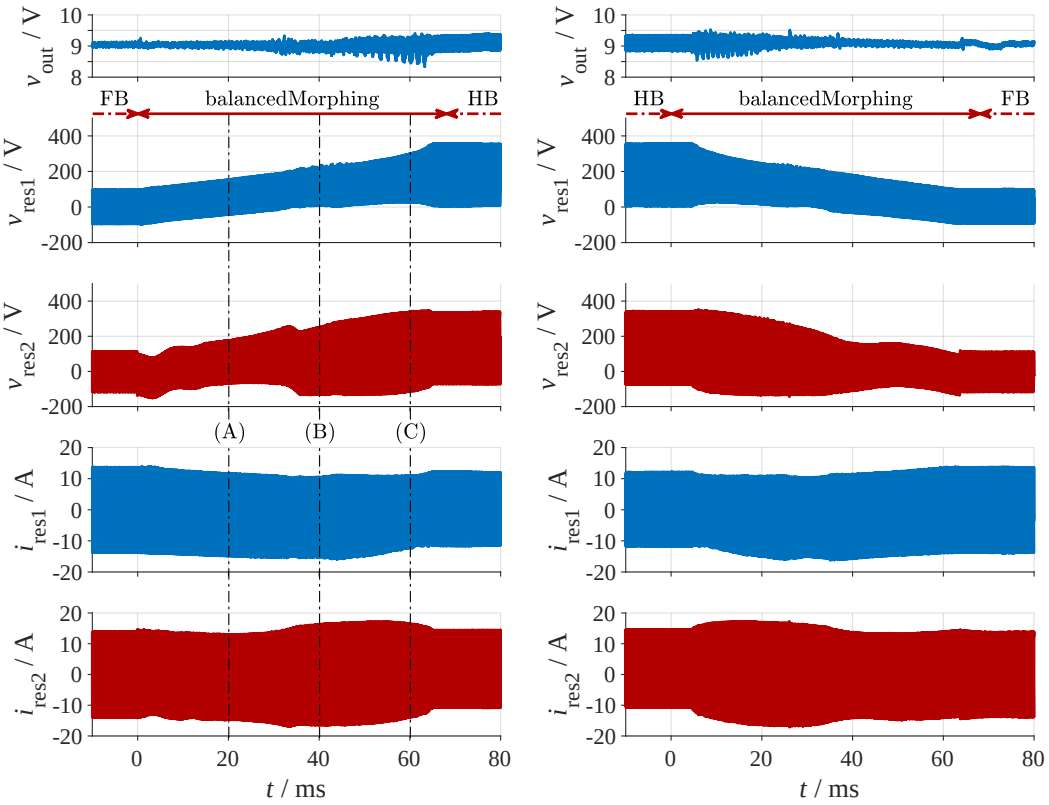
An exemplary simulated transition is depicted in Figure 2.66. The morphing states are colored according to the state diagram in Figure 2.65. The depicted output currents are filtered with a low pass filter at a cut-off frequency of $\omega = 10\,\text{kHz}$.



(a) FBM to HBM transition (b) HBM to FBM transition

FIGURE 2.66: Simulated balanced morphing transition from full-bridge to half-bridge configuration and reverse showing the balanced rail's duty cycles d_{21}, d_{22} and phase shift d_{PS2}, the switching frequency f_{sw}/f_{res}, output voltage v_{out} and resonant and magnetizing currents for both rails (parameters: Config$_{2.1aa}$).

The diagram depicts the primary morphing duty cycle d_{21} as a reference for the morphing transition. Furthermore, the output voltage v_{out}, the normalized switching frequency f_{sw}/f_{res} (where f_{res} is nominal resonant frequency), and the resonant and magnetizing currents of both rails are depicted. The morphing time is set to $t_{morph} = 12\,\text{ms}$. Figure 2.66a depicts the transition from full-bridge to half-bridge configuration, while Figure 2.66b shows the transition from half-bridge configuration to full-bridge configuration. In the transition from full-bridge to half-bridge configuration (Figure 2.66a), the linear increase of the phase shift is well visible in the green area while the duty cycle d_{22} is modified for the balanced power transfer. On the other side, the linearly increasing duty cycle d_{22} is also visible in the green area in the transition from half-bridge to full-bridge configuration. The transition shows that the dynamic magnetizing current increase is well limited, barely surpassing the respective maximum in half-bridge configuration. The resonant current also increases for the balanced rail dynamically over its respective full-bridge



(a) FBM to FDM morphing

(b) FDM to FBM transition

FIGURE 2.67: Experimental measurement results for the balanced morphing transition from full-bridge to frequency-doubler modulation and reverse (parameters: $\text{Config}_{2.1ab}$).

maximum. The output voltage deviation is limited to below 0.5 V.

The balanced morphing transition was employed and tested on the LLC resonant converter depicted in Figure 3.23a. Experimental measurement results are depicted in Figure 2.67. During the implementation it became apparent that the morphing of both rails results in substantial EMI noise disturbing the measurement of the input current (employed as an external analogue-digital converter (ADC), galvanically isolated from the DSP through an isolated serial peripheral interface (SPI)). To ensure a proper measurement of the input current, it was necessary to employ a Σ-Δ modulator [Tex03] for an isolated galvanical transfer of the shunt voltage to the DSP, which was then measured with the DSP ADCs. Furthermore, it proved beneficial to employ the frequency-doubler and alternating-asymmetrical phase-shift equivalent modulations of Figure 2.64. The implementation of a varying frequency, varying duty cycle for both rails as well as a center-based phase-shift between the rails is otherwise particularly difficult in the employed DSP [Tex01] as the built-in phase-shift functionality of the PWM is implemented as a counter pre-load (loaded at the start of each period for the slave PWM), which can result in pulse skipping if the pre-load is similar to the compare register value. For the frequency-doubler and alternating asymmetrical duty cycle implementation, the PWMs of both rails can run in phase such that no use of the built-in phase shift is required. Since both morphing modulations result in equal inverter voltages, the description of this modulation is omitted for the sake of brevity. The transition in Figure 2.67 shows that the balanced morphing transition was successfully achieved. However, an overshoot in

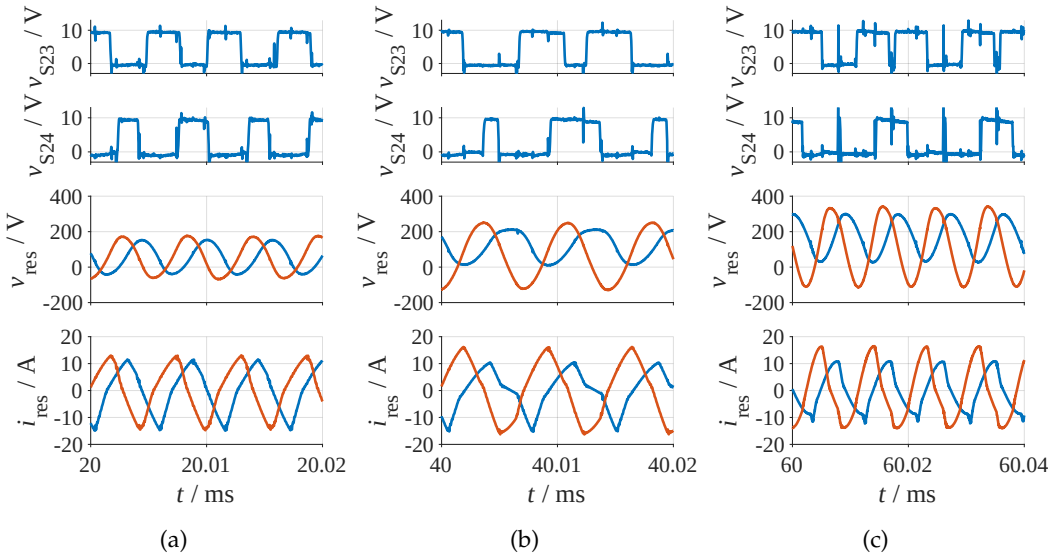


FIGURE 2.68: Close-ups of the intervals depicted in Figure 2.67a.

the resonant currents and a slight overshoot of the resonant capacitor voltage can be noticed.

Measurement results for the intervals depicted in Figure 2.67a are shown in Figure 2.68. From the pulse pattern of the low-side switches S_{23} and S_{24}, it is evident that the full-bridge to frequency doubler transition was tested. Furthermore, the resonant capacitor voltages and currents indicate that the balanced transition is not yet fully ideal since dynamically, the resonant current i_{res2} is still larger compared to i_{res1}. However, the increase is relatively small with only about 15 % compared to the steady state operation of FBM or FD-HBM, which can be considered tolerable. Additionally, the resonant capacitor voltage shows no significant increase during the morphing.

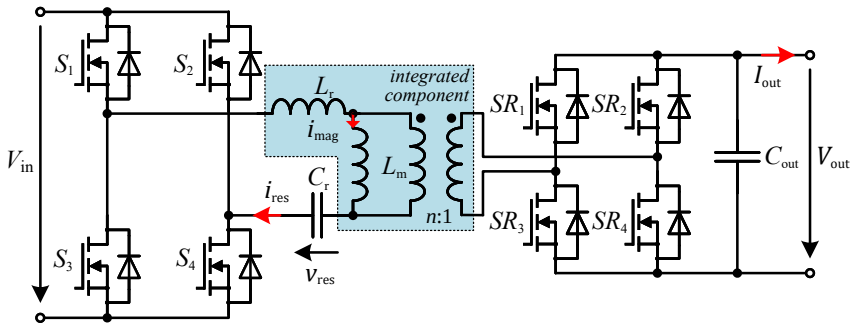


FIGURE 2.69: LLC resonant converter with full-bridge rectifier where the resonant inductance L_r and the magnetizing inductance L_m are integrated into one single magnetic component.

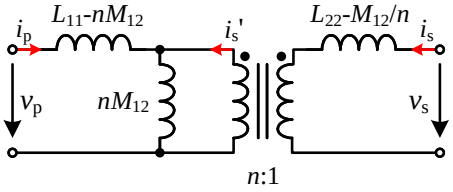
2.1.6 Secondary-Side Resonant Inductance Integration

this section has been previously published in parts in [Reh+22b] *and the presented method has been applied for patent in* [RSB22c].

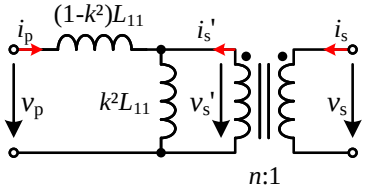
Typically, the LLC uses separate magnetic components for the resonant inductance and the transformer. While the literature describes methods to integrate both into one single component, these methods usually require litz wire for both the primary and secondary winding. For applications with a low-voltage, high-current output, these methods, however, cannot be employed as the secondary winding is conventionally constructed as a single turn, which is hardly possible with litz wire. For these applications, this section proposes an integrated planar transformer where single-turn copper sheets are employed on the secondary side. In an integrated transformer, the transformer and the resonant inductor are combined in one single component. The integrated stray inductance is achieved through an additional ferrite leg on the secondary side. By using interleaving of the primary and secondary windings, proximity losses are mitigated to a large extent. This section discusses realization options and design implications for the transformer. Finally, a prototype is developed achieving a maximum efficiency of about 96 %.

A Introduction and state of the art

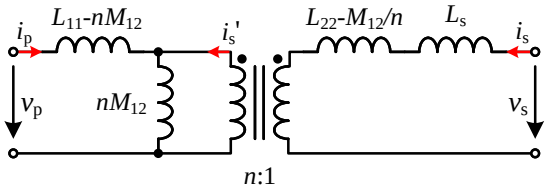
In the past, a variety of different methods have been presented for an integrated transformer. One of the most common methods to adjust the stray inductance of a transformer is to alter the distance between the primary and secondary winding [Cho07; He+19; Jun13; Liu+16a; Mu+15; Zou+18; PS15; SGM20]. However, this results in large fringing field that drastically increases the winding losses [KSB19]. To further increase the stray inductance and guide the magnetic flux between the windings, a ferrite piece (sometimes called *magnetic shunt*) can be placed between the windings [ADF20; Har+13; KSB19; Keu+19; Li+15; LOA18; LOA19; SAS08]. While [ADF20; Har+13; LOA18; LOA19; SAS08] employ methods where the primary and secondary windings were separated by the ferrite stray path, [Li+15; Keu+19; KSB19] shows that a partial interleaving of the primary and secondary winding is possible. In [FLL17; Liu+20; Wan+19], a matrix transformer is employed consisting of four ferrite legs with a shared top and bottom plate. The ferrite legs are hereby beneficially placed in a square pattern to reduce the flux density inside the core in the top and bottom plate. In [GZ21; Wan+20; YQL03], a three-leg transformer is used, where the turn-ratios are chosen to achieve the desired inductance values.



(a) T-type equivalent circuit with arbitrary conversion ratio n



(b) T-type equivalent circuit with primary-side-concentrated stray inductance



(c) T-type equivalent circuit with additional secondary inductance L_s and arbitrary conversion ratio n

FIGURE 2.70: Inductance models of the transformer, (a,b) conventional inductance models; (c) inductance model with additional external secondary inductance L_s.

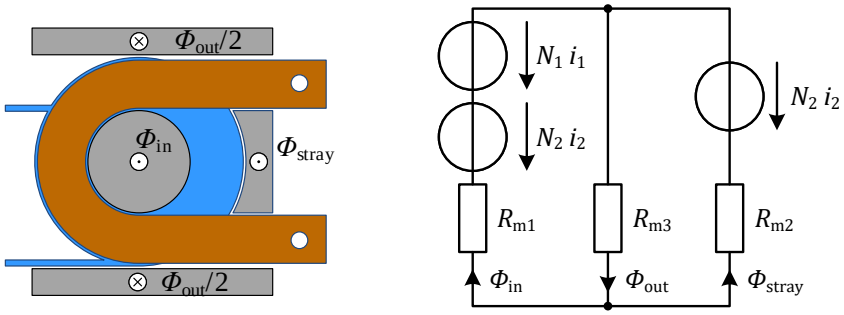
Similarly in [HJL14; CY18], the ferrite leg number is reduced to two by employing "*8*-shaped" windings. In [Lin+19a; ZHX21], a satellite-type structure with a center and several outer ferrite legs is used, where the outer and/or inner ferrite legs are wound with litz wire. A benefit of this structure is that the *satellite* legs allow a primary-series-secondary-parallel converter structure. In [LLL19; YCL02], three-leg ferrite structures are presented where the windings were placed on only two ferrite legs. In [Zha+07; Esc+21], the transformer and resonant inductor are merged into one core where the resonant inductor is placed on top of the transformer such that only a piece of ferrite was shared by both components. Finally, three-chambered solutions are presented in [Blo98; Yan+22], where [Yan+22] shows that a beneficial interleaving can be employed to reduce the external magnetic field.

Many of the above-mentioned methods are only applicable, if both the primary *and* secondary winding have a certain minimum number of turns. For high-current and low-output voltage transformers, the secondary turn number is usually only one such that the above introduced methods that allow the beneficial interleaving of the primary and secondary winding cannot be applied. For that purpose, this section proposes an integrated transformer for high-current low-voltage gain applications by utilizing a stray path on the secondary side.

Any two-winding transformer can be electrically modeled by the self inductances L_{11} and L_{22} of primary and secondary, and the mutual inductance M_{12}.

$$\begin{pmatrix} v_p \\ v_s \end{pmatrix} = \overbrace{\begin{pmatrix} L_{11} & M_{12} \\ M_{12} & L_{22} \end{pmatrix}}^{\boldsymbol{L}} \frac{\mathrm{d}}{\mathrm{d}t} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \tag{2.40}$$

The behavior can be modeled by the T-type equivalent circuit depicted in Figure 2.70a. The conversion ratio n of the ideal transformer of the electrical circuit diagram (ECD) of Figure 2.70 is not necessarily equal to the turns ratio N_1/N_2 of the real transformer but can be chosen freely, since the parameters of the ECD are



(a) Simplified view from the top side on the core design without the top and bottom plate

(b) Equivalent reluctance model

FIGURE 2.71: Concept of the integrated transformer. (a) the core consists of four legs, the inner leg with the flux ϕ_{in}, the stray leg with the flux ϕ_{stray} and the outer legs with the flux ϕ_{out}. The secondary winding (depicted in brown) may have several turns. Here, only one turn is shown. The equivalent reluctance model of the core is depicted in (b).

under-determined [Alb17]. By selecting n to fulfill the condition $L_{22} = M_{12}/n$, the system can be modeled by the primary-side-concentrated stray inductance model depicted in Figure 2.70b where k is the coupling coefficient, which corresponds with the magnetic components of the LLC resonant tank displayed in Figure 2.69. The resonant inductance corresponds with the primary-side concentrated stray inductance $L_{\text{r}} = (1-k^2)L_{11}$ and the magnetizing inductance $L_{\text{m}} = k^2 L_{11}$. If an external inductor L_{s} is placed on the secondary side as depicted in the model in Figure 2.70c, the transformer can be modeled with the primary-side-concentrated T-type model by fulfilling the condition

$$L_{22} - \frac{M_{12}}{n} + L_{\text{s}} \stackrel{!}{=} 0 \tag{2.41}$$

such that the conversion ratio n can be set to

$$n = \frac{M_{12}}{L_{22} + L_{\text{s}}}. \tag{2.42}$$

B Realization of the integrated transformer

The integrated transformer shall be achieved by employing a four-leg transformer core as depicted in Figure 2.71a. By employing such a planar core structure, the transformer can be manufactured easily and with low costs. Furthermore, the structure offers the possibility to include the primary windings directly in the PCB. The reluctance model of this core structure can be described by

$$\begin{aligned} N_1 i_1 + N_2 i_2 - \phi_{\text{in}} R_{\text{m1}} &= \phi_{\text{out}} R_{\text{m3}} \\ N_2 i_2 - \phi_{\text{stray}} R_{\text{m2}} &= \phi_{\text{out}} R_{\text{m3}} \\ \phi_{\text{in}} + \phi_{\text{stray}} &= \phi_{\text{out}}, \end{aligned} \tag{2.43}$$

which can be simplified to

$$\begin{aligned}&\overbrace{\begin{pmatrix} R_{\mathrm{m1}}+R_{\mathrm{m3}} & R_{\mathrm{m3}} \\ R_{\mathrm{m3}} & R_{\mathrm{m2}}+R_{\mathrm{m3}} \end{pmatrix}}^{\boldsymbol{R}_{\mathrm{m}}} \begin{pmatrix} \phi_{\mathrm{in}} \\ \phi_{\mathrm{stray}} \end{pmatrix} \\ &= \overbrace{\begin{pmatrix} N_1 & N_2 \\ 0 & N_2 \end{pmatrix}}^{\boldsymbol{N}} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix}.\end{aligned} \tag{2.44}$$

To achieve the required resonant and magnetizing inductance, the inductance matrix needs to fulfill the condition

$$\boldsymbol{L} = \begin{pmatrix} L_{11} & M_{12} \\ M_{12} & L_{22} \end{pmatrix} \stackrel{!}{=} \begin{pmatrix} L_{\mathrm{r}}+L_{\mathrm{m}} & \frac{L_{\mathrm{m}}}{n} \\ \frac{L_{\mathrm{m}}}{n} & \frac{L_{\mathrm{m}}}{n^2} \end{pmatrix}. \tag{2.45}$$

Therefore, the reluctance matrix needs to fulfill the condition

$$\begin{aligned}\boldsymbol{R}_{\mathbf{m}} &= \begin{pmatrix} r_{\mathrm{m},1,1} & r_{\mathrm{m},1,2} \\ r_{\mathrm{m},2,1} & r_{\mathrm{m},2,2} \end{pmatrix} \\ &= \begin{pmatrix} R_{\mathrm{m1}}+R_{\mathrm{m3}} & R_{\mathrm{m3}} \\ R_{\mathrm{m3}} & R_{\mathrm{m2}}+R_{\mathrm{m3}} \end{pmatrix} \stackrel{!}{=} \boldsymbol{N}\boldsymbol{L}^{-1}\boldsymbol{N}^{\mathrm{T}}.\end{aligned} \tag{2.46}$$

to achieve the desired inductance values.

B1 Realization options The reluctance matrix can be calculated and simplifed according to the definition in (2.46). According to the reluctance matrix definition (2.46), three conditions need to be fulfilled

1. $R_{\mathrm{m1}} \geq 0$:

$$\begin{aligned}&r_{\mathrm{m},1,1} - r_{\mathrm{m},1,2} \geq 0 \\ &= N_1 - N_2 n \geq 0 \\ &\rightarrow \tfrac{N_1}{N_2} \geq n,\end{aligned} \tag{2.47}$$

2. $R_{\mathrm{m2}} \geq 0$:

$$\begin{aligned}&r_{\mathrm{m},2,2} - r_{\mathrm{m},1,2} \geq 0 \\ &= \tfrac{N_1 N_2 n}{L_{\mathrm{r}}} \geq 0,\end{aligned} \tag{2.48}$$

3. $R_{\mathrm{m3}} \geq 0$:

$$\begin{aligned}&r_{\mathrm{m},1,2} \geq 0 \\ &= \tfrac{N_2 n^2 (L_{\mathrm{m}}+L_{\mathrm{r}})}{L_{\mathrm{m}}} - N_1 n \quad \geq 0 \\ &\rightarrow \tfrac{N_1}{N_2} \leq n \tfrac{L_{\mathrm{m}}+L_{\mathrm{r}}}{L_{\mathrm{m}}}.\end{aligned} \tag{2.49}$$

Therefore, the two boundaries for N_1 are defined by (2.47) and (2.49) as

$$\frac{N_1}{N_2} \in \left[n, \frac{n\ (L_m + L_r)}{L_m} \right] = [n, (1+\lambda)n] \tag{2.50}$$

In this range, the turns ratio $\frac{N_1}{N_2}$ can be chosen arbitrarily. The case $N_1 = N_2 n(1+\lambda)$ hereby corresponds to an ideal transformer without any stray flux where the magnetizing inductance L_{m} is connected to an inductor on the secondary side. Due to the high-current low-output voltage application that is investigated in this thesis, it is assumed that $N_2 = 1 \rightarrow \frac{N_1}{N_2} = N_1$.

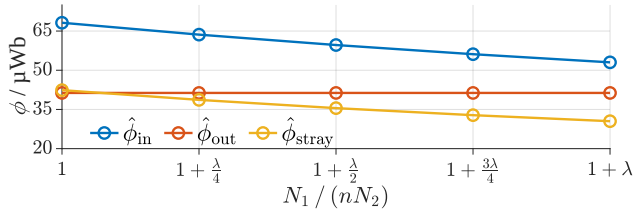


FIGURE 2.72: Quantitative analysis of the turns ratio on the transformer flux. It is evident that there is almost 29 % more flux for ϕ_{in} and approximately 39 % more flux for ϕ_{stray}, if the turns ratio is set equal to the conversion ratio n compared to the case where $\frac{N_1}{N_2} = (1+\lambda)n$ (parameters: Config$_{2.1ac}$).

The choice of the turns ratio $\frac{N_1}{N_2}$ highly influences the flux distribution in the core. The flux in the outside portion of the core always remains the same. However, $\frac{N_1}{N_2}$ influences the flux distribution in the center core and the stray path. Figure 2.72 shows the dependency of the maximum flux on the number of primary turns. It is evident that the maximum center flux $\hat{\phi}_{\text{in}}$ increases by about 29 % compared to an increase of 39 % for the stray flux $\hat{\phi}_{\text{stray}}$ if the turns ratio $\frac{N_1}{N_2}$ is chosen equal to the conversion ratio n compared to the case where the turns ratio is selected $\frac{N_1}{N_2} = (1+\lambda)n$. The maximum flux in the outer leg $\hat{\phi}_{\text{out}}$ hereby remains the same for any turn number and corresponds to the flux of a conventional transformer. If an air gap in the outer leg shall be avoided ($R_{\text{m3}} \approx 0$), it should be noted that either the inductance ratio $\lambda = \frac{L_{\text{r}}}{L_{\text{m}}}$ or the conversion ratio n cannot be selected completely arbitrarily since N_1 and N_2 are integers. If the conversion ratio n is fixed, the inductance ratio λ needs to be selected in the range

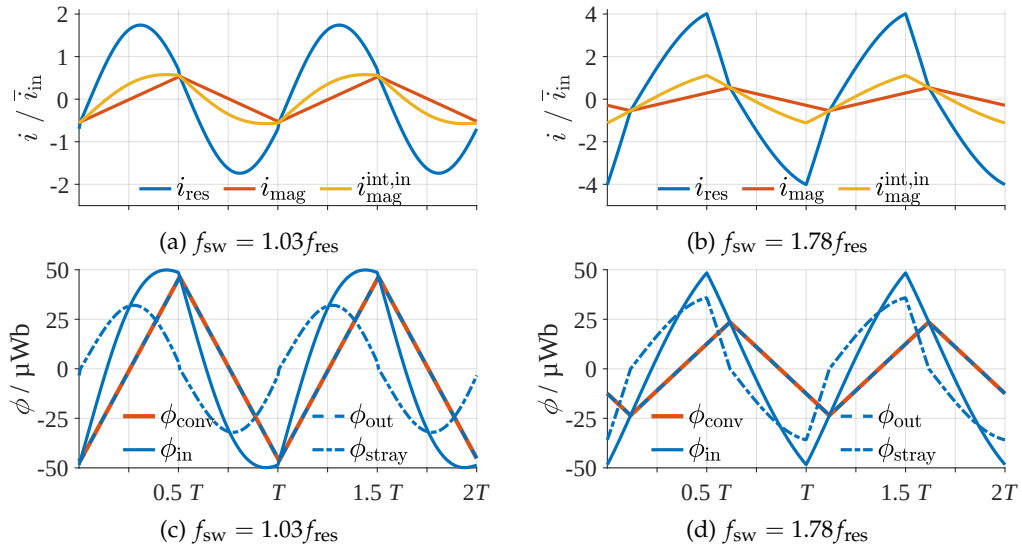
$$\lambda = \frac{N_1}{nN_2} - 1 \tag{2.51}$$

where N_1 is arbitrary. If, on the other hand, the inductance ratio λ is predefined, the conversion ratio n must be selected as

$$n = \frac{N_1}{N_2(1+\lambda)}. \tag{2.52}$$

These constraints must be considered in the design of the resonant tank. However, especially for large conversion ratios, the impact on the design is limited since small variations of the conversion ratio cannot really be avoided due to the large impact of any stray inductance in the connection. Since fringing fields should be avoided outside the transformer, it is assumed that $R_{\text{m3}} \approx 0$ in the following.

B2 Flux shape and implications on the operating field The integrated core structure has a major impact on the flux shape and distribution. Where for the conventional transformer, the transformer flux ϕ_{conv} is proportional to the magnetizing current i_{mag} ($\phi_{\text{conv}}(t) = \frac{L_{\text{m}} i_{\text{mag}}(t)}{N_1}$, [Alb17]), this relation is not valid for the presented solution. While the flux in the stray path ϕ_{stray} is proportional to the secondary current i_{sec} and thus increases primarily with the load current, the flux in the center core cannot be calculated based on the magnetizing current alone. The flux in the center core ϕ_{in} can be calculated as



(a) $f_{sw} = 1.03 f_{res}$ (b) $f_{sw} = 1.78 f_{res}$

(c) $f_{sw} = 1.03 f_{res}$ (d) $f_{sw} = 1.78 f_{res}$

FIGURE 2.73: (a,c) Shape of the flux vs. time for a near-resonant operation (parameters: Config$_{2.1ae}$) and (b,d) over-resonant operation (parameters: Config$_{2.1ad}$). For the resonant operation, the maximum inner transformer flux ϕ_{in} is similar to the conventional flux ϕ_{conv}. However, for an over-resonant operation, the inner transformer flux ϕ_{in} is almost twice the conventional flux ϕ_{conv}.

$$\phi_{in}(t) = \frac{(L_m + L_r)\left[i_{res}(t) - \frac{N_2}{N_1} i_{sec}(t)\right]}{N_1} \tag{2.53}$$

which can be rewritten to

$$\phi_{in}(t) = \frac{L_m(1+\lambda)\left(i_{res}(t) - \frac{1}{n(1+\lambda)} i_{sec}(t)\right)}{N_2 n(1+\lambda)}. \tag{2.54}$$

With the equation of the magnetizing current ($i_{mag} = i_{res} - \frac{1}{n} i_{sec}$) (Figure 2.69), the equation simplifies to

$$\phi_{in}(t) = \frac{L_m\left[i_{mag}(t) + \lambda i_{res}(t)\right]}{N_2 n(1+\lambda)} \tag{2.55}$$

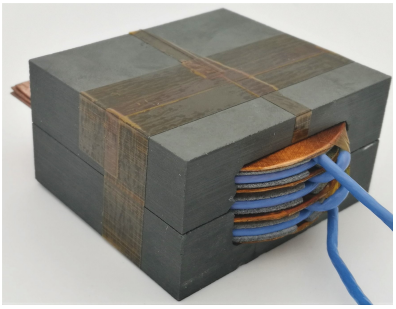
such that, an equivalent magnetizing current $i_{mag}^{int,in}$ can be deduced as

$$i_{mag}^{int,in}(t) = (1+\lambda) i_{res}(t) - \frac{i_{sec}(t)}{n} = i_{mag}(t) + \lambda i_{res}(t), \tag{2.56}$$

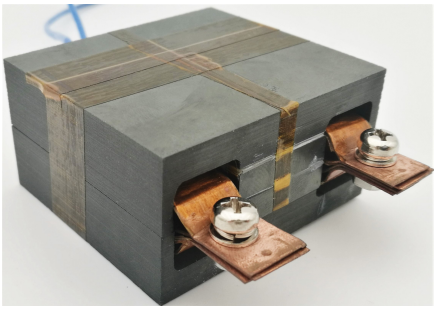
to easily analyze the implications with electric circuit simulations. With (2.56), the inner flux ϕ_{in} can be calculated as

$$\phi_{in}(t) = \frac{L_m i_{mag}^{int,in}(t)}{N_1}. \tag{2.57}$$

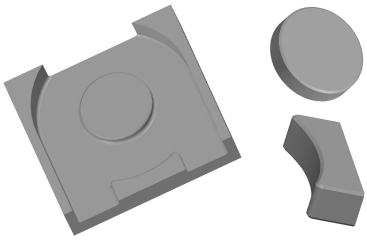
Both equations (2.55) and (2.56) emphasize the impact of the resonant current on



(a) Front with primary windings



(b) Back with stray path and secondary windings



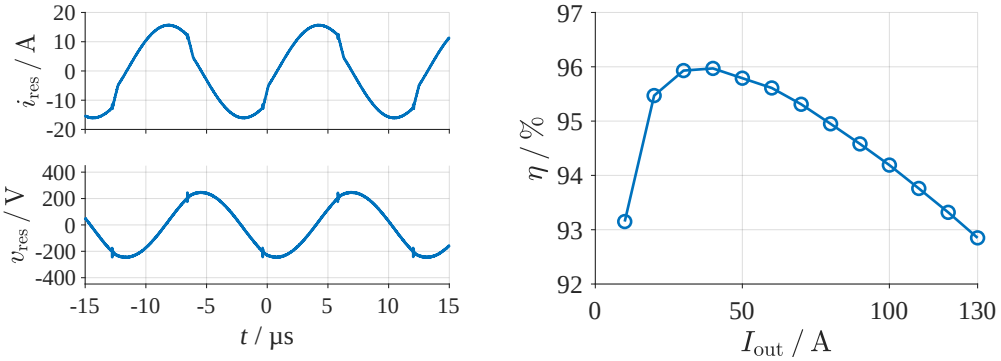
(c) Construction drawing of the transformer base, stray tablet and center tablet

FIGURE 2.74: Manufactured experimental prototype of an integrated transformer. Dimensions of the ferrite body (width×lengths×height): 57 mm×51 mm×30 mm.

the inner transformer flux ϕ_{in}. The impact of the portion of the resonant current i_{res} on the flux must be considered in operation and design. For resonant operation, the time instance where the magnetizing current is maximum does not correspond with the time instance where the resonant current is maximum (cf. Figure 2.73a, 2.73c). However, for operating frequencies much larger than the resonant frequency, the time instances where the magnetizing and resonant current have their respective maximum are much closer together, resulting in a much larger inner transformer flux ϕ_{in} compared to the conventional case ϕ_{conv} (cf. 2.73b, 2.73d). The maximum inner transformer flux ϕ_{in} is similar for the resonant and over-resonant case (cf. Figure 2.73a-2.73d) and most likely does not result in a saturation of the transformer core. However, the increased over-resonant flux does result in much larger losses in the windings compared to the conventional transformer as the larger magnetic field intensity of the fringing fields increases the proximity losses. Therefore, this type of transformer is best used for a resonant operation like in a two-stage converter. In two-stage applications where the converter is operated in resonance like [LJH11; Rue+20; USB20b], the impact on the winding losses are low, making such an integrated solution attractive. If, however, the integrated transformer is employed in applications where a full-power low-gain operation is required, the increased winding losses must be considered in the design of the windings.

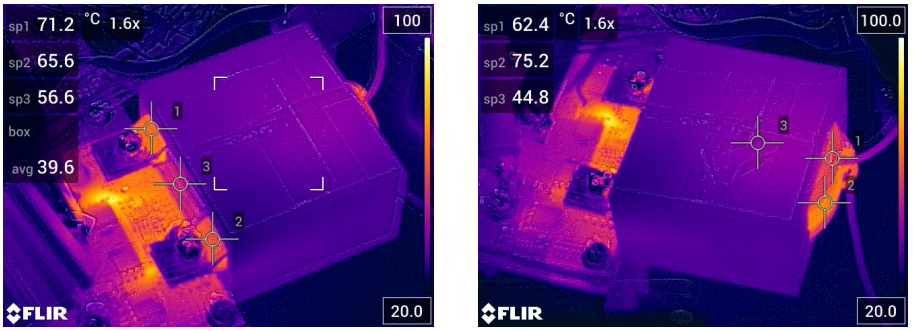
C Verification

Based on the above analysis, the integrated transformer was build up. It is assumed that the application is an LLC that is operated near resonance, with a limited operation range $f_{\text{max}}/f_{\text{res}} \leq 1.2$. The core cross section is designed to achieve the same flux at the maximum operating frequency compared to a conventional transformer with resonant inductor that act as a benchmark. The manufactured transformer is



(a) Current and voltage shapes

(b) Measured efficiency



(c) Thermal analysis (front)

(d) Thermal analysis (back)

FIGURE 2.75: Thermal analysis of the transformer under full load (c,d). The maximum measured temperature is about 75 °C (the secondary PCB is hotter caused by the heating of the high-side drivers); (a) measured current and voltage shapes and (b) efficiency (parameters: $\text{Config}_{2.1af}$). (c,d) thermal analysis of the transformer.

visualized in Figure 2.74.

TABLE 2.7: Measured parameters of the integrated transformer

L_r / µH	38.3
L_m / µH	128.1
n	14.6

The transformer has $N_1 = 18$ primary turns and $N_2 = 1$ secondary turn. The reluctances R_{m1} and R_{m2} are achieved with three air gaps for the center and stray leg. The measured parameters are given in Table 2.7.

The transformer has been put in operation and tested under different load conditions in an operating point near resonance. The resonant capacitance is $C_r = 120$ nF. Figure 2.75c and 2.75d show a thermal measurement of the transformer after 15 min of operation. The transformer itself remains relatively cool with a maximum temperature of 75°C at the windings. The PCB heats up in the proximity of the stray path, which is caused by the fringing field of the air gaps as well as by the heating of the drivers. To reduce the PCB temperature, the board is connected via a copper inlay to the heatsink. The copper inlay is electrically isolated to the PCB and heatsink with a TIM foil. Efficiency measurements are depicted in Figure 2.75b. The transformer was operated with an inverter employing SiC-MOSFETs . The setup reaches

a maximum efficiency of almost 96 % and a full-load efficiency of 92.8 %. An exemplary operation is depicted in Figure 2.75a. The operation shows relatively small oscillations at the switching instants resulting from the high resonant frequency of the integrated resonant inductance.

D Conclusion

The LLC resonant tank requires a resonant and magnetizing inductance. While these are typically representing different components – the resonant inductor and the transformer, this section proposed an integrated component to unite the functionality of both. The proposed planar setup utilizes an additional ferrite leg for the stray path, which can be easily integrated into the ferrite core of the transformer. The section showed that due to the high-current application, a single secondary turn is sufficient to achieve the required stray inductance, which can be assembled using copper sheets. Therefore, the solution presents an easy and cheap alternative to the conventional setup. The theoretical analysis was verified on an integrated transformer of an LLC of 1.8 kW achieving a maximum efficiency of 96 %.

The analysis showed that the presented method is best applied near resonance to avoid the large flux densities at an operation above resonance. Therefore, the integrated transformer is best applied in a two-stage architecture where the first galvanically-coupled stage ensures resonance for the second-stage LLC. For the single-stage concept investigated in this thesis, this type of transformer should not be employed. For the wide-range VTR application, two separate components are, thus, employed for the resonant inductance and the transformer.

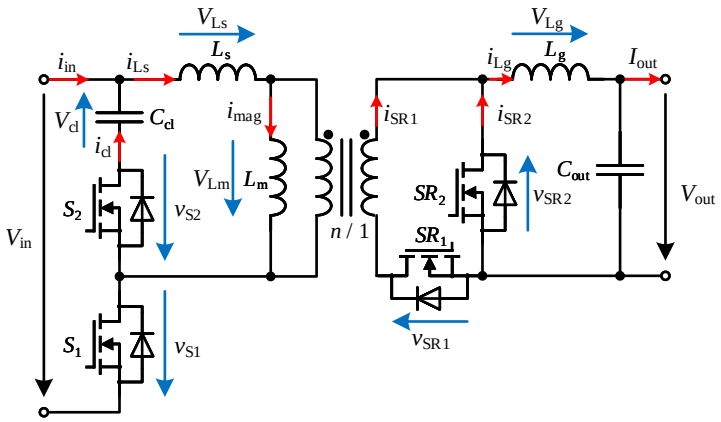


FIGURE 2.76: Circuit diagram of the active-clamp forward converter (ACFC)

2.2 Active-Clamp Forward Converter

The active-clamp forward converter (ACFC) (cf. Figure 2.76) is an extension to the two-transistor forward converter. By adding an additional clamping capacitor C_{cl}, a demagnetizing voltage V_{cl} is created to demagnetize the magnetizing inductance L_m. The demagnetizing voltage is operating-point dependent and varies in dependency of the input and output voltage. It lies in series to the input voltage such that the main switch S_1 and the auxiliary switch S_2 must be designed for a larger blocking voltage. The large load-dependency requires a precise design of the converter to avoid over voltages at high output loads and during load transients.

The topology of the ACFC can provide ZVS for all switches. While ZVS is usually provided for S_2 by the large currents during the energy transfer, for S_1 it can be guaranteed through the magnetizing current ripple if the converter is designed appropriately. During the demagnetization intervals, the current direction of i_{Ls} reverses and the energy stored in L_s discharges the output capacitance of S_1 and charges the output capacitance of S_2. Generally, the ACFC has only been used for low output powers [GMD21] because high turn-off losses and a large parasitic output capacitance prevents ZVS, thus inhibiting the use for higher output powers as a result of large switching losses. With the development of wide-bandgap semiconductors of GaN- or SiC technology, the parasitic output capacitance and turn-off losses of these switches can be dramatically reduced requiring much fewer energy for ZVS. This qualifies the ACFC as an interesting topology with wide-bandgap semiconductors for the use at higher output powers.

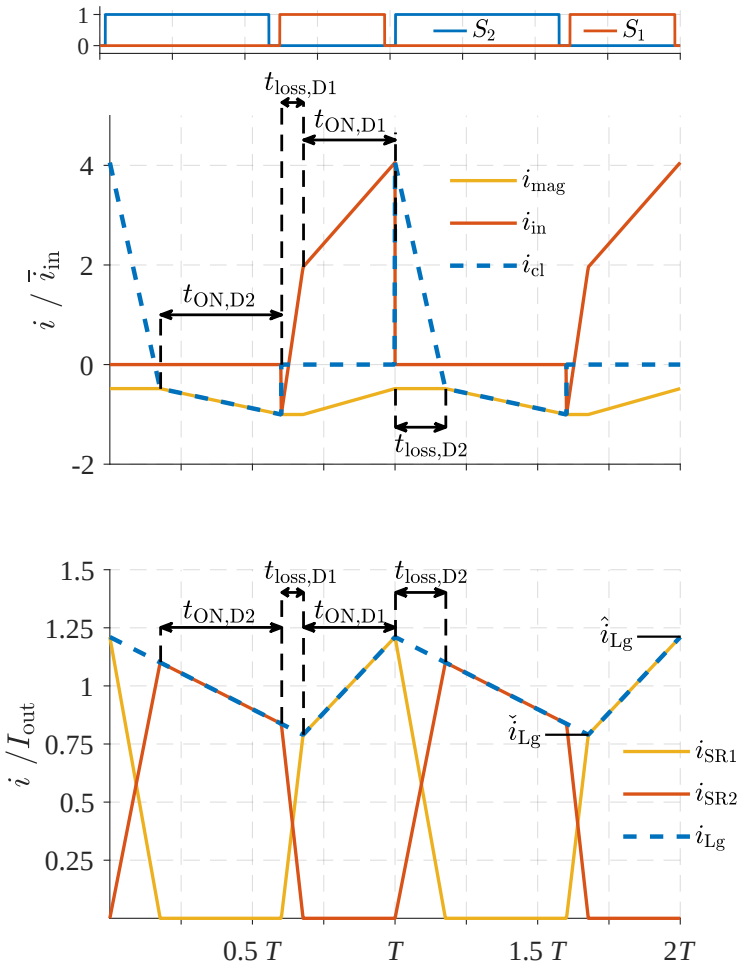


FIGURE 2.77: Shape of the primary and secondary currents of the ACFC in continuous conduction mode (CCM) (parameters: $\text{Config}_{2.2a}$).

2.2.1 Operating principle and modeling for CCM operation

this section has been previously published in parts in [Reh+19a].

During stationary operation, the current waveforms of the ACFC can be divided into four sub-intervals: the energy transfer interval $t_{\text{ON,D1}}$, the demagnetizing interval $t_{\text{ON,D2}}$ and the two duty-cycle loss intervals $t_{\text{loss,D1}}$ and $t_{\text{loss,D2}}$[1]. Figure 2.77 shows the key current waveforms of this topology.

During the interval $t_{\text{loss,D1}}$, the current i_{Ls} rises from the minimum magnetizing current $\check{i}_{\text{mag}}$ by the transformed minimum output inductor current $\check{i}_{\text{Lg}}$. During the interval $t_{\text{loss,D2}}$, the current i_{Ls} falls by the transformed maximum output inductor current $\hat{i}_{\text{Lg}}$. Both intervals lead to reduction of the length of the demagnetizing interval $t_{\text{ON,D2}}$, which is compensated by an increase in the clamp capacitor voltage.

Common calculation methods of the clamp capacitor voltage neglect the influence of these "*loss*" intervals [BA18; DR17; Lin+06; Lin+05; ZU20] and assume that the complete input voltage is applied to L_{m} even though a significant voltage may

[1] the terms *"D1"* and *"D2"* denote the intervals in which S_1 and S_2 are turned on respectively. During an interval with the notation *"D1"*, the main switch S_1 is turned on and during an interval with the notation *"D2"*, the auxiliary switch S_2 is turned on.

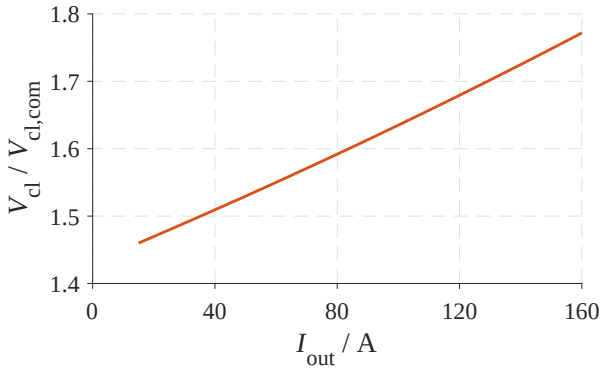


FIGURE 2.78: While common calculation methods assume a load-independent behavior, V_{cl} has a characteristic dependency on the output load. The circuit parameters used to plot this behavior are the ones of the prototype of Figure 3.23c.

drop over L_s. This results in a calculated clamp capacitor voltage lower than the actual one. Commonly, V_{cl} is calculated based only on the input voltage V_{in} and the duty cycle D. With these assumptions, the following voltages applied to L_m result:

$$V_{Lm} = \begin{cases} V_{in} & \text{if } S_1 = 1 \\ -V_{cl} & \text{if } S_1 = 0 \end{cases} \tag{2.58}$$

With the condition $\int_T v_{Lm} dt = 0$, the following equation results for V_{cl}:

$$V_{cl,com} = V_{in} \frac{D}{1-D} \tag{2.59}$$

where the duty cycle D is calculated based on the voltage applied to the output inductor as

$$D = N \frac{V_{out}}{V_{in}}. \tag{2.60}$$

If an ACFC is designed solely with (2.59), V_{cl}, it is evident that the estimated voltage may be much too low. The resulting error can be critical leading to a possible destruction of the applied semiconductors. Figure 2.78 shows the dependency of the clamp capacitor voltage on the output load[1]. It is clear that the error for the calculated voltage of up to 70% is unacceptable and that a more sophisticated design tool is necessary.

In the following model, the intervals $t_{loss,D1}$ and $t_{loss,D2}$ shall not be disregarded and the voltage drop over L_s is taken into account. The operation of the ACFC is divided into the four intervals depicted in Figure 2.77 for CCM. For each of the interval the equivalent circuit is derived, which is a common modeling method for time-domain analysis [SM19; Keu23; Keu+17; Cao14]. This section derives an analytical model in contrast to the derivation of an iterative solution, which is common for resonant converters [SM19; Keu23; Keu+17]. During the modeling process, the following assumptions are set:

[1] the parameters used for this plot are taken from the ACFC-prototype presented in Section 3.4.1

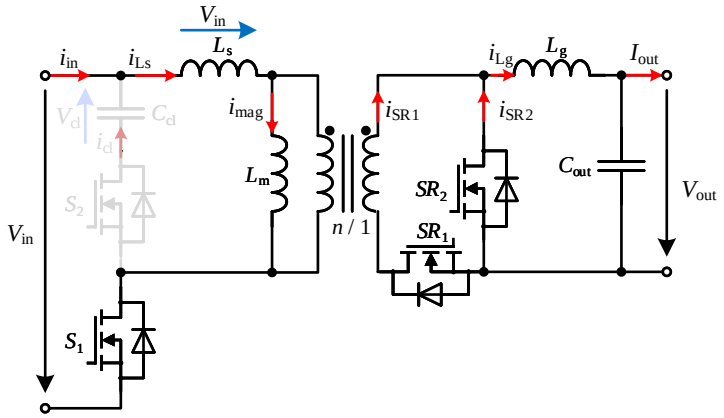


FIGURE 2.79: Equivalent circuit diagram during the interval $t_{\text{loss,D1}}$.

- constant input and output voltage,
- negligible voltage drop over internal resistances in relation to the dominant voltages V_{in}, V_{out} and V_{cl} (high conversion efficiency),
- neglection of parasitic inductances and capacitances (with exception of L_{s}).
- approximately equal average clamp capacitor voltage V_{cl} during the intervals $t_{\text{loss,D2}}$ and $t_{\text{ON,D2}}$[1].

To simplify and shorten the mathematical description, $\hat{i}_{\text{mag}}$ and $\hat{i}_{\text{Lg}}$ represent the maximum of the magnetizing current i_{mag} and the output inductor current i_{Lg} respectively. $\check{i}_{\text{mag}}$ and $\check{i}_{\text{Lg}}$ denote their respective minimum. Furthermore, currents transformed from the secondary side to the primary side are divided by the conversion ratio n ($i'_{\text{sec}} = \frac{i_{\text{sec}}}{n}$), while voltages are multiplied with the winding ratio ($v'_{\text{sec}} = v_{\text{sec}} \cdot n$).

A Duty cycle loss interval $t_{\text{loss,D1}}$

When the main switch S_1 is turned on, the input voltage is applied to series inductor L_{s} and the current i_{Ls} rises such that the current in SR_1 increases as well. Both synchronous rectifier (SR)s on the secondary side are conducting such that the main inductor L_{m} is shorted - the current i_{mag} remains constant. The equivalent circuit diagram of this interval is depicted in Figure 2.79. Since i_{mag} remains constant, i_{s} increases by the transformed minimum output inductor current and the minimum magnetizing current $\check{i}_{\text{mag}}$ such that the interval length can be defined as

$$t_{\text{loss,D1}} = L_{\text{s}} \frac{\check{i}_{\text{Lg}}}{V_{\text{in}}}. \tag{2.61}$$

[1] for the derived model, an average clamp capacitor voltage V_{cl} is calculated for the demagnetizing interval $t_{\text{ON,D2}}$. This voltage may differ slightly from the average clamp capacitor voltage in the interval $t_{\text{loss,D2}}$. To calculate the peak voltage, the characteristic voltage waveform is calculated in section 2.2.1E

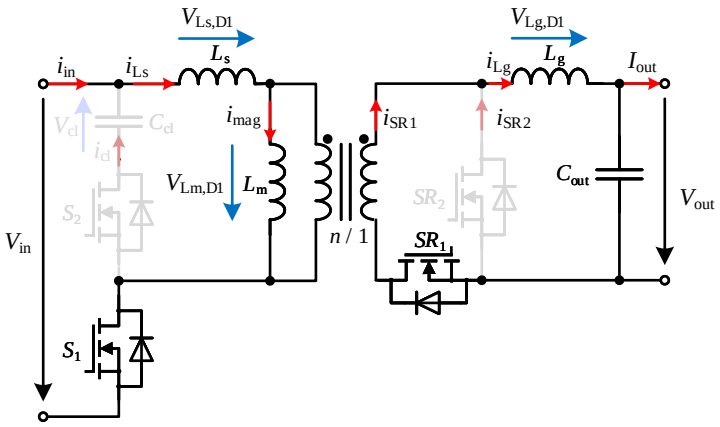


FIGURE 2.80: Equivalent circuit diagram during the interval $t_{ON,D1}$

B Energy transfer interval $t_{ON,D1}$

The energy transfer interval (cf. Figure 2.80) is the only interval in which energy is transferred to the output inductor L_g. The SR SR_1 conducts the full current i_{Lg} while SR SR_2 is blocking. Considering Kirchhoff's voltage and current laws, the voltages applied to the inductors can be calculated with equations (2.62) to (2.66).

$$V_{in} = V_{Ls,D1} + V_{Lm,D1} \tag{2.62}$$

$$V_{Lm,D1} = V'_{Lg,D1} + V'_{out} + V'_D \tag{2.63}$$

As per Kirchhoff's current law, the change in current is used:

$$\Delta i_{Ls} = \Delta i_{Lm} + \Delta i'_{Lg} \tag{2.64}$$

$$\frac{V_{Ls,D1}}{L_s} = \frac{V_{Lm,D1}}{L_m} + \frac{V'_{Lg,D1}}{L'_g} \tag{2.65}$$

The diode voltage V_D in (2.63) can be approximated through a forward voltage V_f[1] and a series resistance R_D as

$$V_D = V_f + R_D I_{out}. \tag{2.66}$$

The approximation with the constant output current I_{out} is correct due to the trapezoidal waveform, which is proved as follows.

$$\frac{1}{t_{ON,D1}} \int_0^{t_{ON,D1}} R_D i_{D1} \mathrm{d}t = R_D I_{out} \tag{2.67}$$

Equations (2.62) - (2.65) can be solved for the voltages $V_{Ls,D1}$, $V_{Lm,D1}$, and $V_{Lg,D1}$. With the calculation of $V_{Lg,D1}$, the interval length of $t_{ON,D1}$ can be calculated with

[1] for a synchronous rectifier, this voltage is zero. However, to extend this model for a rectification with diodes, this term is not omitted here.

(2.68). The voltage applied to the output inductor L_g in the remaining intervals is $-(V_{out} + V_D)$ due to the conduction of SR_2.

$$t_{ON,D1} V_{Lg,D1} = (T - t_{ON,D1})(V_{out} + V_D) \tag{2.68}$$

This allows the calculation of the output current ripple Δi_{Lg} with equation (2.69) enabling the derivation of the maximum and minimum output inductor current $\hat{i}_{Lg}$ and $\check{i}_{Lg}$ with equations (2.70) and (2.71) respectively.

$$\Delta i_{Lg} = \frac{t_{ON,D1}}{L_g} V_{Lg,D1} \tag{2.69}$$

$$\hat{i}_{Lg} = I_{out} + \Delta i_{Lg} \tag{2.70}$$

$$\check{i}_{Lg} = I_{out} - \Delta i_{Lg} \tag{2.71}$$

Furthermore, the current ripple of the magnetizing current Δi_{mag} can be calculated with $V_{Lm,D1}$ as

$$\Delta i_{mag} = \hat{i}_{mag} - \check{i}_{mag} = \frac{V_{Lm,D1} t_{ON,D1}}{L_m}. \tag{2.72}$$

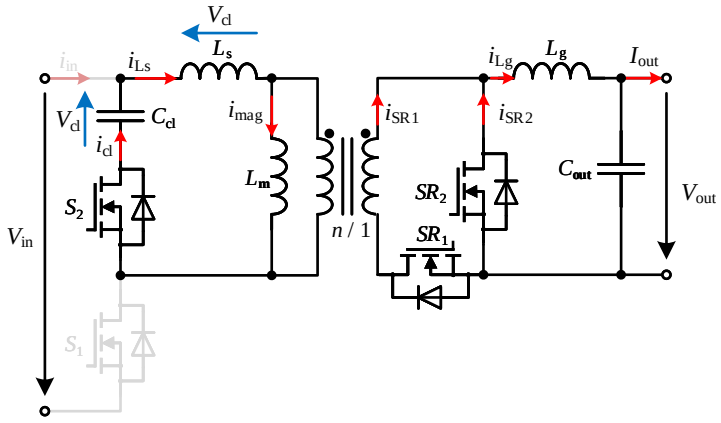


FIGURE 2.81: Equivalent circuit diagram during the interval $t_{\text{loss,D2}}$

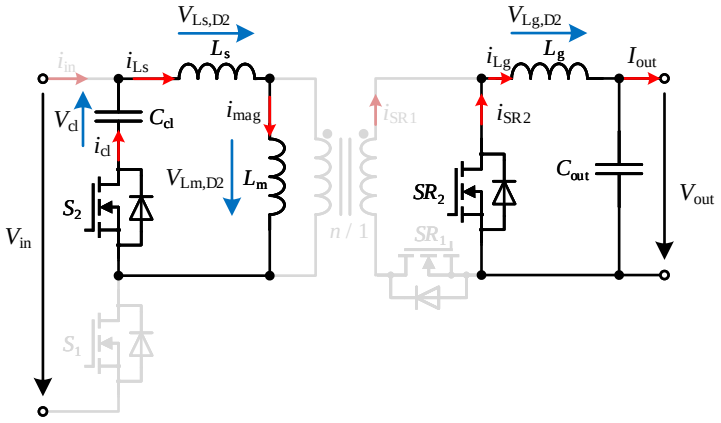


FIGURE 2.82: Equivalent circuit diagram during the interval $t_{\text{ON,D2}}$

C Duty cycle loss interval $t_{\text{loss,D2}}$

During the interval $t_{\text{loss,D2}}$ (cf. Figure 2.81), the current i_{Ls} falls by $\hat{i}'_{\text{Lg}}$ to the maximum magnetizing current $\hat{i}_{\text{mag}}$. The magnetizing inductance is shorted and the magnetizing current remains constant. The interval length can be calculated as

$$t_{\text{loss,D2}} = L_{\text{s}} \frac{\hat{i}'_{\text{Lg}}}{V_{\text{cl}}}. \tag{2.73}$$

The charge Q_{cl1} transferred to C_{cl} is calculated through integration of i_{Ls} as

$$Q_{\text{cl1}} = (\hat{i}_{\text{mag}} + \frac{\hat{i}'_{\text{Lg}}}{2}) t_{\text{loss,D2}}. \tag{2.74}$$

D Active-clamp reset interval $t_{\text{ON,D2}}$

During the demagnetizing interval $t_{\text{ON,D2}}$ (cf. Figure 2.82), the magnetizing inductance is demagnetized through the applied clamp capacitor voltage V_{cl}. The SR SR_1 is blocking and the whole output inductor current i_{Lg} flows through the freewheeling SR SR_2. The voltage applied to the magnetizing inductance is calculated as an inductive voltage divider as

$$V_{\mathrm{Lm,D2}} = V_{\mathrm{cl}} \frac{L_{\mathrm{m}}}{L_{\mathrm{m}} + L_{\mathrm{s}}}. \tag{2.75}$$

The charge flowing into the clamp capacitor C_{cl} is calculated as

$$Q_{\mathrm{cl2}} = t_{\mathrm{ON,D2}} (\hat{i}_{\mathrm{mag}} - \frac{\Delta i_{\mathrm{mag}}}{2}). \tag{2.76}$$

The average voltage applied to L_{m} is zero allowing the definition of equation (2.77). Since V_{cl} and $t_{\mathrm{ON,D2}}$ are both unknown parameters, $t_{\mathrm{ON,D2}}$ is expressed through equation (2.78) such that (2.77) can be solved for V_{cl}.

$$V_{\mathrm{Lm,D1}} t_{\mathrm{ON,D1}} = V_{\mathrm{cl}} \frac{L_{\mathrm{m}}}{L_{\mathrm{m}} + L_{\mathrm{s}}} t_{\mathrm{ON,D2}} \tag{2.77}$$

$$t_{\mathrm{ON,D2}} = (T - t_{\mathrm{ON,D1}} - t_{\mathrm{loss,D1}} - t_{\mathrm{loss,D2}}) \tag{2.78}$$

Two unsolved variables remain in the definition of V_{cl}: $\hat{i}_{\mathrm{mag}}$ and $\check{i}_{\mathrm{mag}}$. One of these can be eliminated with equation (2.72). The remaining unsolved variable can be solved through the definition of the average clamp capacitor charge being zero as

$$Q_{\mathrm{cl1}} + Q_{\mathrm{cl2}} = 0. \tag{2.79}$$

With these derivations, the complete current waveform of the ACFC-operation can be calculated analytically and the average clamp capacitor voltage was derived. The equations were solved with Matlab Symbolic Solver. For the sake of brevity, the complete derivations will not be stated.

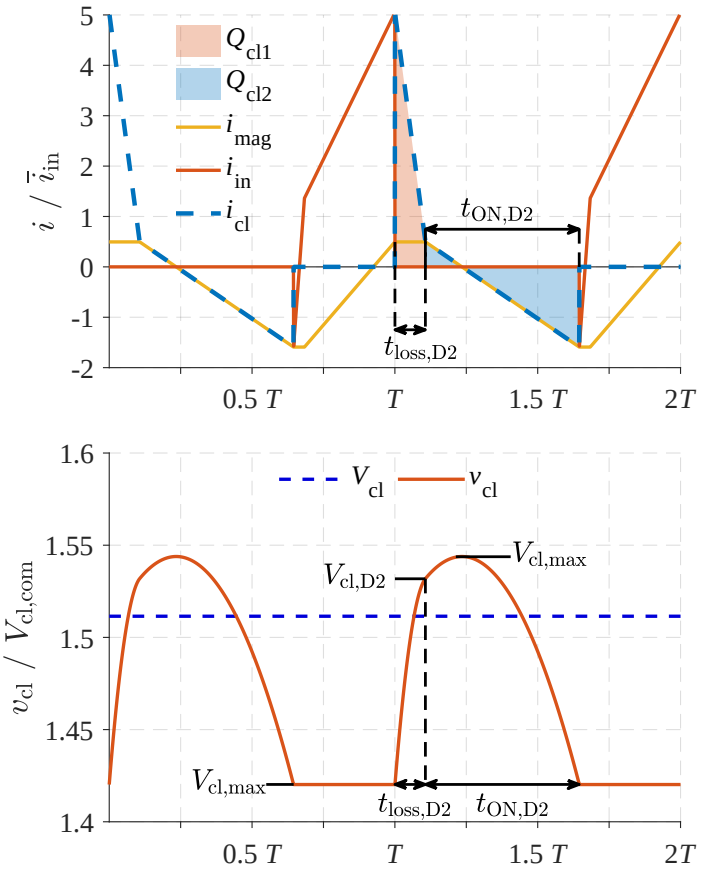


FIGURE 2.83: Shape of the primary current and clamp capacitor voltage in CCM (parameters: Config$_{2.2a}$).

E Approximation of the clamp capacitor voltage peak

In Sections 2.2.1C and 2.2.1D, an average clamp capacitor voltage V_{cl} was assumed. However, the clamp capacitor voltage will vary depending on the size of the clamp capacitance. To estimate the peak clamp capacitor voltage, a model shall be derived to calculate the peak clamp capacitor voltage based on the average voltage V_{cl}.

The clamp capacitor voltage defined in (2.2.1A) to (2.2.1D) is defined as the average voltage during the interval $t_{ON,D2}$ as

$$V_{cl} = \frac{1}{t_{ON,D2}} \int_{t_{ON,D2}} v_{cl}(t)\mathrm{d}t \tag{2.80}$$

The voltage waveform of v_{cl} in this interval can be calculated through integration of the current $i_{Ls} = i_{mag}$ with equation (2.81). $V_{cl,D2}$ is here the initial voltage of v_{cl} at the beginning of this interval.

$$v_{cl}(t) = V_{cl,D2} + \frac{1}{C_{cl\,cl}} \int_t (\hat{i}_{mag} - \frac{\Delta i_{mag}}{t_{ON,D2}}\tau)\mathrm{d}\tau \tag{2.81}$$

$V_{cl,D2}$ can now be calculated through the current waveform in the interval $t_{loss,D2}$ with equation 2.82. $V_{cl,init}$ is here the initial value of v_{cl} in this interval.

$$V_{\mathrm{cl,D2}} = V_{\mathrm{cl,init}} + \frac{1}{C_{\mathrm{cl}}} \int_{t_{\mathrm{loss,D2}}} (\hat{i}_{\mathrm{mag}} + \hat{i}'_{\mathrm{Lg}} - \frac{\hat{i}'_{\mathrm{Lg}}}{t_{\mathrm{loss,D2}}} t) \mathrm{d}t \tag{2.82}$$

By inserting (2.82) in (2.81) in (2.80), equation (2.80) can be rearranged and solved for $V_{\mathrm{cl,init}}$. The voltage waveform is now completely described allowing the calculation of the peak clamp capacitor voltage $\hat{v}_{\mathrm{cl}}$.

The peak clamp capacitor voltage $\hat{v}_{\mathrm{cl}}$ can be calculated analytically. It is given if $i_{\mathrm{Ls}} = 0$. The voltage is rising if $i_{\mathrm{Ls}} > 0$ and falling if $i_{\mathrm{Ls}} < 0$. The peak clamp capacitor voltage can be calculated through a simple case distinction depending only on the maximum magnetizing current. The maximum lies in the interval $t_{\mathrm{loss,D2}}$ for $\hat{i}_{\mathrm{mag}} < 0$ and in the interval $t_{\mathrm{ON,D2}}$ for $\hat{i}_{\mathrm{mag}} \geq 0$. The peak voltage can be calculated through (2.84) where the additional charge Q_{cl} responsible for the peak is calculated as

$$Q_{\mathrm{cl}} = \begin{cases} (\hat{i}_{\mathrm{mag}} + \frac{\hat{i}'_{\mathrm{Lg}}}{2}) t_{\mathrm{loss,D2}} + \frac{\hat{i}_{\mathrm{mag}}}{2} \cdot t_{\mathrm{ON,D2}} \frac{\hat{i}_{\mathrm{mag}}}{\Delta i_{\mathrm{mag}}} & \text{if } \hat{i}_{\mathrm{mag}} \geq 0 \\ \frac{\hat{i}'_{\mathrm{Lg}} + \hat{i}_{\mathrm{mag}}}{2} \cdot t_{\mathrm{loss,D2}} \frac{\hat{i}'_{\mathrm{Lg}} + \hat{i}_{\mathrm{mag}}}{\hat{i}'_{\mathrm{Lg}}} & \text{if } \hat{i}_{\mathrm{mag}} < 0 \end{cases} \tag{2.83}$$

$$\hat{v}_{\mathrm{cl}} = V_{\mathrm{cl,init}} + \frac{Q_{\mathrm{add,Ccl}}}{C_{\mathrm{cl}}} \tag{2.84}$$

F A simplified model of the average clamp-capacitor voltage V_{cl}

The preceding simplified modeling methods [BA18; DR17; Lin+06; Lin+05] assumed an ideal transformer such that the transformed input voltage appears at the secondary side of the transformer during the energy-transfer interval $t_{\mathrm{ON,D1}}$ (cf. Figure 2.77). However, this is not the case since a significant portion of the input voltage may be applied to the series inductance L_{s}. Thus, the output inductor voltage is reduced and $V_{\mathrm{Lg,D1}}$ must be accurately calculated by solving (2.62) - (2.65).

For $V_{\mathrm{Lg,D1}}$ and $\widetilde{V}_{\mathrm{out}} = V_{\mathrm{out}} + V_{\mathrm{D}} = V_{\mathrm{out}} + V_{\mathrm{d}} + R_{\mathrm{d}} I_{\mathrm{out}}$ (V_{d} is the forward voltage of the rectifier, R_{d} is the resistance of the rectifier), this yields

$$V_{\mathrm{Lg,D1}} = -\frac{L_{\mathrm{g}} n \left(-L_{\mathrm{m}} V_{\mathrm{in}} + n \widetilde{V}_{\mathrm{out}} (L_{\mathrm{s}} + L_{\mathrm{m}}) \right)}{n^2 L_{\mathrm{g}} (L_{\mathrm{m}} + L_{\mathrm{s}}) + L_{\mathrm{m}} L_{\mathrm{s}}} \tag{2.85}$$

Thus, the duty cycle $\widetilde{D}$ can be calculated as $\widetilde{D} = \frac{\widetilde{V}_{\mathrm{out}}}{V_{\mathrm{Lg,D1}} + \widetilde{V}_{\mathrm{out}}}$. The duty-cycle loss intervals $t_{\mathrm{loss,D1}}$ and $t_{\mathrm{loss,D2}}$ (cf. Figure 2.77) can be estimated as $t_{\mathrm{loss,D1}} = \frac{I_{\mathrm{out}} L_{\mathrm{s}}}{N V_{\mathrm{in}}}$ and $t_{\mathrm{loss,D2}} = \frac{I_{\mathrm{out}} L_{\mathrm{s}}}{N V_{\mathrm{cl}}}$. The voltage-time area (also called *voltage seconds*) of the voltage applied to the magnetizing inductance L_{m} during $t_{\mathrm{ON,D1}}$ and $t_{\mathrm{ON,D2}}$ must be equal:

$$V_{\mathrm{cl}} (T - t_{\mathrm{loss,D1}} - t_{\mathrm{loss,D2}} - \widetilde{D} T) = V_{\mathrm{in}} \widetilde{D} T. \tag{2.86}$$

In this equation, the voltage V_{in} is used for the magnetizing voltage V_{Lm} during $t_{\mathrm{ON,D1}}$, even though the real voltage $V_{\mathrm{Lm,D1}}$ can be accurately calculated by solving (2.63). This was done as it yields a slightly higher approximation of the clamp capacitor voltage to simplify the lengthy accurate calculation of the clamp capacitor voltage as it was done in the preceding work of [Reh+19a; Reh+19c]. Equation (2.86) can be solved for the clamp capacitor voltage V_{cl} yielding

$$V_{\mathrm{cl}} = -\frac{V_{\mathrm{in}}\left(\sigma + nTV_{\mathrm{in}}V_{\mathrm{out}}\right)}{\sigma - nTV_{\mathrm{Lg,D1}}V_{\mathrm{in}}} \tag{2.87}$$

with (2.85) and

$$\sigma = I_{\mathrm{out}}L_{\mathrm{s}}\left(V_{\mathrm{Lg,D1}} + V_{\mathrm{out}}\right) \tag{2.88}$$

This calculation is much simpler than the calculation developed in [Reh+19a]. The simplified model and the complex model of [Reh+19a] are benchmarked in 2.2.1G.

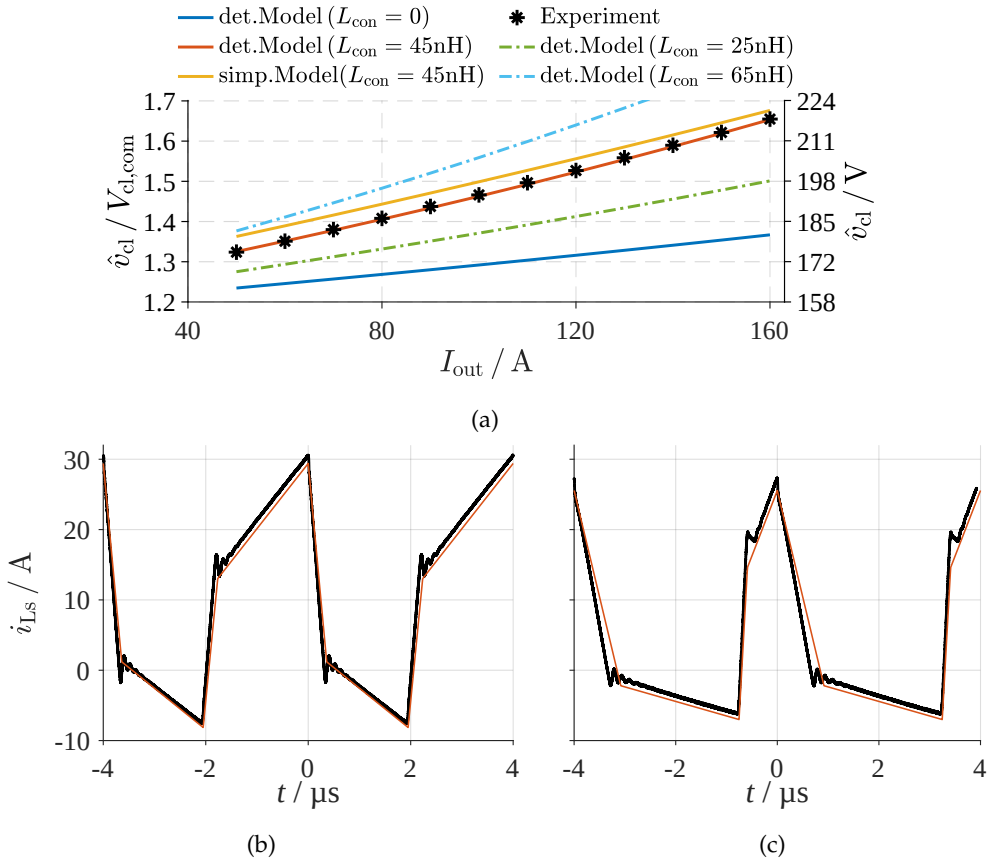


FIGURE 2.84: (a) Validation of the clamp capacitor voltage model (detailed and simplified) for the parameters Config$_{2.2c}$. (b) modeled and measured primary transformer currents for the parameters Config$_{2.2d}$ and (c) the parameters Config$_{2.2e}$.

G Analysis of the model results

this section has been previously published in parts in [Reh+22a].

The develeoped model and the simplified model described in 2.2.1F shall be verified in this section. The inductance matrix of the transformer is given as

$$\boldsymbol{L} = \begin{pmatrix} L_{11} & M_{12} \\ M_{12} & L_{22} \end{pmatrix} \stackrel{!}{=} \begin{pmatrix} L_r + L_m & \frac{L_m}{N} \\ \frac{L_m}{N} & \frac{L_m}{N^2} \end{pmatrix}, \tag{2.89}$$

where the values were measured with a Wayne Kerr 6500B to $L_{11} = 43\,\mu$H, $M_{12} = 6.32\,\mu$H, and $L_{22} = 902\,$nH. If employed in the steady-state model, the calculated clamp-capacitor voltage shows a significant error when compared with the experimental measurement results. However, the inductance measurement of the transformer does not consider the stray inductance of the transformer connectors and the secondary PCB tracks. Due to the significant turns ratio of 7:1, any minor stray inductance L_{con} of the connectors and PCB tracks results in a significant effective primary series inductance increase. When considering the inductance model of the transformer, the secondary series inductance is given by $L_{s2} = L_{22} - \frac{M_{12}}{A}$. Since the system is under-determined, the value A can be chosen freely [Alb17; Keu+19;

KSB19]. To retrieve a primary-concentrated equivalent inductance model that includes L_{con}, the necessary condition is

$$L_{22} - \frac{M_{12}}{A} + L_{con} \stackrel{!}{=} 0 \tag{2.90}$$

This equation must be solved for A. Through the redefinition of n to $n_{new} = A$, the magnetizing inductance $L_{m,new}$ and series inductance $L_{s,new}$ are altered and can be calculated as

$$\begin{aligned} L_{s1,new} &= L_{11} - n_{new} M_{12} \\ L_{m,new} &= n_{new} M_{12}. \end{aligned} \tag{2.91}$$

If the connectors and the PCB tracks are estimated with a stray inductance of $L_{con} = 45\,\text{nH}$, the equivalent inductances are $L_{s1,new} = 3.27\,\mu\text{H}$, $L_{m,new} = 37.8\,\mu\text{H}$ and $n_{new} = 6.48$. These values were used for the calculation of the clamp-capacitor voltage in Figure 2.84a and the depiction of the calculated and measured primary transformer currents in Figure 2.84b and Figure 2.84c. For this assumption of the stray inductance, the prediction of the detailed model fits nearly perfectly. The maximum error is below 1 %. The simplified model, which was developed in 2.2.1F also shows accurate results with errors below 3 %. The voltage is, however, calculated slightly overestimated. Considering the measured and calculated current shape displayed in Figure 2.84b and Figure 2.84c, it is evident that the current slope of the model in the $t_{loss,D1}$ interval fits the measured current slope such that the assumption of a connection stray inductance of $L_{con} = 45\,\text{nH}$ can be considered valid.

2.2.2 Operating principle and modeling for DCM operation

A Calculation of the current shape

The discontinuous conduction (visualized in Figure 2.85) mode can equally be modeled as the continuous conduction mode of Section 2.2.1A-2.2.1D. In fact all previous equations are also valid for the DCM operation with the exception of (2.68). In DCM, the minimum current of the output inductance is zero ($\check{i}_{Lg} = 0$), which means that there is no $t_{loss,D1}$ interval. Therefore, the maximum output current $\hat{i}_{Lg}$ can be expressed as

$$\hat{i}_{Lg} = t_{ON,D1} \frac{V_{Lg,ON}}{L_g}. \tag{2.92}$$

During $t_{ON,D1}$, the charge delivered to the output capacitance is

$$Q_{out,1} = t_{ON,D1} \frac{\hat{i}_{Lg}}{2}. \tag{2.93}$$

The respective time interval in which the output inductor current is decreasing but non-zero can be calculated as

$$t_{DCM} = \hat{i}_{Lg} \frac{L_g}{V_{out}}. \tag{2.94}$$

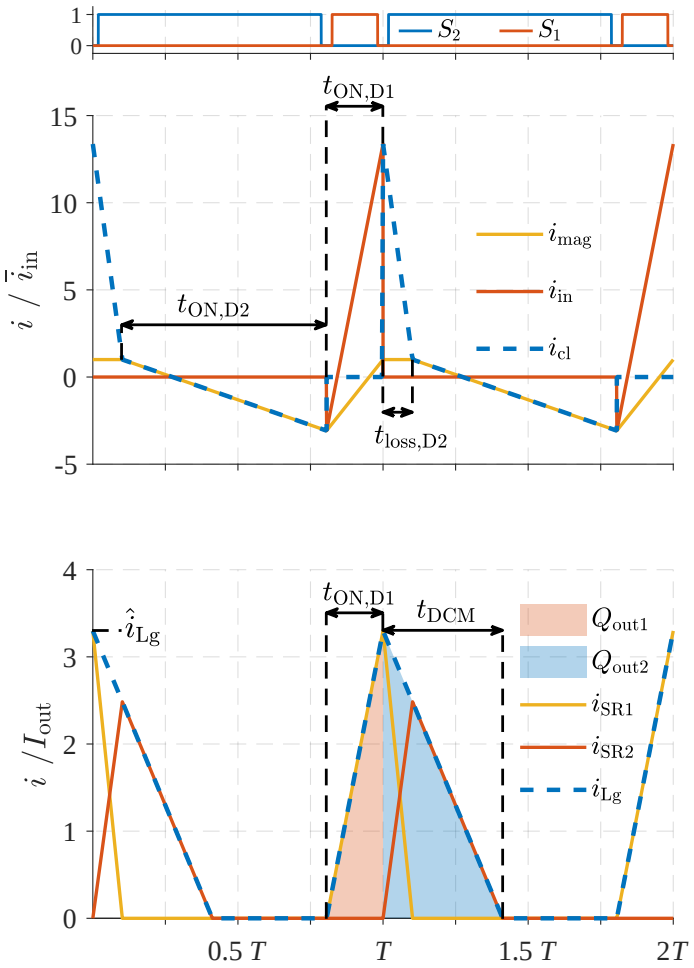


FIGURE 2.85: Shape of the primary and secondary currents of the ACFC in discontinuous conduction mode (DCM) (parameters: $\text{Config}_{2.2f}$).

The charge during this time interval can be calculated as

$$Q_{\text{out},2} = t_{\text{DCM}} \frac{\hat{i}_{\text{Lg}}}{2}. \tag{2.95}$$

Therefore, the final charge balance is

$$I_{\text{out}} = (Q_{\text{out},1} + Q_{\text{out},2})\, f_{\text{sw}}. \tag{2.96}$$

(2.96) can be solved for $t_{\text{ON,D1}}$, such that the whole current shape can be calculated allowing the calculation of the clamp capacitor voltage and RMS currents.

B Analysis of the model results

Figure 2.86b and Figure 2.86c shows the measured primary current shape of the ACFC in DCM with the modeled current shape assuming a secondary stray inductance of $L_{\text{con}} = 45\,\text{nH}$ (see section 2.2.1G). The analysis shows that the modeled current shape is quite similar to the experimentally measured shape. Additionally, Figure 2.86a shows modeled and measured results of the maximum clamp capacitor voltage $\hat{v}_{\text{cl}}$. It is obvious that the influence of the secondary stray inductance $L_{\text{con}} = 45\,\text{nH}$ has only a minor influence on the clamp capacitor voltage in DCM

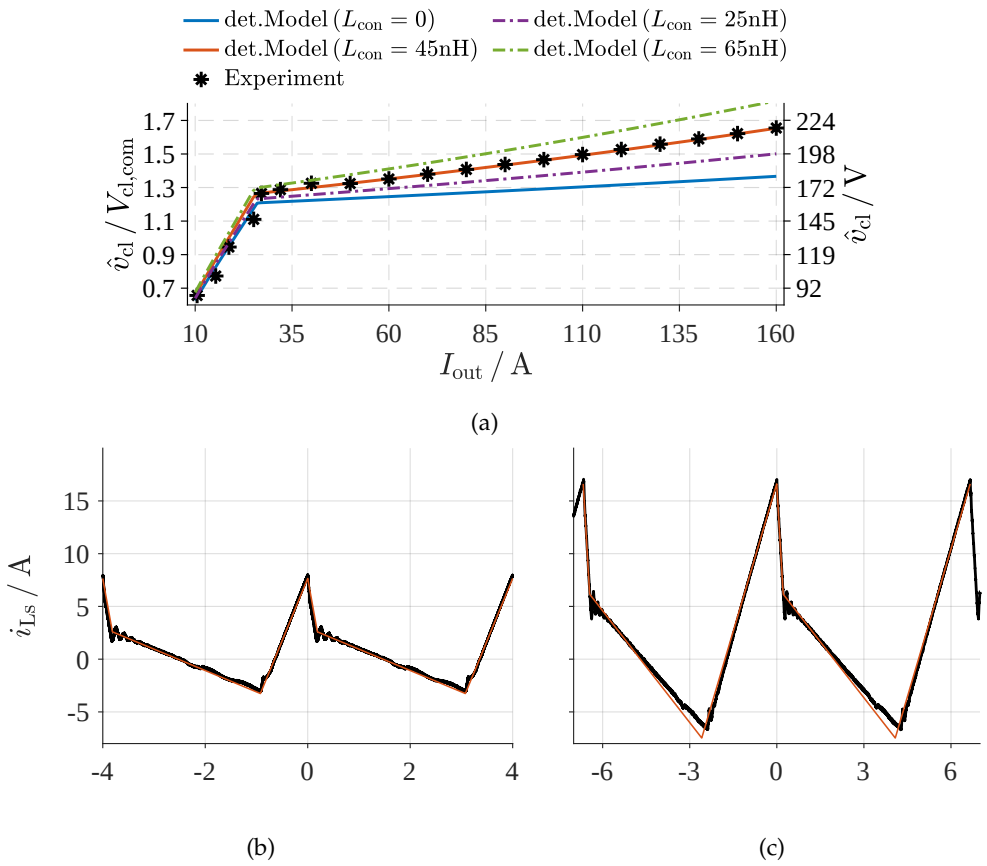


FIGURE 2.86: (a) Validation of the clamp capacitor voltage model (detailed and simplified) for the parameters Config$_{2.2g}$. (b) modeled and measured primary transformer currents for the parameters Config$_{2.2h}$ and (c) the parameters Config$_{2.2i}$.

operation. It is evident that the accuracy of the model is quite high with only small errors.

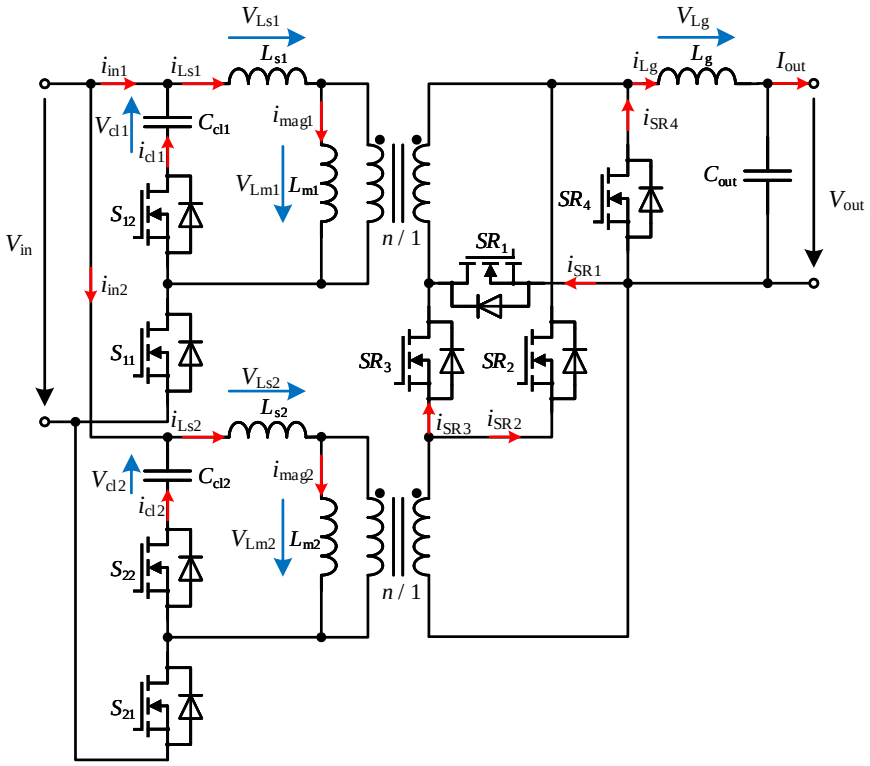


FIGURE 2.87: Circuit diagram of the extended-interleaved ACFC (eiACFC).

2.2.3 Model extension for the extended-interleaved ACFC

this section has been previously published in parts in [Reh+19c].

For increased output powers two ACFCs can be interleaved. Traditional interleaving assumes two converters parallel connected at the input and output voltage. However, for the ACFC, two converters can share a mutual output inductance. By operating the two converters with a phase shift of 180°, the effective frequency applied to the output inductor is doubled, substantially reducing its size. The operation is restricted to a duty cycle of $D = 0.5$. To allow duty cycles over 0.5 an additional diode (or SR) must be added, allowing the two converters to operate on the secondary side in series, as visualized in Figure 2.87. This circuit was proposed by [Zha+09a]. A disadvantage of this eiACFC is that the diodes (or SRs) have to conduct the full output current, whereas in a hard parallel connection of the two converters, the diodes (or SRs) of the single ACFC only conduct half the output current. Due to the advanced operation of the eiACFC, a model shall be developed extending the previously one to this topology. There are two modes of operation:

- pure secondary parallel operation (current shape visualized in Figure 2.88),
- secondary parallel and series operation (series-parallel operation, current shape visualized in Figure 2.89).

In the secondary parallel operation, the voltage applied to the SR SR_4 is only the transferred voltage of one of the both converters. In the secondary series-parallel operation, there are intervals in which the voltage applied to SR_4 is the sum of

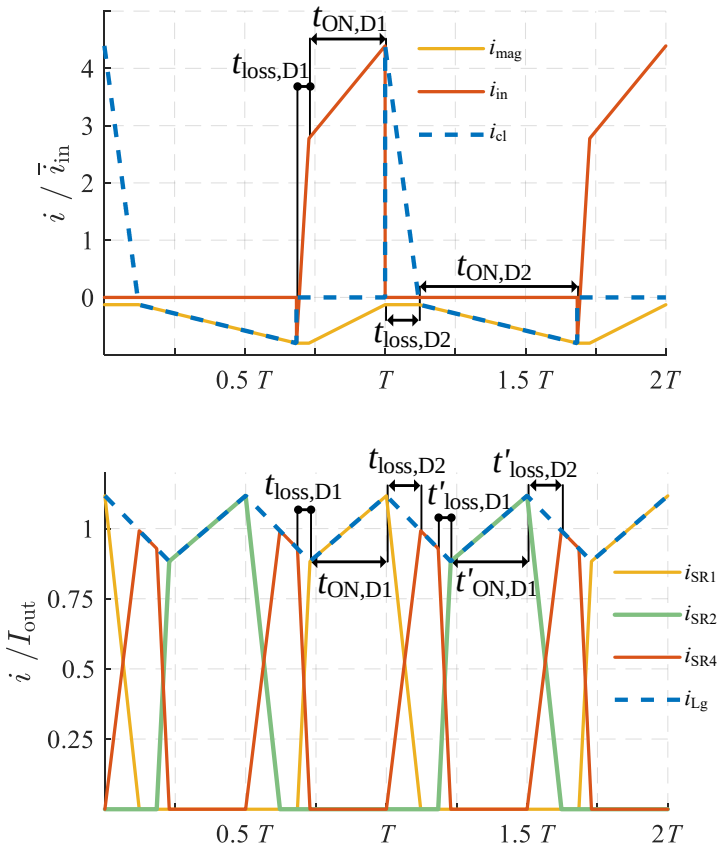


FIGURE 2.88: Exemplary steady-state operation of the eiACFC in pure secondary parallel operation (parameters: $\text{Config}_{2.2j}$).

the transferred voltage of both converters. Due to this separation of the operating modes, the model must be derived individually for both modes.

A Pure secondary parallel operation

The steady-state operation of the eiACFC differs insignificantly from the operation of the non-interleaved ACFC. While for the non-interleaved ACFC power is transferred once per period to the output inductor, for the eiACFC there are two energy-transfer intervals. For that purpose, (2.68) must be altered to

$$2t_{ON,D1}(V_{Lg,D1} - V_{out} - V_D) = (T - 2t_{ON,D1})(V_{out} + V_D). \tag{2.97}$$

With this modification, the steady-state operation can be solved for all relevant parameters as described above. The variable $t_{ON,D1}$ describes, how long $V_{D4} = V'_{Lm}$. If $t_{ON,D1} > \frac{T}{2}$, the converter operates no longer in the pure secondary parallel operation and is factually operating on the secondary side in a series-parallel configuration. Therefore, a steady-state calculator can calculate $t_{ON,D1}$ first and determine in which configuration the eiACFC is operating.

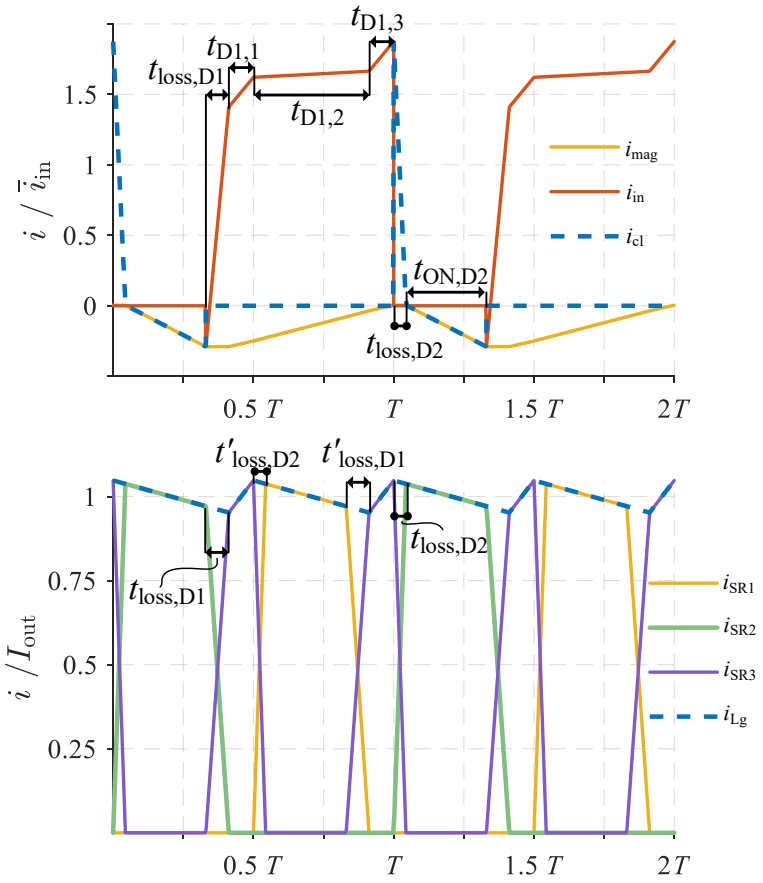


FIGURE 2.89: Exemplary operation of the eiACFC in secondary series-parallel configuration (parameters: $\text{Config}_{2.2k}$).

B Secondary series- and parallel operation

During the secondary series-parallel configuration, the formerly described energy-transfer interval is divided into three sub-intervals: $t_{D1,1}$, $t_{D1,2}$ and $t_{D1,3}$ as depicted in Figure 2.89. In the interval $t_{D1,2}$ where $V_{D4} = V'_{Lm} - V_D$ (secondary parallel operation, i_{Lg} is falling). In the intervals $t_{D1,1}$ and $t_{D1,3}$, the converter is operating on the secondary side in series, i_{Lg} is rising and $V_{D4} = 2V'_{Lm} - V_D$.

B1 Secondary parallel interval $t_{D1,2}$ During the interval $t_{D1,2}$ (cf. Figure 2.90), the eiACFC is operating on the secondary side in parallel as depicted in the equivalent circuit in Figure 2.90. SR SR_1 conducts the full output inductor current i_{Lg}. The voltages applied to the inductances ($V_{Ls,D12}$, $V_{Lm,D12}$ and $V_{Lg,D12}$)[1] can be calculated analogously to the equations (2.62) - (2.65).

B2 Secondary series intervals $t_{D1,1}$ and $t_{D1,3}$ During the secondary-series intervals $t_{D1,1}$ and $t_{D1,3}$ (cf. Figure 2.91), the eiACFC is operating on the secondary side

[1] the symbol subscript have been altered to include the interval extension "*D12*" to refer to this specific interval.

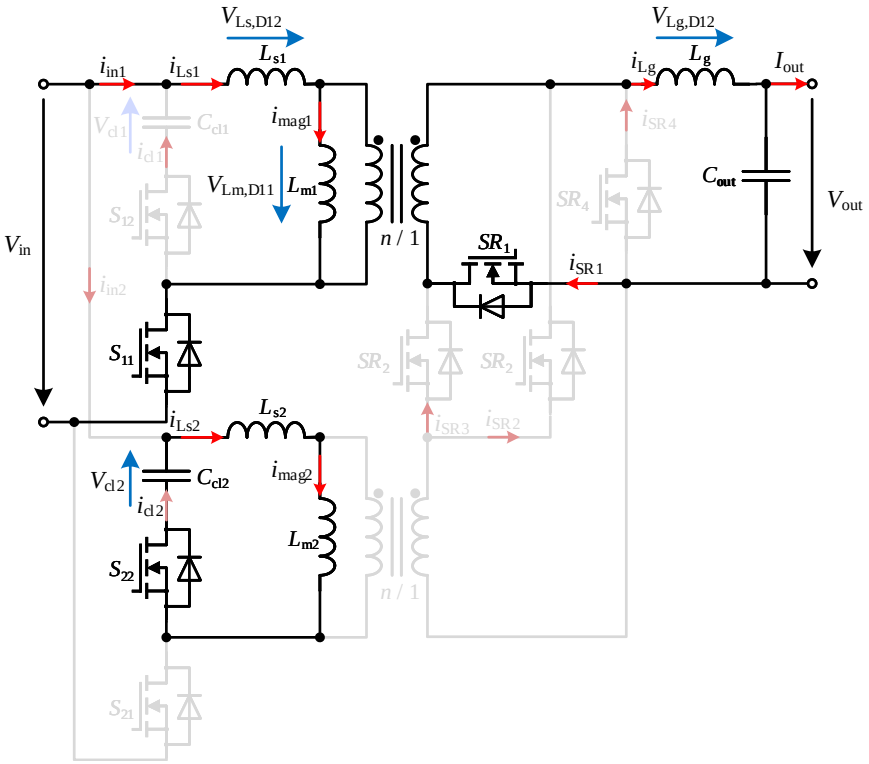


FIGURE 2.90: Equivalent circuit diagram during the interval $t_{D1,2}$

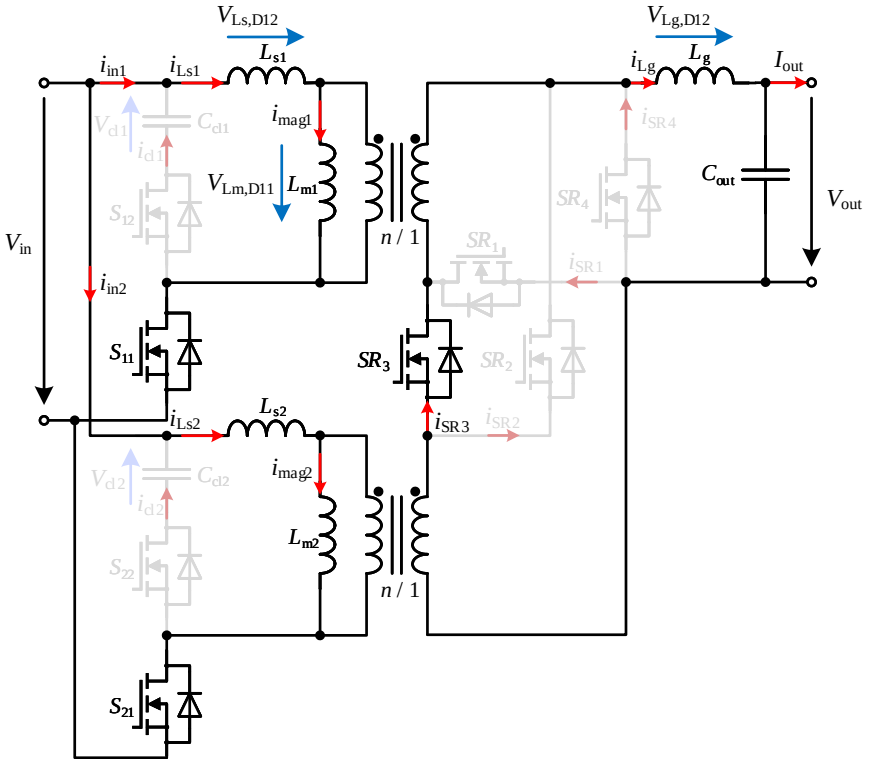


FIGURE 2.91: Equivalent circuit diagram for interval $t_{D1,1}$ and $t_{D1,3}$

in series as depicted in the equivalent circuit in Figure 2.91. Due to the symmetry of operation $t_{D1,1} = t_{D1,3}$. SR SR_3 conducts i_{Lg} and voltage applied to D_4 is $V_{D4} = 2V'_{Lm} - V_D$. While (2.62) and (2.65) are equally valid, (2.63) has to be altered to

$$2V_{Lm,D11} = V'_{Lg} + V'_{out} + V'_D \tag{2.98}$$

With this modification all inductor voltages ($V_{Ls,D11}$, $V_{Lm,D11}$ and $V_{Lg,D11}$) can be calculated[1]. For this mode of operation, (2.68) must be replaced with (2.99), which can be solved for $t_{D1,1}$ by expressing $t_{D1,2}$ with equation (2.100).

$$2t_{D1,1}V_{Lg,D11} = (T - 2t_{D1,1})V_{Lg,D12} \tag{2.99}$$

$$t_{D1,2} = \frac{1}{2}(T - 2t_{D1,1}) \tag{2.100}$$

The expression of $t_{D1,1}/t_{D1,3}$ and $t_{D1,2}$, Δi_{Lg} and Δi_{mag} can be derived with (2.101) and (2.102) respectively.

$$\Delta i_{Lg} = V_{Lg,D12}\frac{t_{D1,1}}{L_g} \tag{2.101}$$

$$\Delta i_{mag} = \frac{1}{L_m}(2t_{D1,1}V_{Lm,D11} + t_{D1,2}V_{Lm,D12}) \tag{2.102}$$

The mathematical description of remaining intervals $t_{loss,D1}$, $t_{loss,D2}$, and $t_{ON,D2}$ is equally valid for the eiACFC such that the steady-state operation can be solved analogously with the modified equations above.

C Analysis of the model results

To test the feasibility and accuracy of the developed model, this section shows the verification through switched circuit simulations using the software PLECS. While Sections 2.2.1G and 2.2.2B evaluated the model using a developed prototype, this section uses results of a simulation model that includes circuit parasitics such as the output capacitance of the primary and secondary MOSFETs . A prototype of the eiACFC has not been developed due to the large RMS currents of the rectifier semiconductors of this high-current application. Each semiconductor conducts the combined output current of both rails, which increases the RMS current dramatically. While each semiconductor only conducts the output current partially, the effect of the increased amplitude weighs heavily such that semiconductors of reduced on-state resistance have to be selected, increasing the costs and losses. For applications of reduced output currents and loads, however, this kind of converter may still be feasible. Therefore, this kind of converter has not been considered for experimental verification such that simulation results are employed only.

Figure 2.92 shows a comparison of the simulation results and the analytically modeled behavior. The clamp capacitor voltage dependency on the output load of the secondary-series operation is depicted in Figure 2.92a, whereas the dependency

[1] to refer to the inductor voltages during the intervals $t_{D1,1}$ and $t_{D1,3}$, the subscript have been altered to include "*D11*".

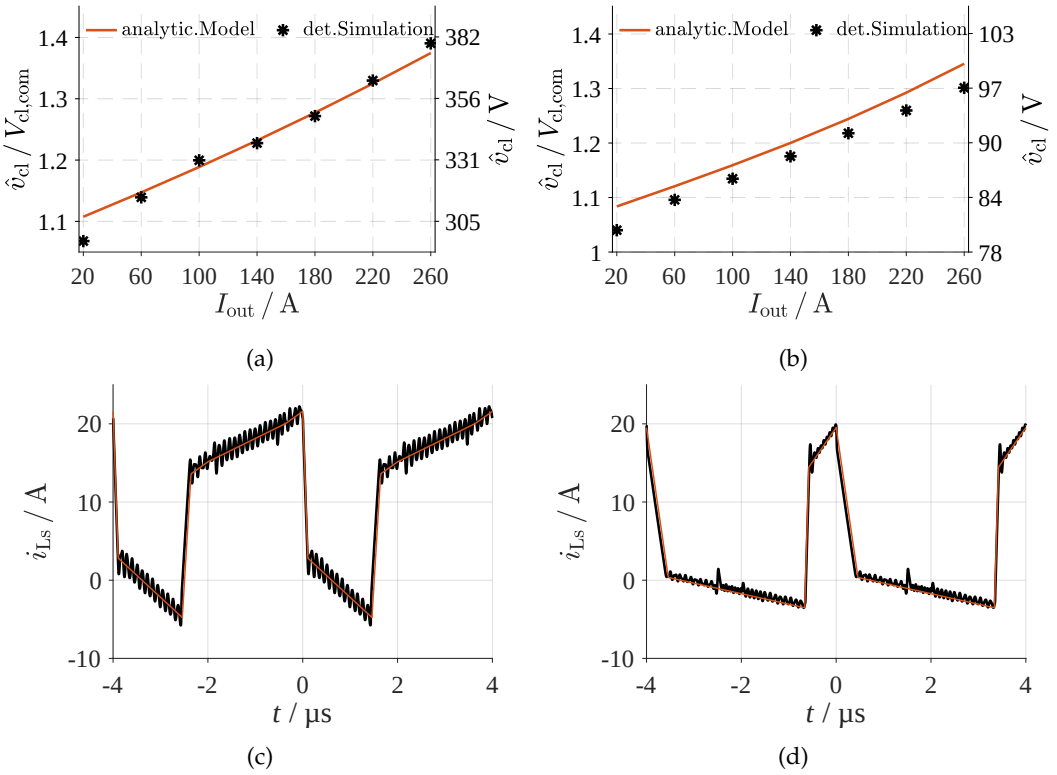


FIGURE 2.92: Validation of the clamp capacitor voltage model in (a) secondary-series configuration (parameters: $\text{Config}_{2.2l}$) and (b) secondary-parallel configuration (parameters: $\text{Config}_{2.2m}$). Modeled and simulated primary transformer currents for (c) the parameters $\text{Config}_{2.2n}$ (secondary-series) and (d) the parameters $\text{Config}_{2.2o}$ (secondary-parallel).

of the secondary-parallel operation is depicted in Figure 2.92b. The primary current of the maximum-load operation is depicted for the secondary-series and secondary-parallel operation in Figures 2.92c and 2.92d respectively.

All results show that the analytical model fits the simulation results very well. The error of the clamp capacitor voltage is below 5 % and the current shape is modeled very accurately. These results show that the model is feasible to be used in the design process of the converter.

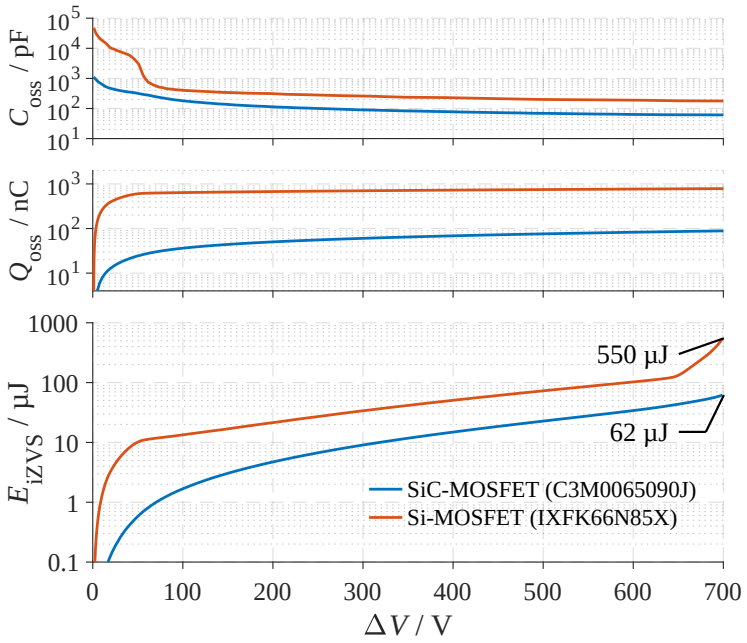


FIGURE 2.93: Voltage-dependent output capacitance C_{oss}, output charge Q_{oss} and incomplete ZVS losses E_{iZVS} for silicon (Si) and SiC semiconductors.

2.2.4 Zero-voltage switching analysis

this section has been previously published in parts in [Reh+22a].

Wide-bandgap semiconductors enabled the ACFC to achieve ZVS more easily and limit potential turn-on losses when switching with a residual voltage ΔV because the output capacitance is much smaller compared to semiconductors made of silicon - the circuit needs to provide a much smaller commutation charge to discharge the output capacitance of the switches. Figure 2.93 shows, for comparison, the output capacitance, output charge, and incomplete ZVS losses of an 850 V silicon MOSFET (IXFK66N85X, [IXY16]) and a 900 V SiC MOSFET (C3M0065090J, [Cre19a]) over the input/residual voltage. At a voltage of 700 V, the output charge is about nine times larger for the silicon switch compared to the SiC version. The same applies for the incomplete ZVS losses, which were calculated using [Kas+16] for an input voltage of 700 V. The analysis shows that silicon-carbide MOSFETs present an overwhelming advantage when using active-clamp converters as the series inductor L_s needs to provide a much smaller energy to discharge the output capacitor of the main and auxiliary switch. Considering the discharge of the main switch, the energy of the series inductor can be calculated as

$$E_{Ls} = \frac{1}{2} L_s \check{i}_{mag}^2. \tag{2.103}$$

Considering the discharge of the auxiliary switch, the energy can be calculated with the magnetizing current and output current as

$$E_{Ls} = \frac{1}{2} L_s (\hat{i}_{mag} + \hat{i}'_{Lg})^2. \tag{2.104}$$

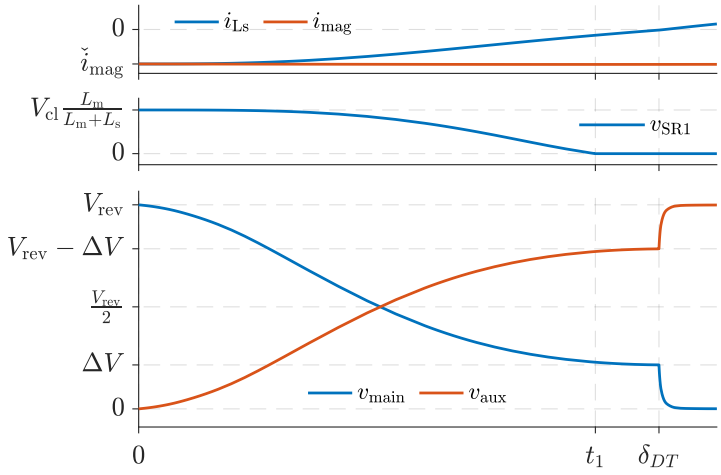


FIGURE 2.94: Exemplary simulated incomplete ZVS operation (parameters: $\text{Config}_{2.2p}$).

The analysis of (2.2.1) showed that the current amplitude of the energy in (2.104) is always larger compared to (2.103) because the current amplitude of the output inductor adds to the maximum magnetizing current. ZVS is, therefore, harder to achieve for the main switch than for the auxiliary switch. The following analysis will, therefore, focus on the switching behavior of the main switch. Considering (2.104), zero-voltage switching can be achieved for the main switch with a small minimum magnetizing $\check{i}_{mag}$[1], which can be decreased by designing the magnetizing inductance L_{mag} smaller or through a large series inductance L_s. For the design of the active-clamp converter, it is vital to design these system components properly to avoid large switching losses at full or partial load. The analysis of the switching transition is divided into two parts. In Section 2.2.4A, the conventional switching transition is analyzed while Section 2.2.4B considers the special case, where ZVS may be naturally achieved.

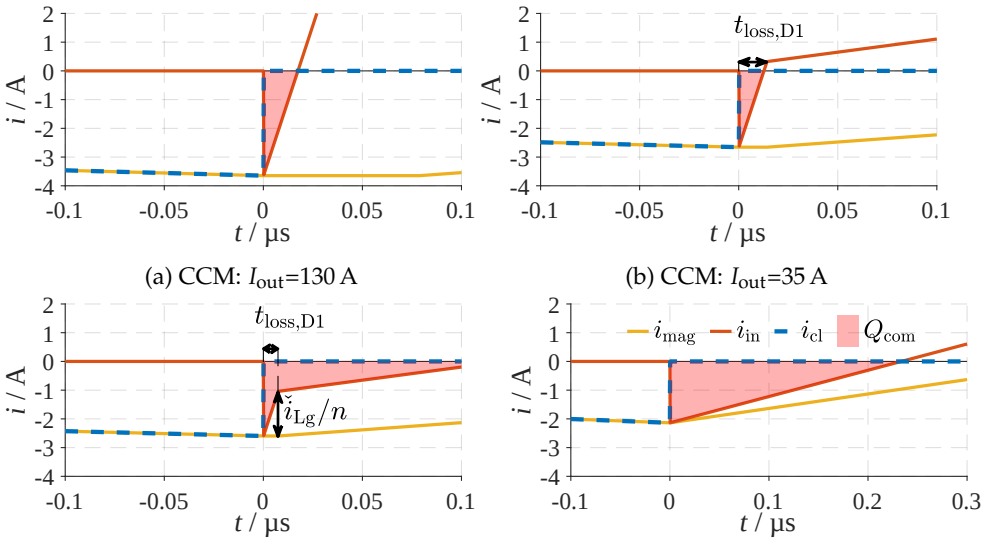
A Conventional switching transition

In [Kas+16], a ZVS condition and a method to calculate the residual voltage are derived for galvanically-coupled converters. However, as the ACFC is a galvanically-isolated converter - the output capacitance of the secondary diodes/synchronous rectifiers participates in the switching transition, this method cannot be applied because two non-linear capacitors cannot be considered[2]. In [Lin+06], the switching behavior was analyzed by considering a circuit composed of the magnetizing inductance L_m, the series inductance L_s and the output capacitance of the main switch $C_{oss,S1}$ and solving the differential equations. In this analysis, the output capacitance of the auxiliary switch $C_{oss,S2}$ and the synchronous rectifier $C_{oss,SR1}$ were disregarded while $C_{oss,S1}$ was considered constant.

Figure 2.94 shows an exemplary switching transition. The simulation results, which considered the non-linear output capacitance of the primary *and* secondary

[1] in steady-state, the mean magnetizing current is negative.

[2] in [Kas+16] the residual voltage was calculated by assuming an energy balance before and after the switching transition, which could be solved for the residual voltage ΔV, while assuming i_{Ls} zero. For galvanically coupled converters, this is not possible. Besides ΔV, the transition has to be solved for i_{mag} and v_{SR1}, which can only be done numerically through a step-wise solution of the differential equations.



(a) CCM: I_{out}=130 A (b) CCM: I_{out}=35 A

(c) CCM: I_{out}=25 A (d) DCM: I_{out}=10 A

FIGURE 2.95: Simplified simulation of the ACFC in (a) CCM (parameters: $\text{Config}_{2.2q}$), (b) CCM with intermediate output current (parameters: $\text{Config}_{2.2r}$), (c) low output current (parameters: $\text{Config}_{2.2s}$) and (d) DCM (parameters: $\text{Config}_{2.2f}$).

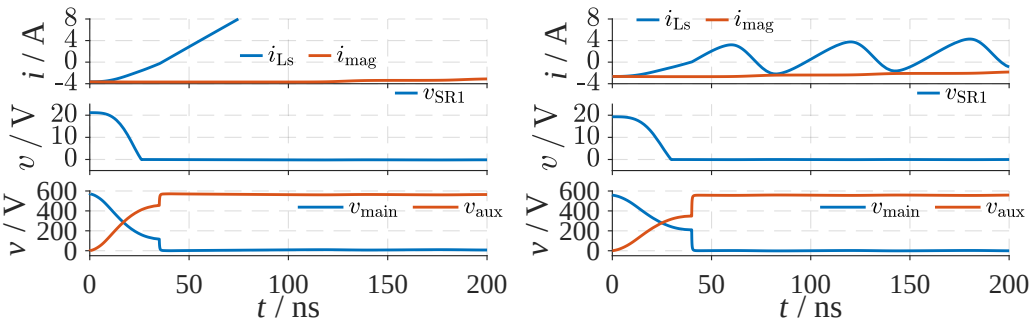
semiconductors, show that i_{Ls} increases immediately after turn-off of S_2 while i_{mag} stays nearly constant. During the dead time, the voltage applied to the magnetizing inductance is nv_{SR1}. Due to the large inductance, the current changes insignificantly. This shows that L_{m} does not participate in resonance. As depicted in Figure 2.93, the output capacitance $C_{\text{oss,S1}}$ is highly non-linear such that it cannot be considered constant and the capacitance of the auxiliary switch $C_{\text{oss,S2}}$ should not be disregarded to avoid large errors. It is, therefore, not possible to consider the switching transition as a resonant transition consisting of constant elements.

The most accurate method for calculating the residual voltage ΔV and therewith the incomplete ZVS losses is to simulate the transition while considering the non-linear output capacitors of the primary switches and rectifiers. However, this is very time consuming while designing the converter and considering hundreds of circuit designs in combination with several different semiconductors.

B ZVS at low output currents

When reducing the output current, the minimum magnetizing current $\check{i}_{\text{mag}}$ increases because the charge Q_{cl1} (Figure 2.83) reduces due to the lower transferred current. This means that there is less energy available to achieve ZVS of the main switch effectively, resulting in an increased residual voltage ΔV. However, if the output current is sufficiently low, the commutation charge Q_{com} increases, facilitating ZVS and reducing the residual voltage. This is caused by the fact that primary current slope $\dot{i}_{\text{Ls}}$ is much larger in the interval $t_{\text{loss,D1}}$ than in the interval $t_{\text{ON,D1}}$ (Section 2.2.1). If the transformer current i_{Ls} is negative at the end of the interval $t_{\text{loss,D1}}$, the commutation charge is significantly increased.

Figure 2.95 shows simplified simulations of the ACFC at the same input and output voltage for the same set of parameters at different output currents. While the commutation charge decreases for an output current of $I_{\text{out}} = 35\,\text{A}$ (Figure 2.95b)



(a) CCM: I_{out}=130 A

(b) CCM: I_{out}=35 A

(c) CCM: I_{out}=25 A

(d) DCM: I_{out}=10 A

FIGURE 2.96: Simulation of the ACFC in (a) CCM at a large output current (parameters: $\text{Config}_{2.2q}$), (b) CCM with an intermediate output current (parameters: $\text{Config}_{2.2r}$), (c) CCM with a low output current (parameters: $\text{Config}_{2.2s}$) and (d) DCM (parameters: $\text{Config}_{2.2t}$); all simulations with nonlinear parasitics included. Semiconductors with nonlinear output capacitance considered. Semiconductor selection: $\text{Config}_{2.2u}$.

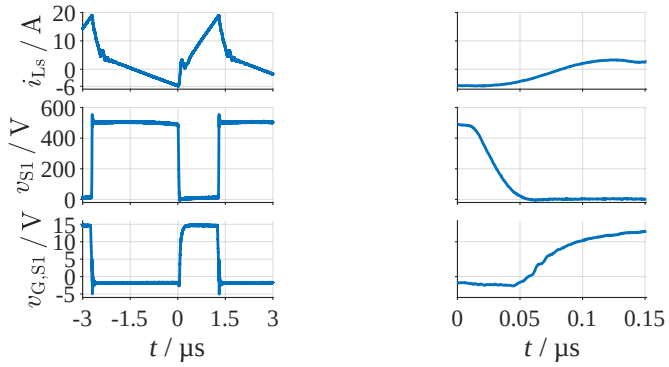
compared to the case of $I_{out} = 130\,\text{A}$ (Figure 2.95a), the charge increases significantly for Figure 2.95c and Figure 2.95d. Considering the above description and simulations, the output current where ZVS is most critical to achieve is given at the condition

$$\check{i}_{mag} + \frac{\check{i}_{Lg}}{n} = 0, \tag{2.105}$$

where the output current can be calculated using the derived model (Section 2.2.1).

Simulations with the output capacitance of the primary and secondary semiconductors are provided in Figure 2.96. The results show that the residual voltage increases significantly from Figure 2.96a to 2.96b whereas for ZVS is automatically achieved for the cases Figure 2.96c and 2.96d. It is, thus, critical to design the converter for the condition (2.105) and to carefully choose the dead time to achieve ZVS in all operating points.

It has been tested whether the converter achieves ZVS for the nominal operating point at ($V_{in} = 345\,\text{V}$, $V_{out} = 14\,\text{V}$, $I_{out} = 64\,\text{A}$). Figure 2.97a shows the nominal operation with the drain-source v_{S1} and gate voltage $v_{G,S1}$ of the main switch S_1 and the primary transformer current i_{Ls}. Figure 2.97b shows a zoom to the switching transient. It is evident that ZVS was achieved and that the transformer current is still negative when the drain-source voltage v_{S1} reaches zero.



(a) (b)

FIGURE 2.97: ZVS analysis for the nominal operating point measured on the prototype of Figure 3.23c. (a) Measured operation and (b) zoom to the switching transient.

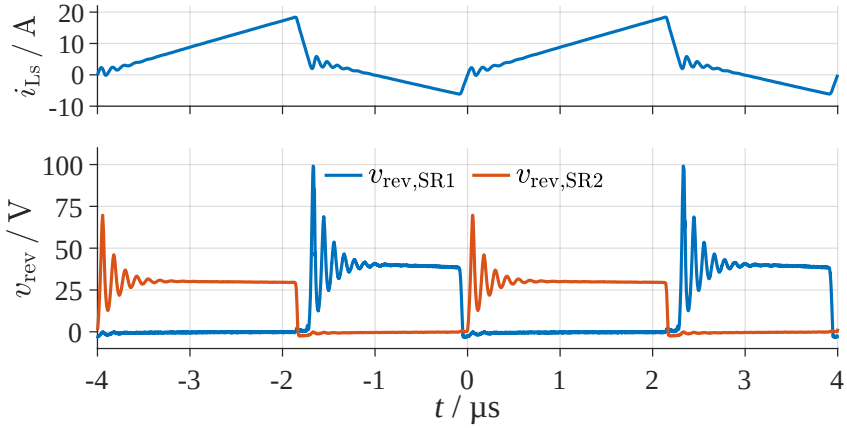


FIGURE 2.98: Measurement of the conventional blocking voltage shape of the synchronous rectifiers with no snubber attached (parameters: $\text{Config}_{2.2v}$).

2.2.5 An active snubber for limitation of the rectifier over voltages

this section has been previously published in parts in [Kor+21]. *the concept was analyzed and evaluated in the thesis* [Kor20b], *which was supervised and proposed by the author. The presented method has been applied for patent in* [Reh+21a].

Considering the low-voltage, high-current application discussed in this thesis, the application of synchronous rectifiers on the secondary side is mandatory. These MOSFETs have a considerable output capacitance usually much larger compared to power diodes for such applications. Together with the unpreventable and necessary leakage inductance of the transformer, the output capacitance forms a resonant circuit leading to an overshoot in the blocking voltage of the rectifiers. Additionally, the synchronous rectifiers are actively pulsed such that a turn-off at a large current can not necessarily be avoided due to the significant current slopes $\mathrm{d}i/\mathrm{d}t$. The current is, thus, flowing through the body diode, such that the reverse-recovery effect further amplifies the voltage overshoot. Compared to the LLC, which is a voltage-fed topology where the output capacitance acts as a large lossless snubber, the ACFC is a current-fed topology with no capacitance to reduce the overshoot. Therefore, all topologies with an inductor on the secondary side suffer from large output voltage overshoots at the synchronous recifiers regardless whether the rectification is active or passive [Esc+20; KDG95; MWS89; PJ01; RSB90; Wan+17; ZRG12].

Exemplary waveforms of the blocking voltages and the primary transformer current i_{tr} are depicted in Figure 2.98 showing a considerable overshoot of 150 % compared to the steady-state blocking voltage[1]. The measurements were performed at an input voltage of 220 V and an output current of only 65 A. An operation at larger input voltages and output currents was not possible due to the significant blocking

[1] for a constant capacitance, the overshoot would not surpass 100 % of the blocking voltage. The overshoot of 150 % is a consequence of the voltage-dependency of the output capacitance, which is large for small voltages. For large voltages, however, the capacitance becomes smaller, further amplifying the overshoot.

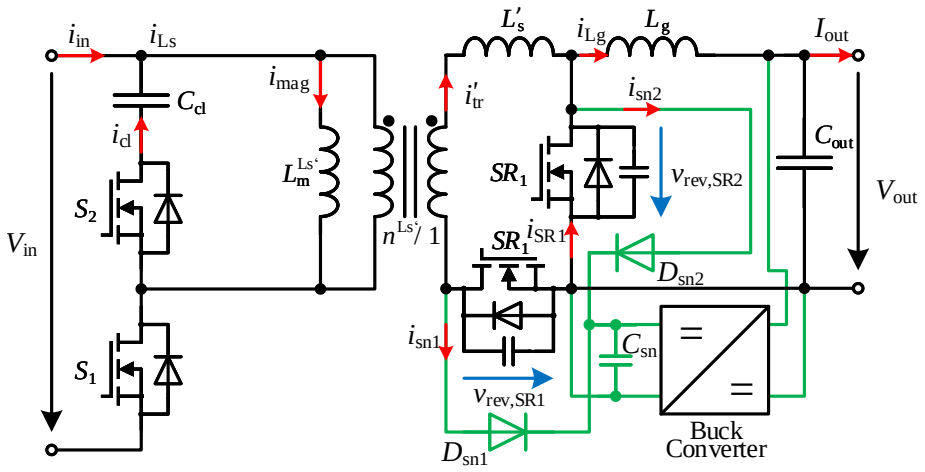


FIGURE 2.99: ACFC with proposed snubber in green. Compared to Figure 2.76, the series inductance L_s was transferred to the secondary side to L'_s such that the magnetizing inductance was altered to $L_m^{Ls'}$ and the transformation ratio was altered to $n^{Ls'}$.

voltages that already reach the maximum blocking voltages allowed for the synchronous rectifiers (*IAUT300N10S5N015*).

In many cases, output voltage overshoots of active or passive devices are damped using *RC* or *RCD* snubbers where the energy of the overshoot is transferred to the capacitance of the snubber *C* to be dissipated in the resistive component *R*. However, as this section will analyze, the energy of the overshoot can be as large as 80 µJ leading to a continuous power consumption of 20 W if the converter is operated at 250 kHz. Obviously, the snubber resistor would need to be set-up by power resistors with special emphasis on the heat dissipation while the power loss results in a substantial decrease of the system efficiency. Thus, authors have come up with a number of different loss-less snubber topologies in preceding publications [DMS98; Lin+19b; Sab+91a; SDM02; Zai17; ZYL04]. However, neither of the described topologies is applicable to the high-power ACFC as they employ additional components in the power path [Lin+19a], suffer from a complex structure with a high component count [ZYL04; DMS98; SDM02], or were designed for other rectifier topologies [Zai17; Sab+91a]. Consequently, the author of this thesis proposes a novel regenerative snubber employing few components with no additional components in the power path. The idea has been proposed by the author during the completion of the supervised master thesis in [Kor20b] and has consequently been applied for patent in [Reh+21a]. The proposed snubber was first published to a wider audience by *Korthauer, Rehlaender, et al.* in [Kor+21].

The proposed snubber is depicted in Figure 2.99. It consists of two snubber diodes D_{sn1} and D_{sn2}, a common snubber capacitor C_{sn} and a buck converter that feeds to the output V_{out}. The buck converter, which may or may not be isolated, controls the voltage of the snubber capacitor defining a clamping level for the reverse voltages $v_{rev,SR1}$ and $v_{rev,SR2}$. Additionally, the clamping level can be used to demagnetize the output inductance when a reverse power flow is necessary (i.e. to precharge the input capacitor). This method was already described in [Reh+21a].

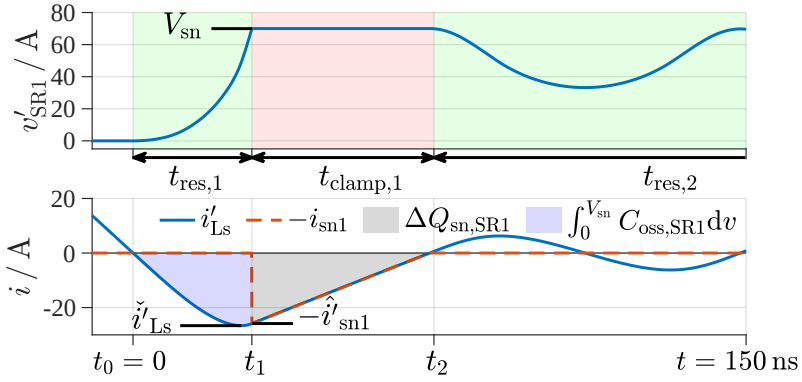
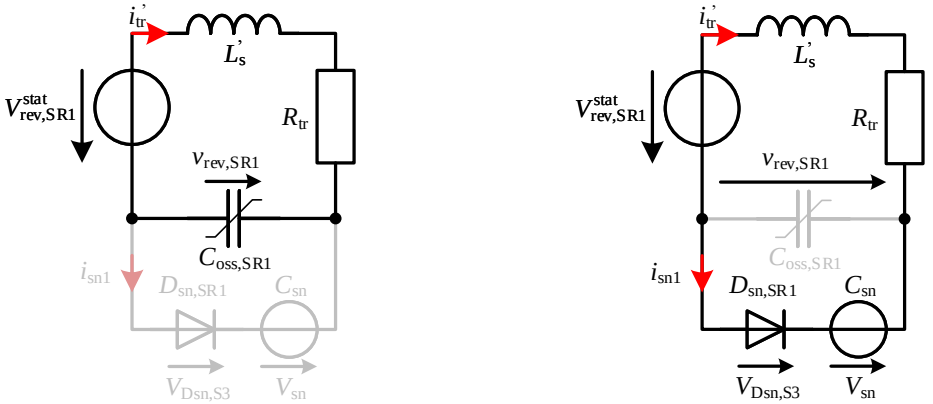


FIGURE 2.100: Exemplary current and voltage shapes of the snubber operation. The operation consists of two resonant intervals depicted in green and a clamping interval depicted in red. The clamping interval is entered when the output capacitance is charged to V_{sn}. During the clamping interval, the snubber diode D_{sn1} is conducting the current i_{sn1} and the charge $\Delta Q_{sn,SR1}$ is delivered to the snubber capacitance C_{sn} (parameters: Config$_{2.2w}$).

A Snubber analysis

The behavior of the snubber was analyzed through a simulation that includes the voltage-dependent output capacitance of the secondary-side rectifiers and the series inductance of the transformer. An exemplary waveforms of the blocking voltage v_{SR1} and the secondary-side transformer current i'_{tr} are depicted in Figure 2.100. The snubber operation can be divided into three intervals: the first resonant interval $t_{res,1}$, the clamping interval $t_{clamp,1}$ and the second resonant interval $t_{res,2}$. The resonant intervals are depicted in green, the clamping interval is depicted in red. For $t < t_0$, the converter operates in the $t_{loss,D2}$ interval, which is described in Section 2.2.1C. After this interval, the secondary-side transformer current reaches zero ($i'_{tr} = 0$) entering the first resonant interval lasting for $t_{res,1}$ and charging the output capacitance from $v_{SR1} = 0$ to V_{sn}. As soon as the blocking voltage reaches the clamping voltage V_{sn}, the converter enters the clamping interval lasting for $t_{clamp,1}$ where the blocking voltage is clamped to the voltage V_{sn}. During this interval, the charge $\Delta Q_{sn,SR1}$ is transferred to the snubber capacitance C_{sn}. When the secondary-side transformer current finally reaches zero again, the converter enters the second resonant interval.

A1 Resonant interval During the resonant intervals, the circuit can be modeled using the equivalent circuit depicted in Figure 2.101a. It is modeled by a secondary-side leakage inductance L'_s by transforming the conventional transformer stray inductance model, which was used during the modeling process in Sections 2.2.1 and 2.2.2, to the secondary side. During this transformation, the magnetizing inductance is also altered to $L_m^{Ls'}$ as depicted in Figure 2.99. The series inductance L'_s, in combination with the voltage-dependent synchronous rectifier output capacitance $C_{oss,SR1}$ forms a resonant circuit, which is depicted in the equivalent circuit of Figure 2.101a. The resistance R_{tr} models the damping of the oscillation and $V_{rev,SR1}^{stat}$ models the steady-state blocking voltage, which can be calculated as $V_{rev,SR1}^{stat} = \frac{V_{cl}}{n^{Ls'}} = \frac{V_{cl}}{n} \frac{L_m}{L_m + L_s}$ (*see* Section 2.2.1). Due to the large value of C_{sn} ($C_{sn} \gg C_{oss,SR1}$), the snubber voltage is modeled as a voltage source. Therefore, the second-order differential equation



(a) Resonant interval (b) Clamp interval

FIGURE 2.101: Equivalent circuit diagrams during the resonant interval (a) and clamping interval (b).

$$-V_{rev,SR1}^{stat} = L_s' \frac{d^2 Q_{oss,SR1}(t)}{dt^2} + R_{tr} \frac{dQ_{oss,SR1}(t)}{dt} + v_{rev,SR1}(t) \tag{2.106}$$

can be derived with

$$C_{oss,SR1}(v_{rev,SR1}(t))\, v_{rev,SR1}(t). \tag{2.107}$$

The voltage dependency of the output capacitance must not be neglected such that (2.106) becomes nonlinear, which prevents an analytical solution. However, as shown in [Kor+21], the equation can be solved iteratively by assuming a constant capacitance $C_{oss,SR1}(v_{rev,SR1}(t_{res,i-1,SR1}))$ for each time instant. The equation, therefore, becomes linear for each time instant, such that specific solution can be found for each time instance $t_{res,i,SR1}$. The results are, thus, the initial condition for the next time instance.

The initial time instant is $t_0 = 0$ with $v_{rev,SR1}(t_0) = 0$ and $i_{tr}'(t_0) = 0$. However, by considering an ideal synchronous rectifier operation, the reverse-recovery effects of the body diode are neglected. Since the converter is operated with large output currents and high current slopes, a significant reverse recovery current $\hat{i}_{rr,bd}$ of the body diode must be considered as

$$\hat{i}_{rr,bd} = \sqrt{Q_{rr,SR1} \frac{V_{rev,SR1}^{stat}}{L_s'}}. \tag{2.108}$$

The reverse recovery charge $Q_{rr,SR1}$ hereby depends on the current slope, the dynamic of the diode and the conducted current [MUR03]. For this analysis the datasheet value is used, which tends to be too large [MG12].

A2 Clamping interval When $v_{rev,SR1}$ reaches the snubber voltage V_{sn}, the diode $D_{sn,SR1}$ starts conducting and clamps the reverse voltage $v_{rev,SR1}$ to the snubber voltage V_{sn}. The equivalent circuit during this clamp interval ($t_1 < t \leq t_2$, cf. Figure 2.100) is depicted in Figure 2.101b. The current i_{Ls}' increases until it reaches zero. The current shape can be expressed using the differential equation

$$\frac{\mathrm{d}i'_{\mathrm{tr}}}{\mathrm{d}t} = \frac{-V^{\mathrm{stat}}_{\mathrm{rev,SR1}} + V_{\mathrm{sn}} - i'_{\mathrm{tr}} R_{\mathrm{tr}}}{L'_{\mathrm{s}}}. \tag{2.109}$$

The initial condition, the current $i'_{\mathrm{Ls}}(t_1)$, is hereby the solution of the last iteration of the preceding resonant interval. It is the maximum current value $-\hat{i}'_{\mathrm{sn1}}$ of the snubber diode. In the clamping interval, the current i'_{tr} increases with a constant slope until it reaches zero[1].

B Snubber design

The snubber circuit needs to transfer the charge that is delivered to the snubber capacitor during the clamping intervals at the turn-off of the synchronous rectifiers SR_1 and SR_2. During each period, the charge delivered to the snubber capacitor is

$$\Delta Q = \Delta Q_{\mathrm{sn,SR1}} + \Delta Q_{\mathrm{sn,SR2}} \tag{2.110}$$

amounting to an average input current of $\bar{i}_{\mathrm{sn,in}} = \Delta Q f_{\mathrm{sw}}$ with the input power

$$P_{\mathrm{sn,in}} = \bar{i}_{\mathrm{sn,in}} V_{\mathrm{sn}} = (\Delta Q_{\mathrm{sn,SR1}} + \Delta Q_{\mathrm{sn,SR2}}) f_{\mathrm{sw}} V_{\mathrm{sn}}. \tag{2.111}$$

The output current can be calculated with the snubber efficiency $\eta_{\mathrm{sn,conv}}$ as

$$I_{\mathrm{sn}} = \eta_{\mathrm{sn,conv}} \frac{P_{\mathrm{sn,in}}}{V_{\mathrm{out}}}. \tag{2.112}$$

It is evident that the output current strongly depends on the operating point and shows a large dependency on the output voltage. Thus, for the lowest output voltage, the snubber circuitry is stressed the most. Considering the simulation results, the snubber has been designed for a maximum output power of 30 W yielding a maximum output current of 4 A.

C Experimental validation

Experimental measurement results of the active-clamp converter with and without the active snubber are depicted in Figure 2.102. Figure 2.102a shows a light-load low-input-voltage operating point without an active snubber. The measurement results show large overshoots of the blocking voltage, which are as high as the rated blocking voltage of the synchronous rectifiers ($-v_{\mathrm{SR}}^{\mathrm{max}} = 100\,\mathrm{V}$) that result from the nonlinear output capacitance of the MOSFETs and the stray inductance of the transformer. In comparison to this measurement, Figure 2.102b shows a measurement with the active snubber, which is operated at $f_{\mathrm{snub}} = 500\,\mathrm{kHz}$ and a buck-converter current of $\hat{i}_{\mathrm{buck}} = 1\,\mathrm{A}$. The average buck-converter current is about $\bar{i}_{\mathrm{buck}} = 350\,\mathrm{mA}$ amounting to a transferred power of $P_{\mathrm{buck}} = \bar{i}_{\mathrm{buck}} V_{\mathrm{out}} = 5.6\,\mathrm{W}$. The efficiency of the converter was $\eta = 94.89\,\%$ without the snubber and $\eta = 94.95\,\%$ with the snubber active. The operation, thus, led to a slight inprovement of the conversion efficiency.

The worst-case full-load operating point of the snubber is depicted in Figure 2.102c. The active-clamp converter is hereby operated at a minimum output voltage of $V_{\mathrm{out}} = 7.5\,\mathrm{V}$ and a maximum input voltage of $V_{\mathrm{in}} = 420\,\mathrm{V}$ at an output current of $I_{\mathrm{out}} = 160\,\mathrm{A}$, stressing the snubber the most. Considering the large buck-converter

[1] the resistance R_{tr} and the resistive component of the diode in reality result in an actual exponential decay. However, as the time constant is large, this is not visible in the simulation of Figure 2.100.

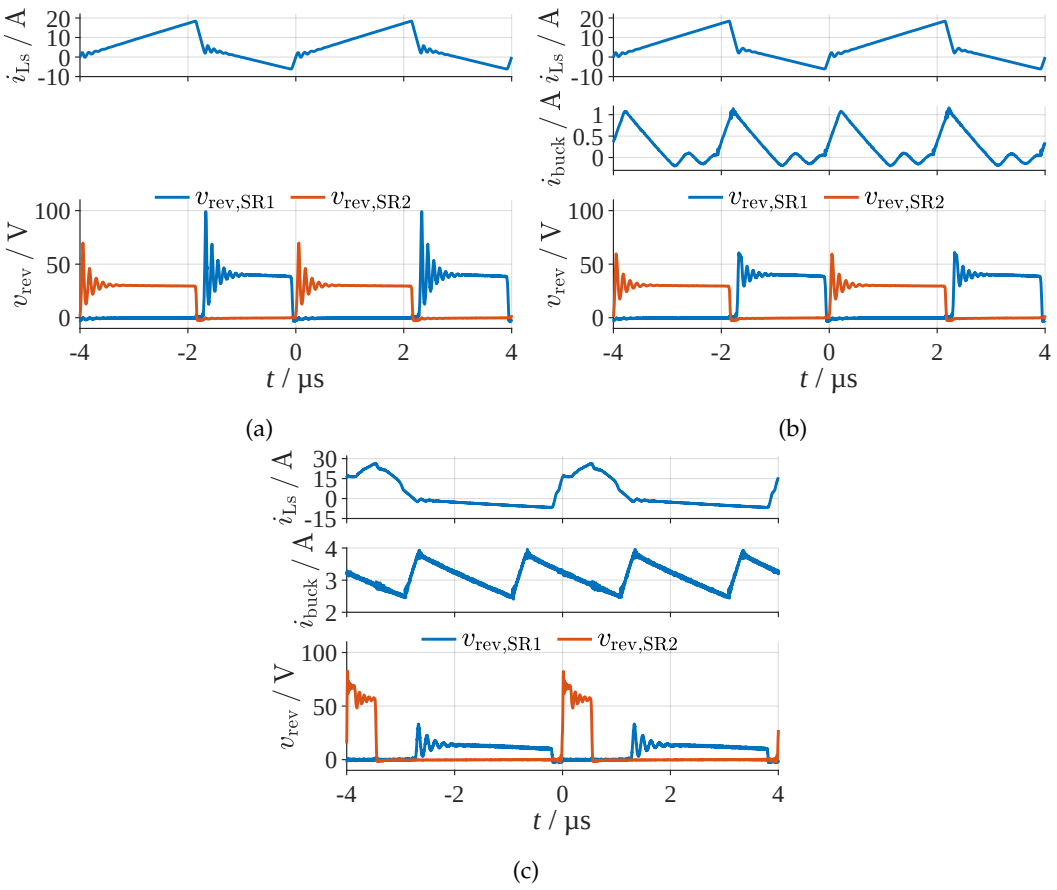
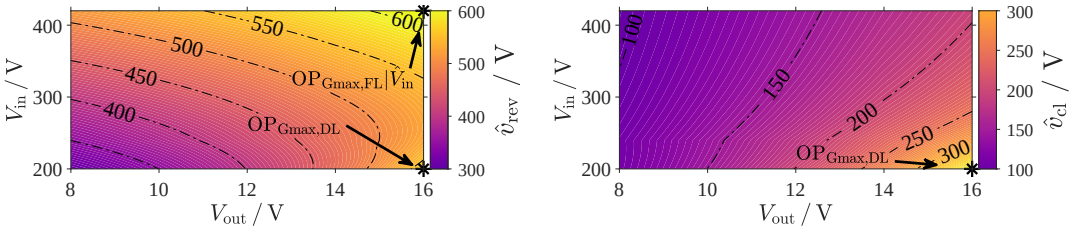


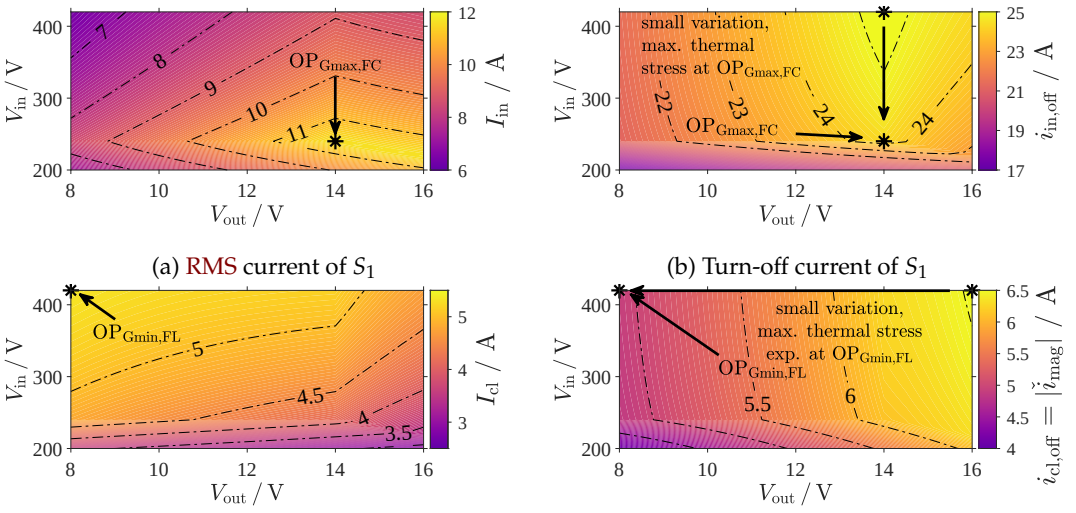
FIGURE 2.102: Experimental measurement results for a light-load operation without an employed snubber (a, parameters: $\text{Config}_{2.2v}$), the same operating point with snubber (b, parameters: $\text{Config}_{2.2x}$) and a full-current low-gain operation (c, parameters: $\text{Config}_{2.2y}$).

current of $\bar{i}_{\text{buck}} = 3.2\,\text{A}$, the transferred power is $P_{\text{buck}} = 24\,\text{W}$ emphasizing the above analysis that the necessary snubber power is too large to be handled by a conventional RC(D) snubber as this would degrade the converter efficiency and make bulky snubber resistors necessary.



(a) (b)

FIGURE 2.103: (a) Maximum reverse voltage $\hat{v}_{rev}$ and (b) maximum clamp capacitor voltage $\hat{v}_{cl}$ in dependency of the input and output voltage.



(a) RMS current of S_1 (b) Turn-off current of S_1

(c) RMS current of S_2 (d) Turn-off current of S_2

FIGURE 2.104: (a,b) Stress values for the main switch S_1 (a) maximum steady-state RMS current I_{in} (b) largest steady-state turn-off current $i_{in,TO}$. (c,d) Stress values for the auxiliary switch S_2 (c) maximum steady-state RMS current I_{cl} (d) highest steady-state turn-off current $i_{cl,TO}$, which is equal to the absolute minimum magnetizing current $|\check{i}_{mag}|$

2.2.6 Definition of characteristic design operation points

To design the active clamp converter, it is necessary to know the characteristic operating points maximizing the specific stress values of the circuit components. The circuit components need to be designed for these specific operating points to avoid over temperatures. For the primary power switches, there are two major loss mechanisms: the conduction losses and the turn-off losses. Since the switching frequency is relatively constant, it is sufficient to analyze the turn-off and the RMS currents to find the operating points with the highest power loss. For the analysis, a sample set of parameters is selected: Config$_{2.2z}$.

The maximum reverse voltage and maximum clamp capacitor voltage are depicted in Figure 2.103a and Figure 2.103b respectively. Figure 2.104a and Figure 2.104b show the RMS current I_{in} and the turn-off current $i_{in,TO}$ respectively for the main switch S_1. The operating point with the largest stress is OP$_{Gmax,FC}$. In this operating point, the conduction losses are at its maximum while the switching losses in this operating point vary little from the largest. For the auxiliary switch S_2, the operation point with the largeest thermal stress is OP$_{Gmin,FL}$ (cf. Figures 2.104c and 2.104d).

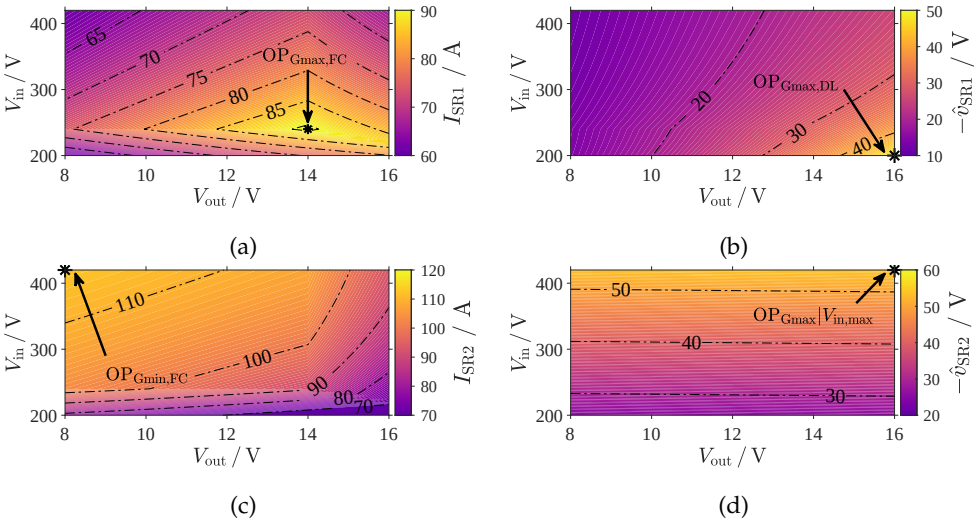


FIGURE 2.105: (a-d) Stress values for the synchronous rectifier: (a) maximum steady-state RMS current I_{SR1}, (b) maximum steady-state blocking voltage $-\hat{v}_{SR1}$, (c) maximum steady-state RMS current I_{SR2}, (d) maximum steady-state blocking voltage $-\hat{v}_{SR2}$.

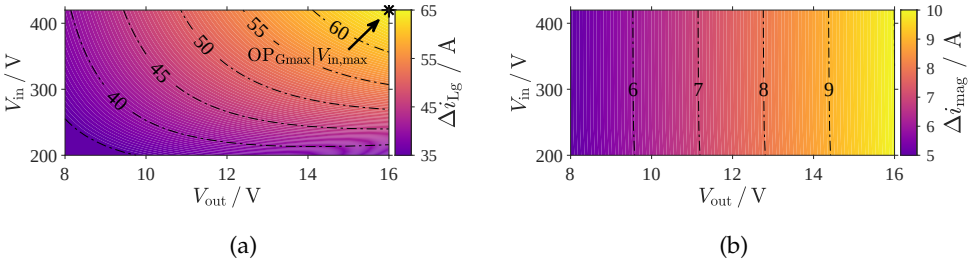


FIGURE 2.106: Maximum ripple of the output inductor current Δi_{Lg} and magnetizing current ripple Δi_{mag}.

In this operating point, the RMS current is at its maximum (cf. Figure 2.104c) and the turn-off current is relatively constant over the entire operation range and differs little from its maximum (cf. Figure 2.104d).

The stress values of the synchronous rectifiers are depicted in Figure 2.105. Figure 2.105a shows the RMS current over the entire operating range considering the maximum output current I_{out}. Figure 2.105b shows the maximum steady-state blocking voltage. $OP_{Gmax,DL}$ is the operating point with the maximum blocking voltage and $OP_{Gmax,FC}$ is the operating point with the maximum RMS current.

The maximum RMS current of SR_2 is depicted in Figure 2.105c; the worst-case operating point is an operation of the minimum gain – $OP_{Gmin,FC}$. The maximum blocking voltage is depicted in Figure 2.105d. The worst-case operating point is

TABLE 2.8: Operating points with the maximum component stress

Abbreviation	OP (V_{in} ,V_{out} ,I_{out})	component
$OP_{Gmax,FC}$	240 V, 14 V, 130 A	SR_1, S_1
$OP_{Gmax,FL}\|\hat{V}_{in}$	420 V, 16 V, 114 A	T, L_g, V_{rev}, V_{SR2}
$OP_{Gmin,FC}$	420 V, 8 V, 130 A	SR_2, S_2
$OP_{Gmax,DL}$	200 V, 16 V, 100 A	C_{cl}, V_{SR1}

$OP_{Gmax}|V_{in,max}$. The ripple current of the converter is depicted in Figure 2.106. Figure 2.106a shows the current ripple of the output inductor L_g with the worst-case operating point $OP_{Gmax}|V_{in,max}$ and Figure 2.106b shows the current ripple of the magnetizing inductance – the maximum current ripple is given at the maximum output voltage V_{out}. Table 2.8 summarizes the aforementioned worst-case operating points of each circuit component.

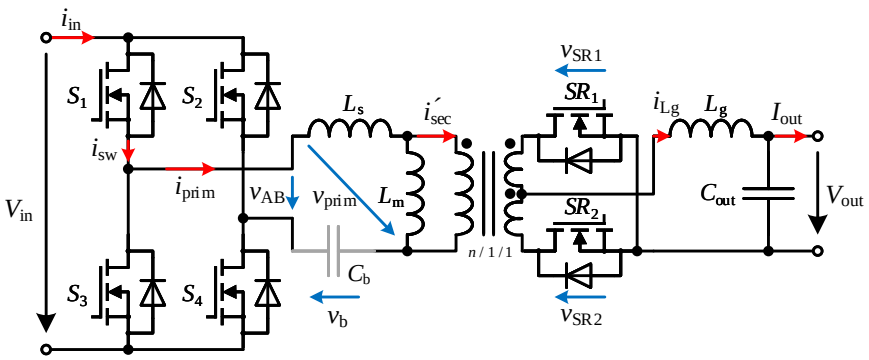


FIGURE 2.107: Circuit diagram of the isolated full-bridge converter.

2.3 Full-Bridge Converter

The isolated full-bridge converter is a widely popular power conversion topology and has been employed in a number of different applications with very high efficiencies. In phase-shift control, the topology was employed for decades [Zha+09b; Sab+91b; LSC15; BBK10b; BBK10a; BBK08]. The hard-switched full-bridge operation[1] results in iZVS losses. However, due to the outstanding performance of GaN and SiC switches, these losses may be tolerable enabling the topology for high-frequency applications [OKN21; RN17; RNN18]. Compared to the phase-shift operation, the primary currents may be significantly lower since there is no freewheeling interval.

2.3.1 Operating modes

The full-bridge converter can be operated in a number of different operating modes that result in different traits. The phase-shift operation can be used to achieve ZVS while resulting in large freewheeling currents that generate losses. The hard-switched full-bridge operation results in iZVS losses. However, for large input voltages, the blocking voltage of the SR MOSFETs may get large[2]. To lower the blocking voltages, the full-bridge converter can be operated in half-bridge mode where one MOSFET of one half bridge is continuously turned on and the two MOSFETs of the other bridge leg are pulsed. In this mode, the blocking voltages are half as large compared to the full-bridge operation.

A Phase-shift operation

To achieve ZVS, phase-shift modulation (cf. Figure 2.108) can be implemented where the gate signals of the two consecutive half bridges are phase shifted by a delay angle resulting in intervals where the inverter voltage is zero. During these intervals, the primary transformer current changes relatively slowly such that sufficient energy may be stored in the series inductor[3] to achieve ZVS for the leading leg switches.

[1] in this type of modulation, the switches are turned on at a residual voltage as there is no current flowing on the primary side before turn-on. This type of turn-on will be designated incomplete zero-voltage switching (iZVS).

[2] since the full-bridge converter is a buck topology only, the transfer ratio of the transformer must also be designed relatively small adding to the voltage stress.

[3] or stray inductance.

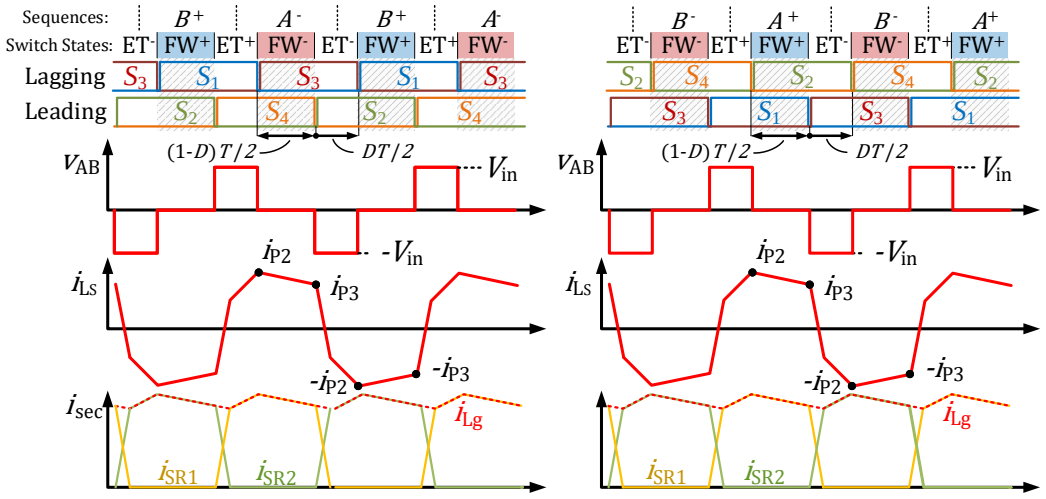
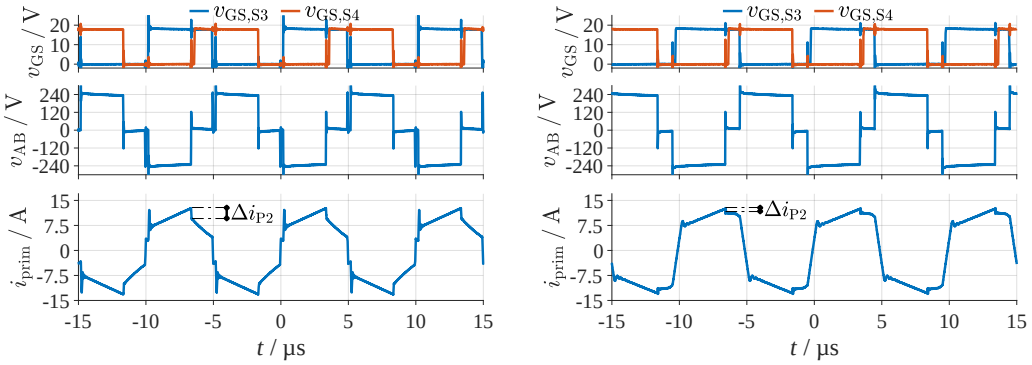


FIGURE 2.108: Current shape of the isolated full-bridge converter in phase-shift operation with inverter voltages and transformer current. Left: leading leg: S_2 and S_4; lagging leg S_1 and S_3. Right: leading leg: S_1 and S_3; lagging leg S_2 and S_4.

To refer to the topology of the isolated full-bridge converter with inductive termination in phase-shift operation, the topology will be designated PSFB. The freewheeling current results in conduction losses that may be detrimental to the converter efficiency. Furthermore, due to the significant output capacitance of the primary and secondary switches, the energy in the series inductance may not be sufficient such that additional measures need to be taken [CL10; JJ07; LC13; Lee+08; RBE93a; RBE93b; RBE94] to ensure ZVS for the primary (leading-leg) switches and avoid the large switching losses resulting from iZVS. An analysis of the loss mechanisms of the conventional phase-shift and the loss-balancing alternating asymmetrical phase-shift modulation were performed in Section 2.1.1A3. By employing the a²PSM, discussed in Section 2.1.1A4, the switching losses can be better distributed.

To accurately design the current shape of this modulation, modeling methods have been presented in [Cao14; BBK10b]. In [Cao14], the primary current during the freewheeling phase was modeled as the transformed secondary-side current i_{Lg}. In [BBK10b], the coupling coefficient of the two secondary windings was considered to accurately model the slope in the freewheeling phase. However, further parasitics influence the current shape. The secondary-side output capacitance of the rectifiers result in a steep current drop while entering the freewheeling interval and resistive elements in the primary circuit yield a further sharp drop of the current while being in the freewheeling phase. Both effects result in a reduced current value i_{P3}, which may prevent ZVS for the leading-leg switches when leaving the freewheeling phase. Two experimental measurement points of this effect are provided in Figure 2.109. Figure 2.109a shows a measurement with a small series inductance value L_s. This yields a large sudden current drop when entering the freewheeling interval. Furthermore, an exponential current decay can be recognized during the freewheeling phase. If the results are compared to the experimental results of Figure 2.109b, it is evident that the sudden drop and the exponential decay are much smaller. The effects can, therefore, be mitigated by choosing a large series inductance. However, this yields an increased duty-cycle loss interval eventually requiring smaller conversion ratios to achieve the maximum gain, which in turn increases the rectifier

blocking voltage. As the described effects are highly-dependent on the circuit parasitics, the conventional modeling procedure of [Cao14; BBK10b] will be adopted in this thesis.



(a) $L_s = 1\,\mu H$ (b) $L_s = 8.5\,\mu H$

FIGURE 2.109: Exemplary measurement results for the phase-shift modulation. (a) small series inductance resulting in large current drop Δi_{P2} in the freewheeling phase, (b) large series inductance yielding a small current drop Δi_{P2}. For (b), the duty-cycle loss intervals are increased yielding reduced freewheeling interval lengths (parameters: $\text{Config}_{2.3a}$, $\text{Config}_{2.3b}$).

B Hard-switched operation

this section has been previously published in parts in [Reh+22c].

The hard-switched full-bridge operation (cf. Figure 2.110) does not achieve ZVS. Instead the MOSFETs are turned on at a residual voltage resulting in iZVS losses. However, due to the outstanding performance of gallium-nitride (GaN) and silicon-carbide (SiC) switches, these losses may be tolerable enabling the topology for high-frequency applications [OKN21; RN17; RNN18]. To refer to the topology of the isolated full-bridge converter with inductive termination in hard-switched operation, this topology will be designated HSFB. Compared to the phase-shift operation, the primary currents may be significantly lower since there is no freewheeling interval. A general disadvantage of the isolated full-bridge converter is that the secondary-side rectifier MOSFETs must be dimensioned for the maximum transferred input voltage

$$v_{\mathrm{SR}} = k\frac{V_{\mathrm{in}}}{n} \tag{2.113}$$

where $k = 1$ for a full-bridge rectifier and $k = 2$ for the center-tapped rectifier. The conversion ratio n is hereby usually chosen to achieve the maximum necessary gain of the converter. For large input voltages, the blocking voltage of the SR MOSFETs or diodes may be intolerable, as diodes with a large blocking voltage need to be employed, increasing both the converter costs and losses. To lower the blocking voltages, the full-bridge converter can be operated in hard-switched half-bridge modulation (HHBM) where one MOSFET of one bridge leg is continuously turned on whereas the other MOSFET of the same bridge leg is turned off. The two MOSFETs of the other bridge leg are pulsed [JI15b]. This mode requires a blocking capacitor C_{b} (cf. Figure 2.107). This blocking capacitance is much larger than the resonant capacitance employed in an LLC, such that the capacitor is ideally charged to the average inverter voltage ($\bar{v}_{\mathrm{b}} = \bar{v}_{\mathrm{AB}}$). In this mode, the blocking voltages are half as large as in the full-bridge operation since the blocking capacitor C_{b} on the primary side absorbs half the input voltage V_{in}. The hard-switched half-bridge modulation is hereby very similar to the half-bridge modulation of the LLC, which was intensively covered in [IAP16; Wei+20c; Reh+20b; JI15a; JI16; Lia+10; RSB21] and presented in Section 2.1.1B. To distinguish both modulations, the half-bridge modulation of the isolated full-bridge converter will be referred to as HHBM. Together with the hard-switched full-bridge modulation (HFBM), the HHBM enables the converter for wide voltage-transfer ratio applications, where the HFBM is used for large voltage-transfer ratios and the HHBM is used for low voltage-transfer ratios. A disadvantage of this operating mode, however, is that it results in largely unbalanced losses. For that purpose, section Section 2.3.1C proposes a frequency-doubler modulation for the isolated full-bridge converter to better balance the losses of all switches. To the authors' knowledge, no such operation has yet been described for the isolated full-bridge converter. This modulation is hereby similar to the soft-switched frequency-doubler modulation of the LLC. However, it utilizes different pulse patterns. The frequency-doubler modulation of the LLC has been introduced in [IAP16; Lin+16; Wei+20c; WM20; WLM20b]. In Section 2.1.1B it was shown that the modulation has a superior influence on the junction temperature compared to the conventional HBM. To distinguish the soft-switched frequency-doubler modulation of the LLC from the proposed modulation for the isolated full-bridge converter, the

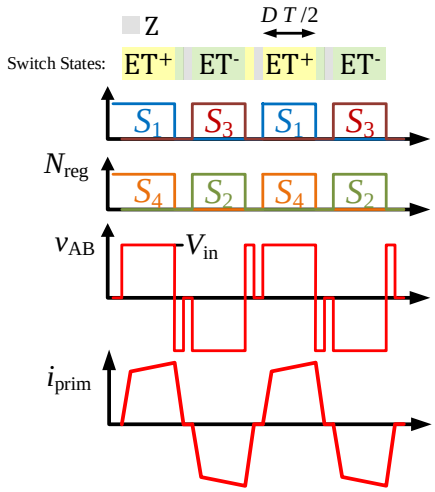


FIGURE 2.110: Hard-switched full-bridge modulation (HFBM) of the isolated full-bridge converter.

presented modulation will be referred to as hard-switched frequency-doubler modulation (HSFDM).

This section is structured as follows: Section 2.3.1B1 introduces the five different switching states and the conventional HFBM. Section 2.3.1B2 presents the four different hard-switched half-bridge modulations. Finally, Section 2.3.1C proposes the hard-switched frequency-doubler modulation and demonstrates its effectiveness on a laboratory prototype.

B1 Hard-switched full-bridge operation A full-bridge inverter is operated in four different switching states where either the channel or the diode is conducting. There are two energy-transfer (ET) states where energy is transferred from the source to the output or to the passive components, and two freewheeling states (FW) where no energy is transferred from the source to the output or to the passive components. The fifth state is the zero (Z) state where the primary current is zero ($i_{\text{prim}} \stackrel{!}{=} 0$) and at least three switches are turned off. The states are:

$$\begin{aligned}
\text{ET}^+ &: \quad S_1 \wedge S_4 \quad \Longrightarrow v_{\text{AB}} = V_{\text{in}}, \\
\text{ET}^- &: \quad S_2 \wedge S_3 \quad \Longrightarrow v_{\text{AB}} = -V_{\text{in}}, \\
\text{FW}^+ &: \quad S_1 \wedge S_2 \quad \Longrightarrow v_{\text{AB}} = 0, \\
\text{FW}^- &: \quad S_3 \wedge S_4 \quad \Longrightarrow v_{\text{AB}} = 0, \\
\text{Z} &: \quad i_{\text{prim}} \stackrel{!}{=} 0 \quad \Longrightarrow v_{\text{AB}} = v_{\text{b}}.
\end{aligned} \tag{2.114}$$

In the full-bridge operation only the two diagonal MOSFETs S_1-S_4 (and S_2-S_3) are turned on such that only the states ET^+ and ET^- are employed. During the turn-on, the primary transformer current increases to approximately the transformed output inductor current i_{Lg}/n. After the energy transfer to the output inductance L_{g}, all gate signals are low such that the primary current is forced through the body diode of the switches S_2-S_3 (and S_1-S_4) until the current reaches zero to enter the zero state Z. All switches remain switched off until the other two diagonal switches are eventually turned on.

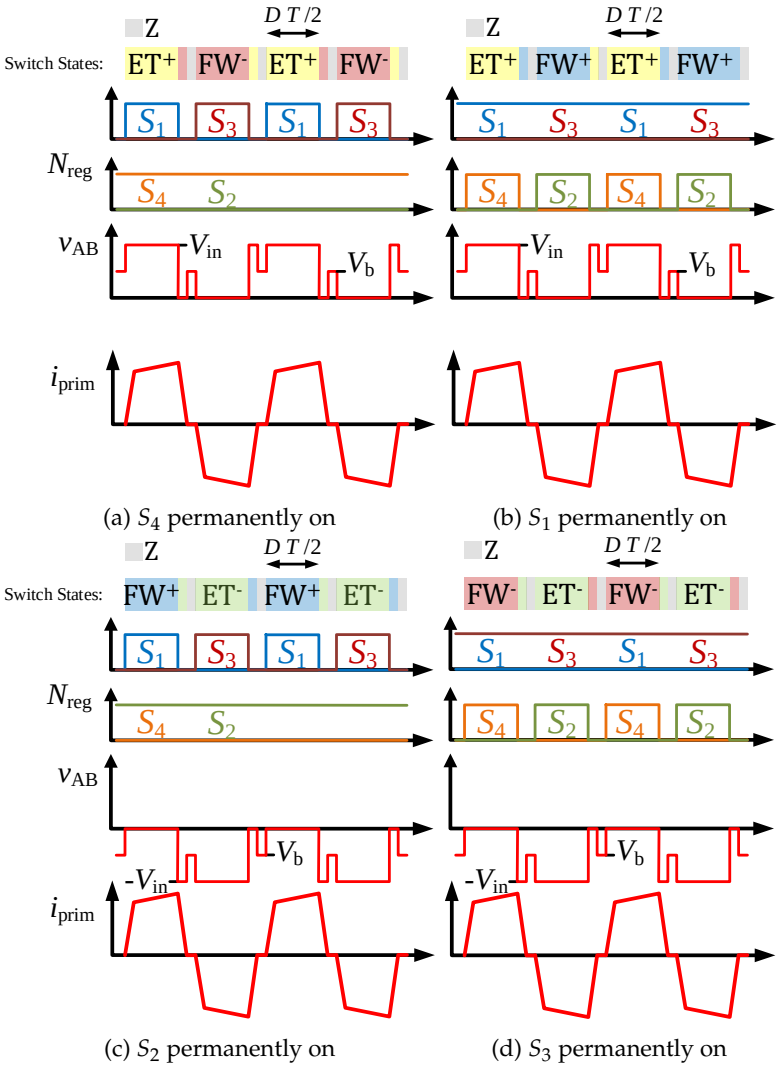


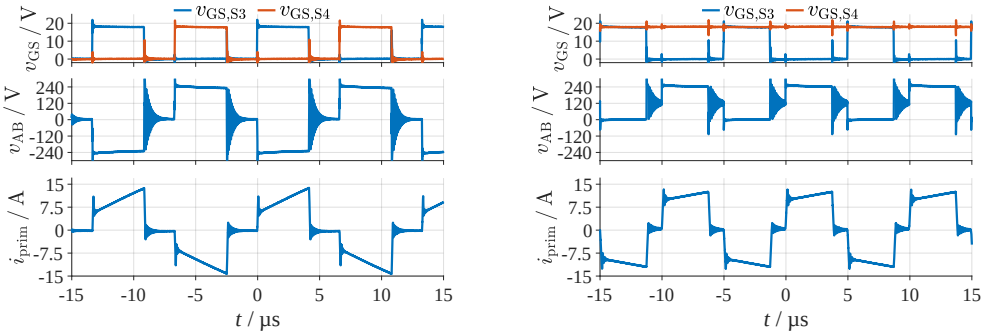
FIGURE 2.111: All possible hard-switched half-bridge modulations (HHBM) with their corresponding switching states (for simplicity, intervals, where the body diode conducts, are not labeled according to the inverter voltage switching state).

B2 Hard-switched half-bridge modulation If a blocking capacitor is employed in the full-bridge converter (as depicted in Figure 2.107); in comparison with the LLC, the capacitance of this component is much larger such that voltage fluctuations are small[1], one MOSFET of the full bridge can be permanently turned on while the two MOSFETs of the other bridge leg are pulsed with the duty cycle D_{HB}. Thus, only one ET state and one FW state are utilized (cf. (2.114)).

In the HHBM, the blocking capacitor absorbs half the input voltage. The voltage is $\bar{v}_{\mathrm{b}} = \frac{V_{\mathrm{in}}}{2}$ if the HHBM employs the switching state ET^{+} or $\bar{v}_{\mathrm{b}} = -\frac{V_{\mathrm{in}}}{2}$ if the switching state ET^{-} is employed. All possible HHBM are depicted in Figure 2.111. Figures 2.111a and 2.111b show modulations that result in $\bar{v}_{\mathrm{b}} = \frac{V_{\mathrm{in}}}{2}$, whereas for Figures 2.111c and 2.111d they result in $\bar{v}_{\mathrm{b}} = -\frac{V_{\mathrm{in}}}{2}$. The modulations of Figures 2.111a and 2.111d can be employed using cost-efficient bootstrap drivers, whereas the pulse patterns depicted in Figures 2.111b and 2.111c require an isolated continuous driver

[1] and the converter is operated far above the resonant frequency.

power supply[1]. Exemplary measurement results of HFBM and HHBM (Figure 2.111a) are depicted in Figure 2.112.



(a) Hard-switched full-bridge modulation (HFBM)

(b) Hard-switched half-bridge modulation (HHBM)

FIGURE 2.112: Exemplary measurement results of the hard-switched operation. (a) HFBM, (b) HHBM.

For the full-bridge modulation of Figure 2.112a, the effective voltage applied to the transformer is $v_{prim} = \pm\frac{V_{in}}{2}$. While this does not reduce the voltage stress of the primary MOSFETs , the blocking voltage of the rectifiers semiconductors is reduced by 50 %. This makes this mode particularly beneficial for applications with a wide input voltage range – switches of a lower blocking voltage can be employed for the rectification in comparison to an operation where the conventional HFBM or PSM is employed only. A disadvantage of this mode of operation is the unbalanced stress of the primary switches. Two switches are pulsed with the duty cycle D_{HB} exhibiting both switching and conduction losses. One switch is permanently turned on being stressed with no switching losses but large conduction losses. Finally, one switch is permanently turned off such that this switch does not experience any losses.

The losses of the MOSFET that are pulsed can be calculated as

$$P_{pulse}^{HHBM} = \overbrace{\frac{1}{2} I_{prim}^2 R_{ds,on}(\vartheta_j)}^{p_{cond,pulse}^{HHBM}} + \overbrace{f_{sw} E_{sw}(i_{off}, V_{in})}^{p_{sw,pulse}^{HHBM}}. \tag{2.115}$$

with the switching losses

$$\begin{aligned} E_{sw}(i_{off}, V_{in}) =& E_{off}(V_{in}, i_{off}) + E_{diss,iZVS}\left(\frac{V_{in}}{2}\right) \\ &+ E_{Df}(i_{off}, V_{in}), \end{aligned} \tag{2.116}$$

the iZVS switching losses E_{iZVS} calculated through [Kas+16] as

[1] in a bootstrap configuration, the switches need to be pulsed as otherwise the gate-voltage power supply is slowly discharged.

$$\begin{aligned} E_{\text{iZVS}}\left(\frac{V_{\text{in}}}{2}\right) &= E_{\text{oss}}\left(\frac{V_{\text{in}}}{2}\right) \\ &\quad + V_{\text{in}}\left(Q_{\text{oss}}(V_{\text{in}}) - Q_{\text{oss}}\left(\frac{V_{\text{in}}}{2}\right)\right) \\ &\quad - \left(E_{\text{oss}}\left(V_{\text{in}}\right) - E_{\text{oss}}\left(\frac{V_{\text{in}}}{2}\right)\right) \end{aligned} \tag{2.117}$$

and the body-diode losses

$$E_{\text{Df}} = \frac{i_{\text{off}} V_{\text{Df}}}{2} t_{\text{loss,D2}} = \frac{i_{\text{off}} V_{\text{Df}}}{2} \frac{L_{\text{s}} i_{\text{off}}}{V_{\text{in}}}. \tag{2.118}$$

The turn-off losses E_{off} are hereby associated to the turn-off current i_{off} and the input voltage V_{in} whereas the iZVS losses E_{iZVS} are calculated with the energy $E_{\text{oss}}(v)$ and charge $Q_{\text{oss}}(v)$ stored in the output capacitance C_{oss} at the voltage v. The diode forward-voltage losses can additionally be calculated with the forward voltage V_{Df}, the stray inductance L_{s} and the commutation time $t_{\text{loss,D2}}$.

To evaluate the loss distribution, the losses of these MOSFETs are divided into the conduction losses $P^{\text{HHBM}}_{\text{cond,pulse}}$ and the switching losses $P^{\text{HHBM}}_{\text{sw,pulse}}$. The MOSFET that is permanently turned on is stressed with the full primary transformer current such that the losses can be calculated as

$$P^{\text{HHBM}}_{\text{p-on}} = I^2_{\text{prim}} R_{\text{ds,on}}(\vartheta_{\text{j}}). \tag{2.119}$$

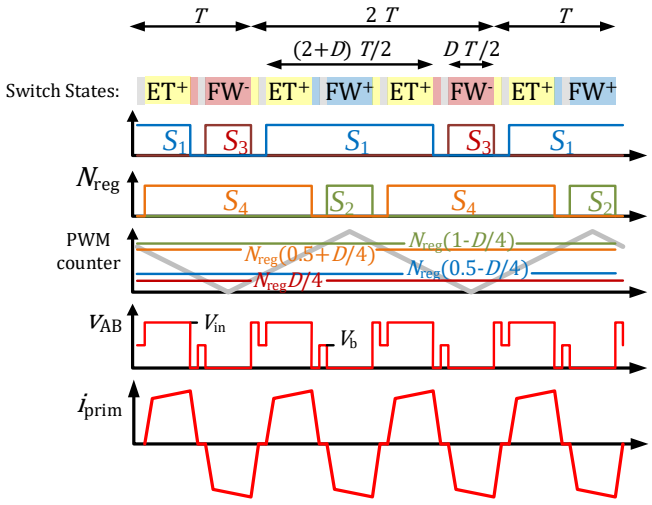
Assuming that the same MOSFET type is employed for all switches and neglecting temperature dependencies of the on-state resistance $R_{\text{ds,on}}$, the overall inverter losses can be calculated as $P_{\text{inv}} = 2I^2_{\text{res}} R_{\text{ds,on}} + 2 f_{\text{sw}} E_{\text{sw}}(i_{\text{off}}, V_{\text{in}})$. The conduction losses of the MOSFET that is permanently turned on are twice as large as the conduction losses of the pulsed switches ($P^{\text{HHBM}}_{\text{p-on}} = 2P^{\text{HHBM}}_{\text{cond,pulse}}$). This may be a problem for converters that employ switches where conduction losses are the dominant loss contributor – the switches have to be designed for a lower on-state resistance, which results in larger conversion costs.

C A loss-balancing frequency-doubler operation

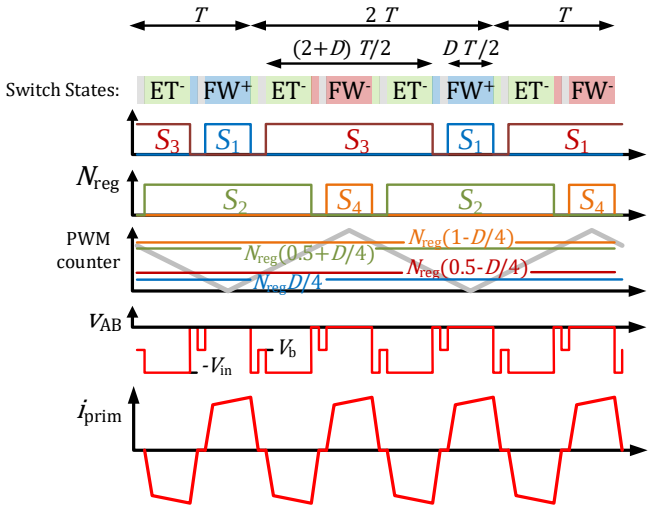
this section has been previously published in parts in [Reh+22c] *and the presented method has been applied for patent in* [RSB22b].

This section presents a novel two-period modulation scheme to improve the unbalanced loss distribution of the HHBM. The loss-balancing operating mode is depicted in Figure 2.113. Figure 2.113a shows a modulation that results in $\bar{v}_{\text{b}} = \frac{V_{\text{in}}}{2}$, while Figure 2.113b shows the one that results in $\bar{v}_{\text{b}} = -\frac{V_{\text{in}}}{2}$.

To achieve the inverter voltage, turn-on interval lengths of $DT/2$ and $(2+D)T/2$ (with $D \in [0,1]$) are used, which are phase-shifted for one bridge leg by T. The operating frequency (the frequency of the primary current i_{prim}) is, therefore, twice (doubled) the switching frequency of the bridge legs. The modulation exploits the fact that two inverter states exist that result in $v_{\text{AB}} = 0$ – FW^+ and FW^-, cf. (2.114).



(a) HSFDM ($\bar{v}_b = \frac{V_{in}}{2}$)



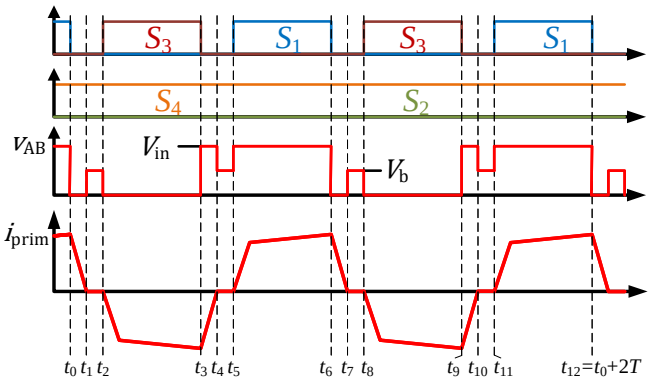
(b) HSFDM ($\bar{v}_b = -\frac{V_{in}}{2}$)

FIGURE 2.113: Hard-switched frequency-doubler modulation.

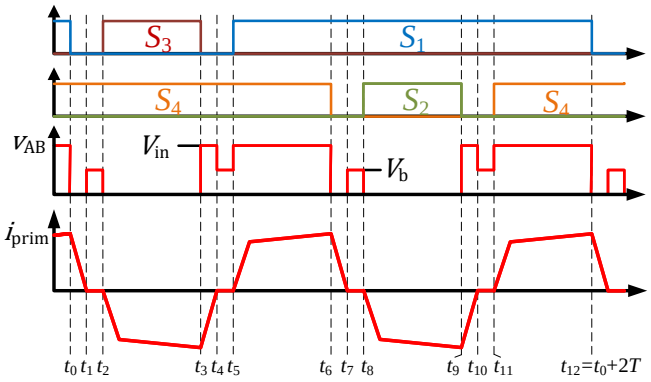
By employing an up-down counter, the modulation can be achieved using four compare values where every half bridge uses only two. This means that this type of modulation can be easily implemented on a DSP/microcontroller (e.g. in TI C2000 controllers using the action-qualifier control registers, AQCTL) similar to the loss balancing phase-shift modulation, which was addressed in Sections 2.1.1A4 and 2.1.1A5. The compare values are $N_{reg}(1 - D/4)$, $N_{reg}(0.5 + D/4)$, $N_{reg}(0.5 - D/4)$, and $N_{reg}D/4$. If the counter is below $N_{reg}(0.5 + D/4)$, S_4 is turned on while for the counter value larger $N_{reg}(1 - D/4)$, S_2 is turned on. Similarly, for the counter larger $N_{reg}(0.5 - D/4)$, S_1 is turned on, whereas for the counter smaller $N_{reg}D/4$, S_3 is turned on.

A detailed analysis of the conducting components is provided in Table 2.9 corresponding to the time-series analysis depicted in Figure 2.114. While both modulations have the same components conducting for $t_0 \leq t < t_6$ and $t_{11} \leq t < t_{12}$, for $t_6 \leq t < t_{10}$, the HSFDM has S_1 conducting and S_4 turned off.

During the operation, two diagonal MOSFETs are pulsed with a duty cycle of



(a) HHBM



(b) HSFDM

FIGURE 2.114: Detailed comparison of the HHBM and the HSFDM.

TABLE 2.9: Analysis of the conducting components during HHBM and HSFDM

	t_x, t_y with $t_x \leq t < t_y$			
	t_0, t_1	t_1, t_2	t_2, t_3	t_3, t_4
	conducting component			
HHBM	D_3 , S_4	-	S_3, S_4	D_1, S_4
HSFDM	D_3 , S_4	-	S_3, S_4	D_1, S_4

	t_x, t_y with $t_x \leq t < t_y$			
	t_4, t_5	t_5, t_6	t_6, t_7	t_7, t_8
	conducting component			
HHBM	-	S_1, S_4	D_3, S_4	-
HSFDM	-	S_1, S_4	D_2, S_1	-

	t_x, t_y with $t_x \leq t < t_y$			
	t_8, t_9	t_9, t_{10}	t_{10}, t_{11}	t_{11}, t_{12}
	conducting component			
HHBM	S_3, S_4	D_1, S_4	-	S_1, S_4
HSFDM	S_1, S_2	D_4, S_1	-	S_1, S_4

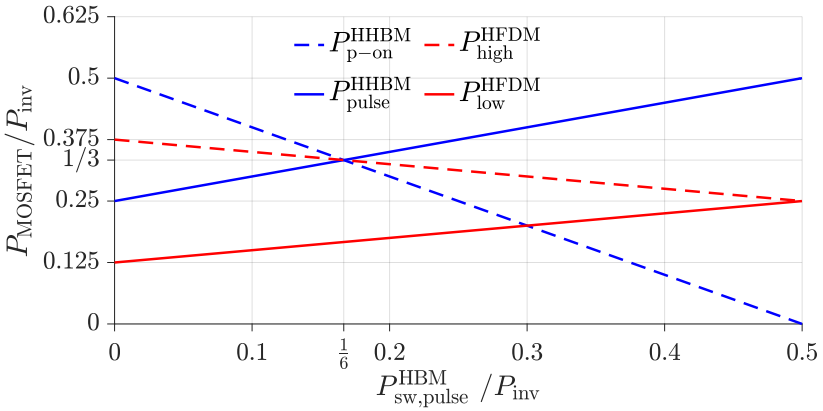


FIGURE 2.115: Modeled normalized losses of the HHBM and HSFDM.

$DT/2$, whereas the other two MOSFETs are pulsed with $(2+D)T/2$. The losses of the MOSFETs are $P^{\text{HFDM}}_{\text{low}}$ and $P^{\text{HFDBM}}_{\text{high}}$ respectively. The losses of the MOSFETs that are turned on for $(2+D)T/2$ can be calculated as

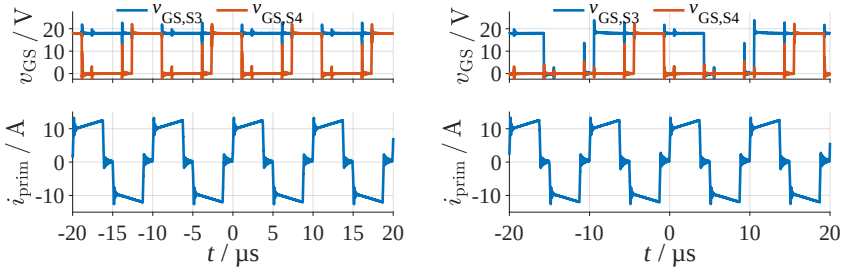
$$P^{\text{HFDM}}_{\text{high}} = \overbrace{\frac{3}{4} I^2_{\text{prim}} R_{\text{ds,on}}(\vartheta_j)}^{1.5\,P^{\text{HHBM}}_{\text{cond,pulse}} = 0.75\,P^{\text{HHBM}}_{\text{p-on}}} + \overbrace{\frac{1}{2} f_{\text{sw}} E_{\text{sw}}(i_{\text{off}}, V_{\text{in}})}^{0.5\,P^{\text{HHBM}}_{\text{sw,pulse}}}. \tag{2.120}$$

The overbrace comments put these losses in relation to the conventional HHBM while neglecting the temperature dependencies of the on-state resistance. The switches are turned on and off every two periods T of the primary current while the switches conduct for three quarters of the time. The lower losses $P^{\text{HFDM}}_{\text{low}}$ of the switches that are only turned on for $DT/2$, on the other hand, can be calculated as

$$P^{\text{HFDM}}_{\text{low}} = \overbrace{\frac{1}{4} I^2_{\text{prim}} R_{\text{ds,on}}(\vartheta_j)}^{0.5\,P^{\text{HHBM}}_{\text{cond,pulse}} = 0.25\,P^{\text{HHBM}}_{\text{p-on}}} + \overbrace{\frac{1}{2} f_{\text{sw}} E_{\text{sw}}(i_{\text{off}}, V_{\text{in}})}^{0.5\,P^{\text{HHBM}}_{\text{sw,pulse}}}. \tag{2.121}$$

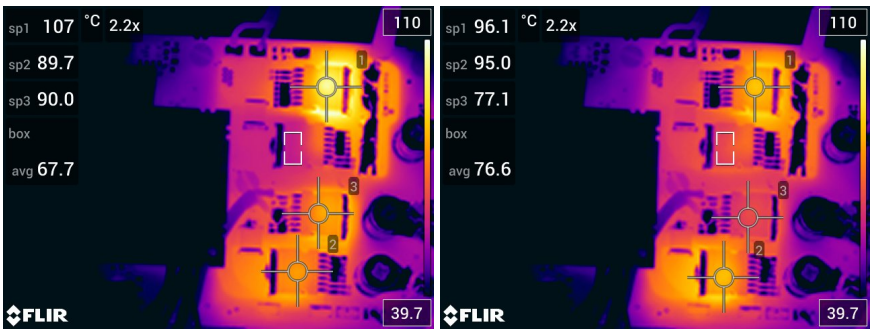
Thus, the overall losses P_{inv} of this modulation are the same compared to the conventional HHBM. Furthermore, also the number of switching transitions is the same and always two switches conduct the current. To evaluate the performance of this modulation, the HHBM and the HSFDM shall be evaluated for different loss distributions of the conduction losses and the switching losses. The reference is the conventional HHBM. Figure 2.115 shows a loss analysis assuming a constant on-state resistance $R_{\text{ds,on}}$. The losses of the MOSFETs are depicted over the ratio of the switching losses $P^{\text{HHBM}}_{\text{sw,pulse}}$ to the overall losses of the operation P_{inv}. An abscissa value of $P_{\text{sw,pulse}}/P_{\text{inv}} = 0$ means that the switching losses are negligible while an abscissa value of $P_{\text{sw,pulse}}/P_{\text{inv}} = 0.5$ refers to an ideal setup where the conduction losses are negligible.

Obviously, the modulation always distributes the losses more equally among all MOSFETs compared to the conventional HHBM. While for $P^{\text{HHBM}}_{\text{sw,pulse}}/\,P_{\text{inv}} < \frac{1}{6}$ (dominant conduction losses in $P^{\text{HHBM}}_{\text{pulse}}$), the switch that is permanently turned on experiences the largest losses, for $P^{\text{HHBM}}_{\text{sw,pulse}}/P_{\text{inv}} > \frac{1}{6}$ (dominant switching losses in $P^{\text{HHBM}}_{\text{pulse}}$), the switches that are pulsed face the largest losses. The MOSFET being

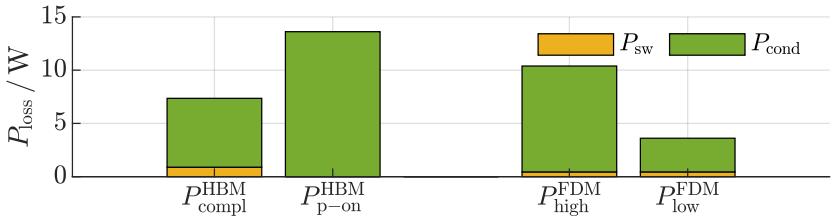


(a) HHBM (b) HSFDM

FIGURE 2.116: Comparison of the implemented modulations (parameters: $\text{Config}_{2.3c}$).



(a) HHBM (b) HFBM



(c) modeled MOSFET losses

FIGURE 2.117: (a,b) Comparison of the MOSFET temperatures and (c) modeled MOSFET losses (parameters: $\text{Config}_{2.3c}$). The maximum temperature is reduced by 11 K.

subject to the largest losses of the HSFDM (P^{HFDM}_{high}) always shows lower or identical overall losses than the most-stressed MOSFET of the conventional HHBM. Only for $P^{HHBM}_{sw,pulse}/P_{inv} = \frac{1}{6}$ where the overall conduction and switching losses are equal in P^{HHBM}_{pulse} ($P^{HHBM}_{sw,pulse} = P^{HHBM}_{cond,pulse}$), the losses of the maximum stressed switches in the HHBM are the same as the maximum stressed switches in the HSFDM. As mentioned above, this diagram simplifies the losses by assuming a temperature-independent on-state resistance. For the left side of the diagram ($P^{HHBM}_{sw,pulse}/P_{inv} < \frac{1}{6}$) this can result in a significant under-representation of the HHBM losses (P^{HHBM}_{p-on}) since the on-state resistance usually shows a significant dependency on the junction temperature. This results in a larger advantage of the HSFDM for $P^{HHBM}_{sw,pulse}/P_{inv} < \frac{1}{6}$ and a smaller advantage for $P^{HHBM}_{sw,pulse}/P_{inv} > \frac{1}{6}$.

The HHBM and HSFDM were both employed on an isolated full-bridge converter utilizing SiC MOSFETs of type *SCT3120AW7* (Rohm, 650 V, 120 mΩ @ 25 °C).

The input voltage was $V_{in} = 250\,V$, the output voltage $V_{out} = 8\,V$ at an output current of $I_{out} = 110\,A$. The primary current i_{prim} and gate voltages v_{GS} of

the low-side switches S_3 and S_4 are depicted for the HHBM and HSFDM in Figure 2.116a and Figure 2.116b, respectively. It is evident that both modulations result in equal primary currents. A thermal analysis of both operating modes is depicted in Figure 2.117a and Figure 2.117b. From top to bottom the switches are: S_1, S_3, S_2, S_4. By employing the HSFDM, the maximum MOSFET temperature was reduced by about 11 K. A loss model is depicted in Figure 2.117c. The experiments were performed at thermal steady state at the same operating conditions and correspond to Figure 2.116.

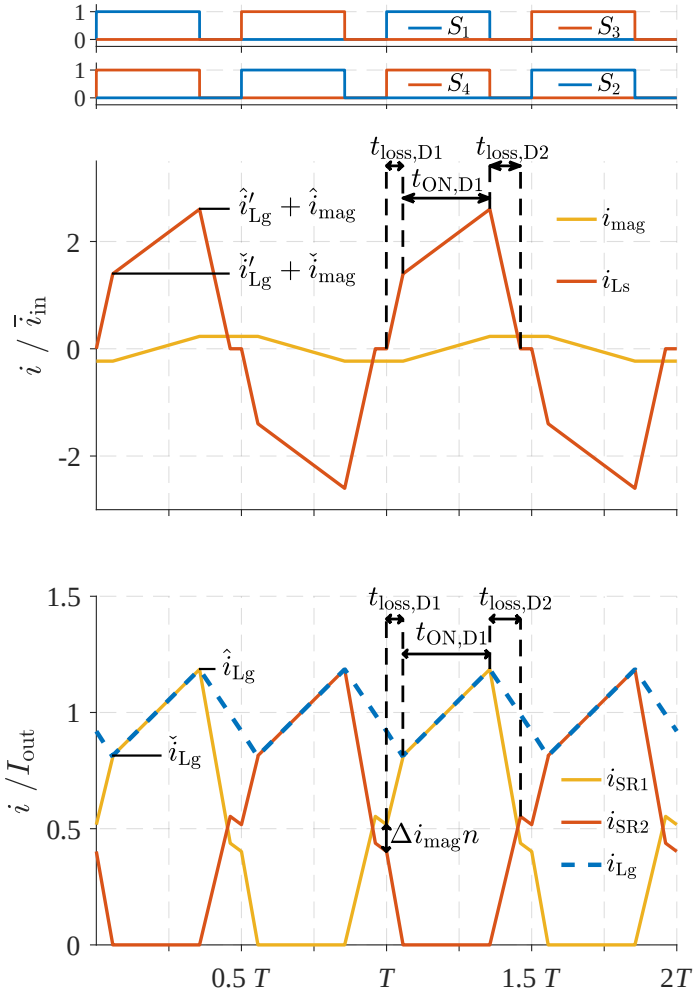


FIGURE 2.118: Shape of the primary and secondary currents of the isolated full-bridge converter in continuous conduction mode (CCM) (parameters: Config$_{2.3d}$).

2.3.2 Hard-switched operation model including the magnetizing current and series inductance

The model of the hard-switched operation is quite similar to the steady-state model of the active-clamp converter. The operation can be divided into similar intervals and some equations are also equal. For a full picture, this section will describe all the necessary equations to model the behavior. The operation of the isolated full-bridge converter is symmetrical. Therefore, this section focuses on one half period where the switches S_1 and S_4 (cf. Figure 2.107) are turned on and off. The steady-state operation is modeled with the following assumptions:

1. the commutation time is negligible in contrast to the switching frequency,
2. the influence of all parasitic components except the series inductance L_s is negligible,
3. the voltage drop of series resistances is negligible compared to the input voltage.

A Conventional continuous conduction mode with non-effective magnetizing inductance

The operation can be modeled according to Figure 2.118 with three intervals: the two duty-cycle loss intervals $t_{\text{loss,D1}}$ (2.3.2A2) and $t_{\text{loss,D2}}$ (2.3.2A3) and the energy-transfer interval $t_{\text{ON,D1}}$ (2.3.2A1). These intervals are explained in the following sections.

A1 Energy transfer interval $t_{\text{ON,D1}}$ The energy transfer interval is the only interval in which energy is transferred to the output inductor L_g. The diode D_1 conducts the full current i_{Lg} while diode D_2 is blocking. Considering Kirchhoff's voltage and current laws, the voltages applied to the inductors can be calculated with equations (2.123) to (2.127). The effective input $V_{\text{in,eff}}$ voltage is hereby determined by the mode of operation (2.122). For the half-bridge operation, the effective input voltage is halved since the blocking capacitor absorbs half the input voltage.

$$V_{\text{in,eff}} = \begin{cases} V_{\text{in}} & \text{if full} - \text{bridge operation} \\ \frac{V_{\text{in}}}{2} & \text{if half} - \text{bridge operation} \end{cases} \tag{2.122}$$

$$V_{\text{in,eff}} = V_{\text{Ls,D1}} + V_{\text{Lm,D1}} \tag{2.123}$$

$$V_{\text{Lm,D1}} = V'_{\text{Lg,D1}} + V'_{\text{out}} + V'_{\text{D}} \tag{2.124}$$

As the Kirchhoff's current law, the change in current is used:

$$\Delta i_{\text{prim}} = \Delta i_{\text{Lm}} + \Delta i'_{\text{Lg}} \tag{2.125}$$

$$\frac{V_{\text{Ls,D1}}}{L_{\text{s}}} = \frac{V_{\text{Lm,D1}}}{L_{\text{m}}} + \frac{V'_{\text{Lg,D1}}}{L'_{\text{g}}} \tag{2.126}$$

The diode voltage V_D in (2.124) can be approximated through a forward voltage V_f and a series resistance R_D as

$$V_{\text{D}} = V_{\text{f}} + R_{\text{D}} I_{\text{out}}. \tag{2.127}$$

Equations (2.123) - (2.126) can be solved for the voltages $V_{\text{Ls,D1}}$, $V_{\text{Lm,D1}}$, and $V_{\text{Lg,D1}}$. With the calculation of $V_{\text{Lg,D1}}$, the interval length of $t_{\text{ON,D1}}$ can be calculated with (2.128). The voltage applied to the output inductor L_g in the remaining intervals is $-(V_{\text{out}} + V_{\text{D}})$. This solution of the transfer interval length solves the complete operation and can be used in all subsequent equations.

$$t_{\text{ON,D1}} V_{\text{Lg,D1}} = (T - t_{\text{ON,D1}})(V_{\text{out}} + V_{\text{D}}) \tag{2.128}$$

This allows the calculation of the output current ripple Δi_{Lg} with equation (2.129) enabling the derivation of the maximum and minimum output inductor current $\hat{i}_{Lg}$ and $\check{i}_{Lg}$ with equations (2.130) and (2.131) respectively.

$$\Delta i_{\mathrm{Lg}} = \frac{t_{\mathrm{ON,D1}}}{L_{\mathrm{g}}} V_{\mathrm{Lg,D1}} \tag{2.129}$$

$$\hat{i}_{\mathrm{Lg}} = I_{\mathrm{out}} + \Delta i_{\mathrm{Lg}} \tag{2.130}$$

$$\check{i}_{\mathrm{Lg}} = I_{\mathrm{out}} - \Delta i_{\mathrm{Lg}} \tag{2.131}$$

Furthermore, the current ripple of the magnetizing current Δi_{mag} can be calculated as

$$\Delta i_{\mathrm{mag}} = \hat{i}_{\mathrm{mag}} - \check{i}_{\mathrm{mag}} = \frac{V_{\mathrm{Lm,D1}} t_{\mathrm{ON,D1}}}{L_{\mathrm{m}}}. \tag{2.132}$$

A2 Duty cycle loss interval $t_{\mathrm{loss,D1}}$ When the main switches S_1 and S_2 are turned on, the input voltage is applied to series inductor L_{s}, and the current i_{prim} rises. All diodes on the secondary side are conducting such that the magnetizing inductance L_{m} is shorted - the current i_{mag} remains constant. Since i_{mag} remains constant, i_{prim} increases by the sum of transformed minimum output inductor current and the minimum magnetizing current such that the interval length can be defined as

$$t'_{\mathrm{loss,D1}} = L_{\mathrm{s}} \frac{\check{i}_{\mathrm{Lg}} + \check{i}_{\mathrm{mag}}}{V_{\mathrm{in,eff}}}. \tag{2.133}$$

A3 Duty cycle loss interval $t_{\mathrm{loss,D2}}$ During the interval $t_{\mathrm{loss,D2}}$, the current i_{prim} falls by $\hat{i}'_{\mathrm{Lg}} + \hat{i}_{\mathrm{mag}}$ to the maximum magnetizing current $\hat{i}_{\mathrm{mag}}$. The magnetizing inductance is shorted and the magnetizing current remains constant. The interval length can be calculated as

$$t_{\mathrm{loss,D2}} = L_{\mathrm{s}} \frac{\hat{i}'_{\mathrm{Lg}} + \hat{i}_{\mathrm{mag}}}{V_{\mathrm{in,eff}}}. \tag{2.134}$$

B Continuous conduction mode with effective magnetizing inductance

In the aforementioned CCM, the magnetizing current is freewheeling when no power is transferred from the input to the output inductor. However, this mode is only valid if $i_{\mathrm{Lg}}(t) > i'_{\mathrm{mag}}(t)$. If this condition is not fulfilled, the converter enters another mode of operation where both the magnetizing and output inductor transfer power to the output called CCMb. The current shape of this operating mode is depicted in Figure 2.119. The magnetizing inductance extends the continuous conduction area of the converter. The operation can be divided into the three intervals $t_{\mathrm{ON,D1}}$, $t_{\mathrm{OFF,D1}}$, and $t_{\mathrm{OFF,D2}}$. Similar to the CCM operation, in $t_{\mathrm{ON,D1}}$, energy is transferred from the input to the output inductor and the magnetizing inductance. In the interval $t_{\mathrm{OFF,D1}}$, only the output inductor transfers energy to the output capacitor, whereas in $t_{\mathrm{OFF,D2}}$, energy is transferred to the output by both the output inductor L_{g} and the magnetizing inductance L_{m}.

This section will derive an analytical model to calculate the current shape by solving the following six characteristic equations for the characteristic currents $\hat{i}_{\mathrm{Lg}}$,

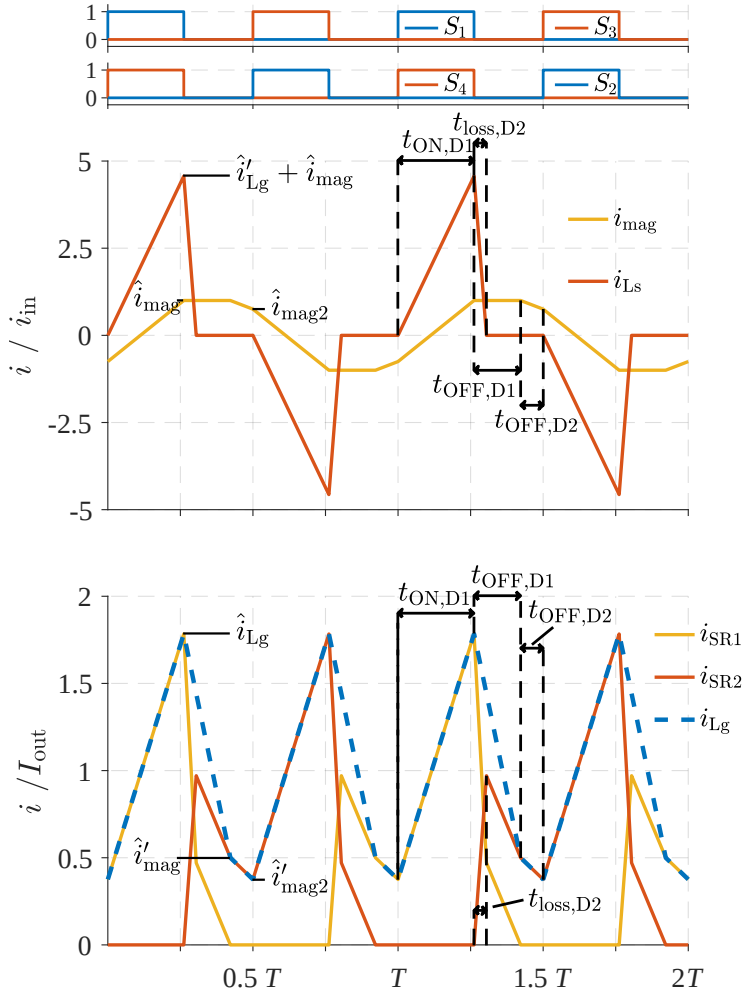


FIGURE 2.119: Shape of the primary and secondary currents of the isolated full-bridge converter in continuous conduction mode with the magnetizing inductance L_{m} participating in the energy transfer (CCMb) (parameters: Config$_{2.4e}$).

$\hat{i}_{\text{mag}}$ and $\hat{i}_{\text{mag2}}$ and the characteristic interval lengths $t_{\text{ON,D1}}$, $t_{\text{OFF,D1}}$, and $t_{\text{OFF,D2}}$. The interval length $t_{\text{loss,D2}}$ can be calculated after solving the current waveform in dependency of $\hat{i}_{\text{mag}}$ and $\hat{i}_{\text{Lg}}$. The characteristic voltages during the energy transfer interval $V_{\text{Lg,D1}}$ and $V_{\text{Lm,D1}}$ can beforehand be calculated by solving (2.123) - (2.126), which are are also valid for this operating mode. With the calculated output inductor voltage, the transfer equation can be defined as

$$V_{\text{Lg,D1}} t_{\text{ON,D1}} - V_{\text{out}} t_{\text{OFF,D1}} - V_{\text{out}} \frac{L_{\text{g}}}{L_{\text{g}} + L'_{\text{m}}} t_{\text{OFF,D2}} = 0. \tag{2.135}$$

The second equation can be defined for the output current I_{out}. The output current can be calculated by integrating over the output inductor current as

$$I_{\text{out}} = \frac{1}{T} \left(t_{\text{OFF,D1}} \frac{\hat{i}_{\text{Lg}} + \hat{i}'_{\text{mag}}}{2} + t_{\text{OFF,D2}} \frac{\hat{i}'_{\text{mag}} + \hat{i}'_{\text{mag2}}}{2} + t_{\text{ON,D1}} \frac{\hat{i}'_{\text{mag2}} + \hat{i}_{\text{Lg}}}{2} \right). \tag{2.136}$$

Three further equations can be defined by the three characteristic currents $\hat{i}_{Lg}$, $\hat{i}_{mag}$ and $\hat{i}_{mag2}$ as formulated in (2.137)-(2.139).

$$\hat{i}_{mag} = -\hat{i}_{mag2} + \frac{V_{Lm,D1} t_{ON,D1}}{L_{mag}} \tag{2.137}$$

$$\hat{i}_{Lg} = \hat{i}'_{mag2} + \frac{V_{Lg,D1} t_{ON,D1}}{L_g} \tag{2.138}$$

$$\hat{i}_{mag} - \frac{L_g}{L_g + L'_m} \frac{V_{out}}{L_g} t_{2,OFF} = \hat{i}_{mag2} \tag{2.139}$$

Further, the symmetry of the current shape can be utilized to formulate the continuity equation

$$t_{ON,D1} + t_{1,OFF} + t_{2,OFF} = \frac{T}{2}. \tag{2.140}$$

Finally, (2.135)-(2.140) can be solved for the characteristic interval lengths and current values. To calculate the full primary current shape, $t_{loss,D2}$ can be calculated according to (2.134).

C Discontinuous conduction model

In DCM, both the output inductor current i_{Lg} and the magnetizing current i_{mag} reduce to zero. The mathematical description of this operating mode is similar to Section 2.3.2B with the difference that $\hat{i}_{mag2} = 0$ and that (2.140) is not valid for this mode. For this mode, five characteristic equations can be setup to solve for the characteristic currents $\hat{i}_{Lg}$ and $\hat{i}_{mag}$ and the characteristic interval lengths $t_{ON,D1}$, $t_{OFF,D1}$ and $t_{OFF,D2}$ (as visualized in Figure 2.120).

The transfer equation is the same as for the CCMb operating mode:

$$V_{Lg,D1} t_{ON,D1} - V_{out} t_{OFF,D1} - V_{out} \frac{L_g}{L_g + L'_m} t_{OFF,D2} = 0 \tag{2.141}$$

With $\hat{i}_{mag}$, the output current can be calculated as

$$I_{out} = \frac{1}{T} \left(t_{OFF,D1} \frac{\hat{i}_{Lg} + \hat{i}'_{mag}}{2} + t_{OFF,D2} \frac{\hat{i}'_{mag}}{2} + t_{ON,D1} \frac{\hat{i}_{Lg}}{2} \right). \tag{2.142}$$

The final three equations can be defined by the two characteristic currents $\hat{i}_{Lg}$, $\hat{i}_{mag}$ and $\hat{i}_{mag2}$ as formulated in (2.143) and (2.144) and the continuity equation as defined in (2.145).

$$\hat{i}_{mag} = \frac{V_{Lm,D1} t_{ON,D1}}{L_{mag}} \tag{2.143}$$

$$\hat{i}_{Lg} = \frac{V_{Lg,D1} t_{ON,D1}}{L_g} \tag{2.144}$$

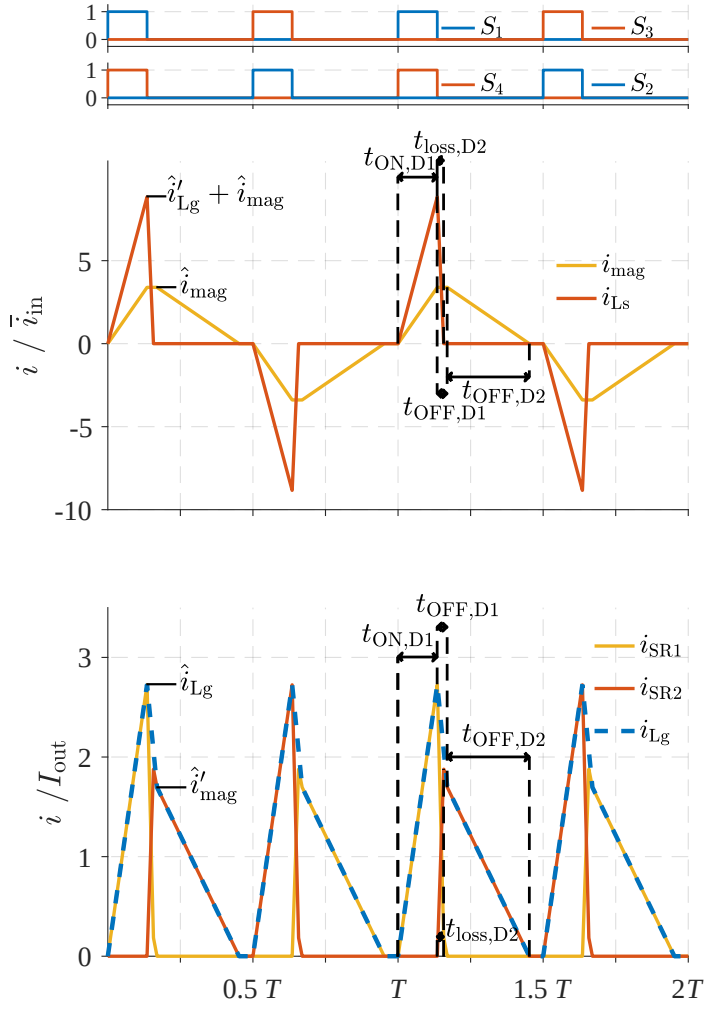


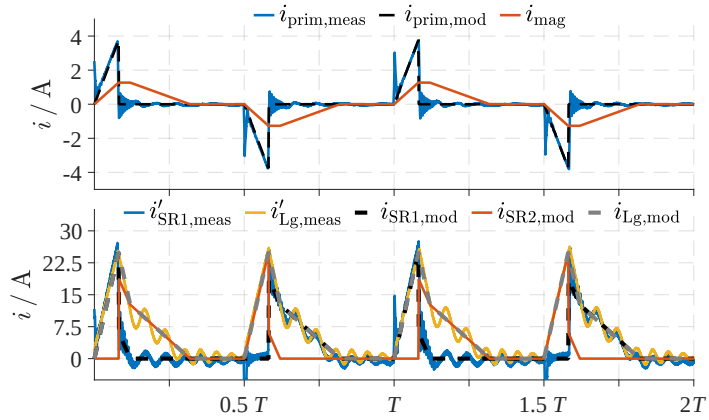
FIGURE 2.120: Shape of the primary and secondary currents of the isolated full-bridge converter in DCM (parameters: $\text{Config}_{2.3f}$).

$$\hat{i}_{\text{mag}} - \frac{L_{\text{g}}}{L_{\text{g}} + L'_{\text{mag}}} \frac{V_{\text{out}}}{L_{\text{g}}} t_{2,\text{OFF}} = 0 \tag{2.145}$$

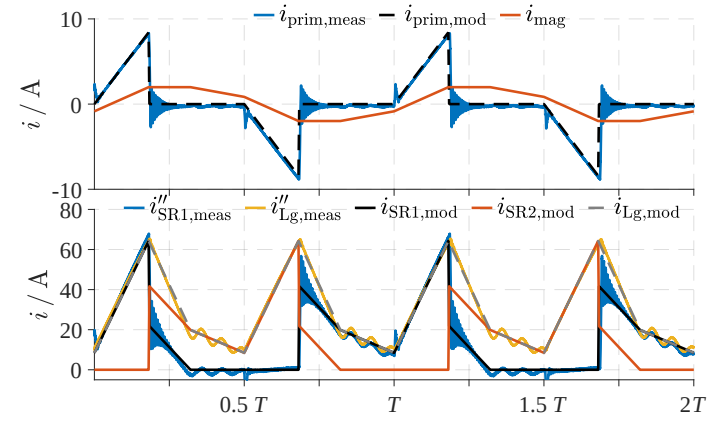
The five characteristic equations (2.141)-(2.145) can be solved for the characteristic interval lengths and current values. To calculate the full primary current shape, $t_{\text{loss,D2}}$ can again be calculated according to (2.134).

D Evaluation

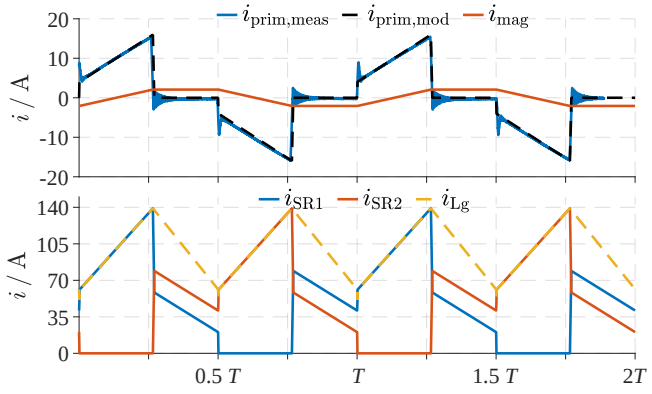
The developed model was benchmarked versus measurements on an experimental prototype in all three modes of operation. The prototype is visualized in Figure 3.23d and the measurement results are depicted together with the model results in Figure 2.121 for low, intermediate and full load. Figure 2.121a visualizes the low-load DCM operation, Figure 2.121b shows the intermediate-load CCMb operation and Figure 2.121c depicts the high-load CCM operation. The measurement results were obtained using a current clamp for measuring the primary transformer current i_{prim} while the secondary-side currents i_{Lg} and i_{SR1} were obtained using Rogowski coils. Due to the current limitation of these measurement devices, the secondary-side currents were only measured for the DCM and CCMb operation. Furthermore,



(a) DCM



(b) CCMb

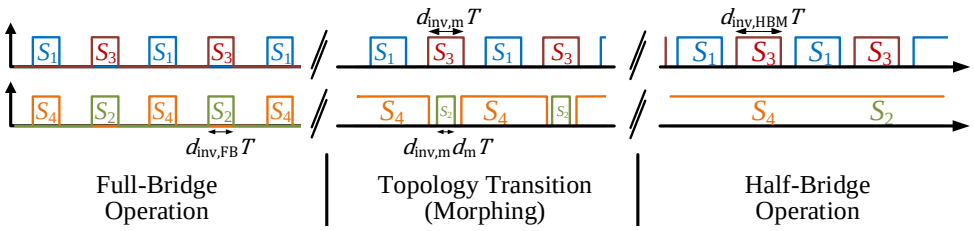


(c) CCM

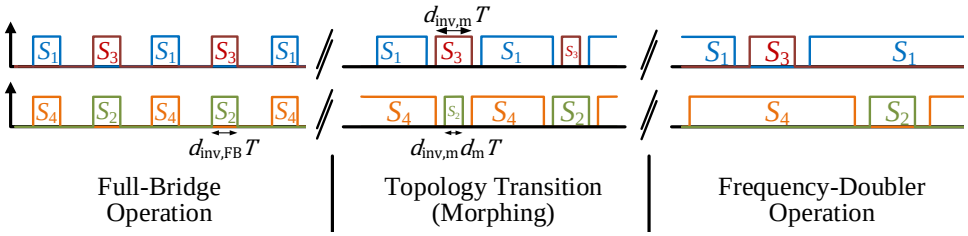
FIGURE 2.121: Experimental measurement results compared to the developed model. (a) DCM operation $i'_{\text{SR1,meas}} = \bar{i}_{\text{SR1,meas}} + \frac{I_{\text{out}}}{2}$, $i'_{\text{Lg,meas}} = \bar{i}_{\text{Lg,meas}} + I_{\text{out}}$ (parameters: $\text{Config}_{2.3g}$), (b) CCMb operation $i''_{\text{SR1,meas}} = \bar{i}_{\text{SR1,meas}} + \frac{I_{\text{out}}}{2}$, $i''_{\text{Lg,meas}} = \bar{i}_{\text{Lg,meas}} + I_{\text{out}}$ (parameters: $\text{Config}_{2.3h}$), (c) CCM operation (parameters: $\text{Config}_{2.3i}$).

the appropriate DC bias is added to the secondary-side current measurements as the Rogowski measurement method does not capture the DC bias.

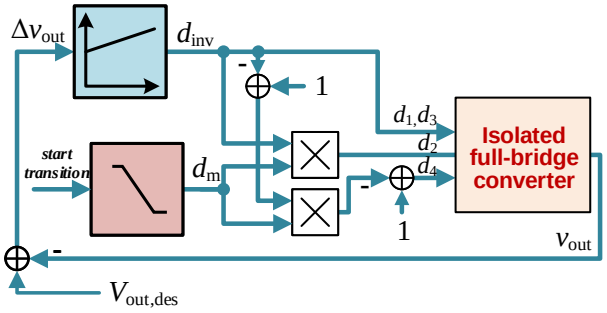
The modeling results show remarkable accuracy. The modeling error is very low and the measurement results capture the general current shape. The current oscillations at DCM and CCMb result from the resonance between the primary stray inductance L_s and the secondary-side parasitic output capacitance of the rectifier semiconductors. Overall, it can be concluded that the model is accurate and can be utilized in the converter comparison and design procedure of Section 3.3.



(a) Qualitive morphing visualization



(b) Qualitive HFDM morphing visualization



(c) Conventional control concept

FIGURE 2.122: (a) Qualitative demonstration of the conventional morphing method; (b) conventional control concept of the morphing as depicted in [JI15b].

2.3.3 Hard-switched topology morphing

this section has been previously published in parts in [RSB22d].

A Introduction and state of the art

To switch from one operating mode to the other while supplying the converter's load, an on-the-fly morphing modulation is required. On-the-fly morphing modulations have been proposed for the LLC in [JI15a; JI16; Reh+21e]. Additionally, an on-the-fly morphing modulation was discussed for the isolated full-bridge converter in [JI15b]. The topology morphing from full-bridge to half-bridge mode is achieved by a gradual increase of the duty cycle of one switch while the duty cycle of the other switch of the same bridge leg is gradually decreased. This is qualitatively visualized in Figure 2.122a and the control concept is displayed in Figure 2.122c[1]. Through this operation, the blocking capacitor is slowly charged such that the voltage applied to the transformer gradually reduces to the half-bridge levels.

This transition, however, has two major flaws. First, it results in an about 50 %

[1] since there are four different half-bridge modulations, four different morphing modulations exist also, which concepts are identical. Therefore, this section focuses on the transition into the half-bridge modulation displayed in Figure 2.111.

larger rectifier blocking voltage $v_{SR1/2}$ at the end of the morphing interval compared to standard full-bridge modulation. If such an on-the-fly morphing transition is desired, the rectifier MOSFETs / diodes must be designed for an increased blocking voltage resulting in larger losses and costs. Second, the transition results in imbalanced rectifier stage currents, which is compensated by the magnetizing current through an offset. This may potentially lead to a saturation of the transformer. To overcome this problem, the transformer must be designed for a larger flux, which consequently results in increased winding losses, higher component costs and larger magnetic components. The two effects will be described in detail in the following paragraphs.

A1 Issue 1: rectifier blocking voltages In full-bridge mode, the inverter output voltage v_{AB} is actively pulsed between $v_{AB} \in \{-V_{in}, V_{in}\}$ while in half-bridge mode the inverter voltage is pulsed between $v_{AB} \in \{0, V_{in}\}$. During the morphing transition, however, the inverter voltage levels are pulsed between $v_{AB} \in \{-V_{in}, 0, V_{in}\}$ and the primary transformer voltage is calculated as $v_{prim} = v_{AB} + v_b$ (cf. Figure 2.107), whereas the blocking capacitor voltage increases from $\bar{v}_b = 0$ (in full-bridge mode) to $\bar{v}_b = \frac{V_{in}}{2}$ in half-bridge mode (cf. Figure 2.123a). Therefore, just before the end of the morphing interval ($v_b \approx \frac{V_{in}}{2}$), the voltage levels applied to the transformer are $v_{prim} \in \{-\frac{V_{in}}{2}, \frac{V_{in}}{2}, \frac{3V_{in}}{2}\}$ such that the maximum transformer voltage level is increased by 50 % compared to the conventional full-bridge operation. Since the resulting blocking voltage of the SR is proportional to the transformer primary voltage, the application of the conventional morphing transition implies the SR-stage to be designed for a larger blocking voltage, which comes with higher losses and costs.

A2 Issue 2: increased magnetizing flux and current During the transition interval, the magnetizing current increases significantly. A simulation of the conventional morphing transition is depicted in Figure 2.123a showing the results for a center-tapped rectifier stage. During the transition interval, the magnetizing current shows a temporary DC-bias of 107 % compared to its unbiased amplitude value in full-bridge operation. Furthermore, the increased blocking voltage of v_{SR2} can be noticed very well. Figure 2.123b and Figure 2.123c visualize the current and voltage shapes at two instances during the transition. In Figure 2.123c, the large spike in the blocking voltage v_{SR2} at the instance when S_2 turns on can be identified as indicated by the red arrow. At this point, the blocking capacitor is almost charged to half the input voltage such that the primary transformer voltage is $v_{prim} \approx \frac{3V_{in}}{2}$.

Considering the state-of-the-art method, a continuous, uninterrupted morphing is only possible by employing rectifier semiconductors with an about 50 % higher blocking voltage and by using a transformer with a sufficient margin of the flux density. As this results in increased losses, and reduced power density, this solution comes at a high price. To utilize semiconductors of smaller blocking voltage and to reduce the transformer volume, this section proposes an alternative solution: a transformer clamping method is described, which avoids voltage peaks at the rectifier semiconductors without requiring additional components in the power path. Furthermore, an increased flux density and/or magnetizing current is avoided by utilizing a modified control method.

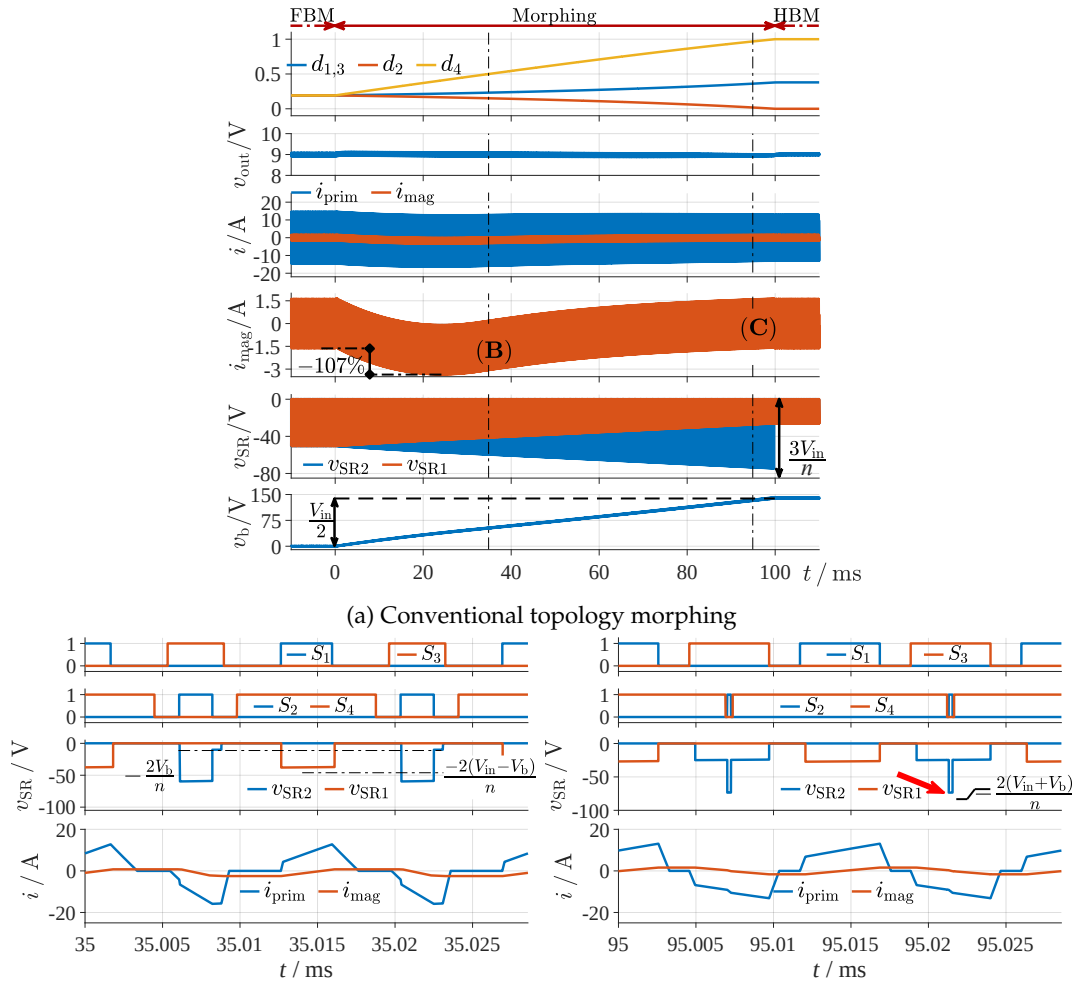


FIGURE 2.123: Conventional morphing as described in [JI15b]. (b,c) zoom to the time instances (B,C) that are displayed in (a) (parameters: $\text{Config}_{2.3j}$).

B Limitation of the rectifier blocking voltage during morphing

An increased blocking voltage is avoided by a primary-side clamping winding of the transformer as depicted in Figure 2.124 in orange. This winding is connected to the input through a clamping diode D_{cl}. The concept additionally shows an active snubber on the secondary side in green to suppress over-voltages being caused by the inductive termination (L_g) of the circuit, the series inductance L_s, and the parasitic output capacitance of the rectifiers [Zai17]. A snubber is required independently of the employed morphing concept.

If the primary transformer voltage v_{prim} surpasses the threshold v_{clamp}^{prim} that is determined by the turns number N_{aux} of the clamping winding, its diode starts conducting and the primary transformer voltage is clamped to the level

$$v_{clamp}^{prim} = \frac{N_p}{N_{aux}} V_{in} + L_\sigma \frac{di_{aux}}{dt} + R_\sigma i_{aux}. \tag{2.146}$$

Therefore, the secondary rectifier voltage is clamped to the voltage level

$$v_{\text{clamp}}^{\text{sec}} = v_{\text{clamp}}^{\text{prim}} \frac{mN_\text{s}}{N_\text{p}}. \tag{2.147}$$

where k is the rectifier coefficient with $m = 1$ representing a full-bridge rectifier and $m = 2$ the center-tapped rectifier stage.

Neglecting the parasitic stray inductance L_σ and stray resistance R_σ, the clamping diode must be dimensioned for the maximum reverse voltage. The reverse voltage is calculated as

$$V_{\text{clamp,rev}} = \begin{cases} V_\text{in}(1 + \frac{N_\text{aux}}{N_\text{p}}) & \text{if HFBM} \\ V_\text{in}(1 + \frac{N_\text{aux}}{2N_\text{p}}) & \text{if HHBM} \end{cases} \tag{2.148}$$

where FBM is the full-bridge mode and HBM is the half-bridge mode. Depending on the maximum input voltage and the selection of the operating regions, the maximum reverse voltage can, thus, appear either in full-bridge or half-bridge mode (since the full-bridge mode can only be utilized for smaller input voltages).

During the clamping interval, the voltage difference between the primary voltage v_prim and the clamping voltage $v_{\text{clamp}}^{\text{prim}}$ is applied to the series inductance L_s, which can be a discrete inductor or a primary stray inductance. During clamping, three windings are conducting current such that the three-winding stray inductance model [Alb17] must be applied. The series inductor voltage is calculated as

$$\begin{aligned} \hat{v}_\text{Ls} =& \hat{v}_\text{prim} - v_{\text{clamp}}^{\text{prim}} = V_\text{in} + v_\text{b} \\ & - \frac{N_\text{p}}{N_\text{aux}} V_\text{in} - L_\sigma \frac{\text{d}i_\text{aux}}{\text{d}t} - R_\sigma i_\text{aux} \end{aligned} \tag{2.149}$$

and is causing a steep primary current (i_prim) increase during the clamping interval t_clamp, which is depicted in Figure 2.125c. The current slope $\frac{\text{d}i_\text{prim}}{\text{d}t} = \frac{v_\text{Ls}}{L_\text{s}}$ is hereby determined by the series inductance. The maximum auxiliary current peak can be calculated with the switching period T as

$$\hat{i}_\text{aux} = \frac{t_\text{clamp}\hat{v}_\text{Ls}}{L_\text{s}} = \frac{d_2 T \hat{v}_\text{Ls}}{L_\text{s}}, \tag{2.150}$$

emphasizing that the maximum auxiliary current can be influenced via the switching frequency $f_\text{sw} = \frac{1}{T}$, modifying the clamping duration t_clamp, and the series inductance L_s. Since L_s determines both the maximum auxiliary current and the duty cycle loss interval length, a tradeoff must be found to achieve a reasonable duty cycle loss and maximum clamping current. In the simulation, it was chosen as $L_\text{s} = 7.5\,\mu\text{H}$.

As shown through (2.146), the clamping voltage is also influenced by the stray inductance L_σ. Any stray inductance of the auxiliary winding increases the clamping voltage level. Therefore, it is most important to achieve an optimal coupling coefficient between the primary winding and the auxiliary winding.

C Limitation of the magnetizing flux over- and undershoot

The simulation results of Figure 2.123a showed that the morphing transition results in a large magnetizing current offset. This chapter analyzes the magnetizing current

overshoot to propose an alternative control concept.

C1 Analysis of the magnetizing current overshoot Since the morphing interval is usually much larger than the switching period ($t_{\mathrm{morph}} \gg T$), it is feasible to analyze the circuit within that interval in a quasi steady state.

While morphing from full-bridge to half-bridge mode, the blocking capacitor needs to be charged from $\bar{v}_{\mathrm{b}} = 0$ to a voltage level $\bar{v}_{\mathrm{b}} = \frac{V_{\mathrm{in}}}{2}$, which requires an average current larger than zero. Assuming a constant charging current, the average primary inductor current $\bar{i}^{\mathrm{m}}_{\mathrm{prim}}$ can be calculated as

$$\bar{i}^{\mathrm{m}}_{\mathrm{prim}} = \frac{Q_{\mathrm{Cb}}(\frac{V_{\mathrm{in}}}{2})}{t_{\mathrm{morph}}} = \frac{C_{\mathrm{b}} V_{\mathrm{in}}}{2 t_{\mathrm{morph}}} \tag{2.151}$$

where t_{morph} is the morphing interval, C_{b} is the blocking capacitance and Q_{Cb} is the charge stored in the blocking capacitor in half-bridge mode.

At first glance, it may appear plausible that this charging current is the root cause of the magnetizing current offset. However, this is not the case. Assuming a blocking capacitance of $C_{\mathrm{b}} = 14\,\mu\mathrm{F}$, an input voltage of $V_{\mathrm{in}} = 280\,\mathrm{V}$ and a morphing time of $t_{\mathrm{morph}} = 100\,\mathrm{ms}$ – a setting being used in all displayed simulations – the average charging current is $\bar{i}^{\mathrm{m}}_{\mathrm{prim}} = 19.6\,\mathrm{mA}$, which is much smaller compared to the magnetizing current offset of about 1.7 A in Figure 2.123a.

Instead, the offset of the magnetizing current is caused by an imbalance in the rectifier currents. Figure 2.123b shows an interval where the offset is relatively large. After the turn-off of S_1, the switch S_4 remains turned on while the current i_{prim} is positive and flowing through the body diode of S_3 such that only the (negative) blocking capacitor voltage (approximately $-60\,\mathrm{V}$) is applied to the series inductance L_{s} leading to a rather small negative current slope. The same happens when S_2 is turned off: the switch S_3 remains on and the current circulates through the body diode of S_4. When S_3 is finally turned off, the primary current commutates to the diagonal path either through the body diodes of S_1 and S_4 (cf. Figure 2.123b) or through the body diode of S_1 and the channel of S_4 (cf. Figure 2.123c) and demagnetizes L_{s} rather fast.

To summarize, during the morphing, there are two intervals with a small absolute slope of the primary current i_{prim}: the turn-on of S_4 with the body diode of S_3 ($i_{\mathrm{prim}} > 0$) and the turn-on of S_3 with the body diode of S_4 ($i_{\mathrm{prim}} < 0$). Both intervals result in an imbalance of the individual rectifier currents. Comparing both currents ($i_{\mathrm{SR1}} = n(i_{\mathrm{prim}} - i_{\mathrm{mag}})$ for $i_{\mathrm{prim}} > i_{\mathrm{mag}}$ and $i_{\mathrm{SR2}} = n(|i_{\mathrm{prim}} - i_{\mathrm{mag}}|)$ for $i_{\mathrm{prim}} < i_{\mathrm{mag}}$), it can be assessed that the increased conduction length through S_4 and the body diode of S_3 during $i_{\mathrm{prim}} > 0$ results in $\bar{i}'^{\mathrm{m}}_{\mathrm{sec}} = \int_T (i_{\mathrm{prim}} - i_{\mathrm{mag}})\mathrm{d}t > 0$. However, since the blocking capacitor is placed in series, the primary current $\bar{i}_{\mathrm{prim}}$ must be equal to the charging current $\bar{i}^{\mathrm{m}}_{\mathrm{prim}}$, which is compensated through a magnetizing current offset.

Accordingly, this magnetizing current offset can be calculated as

$$\bar{i}^{\mathrm{m}}_{\mathrm{mag}} = \bar{i}^{\mathrm{m}}_{\mathrm{prim}} - \bar{i}'^{\mathrm{m}}_{\mathrm{sec}}. \tag{2.152}$$

C2 A modulation with a reduced magnetizing current offset The preceding section showed that the root cause of the magnetizing current offset is the small absolute primary current slope when S_1 is turned off while S_4 remains turned on. At

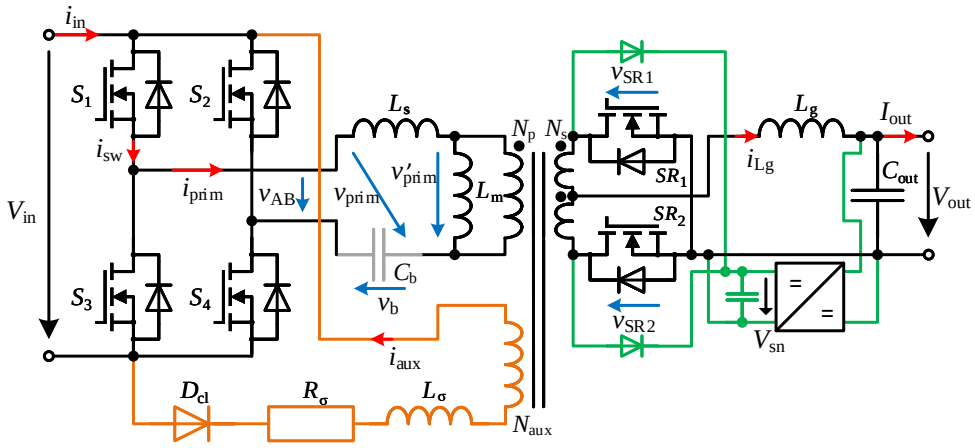


FIGURE 2.124: Isolated full bridge with clamping winding (orange) to avoid over voltages of the rectifier semiconductors and active snubber (green).

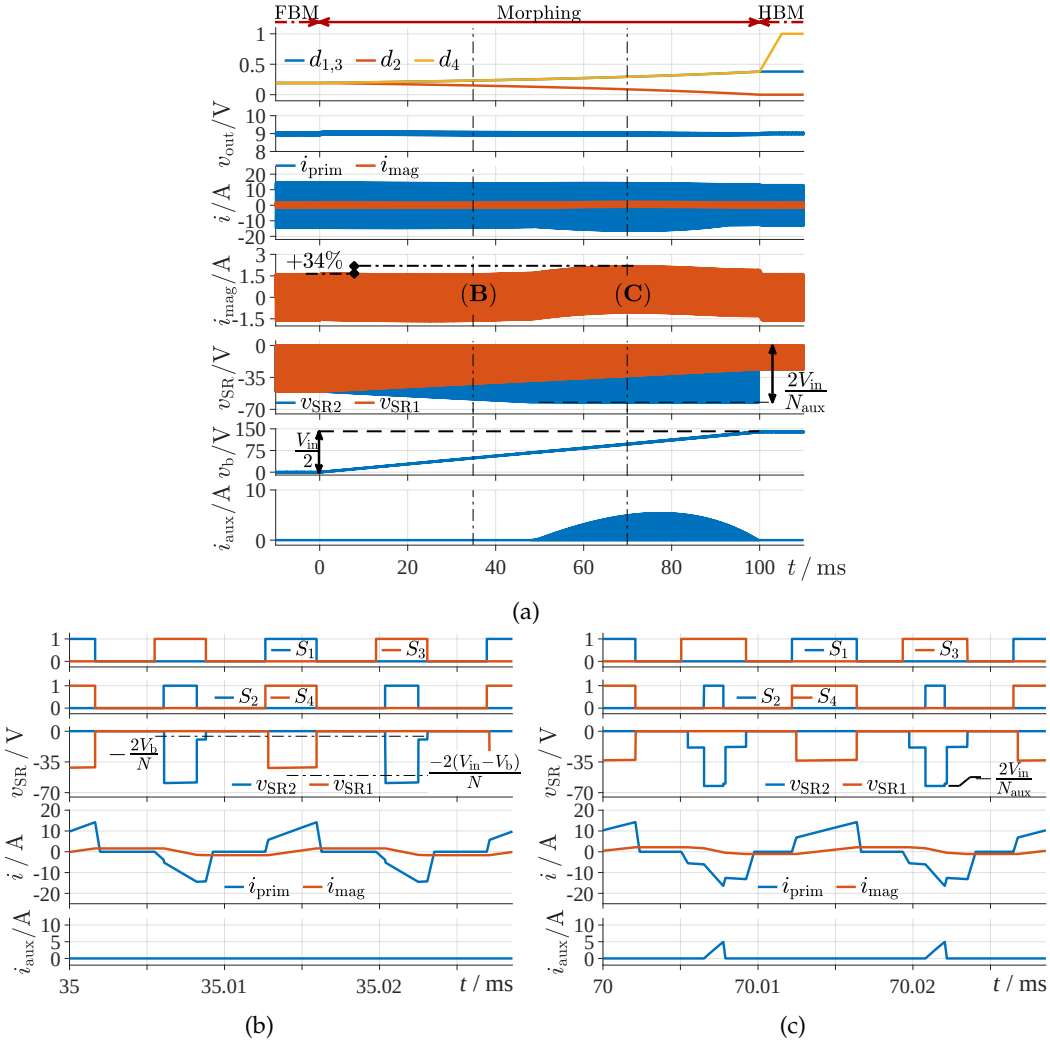


FIGURE 2.125: (a) Visualization of the proposed morphing transition with clamping winding and adjusted duty cycles; (b,c) zoom to the intervals (B,C) depicted in (a) (arameters: $\text{Config}_{2.3j}$).

the beginning of the morphing, this current slope is small since only the (still low)

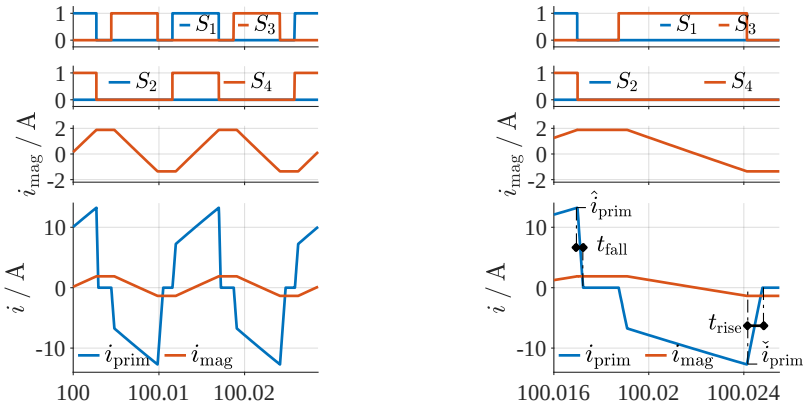


FIGURE 2.126: Persistent magnetizing current offset after the end of the morphing.

blocking capacitor voltage is applied across the series inductance. To overcome this, S_4 can be pulsed with an equal duty cycle compared to S_1 and S_3. This increases the undesired small absolute current slope after the turn-off of S_1 as the current is forced diagonally through the body diodes of S_2 and S_3. The primary voltage v_{prim} is increased from $v_{prim} = -v_b$ to $v_{prim} = -V_{in} - v_b$.

After the blocking capacitor is fully charged (when $d_2 = 0$), the duty cycle of S_4 can be ramped up until it is permanently turned on.

The simulations in Figure 2.125a illustrate this modulation approach. During the morphing, the maximum magnetizing current value increases by 34 % compared to full-bridge modulation, which is significantly smaller compared to the conventional morphing displayed in Figure 2.123a exhibiting 109 %. The now remaining magnetizing current offset follows from those intervals in which the new clamping circuit is activated. The positive clamping current i_{aux} results in an also positive magnetizing current offset.

When the charging of the blocking capacitor is entirely completed ($d_2 = 0$), there is still a remaining magnetizing current offset, which is caused by a difference in the primary current slope. This is visualized in Figure 2.126. Figure 2.126b shows a zoom where the length of slopes can be identified.

When all drive signals are low (while $d_4 = d_1 = d_3$), and there is still a primary current flowing ($|i_{prim}| > 0$), an imbalance in the duration until i_{prim} reaches zero results. When the drive signals are low while $i_{prim} > 0$ (succeeding a turn-on of S_1 and S_4), the voltage applied to the series inductance is $v_{Ls,neg} = -V_{in} - V_b$ leading to a very steep fall time t_{fall} after turning off the primary current at its maximum value $\hat{i}_{prim}$, which is

$$t_{fall} = L_s \frac{\hat{i}_{prim}}{v_{Ls,neg}}. \tag{2.153}$$

When all gate signals are low for $i_{prim} < 0$ (after the turn-on of S_2, S_3), the voltage is $v_{Ls,pos} = V_{in} - V_b$ resulting in a larger rise time t_{rise} after the turn-off current $|\check{i}_{rise}|$, which is

$$t_{\mathrm{rise}} = L_{\mathrm{s}} \frac{|\check{i}_{\mathrm{prim}}|}{v_{\mathrm{Ls,pos}}}. \tag{2.154}$$

The fall and rise times t_{fall} and t_{rise} can be interpreted as duty cycle loss intervals and a difference adds to magnetizing current offset. This magnetizing current offset $\Delta i_{\mathrm{mag},\Delta t}$ can be calculated as

$$\Delta i_{\mathrm{mag},\Delta t} = \frac{\frac{|\check{i}_{\mathrm{prim}}| t_{\mathrm{rise}}}{2} - \frac{\hat{i}_{\mathrm{prim}} t_{\mathrm{fall}}}{2}}{T}. \tag{2.155}$$

If the influence of the magnetizing current i_{mag} on the primary current i_{prim} is small ($|\check{i}_{\mathrm{prim}}| \approx \hat{i}_{\mathrm{prim}}$), the fall time t_{fall} is about a third of the rise time t_{rise} at the end of the morphing interval as $|v_{\mathrm{Ls,neg}}| = 3 v_{\mathrm{Ls,pos}}$ for $V_{\mathrm{b}} = \frac{1}{2} V_{\mathrm{in}}$. Depending on the actual set of parameters, this offset can be quite large, for the simulated parameter set, for instance, it results in an offset of about 26 mA for $t > t_{\mathrm{morph}}$.

C3 Adaption of a variable switching frequency The proposed morphing modulation with a clamping winding still shows a considerable magnetizing current offset resulting in an approximately 34 % larger current value compared to the steady-state modulation ($\hat{p}_{\mathrm{fring,m}} = 1.34$). The offset is primarily caused by the clamping current i_{aux}. By increasing the switching frequency during the transition, it is possible to reduce the dynamic magnetizing current offset and decrease the magnetizing current ripple to fully compensate the effect of the offset on the maximum magnetizing current. To avoid an increased magnetizing current, the frequency is increased by 50 % before the start of the morphing transition and again reduced after 60 % of the morphing time. The reduction may be necessary as the relative duty cycle loss is larger for increased switching frequencies, which may prevent a sufficient gain near half-bridge mode if the switching frequency is not reduced. Additionally, the duty cycle d_4 is increased after 60 % of the morphing time to avoid the effect described in (2.155). Additionally, the aforementioned imbalance of the rectifier currents can somewhat compensate the effects of the clamping current.

Figure 2.127 shows a simulation with the adapted switching frequency and duty cycle d_4. A dynamic increase in the magnetizing current can be largely prevented. These results prove the combination of both adaptions may be used to increase the transformer core utilization.

D Experimental validation

The aforementioned concepts were employed on a prototype shown in Figure 2.128a and being characterized by the parameters in Table 2.10. The transformer consists of $N_{\mathrm{p}} = 10$ primary turns while the clamping winding has $N_{\mathrm{aux}} = 9$ turns. The secondary side comprises single-turn windings $N_{\mathrm{s1}} = N_{\mathrm{s2}} = 1$ made of copper sheets. For the series inductance, a coil with $L_{\mathrm{s}} = 7.2\,\mu\mathrm{H}$ was selected. The clamping diode is a 1200 V device.

To accurately measure the magnetizing flux during the morphing, it is necessary to account for the DC offset as well as the switching-frequency impact on the flux. It is, thus, not possible to measure the voltage-second of a test winding as the time integral of several tens of milliseconds would yield large errors. To account for the DC and the switching-frequency component of the flux signal, the I-prober 520 by

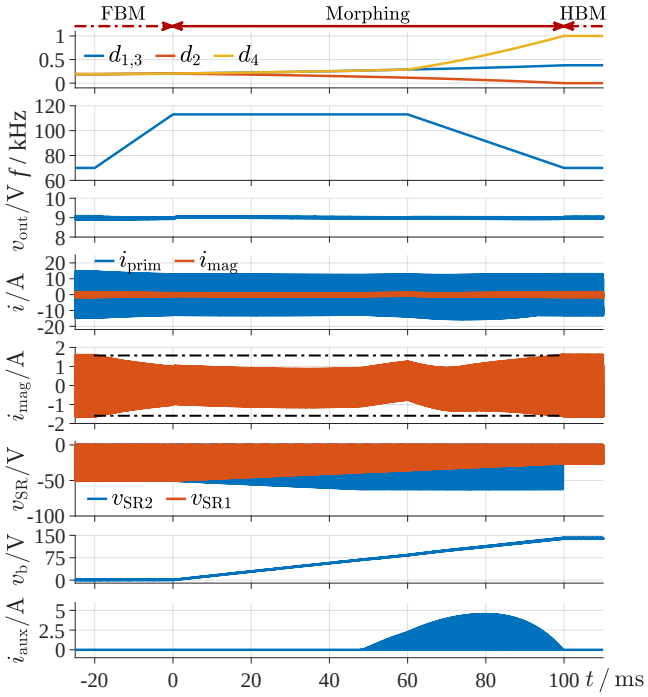


FIGURE 2.127: Morphing transition with adapted switching frequency and duty cycle d_4 to reduce the maximum magnetizing current (parameters: $\text{Config}_{2.3j}$).

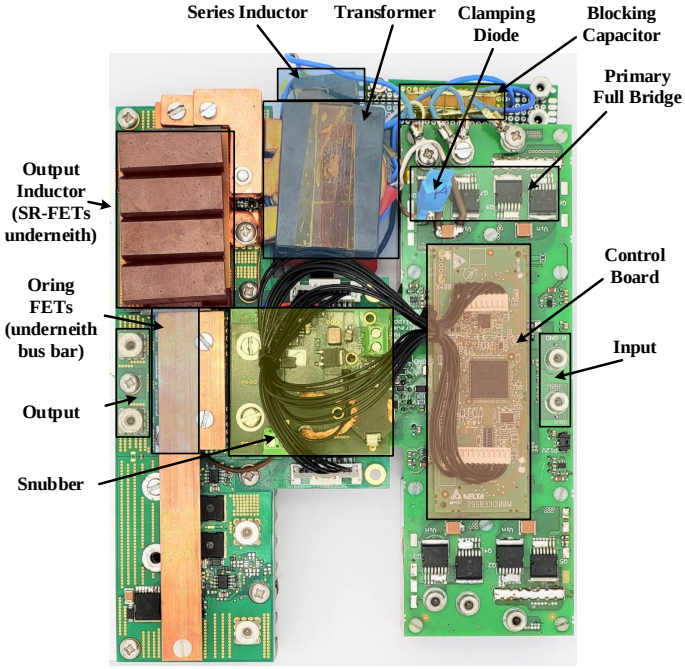
TABLE 2.10: Prototype parameters

Component	Type
Primary MOSFETs	C3M0060065J
Rectifier MOSFETs	IAUT300N10S5N015 (2 par.)
Clamping diode	VS-20ETF10-M3
ORing FETS	IPT026N10N5 (3 parallel)
Series inductance	7.5 µH, PQ32/25
Transformer (N_p:N_{aux}:N_{s1}:N_{s2})	10:9:1:1, ER54/38/30
Blocking capacitance	14 µF

AIM TTi was used, offering a wide measurement range between DC and 5 MHz. It can measure a maximum flux density of 2.5 mT, such that the probe can be employed at the glue spots where the flux density is low. Even the small gap where the glue is applied produces a sufficient fringing flux to measure the flux shape implicitly. The measurement setup is displayed in Figure 2.128b.

Two exemplary operating points are depicted in Figure 2.129 showing a full-bridge operation in (a) and a half-bridge operation in (b). The flux sensor measures the fringing flux b_f, which is of a similar shape to the magnetizing current of the converter. It is evident that the measurement of the fringing flux b_f accurately represent the magnetizing flux such that this sensor can be successfully employed for the measurement of the morphing.

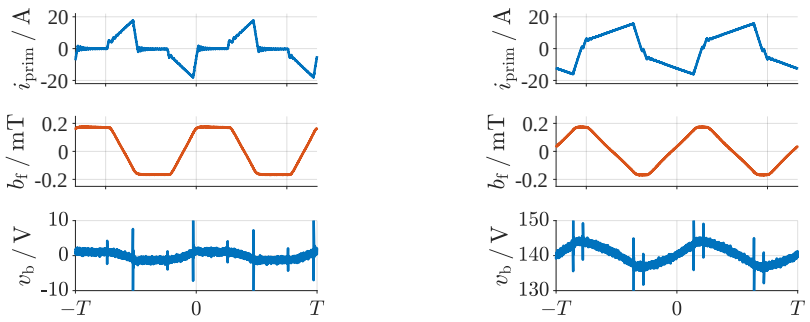
An exemplary transition was performed for an input voltage of $V_{in} = 280\,V$ and output voltage of $V_{out} = 9\,V$ at an output current of $I_{out} = 100\,A$. The switching frequency and duty cycles were set according to the simulation of Figure 2.127.



(a)

(b)

FIGURE 2.128: (a) Developed (two-rail) prototype with only one rail equipped; (b) setup to measure the flux of the transformer.



(a) (b)

FIGURE 2.129: Measurement results for full-bridge mode (a) and half-bridge mode (b). The measurement of the fringing field accurately represents the shape of the magnetizing flux inside the transformer.

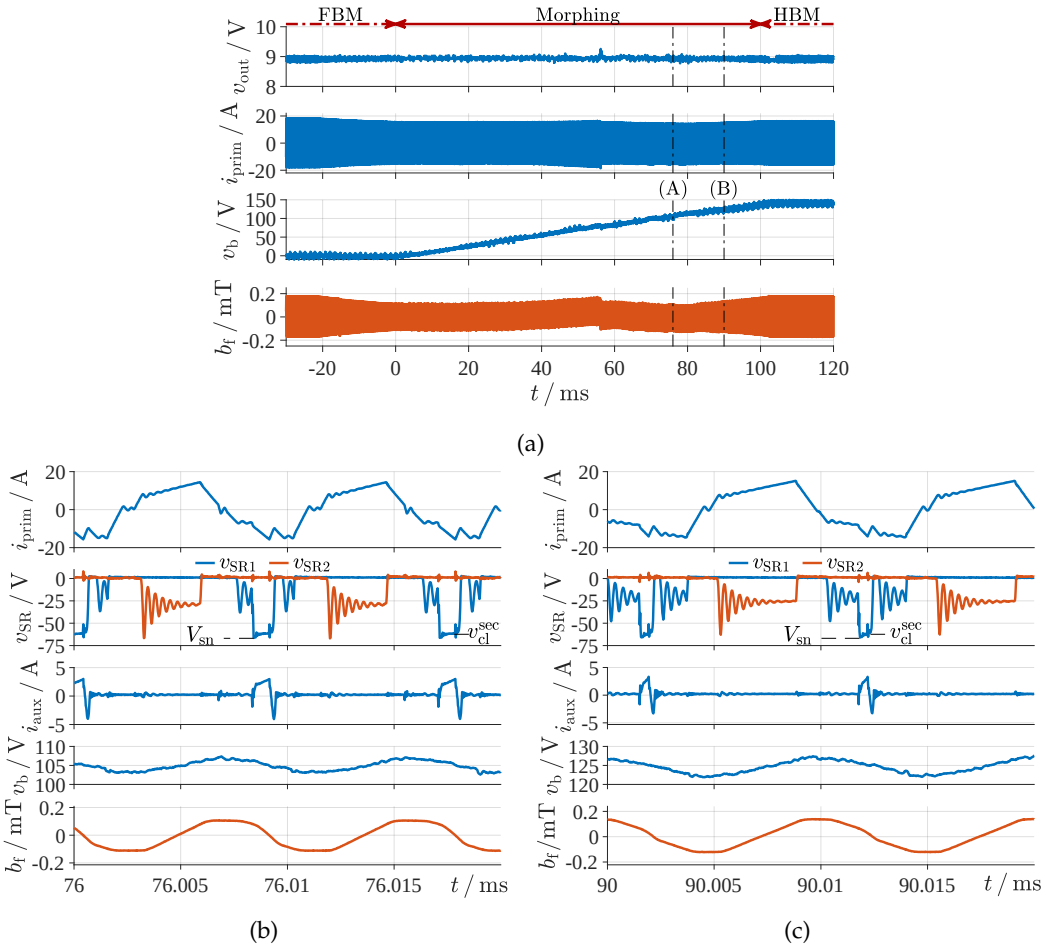


FIGURE 2.130: Experimental measurement results of the clamped topology morphing. (b,c) zoom to the time instances (B,C) displayed in (a) (parameters: $\text{Config}_{2.3k}$).

The measurement results are depicted in Figure 2.130. It is evident that the output voltage was smoothly controlled with no large under- or overshoots. Similarly, during the morphing, the transformer flux stays below the respective maxima and minima of the full- and half-bridge operation. Zooms are shown for two time instances in Figure 2.130b and Figure 2.130c. It is obvious that the synchronous-rectifier blocking voltage was limited through the clamping winding and the snubber. While the snubber limits the blocking voltage during the first couple of nanoseconds, the clamping winding limits the rectifier voltage for most of the time. Neglecting stray components, the designed secondary-side clamping voltage is 62 V (according to (2.147)). The measured secondary-side clamping voltage is about 63 V proving the above analysis.

The most notable difference between the simulations of Figure 2.127 and the measurement results displayed in Figure 2.130 is the reverse-recovery current of the clamping diode. This reverse-recovery alters the shape of the primary current i_{prim} and the blocking voltage v_{SR1}. For v_{SR1}, it results in an interval after clamping where $v_{\text{SR1}} = 0$.

Overall, the experimental results prove the proposed concept. The reverse voltages of the synchronous rectifier devices were well limited while the transformer

flux does not show a significant increase compared to the half- or full-bridge operation.

E A realization option with TVS diodes

The aforementioned method requires an additional winding N_{aux} on the transformer with a good coupling coefficient to the primary winding N_{p}. This may be costly, produces additional winding losses and may increase the transformer size. The method, thus, comes with a high price as it reduces the efficiency and increases the costs. For that purpose, this section describes a method where the additional clamping winding is replaced by two additional diodes of which at least one of them is a transient voltage suppressor (TVS) diode.

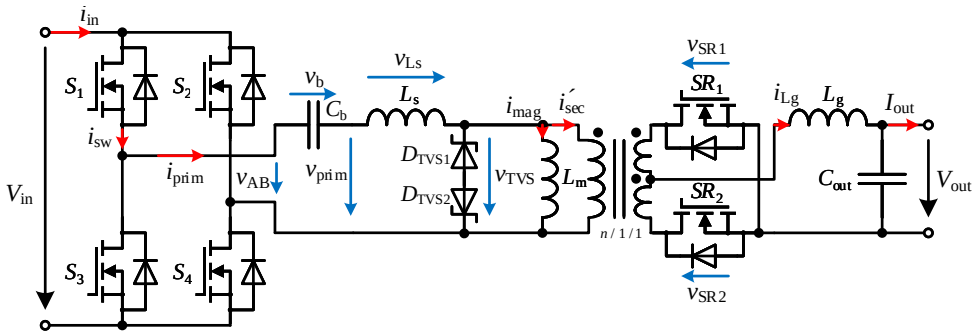


FIGURE 2.131: Isolated full-bridge converter with discrete series inductance L_{s} and TVS diodes for synchronous rectifier over voltage protection. Both TVS diodes are required if the circuit is to enter both half-bridge configurations ($\bar{v}_{\text{b}}^{\text{HB}} \in \{-\frac{V_{\text{in}}}{2}, \frac{V_{\text{in}}}{2}\}$). If the circuit is to enter only one of the half-bridge configurations, one of the TVS diodes can be replaced by an ordinary diode.

The circuit is depicted in Figure 2.131. The inductance L_{s} is a discrete component whereas the stray inductance of the transformer T is neglected in the visualization. The clamping circuit is similar to the clamping circuitry of the LLC presented in [Fig+11]. However, whereas [Fig+11] used a connection to ground and the high input voltage potential, this is not possible here. The diodes are instead connected in parallel to the transformer. In the visualization both diodes are depicted as TVS diodes. However, two TVS diodes are only necessary if the converter is to enter both half-bridge configurations ($\bar{v}_{\text{b}}^{\text{HB}} \in \{-\frac{V_{\text{in}}}{2}, \frac{V_{\text{in}}}{2}\}$). If, however, only one half-bridge configuration is required, one of these diodes can be replaced by a common diode. If the converter is to transition from $\bar{v}_{\text{b}} = 0$ to $\bar{v}_{\text{b}} = \frac{V_{\text{in}}}{2}$, the diode D_{TVS1} can be replaced by a normal diode, whereas if the converter is to transition from $\bar{v}_{\text{b}} = 0$ to $-\bar{v}_{\text{b}} = \frac{V_{\text{in}}}{2}$, the diode D_{TVS2} can be replaced by a normal diode.

The TVS clamping voltage $V_{\text{clamp}}^{\text{TVS}}$ should be selected as the maximum selected stationary transformed synchronous-rectifier voltage $v_{\text{clamp}}^{\text{sec}}$such that the TVS voltage is dimensioned as

$$V_{\text{clamp}}^{\text{TVS}} = \frac{n}{k} v_{\text{clamp}}^{\text{sec}}. \tag{2.156}$$

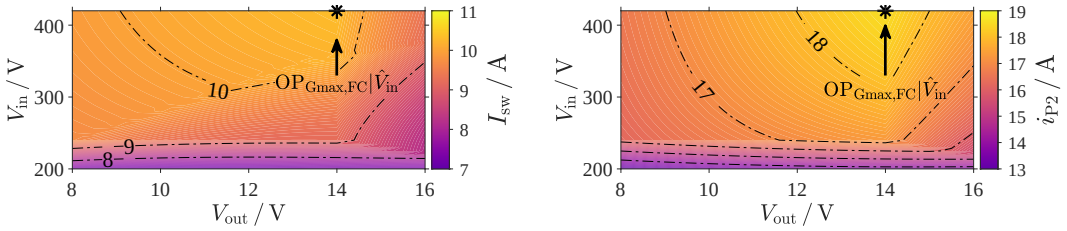
where again k is the rectifier coefficient with $k = 1$ representing a full-bridge rectifier and $k = 2$ the center-tapped rectifier stage and n is the conversion ratio of the transformer.

If the voltage $|v_{\text{prim}}|$ exceeds the maximum absolute TVS voltage $|v_{\text{TVS}}|$, the

diodes start conducting such that the voltage difference is applied to the series inductance $v_{\mathrm{Ls}} = v_{\mathrm{prim}} - v_{\mathrm{TVS}}$. One of the diodes hereby conducts in its forward direction with a negligible forward voltage whereas the other diode is clamping to its reverse voltage $V_{\mathrm{clamp}}^{\mathrm{TVS}}$, which was selected according to (2.156). For a conventional operation in half-bridge or full-bridge operation, the voltages applied to the transformer $v_{\mathrm{prim}}^{\mathrm{conv}}$ should be always smaller than the TVS voltage ($|v_{\mathrm{prim}}^{\mathrm{conv}}| < V_{\mathrm{clamp}}^{\mathrm{TVS}}$) such that the TVS diodes are not conducting.

F Conclusion

The conventional morphing of the isolated full-bridge converter shows some considerable voltage stress for the rectifier semiconductors and an increased magnetizing flux for the transformer. This issue was solved by using an additional clamping winding and a modified modulation scheme. Simulation results and experiments prove the proposed concepts showing that the rectifiers' reverse voltage was substantially reduced by about 20 % while the transformer does not show any increased magnetizing flux. With the introduced methods, rectifier elements of reduced blocking voltage can be employed and the transformer can be designed with an about 50 % reduced core cross section. Additionally, a variant with TVS diodes is presented that does not require an additional winding on the transformer.



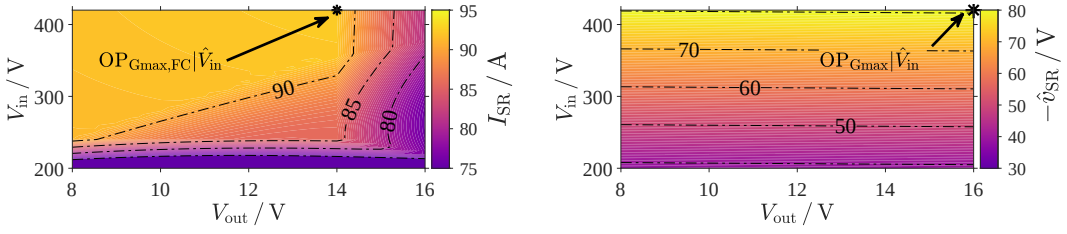
(a) RMS current of S_1 (b) turn-off current of S_1

FIGURE 2.132: Visualization of the primary switch RMS current and turn-off current over the input and output voltage at full load.

2.3.4 Characteristic operating points of the phase-shifted full bridge

It is suitable to choose characterizing operating points for the design of the phase-shifted full-bridge in order to analyze the stressing values through a frequency-independent method in a later stage. Therefore, this section provides an analysis of the full-load and partial-load stressing values over the input and output voltage. The characteristic operating points are then used for the converter design in $\text{Config}_{2.3l}$.

Figure 2.132 depicts the switch RMS current I_{sw} (Figure 2.132a) and the leading-leg turn-off current i_{P2}[1] (Figure 2.132b) over the input and output voltage at full load. As was noted in Section 2.3.1A, the stressing values are calculated neglecting parasitic components. For input voltages below $V_{in} = 240\,\text{V}$, it is evident that the derated load reduces both stressing values. The operating point with the largest RMS current I_{sw} and turn-off current i_{P2} is $\text{OP}_{\text{Gmax,FC}}|\hat{V}_{in}$. At this operating point, the full current is delivered to the output (no power limitation). Furthermore, the increased output inductor ripple (see Figure 2.134a) adds to the component stress.



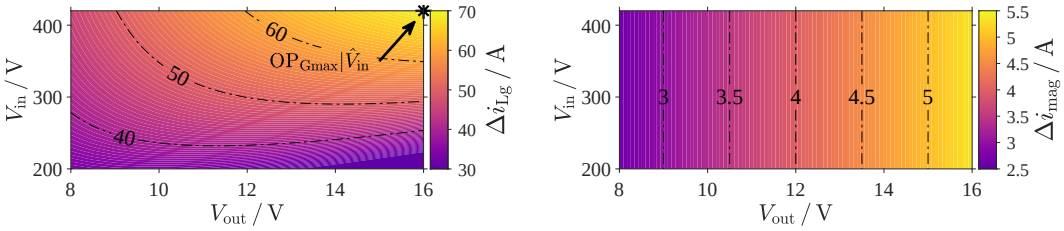
(a) (b)

FIGURE 2.133: Visualization of the synchronous rectifier RMS current I_{SR} and rectifier blocking voltage $\hat{v}_{SR}$ over the input and output voltage.

The stressing values of the synchronous rectifiers are depicted in Figure 2.133. Figure 2.133a shows the RMS current I_{SR} over the input and output voltage, whereas Figure 2.133b depicts the blocking voltage $-\hat{v}_{SR}$. For the RMS current again the operating point $\text{OP}_{\text{Gmax,FC}}|\hat{V}_{in}$ is the one with the highest values. For higher output voltages, the output power is limited to $P_{out} = 1.82\,\text{kW}$, resulting in a reduced output current, the effect of which can be clearly recognized. Each synchronous rectifier conducts the output current[2] for one half period such that for almost the entire operating range, the RMS current is similar. However, the effect of the output inductor

[1] while it is here referred to as leading-leg turn-off current, it is of course possible to employ the a²PSM; for the analysis of the stressing values, the employed modulation, however, is insignificant.

[2] the maximum output current is constant within the range $V_{out} \in \{8, 14\}\,\text{V}$, $V_{in} \in \{240, 420\}\,\text{V}$.



(a) (b)

FIGURE 2.134: Visualization of the output current ripple Δi_{Lg} and magnetizing current ripple Δi_{mag} over the input and output voltage.

TABLE 2.11: Operating points with the maximum component stress

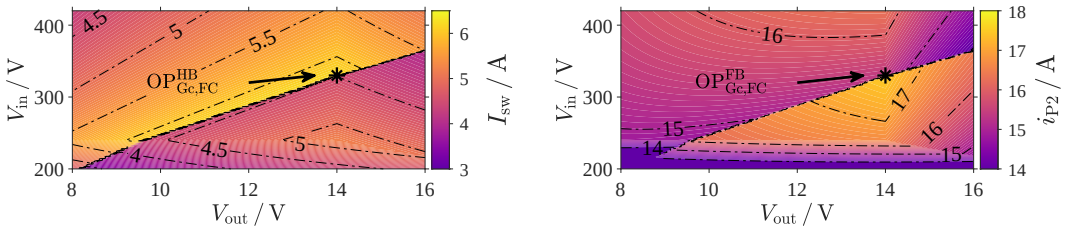
Abbreviation	OP (V_{in} ,V_{out} ,I_{out})	component
$OP_{Gmax,FL}\|\hat{V}_{in}$	420 V, 16 V, 114 A	T, L_g, V_{SR}
$OP_{Gmax,FC}\|\hat{V}_{in}$	420 V, 16 V, 114 A	I_{SR}, I_{sw}, i_{P2}
$OP_{Gmax,DL}$	200 V, 16 V,100 A	D

ripple is also visible here as it results in a larger RMS current for higher input and output voltages. The synchronous rectifier voltage $-\hat{v}_{SR}$[1] increases with increased input voltages, which is expected. The operating point with the maximum synchronous rectifier voltage is $OP_{Gmax}|\hat{V}_{in}$. The slightly higher synchronous rectifier voltage at higher output voltages hereby results from the inductor voltage calculation during $t_{ON,D1}$. However, this effect is only minor and insignificant for the stressing values.

Figure 2.134 shows the current ripple of the magnetizing current (Δi_{mag}) and the output inductor (Δi_{Lg}). The output inductor current ripple increases with the input and output voltage (Figure 2.134a) whereas the ripple of the magnetizing current increases with the output voltage only (Figure 2.134b). For both components, the operating point $OP_{Gmax}|\hat{V}_{in}$ can be considered characteristic and should be used to dimension the converter.

All characteristic operating points are summarized with their corresponding input and output voltage and output current in Table 2.11. These are used for the later design and comparison of the converter topologies in Section 3.3.

[1] the voltage is visualized for a center-tapped rectifier. For a full-bridge rectifier, the voltage would be half as large.



(a) RMS current of S_1

(b) Turn-off current of S_1

FIGURE 2.135: Visualization of the primary switch RMS current I_{sw} and turn-off current i_{P2} over the input and output voltage. For the half-bridge mode (top-left), the switch current is visualized for frequency-doubler modulation.

2.3.5 Characteristic operating points of the isolated full-bridge converter

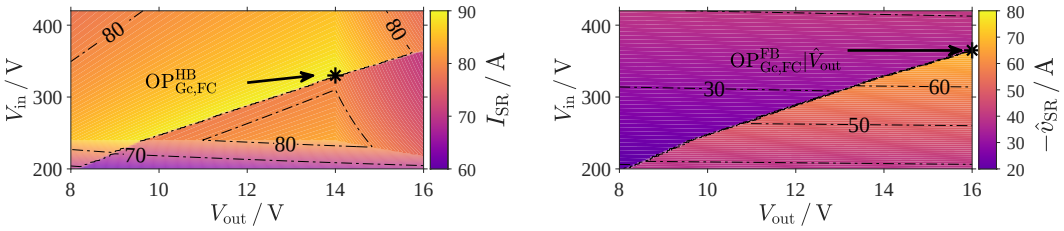
Similar to the phase-shifted full-bridge, it is also necessary to choose characterizing operating points for the design of the isolated full-bridge converter. However, similar to the LLC resonant converter that is driven with different operating modes, the same applies for the isolated full-bridge converter. For this analysis, it shall be considered that the converter changes operating modes from full-bridge to half-bridge whenever the voltage-transfer ratio allows it. Again, the analysis is conducted for full-load and partial-load stressing values over the input and output voltage. The characteristic operating points are then used for the converter design and comparison in $\text{Config}_{2.3m}$.

Figure 2.135 depicts the switch RMS current I_{sw} (Figure 2.135a) and turn-off current i_{P2} (Figure 2.135b) over the input and output voltage at full load. The mode change is clearly visible (full-bridge mode for the lower right, half-bridge mode for the upper left) and also the derated operating region below an input voltage of $V_{in} = 240\,\text{V}$ is evident. The operating point with the largest RMS current I_{sw} and turn-off current i_{P2} is $OP^{HB}_{Gc,FC}$. At this operating point, the full current is delivered to the output (no power limitation) and the duty cycle is high. Additionally, the HSFDM operation is considered for the half-bridge configuration adding to the semiconductor stress.

The stressing values of the synchronous rectifiers are depicted in Figure 2.136. Figure 2.136a shows the RMS current I_{SR} over the input and output voltage whereas Figure 2.136b depicts the blocking voltage $-\hat{v}_{SR}$. For the RMS current again the operating point $OP^{HB}_{Gc,FC}$ is the one with the highest values. The duty cycle is hereby the maximum yielding large RMS currents. The synchronous rectifier voltage $-\hat{v}_{SR}$[1] increases with increased input voltages. As previously noted, the maximum synchronous rectifier voltage is limited by the mode change (upper left). For large input voltages, the converter is switched to the half-bridge mode reducing the blocking voltages by a factor of two. The operating point with the maximum synchronous rectifier voltage is $OP^{FB}_{Gc,FC}|\hat{V}_{out}$.

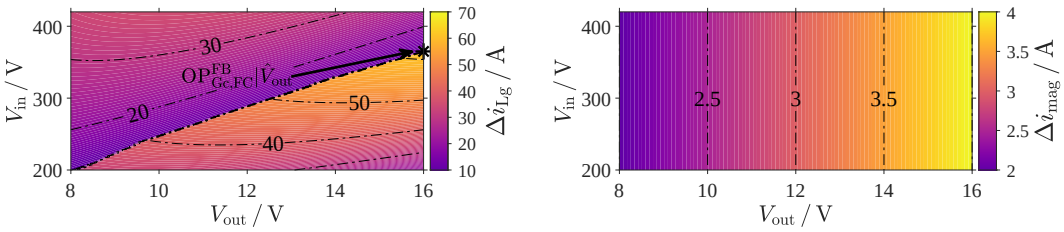
Figure 2.137 shows the current ripple of the magnetizing current (Δi_{mag}) and the output inductor (Δi_{Lg}). The output inductor current ripple increases with the input and output voltage (Figure 2.137a) and again is also limited by the mode change.

[1] the voltage is visualized for a center-tapped rectifier. For a full-bridge rectifier, the voltage would be half as large.



(a) (b)

FIGURE 2.136: Visualization of the synchronous rectifier RMS current I_{SR} and rectifier blocking voltage $\hat{v}_{SR}$ over the input and output voltage.



(a) (b)

FIGURE 2.137: Visualization of the output current ripple Δi_{Lg} and magnetizing current ripple Δi_{mag} over the input and output voltage.

The operatig point with the largest ripple is $OP^{FB}_{Gc,FC}|\hat{V}_{out}$. The magnetizing current increases with the output voltage only (Figure 2.137b). The mode change does not have any effect on the magnetizing current as the half-bridge mode requires twice as large duty cycles that add to the current ripple. For the magnetizing current, the operating point with the largest ripple ($OP_{Gmax}|\hat{V}_{in}$) can be considered characteristic and should be used to dimension the converter.

All characteristic operating points are summarized with their corresponding input and output voltage and output current in Table 2.12. These are used for the later design and comparison of the converter topologies in Section 3.3.

TABLE 2.12: Operating points with the maximum component stress

Abbreviation	OP (V_{in} ,V_{out} ,I_{out})	component
$OP^{FB}_{Gc,FC}$	$*$, 14 V, 130 A	I_{sw}, I_{SR}
$OP^{HB}_{Gc,FC}$	$*$, 14 V, 130 A	i_{P2}
$OP^{FB}_{Gmax,FL}$	$*$, 16 V, 114 A	$\hat{v}_{SR}$, Δi_{Lg}, Δi_{mag}
$OP_{Gmax,DL}$	200 V, 16 V,100 A	D

2.4 On the Analysis Efficacy for 800 V Systems

this section has been previously published in parts in [RSB22e]
and the presented method has been applied for patent in [RSB22a].

The aforementioned analysis focused specifically on traction batteries with a nominal voltage of 400 V. However, the 800 V battery is becoming more and more relevant in electric vehicles, which yields the question, how relevant the aforementioned analysis is for an increased traction battery voltage. This section shows that when employing flying-capacitor inverters as a replacement of the conventional half- or full-bridge, the aforementioned analysis is in part transferable. This is specifically advantageous as due to the beneficial figure of merit of lower-voltage semiconductors [Azu+19; Deb17; Kol21b; Kol21a], switching losses and conduction losses can be reduced when employing semiconductors of a lower blocking voltage. As a result, multi-level flying capacitor have been shown to be an attractive solution for power-factor correction stage (PFC)s and inverter stages due to their increased output frequency[1] and the application of semiconductors of lower voltage. For PFCs or inverters they show outstanding performance [Lei+17; Azu+21; Azu+19]. However, flying-capacitor inverters have not yet been discussed in the application of DC-DC converters.

Consequently, this section analyzes the 3-level (3L) flying capacitor (FC) module as a replacement for the conventional half bridge or full bridge to be employed for higher input voltages. It discusses flying-capacitor voltage control options when being employed for the conventional half- or full-bridge LLC with a flying-capacitor inverter and proposes a simple-to-implement modulation to fully utilize the benefits of the 3L structure of the FC module. It explores potential applications to propose a flying capacitor phase shift converter and a three-phase 3L LLC with a five-level line-to-line voltage.

2.4.1 Introduction

The FC cell (cf. Figure 2.138b) can be used to replace the traditional full-bridge inverter as visualized in Figure 2.138a. The flying capacitor inverter can hereby be operated among the following switching states, which are visualized in Figure 2.139:

- $v_{\mathrm{inv}} = V_{\mathrm{in}}$ (ET^{+}, see Figure 2.139a),
- $v_{\mathrm{inv}} = 0$ (ET^{-}, see Figure 2.139b),
- $v_{\mathrm{inv}} = V_{\mathrm{in}}/2$ (FW^{+}, see Figure 2.139c),
- $v_{\mathrm{inv}} = V_{\mathrm{in}}/2$ (FW^{-}, see Figure 2.139d).

The inverter output, thus has the voltage levels $v_{\mathrm{inv}}^{\mathrm{FC}} = \{V_{\mathrm{in}}, \frac{V_{\mathrm{in}}}{2}, 0\}$. For an input voltage of 800 V, these levels are $v_{\mathrm{inv}}^{\mathrm{FC}} = \{800\,\mathrm{V}, 400\,\mathrm{V}, 0\,\mathrm{V}\}$. The voltage levels of the flying-capacitor inverter are in direct correlation to the voltage levels of a full-bridge inverter, which were visualized in Figure 2.5. These voltage are $v_{\mathrm{inv}}^{\mathrm{FB}} = \{V_{\mathrm{in}}, 0, -V_{\mathrm{in}}\}$.

[1] by employing a multi-level converter, the mean switching frequency of the individual switches is kept constant whereas the frequency of the complete stage increases [Ada+09; SWT16; Wan+04]. Furthermore, the applied voltage steps are reduced, which results in a lower current ripple.

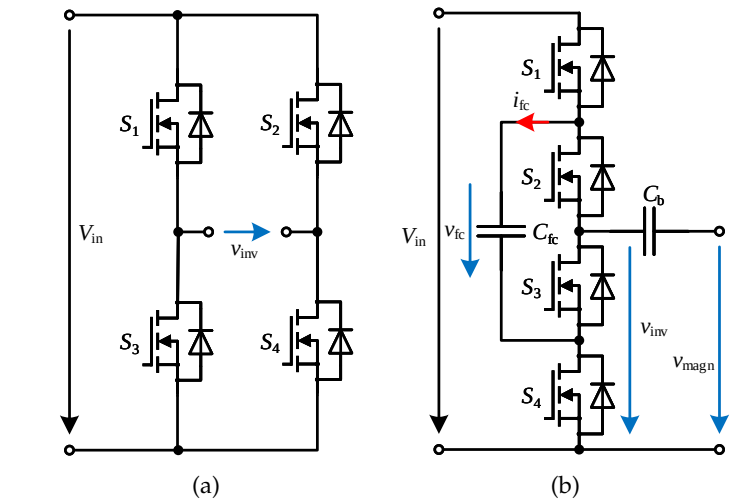


FIGURE 2.138: (a) Traditional full-bridge module, and (b) the flying capacitor module with a blocking capacitor.

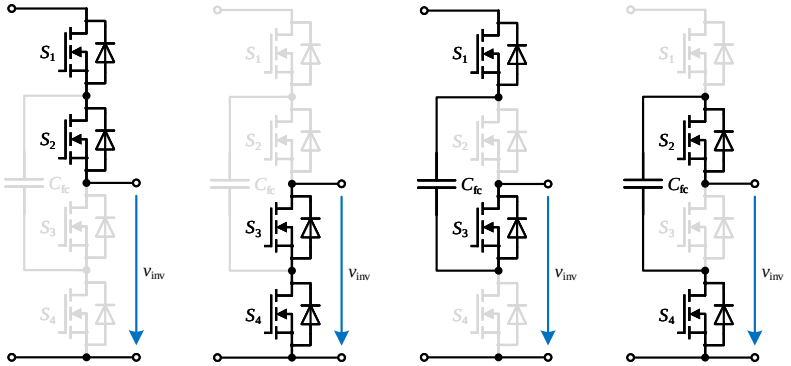


FIGURE 2.139: Switching states of the flying-capacitor module.

For an input voltage of 400 V, these levels are $v_{inv}^{FB} = \{400\,V, 0\,V, -400\,V\}$. The voltage levels of a flying capacitor inverter operated at 800 V, are, thus, equal to the voltage levels of a full-bridge inverter operated at 400 V with the only difference being the offset of the flying-capacitor voltage inverter voltage by 400 V, which needs to be blocked by a capacitor (cf. C_b in Figure 2.138b). The subsequent voltage levels applied to the magnetic components (v_{magn} in Figure 2.138b) are then equal to the inverter voltage of the full-bridge inverter (cf. Figure 2.138a). The flying-capacitor inverter and full-bridge inverter are compared for the two different voltage levels in Table 2.13.

Exemplary applications of a flying-capacitor inverter are converters that typically employ a primary full-bridge like the full-bridge LLC or HSFB. However, in contrast to the full-bridge inverter where the voltage levels are predetermined, the flying capacitor voltage v_{FC} must be controlled to half of the input voltage ($v_{FC} = V_{in}/2$) to ensure that every MOSFET is only stressed with half of the input voltage and avoid a dynamic increase of this voltage.

Therefore, Section 2.4.2 focuses on controlling the flying capacitor voltage and proposes an easy-to-implement 3L modulation to fully exploit the 3L structure of the FC converter, enabling a quasi phase-shift modulation voltage pattern to control the flying-capacitor voltage and to propose a stable phase-shift flying-capacitor

TABLE 2.13: Comparison of the full-bridge inverter and the flying-capacitor inverter.

	flying-capacitor inverter at $V_{in} = 800\,V$ ($v_{fc} = 400\,V$)	full-bridge inverter at $V_{in} = 400\,V$
inverter voltage levels	{800 V, 400 V, 0 V}	{400 V, 0 V, -400 V}
primary magnetics voltage levels	{400 V, 0 V, -400 V}	{400 V, 0 V, -400 V}
blocking capacitor voltage (in full-bridge mode)	400 V	0 V
primary semiconductor rated voltage	650 V	650 V
number of primary inverter switches	4	4

modulation. With the proposed control mechanism and modulations, this section proves that the analysis of Section 2.1 and Section 2.3 is equally valid for 800 V systems when a flying-capacitor module is employed instead of the full-bridge inverter that was discussed in Sections 2.1 and 2.3[1].

Section 2.4.3 focuses specifically on the flying-capacitor realization of the active-clamp converter where the traditional half-bridge leg of the active-clamp converter is replaced by the flying-capacitor module enabling a variety of modulations that facilitate ZVS of the primary inverter switches. This section, therefore, proves the validity of Section 2.2 for 800 V systems when employing a flying-capacitor inverter.

2.4.2 Controlling the flying-capacitor voltage and enabling a flying-capacitor phase-shift modulation

To fully utilize the FC module, a control mechanism must be found to regulate the FC voltage and avoid a run-off which would result in an uncontrollable converter and a destruction of the inverter switches.

A Phase-shift operation in flying-capacitor DC-DC converters

When utilizing a phase-shift modulation to the FC module, the switching signals of the semiconductors S_1, S_4 (cf. Figure 2.138b) are phase shifted to the input signals of S_2, S_3 as depicted in Figure 2.140a. Compared to the traditional phase-shift modulation of the full-bridge inverter, this modulation cannot be as easily adapted since for either phase-shift modulation (Figure 2.140a, 2.140b), the flying capacitor current is either negative (cf. Figure 2.140a) or positive (cf. Figure 2.140b) resulting in a run-off of the flying capacitor voltage v_{FC}. Additionally, in the phase-shift modulation,

[1] for the sake of brevity, Section 2.4.2 will omit the description of the flying-capacitor half-bridge operation as it is very similar to the flying-capacitor phase-shift modulation described in this section. It shall be noted at this point that the flying-capacitor half-bridge configuration can be achieved by employing the frequency-doubler modulation transferred to the flying-capacitor inverter. The flying-capacitor half-bridge modulation is naturally unstable and can not be employed.

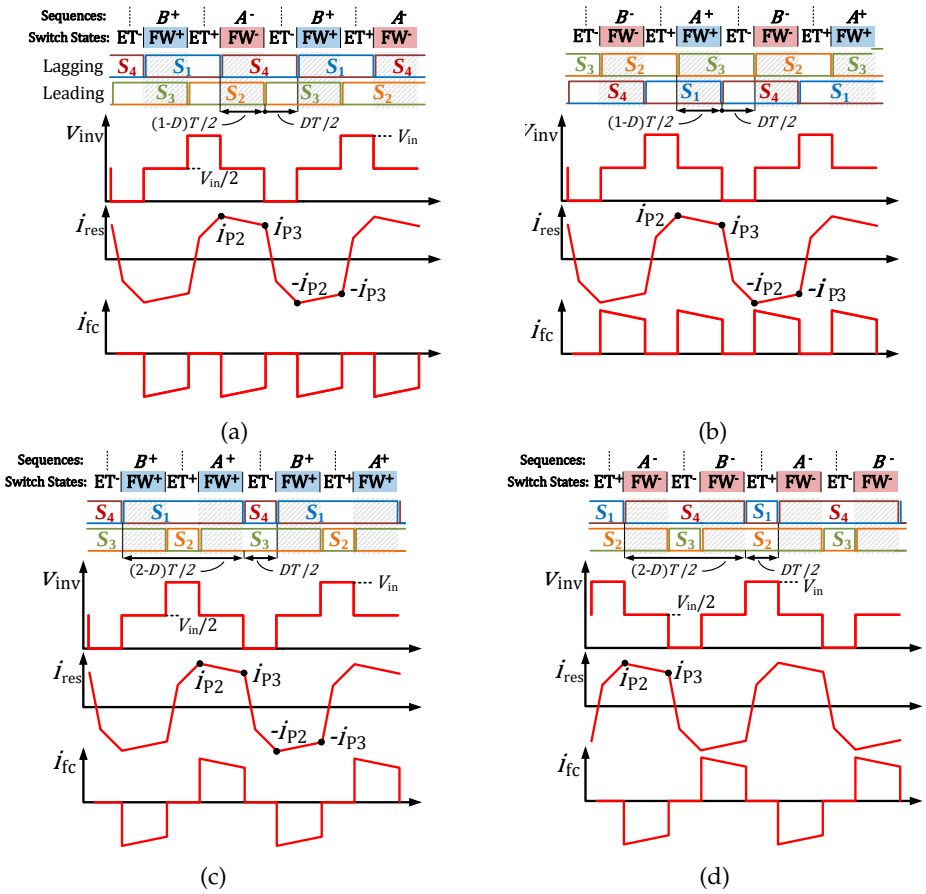


FIGURE 2.140: (Unstable) phase-shift modulation (a,b) and asymmetrical phase-shift modulation (c,d).

the MOSFETs are stressed with different turn-off currents [Mih04; KD21; Reh+21d] as visualized in Figure 2.140a, 2.140b (current values named after [BBK10b]) and conduction losses [Reh+21d].

The same voltage pulses of the phase-shift modulation can also be achieved by the asymmetrical phase-shift modulation or duty-cycle modulation depicted in Figures 2.140c and 2.140d [She+16; WG18; KD21]. This modulation results in positive and negative flying-capacitor currents enabling a full utilization of the three levels of the flying capacitor module in a quasi phase-shift-modulation voltage pattern. However, the modulation results in unbalanced losses since two switches are turned on for $(2-D)T/2$ where $D \in [0,1]$, whereas the other two switches are only turned on for $DT/2$, resulting in unbalanced conduction losses. Additionally, the switches are also turned off at different current levels resulting in unbalanced switching losses.

In the conventional phase-shift modulation, the switching intervals are repeated every period of the transformer current. If the switches S_2 and S_4 are operated as the leading leg, the intervals are repeated in the order

$$\begin{aligned} &\mathbf{ET}^{+}(S_1, S_2) \rightarrow \mathbf{FW}^{-}(S_2, S_4) \rightarrow \\ &\mathbf{ET}^{-}(S_3, S_4) \rightarrow \mathbf{FW}^{+}(S_1, S_3). \end{aligned} \tag{2.157}$$

If the switches S_1 and S_3 are operated as the leading leg, the intervals are repeated in the reverse order:

$$\begin{aligned}&\mathbf{ET}^{+}(S_1, S_2) \rightarrow \mathbf{FW}^{+}(S_1, S_3) \rightarrow \\ &\mathbf{ET}^{-}(S_3, S_4) \rightarrow \mathbf{FW}^{-}(S_2, S_4).\end{aligned} \tag{2.158}$$

Considering the preceding states, four different sequences can be derived: the transition through a freewheeling interval from ET^{+} to ET^{-} labeled type A sequence and the transition through a freewheeling interval from ET^{-} to ET^{+}, which are labeled type B sequence [Reh+21d]. Both transitions can utilize either the positive or negative freewheeling state, which is emphasized through the superscript.

For the A type or B-type transition, the flying capacitor can be either charged or discharged (assuming steady state). The A^{+} transition hereby results in a charging current, whereas the A^{-} transition results in a discharging current:

$$\boldsymbol{A}^{+}(i_{\mathrm{fc}} > 0)): \ \mathbf{ET}^{+}(S_1, S_2) \rightarrow \mathbf{FW}^{+}(S_1, S_3) \rightarrow \mathbf{ET}^{-}(S_3, S_4), \tag{2.159}$$

and

$$\boldsymbol{A}^{-}(i_{\mathrm{fc}} < 0): \ \mathbf{ET}^{+}(S_1, S_2) \rightarrow \mathbf{FW}^{-}(S_2, S_4) \rightarrow \mathbf{ET}^{-}(S_3, S_4). \tag{2.160}$$

The two possible transitions from ET^{-} to ET^{+} (labeled type-B sequence) can also result in a discharging current (B^{+}) or a charging current (B^{-}):

$$\boldsymbol{B}^{+}(i_{\mathrm{fc}} < 0): \ \mathbf{ET}^{-}(S_3, S_4) \rightarrow \mathbf{FW}^{+}(S_1, S_3) \rightarrow \mathbf{ET}^{+}(S_1, S_2) \tag{2.161}$$

and

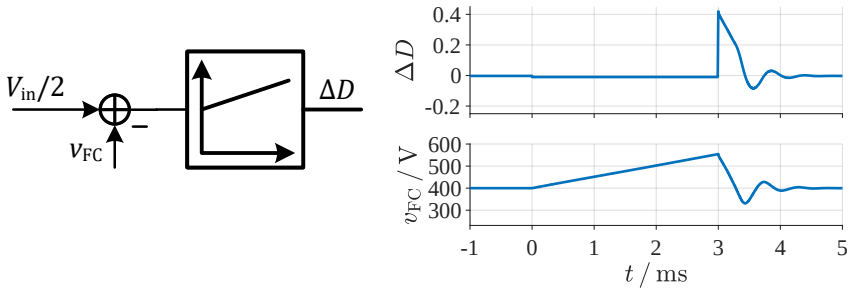
$$\boldsymbol{B}^{-}(i_{\mathrm{fc}} > 0): \ \mathbf{ET}^{-}(S_3, S_4) \rightarrow \mathbf{FW}^{-}(S_2, S_4) \rightarrow \mathbf{ET}^{+}(S_1, S_2). \tag{2.162}$$

This analysis emphasizes the description of above. The conventional phase-shift modulation either results in a continuous discharging current (Figure 2.140a) or continuous charging current (Figure 2.140b).

B Flying-Capacitor Voltage Control for LLC Resonant Converters

While a full utilization of the traditional phase-shift (Figure 2.140a, 2.140b) modulation is not possible for the FC DC-DC converter, the introduction of a phase shift to the gate signals between S_1-S_4 and S_2-S_3 can be utilized to control the FC voltage in an LLC that is traditionally operated with 50 % duty cycle and no phase shift. While ideally the FC current is zero for when there is no phase-shift, even a small delay in the operation may lead to a run-off of the FC voltage and can, therefore, result in a destruction of the switches. By operating S_2-S_3 as the lagging leg (cf. Figure 2.140a, 2.140b) if $v_{\mathrm{FC}} < V_{\mathrm{in}}/2$, and S_1-S_4 as the leading leg if $v_{\mathrm{FC}} > V_{\mathrm{in}}/2$ (in each with only a minor phase shift) the flying capacitor voltage can be controlled.

The control concept to stabilize v_{FC} to $V_{\mathrm{in}}/2$ is depicted in Figure 2.141a. For $\Delta D < 0.5$, the switches S_1-S_4 are leading with the switches S_2-S_3 lagging; for $\Delta D > 0.5$, the switches S_2-S_3 are leading while S_1-S_4 are lagging. Simulation results are depicted for an 2.4 kW LLC in Figure 2.141b for $C_{\mathrm{fc}} = 2\,\mu\mathrm{F}$ with $V_{\mathrm{in}} = 800\,\mathrm{V}$ and $V_{\mathrm{out}} = 48\,\mathrm{V}$, $I_{\mathrm{out}} = 50\,\mathrm{A}$. The resonant parameters are $L_{\mathrm{r}} = 30\,\mu\mathrm{H}$, $L_{\mathrm{m}} = 300\,\mu\mathrm{H}$,



(a) (b)

FIGURE 2.141: (a) Control concept to adjust the flying capacitor voltage v_{FC}. For $\Delta D < 0$, the switches S_1-S_4 are leading, for $\Delta D > 0$, they are lagging; (b) simulation results proving the concept.

$C_r = 90\,\text{nF}$, and $n = 7$. For $0 < t < 3\text{ms}$, the control was turned off. After $t = 3\,\text{ms}$, the control was turned back on, resulting in a stabilization of the flying capacitor voltage. For $\Delta D < 0$, the switches S_1-S_4 are leading; for $\Delta D > 0$ they are lagging. The results show that the flying capacitor voltage can be well controlled to half of the input voltage V_{in}.

C A loss-balancing phase-shift modulation for flying-capacitor DC-DC converters

The preceding section showed that the conventional phase-shift modulation is unsuitable for the application as a flying-capacitor DC-DC converter as it results in a continuous charge or discharge of v_{fc}. While the asymmetrical phase-shift modulation of Figures 2.140c and 2.140d may be an option to utilize quasi phase-shift modulation voltage shapes, it is a non-ideal solution as it results in unbalanced semiconductor losses. To utilize the full potential of the phase-shift modulation in LLCs, this chapter presents a multi-level modulation to achieve quasi-phase-shift modulation voltage shapes. Benefits of phase-shift modulation in LLCs are the potential of employing it for start-up purposes [Che+14; Yan+16], a low-gain loss reduction [MW14; Lo+11; Kim+14; Kim+15], an extension of the operation in wide voltage-transfer ratio applications [Liu+14; Sha+16; RSB21; Reh+20a] or in balancing when utilizing interleaving of multi-rail LLCs [FSG14; Reh+20b; MK16]. To utilize the benefits of the phase-shift operation, several concepts have been presented in literature [AJ06; Guo+18] where both concepts employed additional switches or additional capacitors and diodes. However, this section shows that a modulation exists to achieve these voltage shapes without the need of additional components.

The a²PSM is depicted in Figure 2.142. It uses the same pulse pattern that was used for a conventional full-bridge inverter in [Mih04; KD21; Reh+21d]. To the author's knowledge, no such modulation has yet been utilized to a multi-level inverter. The modulation consists of turn-on intervals of the length $(2-D)T/2$, $T/2$, $DT/2$ and $T/2$ where the pulses are phase-shifted from S_1-S_4 to S_2-S_3 by T. The modulation can be easily implemented on a DSP/microcontroller (e.g. in TI C2000 controllers using the action-qualifier control registers, AQCTL) by using an up-down counter. By employing two PWM units, the same synchronized up-down counter can be utilized where the compare values for one PWM unit (yellow lines) are $(2-D)N_{reg}/4$ and $N_{reg} - DN_{reg}/4$ while for the other PWM unit (dark red lines), they are $DN_{reg}/4$ and $(2+D)N_{reg}/4$. During up-count, the flying-capacitor current is

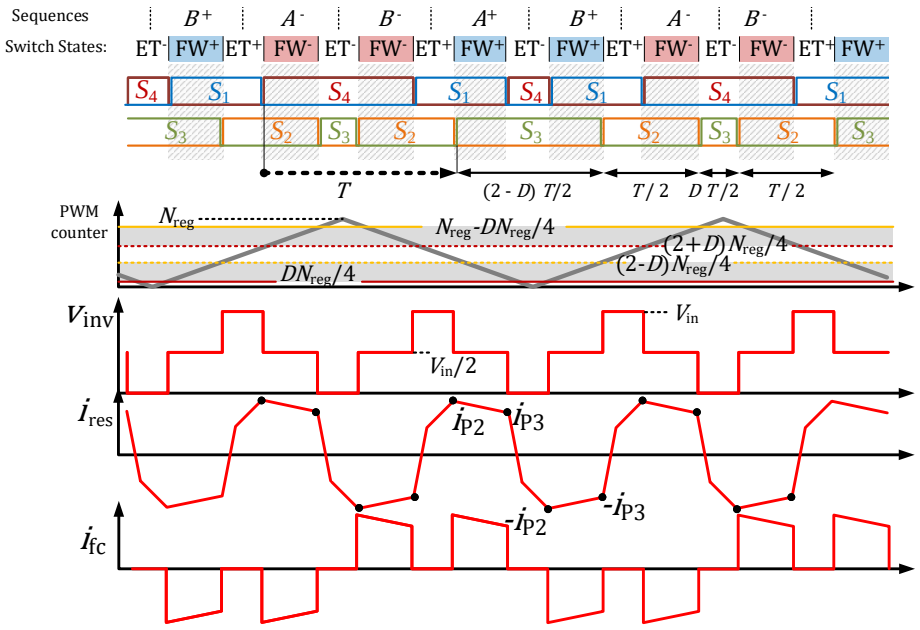


FIGURE 2.142: 3L alternating asymmetrical phase-shift modulation with balanced flying-capacitor currents.

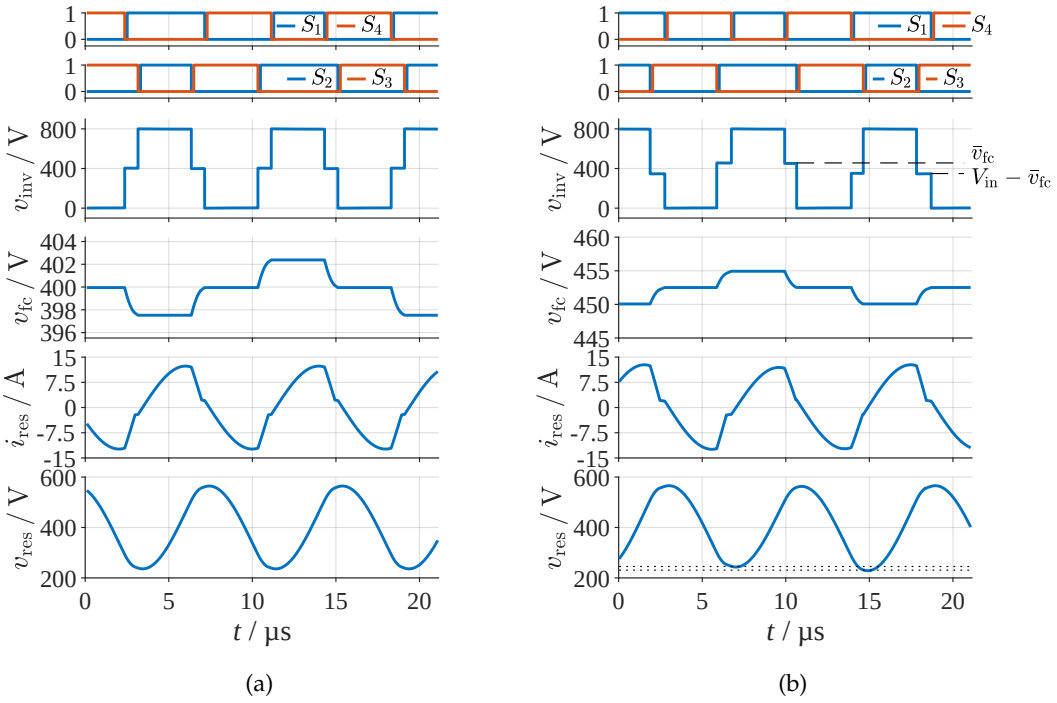


FIGURE 2.143: 3-Level LLC simulation results. (a) balanced operation, (b) unbalanced operation with undesired phase shift of 80 ns for S_1 and S_4 leading to an undesired flying capacitor voltage.

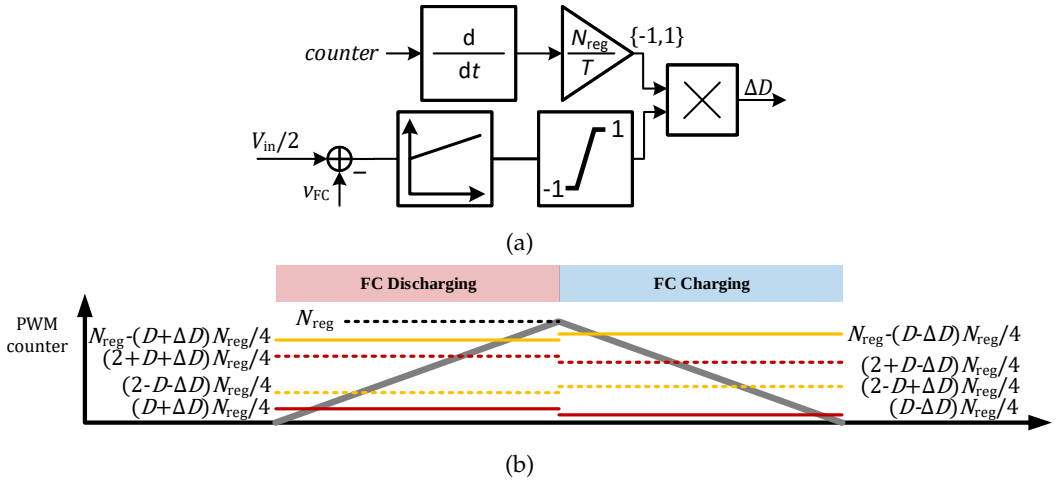


FIGURE 2.144: (a) Control concept to adjust the flying capacitor voltage v_{FC} in the a²PSM. Depending on the counter slope, the compare values are altered; (b) Visualization of the adapted compare values to balance the flying-capacitor voltage by increasing the charging intervals.

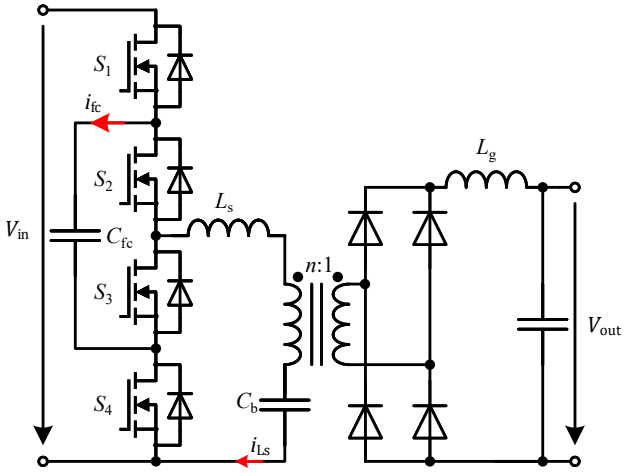


FIGURE 2.145: 3L phase-shift converter with a blocking capacitor C_b.

negative while for down count, it is positive considering steady state[1]. Exemplary simulation results are depicted in Figure 2.143. Figure 2.143a shows ideal simulation results with no delays in the PWM signals. A simulation with an exemplary 80 ns phase shift between the signals of S_1/S_4 and S_2/S_3 is depicted in Figure 2.143b. This modulation results in a non-ideal flying capacitor voltage v_{fc}. In average the voltage is $\bar{v}_{fc} = 452\,V$, 52 V higher than the ideal voltage of $\bar{v}_{fc} = \frac{V_{in}}{2} = 400\,V$. However, contrary to the conventional phase-shift modulation depicted in Figure 2.141b, this does not lead to a continuously increasing/decreasing flying capacitor voltage but results in a steady state offset in the voltage.

A control of the flying-capacitor voltage can be achieved by modifying the compare values for the up- and down count respectively by increasing or decreasing

[1] in this modulation there are two subsequent positive and negative current pulses delivered to the flying capacitor. That means that the FC voltage ripple is twice compared to the modulation depicted in Figures 2.140c and 2.140d. However, this does not mean that the FC capacitance needs to be designed twice as large because the capacitance should be designed large enough to suppress dynamics of the system.

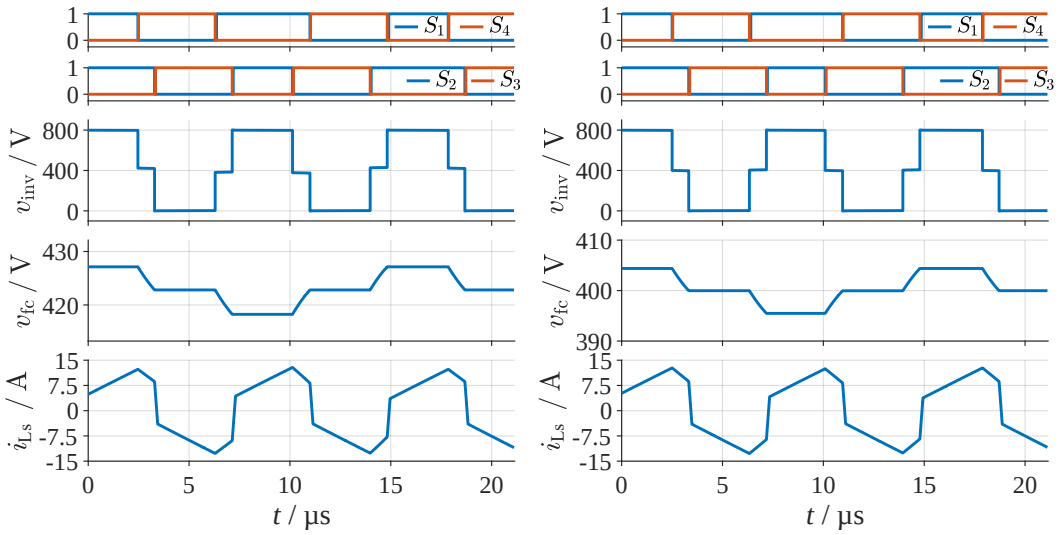


FIGURE 2.146: 3-Level PSFB converter simulation results. (a) unbalanced operation with undesired delay of 20 ns for S_1 leading to an undesired flying capacitor voltage (b) balanced operation (controlled, $\Delta D = 0.01$) with undesired delay of 20 ns for S_1 leading to the desired operation.

the freewheeling intervals during the respective counter slope. The upper two compare values are, thus, modified to $(2 + D - \Delta D)N_{\mathrm{reg}}/4$ and $N_{\mathrm{reg}} - (D - \Delta D)N_{\mathrm{reg}}/4$ whereas the lower two compare values are modified to $(2 - D + \Delta D)N_{\mathrm{reg}}/4$, and $(D - \Delta D)N_{\mathrm{reg}}/4$ where ΔD is determined as visualized in Figure 2.144a. The modified compare values are depicted in Figure 2.144b.

With the proposed modulation, it is possible to create a flying-capacitor phase-shift converter (*phase-shifted full bridge* as depicted in Figure 2.145. The blocking capacitor C_{b} is used to block half of the input voltage and is setup with a large capacitance. Simulation results are depicted in Figure 2.146 where Figure 2.146a shows a simulation with an introduced delay of 20 ns for S_1 and Figure 2.146b shows simulation results with the balance control, resulting in the desired flying capacitor voltage.

D Mode control of the flying capacitor voltage in the loss-balancing modulation

While the preceding section presented a modulation to balance the flying capacitor voltage, it is also possible to control the operating mode to dynamically control the flying capacitor voltage when necessary[1]. For that purpose, the conventional phase-shift modulation that was presented in Figure 2.140 can be employed. Figure 2.147 shows the standard PSM with an up-down counter as it was used for the 3L-a²PSM. By comparing it to the 3L-a²PSM visualized in Figure 2.142, it is evident that the same compare values can be employed with different actions during up and down count[2]. These modes can, thus, be used for controlling the flying capacitor voltage. An exemplary state machine is visualized in Figure 2.148.

This state machine was implemented in a simulation model and the results are

[1] the flying capacitor voltage may drift during transients. It can also be necessary to control the flying capacitor voltage during startup.

[2] considering the employed Texas Instruments controllers, this can be done through modification of the action qualifier registers.

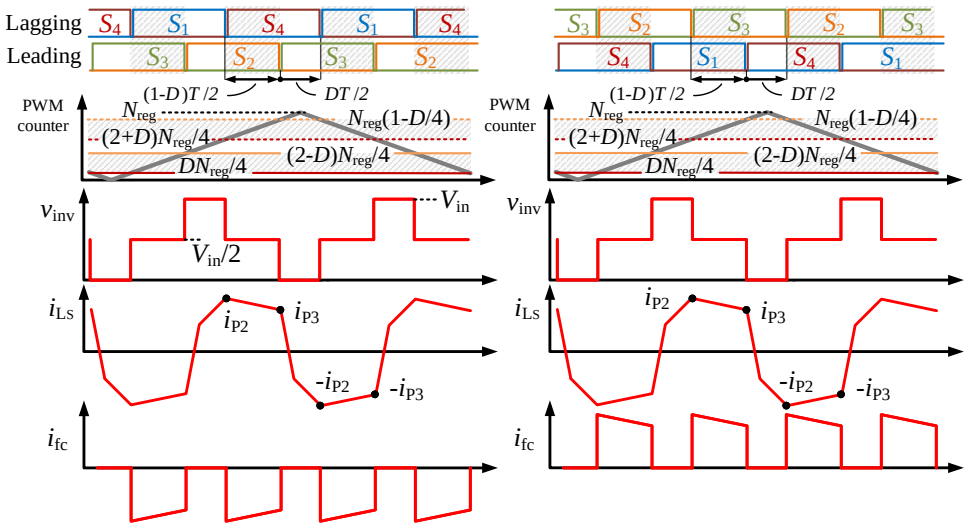


FIGURE 2.147: Standard three-level phase-shift modulation employed with an up-down counter

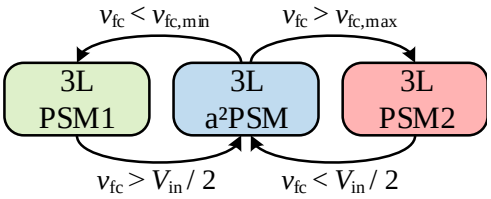


FIGURE 2.148: Exemplary state machine for controlling the flying capacitor voltage using three modes of operation.

visualized in Figure 2.149. Figure 2.149a shows the overall simulation with reference steps at $t = 0\,\text{ms}$ and $t = 0.2\,\text{ms}$ whereas Figures 2.149b and 2.149c show the transition from one mode to the other. The charging PSM is visualized in orange and abbreviated PSM$^+$ whereas the discharging PSM is visualized in green and abbreviated PSM$^-$. The top and bottom threshold for an acceptable flying capacitor voltage v_{fc} is visualized in grey in Figure 2.149a. The results show that there is no oscillation stemming from the mode change in the primary transformer current i_{Ls}. The flying capacitor voltage is smoothly increased and decreased. It can, therefore, be assessed that type of flying capacitor voltage control is working successfully.

E Efficacy of flying-capacitor inverters to replace full-bridge inverters

Multi-level flying-capacitor converters are an attractive solution to exploit the beneficial figure of merit of semiconductors with a lower blocking voltage. The flying-capacitor inverter can be used to replace the full-bridge inverter when higher input voltage are required. The section proved that the phase-shift modulation can be utilized to adjust the flying capacitor voltage of half-bridge LLC and proposed a modulation to fully exploit the 3L structure of the FC module. Consequently, a FC phase-shift converter and a 3L LLC are proposed along with a concept to control the voltage to the desired value. While the 3-level hard-switched full-bridge converter (which concept is equal to the 3-level phase-shift converter) has not been analyzed by this section, it is trivial that the flying-capacitor voltage of this converter can equally be balanced by introducing short freewheeling intervals after the energy-transfer interval.

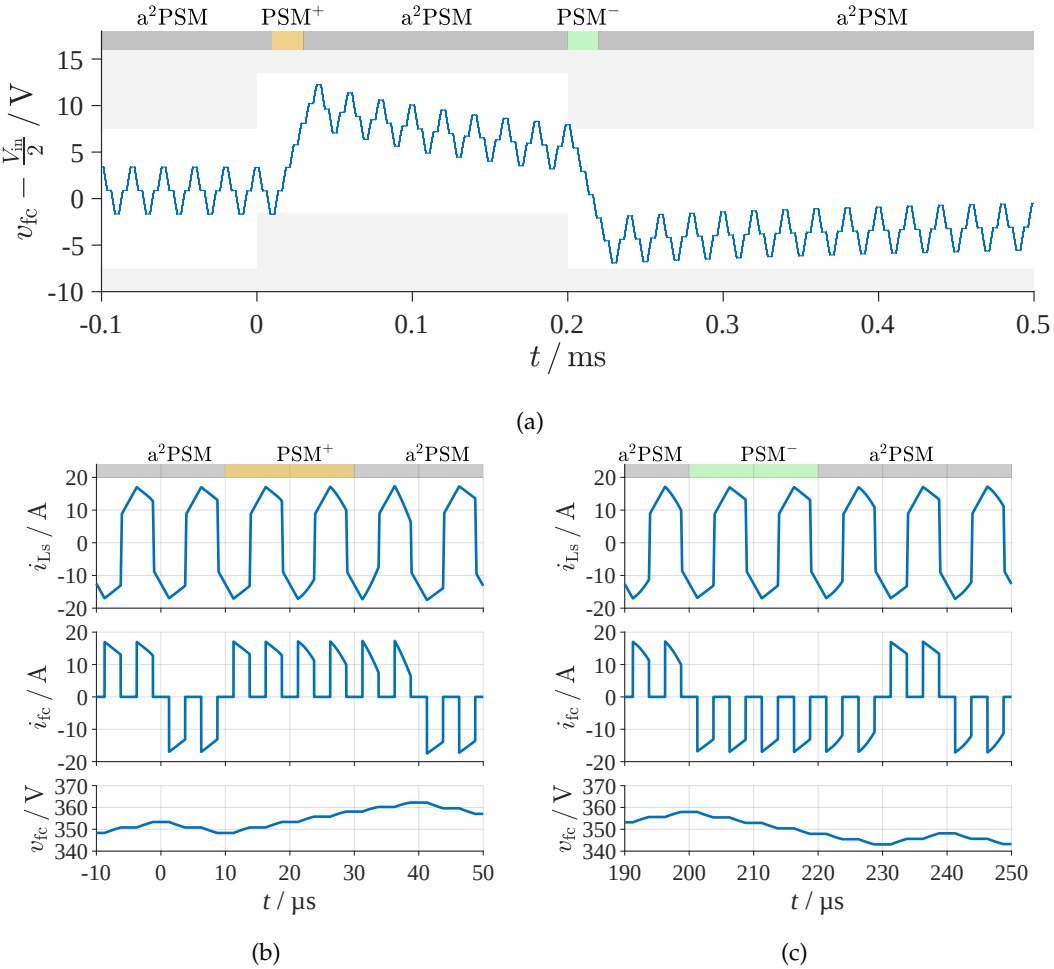


FIGURE 2.149: Exemplary simulation results for controlling the flying capacitor voltage through the state machine visualized in Figure 2.148 with varied reference voltage. (a) continuous simulation with reference step at $t = 0\,\text{ms}$ and $t = 0.2\,\text{ms}$. (b+c) zoom to the mode transitions showing no significant oscillations in the primary current i_{Ls} (parameters: Config$_{2.4a}$).

With the proposed converters and modulations, the aforementioned analysis of the LLC (Section 2.4.2B), the phase-shifted full-bridge and the hard-switched full bridge converter[1] are all directly transferable from the 400 V analysis to 800 V systems.

2.4.3 Flying-capacitor active-clamp converter

Active-clamp forward converters (Figure 2.76) are typically only used for low output powers as zero-voltage switching cannot be easily achieved and power is transferred only once per switching cycle making it a single-pulse topology. This increases the transformer and output inductor size, which is detrimental to the system efficiency

[1] for the hard-switched full-bridge converter, small intervals can be employed with S_1 and S_2 or S_3 and S_4 turned on to control the flying capacitor voltage before all switches are turned off. The interval length is only required to be several nanoseconds long to discharge or charge the flying capacitor voltage depending on the measured voltage. This type of modulation is similar to the control of the LLC, which was introduced in Section 2.4.2B. Due to the trivial nature of this type of modulation, it is not described in further detail.

and power density. Preceding publications, however, proved that the topology can be successfully employed for higher output powers through the use of SiC semiconductors that require much less energy to achieve ZVS and offer low switching losses, enabling high switching frequencies to reduce the size of the magnetic components.

The active-clamp converter, however, still suffers from a couple of flaws: compared to other topologies (LLC, PSFB), the rectifier semiconductors need to be dimensioned for larger RMS currents. Furthermore, the primary semiconductors need to be dimensioned for a larger blocking voltage due to the employment of the clamp capacitor. Finally, ZVS of the main switch S_1 may not always be achievable. While in steady state, the transformer current is negative at the turn-off of S_2, enabling at least partial discharge of the parasitic capacitance of S_1, the energy may not be sufficient to achieve complete ZVS. The three aforementioned flaws will be addressed in more detail.

A Issues of the conventional active-clamp converter

A1 Large freewheeling RMS currents in the low-gain operation Whereas for the aforementioned topologies, the output currents is essentially evenly distributed between the rectifiers, this is not the case for the ACFC – the two rectifier semiconductors (SR_1, SR_2, cf. Figure 2.76) do not conduct the same RMS current. For duty cycles larger 50 %, the rectifier SR_1 conducts the largest current while for duty cycles smaller 50 %, the freewheeling rectifier SR_2 conducts the largest current.

The duty cycle is naturally limited by the operation of the converter because it increases the clamp capacitor voltage V_{cl} and herewith the blocking voltage of the primary semiconductors ($V_{\mathrm{in}} + V_{\mathrm{cl}}$).

The RMS current of SR_1 is, thus, limited by the maximum gain operation. For SR_2, however, the maximum RMS current is characterized by the minimum gain operation. If a very low voltage transfer voltage is required, the required duty cycle becomes very small such that the freewheeling rectifier SR_2 conducts the current for most of the time increasing its RMS current and losses. For wide voltage-transfer ratio applications, the maximum RMS current of SR_2 is typically much larger than the RMS current of SR_1 such that rectifiers of reduced on-state resistance may be required increasing the conversion costs.

A2 Larger primary blocking voltages The primary semiconductors of the active-clamp forward converter need to be dimensioned for the sum of the input voltage V_{in} and clamp capacitor voltage V_{cl}. The clamp capacitor voltage is hereby largely dependent on the duty cycle D. The clamp capacitor voltage is commonly calculated as described in (2.59) and (2.60). These calculation, however, are not accurate for larger output powers as they neglect the duty-cycle-loss intervals (*see* Section 2.2.1) - the real clamp voltage is typically much larger and can be calculated using the formulas derived in Sections 2.2.1A to 2.2.1F. The largest blocking voltage may be either experienced in the operating point with the largest gain (minimum input voltage and maximum output voltage at maximum output power) or at the operating point with the largest gain at the maximum input voltage.

A3 Potential loss of ZVS The active-clamp converter can achieve ZVS for both primary semiconductors. Due to the large transformer current after the turn-off of S_1, ZVS can essentially be guaranteed for wide-bandgap semiconductors for S_2.

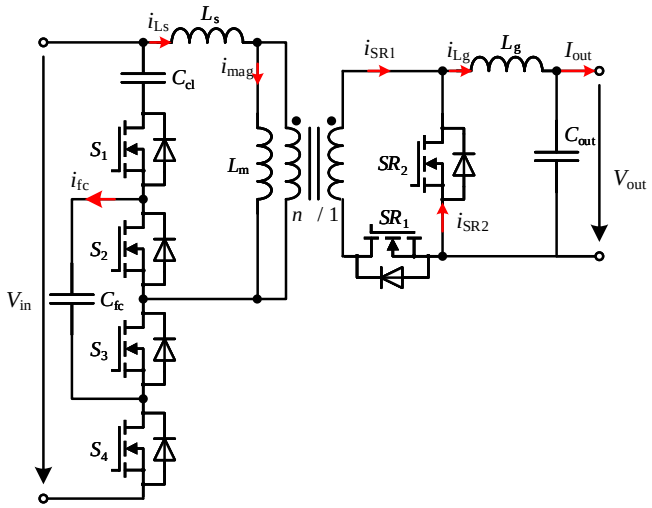
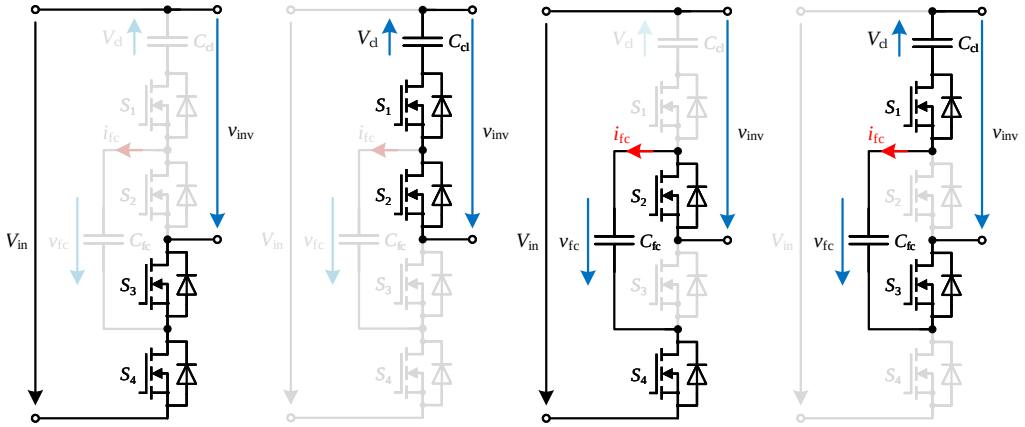


FIGURE 2.150: Proposed 3-level flying-capacitor active-clamp forward converter



(a) ET$^+$: $v_{inv} \approx V_{in}$ (b) DM$^-$: $v_{inv} \approx -V_{cl}$ (c) FW$^-$: $v_{inv} \approx V_{in} - v_{fc}$ (d) FW$^+$: $v_{inv} \approx v_{fc} - V_{cl}$

FIGURE 2.151: Switching states of the flying-capacitor active-clamp inverter module.

However, the turn-off current of S_2 is much smaller and is influenced by the magnetizing current ripple and offset. The (negative) offset is hereby load dependent (*see* Section 2.2.1) and reduces with decreasing load such that less energy is available to achieve ZVS of the main switch S_1.

B The three-level flying-capacitor active-clamp forward converter

The traditional two-switch inverter of the ACFC, S_1 and S_2 in Figure 2.76 can be replaced by a 3L flying-capacitor inverter to reduce the blocking voltage of the semiconductors as shown Figure 2.150. By controlling v_{fc} to $0.5(V_{in} + V_{cl})$, the blocking voltage of each primary switch is reduced by a factor of two. Whereas it is not possible to employ 600/650 V MOSFETs for conventional 400 V applications, the 3-level inverter enables inverter switches of this voltage rating and 900 V semiconductors can be used for 800 V applications. To avoid over voltages, it is assumed that $v_{fc} = \frac{V_{in}+V_{cl}}{2}$. If this condition is not achieved, the high-side switches S_1, S_2 and low-side switches S_3, S_4 are stressed with unequal voltages.

B1 Switching states and inverter voltage All switching states of the inverter are depicted in Figure 2.151. The energy-transfer state ET^+ achieves an inverter voltage of $v_{inv} = V_{in}$. The demagnitzing state DM^- results in an inverter voltage of $V_{inv} = -v_{cl}$ and the two freewheeling states FW^+ and FW^- result in $v_{inv} = \frac{V_{in}+v_{cl}}{2}$ considering the flying capacitor voltage v_{fc} is properly balanced. The intermediate inverter voltage resulting from FW^+ and FW^- may be either positive or negative. For $V_{in} > v_{cl}$ (typical for low voltage transfer ratios and low duty cycles), $FW^{+/-}$ results in $v_{inv} > 0$ such that i_{Ls} remains increasing. For $V_{in} < v_{cl}$ (typical for large voltage-transfer ratios at low input voltages), the intermediate voltage state is negative ($v_{inv} < 0$) such that the primary current i_{Ls} is decreasing.

The freewheeling intervals can be placed behind the energy transfer interval ET^+ or the demagnetizing interval DM^-. This makes additional switching strategies possible to fully exploit the 3L inverter. In these pulse patterns, it is necessary to balance the flying capacitor current to avoid a run-off of the flying capacitor voltage. For that purpose, all of the presented pulse patterns employ a two-period modulation switching from one freewheeling state to the other.

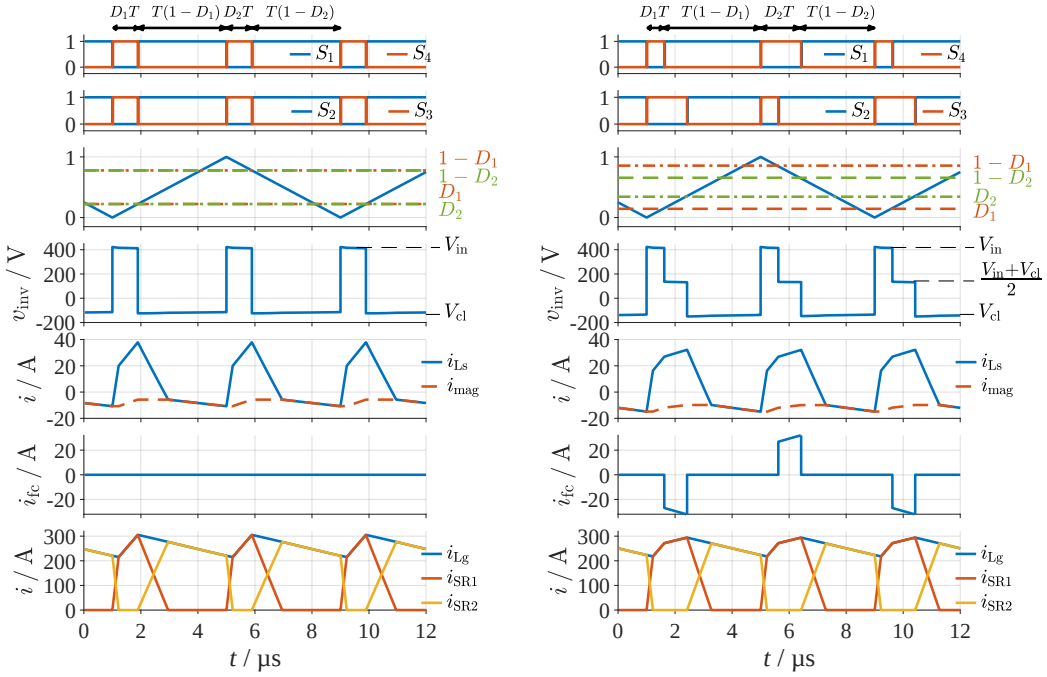
B2 Pulse pattern for reduced freewheeling RMS currents For $V_{in} > v_{cl}$, the freewheeling inverter voltage is positive. If an energy transfer interval ET^+ precedes the freewheeling interval, the primary and secondary currents are increasing essentially increasing the effective duty cycle to reduce the conduction time of the freewheeling semiconductor SR_2. This increases the RMS current of SR_1. However, SR_1 is typically designed for the largest duty cycle, such that an increased RMS current in the low-gain operation will not lead to thermal problems.

The pulse pattern, which is depicted in Figure 2.152b repeats every two periods T and consists of intervals of the lengths D_1T, $(1-D_1)T$, D_2T, and $(1-D_2)T$. The pulse patterns of S_1, S_4 are essentially phase-shifted by T compared to the pulse pattern of S_2, S_3. The pattern can be implemented using a synchronized up-down counter. S_4 is turned on at 0 and 1 while being turned off at D_1 on up-count and $(1-D_2)$ on down-count. S_1 is pulsed complementary with a dead time. S_3 is turned on at zero and 1 and turned-off at D_2 on up-count and $(1-D_1)$ on down-count.

In the pulse pattern, the converter switches from an energy-transfer state ET^+ to the freewheeling state $FW^{+/-}$ to the demagnetizing state DM^- every period while alternating between the freewheeling states FW^+ and FW^- from one period T to the next. The flying capacitor voltage V_{fc} can be controlled by adjusting the duty cycle D_2 by ΔD – for S_4 the interval is adjusted to $(D_2+\Delta D)T$, whereas for S_3 it is adjusted to $(D_2-\Delta D)T$. For $\Delta D > 0$, this increases the charging time where the flying capacitor voltage is increasing and reduces the discharging time where V_{fc} is reducing.

During the turn-on of S_1 and S_3, the freewheeling current flows through the clamp capacitor. For reasons of the large current, the clamp capacitance must be selected larger to reduce the voltage ripple. The average clamp capacitor current is zero over two period ($\frac{1}{2T}\int i_{cl}\mathrm{d}t$). Therefore, the freewheeling current is compensated by a (negative) magnetizing current offset, which must be considered to avoid saturation of the transformer.

B3 Pulse pattern for facilitated ZVS of S_3, S_4 Depending on the design of the converter, ZVS may not always be achievable because the energy stored in the series



(a) Conventional two-level pulse pattern (b) 3L pulse pattern

FIGURE 2.152: Comparison of the (a) conventional voltage pulses and (b) the 3-level pulse pattern to reduce the freewheeling RMS current of SR_2 in the low-gain operation. With the depicted adapted pulse pattern of (b) the freewheeling RMS current I_{SR2} is reduced by about 9.5 % from 199 A to 180 A effectively reducing the resistive synchronous rectifier losses by about 18 % (parameters: Config$_{2.4b}$).

inductance L_{s} is insufficient to achieve ZVS for the main switch S_1 (in the conventional ACFC, Figure 2.76) or to achieve ZVS for both switches S_3 and S_4 for the case of the 3L-ACFC.

For the 3L-ACFC, however, ZVS can be facilitated for operating point of $v_{\mathrm{cl}} > V_{\mathrm{in}}$ through a special pulse pattern. This pulse pattern is depicted in Figure 2.153.

The pulse pattern equally consists of turn-on intervals of D_1T, $T(1-D_1)$, D_2T and $T(1-D_2)$. However, compared to the pulse pattern depicted in Figure 2.152b, S_1 and S_2 are now turned on at zero and 1 resulting in a freewheeling interval FW$^{+/-}$ after the demagnitizing interval DM^{-}. After entering the magnetizing interval, the series inductor current remains constant such that the turn-on of S_3 or S_4 can be automatically achieved. During the magnetizing interval, the series inductor current remains decreasing such that ZVS may also be achieved when leaving the freewheeling interval to enter the energy-transfer interval ET^{+}.

B4 Magnetizing current reduction for facilitated ZVS in the low-load low-gain operation The facilitated ZVS operation presented in Section 2.4.3B3 can only be employed if $v_{\mathrm{cl}} > V_{\mathrm{in}}$. This is not the case if the converter is operated at a low gain and large input voltages (cf. Figure 2.154). Therefore, ZVS may not be achieved. However, when employing the modulation presented in Section 2.4.3B2, the magnetizing current is reduced through an offset, which is caused by the freewheeling interval FW^{+}. This can be used to reduce the magnetizing current in the low-gain

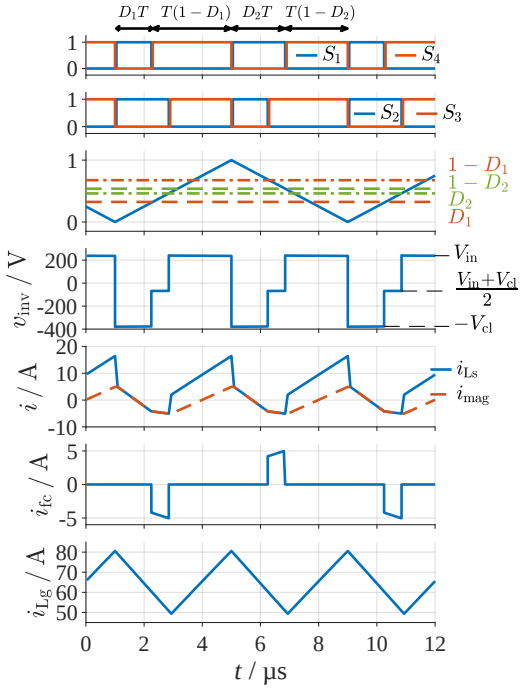


FIGURE 2.153: 3-level pulse pattern to facilitate ZVS of S_3 and S_4 (parameters: $\mathrm{Config}_{2.4c}$).

and low-load operation to facilitate ZVS of the switches S_3 and S_4.

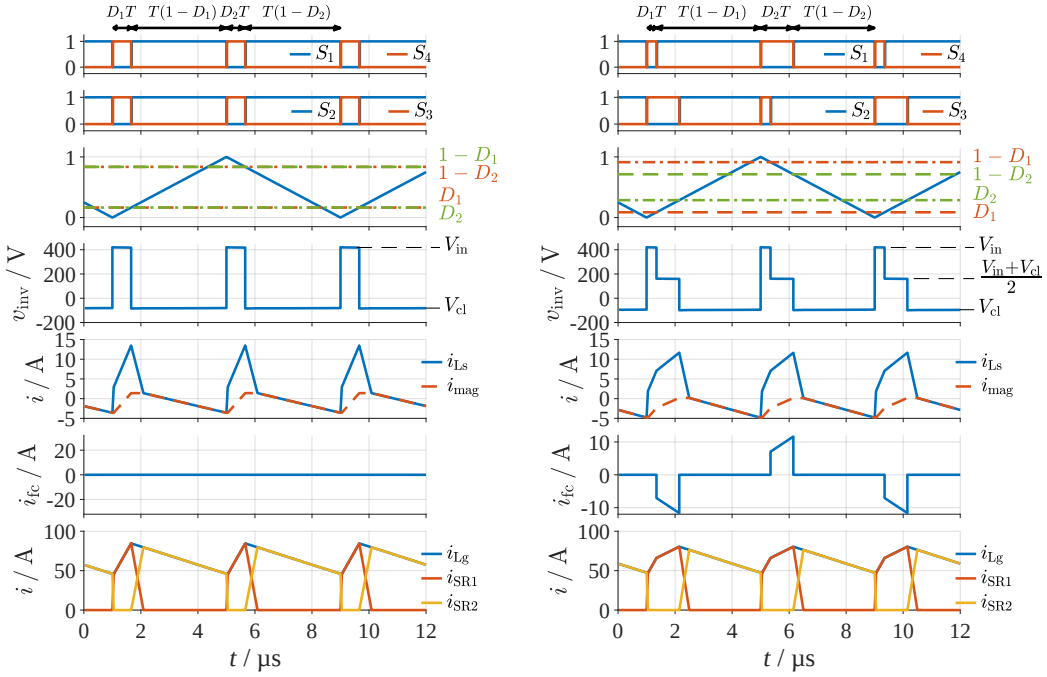
C Efficacy of 800 V flying-capacitor active-clamp converters

When using the active-clamp converter in 800 V systems, the converter requires primary semiconductors of a voltage rating of 1800 V, which are costly and have large losses. By using a 3-level flying capacitor active-clamp forward converter the voltage rating can be reduced from 1800 V to 900 V. Additionally, the 3-level structure can be utilized for beneficial modulations to reduce the maximum secondary-side RMS currents and facilitate ZVS of the primary switches.

With the proposed converter, the aforementioned analysis of the active-clamp converter can be transferred to the 3-level active-clamp converter under the assumption that the conversion ratio is increased from the 2-level structure from $n^{\mathrm{2L}}_{\mathrm{ACFC}}$ to the 3-level value of $n^{\mathrm{3L}}_{\mathrm{ACFC}} = 2n^{\mathrm{2L}}_{\mathrm{ACFC}}$ as the applied voltage levels are doubled. A disadvantage of using the active-clamp converter in a flying-capacitor setting is that the switch count does double, which is a clear drawback compared to the full-bridge type inverters investigated in Section 2.4.2 as the original benefit of only two primary switches is lost.

2.4.4 Conclusion

The analysis of Sections 2.1 to 2.3 can be transferred to 800 V systems by using a flying-capacitor inverter instead of the original full-bridge inverter for the LLC and HSFB/PSFB or replacing the half-bridge in the ACFC. All operating modes can be transferred to this inverter structure when controlling the flying-capacitor voltage. The LLC converter and PSFB/HSFB are directly transferable with an equal switch



(a) (b)

FIGURE 2.154: Comparison of the (a) conventional voltage pulses and (b) adapted voltage pulses for the 3L ACFC converter operated at low load and low gain. With the adapted pulse pattern of (b), the minimum magnetizing current is reduced from $\check{i}_{\mathrm{mag}} = -3.58\,\mathrm{A}$ to $\check{i}_{\mathrm{mag}} = -4.84\,\mathrm{A}$ facilitating ZVS of the switches S_3 and S_4. With the adapted modulation, the energy stored in L_{s} is increased by 83 % (parameters: $\mathrm{Config}_{2.4c}$).

count, blocking voltage and magnetics voltage levels with the only further modification being the increased voltage level of the resonant or blocking capacitor. For the ACFC, the modification comes with the drawbacks of an increased magnetics input voltage, a doubled switch count with advantageous being only facilitated ZVS. It must be stated that the efficacy of the ACFC with a FC is, therefore, very limited.

Chapter 3

Topology Comparison

The selection of a suitable topology for a given application is one of the most important and impactful decisions in power electronics. The designer is faced with a variety of different topologies with a diversity of optimization options. Furthermore, the design is a tradeoff of finding a circuit that is optimum in terms of *efficiency*, *power density* and *costs*, which design goals often contradict each other. The efficiency may be optimized by employing high-quality materials and components, which also results in an increased power density. However, the high-quality materials may in terms lead to increased costs [Bül10]. The switching frequency is hereby one of the most important design parameters. By increasing the switching frequency, the power density can be increased by reducing the size of the passive components; however, this also results in increased switching and winding losses.

This chapter compares the aforementioned topologies by investigating their stress values. Section 3.1 reviews existing topology design and comparison methodologies. Section 3.2 introduces a switching-frequency independent design and comparison methodology, which is employed to compare the topologies in Section 3.3 and the select the LLC resonant converter, the active-clamp forward converter and the hard-switched full-bridge for experimental evaluation. Finally, the three selected topologies are experimentally benchmarked in Section 3.4 and a conclusion is given in Section 3.5.

3.1 State of the Art in Topology Comparison Methodologies

In the past a variety of different evaluation methods have been presented. Many methodologies compare separate designs for the compared converters to derive a loss or efficiency comparison [LK17; POD14; Hu+16a]. Others rely on a discussion to derive a suitable topology [Aga+11; Pat+20], which compare the topology based on a qualitative assessment. These methods, however, rely on specific designs that are compared or do not quantitatively compare the topologies.

To quantitatively compare converter topologies, *Carsten* considered in [Car88] characteristic voltage-current products as component load factor (CLF) for each system component where

$$\mathrm{CLF} = V^* I^*. \tag{3.1}$$

Carsten separates between CLFs for semiconductors, inductors, transformers and capacitors. V^* is the characteristic voltage for each component (peak voltage, peak-to-peak voltage or average voltage), whereas I^* is the characteristic current (average current, RMS current, peak-to-peak current). The separate CLFs can be summed up over the number of components in the system to compare different converter topologies. In this comparison, procedure, it is assumed that ripple currents and losses are negligible, which makes the comparison switching-frequency-independent. The comparison is limited to PWM converters where the transistors and rectifiers are single-quadrant devices (positive voltage and current polarity). The method was adapted by *Petersen* in [PA02] for PFC converters and applied to compare two-stage isolated converters. *Petersen* also compared conduction and switching losses by calculating characteristic loss ratios while assuming equal die size and neglecting the influence of semiconductors with different voltage classes. The calculation of a characteristic switching loss ratio, furthermore, is only valid for equal switching frequencies of the compared converters. A similar analysis was performed in [KBK14] where a buck-boost converter was compared to a buck+boost converter. Switching and conduction losses were calculated with respect to a reference by considering characteristic dependencies to the employed area of silicon. By calculating a characteristic loss ratio, the performance of the two topologies was evaluated. A disadvantage of this method is that the voltage classes of the semiconductors employed in the four-switch buck-boost converter is not considered in the comparison. As the primary and secondary half bridge are stressed with the input and output voltage respectively, they can be designed for different voltage levels, which affects the necessary amount of silicon as well as the conduction and switching losses. The volume of inductors and capacitors was assessed based on the energy stored in the components while assuming characteristic current and voltage ripples.

Cohen [Coh93] introduced redefined load factors to account for conduction losses in semiconductors, accounting for inductors through their voltage-time product and capacitors through their stored energy. In contrast to the methods of [Car88] and [PA02], the load factors is suited for a comparison of semiconductors of different voltage classes as the transistor load factors employed a characteristic exponent to account for the increase of the on-state resistance. In the described topology comparison, specific switching frequencies and maximum ripple currents were assumed while the effect of circuit elements like the magnetizing/leakage inductance were neglected. Squared currents were assumed in the calculation of the stress factors.

Wittenbreder refined the CLF analysis in [Wit06a; Wit06c; Wit06b] by assuming equal resources for the compared topologies – an equal amount of silicon, magnetic area and capacitor volume. *Wittenbreder* introduced characteristic component stress factors for the semiconductors, inductors and capacitors while each stress factors can be assigned a weight to adjust for the resources assigned to that component. The methodology has been widely applied in research [MKA14; MZM18; Pit+14; ZMA17]. The component stress factor analysis assumes negligible current ripples (block currents) and no losses. The stress factors are calculated for their individual worst-case operating point.

The component stress method by *Wittenbreder* was adopted by [Bül10]. To account for the losses and converter volume he introduced separate indicators for losses and volume/costs. *Bülo* calculates five characteristic loss indicators for bi- and

unipolar semiconductors, switching losses, inductors, and transformers. To evaluate the volume of systems components, he introduced three volume indicators for semiconductors, inductors, and capacitors. A characteristic attribute of his indicators are exponents that introduce a characteristic scaling based on every influence factor. This ensures that the necessary amount of silicon for topologies employing semiconductors of different voltage classes is accurately accounted for. His method was used to evaluate the performance of a novel DC/3AC-converter in [AKB17] by investigating the volume of each system component in relation to a reference topology.

The aforementioned methods compare topologies by calculating performance indicators only. These evaluated the performance of a system through scalar values. However, these methods lack precision as the real converter performance with respect to losses, power density, and costs is not evaluated. These factors are only evaluated through indicators. An accurate representation of the performance when employing different semiconductor, inductor, or capacitor technologies is not possible. To evaluate topologies as accurately as possible while considering all possible technologies, high-precision pareto-optimization can be performed evaluating losses, power density [BKG12; NHK22; Lan+22; KBK14], and including costs [BK17]. A topology comparison based on a pareto optimization is arguably the most precise method as it calculates hundreds of different converter designs to select the design most suitable to the requirements. In [BK17] a 3L dual-active bridge (DAB) was compared to a five-level DAB. The topology parameters (inductance, capacitance, winding ratio) were kept fixed and were only scaled with the switching frequency. The inductors were designed to achieve ZVS at the lowest switching frequency to be evaluated while for larger switching frequencies, incomplete ZVS was accepted to avoid large reactive currents. Furthermore, separate components were used for the magnetizing inductance and the series inductor while the transformer was constructed to achieve a low stray and large magnetizing inductance. An integration of the series inductor and magnetizing inductor into the transformer was not pursued.

3.2 A Design-Based Operating-Frequency Independent Topology Comparison

this section has been previously published in parts in [Reh+19b].

One of the most important factors of the design is the choice of the switching or resonant frequency. The choice of the frequency influences the switching losses, the ZVS capability, the size of the magnetic components and capacitors, as well as the losses of the magnetic components [BKG12; SSM19c]. Many of the aforementioned rely on a choice of a single switching or resonant frequency and are, thus, limited to this specific design. It is not possible to analyze the stress values based on an overview of a map of available designs. Furthermore, the design process is usually an iterative endeavor requiring an adaption of several circuit components [Sch22]. A recalculation of the stress values is, thus, required for every iteration.

This section describes a comparison and design methodology where the circuit parameters are normalized to derive frequency-independent circuit values, which

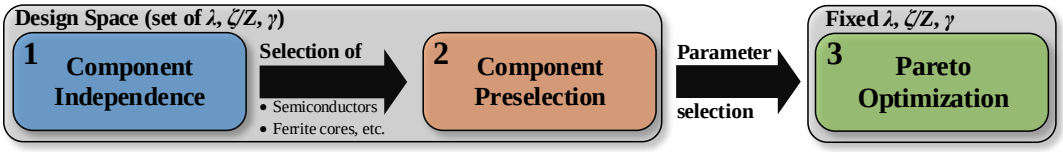


FIGURE 3.1: Exemplary three-step optimization process.

allow a comparison based on many different designs where the numeric stress values are independent from a chosen switching or resonant frequency. By calculating the stress values for a number of different converter designs, the effect of any iterative redesign of the circuit value can be easily comprehended[1].

The switching or resonant frequency can then be selected in a later step allowing a pareto optimization of the circuit. A possible design flow is depicted in Figure 3.1. In the first step, component-independent stress values are compared to select suitable semiconductors and ferrite cores for a second step comparison based on preselected components. For these two steps, a design set based on normalized circuit parameters are used. Finally, for a third step, a pareto optimization can be performed to derive the best design considering costs, power density, and losses. This thesis will focus on the first step, the component-independent comparison based on normalized stress values.

The stress values are compared using time-domain models as these models are the most accurate [SM20]. The time-domain solutions are calculated based on the models that are described in Sections 2.2 and 2.3 for the ACFC and HSFB, the time-domain model of [Cao14] for the PSFB, and the developed time-domain solution of [Keu23; Her+16; Fig16] for the LLC.

[1] that means that the effect of a modified series inductance of the ACFC on the blocking voltage of the primary and secondary semiconductors can be immediately analyzed without recalculating the circuit just by analyzing the calculated design maps.

3.2.1 Normalization of the system components

To compare converters without pre-choosing a switching frequency, it is necessary to derive frequency independent system parameters. Consider the inductor voltage $u_{\mathrm{L}}(ft)$. This voltage is frequency dependent and stretches and compresses with the frequency f[1]. The inductor current can be calculated as

$$i_{\mathrm{L}}(t) = \frac{1}{L}\int u_{\mathrm{L}}(ft)\mathrm{d}t. \tag{3.2}$$

The inductance can be defined as a constant factor divided by the frequency.

$$L = \frac{\zeta}{f} \tag{3.3}$$

If the frequency is scaled with the variable α, t can be substituted to $\tau = \alpha t$ to

$$\begin{aligned} i_{\mathrm{L,ff}}(t) &= \frac{\alpha f}{\zeta}\int u_{\mathrm{L}}(\alpha f t)\mathrm{d}t \\ &= \frac{\alpha f}{\zeta}\int \frac{u_{\mathrm{L}}}{\alpha}(\alpha\tau)\mathrm{d}\tau \\ &= \frac{f}{\zeta}\int u_{\mathrm{L}}(\alpha\tau)\mathrm{d}\tau = i_{\mathrm{L}}(t). \end{aligned} \tag{3.4}$$

This analysis shows that by expressing L through ζ and f, the integral becomes frequency independent. The effect of the inductance L on the current shape can, therefore, be analyzed through ζ frequency-independently.

Many PWM converters consist of several inductors. The inductance of these inductors can be normalized with respect to the reference inductance. Referring to the PSFB and the ACFC, the parameters can be normalized with respect to the switching frequency as

$$\begin{aligned} \zeta &= L_{\mathrm{m}} f_{\mathrm{sw}} \\ \lambda &= \frac{L_{\mathrm{s}}}{L_{\mathrm{m}}} \\ \gamma &= \frac{L_{\mathrm{g}}}{L_{\mathrm{m}}}. \end{aligned} \tag{3.5}$$

It is also possible to reference every inductance to the switching frequency as

$$\begin{aligned} \zeta &= L_{\mathrm{m}} f_{\mathrm{sw}} \\ \Lambda &= L_{\mathrm{s}} f_{\mathrm{sw}} \\ \Gamma &= L_{\mathrm{g}} f_{\mathrm{sw}}. \end{aligned} \tag{3.6}$$

For resonant converters such as the LLC, the system parameters can be normalized by one or several resonant frequencies. It is, therefore, beneficial to normalize

[1] the following analysis has been performed in a similar manner in the supervised master thesis in [Kor20b]

with respect to one particular characteristic frequency. Referring to [Keu23; Keu+17], the parameters of the LLC can be normalized as

$$\begin{aligned} f_{\text{res}} &= \frac{1}{2\pi}\sqrt{\frac{1}{L_\text{r}C_\text{r}}} \\ \lambda &= \frac{L_\text{r}}{L_\text{m}} \\ Z &= \sqrt{\frac{L_\text{r}}{C_\text{r}}}. \end{aligned} \tag{3.7}$$

The resonant tank can, thus, be analyzed with respect to λ and Z only. The number of characteristic parameters, thus, reduces from L_r, L_m, and C_r to λ and Z. The resonant frequency can hereby be chosen in a second step whereby the first-stage analysis of λ and Z is sufficient to choose a design with low resonant and turn-off currents as well as suitable resonant capacitor voltages. For converters that consist of additional resonant capacitors (such as the LLCC converter), the additional resonant frequency can be normalized to the other resonant frequency.

3.2.2 Definition of stress parameters

The normalization of (3.2.1) results in current and voltage shapes that are valid for any chosen switching / resonant frequency. RMS currents, turn-off, turn-on and peak currents can, thus, be analyzed and compared directly while peak voltages (i.e. resonant voltage, or clamp capacitor voltage) can be inspected to avoid exceeding the maximum value.

A Charges

However, parameters such as charges are dependent on the switching frequency and cannot be directly compared. Charges are inversely-proportional to the switching frequency. A frequency-independent stress parameter Q_n can be defined by multiplying the charge with a dummy frequency f_calc, which may be the switching frequency for PWM converters of the operating frequency $f_\text{sw,calc}$ ($f_\text{calc} = f_\text{sw,calc}$) or the resonant frequency $f_\text{r,dummy}$ for resonant converters such as the LLC ($f_\text{calc} = f_\text{r,calc}$).

$$Q_\text{n} = Q f_\text{calc} \tag{3.8}$$

The normalized charge can be used to evaluate the necessary capacitance. The output capacitance can, exemplary, be calculated with the designated switching / resonant frequency f, the maximum acceptable output voltage ripple Δv_out and the normalized output capacitor charge $Q_\text{n,out}$ as

$$C_\text{out} = \frac{Q_\text{n,out}}{f \Delta v_\text{out}} \tag{3.9}$$

B Magnetic components

The design of the magnetic components is mainly influenced by the design choice of the magnetic core because the flux density defines the turn number N and effective

TABLE 3.1: Overview of the selection of compared stress parameters.

Symbol	Parameter
I_{sw}	switch RMS current
i_{to}	turn-off current of the primary semiconductors
V_{sw}	primary semiconductor blocking voltage
I_{prim}	primary transformer RMS current
$\mathcal{B}_{mag}$	stress value for the transformer flux
I_{SR}	RMS current of the synchronous rectifier semiconductors
V_{SR}	blocking voltage of the synchronous rectifier semiconductors
$\mathcal{B}_{Lg}$	stress value for the output inductor flux
$Q_{n,out}$	normalized output charge of the output capacitor

core cross section A_{eff}. The peak flux density $\hat{B}_{Ls}$ of an inductor with an inductance L_s and the current $i_{Ls}(t)$ can be calculated as

$$B_{Ls}(t) = \frac{L_s i_{Ls}(t)}{N A_{eff}}, \tag{3.10}$$

which can be normalized according to (3.5) for PWM converters as

$$B_{Ls}(t) = \frac{\zeta \lambda i_{Ls}(t)}{f_{sw} N A_{eff}}. \tag{3.11}$$

While the numerator of (3.11) is a function of the design configuration (λ, ζ and $i_{Ls}(\lambda, \zeta)$), the denominator is a function of the realization variables, the selected switching frequency f_{sw}, the winding number N, and the selection of the core cross section A_{eff}. The numerator is, thus, a stress value for the size of the magnetic component:

$$\mathcal{B}_{Ls}(t) = \lambda \zeta i_{Ls}(t) = \Lambda i_{Ls}. \tag{3.12}$$

This allows the calculation of characteristic stress values. For the current value $i_{Ls}(t)$, a peak value or a current ripple can be inserted depending on the specific application. For low switching frequencies and applications with a large DC current value, the design can be determined to achieve the maximum flux density, whereas for large switching frequencies the design is determined by the current ripple as a design for the maximum flux density would result in exceedingly large core losses.

Similarly, for transformers, the flux density is defined with the primary turn number N_{prim} and the stray inductance L_σ as[1]

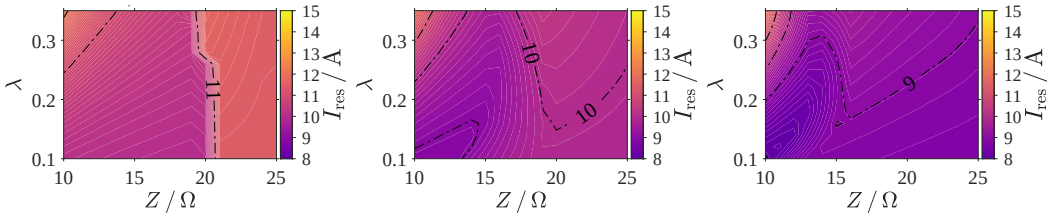
$$B_{Lm}(t) = \frac{(L_m + L_\sigma) i_{mag}(t)}{N_{prim} A_{eff}} = \frac{(1 + \lambda_\sigma) \zeta i_{mag}(t)}{f_{sw} N_{prim} A_{eff}} = \frac{\mathcal{B}_{Lm}}{f_{sw} N_{prim} A_{eff}}. \tag{3.13}$$

$\mathcal{B}_{Lm}$ is a direct indicator of the core size or core losses. By comparing $\mathcal{B}_{Lm}$, it is possible to easily compare the core size of suitable topologies independently from

[1] assuming the concentrated primary stray inductance model where the stray inductance L_σ and magnetizing inductance L_m are concentrated on the primary side – *see* Section 2.1.6.

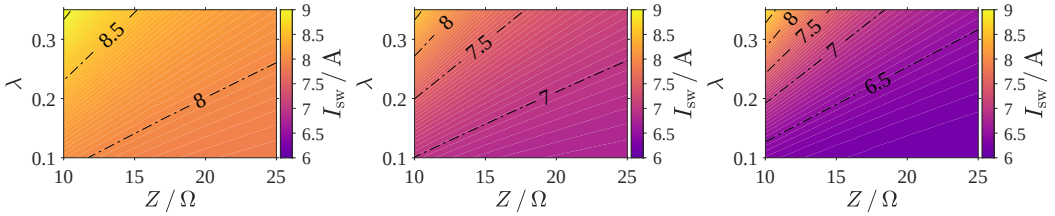
the switching frequencies.

An overview of the compared stress values is given in Table 3.1. The table lists the entirety of compared stress parameters. Hereby, some values are given directly by the topology and not influenced by the design. An example for this, is V_{sw} for the LLC, HSFB, and PSFB, as for this topologies, a full-bridge inverter is employed such that the primary semiconductor blocking voltage is equal to the input voltage. Equally, for the LLC, the blocking voltage V_{SR} is equal to the twice the output voltage if a synchronous rectifier is employed.



(a) $n = 13$ (b) $n = 15$ (c) $n = 17$

FIGURE 3.2: Visualization of the RMS resonant current I_{res} at the operating point $\text{OP}^{\text{FB}}_{\text{change}}$ at the border from full-bridge mode to half-bridge mode over the normalized circuit values Z and λ for various conversion ratios n.



(a) $n = 13$ (b) $n = 15$ (c) $n = 17$

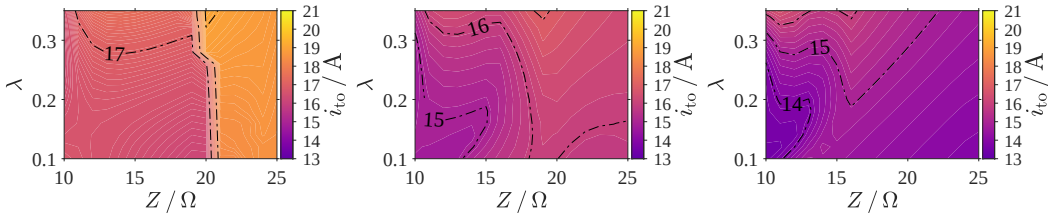
FIGURE 3.3: Visualization of the switch RMS current I_{sw} at the operating point $\text{OP}^{\text{FB}}_{\text{FL}}$ over the normalized circuit values Z and λ for various conversion ratios n.

3.3 Topology Comparison and Preselection

To compare the different converter topologies, this section analyzes the switching-frequency-independent stressing values of each circuit. The LLC component stress is studied in Section 3.3.1. Section 3.3.2 analyzes the stressing values of the ACFC, Section 3.3.3 analyzes the PSFB, the HSFB is investigated in Section 3.3.4. For each topology, the characteristic operating points are taken from the analysis in Chapter 2.

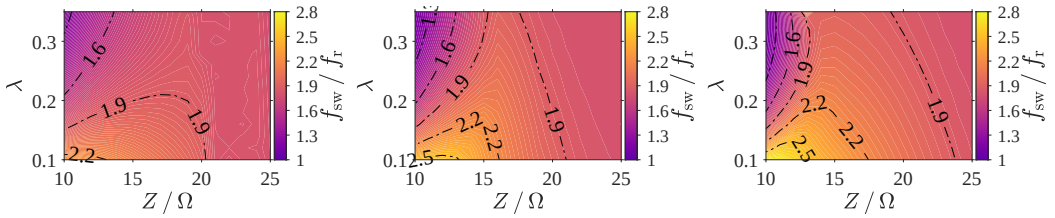
3.3.1 LLC resonant converter

To accurately design the LLC (cf. Figure 2.2a), the stress values are analyzed in dependency of the normalized circuit components Z and λ by using a color map. The influence of the conversion ratio n is considered by using separate color maps for each conversion ratio. The resonant current is depicted in Figure 3.2 for $n \in \{13, 15, 17\}$ for the full-bridge mode at the border to half-bridge mode $\text{OP}^{\text{FB}}_{\text{change}}$. For this operating point, the highest switching frequency can be expected such that this operating point can be characteristic to design the resonant inductor and transformer. Furthermore, for switches with high switching losses, this operating point may experience the largest losses. For low conversion ratios ($n = 13$), a clear step can be identified at roughly $Z = 20\,\Omega$. This is caused by the operating mode change that is moved further and further to low input voltages. For $n = 15$ and $n = 17$, variations in Z and λ purely alter the output voltage and the operating mode is only changed at the maximum input voltage ($V_{\text{n}} = 420\,\text{V}$). The analysis shows that the maximum RMS current can be reduced by increasing the conversion ratio. The lowest RMS current is achieved at $n = 17$.



(a) $n = 13$ (b) $n = 15$ (c) $n = 17$

FIGURE 3.4: Visualization of the turn-off current i_{to} at the operating point OP^{FB}_{change} at the border from full-bridge mode to half-bridge mode over the normalized circuit values Z and λ for various conversion ratios n.



(a) $n = 13$ (b) $n = 15$ (c) $n = 17$

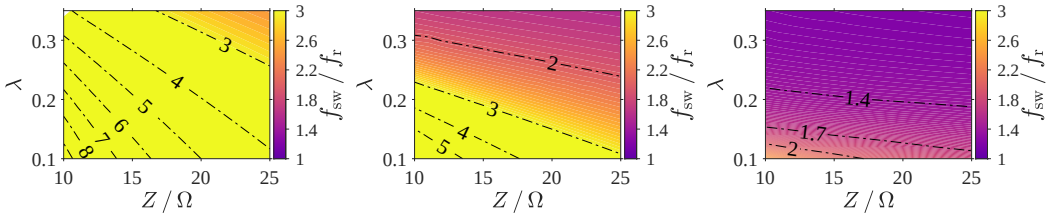
FIGURE 3.5: Visualization of the normalized switching frequency f_{sw}/f_r at the operating point OP^{FB}_{change} at the border from full-bridge mode to half-bridge mode over the normalized circuit values Z and λ for various conversion ratios n.

Figure 3.3 shows the switch RMS current for the operating point with the lowest input voltage at full load in full-bridge mode (OP^{FB}_{FL}). This operating point is characteristic as it experiences the largest RMS currents at relatively low input voltages and switching frequencies. It is characteristic for switches that experience dominant conduction losses. Again, the analysis shows that the RMS current can be significantly reduced by increasing the conversion ratio. While this modification significantly influences the primary switch RMS current, the secondary synchronous rectifier RMS current is barely influenced[1] – I_{SR} does not change significantly. For any value of Z or λ, it is roughly $I_{SR} = 103\,\text{A}$.

The turn-off current of OP^{FB}_{change} is depicted in Figure 3.4. Again, this value is characteristic for switches with dominant switching losses as it influences the switching losses. The corresponding normalized switching frequency is depicted in Figure 3.5. The analysis shows that the turn-off current can be reduced slightly by increasing the conversion ratio from $n = 15$ to $n = 17$ and it also slightly influences the switching frequency. For $n = 17$, the switching frequency is slightly lower.

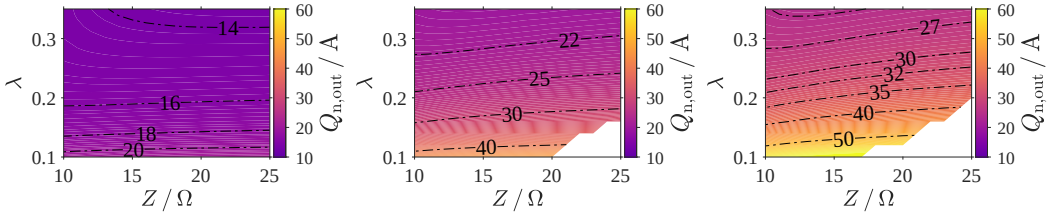
To avoid excessively large switching frequencies in half-bridge mode for the lowest output current, it is necessary to further analyze OP^{HB}_{LL}. For this operating point, the switching frequency should be limit to the necessity of switching to asymmetrical operation or burst operation. The switching frequency is visualized in Figure 3.6. It shows excessively large values for $n = 13$ in Figure 3.6a such that this configuration cannot be used. For $n = 15$, the switching frequency is much lower. However, for most values of Z and λ, it is still excessively large – only for large values of λ and Z, the switching frequency is acceptable. For $n = 17$, the switching frequency is

[1] this is a common result for LLC designs and has also been reported in [USB20b].



(a) $n = 13$ (b) $n = 15$ (c) $n = 17$

FIGURE 3.6: Visualization of the normalized switching frequency f_{sw}/f_r at the minimum-gain operating point $OP^{FB}_{HB,LL}$ over the normalized circuit values Z and λ for various conversion ratios n.



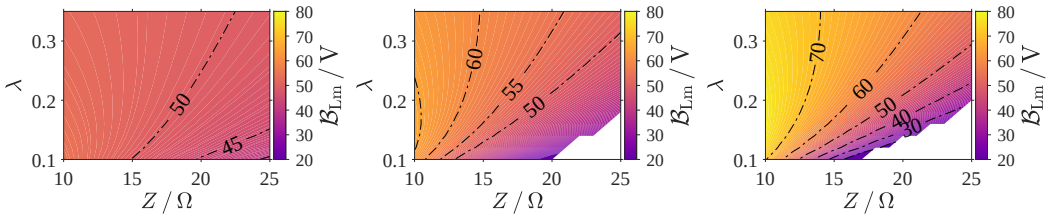
(a) $n = 13$ (b) $n = 15$ (c) $n = 17$

FIGURE 3.7: Visualization of the normalized output charge $Q_{n,out}$ at the operating point OP^{FB}_{DL} at the maximum gain visualized over the normalized circuit values Z and λ for various conversion ratios n.

over the entire design region acceptable.

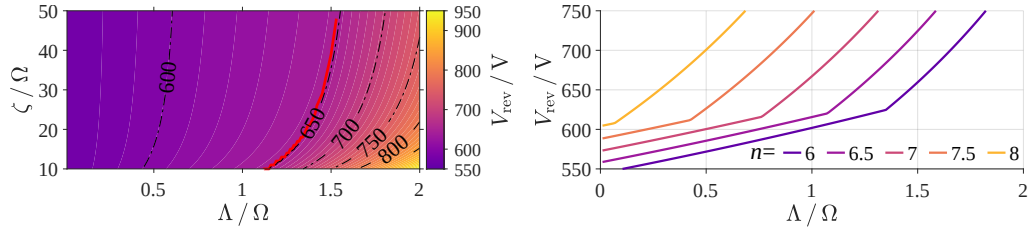
While a larger conversion ratio positively influenced all stress values, Figure 3.7 and Figure 3.8 show that it negatively influences the normalized output charge and the flux density in the transformer. The output charge is about 30 % larger for $n = 17$ compared to $n = 15$ as visualized in Figure 3.7c and Figure 3.7b, respectively. Furthermore, also the magnetizing flux is also larger (cf. Figure 3.8).

Considering the above analysis, the resonant tank values were defined as follows: $Z = 19.4\,\Omega$, $\lambda = 0.333\,\Omega$ and $\zeta = 11.25\,\Omega$ and the conversion ratio is chosen to be $n = 15$. This results in relatively low turn-off and RMS currents while achieving acceptable output charges and flux densities for the transformer. Especially due to the high costs of ceramic capacitors, an acceptable output charge of the converter must be considered.



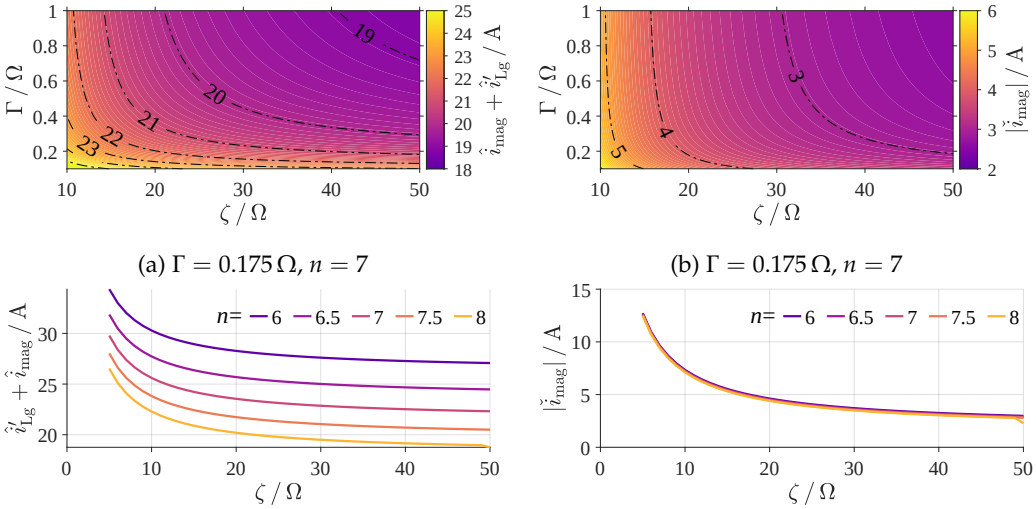
(a) $n = 13$ (b) $n = 15$ (c) $n = 17$

FIGURE 3.8: Visualization of the normalized magnetizing flux $\mathcal{B}_{Lm}$ in the operating point OP^{FB}_{DL} at the maximum gain visualized over the normalized circuit values Z and λ for various conversion ratios n.



(a) $\Gamma = 0.175\,\Omega$, $n = 7$ (b) $\Gamma = 0.175\,\Omega$, $\zeta = 15\,\Omega$

FIGURE 3.9: Maximum primary semiconductor voltage stress of the ACFC. (a) primary semiconductor voltage V_{rev} over Λ and ζ and (b) Λ and n. For very low values of Λ, the voltage can be calculated based on the common equation (2.59).



(a) $\Gamma = 0.175\,\Omega$, $n = 7$ (b) $\Gamma = 0.175\,\Omega$, $n = 7$

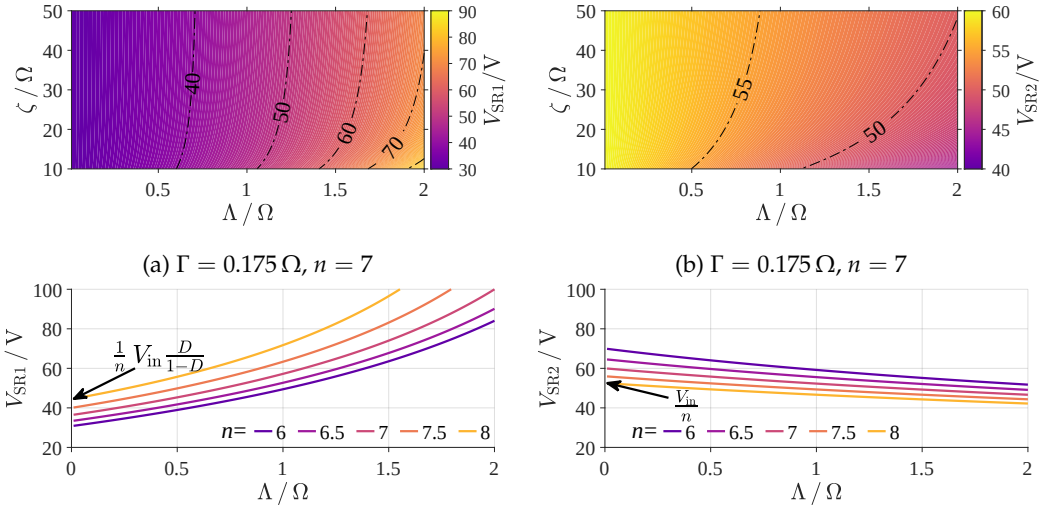
(c) $\Gamma = 0.175\,\Omega$, $\Lambda = 0.75\,\Omega$ (d) $\Gamma = 0.175\,\Omega$, $\Lambda = 0.75\,\Omega$

FIGURE 3.10: Primary semiconductor turn-off current of the ACFC for (a,c) the main switch S_1 ($\hat{i}_{\text{mag}} + \hat{i}'_{\text{Lg}}$) and (b,d) the auxiliary switch ($|\check{i}_{\text{mag}}|$). (a,b) The stress values are depicted over ζ and Γ and (c,d) ζ and Γ.

3.3.2 Active-clamp converter

For the design of the active-clamp converter (cf. Figure 2.76), one of the most critical design aspects is the limitation of the maximum reverse blocking voltage of the primary and secondary semiconductors. For that purpose, the circuit needs to be designed to avoid critically large reverse and clamp voltage ($V_{\text{rev}} = V_{\text{in}} + V_{\text{cl}}$ and V_{cl}). The reverse voltage is visualized over the normalized variables ζ and Λ in Figure 3.9a and for different conversion factors n over Λ in Figure 3.9b[1]. Figure 3.9a depicts two critical operating points simultaneously. In the upper left of the red line, the operating point with the maximum reverse blocking voltage is $\text{OP}_{\text{Gmax,FL}}|\hat{V}_{\text{in}}$, whereas for the lower right of the red line, the most critical operating point is $\text{OP}_{\text{Gmax,DL}}$. The analysis yields three important findings:

[1] for the ACFC four circuit parameters govern the current shape: L_{s}, L_{m}, L_{g} and n (in normalized notation: Λ, ζ, Γ and n) whereas for the LLC, the four normalized values L_{r}, C_{r}, L_{m} and n reduce to the three normalized variables Z, λ and n. Therefore, the visualization of the stress values of the ACFC is different from the LLC. To visualize the effect of the circuit parameters, first, a color map shows the influence of the dominant two circuit parameters on the stress values, and the effect of the conversion ratio is then analyzed over one circuit parameter in a line chart.



(a) $\Gamma = 0.175\,\Omega$, $n = 7$

(b) $\Gamma = 0.175\,\Omega$, $n = 7$

(c) $\Gamma = 0.175\,\Omega$, $\zeta = 15\,\Omega$

(d) $\Gamma = 0.175\,\Omega$, $\zeta = 15\,\Omega$

FIGURE 3.11: Maximum steady state synchronous rectifier voltage of the ACFC. (a) Synchronous rectifier voltage $\hat{v}_{SR1}$ over Λ and ζ and (c) Λ and n. (b) Synchronous rectifier voltage $\hat{v}_{SR2}$ over Λ and ζ and (d) Λ and n. For very low values of Λ, the rectifier voltage can be calculated based on the common equation (2.59).

- the most critical design parameter influencing the reverse blocking voltage is Λ (3.6) (influencing the stray inductance L_s),
- another influence factor is the conversion ratio n,
- the influence of ζ is minor. However, especially for low ζ-values (which may be required to achieve ZVS), the influence must not be disregarded.

When employing MOSFETs of a blocking voltage of 900 V, the reverse voltage should be limited to about 650 - 700 V. It is, thus, important to avoid Λ-values larger than $\Lambda = 1.5$.

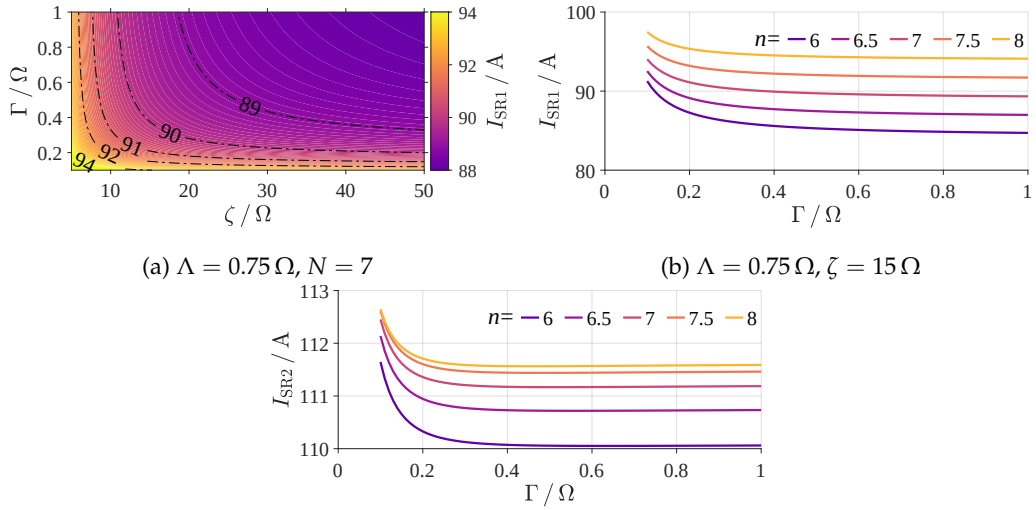
The turn-off of the main and auxiliary MOSFETs are depicted in Figure 3.10. The figures show that the turns ratio has a strong influence on the main switch but not less on the auxiliary switch. The same is true for the influence of the output inductor through Γ. Another big influence factor is the influence of the magnetizing inductance through ζ.

As the reverse voltage largely affects the clamp capacitor voltage V_{cl}, the choice of Λ also has a significant influence on the blocking voltage V_{SR1} of the synchronous rectifier SR_1. The stressing values are again depicted over Λ and ζ in Figure 3.11a and for different n over Λ in Figure 3.11c. In contrast, the blocking voltage V_{SR4} of the synchronous rectifier SR_4 is depicted in Figures 3.11b and 3.11d. Figure 3.11c shows that for $\Lambda \to 0$, the reverse voltage can be calculated using the conventional formula for calculating the clamp capacitor voltage (2.59), whereas the input voltage can be used in Figure 3.11d. While v_{SR1} increases with a rising value of Λ, it actually results in a reduced voltage for v_{SR4}. This is caused by the voltage drop of the series inductance L_s, which reduces the voltage applied to the magnetizing inductance L_m, and in turn, the blocking voltage v_{SR4}.

While the synchronous rectifier voltage shows a large influence on the circuit parameters, they have only a minor influence on the synchronous rectifier currents.

Figure 3.12 shows the RMS currents I_{SR1} and I_{SR2} in dependency to the normalized value Γ and ζ (Figure 3.12a) and Γ and n (Figures 3.12b and 3.12c). For I_{D4} the influence of Γ and ζ is so small that a visualization is omitted.

Finally, the stress values of the magnetizing and output inductance are depicted in Figure 3.13. Figures 3.13a and 3.13b show the minimum normalized flux value in dependency of the series inductance through Λ and magnetizing inductance through ζ (Figure 3.13a) and for various conversion ratios n over the magnetizing inductance through ζ (Figure 3.13b). Figure 3.13c shows the flux ripple and, finally, Figure 3.13d shows the stress values for the output inductance through Γ.

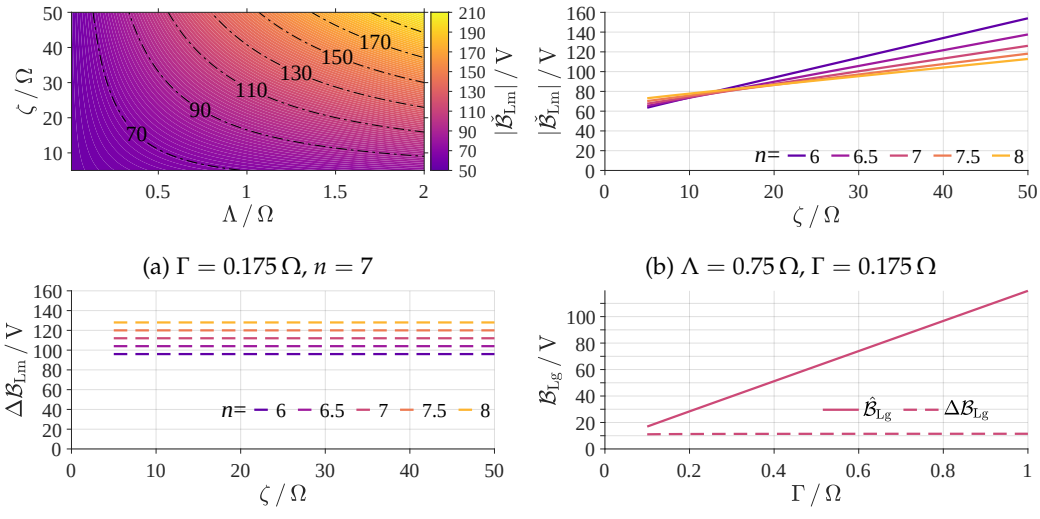


(a) $\Lambda = 0.75\,\Omega$, $N = 7$

(b) $\Lambda = 0.75\,\Omega$, $\zeta = 15\,\Omega$

(c) $\Lambda = 0.75\,\Omega$, $\zeta = 15\,\Omega$

FIGURE 3.12: Maximum synchronous rectifier current I_{SRi} of the ACFC. (a) Rectifier current I_{SR1} over Γ and ζ and (b) over Γ for various conversion ratios n. (c) Rectifier current I_{SR2} over Γ for various n. The dependency of the current I_{SR2} on Γ and ζ is negligible and below 2 %.



(a) $\Gamma = 0.175\,\Omega$, $n = 7$

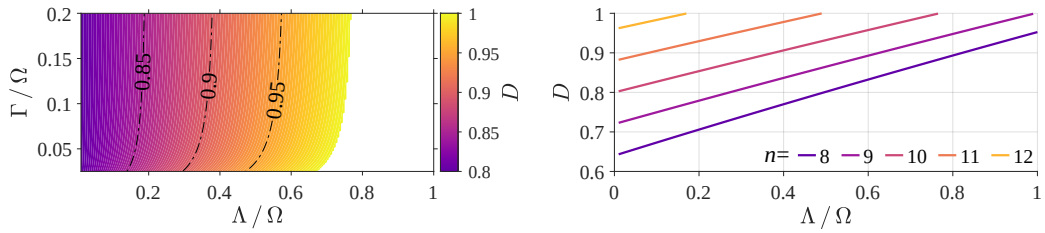
(b) $\Lambda = 0.75\,\Omega$, $\Gamma = 0.175\,\Omega$

(c) $\Lambda = 0.75\,\Omega$, $\Gamma = 0.175\,\Omega$

(d) $\Lambda = 0.75\,\Omega$, $\zeta = 15\,\Omega$, $n = 7$

FIGURE 3.13: Maximum inductor stress value for (a-c) the transformer and (d) the output inductor of the ACFC. (a) minimum inductor stress value over Λ and ζ, (b) minimum inductor stress value over ζ for various conversion ratios n, (c) ripple inductance stress value over ζ and (d) output inductor stress value over Γ.

3.3.3 Phase-shifted full bridge



(a) $\Gamma = 0.175\,\Omega$, $N = 10$ (b) $\Gamma = 0.75\,\Omega$, $\zeta = 15\,\Omega$

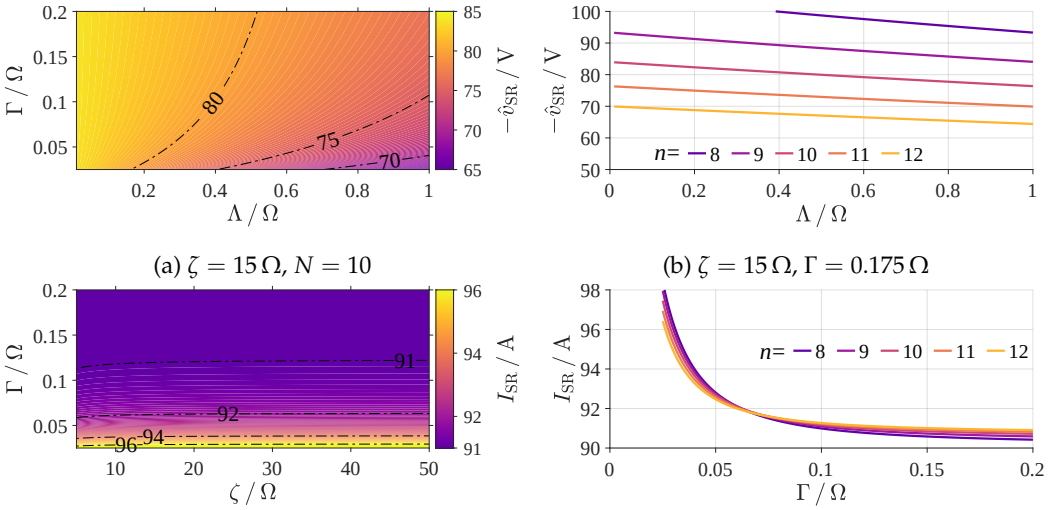
FIGURE 3.14: Duty cycle of the PSFB in dependency of (a) Λ and Γ and (b) over Λ for different conversion ratios n.

While for the active-clamp converter the reverse voltage is the most important design parameter, for the PSFB (cf. Figure 2.107), it is important that the duty-cycle is sufficient to achieve the maximum necessary gain. Figure 3.14 visualizes the duty cycle over the series inductance (Λ) and output inductance (Γ) (fig:Comp:PSFB:D) and for different conversion ratios over Λ in Figure 3.14b. Both the series inductance and conversion ratio have a significant impact on the necessary duty cycle. For the design of the converter, it is necessary to choose these values such that there is a sufficient control margin to account for dynamic transitions and parasitic circuit components.

The secondary stress values of the synchronous rectifiers are visualized in Figure 3.15. Analyzing the blocking voltage (Figures 3.15a and 3.15b), it is evident that a larger stray inductance (Λ) results in lower blocking voltages since the voltage drop over this parameter is increased. While smaller conversion ratios n may be preferable to achieve a large control margin for the duty cycle, for the blocking voltage, they significantly increase the blocking voltage reaching values above 100 V for low values of Λ (Figure 3.15b). Thus, large conversion ratios are preferable to reduce the voltage stress. While the impact of the conversion ratio on the voltage stress is significant, the influence on the RMS current (I_{SR}) is negligible (cf. Figure 3.15d). The major influence factor for the RMS current is the output inductance (Γ). However, even for very small Γ-values, the RMS current only increases by values much smaller than 10 % (Figures 3.15c and 3.15d).

The primary stressing values are depicted in Figure 3.16. The most important influence factors for the primary stressing values are the magnetizing inductance through ζ and the output inductance through Γ. Figure 3.16a shows the influence of these factors on the RMS current I_{sw}, whereas Figure 3.16b also depicts the influence of the conversion ratio n. Figure 3.16c shows the influence of Γ and ζ on the turn-off current i_{P2}, whereas Figure 3.16d depicts the influence of n. It is apparent that the stress of the primary switches can be reduced significantly by choosing a large magnetizing and output inductance.

Finally, the stress values of the magnetizing and output inductance are depicted in Figure 3.17



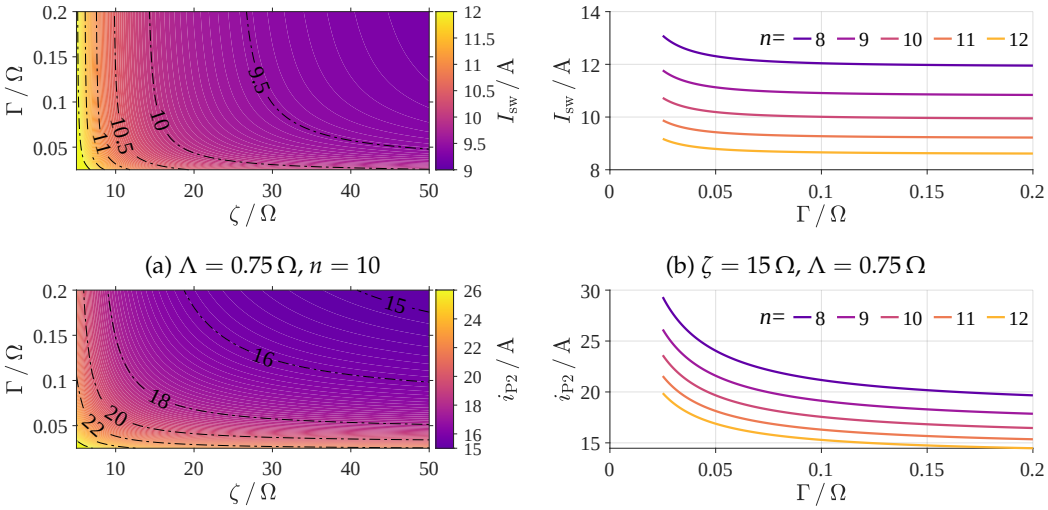
(a) $\zeta = 15\,\Omega$, $N = 10$

(b) $\zeta = 15\,\Omega$, $\Gamma = 0.175\,\Omega$

(c) $\Lambda = 0.75\,\Omega$, $N = 10$

(d) $\Lambda = 0.75\,\Omega$, $\zeta = 15\,\Omega$

FIGURE 3.15: Maximum synchronous rectifier (a,b) blocking voltage $\hat{v}_{SR}$ and (c,d) RMS current I_{SR} of the PSFB.



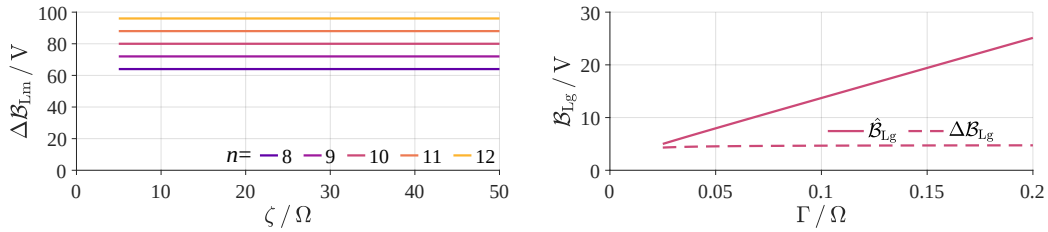
(a) $\Lambda = 0.75\,\Omega$, $n = 10$

(b) $\zeta = 15\,\Omega$, $\Lambda = 0.75\,\Omega$

(c) $\Lambda = 0.75\,\Omega$, $n = 10$

(d) $\Lambda = 0.75\,\Omega$, $\zeta = 15\,\Omega$

FIGURE 3.16: Maximum primary switch (a,b) RMS current $\hat{I}_{sw}$ and (c,d) turn-off current i_{P2} of the PSFB. Cut values that are unachievable (duty cycle).

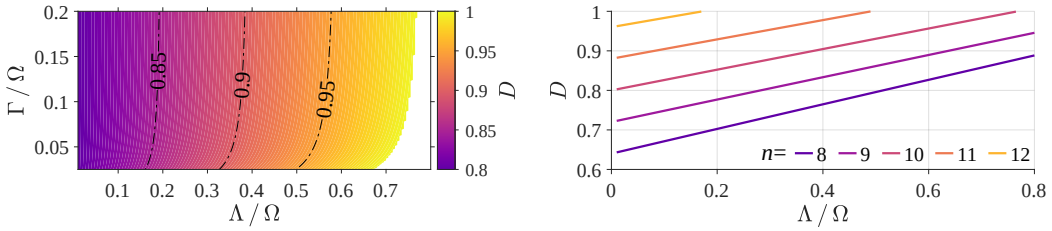


(a) $\Lambda = 0.75\,\Omega$, $\Gamma = 0.175\,\Omega$, $n = 10$

(b) $\Lambda = 0.75\,\Omega$, $\zeta = 15\,\mathrm{n}{=}10\Omega$

FIGURE 3.17: Maximum inductor stress value for (a) the transformer and (b) the output inductor of the PSFB.

3.3.4 Hard-switched full bridge



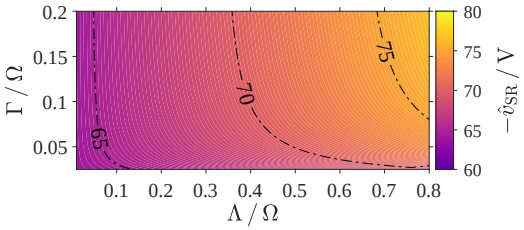
(a) $\Gamma = 0.175\,\Omega$, $n = 10$ (b) $\Gamma = 0.75\,\Omega$, $\zeta = 15\,\Omega$

FIGURE 3.18: Duty cycle of the HSFB in dependency of (a) Λ and Γ and (b) over Λ for different conversion ratios n.

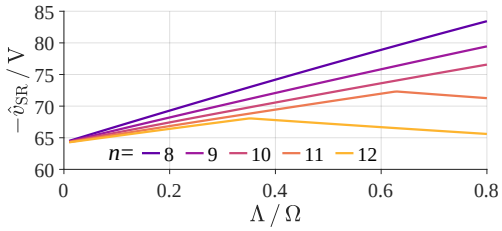
The operating principle of the HSFB is very similar to the PSFB because it employs the same components (cf. Figure 2.107). Thus, the visualization of the duty cycles in Figure 3.18 is nearly congruent to the one of the phase-shifted Figure 3.14. The duty cycle is visualized over Λ and Γ in Figure 3.18a and for different conversion ratios over Λ in Figure 3.18b. Again, both the series inductance L_s and conversion ratio n have a significant impact on the necessary duty cycle D.

The stress values of the synchronous rectifiers are visualized in Figure 3.19. Compared to the phase-shifted full bridge, the stressing values are fundamentally different, especially for the blocking voltage. This is mainly caused by switching from full-bridge mode to half-bridge mode and reverse. While for the phase-shifted full bridge, the blocking voltage reduces with increasing values of Λ, here this is not the case. The blocking voltage actually increases with increasing Λ (Figure 3.19a). For increasing Λ, the input voltage where a switch to half-bridge is possible is actually increased. This, therefore results in increased blocking voltages. However, considering Figures 3.19a and 3.19b, it is evident that this is not always the case. For large conversion ratios n and Λ-values, the blocking voltage eventually decreases again. When the slope of the blocking voltage changes, the converter changes operating mode at the maximum input voltage (420 V) such that the blocking voltage cannot increase further and the voltage drop at the series inductance again reduces the blocking voltage. The influence of the normalized circuit parameters and the conversion ratio n on the RMS current (I_{SR}) is again negligible (cf. Figure 3.19d). The major influence factor for the RMS current is the output inductance (Γ). Comparing the stess values of the phase-shifted full bridge (Figures 3.15c and 3.15d) to the ones of the isolated full-bridge converter, it is evident that the latter yields generally smaller RMS currents, which is caused by the freewheeling interval. For the phase-shifted full bridge, only one synchronous rectifier conducts the output inductor current (*see* Section 2.3.1A), whereas for the isolated full-bridge converter, the current is essentially distributed between both synchronous rectifiers when all primary switches are turned off (*see* Section 2.3.2).

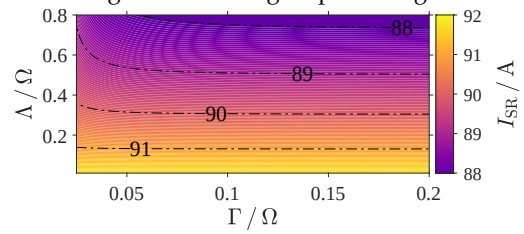
The primary stressing values are depicted in Figure 3.20. The RMS current is visualized in Figures 3.20a and 3.20b, whereas the turn-off current is depicted in Figures 3.20c and 3.20d. Comparing the visualized results to the ones of the phase-shifted full bridge (Figure 3.16), it is apparent that the RMS current is significantly smaller, whereas the turn-off current is similar. This is expected. The operating principle of the isolated full-bridge converter omits the freewheeling interval yielding smaller RMS currents, whereas the maximum turn-off current i_{P2} is the same.



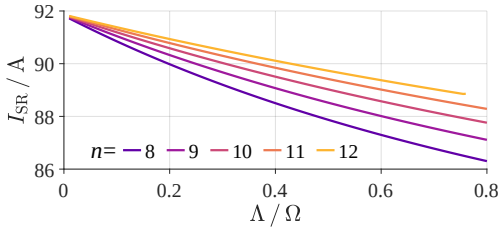
(a) $\zeta = 15\,\Omega$, $n = 10$; note: larger L_s result in a larger mode-change input voltage.



(b) $\zeta = 15\,\Omega$, $\Gamma = 0.175\,\Omega$

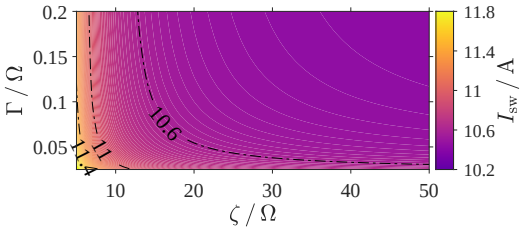


(c) $\Lambda = 0.75\,\Omega$, $n = 10$

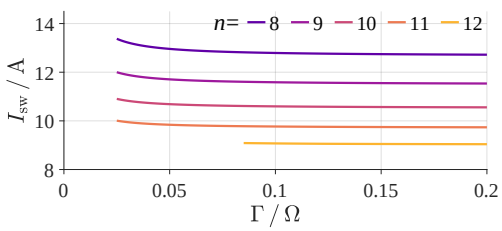


(d) $\zeta = 15\,\Omega$, $\Gamma = 0.175\,\Omega$

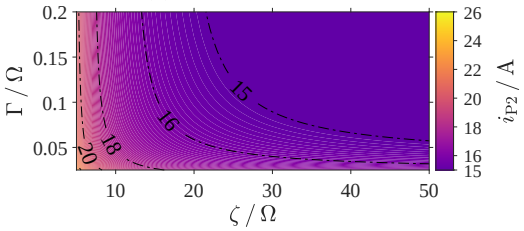
FIGURE 3.19: Maximum synchronous rectifier (a,b) blocking voltage $\hat{v}_{SR}$ and (c,d) RMS current I_{SR} of the HSFB.



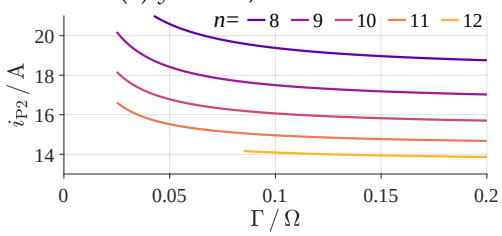
(a) $\Lambda = 0.75\,\Omega$, $n = 10$



(b) $\zeta = 15\,\Omega$, $\Lambda = 0.75\,\Omega$

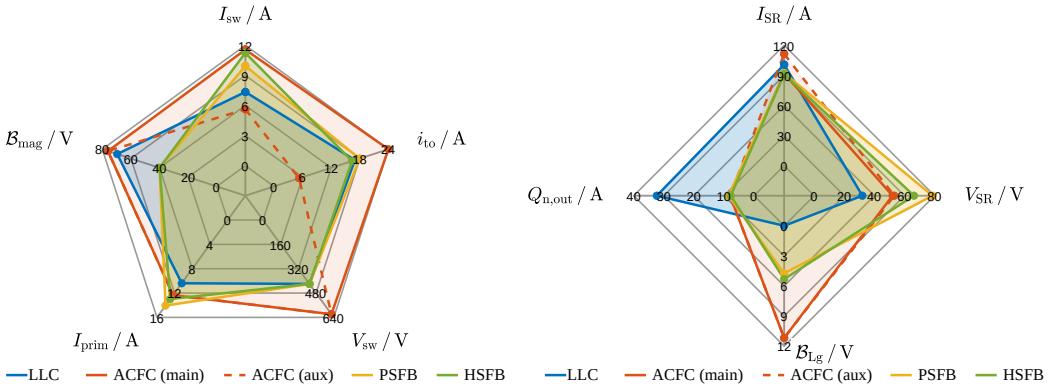


(c) $\Lambda = 0.75\,\Omega$, $n = 10$



(d) $\Lambda = 0.75\,\Omega$, $\zeta = 15\,\Omega$

FIGURE 3.20: Maximum primary switch (a,b) RMS current $\hat{I}_{sw}$ and (c,d) turn-off current i_{P2} of the HSFB.



(a) primary stress values

(b) secondary stress values

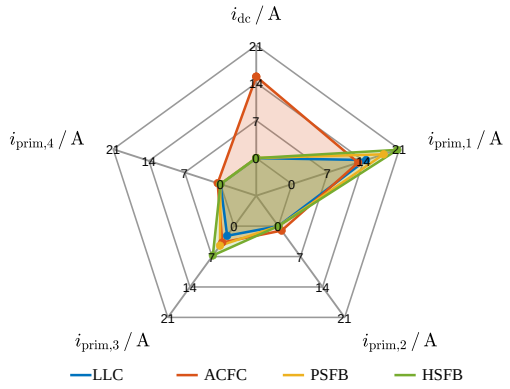
FIGURE 3.21: Worst-case stress values for the compared converters for the primary and secondary side. The secondary-side blocking voltage is visualized for a center-tapped rectifier.

3.3.5 Direct comparison

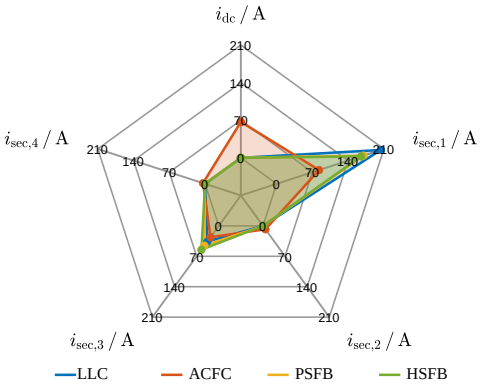
To better compare the different topologies, the worst-case stress values shall now directly be compared in a second step. For that purpose, a sample set of parameters, which matches the set of parameters selected for the prototypes that are described in Section 3.4.1, is selected and the stress values are compared for these sets of parameters. For the LLC, the parameters $Z = 19.4\,\Omega$, $\lambda = 0.333\,\Omega$, and $\zeta = 11.25\,\Omega$ are selected; for the ACFC, the parameters are $\Lambda = 0.75\,\Omega$, $\Gamma = 0.175\,\Omega$, and $\zeta = 11.25\,\Omega$ with $n = 7$, for the PSFB, the set is $\Lambda = 0.5\,\Omega$, $\Gamma = 0.07\,\Omega$, and $\zeta = 20\,\Omega$ with $n = 10$, and finally for the HSFB, the parameters are $\Lambda = 0.15\,\Omega$, $\Gamma = 0.05\,\Omega$ and $\zeta = 15\,\Omega$ with $n = 10$.

The stress values are compared for the primary and secondary side in Figure 3.21 in a spider plot, which allows a direct comparison of the various stress values. However, it shall be emphasized that the spanned area is no measure of the quality of the converter and that the stress values need to be considered individually. The visualization of the primary stress values of Figure 3.21a shows that the LLC has relatively low stress values with the minimum primary transformer current I_{prim}, the lowest maximum switch current I_{sw}, and a good primary switch voltage V_{sw}. However, the transformer stress $\mathcal{B}_{mag}$ is relatively large. Compared to the LLC, the ACFC has a significantly larger switch current I_{sw} and turn-off current i_{to} for a single switch compared to the four switches of the LLC. The auxiliary switch stress (dashed line) is compared to the main switch significantly lower. The ACFC also shows a larger transformer stress compared to the LLC. Comparing the PSFB to the aforementioned converters shows an intermediate switch current I_{sw} and a good turn-off current and transformer stress. Finally, the HSFB shows a good overall performance but requires an additional large blocking capacitor, which is not depicted in the graphs. However, due to the frequency-doubler operation, the switch current is larger compared to the PSFB.

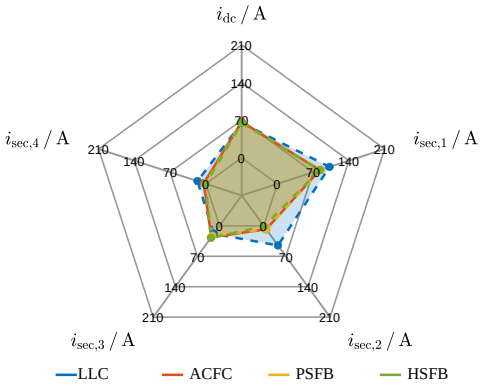
The stress values for the secondary side that are visualized in Figure 3.21b show that the LLC has a very large output charge $Q_{n,out}$ with a small blocking voltage and an intermediate synchronous rectifier RMS current. It benefits from the fact that it does not require an output inductor L_g. In comparison to the LLC, the ACFC shows



(a) Primary fourier coefficients of the transformer current



(b) Secondary fourier coefficients of the (full-bridge) transformer current



(c) Secondary fourier coefficients of the (center-tapped) transformer current

FIGURE 3.22: Fourier coefficients (first five harmonics) of the transformer currents

a much smaller output charge and synchronous rectifier blocking voltage V_{SR}. The RMS currents of the synchronous rectifier are also larger and it shows the largest stress for the output inductor. The PSFB shows quite good stress values for $\mathcal{B}_{Lg}$, I_{SR} and $Q_{n,out}$ but disqualifies itself with the large synchronous rectifier voltage V_{SR}, which is too large even for semiconductors with a voltage rating of 100 V. Finally, the HSFB shows similarly good stress values compared to the PSFB but has a much better synchronous rectifier blocking voltage resulting from the use of half-bridge modulation. This allows the application of 100 V synchronous rectifier MOSFETs .

The RMS current for the primary and secondary side of the transformer have been visualized in Figure 3.21 together with the core stress $\mathcal{B}_{mag}$. However, these stress values do not offer a definitive picture because they do not depict the fourier coefficients of the currents such that the impact of high-frequency amplitudes cannot be considered. For that purpose, Figure 3.22 shows the first five fourier coefficients of the primary transformer currents in Figure 3.22a, with the secondary transformer currents in Figure 3.22b for a full-bridge rectifier of the LLC, PSFB, and HSFB, and the secondary transformer currents in Figure 3.22c for a center-tapped transformer. The value i_{dc} is hereby the DC component of the fourier coefficient describing the average current only producing DC losses and no eddy-current losses. The value $i_{prim,k}$

and $i_{\mathrm{sec},k}$ describes the AC component of the primary and secondary current respectively with k being the frequency component with $k = 1$ being the base operating frequency. The analysis shows that the first-order amplitude of the ACFC is always the lowest of all the converters as this topology shows a significant DC current for the primary and secondary side. Since the DC losses are usually much smaller compared to the high-frequency components, it can be assessed that this topology may experience much smaller winding losses compared to the other topologies. Even if a center-tapped version is employed for the LLC, PSFB, and HSFB, the ACFC has only one secondary winding vs. two for the other topologies.

Considering the aforementioned analysis, the LLC, the ACFC, and the HSFB have been selected for further analysis and experimental evaluation. The PSFB disqualifies itself due to the excessively large synchronous rectifier voltage, which prevents the use of MOSFETs with a blocking voltage of 100 V. The next larger blocking voltage of commonly available MOSFETs is 150 or even 200 V, which come with a significantly larger on-state resistance and costs. According to the procedure presented in Figure 3.1, these values could be used for a Pareto optimization of the converter by limiting the normalized parameters to a range of these values. The Pareto optimization can then be used to analyze hundreds of different designs to output Pareto fronts that can be used to select the converter that is optimal in terms of costs, power density and efficiency. However, for the sake of brevity, the Pareto optimization of the converter is not performed and the evaluation will be limited to an exemplary design.

The resonant frequency of the LLC has been selected to be $f_\mathrm{r} = 100$ kHz as the LLC has a large amplitude of the secondary transformer current. Due to the large currents of the secondary side, litz wires are not an option such that stamped copper sheets are required. This means that eddy currents cannot be suppressed, which prevents high resonant frequencies. With the selected resonant frequency, the resonant tank parameters have been defined with

$$L_\mathrm{r} = \frac{Z}{2\pi f_\mathrm{r}}, \quad L_\mathrm{m} = \frac{L_\mathrm{r}}{\lambda}, \quad C_\mathrm{r} = \frac{1}{2\pi f_\mathrm{r} Z} \tag{3.14}$$

to $L_\mathrm{r} = 31$ µH, $C_\mathrm{r} = 82$ nF, and $L_\mathrm{m} = 93$ µH. The ACFC requires a much larger switching frequency due to the high core stress $\mathcal{B}$. This is also enabled by the significantly smaller secondary-side current amplitude of the transformer. For that purpose, the switching frequency is selected to be $f_\mathrm{sw} = 250$ kHz such that the circuit values can be calculated with

$$L_\mathrm{s} = \frac{\Lambda}{f_\mathrm{sw}}, \quad L_\mathrm{m} = \frac{\zeta}{f_\mathrm{sw}}, \quad L_\mathrm{g} = \frac{\Gamma}{f_\mathrm{sw}} \tag{3.15}$$

to $L_\mathrm{r} = 3$ µH, $L_\mathrm{m} = 45$ nF, and $L_\mathrm{g} = 700$ nH with $N_1 : N_2 = 7 : 1$. Due to the high transformer core stress $\mathcal{B}_\mathrm{mag}$, a second version is also built up with f_sw, $N_1 : N_2 = 15 : 2$ with the same circuit values. Due to the large core stress, which is load-independent, a high light-load efficiency is essentially prevented with $N_1 : N_2 = 7 : 1$ such that a much larger light-load efficiency can be achieved with $N_1 : N_2 = 15 : 2$. The HSFB can be operated at a significantly smaller switching frequency due to the low core stress of the primary side $\mathcal{B}_\mathrm{mag}$ and secondary side $\mathcal{B}_\mathrm{Lg}$. For that purpose, the switching frequency has been selected to be $f_\mathrm{sw} = 75$ kHz such that the circuit parameters can be calculated with (3.15) to $L_\mathrm{r} = 2.5$ µH, $L_\mathrm{m} = 45$ nF, and $L_\mathrm{g} = 700$ nH.

3.4 Experimental Evaluation

To experimentally verify the effectiveness of the three preselected topologies, the LLC, the ACFC, and the HSFB are build up and experimentally tested. Section 3.4.1 gives an overview of the build-up topologies, the cooling system used to dissipate the power loss of the surface-mounted device (SMD) components is discussed in Section 3.4.2, and the stationary performance of the topologies is discussed in Section 3.4.3.

3.4.1 Overview of the developed prototypes

The parameters of all prototypes are listed in Table 3.2 and the developed prototypes are depicted in Figure 3.23. The prototype of the LLC resonant converter with silicon MOSFETs IPW65R080CFDA [Inf12] is depicted in Figure 3.23a. The dimensions of the prototype for two parallel LLCs are (width×length×height) 156 mm × 196 mm × 28 mm amounting to a volume of 0.856 liters without the aluminum chassis, the EMI filter[1] and the transformer as the largest component. On the left side is the input EMI filter connected to the two full-bridge LLC inverters with the control board placed by board-to-board connectors onto the main board in the middle. Between the main board and the rectifier board are the two transformers and the resonant coils. The secondary side of the transformers is directly screwed onto the high-current terminals of the rectifier board. A busbar connects the center-tapped 12 V-potential directly to the low-voltage reverse-polarity protection MOSFETs . The synchronous rectifier MOSFETs are two parallel *Opti-MOS* switches of type *IAUT300N08S5N012* [Inf22], which are bottom cooled through the PCB. To limit the computational complexity of driving the synchronous rectifiers in each of the four modes of operation, they are driven by a self-controlled synchronous driver (*IR11688STRPBF* [Inf15b])[2]. The transformer has a 15-turn primary and two 1-turn secondary windings on an *ER54/28/38* ferrite core. While the primary winding is made of litz wire having a strand diameter of 0.1 mm, the secondary side windings are made of two parallel 0.5 mm copper sheets. The resonant inductor utilizes a 17-turn winding on a *PQ-32/25* core.

The prototype of the LLC with SiC MOSFETs of type C3M0060065J (Cree 650 V, 60 mΩ, [Cre20a])is depicted in Figure 3.23b. The dimensions of the prototype for two parallel LLCs are (width×length×height) 160 mm × 194 mm × 28 mm amounting to a volume of 0.856 liters without the aluminum chassis and the transformer as the largest component. On the left side is the input connected to the two full-bridge LLC inverters, which are packaged in a TO263-7 package. The control board placed by board-to-board connectors onto the main board in the middle. Between the main board and the rectifier board are again the two transformers and the resonant coils. In this picture only one LLC is fully assembled. The secondary side of the transformers is again directly screwed onto the high-current terminals of the rectifier board. Similar to the silicon verison, a busbar connects the center-tapped 12 V-potential

[1] for comparability, the EMI filter is neglected as the Si LLC is the only converter with an EMI filter. The other converters have been developed without such a filter.

[2] the self-controlled integrated driver was used as other methods [SSM19b; BSB19; SSM19a] require a full-bridge on the secondary side whereas for this circuit a center-tapped rectifier is employed. The self-controlled integrated driver measures the drain-source voltage only to drive the secondary switches.

TABLE 3.2: Parameters of the developed prototypes

(a) Si LLC

Component	Type
Primary MOSFETs	IPW65R080CFCC
Rectifier MOSFETs	IAUT300N08S5N012 (2 par.)
ORing MOSFETs	IPT026N10N5 (3 par.)
Resonant inductor	30 µH, $N = 17$,PQ32/25
Transformer (N_p:N_{s1}:N_{s2})	15:1:1,P95, ER54/38/30 $L_m = 90$ µH
Resonant capacitance	80 nF
Resonant frequency	100 kHz

(b) SiC LLC

Component	Type
Primary MOSFETs	C3M0060065J
Rectifier MOSFETs	IAUT300N08S5N012 (2 par.)
ORing MOSFETs	IPT026N10N5 (3 par.)
Resonant inductor	30 µH, $N = 17$,PQ32/25
Transformer (N_p:N_s)	7:1, 15:1, ER54/38/30 P95, $L_m = 90$ µH
Resonant capacitance	80 nF
Resonant frequency	100 kHz

(c) ACFC

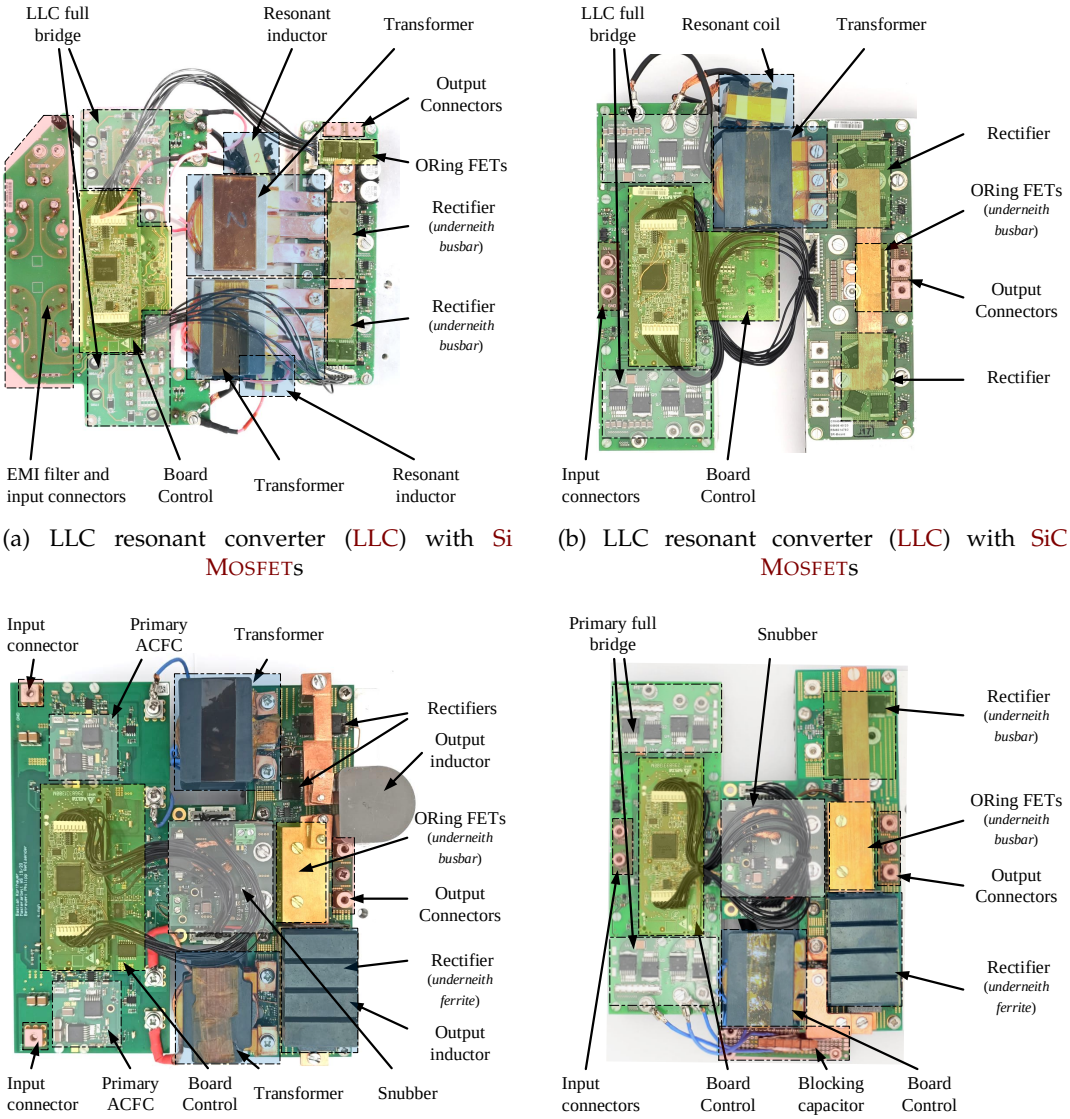
Component	Type
Primary MOSFETs	C3M0065090J, C3M0120090J
Rectifier MOSFETs	IAUT300N10S5N015 (2 par.)
ORing MOSFETs	IPT026N10N5 (3 par.)
Output inductor	700 nH
Transformer (N_p:N_s)	7:1, 15:1, $L_m = 200$ µH P49, ER54/38/30
Clamp capacitance	300 nF
Switching frequency	250 kHz 150 kHz

(d) HSFB

Component	Type
Primary MOSFETs	C3M0060065J
Rectifier MOSFETs	IAUT300N10S5N015 (2 par.)
ORing MOSFETs	IPT026N10N5 (3 par.)
Output inductance	700nH
Transformer (N_p:N_{s1}:N_{s2})	10:1:1, ER54/38/30 P49, $L_m = 200$ µH
Blocking capacitance	14 µF
Switching frequency	75 kHz

directly to the low-voltage reverse-polarity protection MOSFETs . The synchronous rectifier MOSFETs are two parallel *Opti-MOS* switches of type *IAUT300N08S5N012* [Inf22], which are bottom cooled through the PCB. They are again driven by the self-controlled synchronous driver *IR11688STRPBF* [Inf15b]. The transformer has a 15-turn primary and two 1-turn secondary windings on an *ER54/28/38* ferrite core with the same winding structure of the silicon LLC. The resonant inductor again utilizes a 17-turn winding on a *PQ-32-25* core. The output MOSFETs required for the OR-ing functionality are equally the three parallel MOSFETs of type *IPLU300N04S4–R8* [Inf15a]. The prototype is operated at the same resonant frequency compared to the LLC with Si MOSFETs . In the supervised master thesis of *Hankeln* [Han21][1], it has been attempted to operate the LLC at switching frequencies 50 % larger than the chosen resonant frequency of $f_{res} = 100$ kHz. However, the secondary-side winding losses of the transformer prevented an operation at an elevated resonant frequency. The eddy current losses inside the transformer resulted in thermal hotspots of intolerable temperatures. It was also attempted to setup the secondary winding with litz wires. However, this led to intolerable hotspots at the connections. Thus, this converter is equally operated at a resonant frequency of $f_r = 100$ kHz.

[1] in the same thesis, the efficiencies of the Si and SiC that are depicted in Figure 3.25 and Figure 3.26 were measured.



(a) LLC resonant converter (LLC) with Si MOSFETs

(b) LLC resonant converter (LLC) with SiC MOSFETs

(c) Active-clamp forward converter (ACFC)

(d) Hard-switched full-bridge converter (HSFB)

FIGURE 3.23: Hardware photos of the developed prototypes.

The developed dual-rail prototype of the ACFC is depicted in Figure 3.23c. The dimensions of the prototype for two parallel ACFCs are (width×length×height) 193 mm × 210 mm × 28 mm amounting to a volume of 1.13 liters without the aluminum chassis and the transformer as the largest component. The left side of the prototype shows the primary PCB with the two times two primary semiconductors and the control board in the center. For the main switch S_1, the semiconductor *C3M0065090J* (Cree 900 V, 65 mΩ, [Cre19a]) was selected, for the auxiliary MOSFET , the switch *C3M0120090J* (Cree 900 V, 120 mΩ, [Cre20b]) was chosen. Both are bottom-cooled SMD components. The cooling concept will be discussed in Section 3.4.2. The secondary semiconductors are two parallel Infineon Optimos 100 V, 1.5 mΩ MOSFETs (*IAUT300N10S5N015* [Inf17]) for SR_1 and SR_2. The SRs are rectified using a self-sufficient driver (*NCP4305* [ON 16]). The switching frequency was set to 250 kHz to achieve a balance of small magnetic components and switching losses. With the definition of the switching frequency, the transformer was build up with a 7:1 turns ratio consisting of seven primary litz wire windings, three parallel

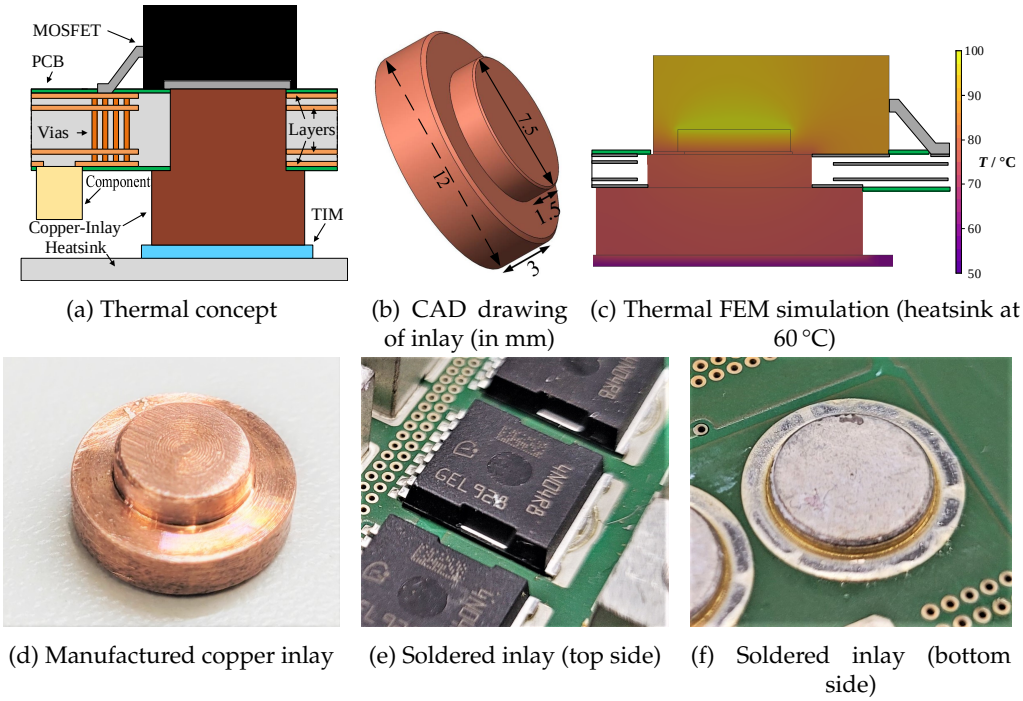
copper sheet windings of 500 µm thickness and the transformer core ER54/38/20. The 15 : 2 transformer is depicted on the top. Between the transformers is the snubber circuit, which is addressed in Section 2.2.5. The right side shows the secondary PCB with the output inductor, which is assembled as a ferrite around a busbar. The synchronous rectifiers are placed below this ferrite and the snubber with the buck converter is placed in the center.

The developed dual-rail prototype of the HSFB is depicted in Figure 3.23d. The dimensions of the prototype for two parallel HSFBs are (width×length×height) 172 mm × 210 mm × 28 mm amounting to a volume of 1.01 liters without the aluminum chassis and the transformer as the largest component. The left side of the prototype shows the primary PCB with the two full-bridge inverters and the control board in the center. For the switches the semiconductor *SCT3120AW7* [ROH20] was chosen as it has a low output capacitance, which is important as this converter is partially hard switching. The MOSFETs are bottom-cooled SMD components. with the same cooling system of the ACFC and SiC LLC discussed in Section 3.4.2. The secondary semiconductors are two parallel MOSFETs of type *IAUT300N10S5N015* (Infineon Optimos 100 V, 1.5 mΩ, [Inf17]) for SR_1 and SR_2. The transformer was build up with a 10:1 turns ratio consisting of 10 primary litz wire windings and three parallel copper sheet windings of 500 µm thickness and the transformer core ER54/38/20. The right side shows the secondary PCB with the output inductor, which is again assembled as a ferrite around a busbar. The synchronous rectifiers are placed below this ferrite and the snubber with the buck converter is placed in the center.

3.4.2 Cooling concept of the SMD power MOSFET

this section has been previously published in parts in [Reh+22a].

To dissipate the heat of SMD semiconductors, a number of different methods has been employed in the past [Str+20]. By introducing thermal vias, the heat can be dissipated through the PCB vias connecting the top and bottom layer [NS11; Gau+13; MZ04; Sha+20]. However, the possible heat dissipation is low resulting in a large thermal resistance. A better heat dissipation can be achieved through pedestals, where a piece of copper is placed between the top and bottom layer [LC10; Wei+19; Str+20]. Similarly, it is also possible to insert a piece of ceramic such as aluminium nitride (AlN) between the top and bottom layer for a reduced thermal resistance [Sha+20]. While these methods allow the application of a multi-layer PCB, the insertion of copper or a piece of ceramic is costly. Another possibility is the use of an insulated metal substrate [Sha+09; LHM15; Jor+09; Jaf+21] where the heat dissipation is very good but the layer number is limited to two. However, the heat dissipation is very good. In this work, the heat dissipation is achieved through a thermal inlay, which can be placed as an SMD component. Figure 3.24a shows the setup. The inlay is placed into the PCB and connected by solder to the sides. The component is placed on the other side on the top layer. A TIM is placed between the copper inlay and the heatsink to achieve the required isolation. The inlay itself acts like a heat spreader as the surface area, which is connected to the TIM is increased. This concept is similar compared to the approach described in [Sie+17] where an external heat spreader that is soldered onto the device, which is made of copper, was



(a) Thermal concept

(b) CAD drawing of inlay (in mm)

(c) Thermal FEM simulation (heatsink at 60 °C)

(d) Manufactured copper inlay

(e) Soldered inlay (top side)

(f) Soldered inlay (bottom side)

FIGURE 3.24: (a) Employed cooling concept for the primary and secondary semiconductors (not to scale). A copper inlay is soldered into the PCB. (b) construction drawing of the inlay (in mm), (c) finite-element method (FEM) thermal simulation of the inlay, (d) manufactured copper inlay, (e) soldered inlay (top side), and (f) soldered inlay (bottom side).

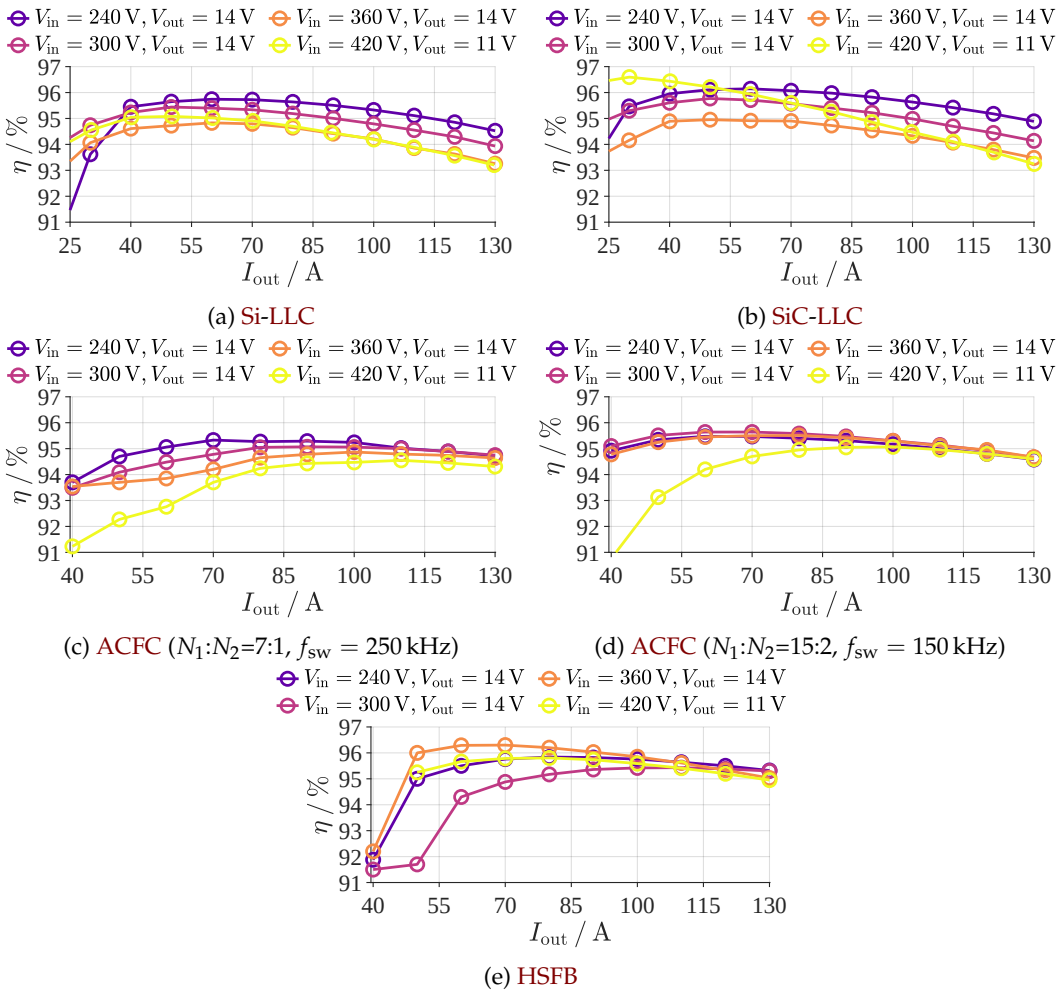
employed for a top-cooled device. In this work, the internal heat spreader that is soldered into the PCB is employed for a bottom-cooled device. A construction drawing of the inlay is depicted in Figure 3.24b. A FEM simulation is depicted in Figure 3.24c for a power dissipation of 20 W and a heatsink temperature of 60 °C. The manufactured inlay is depicted in Figure 3.24d and Figures 3.24e and 3.24f show the inlay that is soldered into the PCB. In the manufacturing process, the PCB is first assembled from the bottom side where the inlay is soldered into the board and then the top side is assembled where the MOSFET is placed onto the inlay.

3.4.3 Stationary performance of the prototypes

this section has been previously published in parts in [Reh+22a].

The efficiencies of all converters are depicted in Figures 3.25 and 3.26. The efficiency of the LLC with silicon MOSFETs is depicted in Figure 3.25a. It achieves a top efficiency of about 96.5 %. For the first three depicted lines, the converter is operated in full-bridge mode, for the yellow line, it is operated in half-bridge mode. The clear reduction in efficiency for lower gains in full-bridge mode resulting from increased switching frequency is clearly recognizable. By switching to half-bridge mode, a large proportion of the losses can be reduced yielding a higher partial load efficiency. Overall, the efficiency is mostly kept above 93 %.

The efficiency of the LLC resonant converter with SiC MOSFETs is depicted in Figure 3.25b. It achieves a top efficiency of about 96.8 %. Again, for the first three



(a) Si-LLC

(b) SiC-LLC

(c) ACFC (N_1:N_2=7:1, $f_{sw} = 250\,kHz$)

(d) ACFC (N_1:N_2=15:2, $f_{sw} = 150\,kHz$)

(e) HSFB

FIGURE 3.25: Measured efficiencies of all the developed converters over the output load.

depicted lines, the converter is operated in full-bridge mode, for the yellow line, it is operated in half-bridge mode. The clear reduction in efficiency for lower gains in full-bridge mode resulting from increased switching frequency is also clearly visible for these switches because most losses are caused by eddy currents in the magnetic components and not in the primary inverter switches. Overall, the efficiency is mostly kept above 93 %.

The developed ACFC achieves a top efficiency of about 95 %. Figure 3.25c shows the measured efficiencies for different operating points over the output current. Since the high core losses are almost load independent, the top efficiency is quite limited and the efficiency reduces substantially for low loads. However, for increased output currents, the efficiency drop is quite limited and the converter achieves similar efficiencies for different operating points. Compared to the results reported in [Reh+22a], the efficiency of the converter was substantially increased by a new rectifier integrated circuit (IC) and by shielding the driver from the magnetic field of the output inductor. To address the high core losses, the converter was modified to a 15:1 transformer (depicted in Figure 3.23c, bottom) with a magnetizing inductance of 105 µH and an increased output inductance of 1.5 µH, which was operated at 150 kHz (*see* Table 3.2). The achieved efficiencies are depicted in Figure 3.25d.

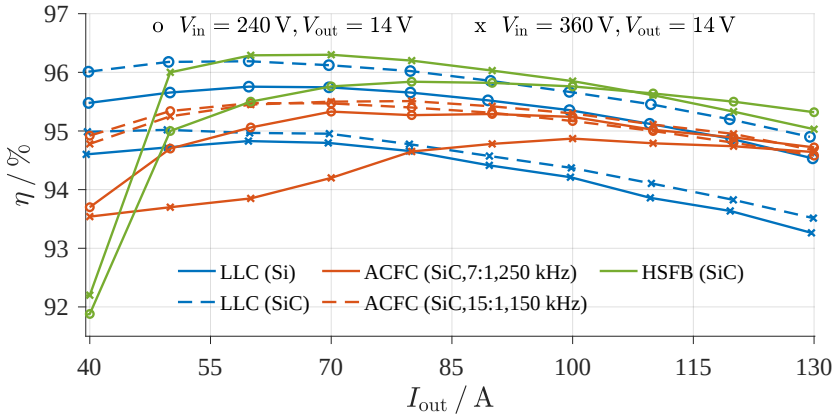


FIGURE 3.26: Comparison of the measured efficiencies of the prototypes for two exemplary operating points.

Compared to the ACFC with a turns ratio of 7:1, the efficiency is substantially increased for low loads by the reduced core losses. The top efficiency is now about 95.8 %.

The efficiency of the hard-switched full bridge with SiC MOSFETs is depicted in Figure 3.25e. It achieves a top efficiency of about 96.5 %. Again, for the first two depicted lines, the converter is operated in full-bridge mode while for the last two lines, it is operated in half-bridge mode. For low output currents, a clear reduction in efficiency can be noticed, which is caused by a deactivation of the synchronous rectifiers. At these currents, the converter enters the DCM or CCMb mode, for which a control of the synchronous rectification has not been developed. If an appropriate control were to be developed, a similar efficiency as for CCM can be expected.

The efficiencies of all the converters are compared in Figure 3.26. By considering the efficiency comparison, it is evident that the efficiency of the LLC resonant converters reduces significantly for smaller voltage-transfer ratios (360 V to 14 V) whereas for an operation near resonance (240 V to 14 V), the efficiency is very high. Compared to the LLC, the ACFC offers relatively constant efficiencies, independently from the operating point, which are also relatively constant over the output load. A similar observation can be made for the HSFB. Overall, the HSFB achieves the highest and most constant efficiency.

3.5 Conclusion

The selection of a suitable isolated topology for a given application is one of the most impactful decisions in power electronics to achieve the required efficiency, power density and costs. The designer is confronted with various different topologies with a diversity of components and their corresponding component stress. However, in the design, the switching frequency is hereby one of the most important design parameters as it influences both the power density, the efficiency, and also the costs. To compare the topologies without selecting a random switching frequency, a frequency-independent topology design and comparison methodology was proposed to compare the LLC resonant converter, the active-clamp forward converter, the phase-shifted and hard-switched full bridge. The comparison was achieved by introducing frequency-independent stress quantities and circuit parameters. By comparing the stress quantities, the circuits can be directly numerically evaluated without requiring the designer to preselect a specific switching frequency or predesign the converter. With the analysis the phase-shifted full bridge has been excluded from the actual experimental evaluation as the rectifier blocking voltage is too large to employ synchronous rectifiers of a blocking voltage of 100 V. The remaining topologies have been experimentally built up and tested. The experimental evaluation showed that the LLC achieves a very high top efficiency but that for intermediate gains, the efficiency reduces significantly due to significantly larger switching frequency as a result from increased switching and winding losses. Compared to the LLC, the ACFC offers relatively constant efficiencies, independently from the operating point, which are also relatively constant over the output load. The high core losses in a configuration with a turns ratio of 7:1 prevent high efficiencies such that only a turns ratio of 15:2 achieves acceptable efficiencies above 95 %. The HSFB achieves a very high peak efficiency, which is also quite constant over the load and gain. Overall, the HSFB achieves the highest and most constant efficiency. Due to the simple and effective control method, it can be considered one of the best topologies for the given application. While it does require switching from half-bridge to full-bridge mode and reverse, the pulse-width control does not have the disadvantages of increased switching frequencies of low gains and the blocking voltage is also limited to 420 V, which is neither load dependent. The HSFB can also be operated at a low (constant) switching frequency (< 100 kHz) due to the low inductor and transformer stress. The reduced switching frequency is in turn beneficial to reduce eddy current losses. Generally, this topology offers low stress values resulting in high efficiencies.

Chapter 4

Conclusion and Outlook

4.1 Conclusion

On-board DC-DC converters are the connecting link between the traction battery and the auxiliary battery coupling the high-voltage traction bus with the low-voltage auxiliary bus. This work addresses wide conversion range necessary to cover the voltage-transfer ratio resulting from the varying state of charge of the traction and auxiliary battery. Three topologies are analyzed for that purpose: the *LLC resonant converter*, the *active-clamp forward converter* and the *isolated full-bridge converter*. The first objective of this thesis is the analysis of these topologies to derive modeling methods, modulation strategies, concepts for magnetic integration, and clamping approaches.

To cover the wide voltage-transfer ratio with an LLC resonant converter, a number of different operating modes is required. Full-bridge and half-bridge mode are used for large and small gains respectively and phase-shift modulation is used for intermediate loads and gains. It is shown that the frequency-doubler modulation and the alternating-asymmetrical phase-shift modulation perform significantly better compared to the half-bridge and phase-shift modulation yielding a substantially lower junction temperature. To switch from one mode to the other, an on the on-the-fly topology morphing concept is required, which conventionally suffers from an increased magnetizing flux during the process. This thesis, thus, proposes an improved modulation to substantially reduce the offset by an average of about 70 %, enabling transformers of reduced core cross sections. Two converter rails are balanced. To utilize ripple cancellation when operating at an equal switching frequency, an asymmetrical balancing modulation and phase-shift modulation is employed in half-bridge and full-bridge mode respectively. This can substantially reduce the output capacitor size. Finally, this thesis proposes a method to integrate the resonant inductance and the transformer with the magnetizing inductance into one magnetic component. The developed planar integration concept can increase the magnetic power density and reduce the component costs.

The operating concept of the ACFC is substantially easier compared to the complex operation of the LLC. However, it requires a snubber to limit the rectifier blocking voltages. Thus, a snubber concept is proposed to clamp the high-voltage oscillations resulting from the resonance of the series inductance and the output rectifiers'

output capacitance. With the proposed snubber, the rectifier blocking voltage can be clamped to a pre-defined value such that rectifiers of a smaller blocking voltage can be employed.

The third topology of interest, is the hard-switched full-bridge converter. To limit the secondary blocking voltages, the circuit is operated in half- and full-bridge mode. To counter the unbalanced losses during half-bridge modulation, a hard-switched frequency-doubler modulation is proposed, which can substantially reduce the maximum switch temperature. To transition from the hard-switched full-bridge modulation to the hard-switched half-bridge operation and reverse, an on-the-fly morphing method is required, which conventionally suffers from two major flaws: an increased transformer flux and increased blocking voltages for the rectifier semiconductors. Thus, an adapted modulation and two clamping approaches are proposed, which can significantly improve the performance.

To compare the three topologies, a design-based frequency-independent topology comparison methodology is proposed to benchmark the converter topologies independently from one of the most important design parameters – the switching frequency. The converters are finally evaluated experimentally. It is shown that the ACFC together with its easy and straightforward control achieves a good and constant efficiency over the entire operating region. However, the topology cannot achieve the high peak efficiency of the HSFB and LLC and shows a clear efficiency reduction for very low loads. If a high low-load efficiency is required, the LLC should be the topology of choice achieving the highest low-load efficiency and a good peak efficiency in operating points with a large gain. However, for lower gains, it suffers from a clear reduction in efficiency and the control concept is complex. The HSFB on the other hand achieves a very stable efficiency in the entire operating range coupled with a good peak efficiency with a slightly easier control concept. However, similarly to the ACFC, the light-load efficiency is also limited.

4.2 Outlook

Building on the insights gained in this thesis, a number of different options for follow-up investigations arise. Based on the analysis of the common-mode implications of the alternating phase-shift modulations of increased modulation lengths, an experimental benchmark of multi-period alternating asymmetrical phase-shift modulations should be performed to experimentally verify the effectiveness. It should also be investigated whether loss-balancing frequency-multiplier modulations with modulation lengths larger than four times the current-shape period can be beneficial for the EMI emissions. This should also be performed for the hard-switched frequency-doubler modulation for the isolated full-bridge converter and its corresponding hard-switched frequency-multiplier modulations.

It should be investigated whether an optimum modulation sequence exist to morph between the operating modes within a few switching periods. This would also enable a continuous morphing between both half-bridge modes to further reduce the switch temperatures while avoiding the undesired temperature ripple. The morphing within several tens of microseconds makes it possible to dwell in each half-bridge mode for several milliseconds only such that the larger thermal time constants of the switch foster network prevents the temperature ripple.

An investigation of a similar magnetic integration for a center-tapped rectifier should be started as this type of rectifier is more common for low-voltage outputs than the full-bridge type. If a similar simple method exists, this would be beneficial for a wide adoption in server power supplies, where the center-tapped rectifier is the most typical rectifier.

For the isolated full-bridge converter, the feasibility of the proposed TVS diode clamping structure should be experimentally investigated and validated. However, the necessity for additional components is one of the major drawbacks when employing the isolated full-bridge converter in half-bridge and full-bridge mode. Therefore, an investigation into an optimal morphing modulation over few switching periods should be performed to analyze whether the clamping circuit can be avoided overall.

To adopt GaN semiconductors for onboard DC-DC converters with a traction battery of 800 V, the effectiveness of the flying-capacitor DC-DC converters should be experimentally verified as the high bus voltage is a clear limitation of the application of high-performing GaN semiconductors in this application.

Finally, the comparison of frequency-independent stress values lacked the inclusion of the most important traits of a converter: costs, power density and efficiency. Therefore, the comparison can be understood as the first step to define the converter parameters before performing a three-dimensional pareto optimization for comparison of the aforementioned traits. The comparison should, thus, be extended for these traits.

Finally, the dynamics of the converter topologies were not subject of the investigation of this thesis. However, since high dynamics are more and more important to reduce the size of the auxiliary lead-acid battery, the analysis should be performed to derive, which topology can achieve the best results in this regard.

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List of Configuration Parameters

The following list contains the parameters used to plot the respective figures and the components used in the measurements.

$\text{Config}_{2.1a}$ Simulation: $V_{in} = 420\,\text{V}$, $V_{out} = 10\,\text{V}$, $I_{out} = 160\,\text{A}$, $\lambda = 0.3$, $Z = 19.3\,\Omega$, $n = 15$, $f/f_r = 2$, $D = 0.35$

$\text{Config}_{2.1b}$ Experiment: $V_{in} = 310\,\text{V}$, $V_{out} = 14\,\text{V}$, $I_{out} = 110\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 80\,\text{nF}$, $n = 15$, $f = 124.8\,\text{kHz}$, $D = 0.76$, MOSFETs: SCT3120AW7

$\text{Config}_{2.1c}$ Experiment: $V_{in} = 310\,\text{V}$, $V_{out} = 14\,\text{V}$, $I_{out} = 110\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 80\,\text{nF}$, $n = 15$, $f = 133\,\text{kHz}$, $D = 1$, MOSFETs: SCT3120AW7

$\text{Config}_{2.1d}$ Experiment: $V_{in} = 200\,\text{V}$, $V_{out} = 4\,\text{V}$, $I_{out} = 10\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 80\,\text{nF}$, $n = 15$, $f = 151\,\text{kHz}$, $D = 0.236$, MOSFETs: SCT3120AW7

$\text{Config}_{2.1e}$ Experiment: $V_{in} = 350\,\text{V}$, $V_{out} = 11\,\text{V}$, $I_{out} = 130\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 80\,\text{nF}$, $n = 15$, MOSFETs: SCT3120AW7

$\text{Config}_{2.1f}$ Experiment: $V_{in} = 420\,\text{V}$, $V_{out} = 5\,\text{V}$, $I_{out} = 80\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 80\,\text{nF}$, $n = 15$, MOSFETs: SCT3120AW7

$\text{Config}_{2.1g}$ Experiment: $V_{in} = 360\,\text{V}$, $V_{out} = 8\,\text{V}$, $I_{out} = 30\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 80\,\text{nF}$, $n = 15$, $f = 170\,\text{kHz}$, MOSFETs: SCT3120AW7

$\text{Config}_{2.1h}$ Simulation: $\lambda = 0.33$, $Z = 18.26$, $n = 15$, $V_{in} = 420\,\text{V}$, $V_{out} = 8\,\text{V}$, $I_{out} = 130\,\text{A}$

$\text{Config}_{2.1i}$ Simulation: $\lambda = 0.166$, $Z = 10.1$, $n = 15$, $V_{in} = 420\,\text{V}$, $V_{out} = 13\,\text{V}$, $I_{out} = 20\,\text{A}$

$\text{Config}_{2.1j}$ Experiment: $V_{in} = 350\,\text{V}$, $V_{out} = 9\,\text{V}$, $I_{out} = 120\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 80\,\text{nF}$, $n = 15$, $f = 104\,\text{kHz}$, $D = 0.4$, MOSFETs: SCT3120AW7

$\text{Config}_{2.1k}$ Experiment: $V_{in} = 420\,\text{V}$, $V_{out} = 4\,\text{V}$, $I_{out} = 80\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 80\,\text{nF}$, $n = 15$, $f = 170\,\text{kHz}$, $D = 0.3$, MOSFETs: SCT3120AW7

$\text{Config}_{2.1l}$ Experiment: $V_{in} = 350\,\text{V}$, $V_{out} = 9\,\text{V}$, $I_{out} = 130\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 90\,\text{nF}$, $n = 15$

$\text{Config}_{2.1m}$ Simulation: $V_{in} = 350\,\text{V}$, $V_{out} = 9\,\text{V}$, $I_{out} = 130\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 90\,\text{nF}$, $n = 15$, MOSFETs: SCT3120AW7

$\text{Config}_{2.1n}$ Simulation: $V_{in} = 350\,\text{V}$, $V_{out} = 9\,\text{V}$, $I_{out} = 130\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m \in \{100\,\mu\text{H}, 270\,\mu\text{H}\}$, $C_r = 90\,\text{nF}$, $n = 14.7$

$\text{Config}_{2.1o}$ Simulation: $V_{in} = 350\,\text{V}$, $V_{out} = 9\,\text{V}$, $I_{out} = 130\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 160\,\mu\text{H}$, $C_r = 90\,\text{nF}$, $n = 14.7$

$\text{Config}_{2.1p}$ Simulation: $V_{in} = 350\,\text{V}$, $V_{out} = 9\,\text{V}$, $I_{out} = 130\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m \in \{100\,\mu\text{H}, 160\,\mu\text{H}, 270\,\mu\text{H}\}$, $C_r = 90\,\text{nF}$, $n = 14.7$

$\text{Config}_{2.1q}$ Simulation: $V_{in} = 350\,\text{V}$, $V_{out} = 9\,\text{V}$, $I_{out} = 130\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m \in \{100\,\mu\text{H}, 270\,\mu\text{H}\}$, $C_r = 90\,\text{nF}$, $n = 14.7$

$\text{Config}_{2.1r}$ Simulation: $V_{in} = 350\,\text{V}$, $V_{out} = 9\,\text{V}$, $I_{out} = 130\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 160\,\mu\text{H}$, $C_r = 90\,\text{nF}$, $n = 14.7$

$\text{Config}_{2.1s}$ Simulation: $V_{in} = 290\,\text{V}$, $V_{out} = 7.5\,\text{V}$, $I_{out} = 130\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 270\,\mu\text{H}$, $C_r = 90\,\text{nF}$, $n = 14.7$

$\text{Config}_{2.1t}$ $\lambda = 0.33$, $Z = 18.26$, $n = 15$, $f_r = 100\,\text{kHz}$.

$\text{Config}_{2.1u}$ Simulation: $V_{in} = 220\,\text{V}$, $V_{out} = 16\,\text{V}$, $I_{out} = 250\,\text{A}$, $\lambda = 0.3$, $Z = 19.3\,\Omega$, $n = 15$, $f_1/f_r = 0.842$, $f_2/f_r = 0.883$, $p_{Lr} = 2.5\,\%$, $p_{Cr} = 2.5\,\%$, $p_{Lm} = 0$

$\text{Config}_{2.1v}$ Simulation: $V_{in} = 320\,\text{V}$, $V_{out} = 16\,\text{V}$, $I_{out} = 250\,\text{A}$, $L_r = 30\,\mu\text{H}$, $L_m = 90\,\mu\text{H}$, $C_r = 90\,\text{nF}$, $n = 15$

$\text{Config}_{2.1w}$ Simulation: $V_{in} = 420\,\text{V}$, $V_{out} = 11\,\text{V}$, $I_{out} = 250\,\text{A}$, $L_r = 30\,\mu\text{H}$, $L_m = 90\,\mu\text{H}$, $C_r = 90\,\text{nF}$, $n = 15$

$\text{Config}_{2.1x}$ Simulation: $\lambda = 0.3$, $Z = 19.3\,\Omega$, $n = 15$, $p_{Lr} = 5\,\%$, $p_{Cr} = 1\,\%$, $p_{Lm} = 5\,\%$

$\text{Config}_{2.1y}$ Experiment: $V_{in} = 420\,\text{V}$, $V_{out} = 14\,\text{V}$, $I_{out} = 260\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 80\,\text{nF}$, $n = 15$.

$\text{Config}_{2.1z}$ Experiment: $V_{in} = 420\,\text{V}$, $V_{out} = 10\,\text{V}$, $I_{out} = 260\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 80\,\text{nF}$, $n = 15$.

$\text{Config}_{2.1aa}$ Simulation: $V_{in} = 420\,\text{V}$, $V_{out} = 12\,\text{V}$, $I_{out} = 260\,\text{A}$, $L_r = 30\,\mu\text{H}$, $L_m = 90\,\mu\text{H}$, $C_r = 90\,\text{nF}$, $n = 15$.

$\text{Config}_{2.1ab}$ Experiment: $V_{in} = 360\,\text{V}$, $V_{out} = 9\,\text{V}$, $I_{out} = 200\,\text{A}$, $L_r = 29.8\,\mu\text{H}$, $L_m = 88\,\mu\text{H}$, $C_r = 80\,\text{nF}$, $n = 15$.

$\text{Config}_{2.1ac}$ Simulation: $V_{in} = 240\,\text{V}$, $V_{out} = 16\,\text{V}$, $I_{out} = 130\,\text{A}$, $L_r = 40\,\mu\text{H}$, $L_m = 140\,\mu\text{H}$, $C_r = 120\,\text{nF}$, $n \in \{14, 15, 16, 17, 18\}$.

$\text{Config}_{2.1ad}$ Simulation: $V_{in} = 420\,V$, $V_{out} = 14\,V$, $I_{out} = 130\,A$, $L_r = 40\,\mu H$, $L_m = 140\,\mu H$, $C_r = 120\,nF$, $n = 14$.

$\text{Config}_{2.1ae}$ Simulation: $V_{in} = 240\,V$, $V_{out} = 16\,V$, $I_{out} = 130\,A$, $L_r = 40\,\mu H$, $L_m = 140\,\mu H$, $C_r = 120\,nF$, $n = 14$.

$\text{Config}_{2.1af}$ Experiment: L_r(integ.)$= 38\,\mu H$, L_m(integ.)$= 128\,\mu H$, $n = 14.6$, $C_r = 140\,nF$, $V_{in} = 240\,V$, $V_{out} = 14\,V$, $I_{out} = 130\,A$, $f = 77.3\,kHz$.

$\text{Config}_{2.2a}$ Simulation: $V_{in} = 420V$, $V_{out} = 14\,V$, $I_{out} = 130\,A$, $L_s = 10\,\mu H$, $L_m = 200\,\mu H$, $L_g = 700\,nH$, $n = 8$, $C_s = 300\,nF$.

$\text{Config}_{2.2b}$ Simulation: $V_{in} = 420V$, $V_{out} = 14\,V$, $I_{out} = [15\,A, 160\,A]$, $L_s = 10\,\mu H$, $L_m = 200\,\mu H$, $L_g = 700\,nH$, $n = 8$, $C_s = 300\,nF$.

$\text{Config}_{2.2c}$ Experiment: $V_{in} = 290V$, $V_{out} = 14\,V$, $L_s = 1.46\,\mu H$, $L_m = 41.8\,\mu H$, $L_g = 700\,nH$, $n = 6.8$, $C_s = 300\,nF$.

$\text{Config}_{2.2d}$ Experiment: $V_{in} = 240\,V$, $V_{out} = 14\,V$, $I_{out} = 130\,A$, $L_s = 1.46\,\mu H$, $L_m = 41.8\,\mu H$, $L_g = 700\,nH$, $n = 6.8$, $C_s = 300\,nF$.

$\text{Config}_{2.2e}$ Experiment: $V_{in} = 420V$, $V_{out} = 8\,V$, $I_{out} = 130\,A$, $L_s = 1.46\,\mu H$, $L_m = 41.8\,\mu H$, $L_g = 700\,nH$, $n = 6.8$, $C_s = 300\,nF$.

$\text{Config}_{2.2f}$ Simulation: $V_{in} = 420V$, $V_{out} = 14\,V$, $I_{out} = 10\,A$, $L_s = 10\,\mu H$, $L_m = 200\,\mu H$, $L_g = 700\,nH$, $n = 8$, $C_s = 300\,nF$.

$\text{Config}_{2.2g}$ Experiment: $V_{in} = 290V$, $V_{out} = 14\,V$, $L_s = 1.46\,\mu H$, $L_m = 41.8\,\mu H$, $L_g = 700\,nH$, $n = 6.8$, $C_s = 300\,nF$.

$\text{Config}_{2.2h}$ Experiment: $V_{in} = 240V$, $V_{out} = 14\,V$, $I_{out} = 30.3\,A$, $L_s = 1.46\,\mu H$, $L_m = 41.8\,\mu H$, $L_g = 700\,nH$, $n = 6.8$, $C_s = 300\,nF$.

$\text{Config}_{2.2i}$ Experiment: $V_{in} = 290V$, $V_{out} = 14\,V$, $I_{out} = 10.5\,A$, $L_s = 1.46\,\mu H$, $L_m = 41.8\,\mu H$, $L_g = 700\,nH$, $n = 6.8$, $C_s = 300\,nF$.

$\text{Config}_{2.2j}$ Simulation: $V_{in} = 340V$, $V_{out} = 12\,V$, $I_{out} = 160\,A$, $L_s = 2\,\mu H$, $L_m = 60\,\mu H$, $L_g = 100\,nH$, $n = 14$, $f_{sw} = 750\,kHz$

$\text{Config}_{2.2k}$ Simulation: $V_{in} = 200V$, $V_{out} = 16\,V$, $I_{out} = 160\,A$, $L_s = 2\,\mu H$, $L_m = 80\,\mu H$, $L_g = 70\,nH$, $n = 14$, $f_{sw} = 750\,kHz$

$\text{Config}_{2.2l}$ Simulation: $V_{in} = 200V$, $V_{out} = 16\,V$, $I_{out} = \{20, 60, 100, 140, 180, 220, 260\}\,A$, $L_s = 2\,\mu H$, $L_m = 60\,\mu H$, $L_g = 700\,nH$, $n = 14$, $C_{cl} = 400\,nF$, $C_{out,prim} = 0.1\,nF$, $C_{out,sec} = 10\,nF$.

$\text{Config}_{2.2m}$ Simulation: $V_{in} = 420\text{V}$, $V_{out} = 8\,\text{V}$, $I_{out} \in \{20\,\text{A}, 60\,\text{A}, 100\,\text{A}, 140\,\text{A}, 180\,\text{A}, 220\,\text{A}, 260\,\text{A}\}$, $L_s = 2\,\mu\text{H}$, $L_m = 60\,\mu\text{H}$, $L_g = 700\,\text{nH}$, $n = 14$, $C_{cl} = 400\,\text{nF}$, $C_{out,prim} = 0.1\,\text{nF}$, $C_{out,sec} = 10\,\text{nF}$.

$\text{Config}_{2.2n}$ Simulation: $V_{in} = 200\text{V}$, $V_{out} = 16\,\text{V}$, $I_{out} = 260\,\text{A}$, $L_s = 2\,\mu\text{H}$, $L_m = 60\,\mu\text{H}$, $L_g = 700\,\text{nH}$, $n = 14$, $C_{cl} = 400\,\text{nF}$, $C_{out,prim} = 0.1\,\text{nF}$, $C_{out,sec} = 10\,\text{nF}$.

$\text{Config}_{2.2o}$ Simulation: $V_{in} = 420\text{V}$, $V_{out} = 8\,\text{V}$, $I_{out} = 260\,\text{A}$, $L_s = 2\,\mu\text{H}$, $L_m = 60\,\mu\text{H}$, $L_g = 700\,\text{nH}$, $n = 14$, $C_{cl} = 400\,\text{nF}$, $C_{out,prim} = 0.1\,\text{nF}$, $C_{out,sec} = 10\,\text{nF}$.

$\text{Config}_{2.2p}$ Simulation: $V_{in} = 420\text{V}$, $V_{out} = 14\,\text{V}$, $I_{out} = 10\,\text{A}$, $L_s = 2\,\mu\text{H}$, $L_m = 80\,\mu\text{H}$, $L_g = 1.5\,\mu\text{H}$, $n = 7$, $f_{sw} = 250\,\text{kHz}$. Main switch: C3M0065090J, auxiliary switch: C3M0120090J, SR rectifier: 2 $\times$ parallel IAUT300N10S5N015.

$\text{Config}_{2.2q}$ Simulation: $V_{in} = 420\text{V}$, $V_{out} = 14\,\text{V}$, $I_{out} = 130\,\text{A}$, $L_s = 2\,\mu\text{H}$, $L_m = 80\,\mu\text{H}$, $L_g = 1.5\,\mu\text{H}$, $n = 7$, $f_{sw} = 250\,\text{kHz}$.

$\text{Config}_{2.2r}$ Simulation: $V_{in} = 420\text{V}$, $V_{out} = 14\,\text{V}$, $I_{out} = 35\,\text{A}$, $L_s = 2\,\mu\text{H}$, $L_m = 80\,\mu\text{H}$, $L_g = 1.5\,\mu\text{H}$, $n = 7$, $f_{sw} = 250\,\text{kHz}$.

$\text{Config}_{2.2s}$ Simulation: $V_{in} = 420\text{V}$, $V_{out} = 14\,\text{V}$, $I_{out} = 25\,\text{A}$, $L_s = 2\,\mu\text{H}$, $L_m = 80\,\mu\text{H}$, $L_g = 1.5\,\mu\text{H}$, $n = 7$, $f_{sw} = 250\,\text{kHz}$.

$\text{Config}_{2.2t}$ Simulation: $V_{in} = 420\text{V}$, $V_{out} = 14\,\text{V}$, $I_{out} = 10\,\text{A}$, $L_s = 2\,\mu\text{H}$, $L_m = 80\,\mu\text{H}$, $L_g = 1.5\,\mu\text{H}$, $n = 7$, $f_{sw} = 250\,\text{kHz}$.

$\text{Config}_{2.2u}$ Simulation: S_1: C3M0065090J, S_2: C3M0120090J, SR_1: IAUT300N10S5N015, SR_2: IAUT300N10S5N015.

$\text{Config}_{2.2v}$ Experiment: $V_{in} = 220\,\text{V}$, $V_{out} = 16\,\text{V}$, $I_{out} = 65\,\text{A}$, $L_s = 1.46\,\mu\text{H}$, $L_m = 41.8\,\mu\text{H}$, $L_g = 700\,\text{nH}$, $n = 6.8$. Snubber inactive.

$\text{Config}_{2.2w}$ Simulation: $V_{in} = 200\,\text{V}$, $V_{out} = 16\,\text{V}$, $I_{out} = 100\,\text{A}$, $L_s = 2\,\mu\text{H}$, $L_m = 150\,\mu\text{H}$, $L_g = 1.5\,\mu\text{H}$, $n = 7.5$.

$\text{Config}_{2.2x}$ Experiment: $V_{in} = 220\,\text{V}$, $V_{out} = 16\,\text{V}$, $I_{out} = 65\,\text{A}$, $L_s = 1.46\,\mu\text{H}$, $L_m = 41.8\,\mu\text{H}$, $L_g = 700\,\text{nH}$, $n = 6.8$. Snubber active.

$\text{Config}_{2.2y}$ Experiment: $V_{in} = 420\,\text{V}$, $V_{out} = 7.5\,\text{V}$, $I_{out} = 160\,\text{A}$, $L_s = 1.46\,\mu\text{H}$, $L_m = 41.8\,\mu\text{H}$, $L_g = 700\,\text{nH}$, $n = 6.8$. Snubber active.

$\text{Config}_{2.2z}$ Simulation: $V_{in} = 200\,\text{V}$, $V_{out} = 16\,\text{V}$, $I_{out} = 100\,\text{A}$, $L_s = 7\,\mu\text{H}$, $L_m = 150\,\mu\text{H}$, $L_g = 1.5\,\mu\text{H}$, $n = 7.5$

$\text{Config}_{2.3a}$ Experiment: $V_{\text{in}} = 240\text{V}$, $V_{\text{out}} = 14\,\text{V}$, $I_{\text{out}} = 100\,\text{A}$, $L_{\text{s}} = 1\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 700\,\text{nH}$, $n = 10$.

$\text{Config}_{2.3b}$ Experiment: $V_{\text{in}} = 240\text{V}$, $V_{\text{out}} = 14\,\text{V}$, $I_{\text{out}} = 100\,\text{A}$, $L_{\text{s}} = 7.5\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 700\,\text{nH}$, $n = 10$.

$\text{Config}_{2.3c}$ Experiment: $V_{\text{in}} = 250\text{V}$, $V_{\text{out}} = 8\,\text{V}$, $I_{\text{out}} = 110\,\text{A}$, $L_{\text{s}} = 1\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 700\,\text{nH}$, $n = 10$.

$\text{Config}_{2.3d}$ Simulation: $V_{\text{in}} = 240\text{V}$, $V_{\text{out}} = 12\,\text{V}$, $I_{\text{out}} = 130\,\text{A}$, $L_{\text{s}} = 15\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 500\,\text{nH}$, $n = 10$.

$\text{Config}_{2.4e}$ Simulation: $V_{\text{in}} = 240\text{V}$, $V_{\text{out}} = 12\,\text{V}$, $I_{\text{out}} = 30\,\text{A}$, $L_{\text{s}} = 15\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 500\,\text{nH}$, $n = 10$, $f_{\text{sw}} = 75.5\,\text{kHz}$.

$\text{Config}_{2.3f}$ Simulation: $V_{\text{in}} = 240\text{V}$, $V_{\text{out}} = 12\,\text{V}$, $I_{\text{out}} = 8\,\text{A}$, $L_{\text{s}} = 15\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 500\,\text{nH}$, $n = 10$, $f_{\text{sw}} = 75.5\,\text{kHz}$.

$\text{Config}_{2.3g}$ Experiment: $V_{\text{in}} = 240\text{V}$, $V_{\text{out}} = 12\,\text{V}$, $I_{\text{out}} = 6\,\text{A}$, $L_{\text{s}} = 1\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 500\,\text{nH}$, $n = 10$, $f_{\text{sw}} = 75.5\,\text{kHz}$.

$\text{Config}_{2.3h}$ Experiment: $V_{\text{in}} = 240\text{V}$, $V_{\text{out}} = 12\,\text{V}$, $I_{\text{out}} = 30\,\text{A}$, $L_{\text{s}} = 1\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 500\,\text{nH}$, $n = 10$.

$\text{Config}_{2.3i}$ Experiment: $V_{\text{in}} = 240\text{V}$, $V_{\text{out}} = 12\,\text{V}$, $I_{\text{out}} = 100\,\text{A}$, $L_{\text{s}} = 1\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 500\,\text{nH}$, $n = 10$.

$\text{Config}_{2.3j}$ Simulation: $V_{\text{in}} = 280\text{V}$, $V_{\text{out}} = 9\,\text{V}$, $I_{\text{out}} = 100\,\text{A}$, $L_{\text{s}} = 7.5\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 700\,\text{nH}$, $n = 10$.

$\text{Config}_{2.3k}$ Experiment: $V_{\text{in}} = 280\text{V}$, $V_{\text{out}} = 9\,\text{V}$, $I_{\text{out}} = 100\,\text{A}$, $L_{\text{s}} = 7.5\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 700\,\text{nH}$, $n = 10$.

$\text{Config}_{2.3l}$ Simulation: $L_{\text{s}} = 2.6\,\mu\text{H}$, $L_{\text{m}} = 150\,\mu\text{H}$, $L_{\text{g}} = 700\,\text{nH}$, $n = 10$.

$\text{Config}_{2.3m}$ Simulation: $L_{\text{s}} = 4\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 700\,\text{nH}$, $n = 10$.

$\text{Config}_{2.4a}$ Simulation: $V_{\text{in}} = 420\text{V}$, $V_{\text{out}} = 16\,\text{V}$, $I_{\text{out}} = 130\,\text{A}$, $L_{\text{s}} = 3\,\mu\text{H}$, $L_{\text{m}} = 200\,\mu\text{H}$, $L_{\text{g}} = 1\,\mu\text{H}$, $n = 10$.

$\text{Config}_{2.4b}$ Simulation: $V_{\text{in}} = 420\text{V}$, $V_{\text{out}} = 8\,\text{V}$, $I_{\text{out}} = 260\,\text{A}$, $L_{\text{s}} = 3\,\mu\text{H}$, $L_{\text{m}} = 45\,\mu\text{H}$, $L_{\text{g}} = 300\,\text{nH}$, $n = 7$.

$\text{Config}_{2.4c}$ Simulation: $V_{\text{in}} = 240\text{V}$, $V_{\text{out}} = 16\,\text{V}$, $I_{\text{out}} = 65\,\text{A}$, $L_{\text{s}} = 3\,\mu\text{H}$, $L_{\text{m}} = 45\,\mu\text{H}$, $L_{\text{g}} = 300\,\text{nH}$, $n = 7$.

$\text{Config}_{2.4d}$ Simulation: $V_{\text{in}} = 420\text{V}$, $V_{\text{out}} = 8\,\text{V}$, $I_{\text{out}} = 65\,\text{A}$, $L_{\text{s}} = 3\,\mu\text{H}$, $L_{\text{m}} = 45\,\mu\text{H}$, $L_{\text{g}} = 300\,\text{nH}$, $n = 7$.

List of Abbreviations

3L	3-level
a²Morph	alternating asymmetrical on-the-fly topology morphing transition
a²PSM	alternating asymmetrical phase-shift modulation
ACFC	active-clamp forward converter
ADC	analogue-digital converter
aPSM	asymmetrical phase-shift modulation
aFDM	asymmetrical frequency-doubler modulation
aHBM	asymmetrical half-bridge modulation
AlN	aluminium nitride
aPSM	asymmetrical phase-shift modulation
aPWM	asymmetrical pulse-width modulation
CCM	continuous conduction mode
ciACFC	common-interleaved ACFC
CLF	component load factor
CM	common mode
DAB	dual-active bridge
DCM	discontinuous conduction mode
DM	differential mode
DSP	digital signal processor
ECD	electrical circuit diagram
eiACFC	extended-interleaved ACFC
EMI	electromagnetic interference
FBM	conventional full-bridge modulation
FBS	full-bridge schematic
FC	flying capacitor
FD-HBM	frequency-doubler half-bridge modulation

FEM	finite-element method
FHA	fundamental-harmonic approximation
FOM	figure of merit
GaN	gallium-nitride
HBM	half-bridge modulation
HBM	half-bridge modulation
HFBM	hard-switched full-bridge modulation
HSFDM	hard-switched frequency-doubler modulation
HHBM	hard-switched half-bridge modulation
HSFB	hard-switched full-bridge converter
IC	integrated circuit
ICE	internal combustion engine
iZVS	incomplete zero-voltage switching
LLC	LLC resonant converter
LUT	look-up table
MOSFET	metal–oxide–semiconductor field-effect transistor
PCB	printed circuit board
PE	protective earth
PFC	power-factor correction stage
PSFB	phase-shifted full bridge converter
PSM	phase-shift modulation
PWM	pulse-width modulation
RMS	root mean square
Si	silicon
SiC	silicon-carbide
SMD	surface-mounted device
SPI	serial peripheral interface
SR	synchronous rectifier
TIM	thermal-interface material
TVS	transient voltage suppressor
VTR	voltage-transfer ratio
ZCS	zero-current switching
ZVS	zero-voltage switching

List of Symbols

A^-		transition from ET^+ through FW^- to ET^-
A	m^2	surface area
A^+		transition from ET^+ through FW^+ to ET^-
A_c	m^2	core cross section
B^-		transition from ET^- through FW^- to ET^+
b	T	magnetic flux density
B^+		transition from ET^- through FW^+ to ET^+
b_{fring}	T	magnetic flux density of the fringing field at the glue spot of a magnetic component
C_{cl}	F	clamp capacitance
C_{fc}	F	flying capacitance
C_{out}	F	output capacitance of a semiconductor
D		duty cycle
D_{asym}		duty cycle in asymmetrical mode of the LLC
d_{inv}		positive inverter voltage duty cycle during morphing
d_m		negative inverter voltage duty cycle during morphing
d_{PS}		equivalent duty cycle in phase-shift modulation
E	W	energy
E_{iZVS}	W	incomplete ZVS losses if a MOSFET is turned on at a residual voltage
ϵ	V	EMI emission (CM and DM)
ET^-		switch state of a full-bridge inverter with switches S_2 and S_3 turned on resulting in an inverter voltage of $v_{AB} \approx -V_{in}$
ET^+		switch state of a full-bridge inverter with switches S_1 and S_4 turned on resulting in an inverter voltage of $v_{AB} \approx V_{in}$
f_{sw}	Hz	switching frequency

f_{res}	Hz	resonant frequency
FW^-		switch state of a full-bridge inverter with switches S_3 and S_4 turned on resulting in an inverter voltage of $v_{\text{AB}} \approx 0\,\text{V}$
FW^+		switch state of a full-bridge inverter with switches S_1 and S_2 turned on resulting in an inverter voltage of $v_{\text{AB}} \approx 0\,\text{V}$
G		converter gain
γ		ratio of the inductances of L_{g} and L_{m}
i_{aux}	A	auxiliary (clamping) current of the HSFB to limit the synchronous rectifier voltage during morphing
i_{buck}	A	buck converter current acting as the snubber of the ACFC
i_{cl}	A	clamp capacitor current of the ACFC
i_{Cout}	A	output capacitor current
i_{DS}	A	drain-source current of a MOSFET
i_{fc}	A	flying capacitor current
i_{in}	A	input current of the converter
i_{in}	A	mean input current of the converter
i_{Lg}	A	output inductor current of L_{g}
i_{Ls}	A	current of the series inductance L_{s}
i'_{Ls}	A	transformed dynamic series inductance current on the secondary side
i_{mag}	A	current of the magnetizing inductance L_{m}
$i_{\text{mag}}^{\text{int,in}}$	A	quasi magnetizing current in an integrated transformer
$\hat{i}_{\text{mag,m}}$	A	maximum magnetizing current during morphing
$\hat{i}_{\text{mag,HB}}$	A	maximum magnetizing current during half-bridge mode
i_{P1}	A	first characteristic current level in phase-shift operation
i_{P2}	A	second characteristic current level in phase-shift operation
i_{P3}	A	third characteristic current level in phase-shift operation
i_{prim}	A	primary current of isolated full-bridge converter

$\bar{i}^{\mathrm{m}}_{\mathrm{prim}}$	A	average primary transformer current of the HSFB during morphing
i_{res}	A	resonant current L_{r}
i'_{sec}	A	transformed secondary transformer current
i'_{sn1}	A	snubber current of the snubber attached to the synchronous rectifier SR_1
$i_{\mathrm{sr}i}$	A	current of the synchronous rectifier i
i_{sw}	A	switch current
i_{to}	A	primary turn-off current of the inverter switches
k		Fourier coefficient
$\tilde{k}$		fourier coefficient to compare equal frequency components for different switching frequencies (*see* (2.18))
$\boldsymbol{L}$	H	inductance matrix
L_{11}	H	primary self inductance of a transformer
L_{22}	H	secondary self inductance of a transformer
λ		ratio of the resonant inductance and magnetizing inductance of the LLC converter
L_{con}	H	inductance of the transformer connection
L_{g}	H	output inductance of the PSFB, HSFB or ACFC
L_{m}	H	magnetizing inductance
$L_{\mathrm{m}}^{\mathrm{Ls}'}$	H	magnetizing inductance of the transformer with the series inductance transformed to the secondary side
L_{r}	H	resonant inductance of the LLC
L_{s}	H	series inductance of the PSFB, HSFB or ACFC
L_{σ}	H	stray inductance of the auxiliary winding of the HSFB
M_{12}	H	mutual inductance of a transformer
$\boldsymbol{N}$		turns matrix
n		conversion ratio of a transformer
n_1		conversion ratio of a center-tapped transformer from the primary winding to the first secondary winding
N_1		primary turns number

n_2		conversion ratio of a center-tapped transformer from the primary winding to the second secondary winding
N_2		secondary turns number
N_{aux}		auxiliary turns number to clamp the secondary synchronous rectifier voltage
$n^{\text{Ls}'}$		conversion ratio of the transformer with the series inductance transformed to the secondary side
N_p		primary turns number of the HSFB
$N_{\text{reg,FB}}$		maximum counter value of a PWM unit during full-bridge mode
$N_{\text{reg,HB}}$		maximum counter value of a PWM unit during half-bridge mode
$N_{\text{reg,m}}$		maximum counter value of a PWM unit during morphing
N_{reg}		maximum counter value of a PWM unit
N_s		secondary turns number of the HSFB
$P_{\text{high}}^{\text{FD-HBM}}$	W	losses of the switches in frequency-doubler mode that are turned on for 75 %
$P_{\text{low}}^{\text{FD-HBM}}$	W	losses of the switches in frequency-doubler mode that are turned on for 25 %
$\hat{p}_{\text{fring,m}}$		ratio of the maximum fringing flux during morphing and in half-bridge mode (*see* (2.36))
$\hat{p}_{\text{fring,m}}$		ratio of the minimum fringing flux during morphing and in half-bridge mode (*see* (2.36))
$P_{\text{inv}}^{\text{HBM}}$	W	losses of the complementary switched MOSFETs in half-bridge mode
$P_{\text{p-on}}^{\text{HBM}}$	W	losses of the permanently turned-on switch in half-bridge mode
$P_{\text{high}}^{\text{HFDM}}$	W	losses of the switches in frequency-doubler mode that are turned on for $(2+D)T/2$
$P_{\text{low}}^{\text{HFDM}}$	W	losses of the switches in frequency-doubler mode that are turned on for $DT/2$
$P_{\text{p-on}}^{\text{HHBM}}$	W	losses of the permanently turned-on switch in half-bridge mode of the HHBM
$P_{\text{pulse}}^{\text{HHBM}}$	W	losses of the switched MOSFETs in half-bridge mode of the HHBM
ϕ_{conv}	Wb	flux in a conventional transformer

ϕ_{in}	Wb	flux in the center leg of an integrated transformer
ϕ_{out}	Wb	flux in the return legs of an integrated transformer
ϕ_{stray}	Wb	flux in the stray leg of an integrated transformer
P_{inv}	W	inverter losses
$\hat{p}_{\text{mag,m}}$		ratio of the minimum magnetizing current during morphing and in half-bridge mode (*see* (2.27))
$\check{p}_{\text{mag,m}}$		ratio of the minimum magnetizing current during morphing and in half-bridge mode (*see* (2.28))
P_{MOSFET}	W	MOSFET losses
Q_{Cb}	C	charge of the blocking capacitor of the HSFB
Q_{com}	C	commutation charge
$\Delta Q_{\text{sn,SR1}}$	C	charge delivered to the snubber per period
R_0	Ω	output resistance
R_{AC}	Ω	output resistance in the fundamental harmonic approximation of an LLC circuit
$R_{\text{DS,Q1}}$	Ω	on-state resistance of a MOSFET in quadrant 1
$R_{\text{DS,Q3}}$	Ω	on-state resistance of a MOSFET in quadrant 3 (negative currents)
$\boldsymbol{R}_{\text{m}}$	$\frac{1}{\text{H}}$	reluctance matrix of an integrated transformer
R_{m1}	$\frac{1}{\text{H}}$	magnetic resistance of an integrated transformer in the center path
R_{m2}	$\frac{1}{\text{H}}$	magnetic resistance of an integrated transformer in the return path
R_{m3}	$\frac{1}{\text{H}}$	magnetic resistance of an integrated transformer in the stray path
$r_{\text{m},i,j}$	$\frac{1}{\text{H}}$	magnetic resistance of the reluctance matrix with the element i, j
R_σ	Ω	stray resistance of the auxiliary winding of the HSFB
R_{th}	$\frac{\text{K}}{\text{W}}$	thermal resistance
S_1		upper left switch of a full-bridge inverter
S_2		upper right switch of a full-bridge inverter
S_3		lower left switch of a full-bridge inverter
S_4		lower right switch of a full-bridge inverter
T	s	switching period

t_{clamp}	s	clamping time
$\vartheta_{\text{a}^2\text{PSM,A},k}$		angle of the fourier coefficients k of the inverter voltage v_{A} in alternating-asymmetrical phase-shift modulation
$\vartheta_{\text{a}^2\text{PSM,B},k}$		angle of the fourier coefficients k of the inverter voltage v_{B} in alternating-asymmetrical phase-shift modulation
$\vartheta_{\text{a}^2\text{PSM},k}$		angle of the fourier coefficients k of the inverter in alternating-asymmetrical phase-shift modulation
ϑ_{j}	K	junction temperature
$\vartheta_{\text{PSM,A},k}$		angle of the fourier coefficients k of the inverter voltage v_{A} in phase-shift modulation
$\vartheta_{\text{PSM,B},k}$		angle of the fourier coefficients k of the inverter voltage v_{B} in phase-shift modulation
$\vartheta_{\text{PSM},k}$		angle of the fourier coefficients k of the inverter in phase-shift modulation
T_{mod}	s	modulation period
t_{morph}	s	morphing transition time
v_1	V	voltage of the main switch S_1 of the ACFC
v_2	V	voltage of the auxiliary switch S_2 of the ACFC
v_{A}	V	inverter voltage of the first half-bridge of a full-bridge inverter
$\hat{v}_{\text{a}^2\text{PSM,A},k}$	V	amplitude of the fourier coefficients k of the inverter voltage v_{A} in alternating-asymmetrical phase-shift modulation
$\hat{v}_{\text{a}^2\text{PSM,B},k}$	V	amplitude of the fourier coefficients k of the inverter voltage v_{B} in alternating-asymmetrical phase-shift modulation
$\hat{v}_{\text{a}^2\text{PSM},k}$	V	amplitude of the fourier coefficients k of the inverter in alternating-asymmetrical phase-shift modulation
v_{AB}	V	inverter voltage
v_{B}	V	inverter voltage of the second half-bridge of a full-bridge inverter
v_{b}	V	voltage of the auxiliary switch S_2 of the ACFC
V_{cl}	V	average clamp capacitor voltage
$V_{\text{cl,rev}}$	V	reverse voltage of the clamping diode of the HSFB
$V_{\text{cl,com}}$	V	clamp capacitor voltage of the ACFC calculated using the ordinary formula

v_{CM}	V	common-mode voltage
$\hat{v}_{\mathrm{com},4T(1),k}$	V	amplitude of the fourier coefficients of the collective common-mode source voltage in four-period alternating-asymmetrical phase-shift modulation with a $A^+ - B^+ - A^+ - B^+ - A^- - B^- - A^- - B^-$ sequence
$\hat{v}_{\mathrm{com},4T(2),k}$	V	amplitude of the fourier coefficients of the collective common-mode source voltage in four-period alternating-asymmetrical phase-shift modulation with a $A^+ - B^- - A^+ - B^- - A^- - B^+ - A^- - B^+$ sequence
$\hat{v}_{\mathrm{com,PSM},k}$	V	amplitude of the fourier coefficients of the collective common-mode source voltage in two-period alternating-asymmetrical phase-shift modulation
$\hat{v}_{\mathrm{com,PSM},k}$	V	amplitude of the fourier coefficients of the collective common-mode source voltage in phase-shift modulation
$v_{\mathrm{GS,S3}}$	V	gate-source voltage of switch S_3
$v_{\mathrm{GS,S4}}$	V	gate-source voltage of switch S_4
v_{GS}	V	gate-source voltage of a MOSFET
V_{in}	V	input voltage of the converter
v_{Lg}	V	voltage of the output inductor L_{g}
v_{Lm}	V	voltage of the magnetizing inductance L_{m}
v_{Ls}	V	voltage of the series inductor L_{s} of the ACFC, HSFB, and PSFB
V_{out}	V	output voltage of the converter
v_{prim}	V	primary transformer voltage
$v_{\mathrm{clamp}}^{\mathrm{prim}}$	V	primary clamping voltage of the HSFB
$\hat{v}_{\mathrm{PSM,A},k}$	V	amplitude of the fourier coefficients k of the inverter voltage v_{A} in phase-shift modulation
$\hat{v}_{\mathrm{PSM,B},k}$	V	amplitude of the fourier coefficients k of the inverter voltage v_{B} in phase-shift modulation
$\hat{v}_{\mathrm{PSM},k}$	V	amplitude of the fourier coefficients k of the inverter in phase-shift modulation
v_{res}	V	resonant capacitor voltage
v_{rev}	V	reverse voltage the primary switches of the ACFC
$v_{\mathrm{rev,SR1}}$	V	dynamic reverse voltage of the forward synchronous rectifier SR_1

$v_{\text{rev,SR2}}$	V	dynamic reverse voltage of the freewheeling synchronous rectifier SR_2
v_{S23}	V	gate-source voltage of the switch S_{23} in an interleaved LLC
v_{S24}	V	gate-source voltage of the switch S_{24} in an interleaved LLC
$v_{\text{clamp}}^{\text{sec}}$	V	secondary clamping voltage of the HSFB
v_{SR1}	V	stationary synchronous rectifier voltage of SR_1
v_{SR2}	V	stationary synchronous rectifier voltage of SR_2
Z	Ω	key impedance of the LLC
ζ	Ω	normalized frequency-independent measure of the magnetizing inductance

Curriculum Vitae

Personal Data

Name	Philipp Rehlaender
Address	Hohenbrunner Weg 8, 82024 Taufkirchen
Birthday	August 23, 1992 in Velbert
Nationality	German

Education

08/2003 – 05/2012	Gynmnasium Theodorianum
10/2012 – 02/2016	Bachelor of Engineering, *Elektrotechnik* South-Westphalia University of Applied Sciences
03/2016 – 08/2017	Master of Science, *Systems Engineering and Engineering Management* South-Westphalia University of Applied Sciences
since 10/2017	PhD thesis in *Electrical Engineering* Paderborn University

Professional Experience

07/2012 – 02/2016	Cooperative Study Program Delta Energy Systems (Germany) GmbH
03/2016 – 09/2017	Electrical Engineer South-Westphalia University of Applied Sciences
10/2017 – 12/2022	Scientific Employee Paderborn University, *Power Electronics and Electrical Drives*
since 01/2023	Application Engineer ON Semiconductor Germany GmbH