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DEVELOPMENT OF A NOVEL SIMPLE-TO-IMPLEMENT DIGITAL CURRENT OBSERVER FOR DC-DC CONVERTERS AND PFC RECTIFIERS

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DECLARATION

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Paderborn, 2025

Mohsin Ejaz Ahmad

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ABSTRACT

In modern switched-mode power supplies, measuring voltage and current is essential for stable operation. These setups are responsible for the control, regulation, and the protection of the power supply. The voltage measurement is simple to implement with high impedance circuits such as a voltage divider or an error amplifier and it does not depend on the characteristics of the power supply. However, measuring the current with physical sensors depends on various parameters of the power electronic circuit, including current rating, switching frequency, and efficiency. Therefore, in developing a power supply, current measurement is a crucial topic as it affects the size and power density of the system.

Currently, there are various types of current sensors that can be divided based on their principle of operation. Moreover, an isolated and low-loss measurement of the inductor current in a half-bridge is possible with two current transformer sensors in series with each switching transistor. However, the presence of these sensors in the commutation leg increases the parasitic inductance of the path, affecting the switching characteristics of the transistors. This research introduces a new concept that reduces the negative influence of current measurement. It is based on the current observer concept in the digital domain and is implemented in a low-cost digital signal processor. This measurement scheme estimates the complete inductor current with one current transformer sensor in the half-bridge leg and auxiliary windings over the power inductor. Thus, this method reduces the inductive component from the commutation loop and improves the switching behavior of the switches. Furthermore, it also reduces the size and the cost of the overall system.

Further, this document presents the implementation of the digital current observer for the DC-DC boost converter and power factor correction rectifiers. The digital equations are documented for each topology and verified with the simulation models. Additionally, the physical measurements are performed with the self-developed prototype. The experimental setup has shown that an acceptable rel-

ative error of **1**.**2**% can be achieved with the digital current observer scheme, thus validating the proposed current measurement concept for the power electronic circuit.

Keywords: current sensors, current transformer sensor, digital current observer, time capture modules, auxiliary windings, current measurement circuit, half-bridge topologies, closed-loop control, boost converter, power fraction correction rectifiers, boost PFC, bridgeless boost HPFC, totem pole PFC, sample correction

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ACRONYMS

DC	direct current
AC	alternating current
SMPS	switched-mode power supply
ADC	analog to digital conversion
CT	current transformer
DSP	digital signal processor
RMS	root mean square
PFC	power factor correction
CCM	continuous conduction mode
DCM	discontinuous conduction mode
BCM	boundary conduction mode
AMR	anisotropic magneto-resistor
SiC	silicon carbide
GaN	gallium nitride
Si	silicon
PCB	printed circuit board
THT	through hole technology
SMD	surface-mounted device
4QC	4-quadrant converter
NPC	neutral point clamped
ESR	equivalent series resistance
PWM	pulse width modulation
TI	Texas Instruments
eCAP	enhanced capture
HRCAP	high-resolution input capture
eQEP	enhanced quadrature encoder pulse
GPIO	general purpose input output

TSCTR	time-stamp counter register
CEVT	capture event
HRPWM	high-resolution pulse width modulation
QDU	quadrature decoder unit
PCCU	position counter control unit
QCAP	quadrature capture unit
QCLK	quadrature clock
QDIR	quadrature direction
UPEVNT	unit position event
QCTMR	capture timer
QCPRD	capture period register
QPOSCNT	position counter
QPOSCMP	quadrature position compare
ISR	interrupt service routine
PFC	power factor correction
SPI	serial peripheral interface
RC	resistor capacitor
BLPFC	bridgeless power factor correction
EMI	electromagnetic interference
UART	universal asynchronous receiver / transmitter
SVM	space vector modulation
CMRR	common-mode rejection ratio

1 INTRODUCTION

In linear or switching power supplies, the precise acquisition of electrical current and voltage is required for the regulation and protection of the device. This is possible by implementing the voltage and current measurement setups at various positions in the power supply, such as after the input electromagnetic interference (EMI) filter, or before the output terminals, or with in the power stage.

In modern switching power supplies, the measurement setup is not only used for monitoring and protection from overcurrent or overvoltage but also for controlling the power supply. Therefore, for the purpose of digital or analog closed-loop control, it is possible that the power stage of the converter may have multiple voltage and current measurement circuits.

The measurement of alternating current (AC) or direct current (DC) voltage is simple to implement. It generally consists of a resistor divider circuit where the high voltage is stepped down to the measurement voltage range. Also, it can be implemented independent of the parameters of the converter. On the other hand, measuring the current in a power electronic converter requires more attention. Since the current sensor needs to be placed in the current path, it depends on the current rating and the switching frequency of the converter. Moreover, adding current sensors to the power stage of the converter has negative influences, such as increase in power losses and stray inductance in the commutation paths.

In this work, current sensors and measurement methods are examined. Furthermore, a novel simple-to-implement observer based current measurement in digital domain is proposed to reduce the number of sensors in the switching converter. This results in fewer negative influences on the power supply and increases overall efficiency and power density.

1.1 DEFINITION OF THE PROBLEM

In modern switched-mode power supply (SMPS), measuring the current through the power inductor is required for digital or analog current control. For this purpose, various types of current sensors can be used to ascertain high-frequency current. These range from simple shunt-based sensors to complex magneto-resistor-based sensors [2], [3]. Each current sensor has its own advantages and disadvantages. For example, a shunt-based sensor can be added in series with the inductor in a low power (e.g., 15 W) converter to measure the inductor current . It offers a cheap and compact solution but adds to the power losses and reduces efficiency [4].

The shunt-based current sensor can be used to measure high current. In this case, the I^2R losses are reduced by selecting a very low shunt resistance in the μΩ range. However, this causes a very small voltage drop (in mV) across the shunt, requiring a precise current monitor to amplify the low voltage drop. Consequently, this increases the overall cost of the current measurement setup.

Current sensors based on the magnetic principle are also used widely in power electronics. These types of sensors have relative low power loss and offer an isolated current measurement output signal. However, their implementation is complex and requires more space in the converter [5]. Moreover, with the introduction of fast-switching silicon carbide (SiC) and gallium nitride (GaN) based power converters, current measurement becomes more challenging. These converters require short commutation paths, and the presence of the current sensors in the current path increases the parasitic inductance of the commutation loop.

In summary, the current measurement influences on the power losses, cost and switching behaviour of the converter. This defines the problem to be discussed in this research work.

1.2 RESEARCH OBJECTIVE AND METHOD USED

From the above discussion, it can be concluded that the appropriate selection of the current measurement setup is essential for the power supply. Therefore, the objective of this research work is to develop a

current measurement scheme that has less negative influence on the switching converter.

The work starts with a literature review consisting of the study of various types of current sensors. For the implementation of the current measurement schemes, a typical half-bridge with an inductor is assumed, as it is commonly found in various power electronic devices. Based on the type of the current sensors and their position in the switching circuit, an efficient scheme is selected. Furthermore, to reduce the number of the current sensors in the half-bridge based topology, the observer based concept is proposed.

The proposed current measurement scheme is validated with the simulations and then verified with practical implementations. In the newly developed scheme, only one CT sensor in the commutation path is used, and the auxiliary windings over the power inductor are employed, thus reducing one magnetic component from the half-bridge leg. Furthermore, the output voltages of the sensor and the secondary windings serve as the inputs to the current observer, which estimates the complete inductor current. Moreover, the current observer is possible to implement in both analog and digital domains. In the presented work, it is implemented in the digital domain with a low-cost DSP.

1.3 OVERVIEW OF CHAPTERS

- The present literature on current sensing schemes is discussed in Chapter 2. This chapter first presents the properties of a typical current measurement method in a power electronic circuit. Furthermore, the types of current sensors are also discussed. Then, the possible current sensing techniques for the half-bridge circuit are compared.
- Chapter 3 discusses the analytical analysis of the current through each component of a converter. For understanding, a 3-level DC-AC inverter is assumed. Such analysis is important to understand the formation of the current at different positions in the circuit.
- The proposed current observer scheme is explained in Chapter 4, where the requirements of this method are also presented.

- The implementation and verification of the digital current observer for DC-DC converter is documented in Chapter 5.
- The implementation and verification of the digital current observer for DC-DC converter is documented in Chapter 6.
- Finally, Chapter 7, summarizes the document with conclusions and results from the prototype.

2

CURRENT MEASUREMENT METHODS IN SWITCHING CONVERTERS

The measurement of current is an essential requirement in switched-mode power supplies, and for this purpose, current sensors are utilized. There exists a wide variety of current sensors based on operation, measurement range, cost, and complexity. In this chapter, the typical requirements of current sensors are described. Furthermore, the types of sensors are documented, and the current measurement setup in the half-bridge power electronic circuit is discussed.

2.1 PROPERTIES OF A CURRENT SENSOR

There are several key specifications of the current sensors, such as current rating, accuracy, measurement delay time, and bandwidth. A detailed discussion of these properties can be found in the literature [6], [7]. Moreover, the mathematical modelling of the current sensor is also possible by understanding the characteristics and operation principles. However, this is not discussed in this work. Below some of the important technical requirements from the literature are listed.

- The current sensor should be **compact** to minimize parasitic inductance in the current path. Moreover, the size of the sensor depends on its packaging and current handling capability.
- The current sensor must be able to withstand **current surges**, and its accuracy should not be affected by higher currents.
- The **response time** of the current sensor should be known so that the systematic error in the measurement can be corrected.
- The current sensor should be suitable for **sensing** either only **AC or DC currents** or both.
- The **current gradients** up to $\frac{\mathrm{kA}}{\mu\mathrm{s}}$ shall be detected by the sensor.

- The current sensing method should have the ability to **filter the electrical noise**. A high common-mode rejection ratio (CMRR), differential measurement, galvanic isolation, and proper grounding play significant role [8].
- The sensing method offers wide **measurement range** (A to kA) with a small absolute error and an error of $< 1\%$ from the measuring scale.
- The sensor should have low **dependence** on temperature and environmental conditions.

2.2 TYPES OF CURRENT SENSOR

A current sensor is a device that detects the flow of the electrical charges through a conductor and converts it into a proportional output voltage. This conversion is governed either by Ohm's law or by magnetic principles, such as Faraday's or Ampere's law. Thus, the fundamental operating principle of a current sensor can be divided in two categories: resistive or magnetic [9].

The resistor-based sensor forms the simplest version of current measurement. The voltage drop across the resistor represents the actual current flowing through it. This measurement offers a very wide bandwidth, from DC to the MHz range. It is capable of sensing current from a few amperes to hundreds of amperes with an accuracy in the range of $0.1\,\% - 2\,\%$. The resistance used as a sensor can be an external resistance (shunt resistor), the parasitic resistance of the current path, or the on-state resistance of the semiconductor switch (SENSEFET). The major drawback with these sensors is the significant power loss at high currents. Moreover, permanent damage to the sensor is also possible due to overcurrent.

The other type of the current sensors operates on the principle of the magnetics, where the magnetic field generated by the flow of the current is detected, and a proportional output voltage is obtained. These sensors have inherent galvanic isolation from the power circuit and low power loss. The bandwidth of these sensors depends on the operating principle and construction. For example, a CT sensor offers the bandwidth from kHz to MHz but cannot measure the DC current. In contrast, a hall-effect based sensor can detect the DC

currents but the AC bandwidth is limited to the kHz range. Similarly, the accuracy also varies widely, 0.1 % – 10 %. The worst accuracy occurs in core-less open loop sensors due to the negative influence of external magnetic fields. The details of the principle of operation of each sensor can be found in the literature [6], [7] and [9].

2.2.1 *Per-unit PCB Area Comparison*

In this section, the commonly used current sensors in power electronic circuits are compared based on the space required for implementation on a printed circuit board (PCB). All of the sensors are able to measure the current up to 15 A. It is a reasonable current for a wide range of the industrial applications where DC-DC converters or AC-DC rectifiers are utilized. The comparison is made using the 3*D* image generated from the PCB design software 'Altium Designer' as shown in Figure 2.1. The components are placed only on the top of the board. Each implementation is explained in the following points.

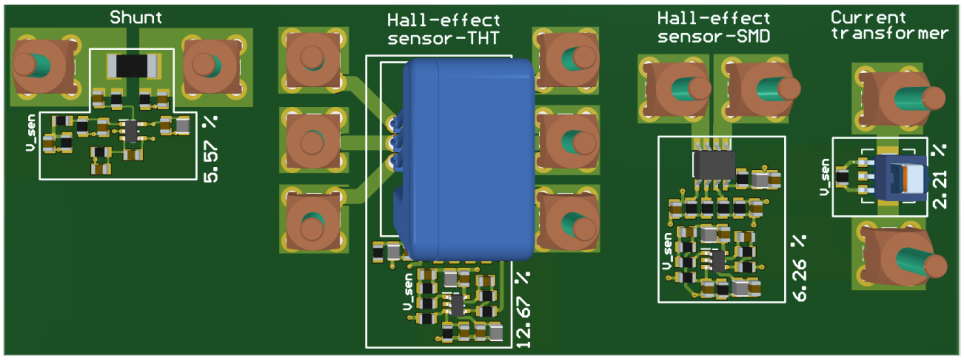


Figure 2.1: Per uni area comparison of current sensors

- The shunt resistor *PSR*100*KTQFJ*2*L*00 in 2512 (6432) housing from ROHM is displayed as the first sensor (starting from the left). It has the resistance of 2 mΩ so that it gives the voltage drop of 30 mV for 15 A. For analog or digital control, this low voltage is usually amplified with an additional amplifier or a current monitor, which requires more space [10]. Here, the area required for such an implementation is estimated to be approximately 5.57 % of the area of the PCB.

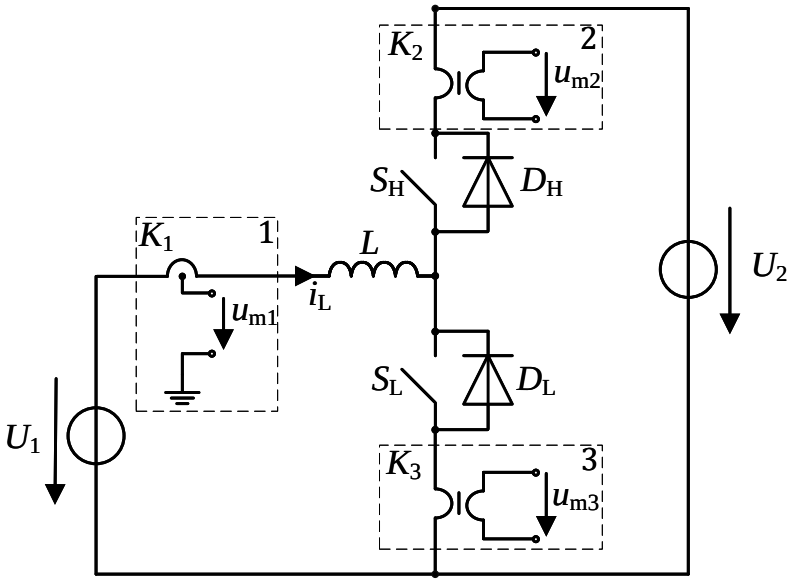
- A closed-loop Hall-effect based current transducer $LXSR15-NPS$ from LEM is shown as the second sensor. It is a through hole technology (THT) device and also requires a unipolar DC voltage for the operation. Furthermore, an additional amplifier is needed to amplify the output voltage. The frequency bandwidth of this sensor is up to 300 kHz. Due to the housing and additional components, this implementation requires approximately 12.67 % of the area of the PCB.
- Another closed-loop Hall-effect based sensor $TMCS1100A1QDR$ from Texas Instruments with an surface-mounted device (SMD) footprint is shown further. It has the same requirements as that of the LEM sensor. As compared to the previous sensor, it has the frequency bandwidth of 80 kHz. But the implementation takes 6.28 % area on the PCB as the housing of the sensor is smaller compared to the THT component.
- The current transformer sensor requires the least area of 2.21 % of the PCB. The CT shown here is $B82801B0724A060$ from EPCOS / TDK. It is an open-loop sensor and does not require additional voltage or an amplifier. The sensed voltage can be scaled with the burden resistor.

In the mentioned per unit areas of the measurement methods, the area taken by the screw connectors is not included. This comparison has shown that current measurement with CT takes the minimum space and does not need additional DC voltage for operation. However, such CT sensors can only measure pulse currents with a typical frequency range of 50 kHz to 1 MHz.

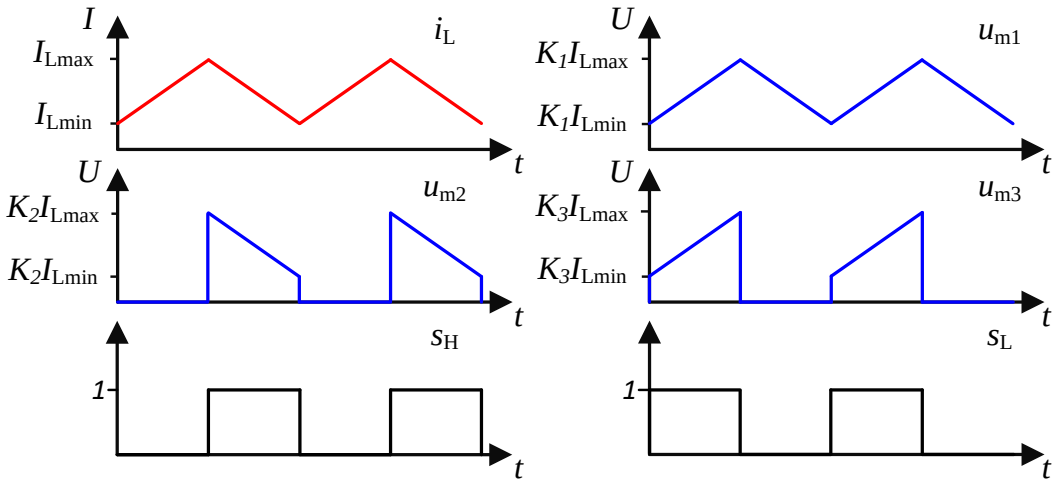
2.3 CURRENT MEASUREMENT IN A HALF-BRIDGE

In this section, the current measurement methods for the half-bridge with an inductor in boost configuration are investigated. The half-bridge leg can consist of two diodes (uncontrolled), a diode and a transistor (non-synchronous), or two transistors (synchronous). Furthermore, this configuration is found in numerous converters, rectifiers, and inverters. For further discussion, the half-bridge with two transistors is assumed, as shown in Figure 2.2(a). The input voltage U_1 and the output voltage U_2 are considered constant, with

$U_2 > U_1$. The switches S_H and S_L switch complementary to each other, and the inductor current i_L varies depending on the states of the switches. Furthermore, in this configuration the current sensors can be placed at positions 1, 2, and 3 [11].



(a)



(b)

Figure 2.2: (a) Half-bridge with possible current sensor arrangements at positions 1, 2, and 3 (b) Curves of Inductor current (red), sensor output voltages (blue) and switching signals (black)

The curves of the inductor current and the output voltages of the current sensors are shown in Figure 2.2(b). The signals s_H and s_L are the switching signals for the high-side and low-side power switches, respectively. The current sensor placed at position 1 is in series with the inductor and carries the complete inductor current i_L. The output voltage u_{m1} of this sensor has the same shape as i_L with K_1 proportionality constant. Moreover, the current sensor at this position must be capable of measuring both the DC current and the high-frequency AC ripple, as the inductor current in CCM operation contains both DC and AC content. Therefore, a shunt-based (non-isolated) sensor, a Hall-effect based sensor or an anisotropic magneto-resistor (AMR) (isolated) sensor can be used.

Alternatively, the complete inductor current can also be sensed by placing the sensors in series with each switch. A sensor at position 2 (or 3) has the output voltage u_{m2} (or u_{m3}) same in shape as of the inductor current during the interval when $s_H = 1$ (or $s_L = 1$); otherwise it is zero. K_2 and K_3 are the proportionality constants of the sensors. For such measurements, CT sensors can be used, as only the AC content of the inductor current flows through the switches. Additionally, there are other current measurement methods used only in the laboratory, such as current measurement with a Rogowski coil (no DC capability) or current sensing with HOKA principle (DC and AC capability) [12]. Here, the discussion proceeds with sensors that are available as components to be placed in the half-bridge circuit.

1. Current sensors based on the magnetic principles, such as Hall-effect or AMR sensors are typically available as closed-loop sensors with the flux compensation and filtering circuit in a signal package. Hence, the output voltage signal can be used for control and protection. In the half-bridge circuit shown above, these types of sensors can be installed at all positions. These sensors are isolated from the power circuit and can sense both DC and AC currents.

   However, there are some disadvantages associated with these sensors. For instance, Hall-effect based sensors are mechanically large and require more installation space. On the other hand, the AMR sensors require a special PCB design where the current

path should be placed under the sensor housing, which is not practical for high currents. Additionally, the cost of these sensors is also relative high as compared to the other sensors. Therefore, these sensors are not considered as first choice in this scenario.

2. Shunt-based current measurement offers a compact and cheap solution. It is capable of sensing both DC and AC currents (up to MHz range). Moreover, it can be implemented at all positions shown in Figure 2.2(a). The major drawbacks of this current sensing method are the I^2R losses and the lack of isolation from the power circuit. These issues can be partially resolved by using a small size and precise shunt resistor with a current monitor, but this increases the cost and required space for the implementation. Despite these drawbacks, shunt-based current sensing remains popular in power electronics applications based on analog control due to its simple implementation. However, due to the power losses, it is not used in this work.

3. The CT-based current sensor can also be utilized to measure the complete inductor current in the half-bridge circuit. However, it can only be placed at positions 2 and 3 as it can sense only the AC current. It is a low-cost sensor, and the implementation is also simple. Moreover, it provides an isolated output voltage and has low power loss. The major disadvantage for this measurement is that the CT needs to be added in the commutation path, which increase the parasitic inductance of the current path. Thus, it affects the switching characteristics of the power switches. Additionally, the outputs of the both sensors are combined in the analog or digital domain to get the full inductor current. Due to the low losses and low cost, this current measurement is preferred.

At present, the current measurement with two CT sensors is the most reliable solution. The outputs u_{m2} and u_{m3} of the sensors are combined by an analog circuit (analog domain) or by an algorithm in a DSP (digital domain) to obtain the DC and AC content present in the inductor current.

2.4 CURRENT OBSERVER CONCEPT

The presence of the sensor in the path of the current influences the power stage of the half-bridge. Therefore, sensor less or observer based current measurement and control methods are proposed in the literature to avoid or to reduce the negative influence of the current sensors [13]. Such techniques are present for DC-DC converters [14], [15] and also for AC-DC rectifiers [16], [17]. These methods results in the reduction of the size and the power losses of the converter as the number of sensors is reduced.

As mentioned in the literature, a simple observer can be implemented as shown in Figure 2.3. First, the voltage across the inductor is measured and stepped down to $u_{L,o}$. It is then passed through an integrated and multiplied by the gain of $1/L$ to estimate the AC content of the inductor current $i_{L,o}$. Moreover, the DC content in i_L is estimated by measuring the input and output voltages and knowing the load at the output. Such sensor less current estimation is not attractive for the industrial application, as the over current detection does not seem practical with this implementation of the current observer.

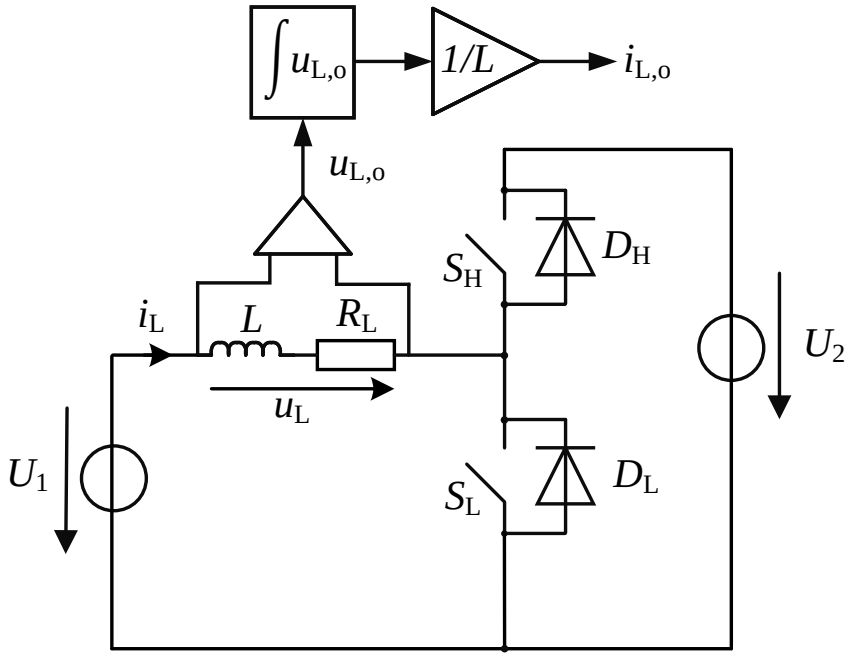


Figure 2.3: Current sensing with the current observer

From section 2.3, it is concluded that the current measurement with a CT offers minimum losses and does not require an external voltage supply or a current monitoring amplifier for operation. However, adding the sensor in the commutation loop increases the parasitic inductance, affecting the switching behavior of the switches and causing additional switching losses. Furthermore, the converters based on SiC and GaN switches, which operate at higher switching frequencies compared to conventional Si-based switches, will face more voltage stress due to the additional parasitic inductance caused by the two current sensors. To overcome this, a current measurement method is proposed here that uses the one current transformer sensor in series with either high-side or low-side switch [18]. It also utilizes auxiliary windings on the inductor to measure the inductor voltage as shown in Figure 2.4. In the figure, only one secondary winding is shown for simplicity in this section.

The voltage u_{L} across the inductor varies with the switching signals s_{H} and s_{L}. If the switching frequency is considered very high compared to the frequency of U_1 and U_2, then the inductor voltage can be assumed as constant during each switching state. Furthermore, the physical inductor current can be expressed in terms of the voltage across the inductor for the switching states as written below.

For $t_0 \leq t \leq t_1$, $s_{\mathrm{L}} = 1$ and $s_{\mathrm{H}} = 0$

$$i_{\mathrm{L}}(t) = \frac{1}{L} \cdot U_1 \cdot (t_1 - t_0) + i_{\mathrm{L}}(t_0) \tag{2.1}$$

For $t_1 \leq t \leq t_2$, $s_{\mathrm{L}} = 0$ and $s_{\mathrm{H}} = 1$

$$i_{\mathrm{L}}(t) = -\frac{1}{L} \cdot (U_1 - U_2) \cdot (t_2 - t_1) + i_{\mathrm{L}}(t_1) \tag{2.2}$$

$i_{\mathrm{L}}(t_0)$ and $i_{\mathrm{L}}(t_1)$ are the initial current values for each interval and are shown in 2.4(b) as I_{Lmin} and I_{Lmax}, respectively. The inductor voltage can be measured and stepped down by using an auxiliary winding. The voltage signal u_{Ls} can be used further to find the volt-second product in 2.1 and 2.2.

The estimation of the voltage-time integral is possible in both analog and digital domains. Implementing this with analog circuits adds de-

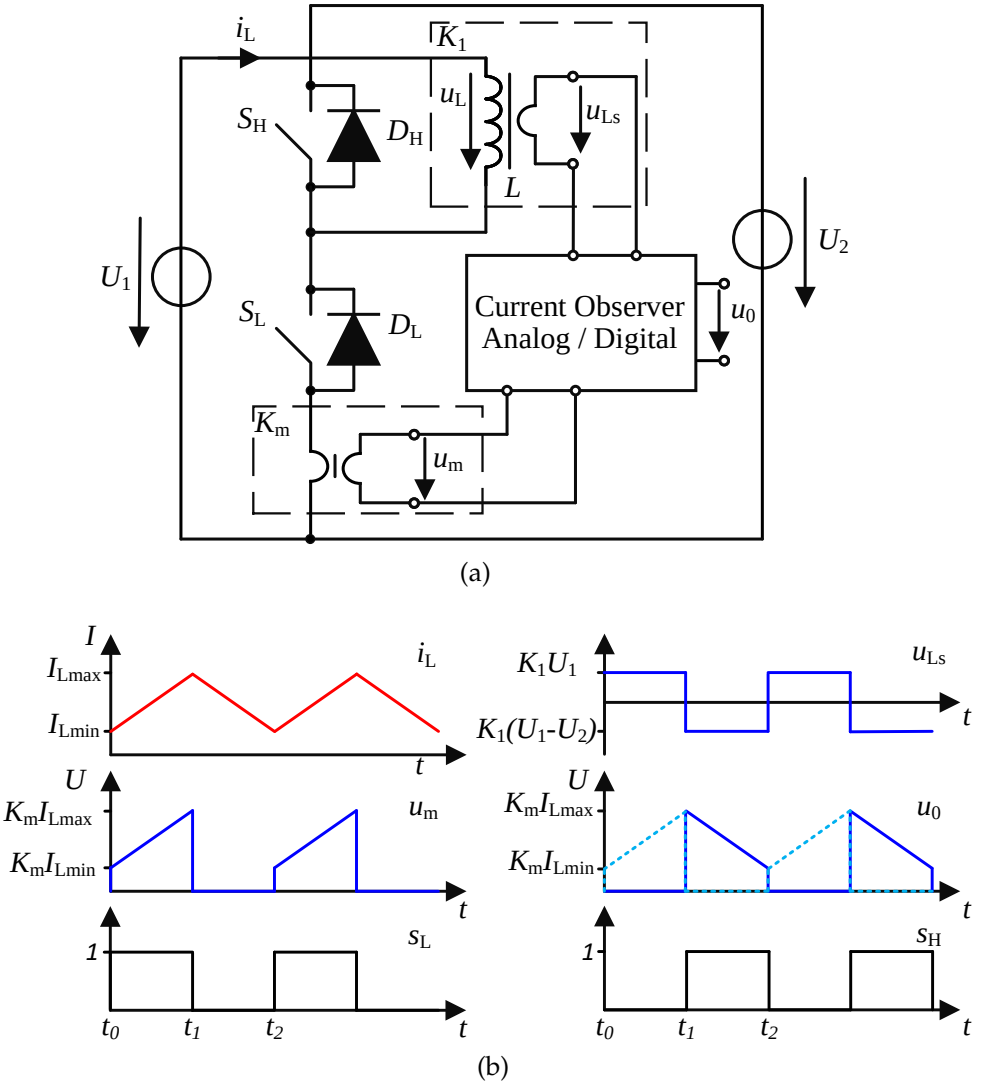


Figure 2.4: Half-bridge boost converter (a) with current observer (b) curves of the sensors corresponding to the switching signals

lays in the computation of u_0 and requries physical space on the PCB. On the other hand, the DSP used for controlling the converter can also be utilized for the digital computation of the current observer equations. However, for the digital implementation, the voltage signal u_{Ls} can not be directly used with the DSP as it contains the negative polarity. It can be avoided by using multiple secondary windings on the inductor and clamping the negative part of the output signals as discussed in 4.2.1. In the next chapters, the implementation of the

digital current observer is documented including the configuration of the modules that are used for the digital estimation of 2.1 and 2.2.

In summary, the methods to measure the current through the inductor of the half-bridge are discussed and compared. From the literature, the use of two current transformers for the inductor current measurement offer an isolated, low-loss and cost-effective solution. Furthermore, the current observer concept is proposed that utilizes one physical current sensor and the auxiliary windings on the inductor. Moreover, this concept has the potential to reduce parasitic inductance in the commutation path and improve the switching characteristics of the power electronic switches.

3

CURRENT ANALYSIS IN A POWER ELECTRONIC CIRCUIT

In order to select the current measurement method and the positions of the current sensors in the power electronic circuit, it is useful to perform a steady state analytical analysis of the topology. This helps in listing the requirements for the sensors, such as the current rating, bandwidth and DC or AC capability. It is also useful in the selection of the active and passive components for the power stage. In this chapter, a DC-AC inverter is used as an example, and the root mean square (RMS) and the average current formulas are documented for each power electronic component [19], [20]. These current formula can be used further to find out the power losses. These inverters are found in various applications, such as traction inverter for electric vehicles and grid-connected systems. Furthermore, the DC-AC inverter can be a 4-quadrant converter (4QC) or a multilevel NPC inverter.

The motivation of this chapter is to help the reader to understand the formulation of current in a typical power electronic circuit. Therefore, a slightly complex 3L T-type NPC inverter is analysed further. However, from the next chapter the focus is shifted to the current measurement for 2L topologies.

3.1 THREE-LEVEL NEUTRAL POINT CLAMPED INVERTER

A simplified three-level NPC inverter is shown in Figure 3.1. The DC input voltage U_{DC} to the inverter is supplied by a battery bank like in automotive industry, or from a converter, or directly from a DC grid. Hence, it is assumed to be constant. The currents i_a, i_b, and i_c at the output terminals have both positive and negative polarities, depending on the output load. The DC-link capacitor bank consists of two physical capacitors, and the voltage across each capacitor is assumed to be half of the DC-link voltage, $\frac{U_{DC}}{2}$. The switching

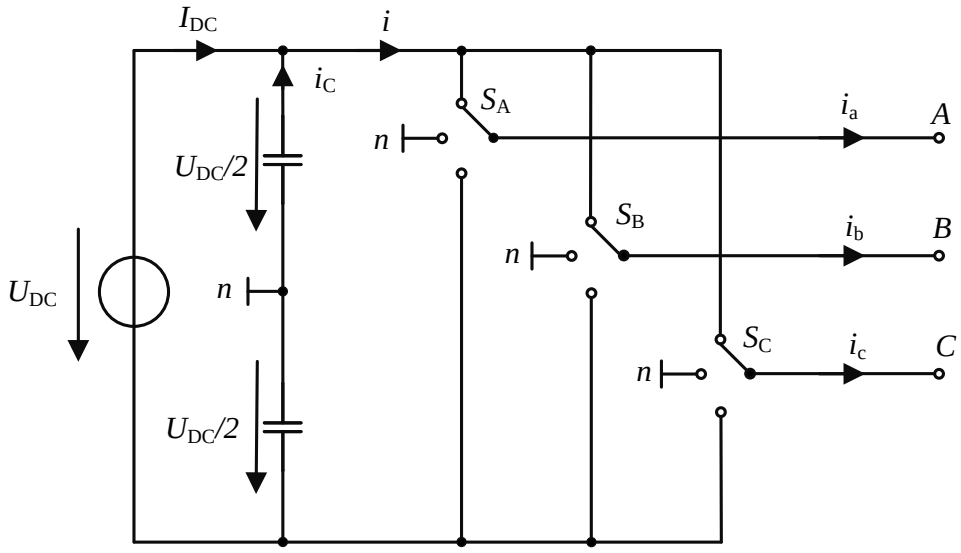


Figure 3.1: Three-level inverter equivalent circuit

signal for each switch can have three states and is controlled by the respective duty cycle signal.

The three states of the switches s_a, s_b, and s_c are

$$s_a,\, s_b,\, s_c = +1, 0, -1 \tag{3.1}$$

$+1$ represents that the switch is connected to the positive rail of U_{DC}, -1 represents that the switch is connected to the negative rail of U_{DC}, and 0 represents that the switch is connected to the center point n of the DC-link. Now, the line voltages u_{ab}, u_{bc}, and u_{ca} can be formulated as

$$\begin{aligned} u_{ab} &= \frac{1}{2} \cdot (s_a - s_b) \cdot U_{DC} \\ u_{bc} &= \frac{1}{2} \cdot (s_b - s_c) \cdot U_{DC} \\ u_{ca} &= \frac{1}{2} \cdot (s_c - s_a) \cdot U_{DC} \end{aligned} \tag{3.2}$$

This shows that the line voltages also switch between different voltage levels depending on the corresponding switching signals. The line voltage u_{ab} can be further written as

$$u_{ab} = \begin{cases} U_{DC} & s_a = +1,\ s_b = -1 \\ \frac{U_{DC}}{2} & s_a = +1,\ s_b = 0 \parallel s_a = 0,\ s_b = -1 \\ 0 & s_a = s_b = 0 \parallel s_a = s_b = +1 \parallel s_a = s_b = -1 \\ -\frac{U_{DC}}{2} & s_a = -1,\ s_b = 0 \parallel s_a = 0,\ s_b = +1 \\ -U_{DC} & s_a = -1,\ s_b = +1 \end{cases} \tag{3.3}$$

u_{bc} and u_{ca} can also be formulated similarly. Further for the analysis, only one line voltage u_{ab} is assumed. It can be seen in 3.3 that the line voltage switches between three levels, i.e., U_{DC}, $\frac{U_{DC}}{2}$, and 0.

The current i that is flowing into the inverter can be expressed as the sum of the product of each line current and the respective switching signal, as written below.

$$i = s_a \cdot i_a + s_b \cdot i_b + s_c \cdot i_c \tag{3.4}$$

Furthermore, if the line currents vary sinusoidally and a three-phase load is assumed at the output, then the currents can be written as

$$\begin{aligned} i_a &= \hat{I} \cdot \sin(\theta - \phi) \\ i_b &= \hat{I} \cdot \sin(\theta - \frac{2\pi}{3} - \phi) \\ i_c &= \hat{I} \cdot \sin(\theta + \frac{2\pi}{3} - \phi) \end{aligned} \tag{3.5}$$

where $\hat{I}$ is the amplitude of the phase current and ϕ represents the phase angle difference between the phase voltage and the current introduced by the load. With these assumptions, the RMS and average values of the current i can be formulated, and these values can be further used to derive the formula for the RMS content of the capacitor current i_C.

3.2 CAPACITOR STRESS CURRENT CALCULATION

The DC-link capacitors are essential components in the multi-level or three-level inverters, and their lifetime is directly influenced by the

thermal stress and the overvoltage operation. Thermal stress occurs due to power loss across the equivalent series resistance (ESR) of the capacitor. The RMS current flowing through the capacitor estimates the losses by ${I_{C,RMS}}^2 \cdot \text{ESR}$. Therefore, it is important to know the RMS current provided by the capacitor to the inverter. In the following section, the analytical formula of $I_{C,RMS}$ is derived and explained.

The current i flowing in to the inverter [c.Fig 3.1] is composed of both DC and AC contents. The DC current is supplied by the attached DC voltage source, while the AC current is introduced by the DC-link capacitors. Hence, the RMS current provided by the DC-ink capacitor bank can be written in terms of the RMS current and the average current of i [19].

$$I_{C,RMS} = \sqrt{{I_{RMS}}^2 - {I_{avg}}^2} \tag{3.6}$$

The current i given in 3.4 depends on the line currents and the switching signals. Furthermore, the switching signals are the output of the pulse width modulation PWM. The input to the PWM are the modulating signals generated by the control algorithm. These signals represent the normalized terminal voltage $u_{a,b,c}$, and for the sinusoidal PWM, these signals can be represented as follows.

$$\begin{aligned} d_a &= M \cdot \sin(\theta) \\ d_b &= M \cdot \sin(\theta - \frac{2\pi}{3}) \\ d_c &= M \cdot \sin(\theta + \frac{2\pi}{3}) \end{aligned} \tag{3.7}$$

Where, M is the modulation index given as

$$M = \frac{u^*}{\frac{U_{DC}}{2}} \tag{3.8}$$

and u^* is the required terminal voltage and it is normalized by the half of the DC-link voltage. For the sinusoidal PWM, the modulation index varies in the range $[0 - 1]$. In literature, various other modulation techniques are also found, where the modulation index varies between $0 \leq M \leq \frac{2}{\sqrt{3}}$, and a higher terminal voltage can be achieved [21]. For further analysis the simplest sinusoidal PWM is assumed as shown in Figure 3.2.

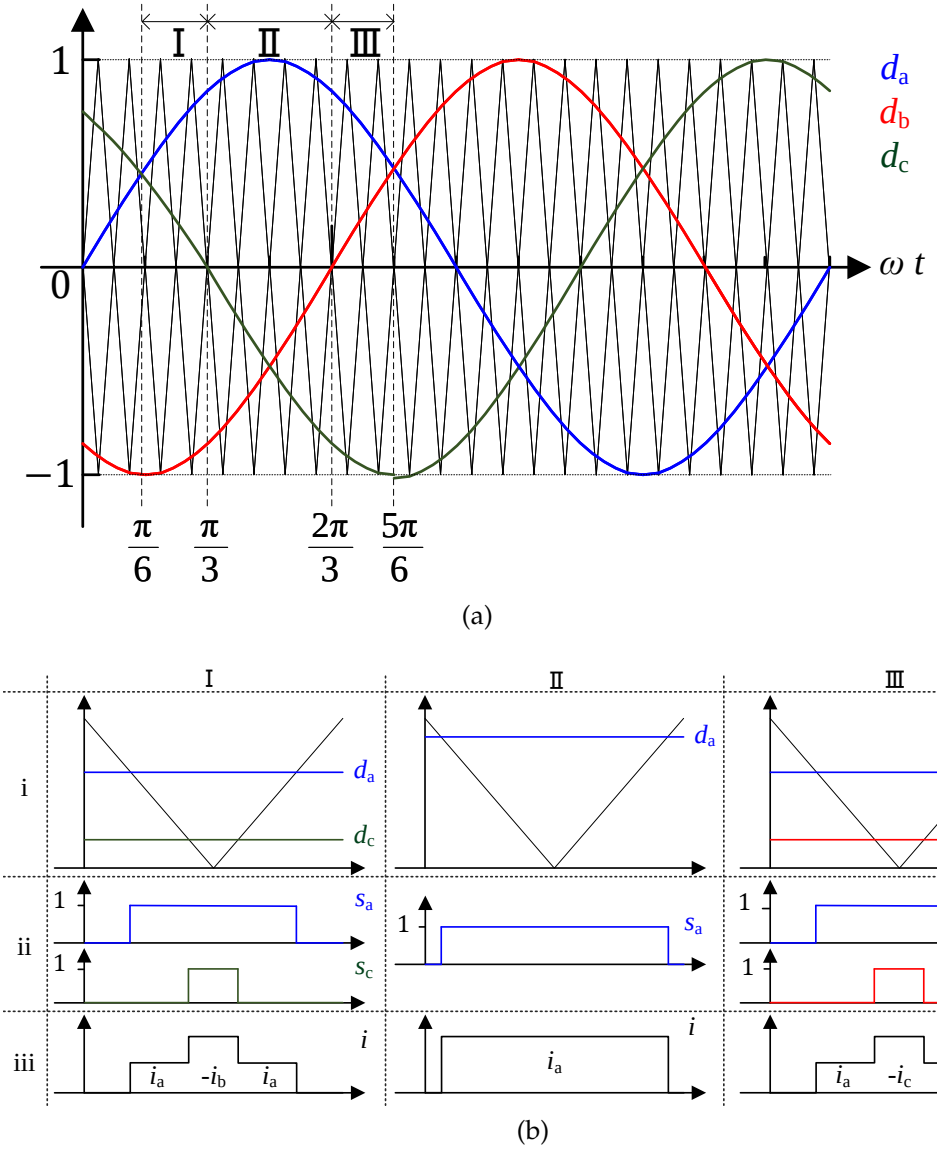


Figure 3.2: (a) modulating sinusoidal signals with triangular carrier signals of PWM (b) current i for one switching instant for each sub-interval

The modulating signals (d_a, d_b, d_c) and the triangular carriers for the PWM are shown in Figure 3.2(a). The analysis can be simplified by considering only the $\frac{2\pi}{3}$ region where d_a is maximum and further dividing this region into three sections: I, II, and III. This is because the global ripple of i is periodic after each $\frac{2\pi}{3}$ interval. Moreover, the negative switching signal for each section is not drawn. The duration of the sections I and III is $\frac{\pi}{6}$, and the duration of the section

II is $\frac{\pi}{3}$. Here, it is assumed that the frequency of the carrier signal is significantly higher compared to the output line currents or the modulating signals. Therefore, for each switching interval, the line currents can be assumed as constant.

The formation of the current i can be explained with Figure 3.2(b). In the figure, the row (i) shows one switching interval of each section I, II and III. The row (ii) gives the switching sates of the switches and the row (iii) displays the shape of i for each switching interval. In the curves, the switching signal is logic 1 when the respective duty signal is greater than the triangular carrier.

In the section-I in 3.2(b), d_a and d_c are positive, and d_b is negative (but not drawn). The instant when $s_a = 1$ and $s_c = 0$, the current i is equal to i_a; and when $s_a = s_c = 1$, $i = |i_b|$ occurs. In the section-II, only d_a is positive, while d_b and d_c are negative. Hence, for the interval where $s_a = 1$, $i = i_a$. In the section-III, d_a and d_b are positive, and d_c is negative. The instant when $s_a = 1$ and $s_b = 0$, $i = i_a$; and when $s_a = s_b = 1$, $i = |i_c|$. Further, for each section, the RMS and the average value of i are written in 3.9, 3.10. These equations are then integrated for the corresponding intervals and used to find out the global I_{avg} and I_{RMS} as written in 3.11, 3.12.

The average value of the current for each section can be written as

$$\begin{aligned} I_{avg,I} &= (d_a - d_c) \cdot i_a + d_c \cdot (-i_b) \\ I_{avg,II} &= d_a \cdot i_a \\ I_{avg,III} &= (d_a - d_b) \cdot i_a + d_b \cdot (-i_c) \end{aligned} \tag{3.9}$$

Similarly, for the RMS value of i for each section the squared value of the respective current is used

$$\begin{aligned} I_{MS,I} &= (d_a - d_c) \cdot i_a^2 + d_c \cdot (-i_b)^2 \\ I_{MS,II} &= d_a \cdot i_a^2 \\ I_{MS,III} &= (d_a - d_b) \cdot i_a^2 + d_b \cdot (-i_c)^2 \end{aligned} \tag{3.10}$$

The expression for the global I_{avg} and I_{RMS} can be written respectively as below.

$$I_{avg} = \frac{3}{2\pi}\left(\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} I_{avg,I}\, d\theta + \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} I_{avg,II}\, d\theta + \int_{\frac{2\pi}{3}}^{\frac{5\pi}{6}} I_{avg,III}\, d\theta\right) \tag{3.11}$$

$$I_{\text{RMS}} = \sqrt{\frac{3}{2\pi}\left(\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} I_{\text{MS,I}}\, d\theta + \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} I_{\text{MS,II}}\, d\theta + \int_{\frac{2\pi}{3}}^{\frac{5\pi}{6}} I_{\text{MS,III}}\, d\theta\right)} \quad (3.12)$$

The integrals in 3.11 and 3.12 can be solved using any mathematical tool, resulting in a simplified expressions. In this case, the MATLAB mathematical solver is used to solve the integrals over θ. The parameters, such as modulation index M, power factor angle ϕ, and current amplitude $\hat{I}$ are assumed to be constant.

All the integrals in the equations 3.11 and 3.12 are simplified and presented in equations 3.13 and 3.15. Furthermore, the complete simplified formulas for I_{avg} and I_{RMS} are given in the equations 3.14 and 3.16 respectively.

$$\begin{aligned}
\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} I_{\text{avg,I}}\, d\theta &= \frac{-\hat{I}\cdot M}{12}\left(\frac{3}{2}\sin\phi - 2\pi\cos\phi + \frac{3\sqrt{3}}{2}\cos\phi\right) \\
\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} I_{\text{avg,II}}\, d\theta &= \frac{\hat{I}\cdot M}{12}\left((2\pi + 3\sqrt{3})\cos\phi\right) \\
\int_{\frac{2\pi}{3}}^{\frac{5\pi}{6}} I_{\text{avg,III}}\, d\theta &= \frac{-\hat{I}\cdot M}{12}\left(3\cos(\phi + \frac{\pi}{6}) - 2\pi\cos\phi\right)
\end{aligned} \quad (3.13)$$

$$I_{\text{avg}} = \frac{3}{4}\hat{I}M\cos\phi \quad (3.14)$$

Similarly,

$$\begin{aligned}
\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} I_{\text{MS,I}}\, d\theta &= \frac{5\hat{I}^2 M\sin(2\phi)}{12} - \frac{5\hat{I}^2 M\cos(2\phi)}{24} - \frac{\hat{I}^2 M}{4} + \frac{\sqrt{3}\hat{I}^2 M}{4} \\
&\quad + \frac{\sqrt{3}\hat{I}^2 M\cos(2\phi)}{6} - \frac{7\sqrt{3}\hat{I}^2 M\sin(2\phi)}{24} \\
\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} I_{\text{MS,II}}\, d\theta &= \hat{I}^2 M\left(\frac{5\cos^2\phi}{6} + \frac{1}{12}\right) \\
\int_{\frac{2\pi}{3}}^{\frac{5\pi}{6}} I_{\text{MS,III}}\, d\theta &= -\frac{5\hat{I}^2 M\sin(2\phi)}{12} - \frac{5\hat{I}^2 M\cos(2\phi)}{24} - \frac{\hat{I}^2 M}{4} + \frac{\sqrt{3}\hat{I}^2 M}{4} \\
&\quad + \frac{\sqrt{3}\hat{I}^2 M\cos(2\phi)}{6} + \frac{7\sqrt{3}\hat{I}^2 M\sin(2\phi)}{24}
\end{aligned}$$

(3.15)

$$I_{\text{RMS}} = \sqrt{\frac{\sqrt{3}\hat{I}^2 M(4\cos^2\phi + 1)}{4\pi}} \tag{3.16}$$

Now, substitute 3.14 and 3.16 into 3.6 to determine the RMS current flowing through the DC-link capacitor.

$$\begin{aligned} I_{\text{C,RMS}} &= \sqrt{\frac{\sqrt{3}\hat{I}^2 M(4\cos^2\phi + 1)}{4\pi} - (\frac{3}{4}\hat{I}M\cos\phi)^2} \\ &= \sqrt{\frac{\hat{I}^2 M(4\sqrt{3}\cos^2\phi + \sqrt{3})}{4\pi} - \frac{9\hat{I}^2 M^2\cos^2\phi}{16}} \\ &= \hat{I}\sqrt{\frac{M}{2}(\frac{4\sqrt{3}\cos^2\phi}{2\pi} + \frac{\sqrt{3}}{2\pi} - \frac{9M\cos^2\phi}{8})} \end{aligned} \tag{3.17}$$

$$I_{\text{C,RMS}} = \hat{I}\sqrt{\frac{M}{2}(\frac{\sqrt{3}}{2\pi} + (\frac{2\sqrt{3}}{\pi} - \frac{9M}{8})\cos^2\phi)} \tag{3.18}$$

The equations 3.14, 3.16 and 3.18 are verified using a simulation model in MATLAB. The parameters are assumed as $\hat{I} = \sqrt{2} \cdot 500$ A, $M = 1$, and $\cos\phi = 1$. The data during the simulation is sampled with 50 ns step size, and the build-in functions of MATLAB are used to find out I_{avg}, I_{RMS}, and $I_{\text{C,RMS}}$. The **relative error** between the simulation-based results and the analytically calculated results is very small, i.e., 0.0011%, indicating that the above stated expressions are correct. Moreover, the model is also simulated with different PWM techniques such as SVM. The obtained data is further analysed and compared with above-documented equations. It shows that the modulation technique has no affect on the RMS current of the capacitor bank and that it only depends on the attached three phase AC load.

3.3 POWER ELECTRONIC SWITCHES CURRENT CALCULATION

Now, the assumed switches S_{A}, S_{B}, and S_{C} in the previous section can be implemented with the power electronic components , such as

MOSFETs or IGBTs. The implementation for these switches can be considered with two possible configurations, as shown in Figure 3.3. In a typical NPC inverter, one switch consists of series connection of four transistors with free wheeling diodes and two clamping diode. In this arrangement, the blocking voltage for each device is lower then the DC-link voltage. Alternatively, a T-type configuration is also possible, which requires fewer components. However, the blocking voltage for all the components is not the same. The components in the outer leg must withstand the complete DC-link voltage, while the components in the inner leg must withstand half of the DC-link voltage [22], [23].

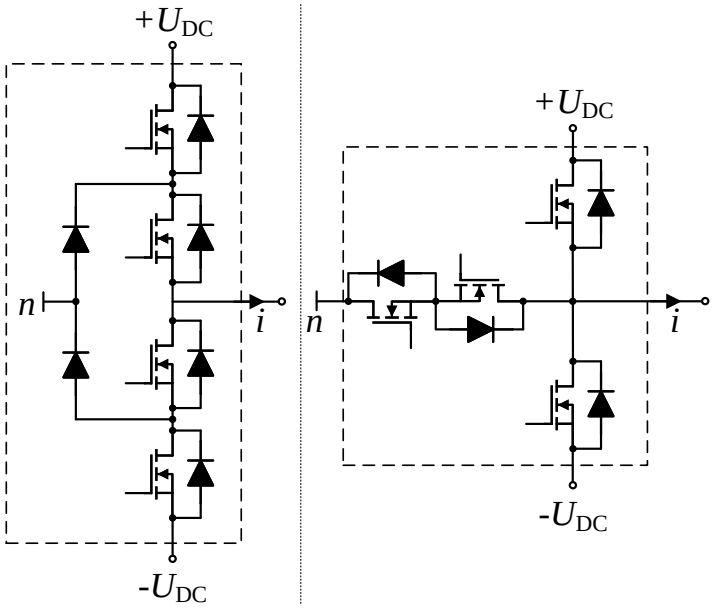


Figure 3.3: Realization of the switches for the three level inverter

In this section, the switches are realized as T-type for the three-level NPC inverter, as shown in Figure 3.4. Two transistors are placed between the positive and negative rails of U_{DC}, and the other two transistors are placed between the output terminal and the n potential of the DC-link to conduct and block the bidirectional current. For S_A, T_1 and T_2 form the outer leg, and T_3 and T_4 form the inner leg of the switch and respectively same applies to the other switches S_B and S_C. Moreover, the switching signals are represented with $s_{1,2,...,12}$ for each transistor shown in the figure. The blocking voltage required

for the outer leg transistors should be greater than the applied U_{DC} and for the inner leg transistors it should be greater than $\frac{U_{DC}}{2}$.

For the analysis of the current, it is assumed that the three phases of the inverter are balanced, and the currents are 120° shifted from each other. Therefore, only one switch S_A, is considered for the analysis. Furthermore, the current flowing out of the terminal A is taken as positive, and the formulas for the components that carry the positive current are written below. Due to the symmetry, these formulas can be applied to the components involved during the negative flow of the current. For the switch S_A, the components involved during each polarity of the current and the switching signals of the transistors are illustrated in Figure 3.5.

For the positive current i_a and in-phase positive u_a voltage [c. Fig 3.5 (b)], the current flows through T_1, T_4, and D_3. The switching signals s_1 and s_3 are complementary to each other, and s_4 remains in a high state for the entire duration of the positive voltage. Similarly, in the case of the negative current i_a and in-phase negative u_a voltage, the current flows through T_2, T_3, and D_4. The switching signals s_2 and s_4 are complementary to each other, and s_3 remains in a high state for the entire duration of the negative voltage.

The case in which the current and voltage are not in phase with each other and have a phase angle ϕ in between as shown in 3.5 (c). This

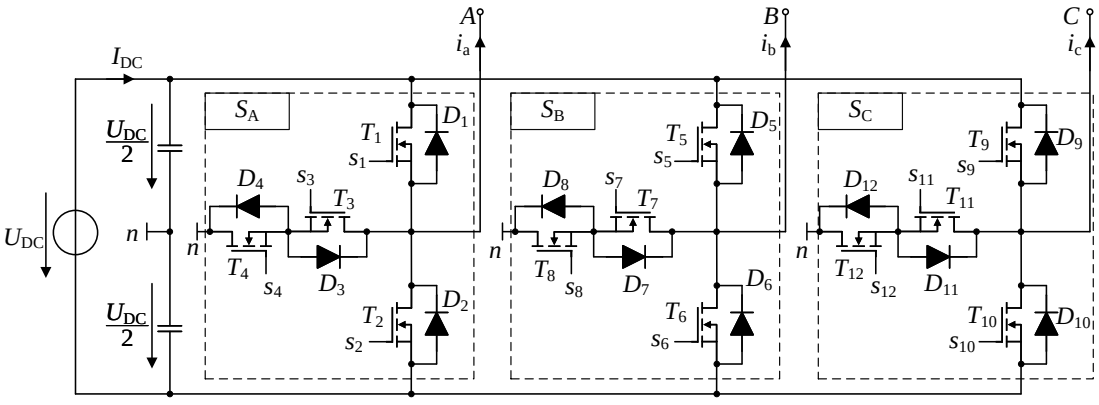


Figure 3.4: T-type NPC three-level inverter with MOSFETs

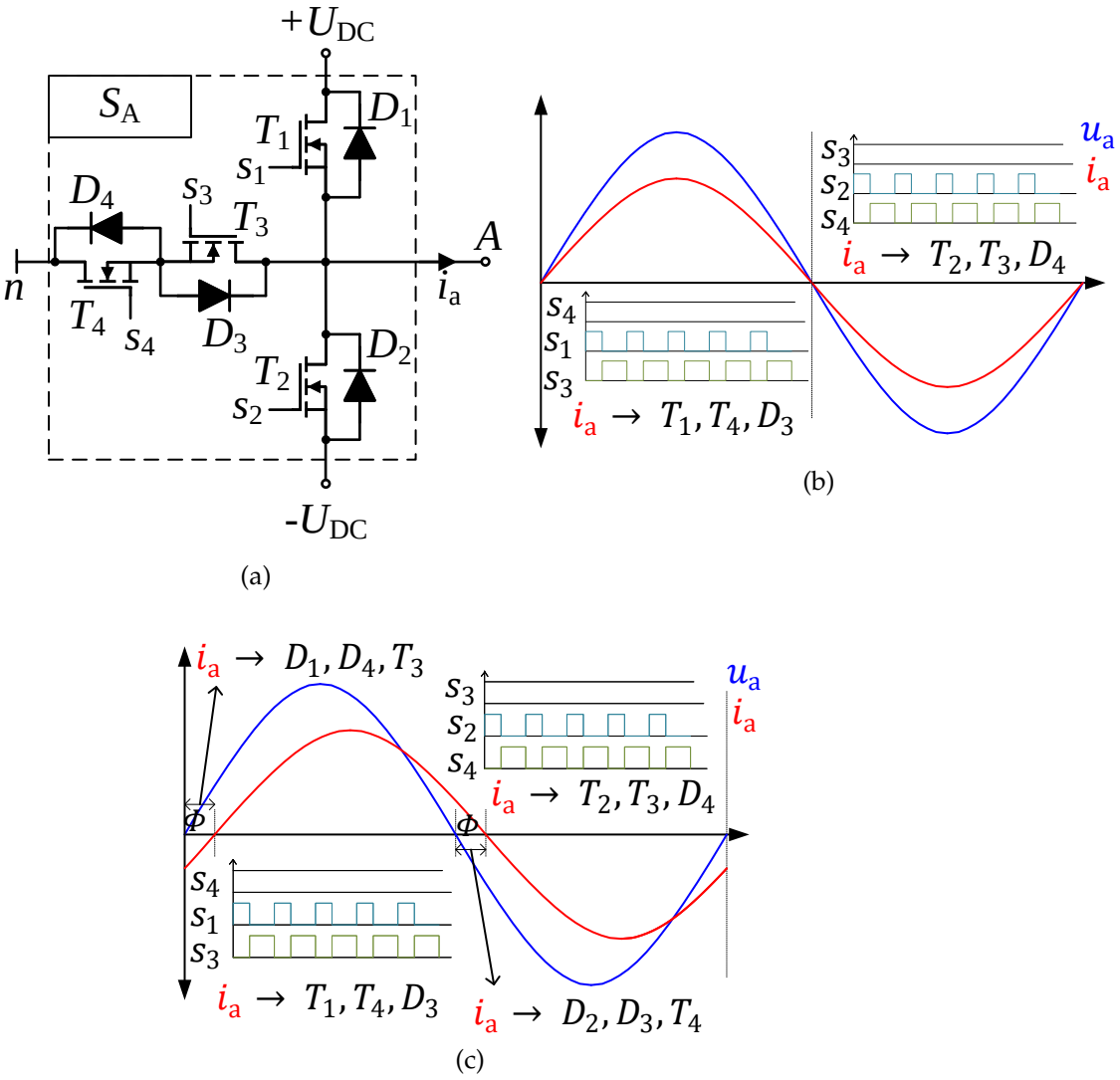


Figure 3.5: Realization of the switch S_A, the switching signals for the transistors and the diodes of S_A for i_a and u_a with (a) $\phi = 0$ (b) and $\phi \neq 0$ (c)

scenario introduces two additional cases. First, when the voltage is positive and the current flows in the negative direction, D_1, D_4, and T_3 conduct the current. During this interval, the switching signals s_1 and s_3 are complementary to each other, and s_4 remains in the high state. Second, when the voltage is negative and the current flows in the positive direction, D_2, D_3, and T_4 conduct the current. During this interval, the switching signals s_2 and s_4 are complementary to each other, and s_3 remains in the high state. Furthermore, the analytical formulas of the RMS and average current for the transistors and diodes during the positive half-cycle of u_a are provided in the following section.

The instantaneous current through each component of S_A depends on the modulating signal d_a and the current i_a, as assumed in equations 3.5 and 3.7, respectively. The formulas of the average and RMS currents are determined for the global interval of conduction for each component. First, the instantaneous current equation is written in terms of θ, and then the integrals are applied. Furthermore, the complex integrals are solved using the mathematical solver tool of MATLAB and the resulting equations are documented in terms of power factor angle ϕ, current amplitude $\hat{I}$, and modulation index M.

The instantaneous current through T_1 is

$$\begin{aligned} i_{T_1}(\theta) &= d_a \cdot i_a \\ &= M \sin(\theta) \cdot \hat{I} \sin(\theta - \phi) \end{aligned} \tag{3.19}$$

The transistor T_1 conducts when the voltage u_a is positive and the flow of the current i_a is out of the terminal A i.e., $\phi \leq \theta \leq \pi$. Hence, the average and RMS current equations for this transistor are

$$I_{T_1 avg} = \frac{1}{2\pi} \int_{\phi}^{\pi} M \sin(\theta) \cdot \hat{I} \sin(\theta - \phi)\, d\theta \tag{3.20}$$

$$I_{T_1 RMS} = \sqrt{\frac{1}{2\pi} \int_{\phi}^{\pi} M \sin(\theta) \cdot \hat{I}^2 \sin^2(\theta - \phi)\, d\theta} \tag{3.21}$$

The integral in 3.20 is evaluated to get the average current through T_1

$$I_{\mathrm{T_1avg}} = \frac{\hat{I}M\sin\phi + \pi\cos\phi - \phi\cos\phi}{4\pi} \tag{3.22}$$

The integral in 3.21 is evaluated to get the RMS current through T_1

$$I_{\mathrm{T_1RMS}} = \hat{I}(\cos\phi + 1)\sqrt{\frac{M}{6\pi}} \tag{3.23}$$

The equations 3.22 and 3.23 are also valid for the transistor T_2 and the conduction interval in this case is $\pi + \phi \leq \theta \leq 2\pi$.

During the positive cycle of i_a, when the transistor T_1 is in the off state, the current flows through the transistor T_4 and the diode D_3. To compute the current formulas for these components of the inner leg, the interval is divided further into ϕ to π and π to $\pi + \phi$ and the instantaneous current is written as

$$i_{\mathrm{T_4}}(\theta) = i_{\mathrm{D_3}}(\theta) = \begin{cases} (1 - d_\mathrm{a}) \cdot i_\mathrm{a}, & \phi < \theta < \pi \\ (1 + d_\mathrm{a}) \cdot i_\mathrm{a}, & \pi < \theta < \pi + \phi \end{cases} \tag{3.24}$$

The average current through the inner leg is

$$I_{\mathrm{T_4avg}} = I_{\mathrm{D_3avg}} = \begin{cases} \frac{1}{2\pi}\int_\phi^\pi (1 - M\sin(\theta)) \cdot \hat{I}\sin(\theta - \phi)\, d\theta, & \phi < \theta < \pi \\ \frac{1}{2\pi}\int_\pi^{\pi+\phi} (1 + M\sin(\theta)) \cdot \hat{I}\sin(\theta - \phi)\, d\theta, & \pi < \theta < \pi + \phi \end{cases} \tag{3.25}$$

and the RMS current is

$$I_{\mathrm{T_4RMS}} = I_{\mathrm{D_3RMS}} = \begin{cases} \sqrt{\frac{1}{2\pi}\int_\phi^\pi (1 - M\sin(\theta)) \cdot \hat{I}^2\sin^2(\theta - \phi)\, d\theta}, & \phi < \theta < \pi \\ \sqrt{\frac{1}{2\pi}\int_\pi^{\pi+\phi} (1 + M\sin(\theta)) \cdot \hat{I}^2\sin^2(\theta - \phi)\, d\theta}, & \pi < \theta < \pi + \phi \end{cases} \tag{3.26}$$

The integral in 3.25 is simplified to get the average current through the inner leg.

$$I_{\mathrm{T_4avg}} = I_{\mathrm{D_3avg}} = \frac{\hat{I}(M\phi\cos\phi - M\sin\phi + 2)}{2\pi} - \frac{\hat{I}M\cos\phi}{4} \tag{3.27}$$

The integral in 3.26 is simplified to get the RMS current through the inner leg.

$$I_{T_4RMS} = I_{D_3RMS} = \frac{\hat{I}}{2\sqrt{3}}\sqrt{3 - (3 + \cos(2\phi)) \cdot \frac{2M}{\pi}} \tag{3.28}$$

The average and RMS current equations for the transistor T_4 and the diode D_3 can also be used for the components that take part during the negative cycle of i_a. These components are the transistor T_3 and the diode D_4 and for the analytical calculation the interval can be divided into $\pi + \phi$ to 2π and 0 to ϕ.

The free-wheeling diode with the outer leg transistor only takes part in the conduction of the current when the voltage u_a and the current i_a are not in phase. The average andRMS currents for these diodes can also be formulated, below is the derivation for D_2 that conducts when the output current is positive and line voltage is negative. The instantaneous current through D_2 is

$$\begin{aligned} i_{D_2}(\theta) &= -d_a \cdot i_a \\ &= -M\sin(\theta) \cdot \hat{I}\sin(\theta - \phi) \end{aligned} \tag{3.29}$$

It has to be integrated over the interval of $\pi \leq \theta \leq \pi + \phi$ and the average and the RMS currents with integration limits are

$$I_{D_2avg} = \frac{1}{2\pi}\int_{\pi}^{\pi+\phi}(-M\sin(\theta)) \cdot \hat{I}\sin(\theta - \phi)\, d\theta \tag{3.30}$$

$$I_{D_2RMS} = \sqrt{\frac{1}{2\pi}\int_{\pi}^{\pi+\phi}(-M\sin(\theta)) \cdot \hat{I}^2\sin^2(\theta - \phi)\, d\theta} \tag{3.31}$$

The integrals in 3.30 and 3.31 are simplified to

$$I_{D_2avg} = \frac{\hat{I}M}{4\pi} \cdot (\sin\phi - \phi\cos\phi) \tag{3.32}$$

$$I_{D_2RMS} = \hat{I}\sqrt{\frac{M(\cos\phi - 1)^2}{6\pi}} \tag{3.33}$$

Similarly, the diode D_1 conducts when the voltage u_a is positive and the current i_a is negative. The interval of conduction for D_1 is equal to ϕ. The average and RMS current for D_1 can be formulated as in the equations 3.32 and 3.33 respectively.

As shown in previous section, a simulation model can be used to validate the above documented formulas. The same MATLAB model of T-type NPC is used with a step size of 50 ns, and the parameters are set as, $M = 1$, $\phi = \frac{\pi}{6}$, and $\hat{I} = \sqrt{2} \cdot 500$ A. The average and RMS currents are computed using simulation data and also calculated analytically. The comparison is shown in the Table 1 in terms of the relative error. It can be seen that the percentage in error is very small, thus the above stated equations are driven correctly.

The analysis in the above sections has assumed the sinusoidal PWM. Such analysis is not commonly found in the literature. Furthermore, this analysis can be extended to other advanced modulation techniques, such as SVM. By using these modulation schemes, the modulation index can be increased, and the power losses of the converter can be reduced, although this requires more computation [24]. The analytical analysis of the three level inverter is not performed with SVM in this thesis. However, during the research, models were developed to compare the power losses of two different types of SVM techniques, i.e., the standard and the 60° clamped. The results of the simulations are shown in the Appendix A of the thesis. Moreover, in this chapter, it has been shown that the current through each component of the power converter can be found analytically, and

	Analytical / A	**Simulation / A**	**Relative error / %**
$I_{T_1 avg}$	155.7125	155.216	5.8×10^{-5}
$I_{T_1 RMS}$	303.9149	303.9252	3.3×10^{-5}
$I_{T_4 avg} / I_{D_3 avg}$	66.7472	66.7452	3.0×10^{-5}
$I_{T_4 RMS} / I_{D_3 RMS}$	176.3310	179.3243	3.7×10^{-5}
$I_{D_2 avg}$	2.6194	2.6211	6.5×10^{-5}
$I_{D_2 RMS}$	21.8201	21.8195	2.8×10^{-5}

Table 1: Comparison of the simulation calculations with the analytical calculations

such equations can be used for the analytical calculation of the power losses of the components. Also, it is very useful in the selection of the components with the required power ratings.

4

DIGITAL CURRENT OBSERVER

The current measurement methods for power converters based on the half-bridge are briefly discussed in Chapter 2. An efficient, isolated, and low-cost current measurement can be achieved using two CT sensors in series with each transistor of the half-bridge. However, this approach has the major drawback of introducing the parasitic inductance in the commutation loop, which causes high voltage spikes across the power switches during commutation.

The high switching frequency converters based on GaN or SiC require a very small stray inductance in the commutation path. Because a slight increase in the inductance in the path of the high $\frac{di}{dt}$ current can cause a large voltage spike, potentially damaging the power electronic switch. Therefore, using two magnetic components (CTs) for current measurement is challenging when operating the modern devices at higher frequencies.

As, the size and cost of the inductor decrease with the increase in the switching frequency, and this also increases the power density of the converter. To fully leverage the advantages of the modern devices, the current measurement need to be improved to minimize the negative impact on the switching characteristics of the switches. This can be achieved by eliminating one of the transformer sensors and implementing a current observer to estimate the entire inductor current.

In this chapter, a novel simple-to-implement digital current observer is explained with the help of a boost converter. Furthermore, the modules of the DSP are also discussed that need to be configured for the digital implementation.

4.1 PRINCIPLE OF OPERATION

In this section, the physical equations for the current observer are derived by assuming the half-bridge in the boost configuration as shown in Figure 4.1.

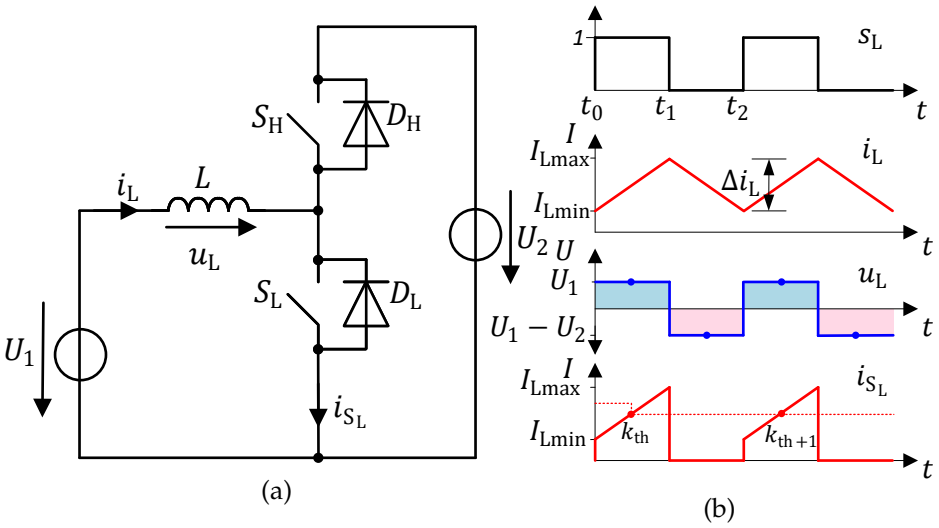


Figure 4.1: (a) boost converter (b) Curves of voltage and current for two switching cycles

Here the inductor voltage measurement and the current sensor in series with the low-side switch S_L is not shown for simplicity. The voltage across the inductor u_L can be measured with auxiliary windings and the current i_{S_L} can be measured with a current transformer sensor. In Figure 4.1(b) the physical voltage and current are shown. For the digital implementation, these quantities are scaled down to the voltage range of the input pins of the digital signal processor.

The switches in the half-bridge are switching complementary, i.e, the switching states are opposite to each other. Consequently, the inductor voltage u_L also changes the states during one switching period [c.f. Fig 4.1(b)]. This voltage can be written for each switching state as follow.

$$u_L(t) = L \cdot \frac{di_L(t)}{dt} \tag{4.1}$$

For $s_L = 1$

$$\begin{aligned} U_1 &= L \cdot \frac{\Delta i_L}{t_1 - t_0} \\ \Delta i_L &= \frac{U_1}{L} \cdot (t_1 - t_0) \end{aligned} \tag{4.2}$$

For $s_L = 0$

$$\begin{aligned} U_1 - U_2 &= L \cdot \frac{\Delta i_L}{t_2 - t_1} \\ \Delta i_L &= \frac{U_1 - U_2}{L} \cdot (t_2 - t_1) \end{aligned} \tag{4.3}$$

If U_1 and U_2 are assumed constant for each switching instant, then the current ripple Δi_L remains the same during the turn-on and the turn-off duration of the switch S_L. Furthermore, in equations 4.2 and 4.3 the product of the voltage and the time is required to compute the current ripple. This product is positive for $s_L = 1$ and it is negative for $s_L = 0$. For the implementation of the current observer in the digital domain, the volt-second product is estimated using the peripheral modules of the DSP. It is further explained in the next sections of this chapter.

The current through the switch S_L flows only when it is conducting and is represented by i_{S_L}. This current can be measured using the CT sensor and the output of the sensor can be sampled at the center of the conduction interval (marked with the red dot on i_{S_L} curve). For CCM and boundary conduction mode (BCM) operation, sampling i_{S_L} provides the average inductor current for one switching interval. Furthermore, the sampled value is used to find the maximum 4.4 and minimum 4.5 values of i_L.

$I_{Lmax,k}$ for the k^{th} interval can be written as

$$\begin{aligned} I_{Lmax,k} &= \frac{\Delta i_L}{2} + i_{S_L,k} \\ I_{Lmax,k} &= \frac{U_{1,k}}{L} \cdot \frac{(t_1 - t_0)}{2} + i_{S_L,k} \end{aligned} \tag{4.4}$$

$I_{Lmin,k}$ for the k^{th} interval can be written as

$$\begin{aligned} I_{Lmin,k} &= \Delta i_L + I_{Lmax,k} \\ I_{Lmin,k} &= \frac{U_{1,k} - U_{2,k}}{L} \cdot (t_2 - t_1) + I_{Lmax,k} \end{aligned} \tag{4.5}$$

The equations 4.4 and 4.5 are derived by assuming the physical inductor voltage and current. These equations form the basic version of the observer for the inductor current in the physical domain. For the implementation in the DSP, the conversion and proportionality constants need to be considered. In DCM operation, the regular sampled value of i_{S_L} does not give the average value, therefore, in the control algorithm a current sample correction block is required in the control algorithm. The topic of sample correction and the operation of the digital current observer in DCM is explained in Chapter 6. Further in this chapter the realization of the current observer in the digital domain is discussed.

4.2 DIGITAL VOLTAGE-TIME PRODUCT ESTIMATION

The challenging step in the implementation of the digital current observer for the half-bridge circuit is the integration of the inductor voltage for each switching interval. While it is possible to implement the integral in the analog domain, this approach requires space on the PCB and introduces additional delays from the analog circuits. Since the modern converters primarily use the low-cost DSPs for firmware and control, the goal is to utilize more resources from these processors to estimate the area under curve of the inductor voltage.

4.2.1 *Required digital signals*

For the digital estimation of the voltage-time product, the voltage across the inductor u_L should be scaled down to the voltage range of the input pins of the DSP. This can be accomplished with the secondary windings over the main inductor. The output voltage curves of the auxiliary windings are shown in Figure 4.2. The signals u_{LADC1} and u_{LADC2} provide the scaled-down u_L voltage for T_e and T_a intervals respectively. The turns ratio for these windings should be same and the stepped-down voltage signals should not exceed the allowed maximum voltage of the analog input pins of the DSP. The signals are then regularly sampled to ascertain the voltage across the inductor.

The other two signals u_{LCAP1} and u_{LCAP2}, are used to record the duration of the time intervals T_e and T_a. These signals are the input

to the capture modules of the digital signal processor. The number of turns for these windings can be different from the windings used to estimate the voltage across the inductor. Moreover, an offset U_{off} is also added to the output of these windings. The offset is required for the capture module so that the module can identify the rising and falling edges of the input pulses.

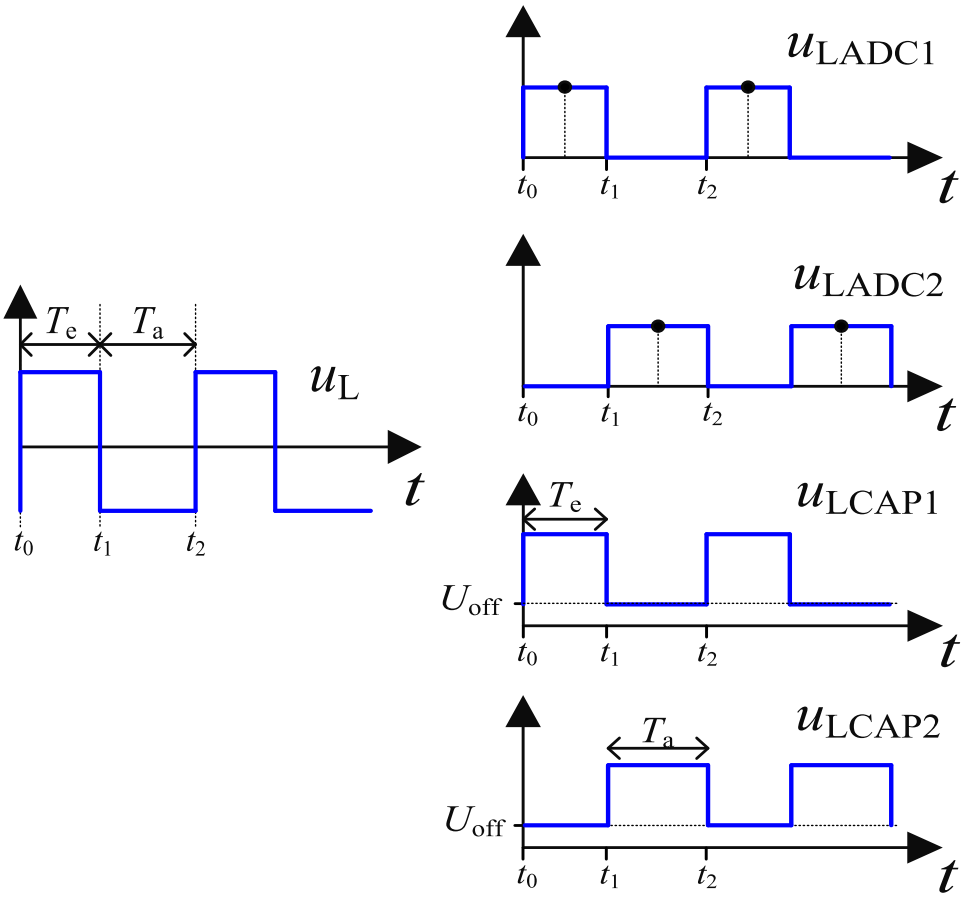


Figure 4.2: Inductor voltage measurement for capture modules

Hence, from these signals, the voltage and the time for equations 4.4 and 4.5 can be estimated digitally. The following sections of this chapter further discuss the working and the configuration of the analog-to-digital conversion and time capture modules of the digital signal processor.

4.3 INDUCTOR VOLTAGE SAMPLING

The analog-to-digital conversion module of the DSP can be configured in various ways to sample the input signal [25]. In power electronics, the sampling instant of the input pulse signal is synchronized with carrier signal of the pulse width modulation module of the DSP [26]. The three different cases that are generally used for sampling are represented in Figure 4.3 and are explained below.

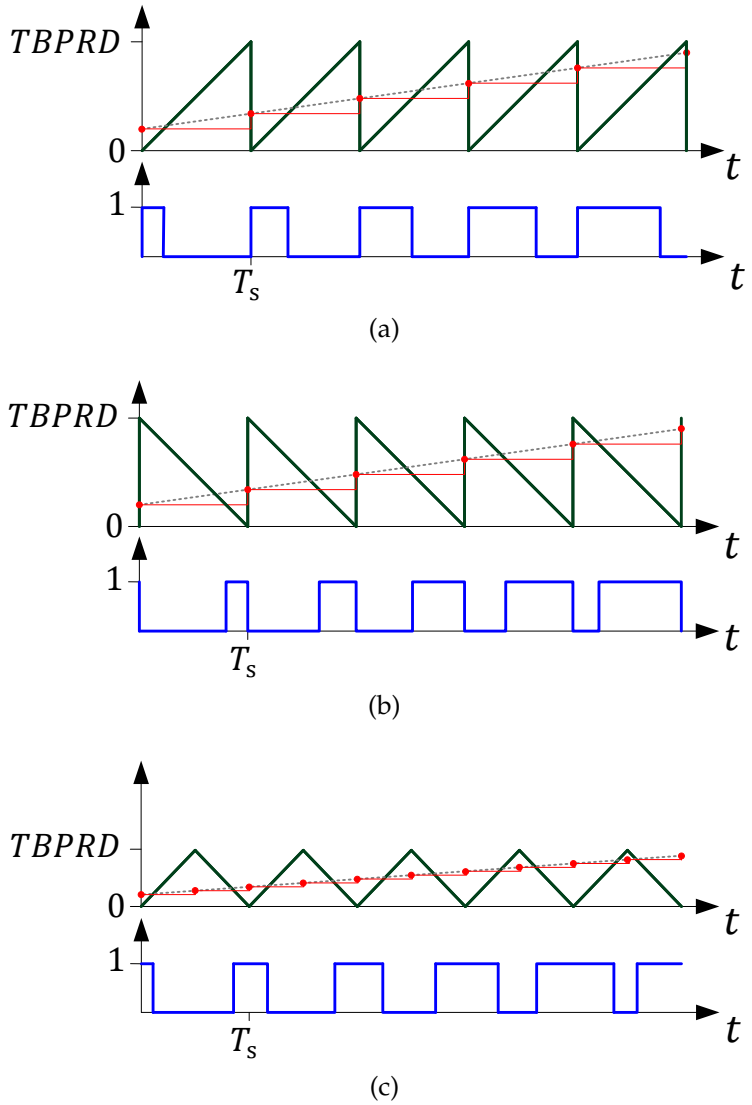


Figure 4.3: Regular sampling in a digital circuit (a) with up-counter (b) with down-counter (c) with up-down counter

In the digital domain, the carrier signal of the PWM block is assumed with a fast counter. The maximum value of the counter, $TBPRD$, is defined based on the required switching frequency f_s of the PWM and the frequency of the clock signal f_{clk} of the PWM. In the figures above, the green curve represents the fast counter (carrier), the dotted line represents the input signal at the analog to digital conversion (ADC) pin, which is sampled and acts as modulating signal (shown as red curve). The blue curve represents the pulse width modulated signal. For the positive slope [c. Fig.4.3(a)] and the negative slope [c. Fig.4.3(b)] counters the relation between the two frequencies is given below.

$$f_{clk} = (TBPRD + 1) \times f_s \tag{4.6}$$

For the up-down counter [c. Fig.4.3(c)]

$$f_{clk} = 2 \times TBPRD \times f_s \tag{4.7}$$

In the case of the positive slope counter, the counter counts up to the defined $TBPRD$ value and then resets to zero. In the case of the negative slope counter, the counter counts down to zero and resets to the defined $TBPRD$ value. With these counters, the input signal can be regularly sampled at the reset instant. Therefore, in the up-counter, the ADC input signal is sampled at the rising edge of the PWM signal, and in the down-counter, it is sampled at the falling edge of the PWM signal. The sampled value is held until the next sampling instant.

In case of the up-down counter, the regular sampling instant can be either set to the maximum value of the counter, the zero value of the counter, or both. Therefore, the sample of the analog signal can be taken at the middle of the high state and the low state of the PWM signal. This results in more reliable sample, as the noise at the switching instants can be avoided.

From the above discussion, it can be concluded that the physical inductor voltage u_L shown in the above figure 4.2 can be estimated in both intervals. First, the sampling is synchronized with the up-down counter of the PWM module. Then, the signals u_{LADC1} and

u_{LADC2} can be sampled at the center of the T_{e} and T_{a} intervals. The proportionality constant, which is the turn ratio, should be used for the digital implementation of the current observer equations.

4.4 TIME CAPTURE MODULES

The signals u_{LCAP1} and u_{LCAP2} from the auxiliary windings are further used to estimate the duration of T_{e} and T_{a} time intervals [c.Fig. 4.2]. This is possible by using the time capture modules present in the digital signal processor. These modules have the configurable fast counters, such that when a pulse train signal is applied to the input of the module, it returns the number of clocks for which the input signal stays high (3.3 V) or low (0 V) [27]. Hence, the time intervals $(t_1 - t_0)$ and $(t_2 - t_1)$ in equations 4.4 and 4.5 are estimated digitally in terms of the number of clock cycles between the rising and falling edges of u_{LCAP1} and u_{LCAP2}. The frequency of the clock signal of the capture module can also be assumed as f_{clk} similar to that of the PWM module.

The time capture modules are present in almost every digital signal processor. In this work, the DSP based on *C*2000 real-time microcontroller from TI is used, as it is familiar in the power electronic industry and also finds various applications in the electrical drives [28]. These microcontrollers offer enhanced control peripherals that possess high frequency counters. The counter variables can be read either by generating special interrupts or by simply configuring the modules.

The enhanced peripherals that are present in the TI's DSP that can be configured as the capture modules are

- enhanced capture (eCAP) module
- high-resolution input capture (HRCAP) module
- enhanced quadrature encoder pulse (eQEP) module

The number of these modules varies from one DSP to another. In the low-cost basic controller, at least one eCAP or one eQEP module is present. In the upper basic models (still low-cost), more than one of

each module is present. A short comparison between three DSPs is represented in the Table 2.

Digital signal processor	Modules	Quantity
TMS320F28027	eCAP	1
TMS320F28035	eCAP	1
	HRCAP	1
	eQEP	1
TMS320F28069	eCAP	3
	HRCAP	2
	eQEP	4

Table 2: Comparison of capture modules in TI's mircrocontrollers

The input to these modules is selected by programming the general purpose input output (GPIO) pins of the digital signal processor. The basic structure and configuration of each module is discussed below.

4.4.1 *Enhanced capture module*

This module is used for the measurement of the time between the events of a pulse train input signal. For example, speed and position measurement sensors (e.g., incremental encoder) output the pulse train signals that can be decoded with this module. Furthermore, in current and voltage measurement techniques, modulators are used such as delta-sigma modulator. In this case, the duty cycle of the output signal is proportional to the value of the sensed quantity; hence, the width of the pulse can be found with the eCAP module. The basic structure of the eCAP module is shown in Figure 4.4. In this module, the fast counter is named as time-stamp counter register (TSCTR), which can be synchronized with the digital signal *SyncIn*. Moreover, when this counter overflows, it resets to zero.

From the above figure, the configuration steps of the eCAP module can be explained in simple word as below.

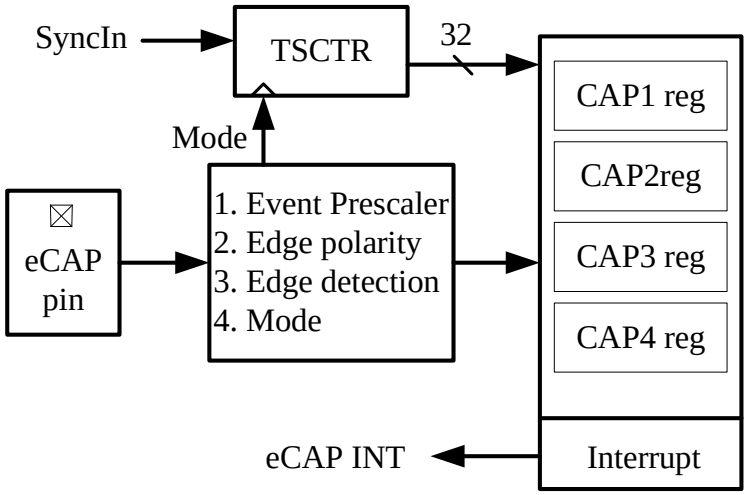


Figure 4.4: eCAP function diagram

1. Configuration of the GPIO pin for the capturing module and enabling the clock of the module.
2. The input signal can be prescaled in the multiples of 2 or it can be bypassed completely.
3. The capture event (CEVT) is defined for each of the capture registers $CAPx$. It is either the rising edge event or the falling edge event of the input pulse signal. Moreover, in the eCAP module, four capture registers are present, and two of them are assumed for Figure 4.5.
4. The mode defines the basic function of the module. It can be set either to get the absolute value of the TSCTR at the defined events or to get the difference of the number of clocks between the events (delta-mode).
5. Based on the requirement of the interrupt service routine, the interrupt can be generated at the capture events. However, the interrupt is not necessary to read the $CAPx$ registers.

If u_{LCAP1} is assumed to be the input of the eCAP module and it is required to find the time T_{e}, i.e, for which the u_{L} stays positive, then the capture module has to be configured in delta-mode, as explained in Figure 4.5. In this mode, the 32-bit counter $TSCTR$ resets after each defined event. The *MOD counter* counts the number of events,

and to use two capture events for $CAP1$ and $CAP2$ registers, it counts up to 1 and then resets. To use all four capture registers, it is set to 3. If $CAP1$ is defined for the falling edge event and $CAP2$ is defined for the rising edge event, then $CAP1$ stores the $TSCTR$ value for the time interval in which u_{LCAP1} is high. Furthermore, the figure displays the operation for two switching periods where $CAP1$ returns C_1, the number of clock cycles for T_{e} intervals, and $CAP2$ returns the number of clock cycles for T_{a} intervals. From this capture module only the variable C_1 corresponding to T_{a} interval is used for the digital current observer algorithm. Similarly, the signal u_{LCAP2} is used as the input for the other available capture module, and from this module, only the variable C_2 corresponding to T_{a} interval is determined. The reason to use two capture modules is to estimate the duration of all switching states of the half-bridge. Here, only the continuous conduction mode is assumed and the estimation of the time duration is possible with only one capture module. However, it is not efficient when the half-bridge is operating in discontinuous conduction mode. This is discussed further where the current observer concept is implemented for the power factor correction rectifiers.

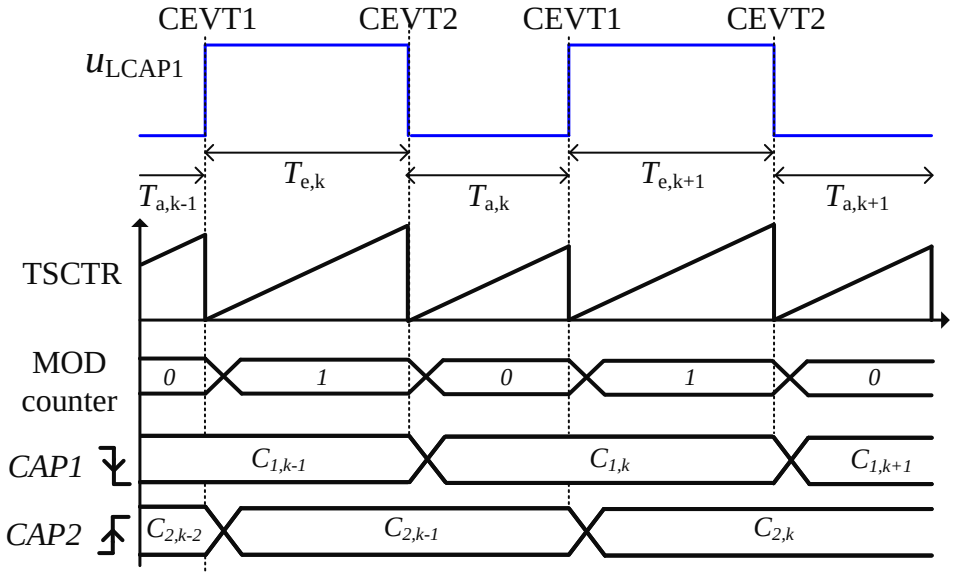


Figure 4.5: eCAP operation in delta-mode

4.4.2 *High-resolution capture module*

The function and application of this module are similar to the eCAP, but it can also be configured for the high resolution (i.e., hundreds of picoseconds). However, it works only in the delta-mode and returns the number of clock cycles between the rising and falling events. The high resolution is provided by an additional calibration logic block that is internally connected to the high-resolution pulse width modulation (HRPWM). This module can be clocked asynchronously or synchronously to the digital signal processor clock. When operating with the DSP clock, it operates in the normal capture mode and has the resolution of $+/-1$, as in case of the eCAP module. For the operation in high-resolution capture mode, it needs to be clocked asynchronously. Moreover, to read the counter register of this capture module, the program code does not require special interrupt, similar to the eCAP module. The major difference from the previous module is that here the counter registers are 16-bit in length. Furthermore, details about the structure can be found in the reference manual [28].

4.4.3 *Enhanced quadrature encoder pulse module*

The primary function of this module is to estimate the position, direction, and speed of a rotating machine. The output of a linear or rotary incremental encoder placed at the shaft of the machine can be interfaced with the eQEP module of the digital signal processor. This module consists of mainly three blocks: quadrature decoder unit (QDU), position counter control unit (PCCU), and quadrature capture unit (QCAP), as shown in Figure 4.6. The inputs to this module are the quadrature signals named as QA and QB (two square pulse signals with a 90° phase difference) and an index signal QI which indicates one complete revolution of the shaft. Further details of this module can be found in the handout from TI [29]. This module can also be configured as a time capture unit as discussed below.

In this case, there is one input pulse train signal which can be assigned to QA. The other inputs QB and QI, are set to zero potential. The QDU generates the quadrature clock (QCLK) from the QA input. The clock is generated on each of the rising and falling edge of QA.

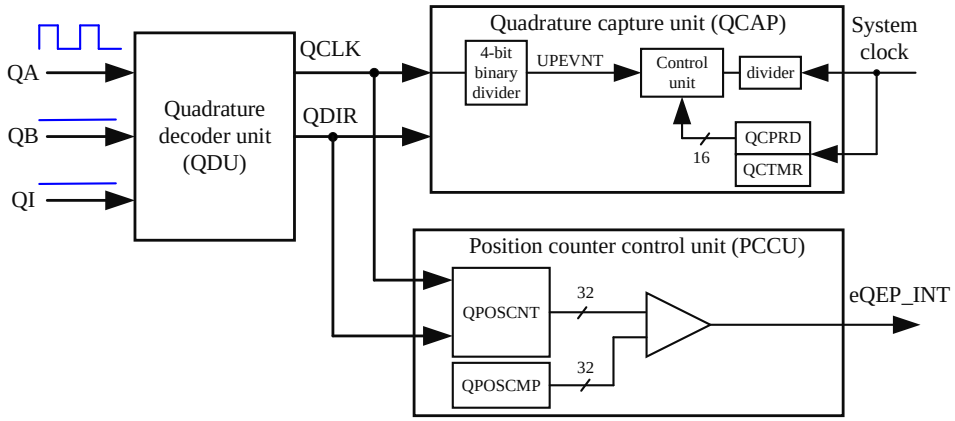


Figure 4.6: eQEP main building blocks

The clock signal is further an input to the position counter control unit and the quadrature capture unit. In QCAP, the unit position event (UPEVNT) is generated from QCLK via binary divider. Moreover, it also contains a 16-bit capture timer (QCTMR) that is synchronized with the system clock. The value of the timer is stored in capture period register (QCPRD) on every UPEVNT inside the control unit. To estimate the period of the input signal, the UPEVNT is generated after every second QCLK pulse, and the timer value is stored in the 16-bit QCPRD register. This value corresponds to the the clock cycles present in one complete switching period T_S.

The PCCU block is further utilized for the estimation of the pulse width. It has a position counter (QPOSCNT) increments or decrements based on the QCLK pulses and the quadrature direction (QDIR). Here, direction is of no importance as QB is at zero potential. The maximum value for the position counter is set to 1; therefore, it counts only $0-1-0-1$... and so on. Furthermore, the output of QPOSCNT is compared with the value stored in the quadrature position compare (QPOSCMP) register. It is set to 0 such that every time when QPOSCNT is equal to zero it generates an interrupt and the QCTMR value can be read at this instant. The timer value at the interrupt corresponds to the number of clock cycles counted for the width of the input pulse. Hence, eQEP is configured as a time capture module [30].

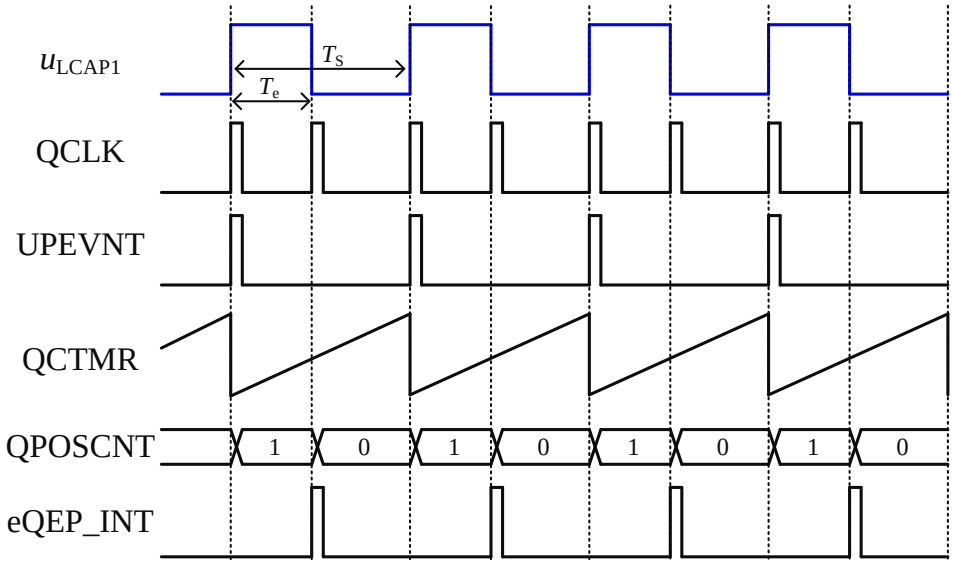


Figure 4.7: eQEP operation as a time capture module

The operation of eQEP module as a time capture is displayed in Figure 4.7. The input QA can be assumed to be either u_{LCAP1} or u_{LCAP2} [c.fig 4.4]. QCLK from the decoder is generated on each edge of the input signal. It passes through the divider in QCAP and gives unit position event pulses. At each UPEVNT pulse, the timer value is stored in QCPRD register, and this estimates the number of clock cycles in the T_S interval. For the pulse width estimation, an interrupt must be generated with position compare unit present in PCCU. At the interrupt instant, QCTMR counter value corresponds to the number of clock cycles in the T_e interval.

A short comparison between the modules is given in Table 3. The use of eCAP for time estimation is preferred because it is easy to configure and does not require any interrupt to read the capture registers. Moreover, for the practical verification of the current observer two enhanced capture modules are used. An analog circuit is required to get the signals for the capture modules and the ADC inputs. For the capture modules, the input signal must have a minimum difference of 1.5 V between the two edges. Therefore, in the practical implementation, four signals are generated from the secondary windings of

	eCAP	**HRCAP**	**eQEP**
Initialization	simple	moderate	complex
Interrupt	no	no	yes, for T_e estimation
Accuracy	± 1	± 1 (normal mode)	± 20 (requires correction)

Table 3: Comparison of the capture modules

the inductor: two for time capturing and two to sample the inductor voltage for each switching state.

5

IMPLEMENTATION OF DIGITAL CURRENT OBSERVER FOR DC-DC CONVERTER

In the previous chapter, the digital current measurement method based on the observer concept has been introduced. This method, grounded in its operational principles and the necessary software and hardware requirements, can be implement to various DC-DC converters, including buck, boost, and buck-boost converters.

In this chapter, the implementation of the digital current observer is focused for a boost converter. The chapter begins with an overview of the boost converter, followed by the derivation of the digital equations for the current observer. Additionally, the closed-loop control with simulation results and experimental results from a self-developed prototype are also presented.

5.1 BOOST CONVERTER

The boost converter, consisting of the half-bridge with two MOSFETs is shown in Figure 5.1. The input voltage U_1 is assumed to be constant. The output voltage U_2 is controlled by the DSP via the switching signals (s_H and s_L). For steady state operation, variations in U_2 can be ignored, and it can also be considered as constant.

In case of the boost operation, the input voltage is smaller than the output voltage ($U_1 < U_2$). The input voltage and the output voltage are measured and fed to the DSP as U_{in} and U_{out}, respectively. The current i_L through the inductor is sensed with a single CT sensor, which is placed in series with the low-side switch and has the output voltage u_M across the burden resistor R_B. The auxiliary windings on the inductor L step down the inductor voltage. Furthermore, the negative polarity from the secondary winding signals is clamped with a diode to get u_{LCAP1}, u_{LCAP2}, u_{LADC1}, and u_{LADC2}. In the figure 5.1, only one secondary winding is drawn for simplicity.

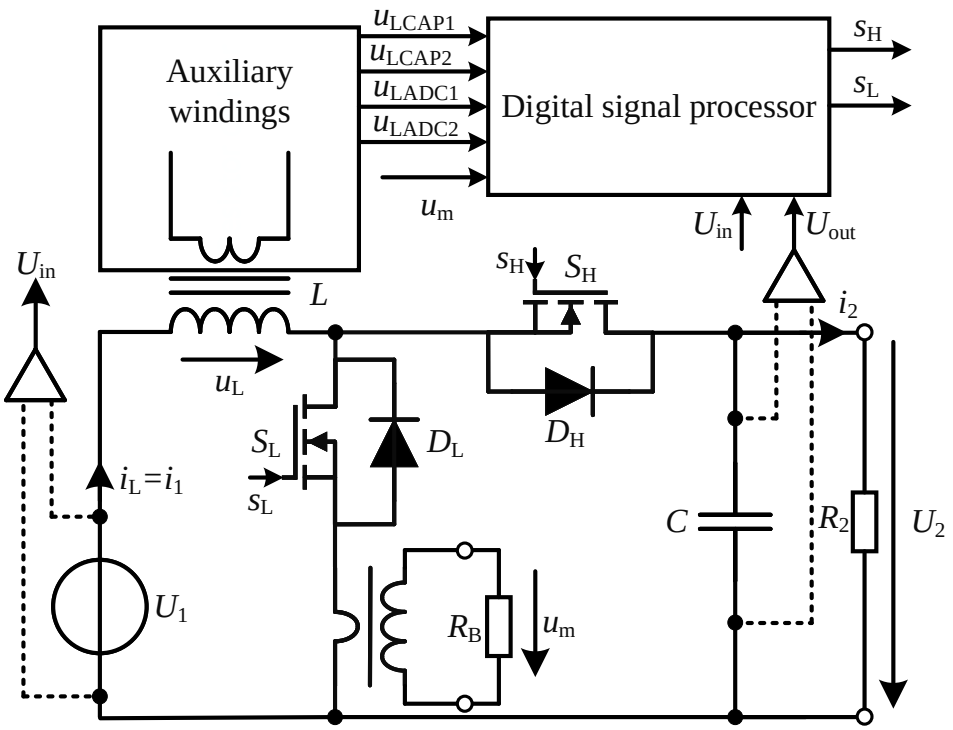


Figure 5.1: Boost converter with one CT and the auxiliary windings on the inductor

The physical inductor voltage and current curves, along with the respective inputs to the DSP, are shown in Figure 5.2. The sampling instants are marked with dotted vertical lines on the ADC inputs of the processor. Moreover, u_{LCAP1} is used to estimate the number of clock cycles during which the inductor current has a positive slope, while u_{LCAP2} is used to estimate the number of clock cycles during which the inductor current has a negative slope. The proportionality constant of the current sensor is K_m, whereas the proportionality constant for the inductor voltage conversion is K_S. This constant is the ratio of N_{S2} , the number of turns of the auxiliary winding of u_{LADC1} (or u_{LADC2}), to N_P, the number of turns of the primary winding of the inductor.

The conduction duration of the switch S_L is T_e and for the S_H it is T_a. Whereas, T_S represents one switching interval. During the steady state operation in CCM the duty cycle D is

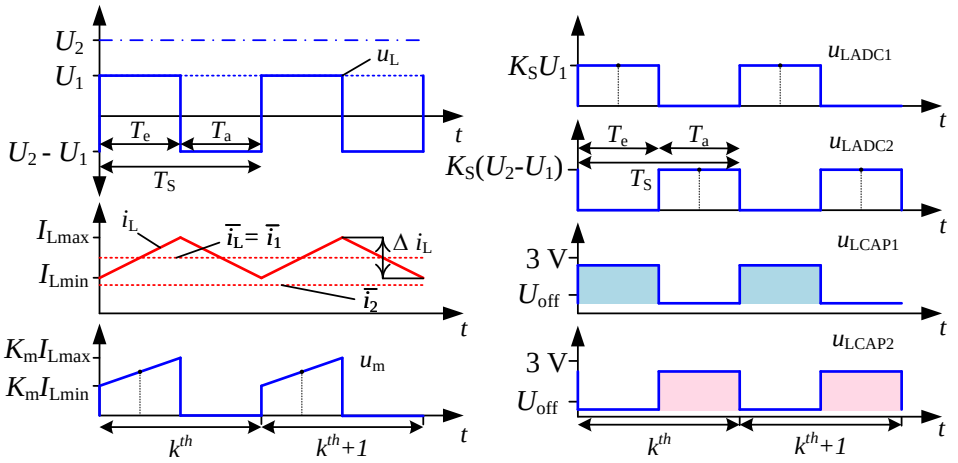


Figure 5.2: Inductor voltage and current curves and the corresponding input voltage signals for the DSP

$$D = \frac{T_e}{T_S} \tag{5.1}$$

Further the voltage ratio is given in Equation 5.2 and the inductor current ripple is given in Equation 5.3

$$\frac{U_1}{U_2} = 1 - D \tag{5.2}$$

$$\begin{aligned} \Delta i_L &= I_{Lmax} - I_{Lmin} \\ \Delta i_L &= D(1-D) \cdot \frac{T_S}{L} \cdot U_2 \end{aligned} \tag{5.3}$$

To estimate the T_e and T_a time intervals, two capture modules are used as proposed in the previous chapter. The capture module with the input u_{LCAP1} provides the estimated number of DSP clock cycles for the T_e interval, while the capture module with the input u_{LCAP2} provides the estimated number of DSP clock cycles for the T_a interval [c.Fig. 5.2]. If C_1 and C_2 represent the outputs of the capture modules with u_{LCAP1} and u_{LCAP2} as inputs, respectively, then

$$\begin{aligned} T_e &= \frac{C_1}{f_{clk}} \\ T_a &= \frac{C_2}{f_{clk}} \end{aligned} \tag{5.4}$$

where f_{clk} is frequency of the DSP clock or the counter clock of the capture module. Furthermore, from the section 4.1, the equations 4.4 and 4.5 can be used to rewrite the equations for the current observer in the digital domain as in 5.5 and 5.6.

$$K_m I_{Lmax,k} = \frac{1}{2} \frac{K_m}{K_S} \frac{u_{LADC1,k}}{L} \frac{C_{1,k}}{f_{clk}} + u_{m,k} \tag{5.5}$$

$$K_m I_{Lmin,k} = -\frac{K_m}{K_S} \frac{u_{LADC2,k}}{L} \frac{C_{2,k}}{f_{clk}} + K_m I_{Lmax,k} \tag{5.6}$$

Moreover, the sample of the output of the current transformer, u_m at the center of T_e interval, gives the mean value of the inductor current for each switching cycle. These sampling instants are indicated with the dotted line in figure 5.2. The variables with the subscript k update after regular intervals, depending on the structure of the DSP algorithm. Furthermore, the computation time of the algorithm can be reduced if the constants are defined only once during initialization.

5.1.1 *Closed-loop control*

The aim of the boost converter is to step up the input voltage U_1 to a higher voltage value of U_2. This can be achieved more simply by adjusting the duty cycle of the converter to a constant value determined by the voltage ratio 5.2. This control structure does not require the measurement of any quantities, making it an open-loop control that inherently does not compensate for external disturbances. Generally, for the dynamic behaviour of the converter, a reliable closed-loop control is needed.

The implementation of the closed-loop control requires the measurement of the input and output voltages, as well as the inductor current. The outputs of the sensors are then used in the feedback loop. Such a control concept is presented in Figure 5.3 and similar control concepts can be found in the literature. It consists of an inner current control loop and an outer voltage control loop. The inner loop is implemented for the average inductor current over a switching interval T_S [31]. For the boost converter shown in 5.2 the inductor current is not measured directly but the CT sensor is assumed in

series with the low-side switch. Hence, the average inductor current is determined by sampling the u_{m} at the center of the pulse. The sampling instants for u_{m}, u_{LADC1} and u_{LADC2} curves are marked with the dotted lines in figures 5.2 and 5.3.

For the operation of the boost converter in the closed loop, the control is implemented in the digital domain. The algorithm is divided into multiple tasks (marked with the dotted rectangles [c.fig 5.3]) and defined as small functions. These functions are called regularly via the interrupt service routine (ISR). These regular ISRs can be generated using the PWM or ADC module, allowing for the updating of variables that record the measurement signals and the capture module signals at each switching frequency. Moreover, depending on the run time of each function, multiple functions can be executed within a single ISR.

The outer loop in the control algorithm consists of the voltage controller. It takes the sampled output voltage $U_{\mathrm{out,ADC}}$ as an input. It further computes the difference with the set reference U^{*}_{out}, which is sent to the PI-controller. This controller generates the reference value u^{*}_{m} for current control. The difference between the reference u^{*}_{m} and the sampled value of the current sensor output $u_{\mathrm{m,ADC}}$ is computed. The current controller takes the difference as input and provides the small signal duty cycle, which then is added to the duty cycle calculated by the feed forward block. The feed forward is implemented using 5.2 and takes sampled values of the input and output voltages ($d_{\mathrm{ff}} = D$). The duty cycle value is then scaled to obtain the modulation signal for the PWM. The low-power pulse width signals generated by the DSP are then fed to the gate driver circuit, which generates s_{H} and s_{L} signals to drive the power transistors.

The current observer block is implemented using 5.5 and 5.6. The constant products $\frac{K_{\mathrm{m}}}{K_{\mathrm{S}}} \cdot \frac{1}{2Lf_{\mathrm{clk}}}$ and $\frac{K_{\mathrm{m}}}{K_{\mathrm{S}}} \cdot \frac{1}{Lf_{\mathrm{clk}}}$ are defined once during the initialization. To validate the results, the estimated maximum, mean and the minimum values of the current observer are communicated and displayed on the oscilloscope using a hardware monitor. The communication is not the necessary part in the algorithm and can be commented out from the code after verification.

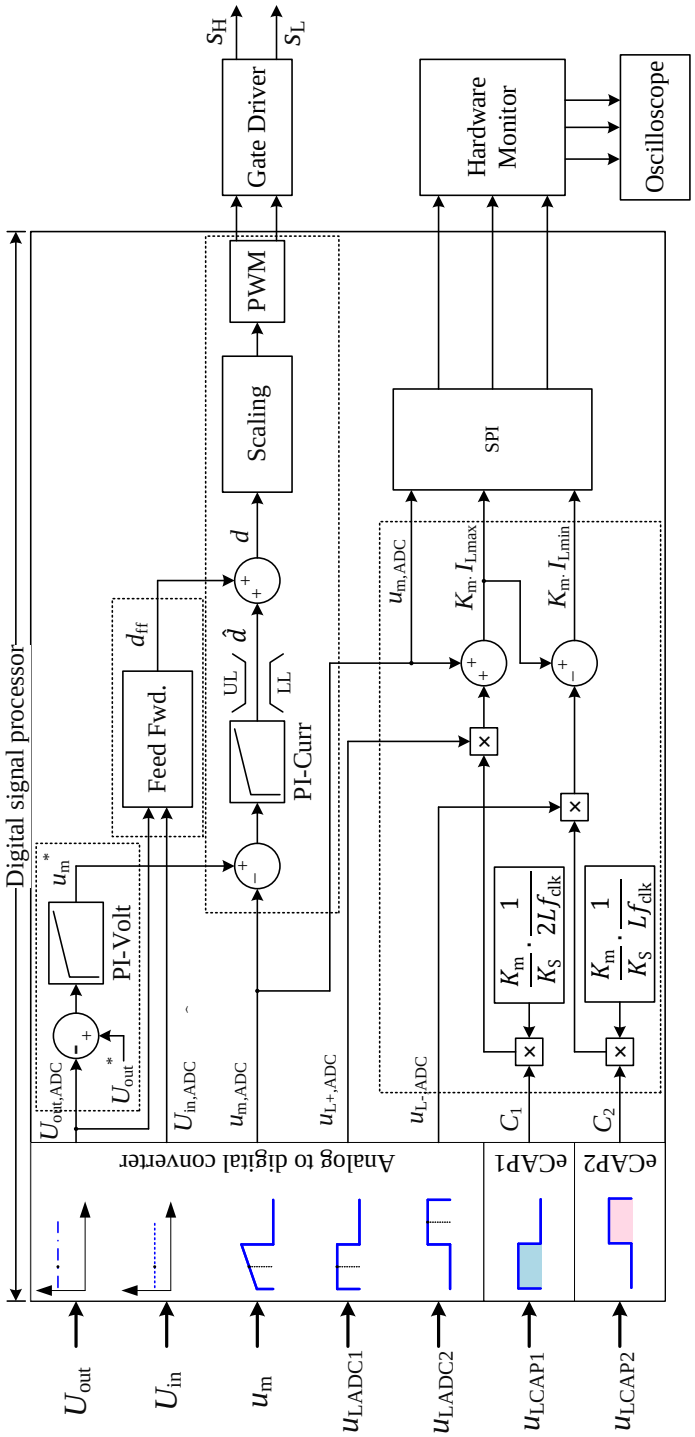


Figure 5.3: Closed-loop control and digital current observer algorithm for a boost converter

5.2 SIMULATION MODEL

The control concept and the digital current observer explained above for the boost converter are verified using a simulation model in MATLAB. The boost converter is assumed for the parameters mentioned in table below.

Input voltage, U_1	$50\,\mathrm{V} - 325\,\mathrm{V}$
Output voltage, U_2	$400\,\mathrm{V}$
Switching frequency, f_S	$100\,\mathrm{kHz}$
Output power, P_2	$1\,\mathrm{kW}$
Boost inductance, L	$219\,\mu\mathrm{H}$
Output Capacitance, C	$780\,\mu\mathrm{F}$

Table 4: Boost converter simulation model parameters

The control design can be initiated with the dynamic averaging of the boost converter. The differential equations of the inductor current and the output voltage for $s_L = 1$ and $s_L = 0$ in CCM are written in Equation 5.7 and Equation 5.8.

$$\begin{aligned} \frac{di_L(t)}{dt}\Big|_{s_L=1} &= \frac{U_1}{L} \\ \frac{di_L(t)}{dt}\Big|_{s_L=0} &= \frac{U_1 - u_2(t)}{L} \end{aligned} \tag{5.7}$$

$$\begin{aligned} \frac{du_2(t)}{dt}\Big|_{s_L=1} &= -\frac{i_2(t)}{C} \\ \frac{du_2(t)}{dt}\Big|_{s_L=0} &= \frac{i_L(t) - i_2(t)}{C} \end{aligned} \tag{5.8}$$

Here it is assumed that the input voltage is constant and can be denoted as U_1. The output voltage $u_2(t)$ and the inductor current $i_L(t)$ are controlled by the duty cycle $d(t)$. Furthermore, high frequency switching details of the state variables can be ignored by considering their average values. Hence, the derivatives of the average inductor current $\bar{i}_L(t)$ and the average output voltage $\bar{u}_2(t)$ can be formulated as in Equation 5.9 and Equation 5.10, respectively.

$$\frac{d\bar{i}_{\mathrm{L}}(t)}{dt} = \frac{1}{L} \cdot (U_1 - (1 - d(t))u_2) \tag{5.9}$$

$$\frac{d\bar{u}_2(t)}{dt} = \frac{1}{C} \cdot (-\bar{i}_2 + (1 - d(t))\bar{i}_{\mathrm{L}}) \tag{5.10}$$

The average output current $\bar{i}_2$ can be replaced by $\frac{\bar{u}_2}{R}$ and the state space equation of the boost converter in CCM can be written as in 5.11.

$$\begin{bmatrix} \frac{d\bar{i}_{\mathrm{L}}(t)}{dt} \\ \frac{d\bar{u}_2(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-d(t)}{L} \\ \frac{1-d(t)}{C} & -\frac{1}{RC} \end{bmatrix} \times \begin{bmatrix} \bar{i}_{\mathrm{L}}(t) \\ \bar{u}_2(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} U_1 \tag{5.11}$$

It shows that the boost converter is non-linear, and it is necessary to linearize the system around a steady-state operating point to obtain the small-signal transfer functions. Furthermore, the constant input voltage is related to the average output voltage as in 5.2 which forms the feed forward block. Hence, 5.9 can be written as:

$$\begin{aligned} \frac{d\bar{i}_{\mathrm{L}}(t)}{dt} &= \frac{1}{L} \cdot ((1 - D)\bar{u}_2(t) - (1 - (D + \hat{d}(t)))\bar{u}_2(t)) \\ \frac{d\bar{i}_{\mathrm{L}}(t)}{dt} &= \frac{\bar{u}_2(t)}{L}\hat{d}(t) \end{aligned} \tag{5.12}$$

The Laplace transformation of the 5.12 equation gives the small signal transfer function of the boost converter that can be written as below.

$$G_{\mathrm{is}}(s) = \frac{\bar{i}_{\mathrm{L}}(s)}{\hat{d}(s)} = \frac{\bar{u}_2}{Ls} \tag{5.13}$$

Hence, the converter acts as an ideal integrator at the chosen operating point. A PI-current controller can be considered as in 5.14. The gain k_{pi} can be determined for the required crossover frequency and phase margin.

$$G_{\mathrm{ic}}(s) = k_{\mathrm{pi}}\frac{1 + sT_{\mathrm{ni}}}{sT_{\mathrm{ni}}} \tag{5.14}$$

The plots in Figure 5.4 show that the gain k_{pi} of the current controller is set such that at the crossover frequency of $\omega_{ci} = 31416\frac{1}{s}$, a phase reserve $\phi_{ci} = 45^\circ$ is achieved for $G_{io}(s) = G_{is}(s) \cdot G_{ic}(s)$, i.e., the gain of the open loop. Further the closed current loop transfer function G_i is needed for the design of the voltage controller and it is written as below.

$$G_i(s) = \frac{G_{io}(s)}{1 + G_{io}(s)} \tag{5.15}$$

The transfer function of the output filter composed of capacitor C and the load resistor R_2 is written in Equation 5.16. Now the plant transfer function for the voltage controller can be determined as in Equation 5.17. Here, the average input voltage $\bar{u}_1$ is equal to the constant DC input voltage U_1.

$$G_{RC}(s) = \frac{\bar{u}_2}{\bar{i}_L} = (1 - d) \cdot \frac{R_2}{1 + sR_2C} \tag{5.16}$$

$$\begin{aligned} G_{us}(s) &= G_i(s) \cdot G_{RC}(s) \\ &= \frac{\bar{u}_1 \cdot R_2 \cdot k_{pi}(1 + sT_{ni})}{(1 + sR_2C)(T_{ni}Ls^2 + \bar{u}_2 k_{pi} T_{ni} s + \bar{u}_2 k_{pi})} \end{aligned} \tag{5.17}$$

A PI-voltage controller can be designed according to the demanded crossover frequency and the phase reserve as it has done for the current controller. The proportional integral controller for the voltage control can be written as in Equation 5.18. A phase reserve $\phi_{cu} = 45^\circ$ is achieved for the open-loop voltage control i.e., $G_{uo}(s) = G_{us}(s) \cdot G_{uc}(s)$ at $\omega_{cu} = 6283\frac{1}{s}$. The control requirements can be changed by varying the gain k_{pu}. The bode plot curves for the voltage control are shown in Figure 5.5.

$$G_{uc}(s) = k_{pu}\frac{1 + sT_{nu}}{sT_{nu}} \tag{5.18}$$

A boost converter with the parameters mentioned in Table 4 is simulated in MATLAB with the closed-loop control as discussed

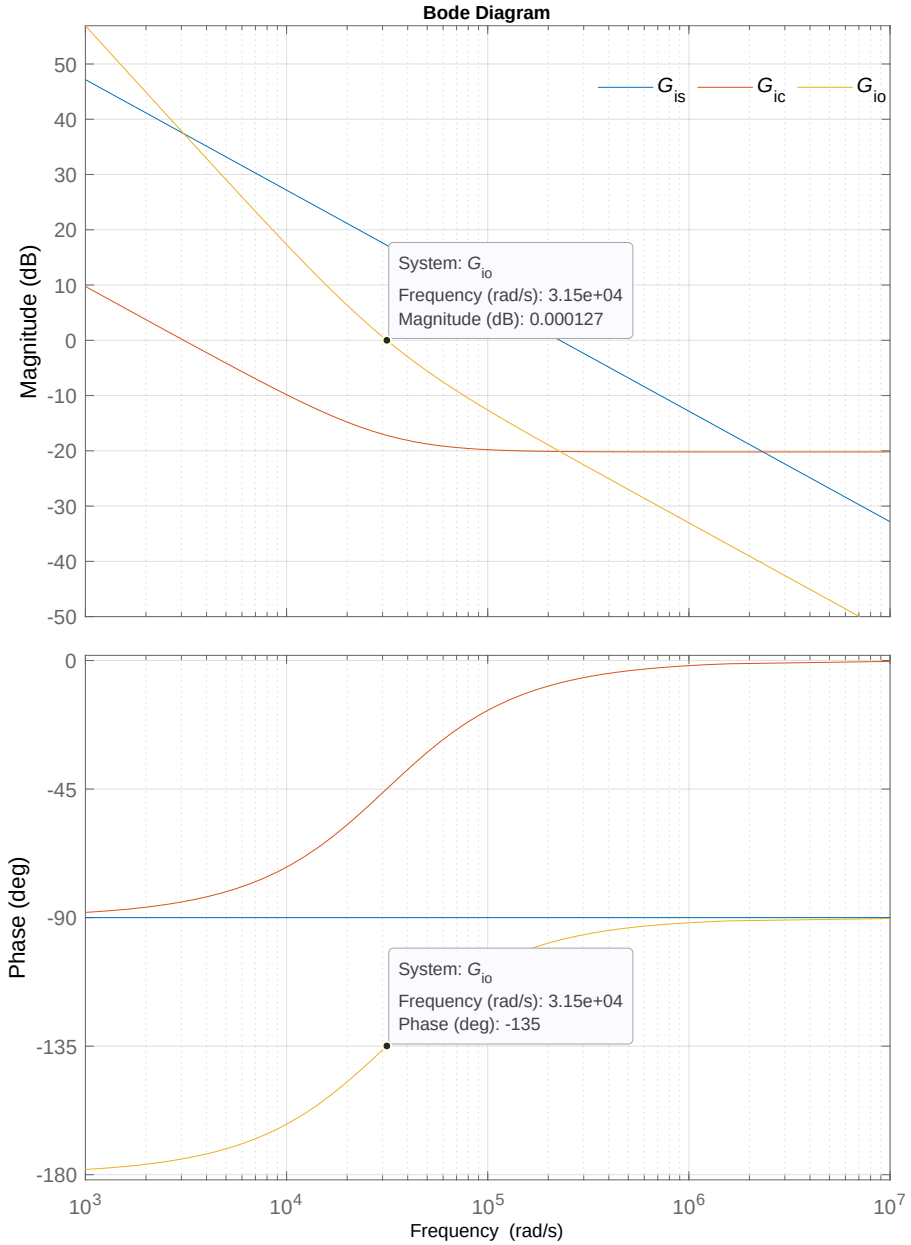


Figure 5.4: Bode plots of G_{is}, G_{ic}, and G_{io}

above. Moreover, the current observer equations are also used for the online estimation of the inductor current. To verify the control algorithm in the simulation model, a change in load is considered at 25 ms of the simulation time. The simulation results are shown in the Figure 5.6 for different input voltages. Further, it shows that

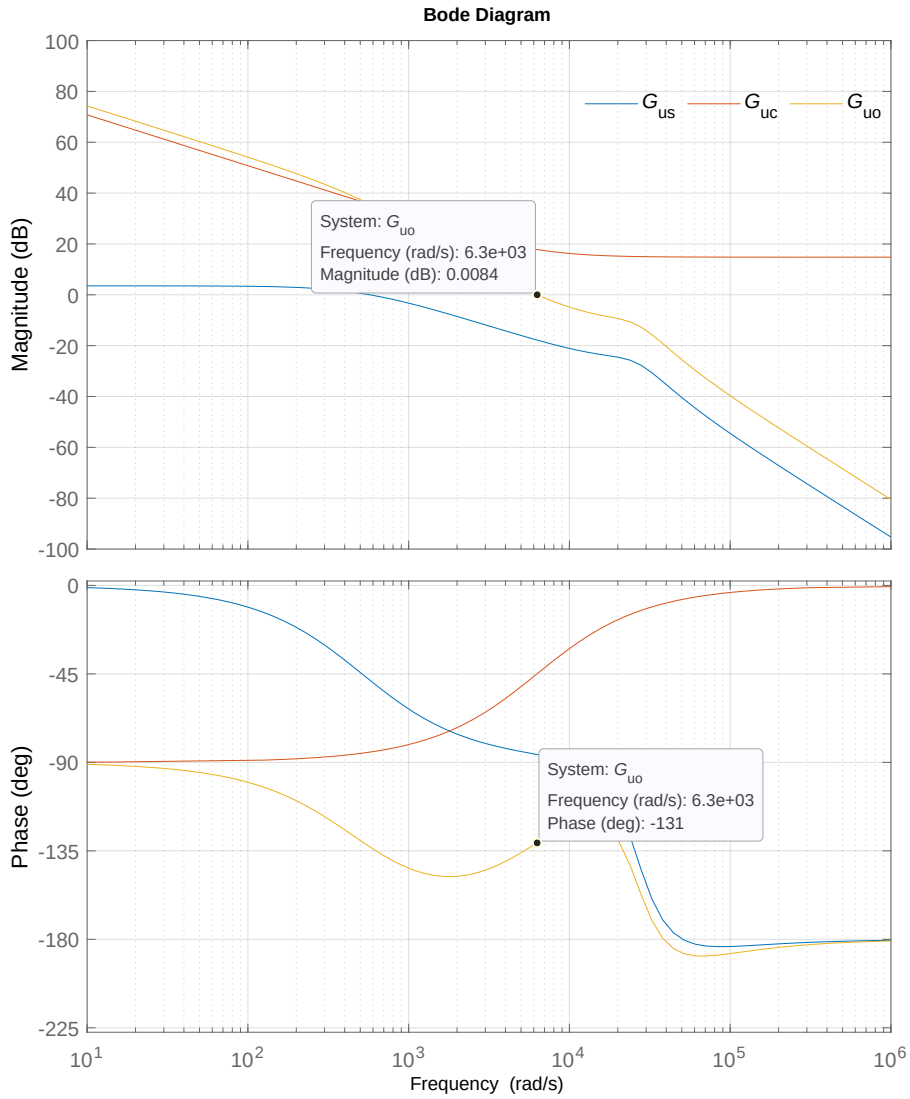


Figure 5.5: Bode plots of G_{us}, G_{uc}, and G_{uo}

the inductor current decreases as the output load decreases and the output voltage settles to the reference value 400 V after the load step.

In the simulation, the current measurement is implemented by sensing the current through the low-side switch. Furthermore, the sensed signal is regularly sampled and used in the control algorithm and for the implementation of the current observer equations. Therefore, the simulation validates that a physical closed-loop boost converter

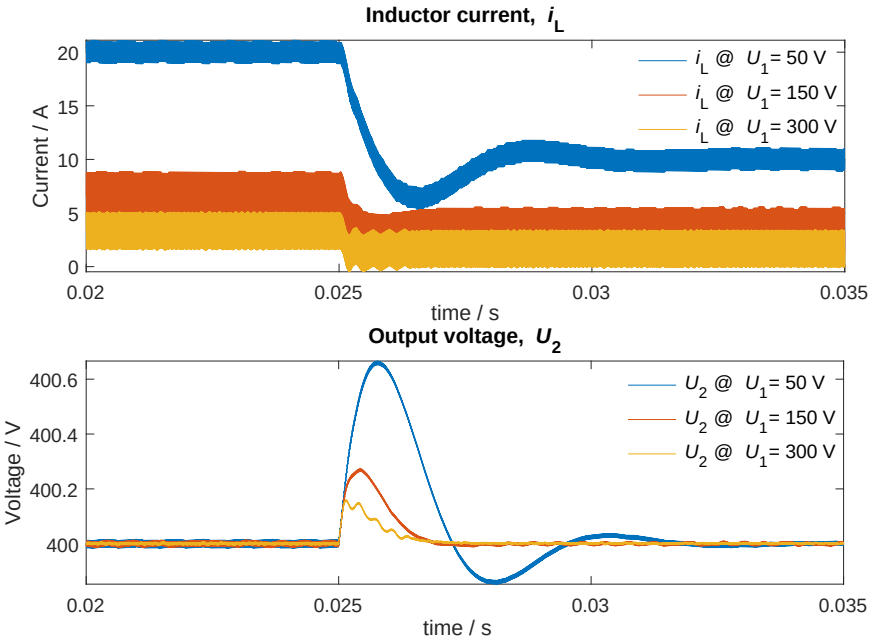


Figure 5.6: Inductor current i_L and output Voltage U_2 for different input voltages U_1

can be implemented by using only one current sensor in the commutation leg. The output of the current observer algorithm is shown in Figure 5.7. Here the input voltage is 300 V and the output is 400 V. From the simulations, the relative error between the estimated and the analytically calculated inductor current ripple is 0.065%.

The simulation model has validated the concept. Hence, it is further implemented on the prototype and the experimental results from the developed boost converter are presented in the next section.

5.3 EXPERIMENTAL SETUP

For the validation of the digital control and the current observer algorithm, a self-developed prototype is used. The prototype includes a boost converter that can be extended to a boost PFC rectifier to test the current measurement setup for the rectified sinusoidal current. Furthermore, a bridgeless boost HPFC is also present on the board to verify the current observer algorithm for the sinusoidal inductor

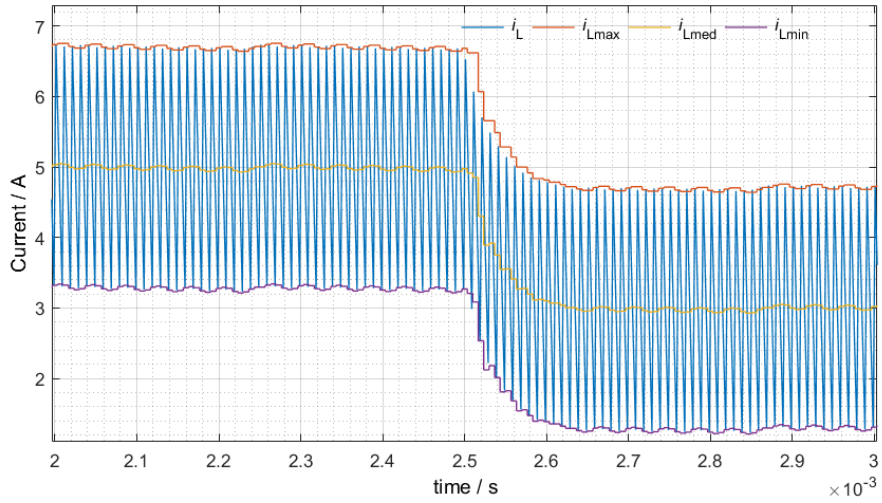


Figure 5.7: Output of the current observer algorithm i_{Lmax}, i_{Lmed} and i_{Lmin} against inductor current i_L

current. The current measurement for the PFCs is discussed in the next chapter. The developed prototype is shown in Figure 5.8. The control card is from Texas Instruments with $TMS320F28035$ microcontroller. It has a 32-bit microcontroller unit (MCU) with 60 MHz frequency.

The prototype requires one 12 V supply to power the measurement and control circuit. The switches labelled with 'Boost PFC MOSFETs' are used for the implementation of the boost converter. The current sensor is self-developed and based on the current transformer principle. The wire connecting the source of the low-side switch to the ground passes through the ferrite toroid core ($N30$) from EPCOS-TDK electronics [c.fig 5.1]. It also acts as the primary turn of the CT sensor. Furthermore, the burden resistor R_B, the CT sensor output voltage u_m, and the number of turns on the secondary n are related to the primary side pulsed current i_{S_L} as written in Equation 5.19. Here, the magnetization incuctance of the core is not considered.

$$u_m = \frac{i_{S_L}}{n} \cdot R_B \tag{5.19}$$

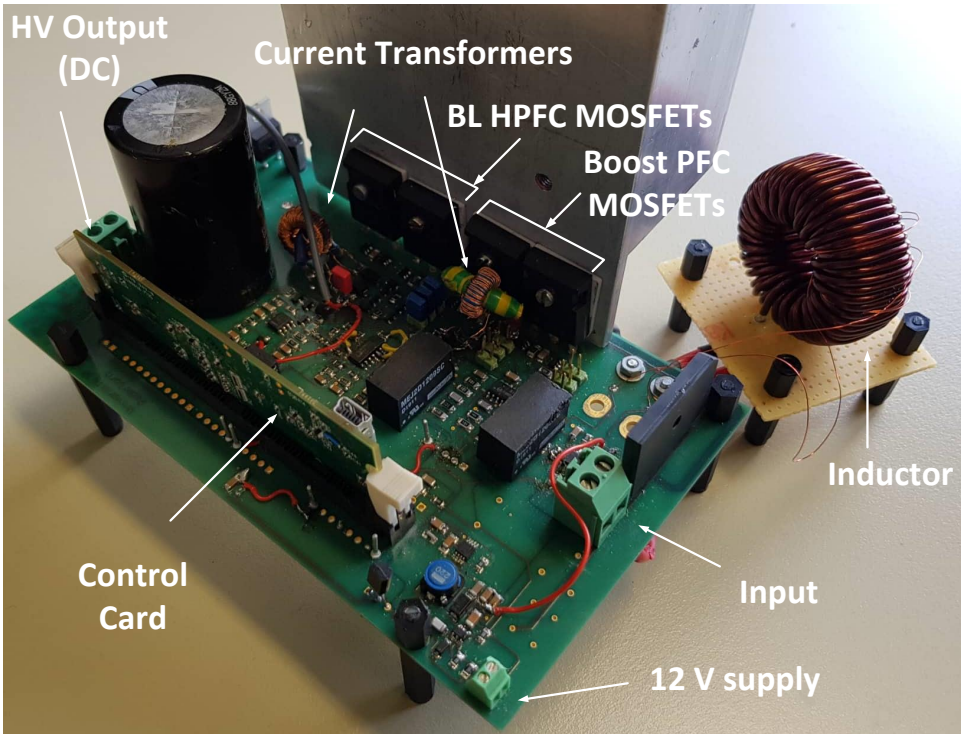


Figure 5.8: Prototype for the experimental verification

An ultra-fast recovery diode with a high DC reverse blocking voltage is also required. It is used to block the negative voltage that occurs at the secondary winding of the CT due to switching noise.

5.3.1 *Current measurement circuit design*

The analog circuit required to measure the output voltage of the current sensor is shown in Figure 5.9. The primary turn of the current transformer is attached to the current source i_{S_L}. It is positive for some interval of the time period and zero for the rest of the time period. In case of the boost converter, it is the current that flows through the low-side switch of the half-bridge and also through the primary turn of the series placed CT sensor [c.fig 5.1]. Moreover, the curves of the primary current i_{S_L}, the voltage across the secondary winding u_{des} and the output voltage u_m of the CT sensor are represented in Figure 5.10.

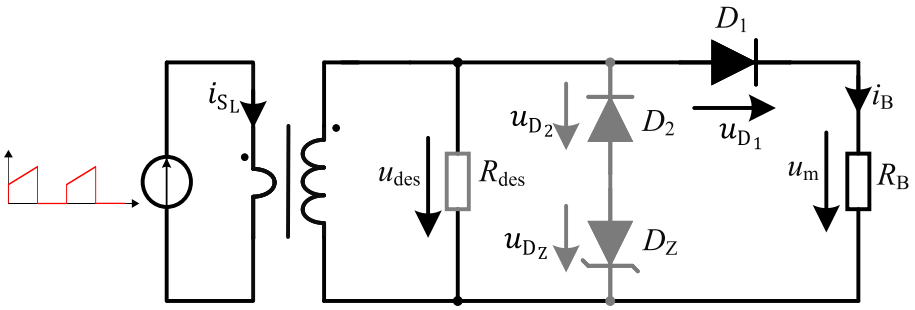


Figure 5.9: Analog circuit required for the current transformer sensor

The current through the primary winding contains a DC component that is not transferred to the secondary side, leading to partial or complete one-sided saturation of the CT core. However, since the current i_{S_L} remains zero during the interval T_a [top curve c.fig 5.10] and never becomes negative, the correct DC component can be reconstructed on the secondary side by using the diode D_1 in series with the burden resistor R_B. During the T_e interval, the current through the primary winding induces the current in the secondary winding such that the diode D_1 is forward-biased and the current flows through R_B. During the T_a interval, the current in the primary winding is zero, and the diode D_1 is reverse-biased due to the negative current induced in the secondary winding at the falling edge of the pulse current in the primary winding. This allows the demagnetization current to flow through R_{des}, providing a path to desaturate the core and prevent one-sided saturation. As a result, the voltage u_m exhibits a shape similar to that of the pulse current in the primary winding.

Further, the curve u_{des} appears across the resistor R_{des}. During the T_e interval, it has the same shape as of the pulse in the primary winding and the amplitude of this voltage is the sum of voltage across the diode D_1 and the voltage across the burden resistor [32]. This resistor is useful for the measurement of high frequency current pulses as it reduces the t_a interval. The drawback of this additional resistor is a relatively high negative peak in u_{des} curve during t_a. The peak occurs because the voltage-time product of the voltage u_{des} for both T_e and T_a intervals has to be equal. Furthermore, the decaying voltage curve across R_{des} is sinusoidal due to the parasitic

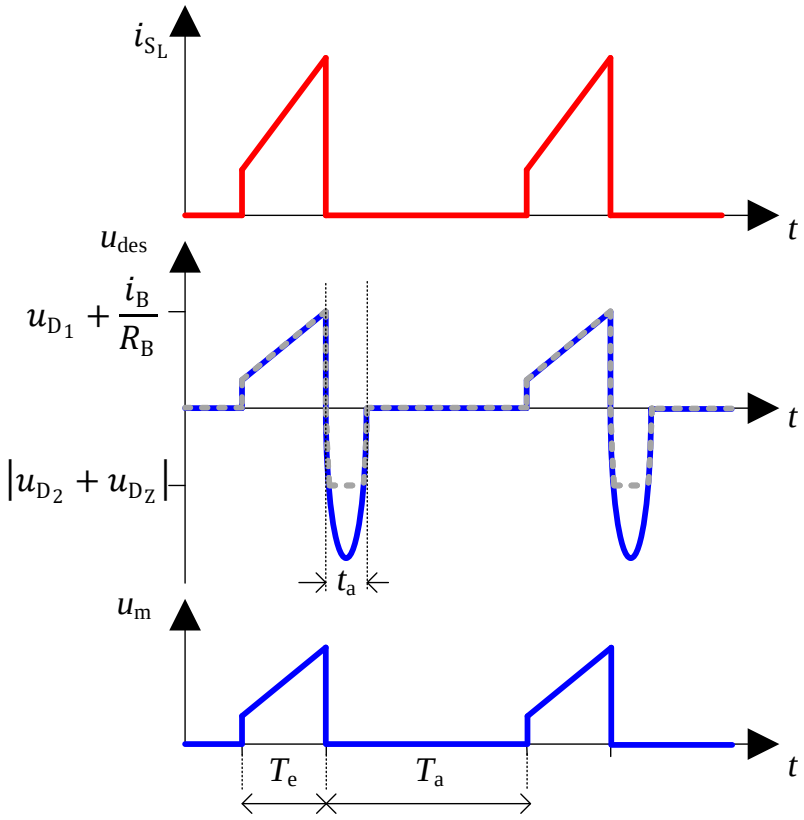


Figure 5.10: Corresponding curves of the CT sensor analog circuit

capacitance of the secondary winding of the CT thus, forming a resonant circuit.

Moreover, the value of R_{des} should be much higher than R_B so that almost negligible current flows through R_{des} during T_e. This CT-based current measurement affects the width of the pulsed current, as a sufficient time is always required to desaturate the core. In case of the duty cycle close to 100 % , there might not be enough time for the core to desaturate, which can result in high measurement error. Hence, for practical implementation, it is necessary to determine the maximum width T_e for the maximum value of the positive u_{des} voltage.

Furthermore, the reverse breakdown voltage of the diode D_1 should be greater than the negative peak of u_{des} during t_a. The peak can be clamped with a diode D_2 and a zener diode D_Z. The diode D_2

becomes forward bias for the negative u_{des}, and D_Z clamps the negative peak. For the positive u_{des}, D_2 becomes reverse bias and the diode D_1 conducts. The diodes D_2 and D_Z can be avoided by carefully selecting the number of secondary turns of the CT and the reverse breakdown voltage of D_1.

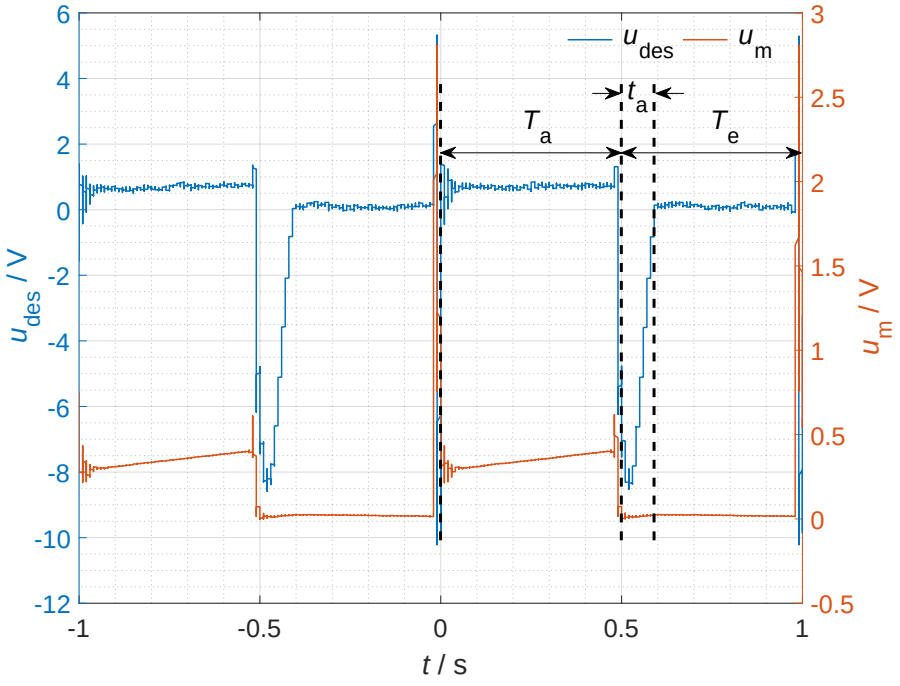


Figure 5.11: u_{des} and u_{m} voltages of the implemented CT sensor analog circuit

The above discussed schematic is implemented without the clamping circuit for the boost converter. The physical voltages u_{des} and u_{m} for one of the current measurements are shown in Figure 5.11.

The blue curve represents the voltage across R_{des}, while the orange curve shows the voltage across the burden resistor R_{B}. The time intervals are also indicated, and the switching frequency of the converter is 100 kHz. The voltage u_{m} during the T_{a} interval is lower compared to u_{des} due to the voltage drop across the D_1 diode. Furthermore, the negative peak in u_{des} indicates the desaturation of the transformer core. For this implementation, D_1 with $-40\,\text{V}$ reverse breakdown

voltage is used. The burden resistor is selected such that 1 V appears across R_B for 10 A primary current. Moreover, the experiments showed that to avoid the saturation of the CT core the maximum duty cycle of the primary pulsed current should not exceed 85 %.

For the design of the CT core, one important parameter is the maximum flux density. The size of the core is not affected by the primary current; rather, it depends on the voltage that develops across the burden resistor. Hence, the voltage u_m has a proportional influence on the maximum flux density B_{max} of the core, and this relation can be written as below.

$$B_{max} = \frac{u_{m,max} \cdot d_{max}}{n \cdot A_e \cdot f_S} \tag{5.20}$$

Where d_{max} is the maximum duty cycle, n is the number of secondary turns, A_e is the cross sectional area of the core, and f_S is the switching frequency or the frequency of the primary current pulse. From the equation 5.20, if $u_{m,max}$ is increased, B_{max} will also increase. Therefore, to keep B_{max} constant, either the area or the operating frequency should should be increased. Typically, B_{max} is selected below 200 mT during the design of the CT.

5.3.2 *Verification of current observer algorithm*

The analog circuit for the current measurement is implemented without the clamping diodes. The number of turns of the secondary winding are $n = 60$. The burden resistor R_B is of 10 Ω and R_{des} of 5.1 kΩ is used. A fast recovery rectifier diode $ES1D$ is used as D_1 to block the negative peak in u_{des}.

For the implementation of the current observer two capture modules are configured. One is used to capture the number of the DSP clock cycles during which the inductor current is rising, and the other capture module captures the number of clock cycles during which the inductor current is falling. Moreover, the ADC input pins are also configured to regularly sample the inductor voltage. After configuring the modules, the current observer equations 5.5 and 5.6 are written in digital domain.

The boost converter is operated with different input voltages 100 V, 200 V, and 300 V and the output is set to 400 V. The physical inductor current i_{L} and the output of the current transformer u_{m} curves are recorded with the oscilloscope. Moreover, the output of the current observer algorithm is also validated. The digital values of i_{Lmax}, i_{Lmed}, and i_{Lmin} are also visualized on the oscilloscope with the help of the serial peripheral interface (SPI)-based hardware monitor. The stored data from the oscilloscope is then analyzed and plotted with MATLAB.

The results of the current observer algorithm for the boost converter delivering 500 W with input voltages of 100 V, 200 V, and 300 V, and an output of 400 V, are shown in Figure 5.12, Figure 5.13, and Figure 5.14, respectively. In these figures, the top plots show the physical inductor current measured with the current probe alongside the scaled output of the digital current observer, while the bottom plot shows the output voltage of the current transformer. The current probe used for the measurement is the LeCory $CP031A$. It has the bandwidth of 100 MHz and can measure up to 30 A with a minimum sensitivity $\frac{1\,\mathrm{mA}}{div}$. For each experiment, the current observer output is compared to the current measured by the probe and the relative error is determined.

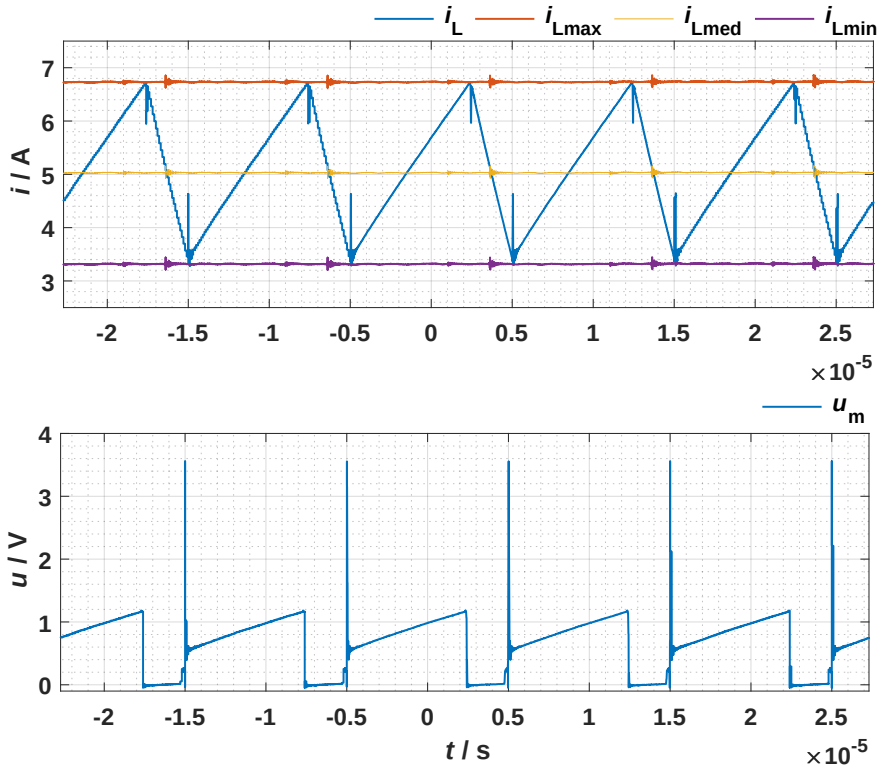


Figure 5.12: Inductor current and current observer output (top), CT sensor output (bottom) with input voltage of 100 V

	I_{Lmax}	I_{Lmed}	I_{Lmin}
Current Probe	6.712 A	5.088 A	3.314 A
Current observer	6.740 A	5.058 A	3.282 A
Relative error	0.417 %	0.589 %	0.965 %

Table 5: Current observer relative error at $U_1 = 100\,\text{V}$

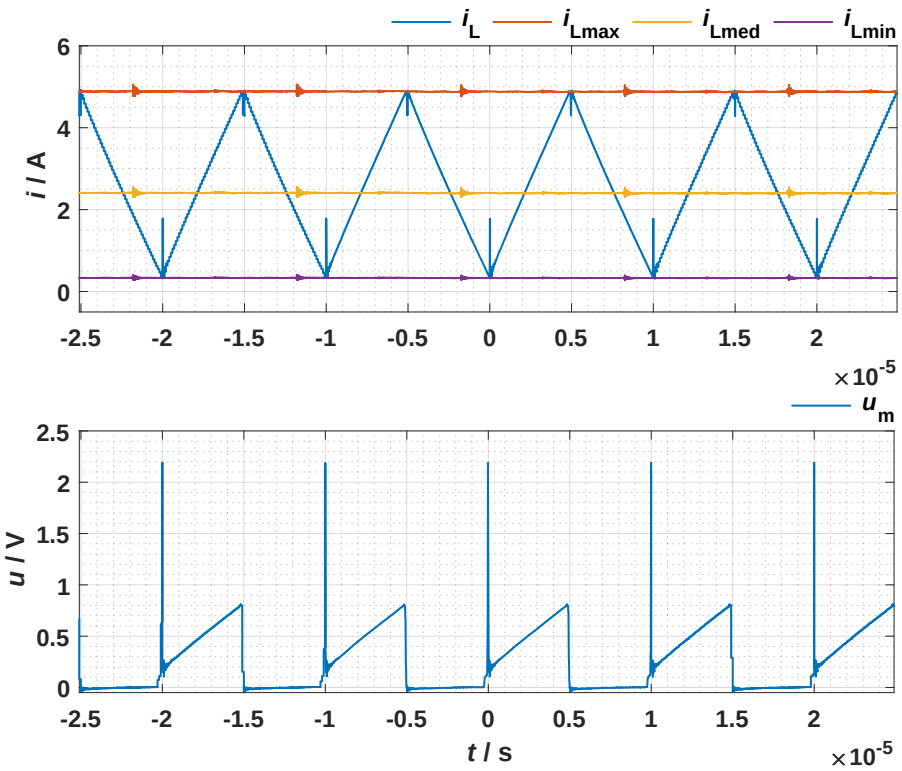


Figure 5.13: Inductor current and current observer output (top), CT sensor output (bottom) with input voltage of 200 V

	I_{Lmax}	I_{Lmed}	I_{Lmin}
Current Probe	4.871 A	2.399 A	0.476 A
Current observer	4.842 A	2.421 A	0.484 A
Relative error	0.595 %	0.917 %	1.681 %

Table 6: Current observer relative error at $U_1 = 200\,\mathrm{V}$

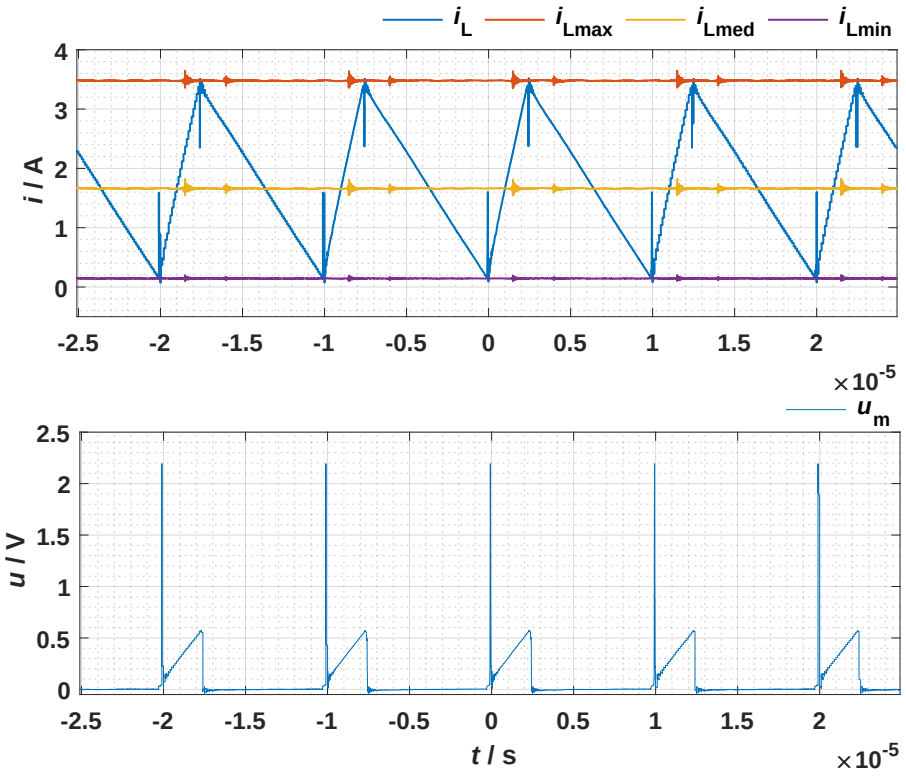


Figure 5.14: Inductor current and current observer output (top), CT sensor output (bottom) with input voltage of 300 V

	I_{Lmax}	I_{Lmed}	I_{Lmin}
Current Probe	3.475 A	1.675 A	0.152 A
Current observer	3.506 A	1.656 A	0.145 A
Relative error	0.892 %	0.957 %	4.605 %

Table 7: Current observer relative error at $U_1 = 300\,\mathrm{V}$

The experimental results are summarized in Table 5, Table 6, and Table 7. The relative error is also calculated with reference to the current probe signal. The relative error is higher for the lower estimated current values due to the increased cumulative error at lower currents involved at each stage of the computation.

In summary, in this chapter the current observer for the boost converter is implemented. In this case, the digitally implemented control

algorithm does not have any benefit from the current observer; it is an additional part of program code that estimates the inductor current. However, the hardware implementation benefits from estimating the complete inductor current with only one current sensor. It reduces the cost and parasitic inductance in the commutation path. Furthermore, the analog circuit of the current transformer is also discussed. This circuit can be used where the primary current is pulsating and the current is unipolar. It can be extended for a bipolar current that will be discussed in the next chapter. Moreover, the experimental results have shows that the relative error in the ripple of the inductor current becomes 1.1 % even at lower I_{Lmin}. This error is not very significant and therefore, such implementation can be extended and tested for the PFC rectifiers.

6

IMPLEMENTATION OF A CURRENT OBSERVER FOR PFC RECTIFIERS

In various applications of power electronics, the AC line voltage needs to be converted to the DC voltage. This conversion is possible with the arrangement shown in Figure 6.1. It consists of a diode bridge rectifier connected to the AC source, with the DC terminals connected across the output filter. From the curves, it can be seen that such rectification has a very poor power factor, leading to low efficiency and high harmonic distortions in the source current. Furthermore, due to the passive nature of the diode, the current drawn from the AC line voltage cannot be controlled and depends solely on the output resistor capacitor (RC)-filter [33], [34]. Moreover, in this configuration, the output voltage is limited to the peak value of the input voltage. Therefore, such rectification is not directly used.

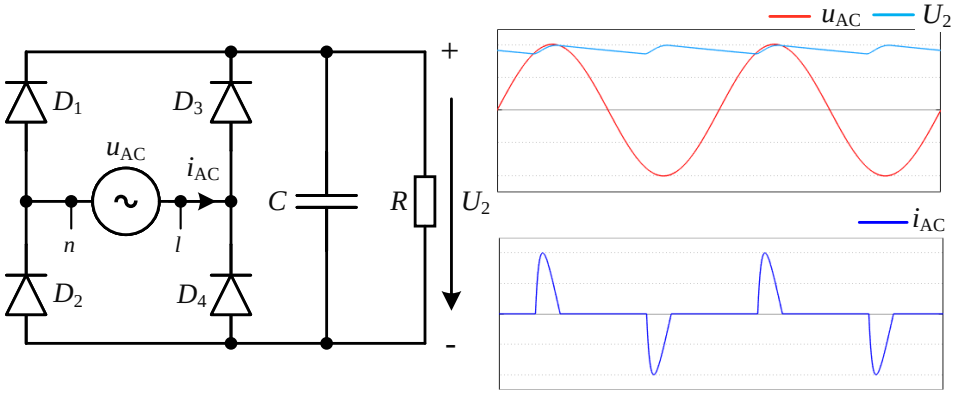


Figure 6.1: Diode bridge rectifier with typical voltage and current curves

The power factor can be improved in the above configuration by controlling the current drawn from the AC source. This can be achieved by adding the boost converter between the DC output of the diode bridge and the output RC-filter, as shown in Figure 6.2. This configuration forms the basic and very popular rectifier also known as the boost PFC rectifier. Now, the AC line current, i_{AC}, does not only

depend on the output filter but also on the duty cycle of the switching transistor. The switching sequence s_L of the power transistor is regulated such that the current drawn from the source is in line with the AC line voltage.

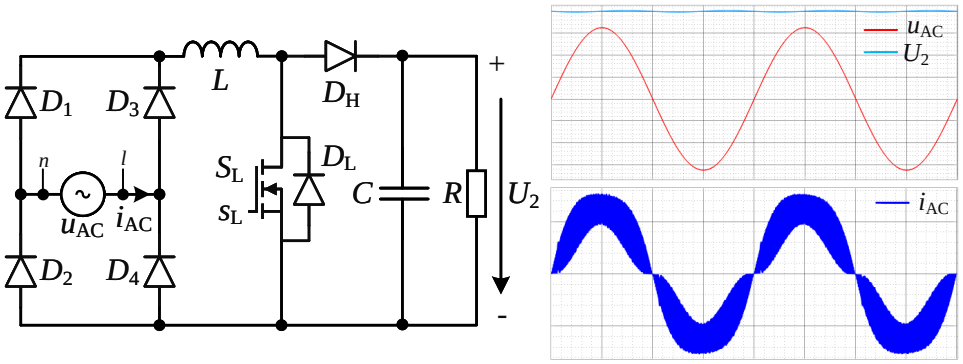


Figure 6.2: Boost PFC rectifier with typical voltage and current curves

The phase shift between the source current i_{AC} and the source voltage u_{AC} is very small, resulting in a power factor close to unity. Moreover, the current i_{AC} also carries the varying inductor current ripple. Several PFC rectifier topologies in the literature do not require a passive diodes bridge at the input; instead, rectification is performed with power transistors and power diodes [35]. Hence, rectification and boost operation can be achieved with fewer power electronic components.

Inductor current measurement plays a crucial role in controlling the PFC rectifier. The type of the current sensor depends on cost, required bandwidth, and the power losses, as discussed in previous chapters. In this chapter, the digital current observer is proposed and implemented for the PFC rectifiers. In the beginning, the chapter provides an overview of three different rectifier topologies: boost PFC, bridgeless boost HPFC, and totem-pole PFC rectifier. The operation of each rectifier and the formation of the current through the boost inductor are discussed. Furthermore, the implementation of the digital current observer for each rectifier is presented.

The closed-loop control for the PFC rectifier is also mentioned in this chapter. In totem pole PFC section, it is shown that the control can

be improved with the digital current observer. Moreover, the control and the current observer concept are validated with the simulation models. For verification of the simulations, a DSP-based digital closed loop is implemented and the experimental results are included in this chapter.

6.1 BOOST POWER FACTOR CORRECTION RECTIFIER

The boost PFC rectifier consists of the diode bridge rectifier at the input followed by the boost converter and the output filter, as shown in Figure 6.3 [36], [37]. These three parts are marked with grey dotted blocks in the diagram. The sinusoidal input voltage u_{AC} is rectified to the voltage u_1. The average and the RMS value of u_1 are given as below.

$$U_{1,\mathrm{avg}} = \frac{2 \cdot U_{\mathrm{AC,max}}}{\pi} \tag{6.1}$$

$$U_{1,\mathrm{rms}} = \frac{U_{\mathrm{AC,max}}}{\sqrt{2}} \tag{6.2}$$

whereas $U_{\mathrm{AC,max}}$ represents the maximum value of the input AC voltage, ideally, the RMS values of u_1 and u_{AC} are equal. However, due to the losses of the diodes, u_1 has a slightly lower RMS value.

The boost converter operates with an input voltage u_1 and an output voltage U_2. The switches S_{H} and S_{L} of the converter operate in the complementary switching to avoid short circuiting the half-bridge. The red dotted loop represents the inductor current path when the switching signals are $s_{\mathrm{L}} = 1$ and $s_{\mathrm{H}} = 0$, and the blue dotted loop represents i_{L} path when the switching signals are $s_{\mathrm{L}} = 0$ and $s_{\mathrm{H}} = 1$ [c.Fig. 6.3(a)].

The source voltage u_{AC} and the current i_{AC} are in phase with each other. Similarly, the input voltage of the boost converter u_1 and the inductor current i_{L} are in line, as shown in Figure 6.3(b). This results in the power factor close to unity. Moreover, a zoomed-in view of the currents through the switches S_{L} and S_{H} is also sketched in the figure. The output voltage U_2 is considered constant, but in reality,

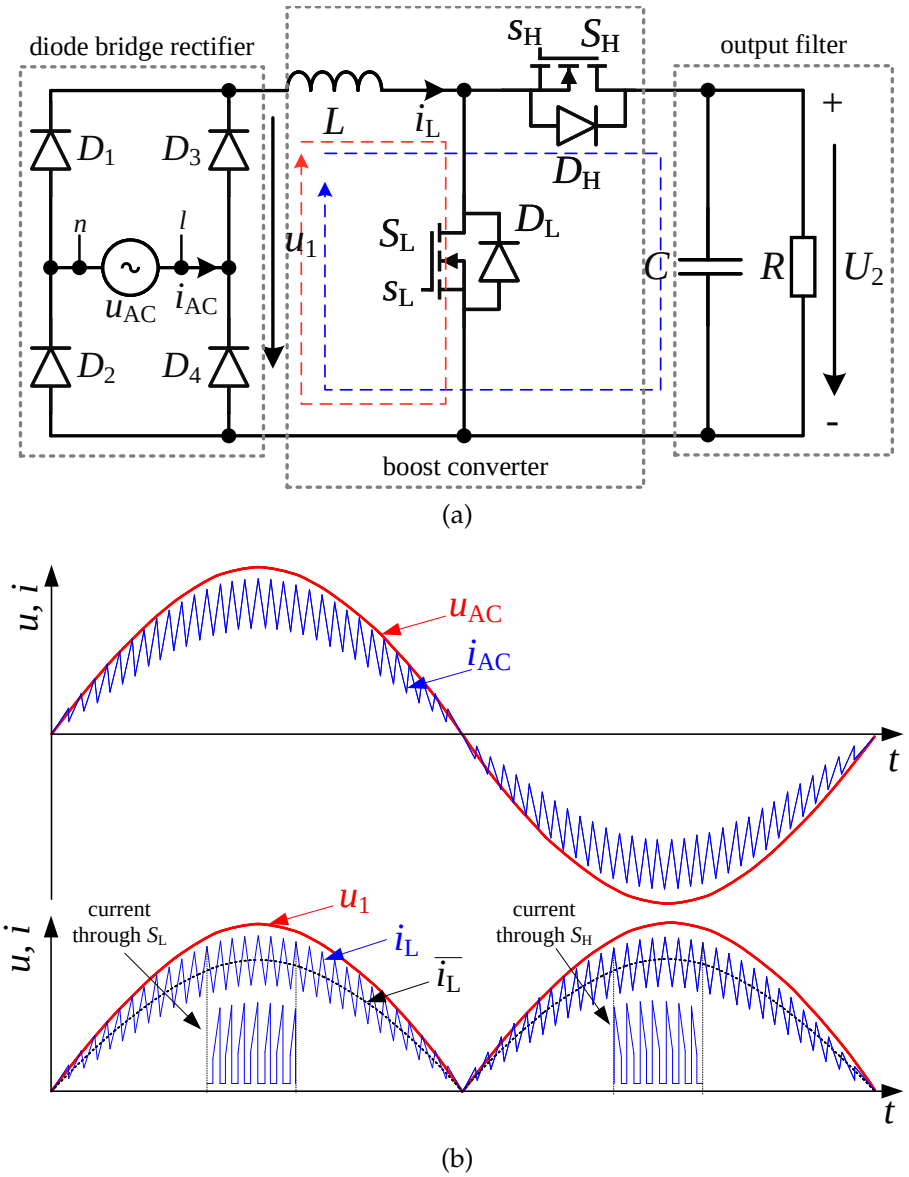


Figure 6.3: (a) Boost PFC rectifier (b) source AC voltage and current (top), diode bridge output voltage u_1, inductor current i_L and average inductor current $\bar{i}_L$ (bottom)

it also has a small AC component with a global frequency twice that of the source frequency.

6.1.1 *Current measurement setup*

Similar to the boost converter, measuring the inductor current is required to implement the closed-loop control for the boost PFC rectifier. The complete inductor current can be measured either by placing a sensor in series with the inductor or by placing two sensors in series with each transistor, as discussed in Section 2.3.

In this topology, the inductor current i_{L} is unipolar with a global frequency twice of the source current i_{AC}. Additionally, it also has the ripples due to the switching of the transistors. During each switching interval, the inductor current rises when $s_{\mathrm{L}} = 1$ and $s_{\mathrm{H}} = 0$, and falls when $s_{\mathrm{L}} = 0$ and $s_{\mathrm{H}} = 1$. This results in a pulsating current through the switches that can be sensed with the current transformer sensors, as mentioned for the boost converter.

Hence, for the implementation of the digital control with the DSP, one current sensor in series with the low-side switch is sufficient to estimate the average inductor current $\bar{i}_{\mathrm{L}}$ for one switching interval. This remains valid until the PFC operates in continuous conduction mode. During discontinuous conduction operation, the controller must perform online estimation to determine the correct average inductor current. Moreover, due to the presence of the boost converter in the middle stage, the previously proposed current measurement setup with one CT sensor in series with the low side switch can be used here.

6.1.2 *Current observer realization*

The digital current observer for the inductor current in the boost PFC rectifier can be realized similarly to the boost converter. The output of the current sensor provides the average value of i_{L}. The maximum and the minimum values of i_{L} for each switching interval are estimated in the digital domain. Furthermore, secondary windings are required over the boost inductor for measuring the inductor voltage and the width of the switching intervals.

In case of the boost PFC rectifier, the voltage across the inductor switches within a varying voltage envelop over each mains half cycle. The maximum voltage level of this envelop is the rectified AC

source voltage u_1, and the minimum voltage level is always $u_1 - U_2$. Moreover, the rectifier operation switches between continuous and discontinuous conduction modes near the zero crossings. During CCM, the inductor voltage is switching between two states, u_1 and $u_1 - U_2$, while during DCM, it switches between three states: u_1, $u_1 - U_2$ and 0 as shown in Figure 6.4.

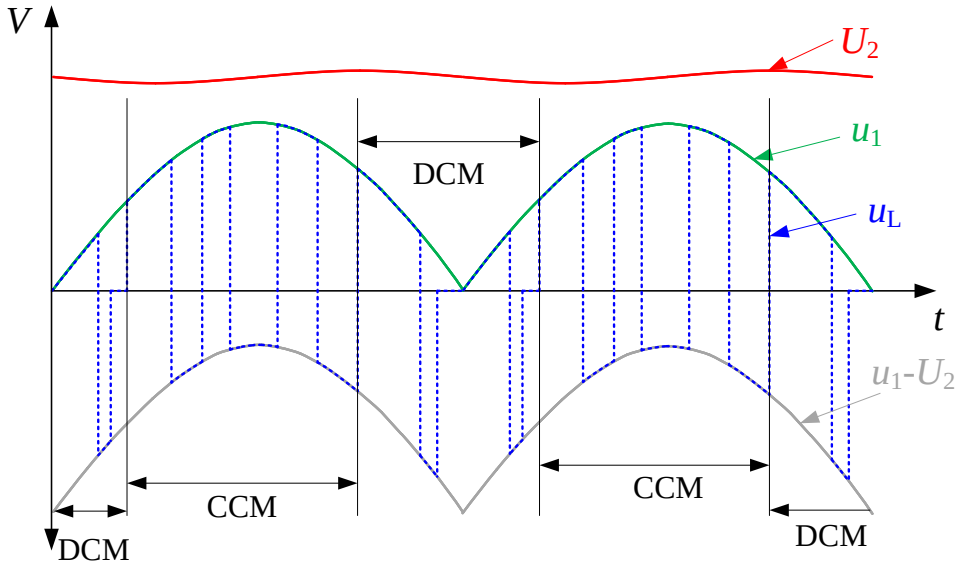


Figure 6.4: Voltage across the inductor in the boost PFC rectifier

The current observer algorithm implemented previously for the boost converter can be extended to the boost PFC rectifier. During CCM operation, the algorithm estimates the maximum, mean, and minimum values as stated in equations 5.5 and 5.6. Moreover, the switching frequency of the converter is assumed to be much higher than the input source frequency; therefore, the inductor voltage can be assumed constant for each switching state.

During DCM operation of the PFC, the equations of the current observer algorithm need to be modify. Now, the converter goes through three different states in one switching period, as shown in Figure 6.5. The voltage and current curves of the inductor and the corresponding input voltage signals for the DSP during discontinuous conduction

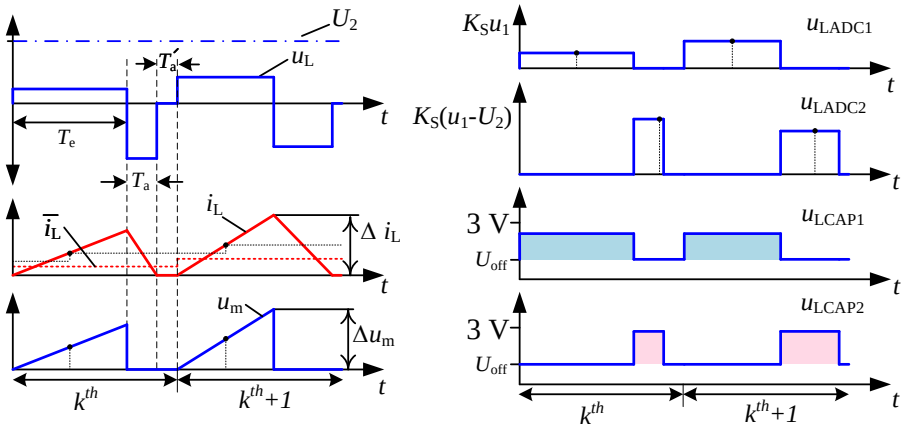


Figure 6.5: Inductor voltage u_L, inductor current i_L and the current observer input signals during DCM operation of the PFC rectifier

mode are also sketched in the figure. Moreover, each switching period is divided into T_e, T_a, and T_a' time intervals.

During the T_e interval, the low-side switch conducts and the energy is stored in the inductor. For this interval, the inductor current can be measured with the CT sensor in series with the switch S_L. The output voltage u_m of the sensor can be regularly sampled at the ADC input pin of the digital controller. This sampled value does not represents the average value of the inductor current; rather, it represents half of the inductor current ripple Δi_L. Furthermore, during T_e interval, the voltage across the inductor is u_1. It can be stepped down by the auxiliary winding with proportionality constant K_s to form u_{LADC1}. This signal is also regularly sampled at the ADC input pin of the DSP. For the estimation of the width of the T_e interval, u_{LCAP1} signal can be used as input to the time capture module of the DSP.

During T_a interval, the high-side switch conducts and the inductor current decreases to zero with the voltage across the inductor $u_1 - U_2$. The regular sampling of u_{LADC2} to measure the voltage across the inductor during this interval cannot be used because the signal can reach zero before the sampling instant. However, u_{LCAP2} can be used to estimate the T_a interval. During T_a', the inductor current stays zero because the voltage across the inductor also remains zero. From the given digital signals, the current observer equations for the

discontinuous operation of the boost PFC rectifier can be written as following.

$$\begin{aligned} T_e &= \frac{C_1}{f_{clk}} \\ T_a &= \frac{C_2}{f_{clk}} \end{aligned} \tag{6.3}$$

Where C_1 and C_2 are the outputs of the time capture modules, given in terms of the number of DSP clock cycles during T_e and T_a intervals. The frequency of the clock signal of the capture module or the processor is represented by f_{clk}.

The equation for the estimation of the maximum and the mean value of the inductor current for a switching instant k is given below.

$$K_m I_{Lmax,k} = 2 \cdot u_{m,k} = \Delta u_{m,k} \tag{6.4}$$

$$K_m I_{Lmed,k} = u_{m,k} \cdot \left(\frac{C_{1,k}}{f_{clk}} + \frac{C_{2,k}}{f_{clk}}\right) \cdot f_S \tag{6.5}$$

Whereas the minimum value can be assumed to be zero, as the voltage across the inductor is theoretically zero. Furthermore, the current observer equations are scaled with K_m, which is the proportionality constant of the current sensor.

Hence, for the implementation of the digital current observer for the boost PFC, the algorithm must differentiate between the CCM and DCM modes and use the corresponding equations for the estimation. Furthermore, the aforementioned current observer equations are validated with the simulation model, as documented in the next section.

6.2 BRIDGELESS BOOST HPFC RECTIFIER

In the boost PFC rectifier, the AC input is first rectified with the diode bridge. This adds to the continuous losses and decreases the efficiency of the rectifier. Higher efficiency can be achieved with

another class of power factor rectifiers known as bridgeless power factor correction BLPFC rectifiers [38]. In these rectifiers, the passive diode bridge is more or less eliminated, thus, resulting in lower conduction losses.

The rectifiers from the BLPFC category have the power inductor connected in series with the AC source. Therefore, the inductor current is bipolar and needs to be in phase with the input voltage to achieve unity power factor. In this section, the operation of the bridgeless boost HPFC, the inductor current measurement setup, and the realization of the digital current observer are discussed further. This rectifier consists of one bidirectional switch S in series with the inductor L. Additionally, it requires two fast-switching diodes (D_1, D_2) and two slow-switching diodes (D_3, D_4). The fast switching diodes allow the Si-MOSFETs to be driven in the hard switching CCM operation. The rectifier is shown in Figure 6.6.

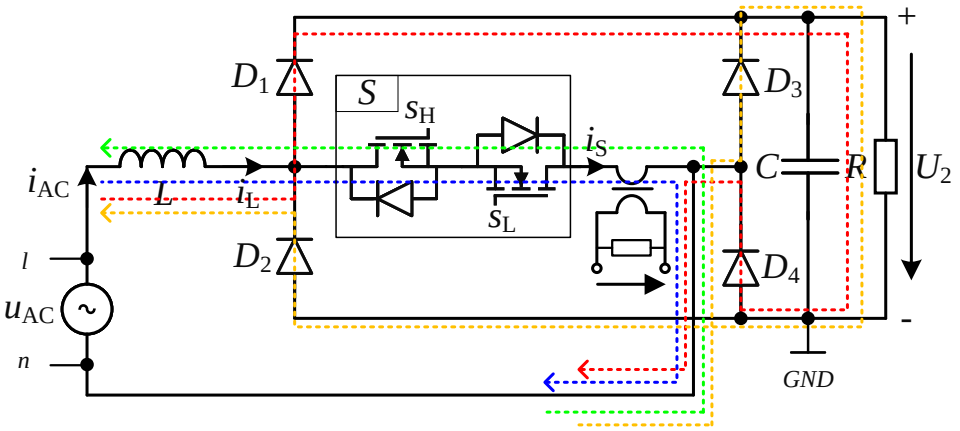


Figure 6.6: Inductor current paths for various switching states of the bridgeless boost HPFC

The paths of the inductor current i_L for the positive and negative mains half cycles are shown with the dotted lines in the figure 6.6. During the positive cycle of u_{AC}, the current i_L follows the path of the blue dotted line when the switch S is conducting. It flows through the switch and the current sensor and returns to the source. When the switch is in the blocking state during the positive mains half cycle, the current follows the red dotted line. It flows through

the fast diode D_1 to the load and returns to the node n via the slow diode D_4.

For the negative mains cycle, when the switch S is conducting, the green dotted line represents the path of the current. The yellow dotted line shows the current path when S is in blocking state. In this rectifier, the node GND is shorted to n of the source during the positive u_{AC} cycle and during the negative u_{AC} cycle GND potential is equal to $-U_2$. This shows that the EMI characteristic of this topology is different from the typical boost PFC, where GND is at $-U_2$ for the both mains half cycles.

6.2.1 *Current measurement setup*

In the BLPFC, the current through the inductor i_L is the same as the source current i_{AC}. It can be measured by placing the sensor at different positions in the rectifier, and the type of the sensor depends on the position. For example, if the sensor is placed in series with the inductor, it should have a wide bandwidth ranging from a few Hz to MHz. Alternatively, if the sensor is placed in series with the switch S, the bandwidth range is shifted to only higher frequencies, such as a few kHz to MHz. The current through the inductor i_L and the current through the switch i_S are sketched in Figure 6.7. It can be seen in the curves that the inductor current has both a global (low) frequency and a local (high) frequency content. The low frequency is the same as that of the AC grid, while the high frequency is equivalent to the switching frequency of the switch. In contrast, the current i_S is composed only of high switching frequency.

Based on the comparison of the current sensors from chapter 2, a low-loss current measurement is possible with the current sensor in series with the switch S, as shown in figure 6.6. However, it is now necessary to sense both polarities of the current. This can be achieved using various methods, such as by implementing a rectifier at the output of the current transformer sensor with the fast-switching Schottky diodes.

In the experimental setup presented in 6.6, the bidirectional current is sensed by implementing two secondary windings on the core of the

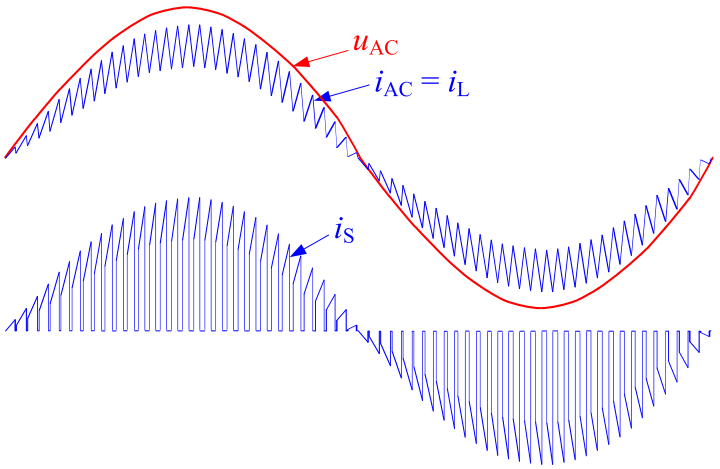


Figure 6.7: Curves of the source AC voltage and the current (top) and the switch S current (bottom)

CT sensor. The analog circuit required for the current measurement is shown in Figure 6.8. The primary winding consists of one turn and carries the current i_S. For the positive mains cycle, the transistor marked with $(+)$ is shorted and provides the positive voltage across the burden resistor, while the other transistor marked with $(-)$ is open. For the negative mains cycle, the switching of the transistors is reversed. The output voltage u_m can be directly connected to the analog input pin of the digital signal processor.

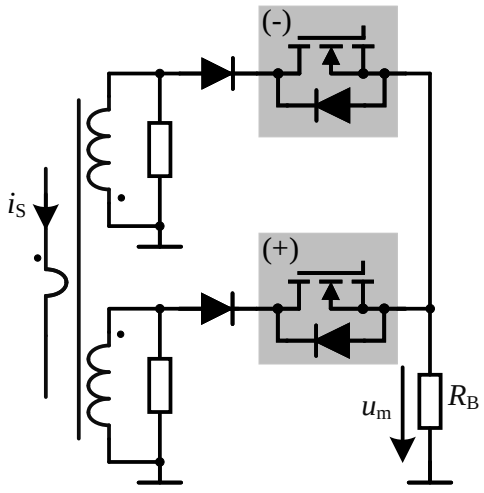


Figure 6.8: Current measurement setup for the BLPFC rectifier

6.2.2 *Current observer realization*

The digital current observer algorithm can be implemented for the bridgeless boost HPFC rectifier by further extending the concept from the section 6.1.2. The challenge here is to adopt the algorithm for the negative current estimation using the available measurement signals. The basic concept remains the same: the output of the current measurement circuit provides the mean value of the inductor current for one switching interval. Furthermore, the voltage signals from the auxiliary windings on the inductor are used to measure the voltage across the inductor and to estimate the durations of the switching intervals.

The voltage u_L across the inductor in the HPFC rectifier switches within a varying maximum and minimum voltage envelop for the positive and the negative mains half cycle. For the positive mains half cycle, the maximum voltage level is u_1 and the minimum voltage level is $u_1 - U_2$. For the negative mains half cycle, the maximum voltage level is $U_2 - u_1$ and the minimum voltage level is u_1. This is also shown in Figure 6.9. In the figure, the input voltage u_{AC} is represented with u_1. The switching inductor voltage u_L is drawn with blue dotted lines. Furthermore, during DCM, u_L switches between three states and during CCM operation, it switches between two states.

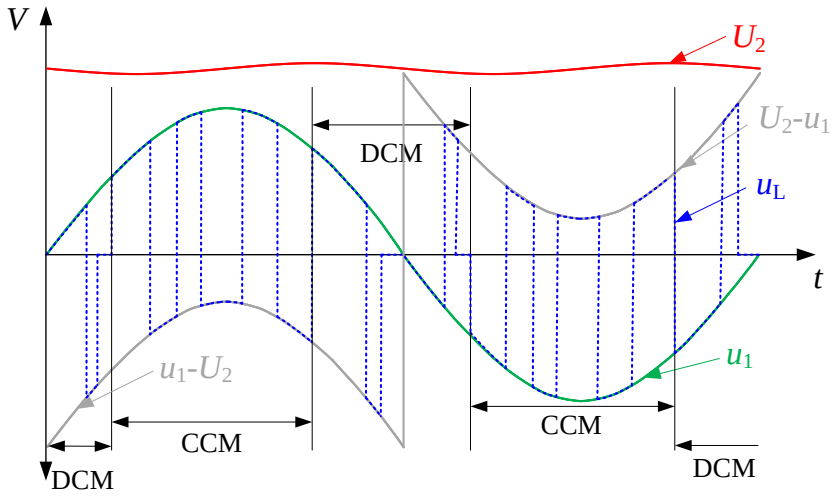


Figure 6.9: Voltage across the inductor in the BLPFC rectifier for the complete AC cycle

The voltage across the inductor is not identical during each half cycle. Therefore, the current observer algorithm must distinguish between the positive and negative mains half cycle. The difference between the secondary winding outputs for two switching intervals for each mains half cycle is shown in Figure 6.10. For the positive mains half cycle, u_{LADC1} represents the voltage across the inductor for T_{e} interval, and u_{LADC2} represents the voltage across the inductor for T_{a} interval. For the negative mains half cycle, u_{LADC1} represents the voltage across the inductor for T_{a} interval, and u_{LADC2} represents the voltage across the inductor for T_{e} interval. Here, K_{S} is the proportionality constant of the voltage conversion.

The regular sampling instants for u_{LADC1} and u_{LADC2} are also different for the positive and negative mains half cycle. For the positive mains half cycle, u_{LADC1} is sampled at the middle of the T_{e} interval, and u_{LADC2} is sampled at the middle of the T_{a} interval. For the negative mains half cycle, u_{LADC1} is sampled at the middle of the T_{a} interval, and u_{LADC2} is sampled at the middle of the T_{e} interval. This is important for configuring of the analog input pins of the digital signal processor.

For the capture modules, the inputs are u_{LCAP1} and u_{LCAP2}. For the positive mains half cycle, the capture module with u_{LCAP1} as input counts the number of clock cycles for the T_{e} time interval, and the capture module with u_{LCAP2} as input counts the number of clock cycles for the T_{a} time interval. For the negative mains half cycle, u_{LCAP1} is used to estimate the width of T_{a} time interval, and u_{LCAP2} is used to estimate the width of T_{e} time interval.

As in section 5.1, it is assumed that C_1 represents the number of clock cycles counted by the capture module with u_{LCAP1} input and C_2 represents the number of clock cycles counted by the capture module with u_{LCAP2} input. The frequency of the clock signal to the capture modules is represented as f_{clk}. For the positive mains half cycle, T_{e} and T_{a} are

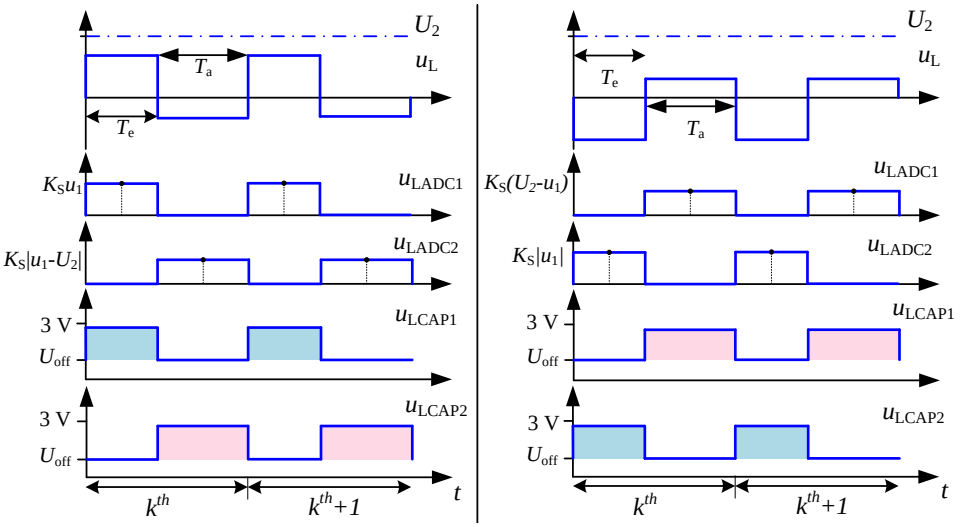


Figure 6.10: Voltage across the inductor and the auxiliary windings outputs for the positive (left) and the negative (right) mains half cycle in the BLPFC rectifier

$$\begin{aligned} T_e &= \frac{C_1}{f_{clk}} \\ T_a &= \frac{C_2}{f_{clk}} \end{aligned} \tag{6.6}$$

and for the negative mains half cycle, T_e and T_a are

$$\begin{aligned} T_e &= \frac{C_2}{f_{clk}} \\ T_a &= \frac{C_1}{f_{clk}} \end{aligned} \tag{6.7}$$

Furthermore, it is assumed that u_m represents the output of the current measurement circuit and K_m represents the proportionality constant between the physical current and u_m. The digital current observer equations for the positive mains half cycle are written below.

$$K_m I_{Lmax,k} = \frac{1}{2}\frac{K_m}{K_S}\frac{u_{LADC1,k}}{L}\frac{C_{1,k}}{f_{clk}} + u_{m,k} \tag{6.8}$$

$$K_m I_{Lmin,k} = -\frac{K_m}{K_S}\frac{u_{LADC2,k}}{L}\frac{C_{2,k}}{f_{clk}} + K_m I_{Lmax,k} \tag{6.9}$$

Also, the digital current observer equations for the negative mains half cycle can be written as below.

$$K_m I_{Lmax,k} = \frac{1}{2}\frac{K_m}{K_S}\frac{u_{LADC2,k}}{L}\frac{C_{2,k}}{f_{clk}} + u_{m,k} \tag{6.10}$$

$$K_m I_{Lmin,k} = -\frac{K_m}{K_S}\frac{u_{LADC1,k}}{L}\frac{C_{1,k}}{f_{clk}} + K_m I_{Lmax,k} \tag{6.11}$$

The equations 6.8 to 6.11 are valid for the continuous conduction mode CCM operation. During the discontinuous conduction mode DCM operation, the digital inductor current ripple Δu_m can be estimated by multiplying the sampled u_m signal by 2. The mean inductor current value can be estimated by the digital current observer by averaging the sampled u_m over the switching interval. For the switching interval k, the digital current observer equations are

$$\Delta u_{m,k} = 2 \cdot u_{m,k} = K_m I_{Lmax,k} \tag{6.12}$$

$$K_m I_{Lmed,k} = u_{m,k} \cdot \left(\frac{C_{1,k}}{f_{clk}} + \frac{C_{2,k}}{f_{clk}}\right) \cdot f_S \tag{6.13}$$

The estimated minimum inductor current during DCM can be assumed as zero, as the voltage drop across the inductor is zero. Furthermore, the digital current observer equations are scaled with the proportionality constant of the current sensor, K_m.

The aforementioned current observer equations for the HPFC are validated with the simulation model and are documented in the next section.

6.3 TOTEM-POLE PFC

The totem-pole PFC consists of a rectifier bridge, with one leg made up of power transistors and the other leg composed of power diodes.

The AC line is fed to the rectifier bridge through a boost inductor. This is the only bridgeless PFC that does not require fast-switching diodes when the silicon (Si)-based, or modern SiC or GaN-based transistors are used. Furthermore, if the bridge leg is made up of Si-based MOSFETs, it should operatein BCM or DCM modes to avoid the hard switching.

A typical totem-pole PFC is shown in Figure 6.11. The dotted lines indicate the flow of the inductor current for the switching states during the positive and negative mains half cycle. In the grey box for each component, the state during which it conducts is indicated.

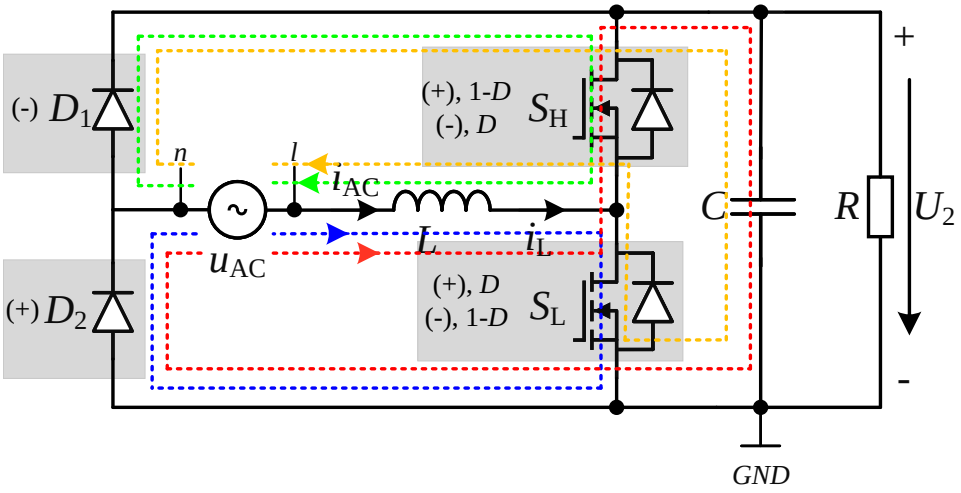


Figure 6.11: Inductor current paths for various switching states of the totem-pole PFC

During the positive mains half cycle of u_{AC}, the blue dotted line shows the path of the inductor current i_L, where the switch S_L conducts during the duty cycle D. The red dotted line indicates the path of i_L when the switch S_H conducts for $1 - D$ interval of the switching period. Additionally, the diode D_2 is forward-biased, and node n is shorted to the GND potential.

During the negative mains half cycle of the input voltage, the green dotted line shows the path of the inductor current i_L, where the switch S_H conducts during the duty cycle D. The yellow dotted line represents the path of i_L when the switch S_L conducts for the

$1 - D$ interval of the switching period. Furthermore, during the negative half cycle of u_{AC}, the diode D_1 is forward-biased, and the GND node is at $-U_2$ potential. This shows that the electromagnetic interference EMI of this topology is similar to the bridgeless boost HPFC discussed previously.

6.3.1 *Current measurement setup*

The inductor current i_L in the totem-pole PFC is aligned with the source current i_{AC} [cf.6.7 top curves]. It includes both positive and negative polarities. The complete i_L can be measured by placing sensors at different points in the rectifier. The type of the sensor depends on its position and the shape of current. For example, any sensor with a bandwidth ranging from a few Hz to MHz can be used in series with the inductor or power transistors. Furthermore, two current transform CT sensors can be placed in series with each transistor to measure the full inductor current. The advantages and the disadvantages of both methods can be concluded from chapter 2.

For the totem-pole PFC, a low-loss current measurement can be achieved using two CTs in series with both transistors S_H and S_L, as the current through the switches consists of the switching pulses. During the positive mains half cycle, the CT sensor in series with S_L outputs for the DT_S interval, while the CT sensor in series with S_H outputs for the $(1 - D)T_S$ interval. During the negative mains half cycle, the CT sensor in series with S_H outputs for the DT_S interval, and the CT sensor in series with S_L outputs for the $(1 - D)T_S$ interval. This is illustrated in Figure 6.12 with reference to the switching signals s_L and s_H which are the control signals for the low-side and high-side switches, respectively. Moreover, the curves drawn above the horizontal axis represent positive values and the curves drawn below the horizontal axis represents the negative values.

The outputs of the current transformer sensors are positive for the positive i_L and negative for the negative flow of the inductor current. Therefore, the analog circuitry must be capable of rectifying the negative output from the current sensors so that the final output voltage signal from the current measurement can be sampled through the analog input pin of the digital signal processor.

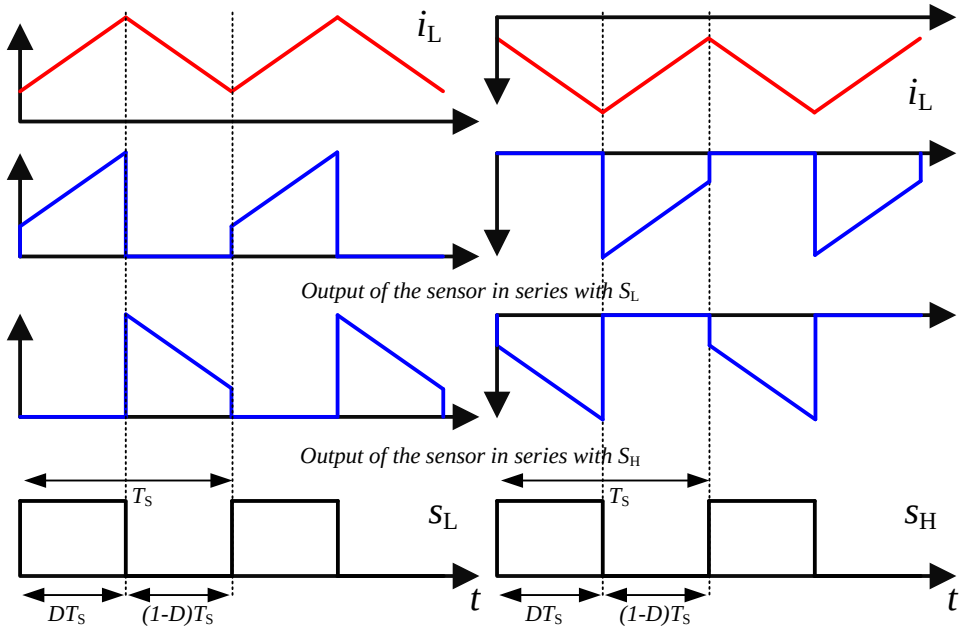


Figure 6.12: Inductor current and output of the sensors in series with the transistors for the positive (left) and the negative (right) mains half cycle

As discussed in the previous topologies, current measurement is proposed using only one current sensor and a digital current observer. Similarly, for this PFC topology, only one current transformer CT is assumed as the physical current sensor in series with the low-side switch S_L. The circuit required further with the CT sensor is shown in Figure 6.13. The current i_S flows through the low-side switch S_L, representing the current through the single turn of the primary winding of the CT. The pink arrow indicates the direction of the current for the positive mains half cycle, while the blue arrow shows the flow of current for the negative mains half cycle.

Small-package logic-level MOSFETs are used to control the flow of the current in the circuit connected to the secondary side of the current transformer. The transistors conducting during the positive mains half cycle are marked with $(+)$, while those conducting during the negative mains half cycle are marked with $(-)$. Two burden resistors are also employed: resistor $R_{B,D}$ produces an output during the positive mains half cycle, represented by $u_{m,D}$, while $R_{B,1-D}$ generates an output during the negative mains half cycle, represented by $u_{m,1-D}$.

The output voltage signals across the burden resistors are connected to the analog input pins of the DSP. Additionally, the common node of the two resistors is considered the analog ground of the measurement circuit.

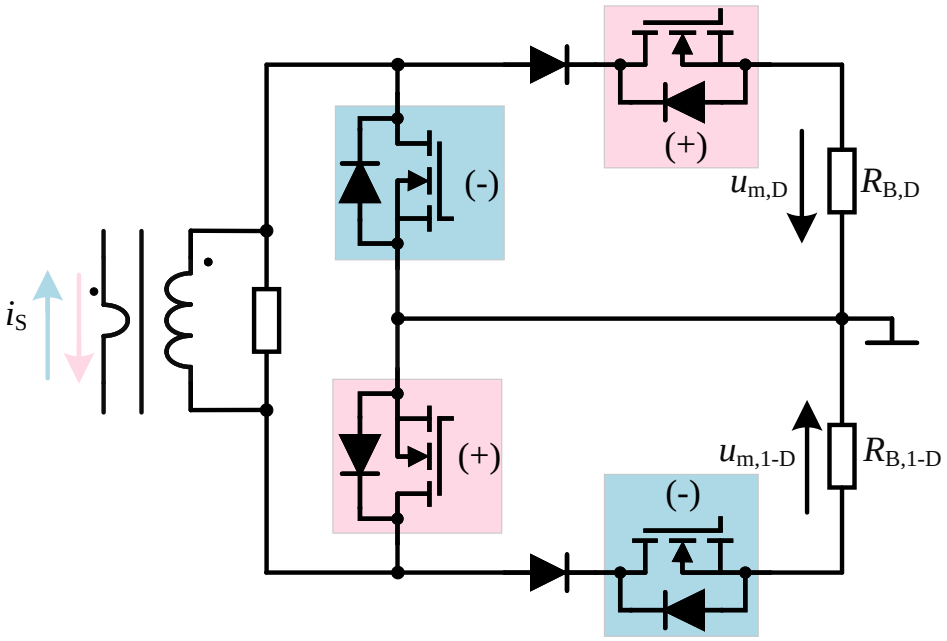


Figure 6.13: Current measurement circuit for the current through the switch S_L

The current measurement shown for the boost HPFC rectifier in figure 6.8 can also be used for this rectifier. In that case, the output voltage u_m need to sample for both T_e and T_a intervals. Further, for the positive mains half cycle the sample at the center of T_e interval and for the negative mains half cycle the sample at the center of T_a interval will be used in computation. Furthermore, the current measurement shown in this section can be used for the boost HPFC rectifier but in that case the instant to sample the voltages across both burden resistors will only be at the center of T_e interval. Moreover, current transformer sensors with single secondary winding have less copper, compact, cheap and easy for series production. Therefore, in this section an alternative to the previously shown method is discussed.

6.3.2 *Current observer realization*

The digital current observer concept can be implemented for the totem-pole PFC using a single current transformer as the physical sensor and secondary windings on the boost inductor. The key difference from previous topologies is the use of two burden resistors for current sensing. However, the basic concept remains the same: the voltage across the burden resistors is used to compute the mean value of the inductor current. Additionally, the voltage signals from the auxiliary windings are employed to step down the inductor voltage for measurement and to estimation the duration of the switching time intervals.

The voltage across the inductor in this rectifier is similar to the bridgeless boost HPFC as shown in Figure 6.9. It is switching between the varying positive and negative voltage levels during each mains half cycle. In the positive mains half cycle, when $s_L = 1$ and $s_H = 0$, the inductor voltage equals to the input AC voltage, u_1 (here: $u_{AC} = u_1$). When $s_L = 0$ and $s_H = 1$, the inductor voltage is $u_L = u_1 - U_2$. During the negative mains half cycle, when $s_H = 1$ and $s_L = 0$, the inductor voltage is u_1, and when $s_L = 1$ and $s_H = 0$, the voltage across the inductor becomes $u_L = U_2 - u_1$. Furthermore, the output voltage signals from the auxiliary windings are similar to those shown in Figure 6.10. This indicates that for the totem-pole PFC, the volt-second product can be estimated in a manner analogous to the bridgeless boost HPFC.

The voltages $u_{m,D}$ and $u_{m,1-D}$ across the burden resistors correspond to the physical inductor current. The shape of the voltage curve $u_{m,D}$ represents the inductor current during the DT_S interval in the positive mains half cycle, while $u_{m,1-D}$ represents the inductor current for the $(1-D)T_S$ interval in the negative mains half cycle. The regular sampling instant of $u_{m,D}$ occurs at the mid point of the DT_S interval, and for $u_{m,1-D}$ the sampling is in the middle of $(1-D)T_S$ interval as shown in Figure 6.14(a). These sampling instants capture the mean inductor current over one switching interval during CCM operation. The equations for the digital current observer, to estimate the inductor current in CCM are presented below.

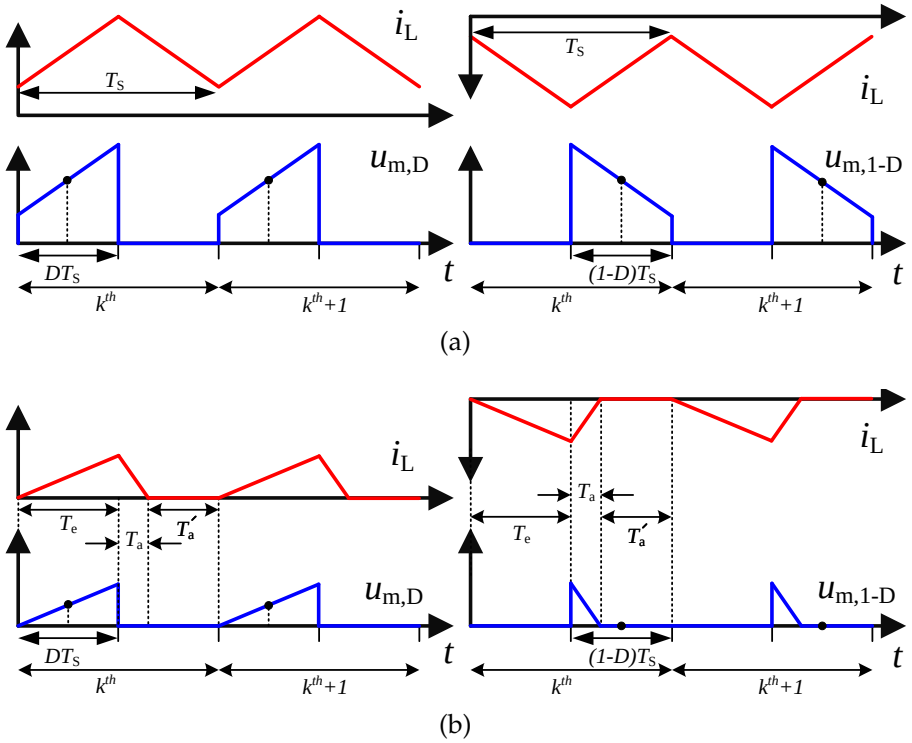


Figure 6.14: Inductor current i_L (red) and the current measurement voltage signals $u_{m,D}$ and $u_{m,1-D}$ (blue) for the positive (left) and the negative (right) mains half cycle for the totem-pole PFC (a) in CCM operation (b) in DCM operation

During the positive mains half cycle

$$K_m I_{Lmax,k} = \frac{1}{2} \frac{K_m}{K_S} \frac{u_{LADC1,k}}{L} \frac{C_{1,k}}{f_{clk}} + u_{m,D,k} \tag{6.14}$$

$$K_m I_{Lmin,k} = -\frac{K_m}{K_S} \frac{u_{LADC2,k}}{L} \frac{C_{2,k}}{f_{clk}} + K_m I_{Lmax,k} \tag{6.15}$$

During the negative mains half cycle

$$K_m I_{Lmax,k} = \frac{1}{2} \frac{K_m}{K_S} \frac{u_{LADC2,k}}{L} \frac{C_{2,k}}{f_{clk}} + u_{m,1-D,k} \tag{6.16}$$

$$K_m I_{Lmin,k} = -\frac{K_m}{K_S} \frac{u_{LADC1,k}}{L} \frac{C_{1,k}}{f_{clk}} + K_m I_{Lmax,k} \tag{6.17}$$

During DCM operation, the totem-pole rectifier experiences three distinct states with time intervals T_e, T_a, and T_a', as shown in Figure 6.14(b). The digital current observer equations for the DCM operation during the positive mains half cycle can be formulated similarly to those for the boost PFC rectifier. Notably, Figure 6.5 can be revisited with the modification that the output of the current transformer measurement circuit is represented as $u_{m,D}$. Consequently, the digital current observer equations for estimating both the maximum and mean inductor currents over one switching interval k are provided below.

$$K_m I_{Lmax,k} = 2 \cdot u_{m,D,k} = \Delta u_{m,k} \tag{6.18}$$

$$K_m I_{Lmed,k} = u_{m,D,k} \cdot \left(\frac{C_{1,k}}{f_{clk}} + \frac{C_{2,k}}{f_{clk}}\right) \cdot f_S \tag{6.19}$$

Estimating the inductor current during the DCM operation for the negative mains half cycle presents a special case. The current measurement output voltage $u_{m,1-D}$ is sampled at the midpoint of the $(1-D)T_S$ interval. At zero crossings, it is possible that the sampled value is zero, as depicted in Figure 6.14(b). The black dots on the $u_{m,D}$ and $u_{m,1-D}$ indicate the sampling instants. Despite this, it remains feasible to implement the digital current observer in this scenario. One approach is to shift the sampling instant at the start of the $(1-D)T_S$ interval and estimate the inductor current ripple. However, this method is generally not recommended in practice due to potential switching noise at the start of the $(1-D)T_S$ interval.

An alternative approach to fully estimate the inductor current involves using only the output signals from the secondary windings of the inductor. The voltage curves for DCM operation during the negative mains half cycle are shown in Figure 6.15. In this approach, the voltage signal u_{LADC2}, which is sampled at the middle of $T_e = DT_S$ and is fed into the ADC input pin of the DSP. Meanwhile, u_{LCAP1} and u_{LCAP2} are used to estimate the duration of the time intervals and are input to the time capture modules of the DSP. The digital current observer equations for estimating both the maximum and

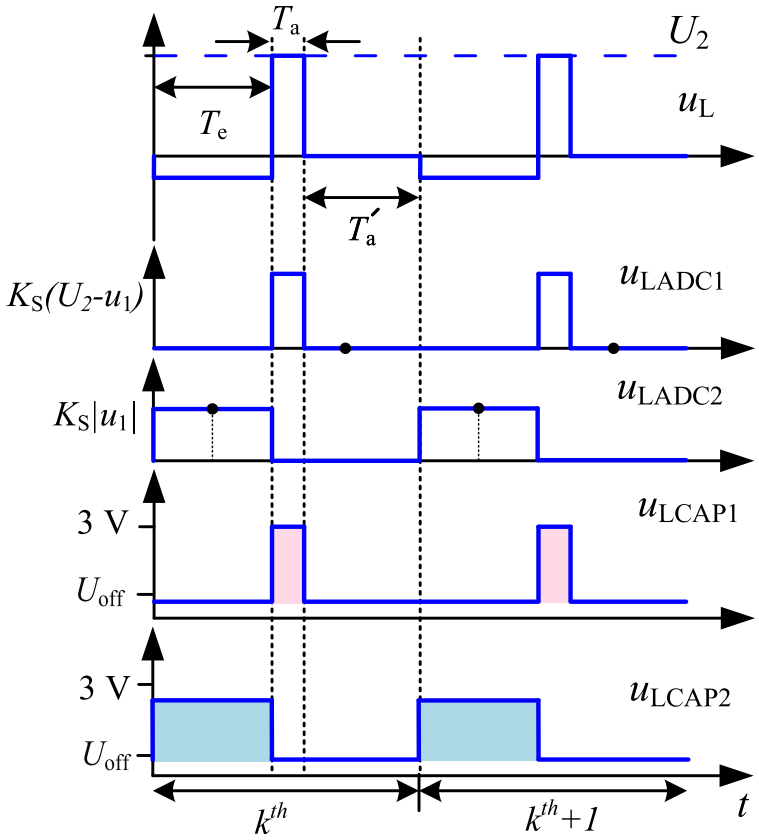


Figure 6.15: Auxiliary windings output voltage curves for the DCM operation during the negative mains half cycle

mean inductor currents over one switching interval k are provided below.

$$K_m I_{Lmax,k} = \frac{K_m}{K_S} \frac{u_{LADC2,k}}{L} \frac{C_{2,k}}{f_{clk}} = \Delta u_{m,k} \tag{6.20}$$

$$K_m I_{Lmed,k} = \frac{K_m I_{Lmax,k}}{2} \cdot \left(\frac{C_{1,k}}{f_{clk}} + \frac{C_{2,k}}{f_{clk}}\right) \cdot f_S \tag{6.21}$$

In all the current observer equations above mentioned, K_m represents the proportionality constant for current measurement, while K_S donates the proportionality constant for voltage conversion. The output of the capture module with the u_{LCAP1} input is indicated as $C1$, and the output of the capture module with u_{LCAP2} input is indicated as $C2$. The frequency of the clock of the DSP or the capture modules is f_{clk}, and f_S represents the switching frequency.

6.4 CLOSED-LOOP CONTROL

This section discusses the implementation of digital control for the power factor correction (PFC) rectifier, as outlined in [39]. The fundamental concept of this control is similar to that described in the previous chapter in 5.1.1. It consists of an inner current control loop based on the average current and an outer voltage control loop [40]. The output voltage, after analog-to-digital conversion $U_{\text{out,ADC}}$, is subtracted from the reference output voltage U^*_{out} to obtain the error signal for the voltage controller. This controller then generates the peak reference value $\hat{u}_{\text{m}}$, which is multiplied by the normalized absolute value of $u_{\text{in,ADC}}$. The result of this multiplication serves as the reference value for the current controller. The current controller produces an output $\hat{d}$ that determines the required adjustment in the duty cycle, in addition to the feed forward duty cycle d_{ff}. The sum of both duty cycles d is then scaled for the PWM logic, which is configured individually for each PFC topology. The control structure of the typical PFC is shown in Figure 6.16. Since the physical inductor current is sensed by the DSP with voltage signals, the internal control variables representing the current are donated by u.

A typical power factor correction rectifier continuously switches between the DCM and CCM operations near the zero crossings of the input voltage. This results in different duty cycle to the inductor current transfer function for the continuous and the discontinuous conduction modes. Consequently, the "Feed Fwd." block must compute the feed forward duty cycle for the CCM operation i.e., $d_{\text{ff,CCM}}$ and the duty cycle for the DCM operation i.e., $d_{\text{ff,DCM}}$. The overall feed forward duty cycle d_{ff} is then determined as the minimum of these two values [41]. The equations for calculating the feed forward duty cycle in the digital signal processor are stated below.

$$d_{\text{ff,CCM}} = 1 - \frac{|u_{\text{in}}|}{U_{\text{out,ADC}}} \tag{6.22}$$

$$d_{\text{ff,DCM}} = \sqrt{d_{\text{ff,CCM}} \cdot \frac{K_{\text{S}}}{K_{\text{m}}} \frac{u^*_{\text{m}}}{|u_{\text{in}}|} \cdot 2Lf_{\text{S}}} \tag{6.23}$$

$$d_{\text{ff}} = \min(d_{\text{ff,CCM}}, d_{\text{ff,DCM}}) \tag{6.24}$$

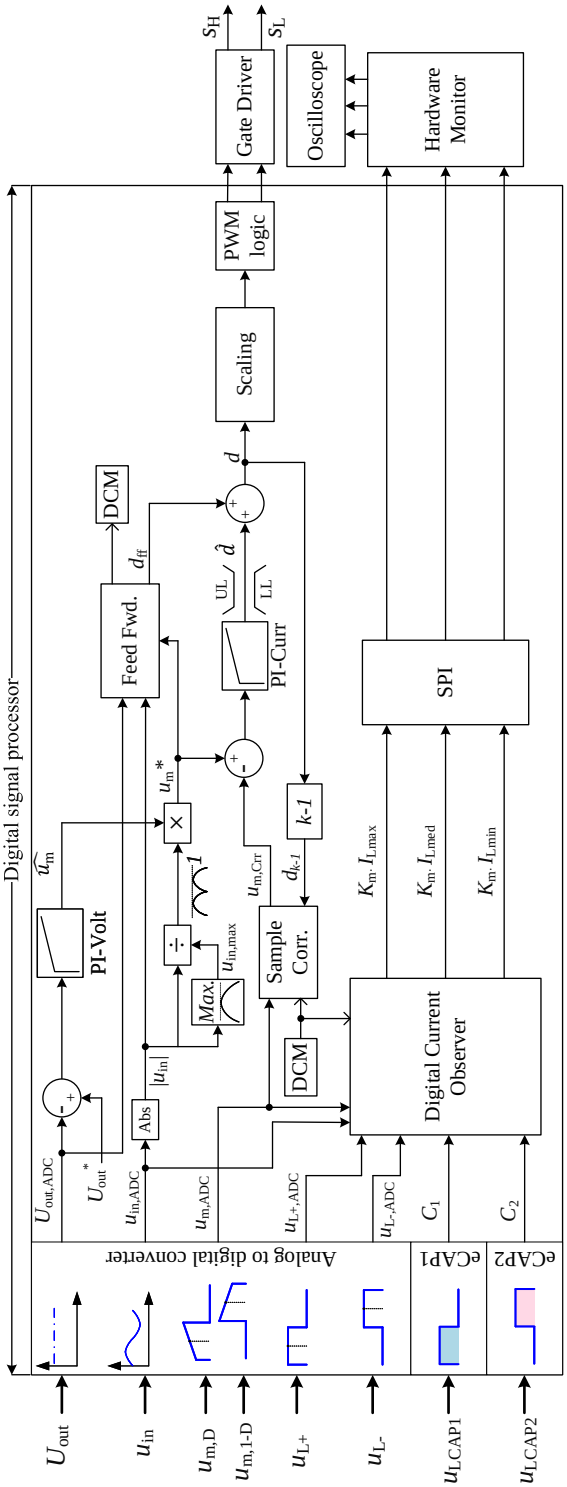


Figure 6.16: Digital closed loop control structure of a typical PFC rectifier

Moreover, the PFC rectifier operates in DCM when $d_{\mathrm{ff,CCM}} > d_{\mathrm{ff,DCM}}$. This condition can be further simplified and can be expressed for the DSP as in Equation 6.24 [42].

$$d_{\mathrm{ff,CCM}} > \frac{K_{\mathrm{S}}}{K_{\mathrm{m}}} \frac{u_{\mathrm{m}}^{*}}{|u_{\mathrm{in}}|} \cdot 2Lf_{\mathrm{S}} \tag{6.25}$$

Hence, the "Feed Fwd." block has three inputs: $U_{\mathrm{out,ADC}}$, $|u_{\mathrm{in}}|$, and u_{m}^{*}. It generates the feed forward duty cycle d_{ff} and outputs a flag variable DCM [43].

The DCM flag is utilized in the sample correction block. During DCM operation of the PFC, the sampled current $u_{\mathrm{m,ADC}}$ does not accurately represent the average current over one switching cycle, unlike in CCM operation [44]. This systematic error should be compensated online using the sample correction block. The equation for the corrected current sample $u_{\mathrm{m,Crr}}$ at a switching instant k is provided in Equation 6.25.

$$u_{\mathrm{m,Crr,k}} = u_{\mathrm{m,ADC,k}} \cdot \frac{d_{\mathrm{k-1}}}{d_{\mathrm{ff,CCM}}} \tag{6.26}$$

In the totem-pole PFC with a single current transformer, operating in DCM during the negative mains half cycle [c.fig6.14(b)], it is possible for the sampled $u_{\mathrm{m,ADC}}$ to be zero, resulting in $u_{\mathrm{m,Crr}} = 0$. To mitigate this sampling error, the output $K_{\mathrm{m}} I_{\mathrm{Lmed}}$ (as given in eq. 6.20) from the digital current observer can be utilized in the sample correction algorithm. Thus, $u_{\mathrm{m,Crr}}$ can be set to $K_{\mathrm{m}} I_{\mathrm{Lmed}}$. This novel approach of integrating the digital current observer into the rectifier control strategy is detailed in the publication by the author [45].

6.5 SIMULATION MODEL

The control concept and digital current observer explained in the previous section are implemented for the three PFC rectifiers in MATLAB/Simulink. The parameters for the rectifiers are given in the Table 8.

The dynamic control theory and the derivation of the gain parameters for the current and voltage controller are similar to the DC-DC boost

Input voltage RMS, u_{AC}	$230\,V \pm 20\%$
Output voltage, U_2	$400\,V$
Switching frequency, f_S	$100\,kHz$
Output power, P_2	$1\,kW$
Boost inductance, L	$219\,\mu H$
Output Capacitance, C	$780\,\mu F$

Table 8: Boost converter simulation parameters

converter and, therefore, are not discussed here. Additionally, in the simulation models, the current measurement is assumed with only one current sensor. For the boost PFC and the totem-pole PFC rectifier, the current sensor position is assumed in series with the low-side switch and for the bridgeless boost HPFC rectifier, it is assumed in series with the transistor.

The simulation results of the boost PFC rectifier are shown in the figures below. The outputs of the current observer algorithm for two mains half cycles are plotted corresponding to the physical inductor current i_L as shown in Figure 6.17. In the curves, the inductor current i_L is low for the first mains half cycle $[0.02\,s - 0.03\,s]$ and it is set high for the second half cycle $[0.03\,s - 0.04\,s]$. In this figure, the DCM detection flag is also plotted. It is high when the PFC is operating in discontinuous mode and it is low for the continuous conduction mode.

The current that flows through the low-side switch in the boost PFC is measured with the current measurement block in the simulation model. It is then sampled to get i_{Lm} as shown in Figure 6.18. It is also further used in the control and in the digital current observer algorithm. The mean value generated by the current observer is plotted in comparison to the i_{Lm} and is shown in the figure below. Moreover, the relative error of the two currents can also be computed with respect to the average current that flows through the inductor for each mains half cycle. In the simulation model, the relative error of i_{Lm} from the average inductor current is 2.67% and the relative error of i_{Lmed} is 0.31%. Due to the presence of the DCM, i_{Lm} shows higher error as compared to the current observer output i_{Lmed}. Hence,

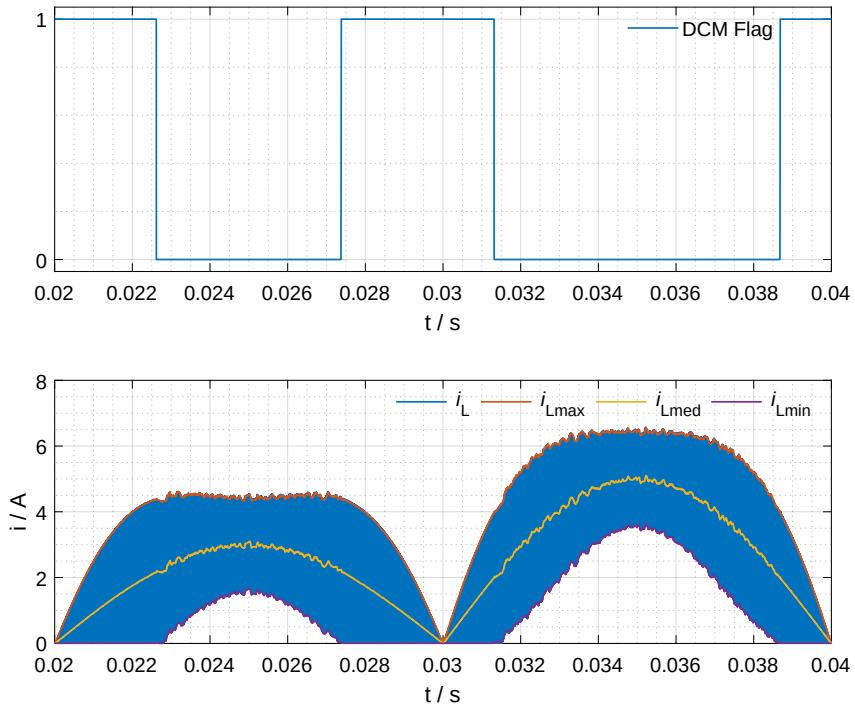


Figure 6.17: Boost PFC simulation model curves, top: DCM detection flag, bottom: current observer outputs with physical inductor current i_L

it validates the digital current observer concept for the boost PFC rectifier.

The simulation modelling is proceeded further to the bridgeless boost HPFC rectifier. For the implementation of the control loops the current measurement block is placed in series with the bidirectional switch. Hence, after the regular sampling of the switch current, it is further used in the inner current control loop and the digital current observer algorithm. The simulation output of the current observer and the *DCM* detection signal for two mains cycles are shown in Figure 6.19. The *DCM* flag is high for the discontinuous operation of the rectifier and it is low for the continuous operation. Moreover, the width of *DCM* flag signal is wider around the zero crossing at 0.01 s as compared to the width around the zero crossings at 0.02 s and

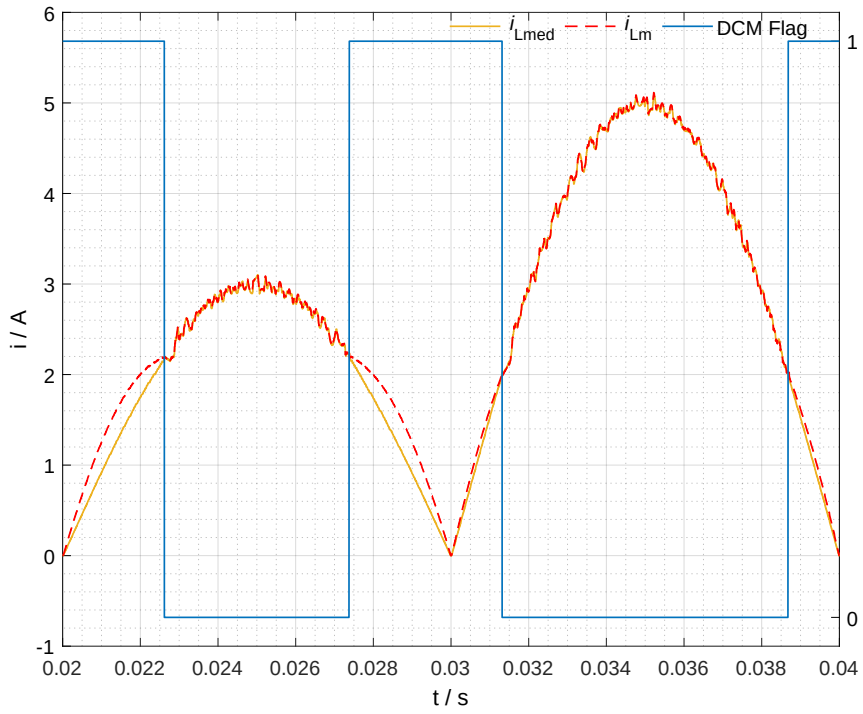


Figure 6.18: Comparison of the sampled current measurement simulation block output i_{Lm} with current observer i_{Lmed} output for the boost PFC rectifier

0.03 s. It is due to the longer DCM operation of the rectifier around 0.01 s as the inductor current required in the first mains cycle is low.

The simulation results can be verified by calculating the percentage of the relative error present in i_{Lmed} and i_{Lm} with respect to the average inductor current over each mains half cycle. In the simulation model, the relative error of the average of $|i_{Lm}|$ from the average $|i_L|$ is 2.59% for the two mains cycle and the relative error of the average of $|i_{Lmed}|$ is 0.34%. This can also be seen in the Figure 6.20 where the two signals are plotted over each other. The difference in the curves is prominent in the DCM operation of the rectifier. It shows lower error in the mean value estimated by the digital current observer.

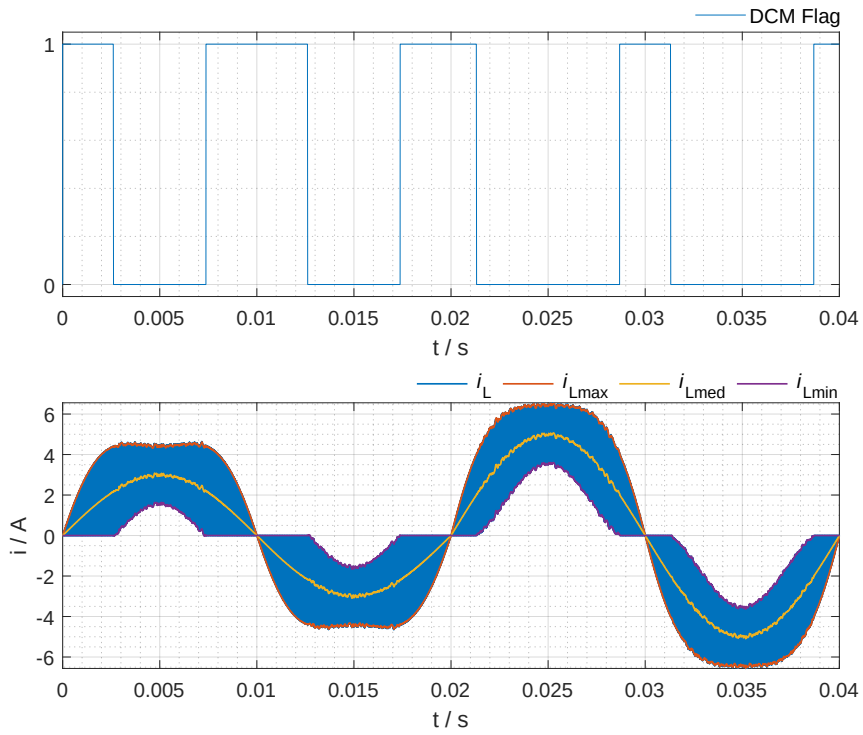


Figure 6.19: Bridgeless boost HPFC simulation model curves for two mains cycles, top: DCM detection flag, bottom: current observer outputs with physical inductor current i_L

The simulation model for the totem-pole PFC is also developed to investigate the digital current observer concept. In this model, the current measurement block is placed in series with the low-side switch as in boost PFC rectifier. Further, the regular sample of this switch current is used as the feedback signal in the current control loop and further in the current estimation. The simulation output of the current observer for the totem-pole PFC and the *DCM* detection signal for two mains cycles are shown in Figure 6.21. These curves are similar to the curves from the simulation model of HPFC rectifier. The *DCM* flag is logic high 1 when the rectifier operates in DCM and it is logic low 0 for the CCM operation. Moreover, the DCM operation stays longer for the low inductor current such as around the zero crossing at 0.01 s.

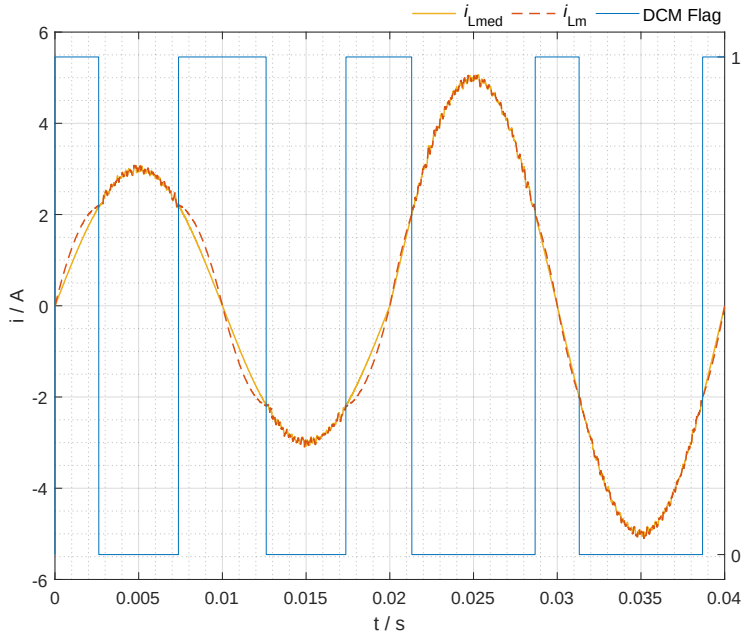


Figure 6.20: Comparison of the sampled current measurement simulation block output i_{Lm} with current observer i_{Lmed} output for the bridgeless boost HPFC rectifier

In the DCM operation during the positive mains half cycle of the totem-pole PFC, the sample correction algorithm has the sample of the current at the center of the measurement pulse [c.fig 6.14(b) $u_{\mathrm{m,D}}$ curve]. This sample represents the half of the ripple of the curve. Therefore, the sample correction works well for the positive mains half cycle. While it is not the case for the DCM operation during the negative mains half cycle [c.fig 6.14(b) $u_{\mathrm{m,1-D}}$ curve]. Now the sample can be corrected based on the assumption that the curve remains sinusoidal [42] or the output i_{Lmed} of the current observer can be used. The mean value from the current observer is based on the measurement signals and it already represents the corrected value as in equation (6.20). The simulation curves from the model are presented in Figure 6.22. Here, three current curves are shown i.e., output of the current observer i_{Lmed}, the sample current from the sensor i_{Lm}, and the corrected value of the sample from sample correction block i_{mCrr}. The bottom plot shows the zoomed in view of the zero crossing at 0.01 s. It can be observed that before the zero crossing the i_{mCrr} curve is close the current observer i_{Lmed}

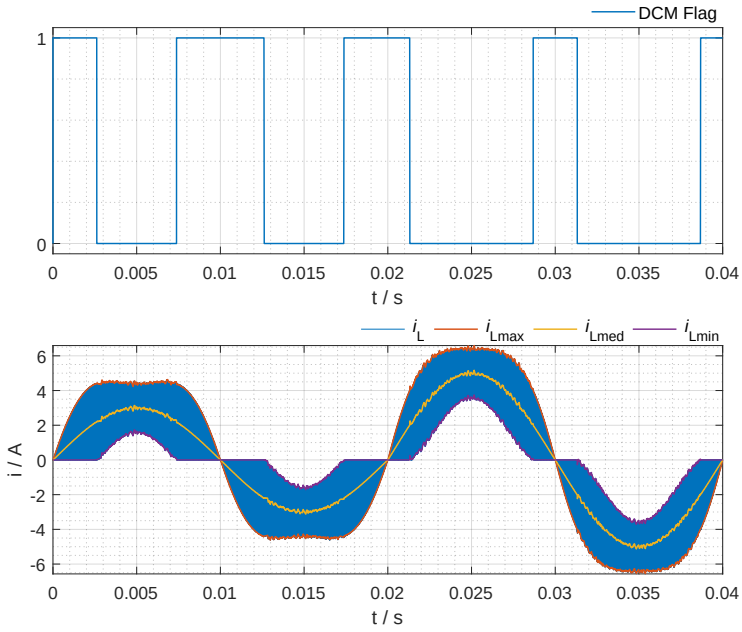


Figure 6.21: Totem-pole PFC simulation model curves for two mains cycles, top: DCM detection flag, bottom: current observer outputs with physical inductor current i_L

because both represents the mean value. Whereas, after the zero crossing, i_{mCrr} deviates from the mean curve. Hence, it shows that the digital current observer concept can be further utilized in the sample correction or in the digital control of the converter.

6.6 EXPERIMENTAL SETUP

To evaluate the simulations of the PFC rectifiers the same self-developed prototype in Section 5.3 [c.fig 5.8] is used. The prototype was previously operated as the boost converter with the DC input directly connected to the boost converter. Now the prototype is adopted for the boost PFC operation with the input to the power stage from the AC source. A single phase bridge rectifier *GSIB*1540 is used to rectify the AC input voltage. The bridge is able to conduct 15 A and has the DC voltage rating of 400 V. The output of the bridge rectifier is then connected to the boost inductor. Hence, the boost PFC power stage is formed. The current measurement setup remains the same as the

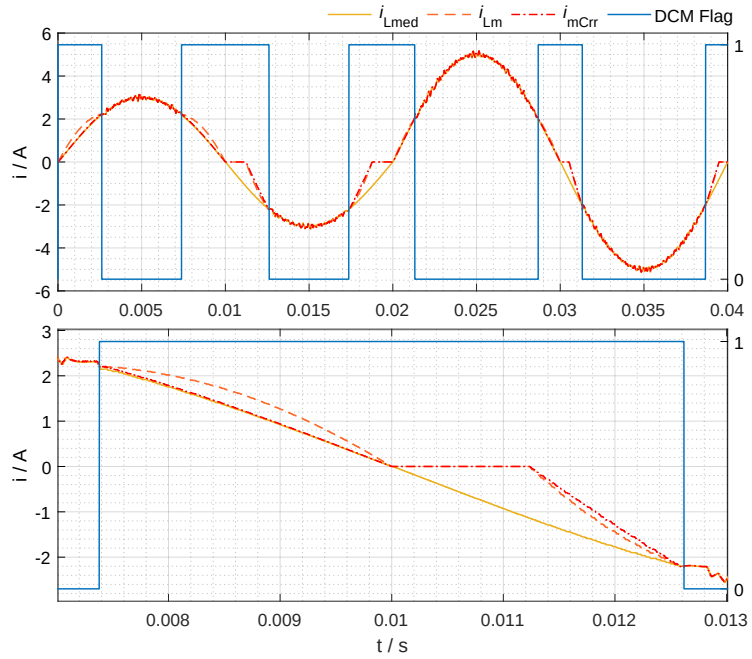


Figure 6.22: Comparison of the sampled current measurement simulation block output i_{Lm} with current observer i_{Lmed} output for the totem-pole PFC rectifier

current is unidirectional like in the boost converter. It consists of single current transformer sensor in series with low-side switch. This gives the output voltage corresponding to the switch current which can be sampled at the analog pin of the digital signal processor.

Furthermore, the bridgeless boost HPFC is also bring to operation on the same prototype. The current measurement sensor is placed in series with the bidirectional switch. The bidirectional switch consists of two discrete switches and are shorted with the source terminals. The core of the current transformer sensor has two windings to sense the bipolar switching current. The output of the two windings are then combined through an analog circuit as discussed previously. The switching frequency for both rectifiers is 100 kHz and the inductance of 219 µH is used. The experimental results are also presented in the publications [45] and [46] by the author. In the below remaining section, the measurements obtained during the research are presented.

The digital control algorithm for the bridgeless boost HPFC rectifier is implemented on the low cost DSP with *F*28035 controller from Texas Instruments . For the validation of the control algorithm and the digital current observer, the registers in the digital signal processor are debugged via UART communication. It is always helpful in the validation of the sampling of the analog signals or the peripheral modules of the processor. The top plots of the Figure 6.23 show the curves of the input voltage and output voltage read by the analog input pins of the DSP. In the bottom section, the curves represent the output of the two capture modules i.e., eCAP and HRCAP.

During the positive mains half cycle, C_1 gives the number of DSP clock cycles for which the voltage across the inductor remains positive and C_2 gives the number of DSP clock cycles for which the voltage across the inductor remains negative. While in the negative mains half cycle, the outputs C_1 and C_2 get swapped because now the voltage across the inductor is negative when the switch is conducting and it is positive when the switch is in blocking state [c.fig 6.10]. Hence, this shows that the capture modules are functioning properly for the corresponding auxiliary winding output signals. Moreover, the curves shows some oscillations due to slow UART communication. For further validation of the digital control and the digital current observer the curves are stored directly from the oscilloscope.

The curves for the rectifier operating at 500 W are shown in Figure 6.24 and Figure 6.25. These figures are the screen shot images taken from the oscilloscope. The yellow colour channel is *C*1, red is *C*2, blue is *C*3 and green is *C*4. The scaling factors are displayed on the images for each curve. The AC input voltage of 230 V RMS is applied to the rectifier and it gives the DC output voltage of 380 V. The frequency of the DC-link ripple voltage can be seen as two times of the frequency of the AC input voltage. Moreover, the inductor current on channel *C*3 is in phase with the input voltage and it shows the power factor correction close to unity. This is achieved in the digital control by multiplying the unity rectified sinusoidal signal with the output of the voltage controller. The rectified sinusoidal signal is formed by dividing the measured input voltage with the maximum value of the input voltage [c.fig. 6.16].

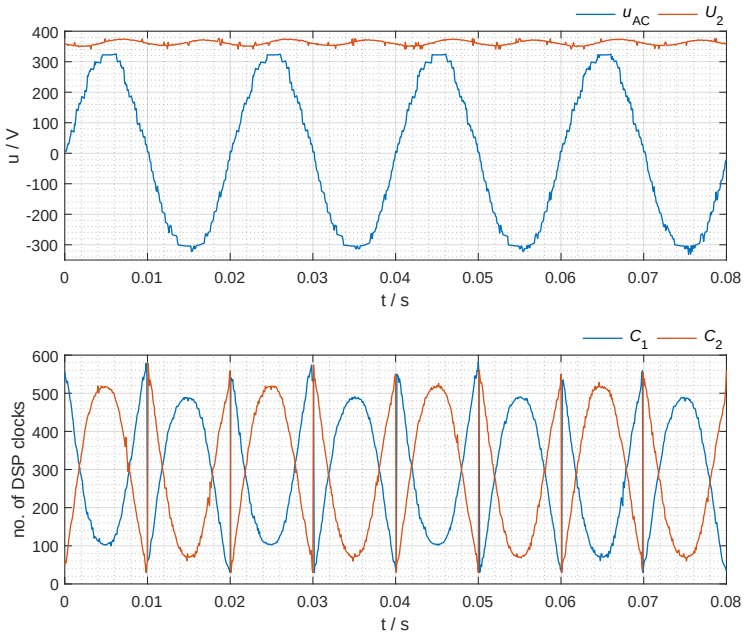


Figure 6.23: UART debugging, top: analog samples of u_{AC} and U_2 scaled to physical values, bottom: output of the capture modules for the bridgeless boost HPFC

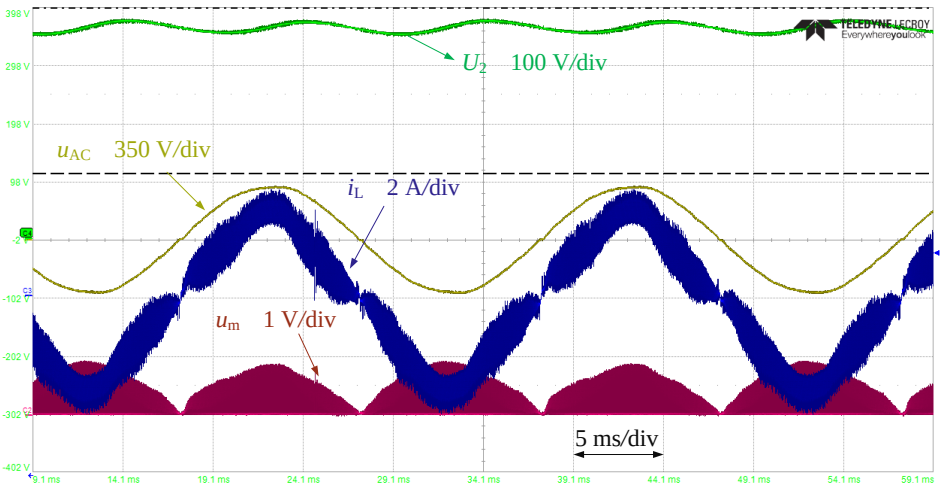


Figure 6.24: Bridgeless boost HPFC curves input voltage u_{AC} $(C1)$, voltage across the burden resistor u_m $(C2)$, inductor current i_L $(C3)$ and output voltage U_2 $(C4)$

Furthermore, the output of the current measurement setup for the bipolar inductor current is displayed on the channel C2. The voltage across the burden resistor u_{m} remains positive for both polarities of the inductor current i_{L}. This voltage consists of pulses and it is regularly sampled at the center of each pulse . Further, it is used in the inner current control loop. The DCM detection flag from the digital control algorithm is shown in green curve in 6.25 corresponding to the input voltage u_{AC} and the inductor current i_{L}. The GPIO output of the *DCM* flag is high 3.3 V at the zero crossings of the input voltage. Hence, these figures validates the digital control algorithm for the PFC rectifier.

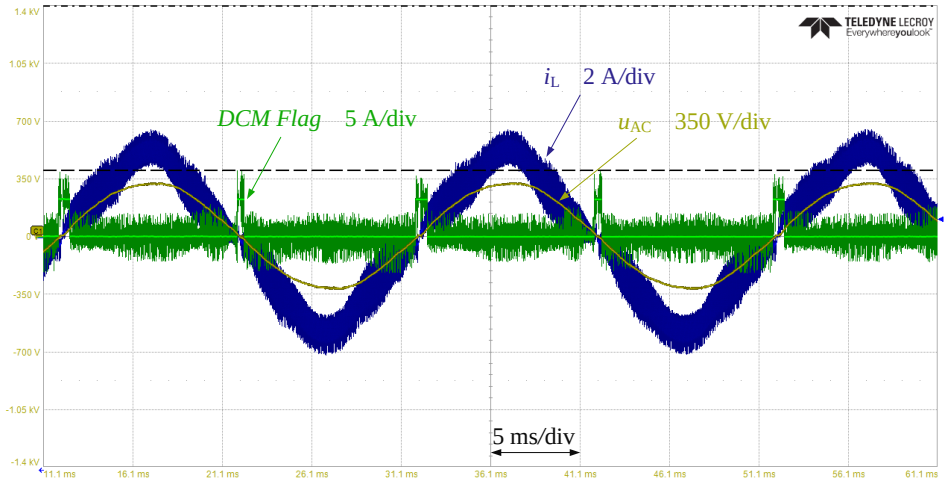


Figure 6.25: DCM detection algorithm validation

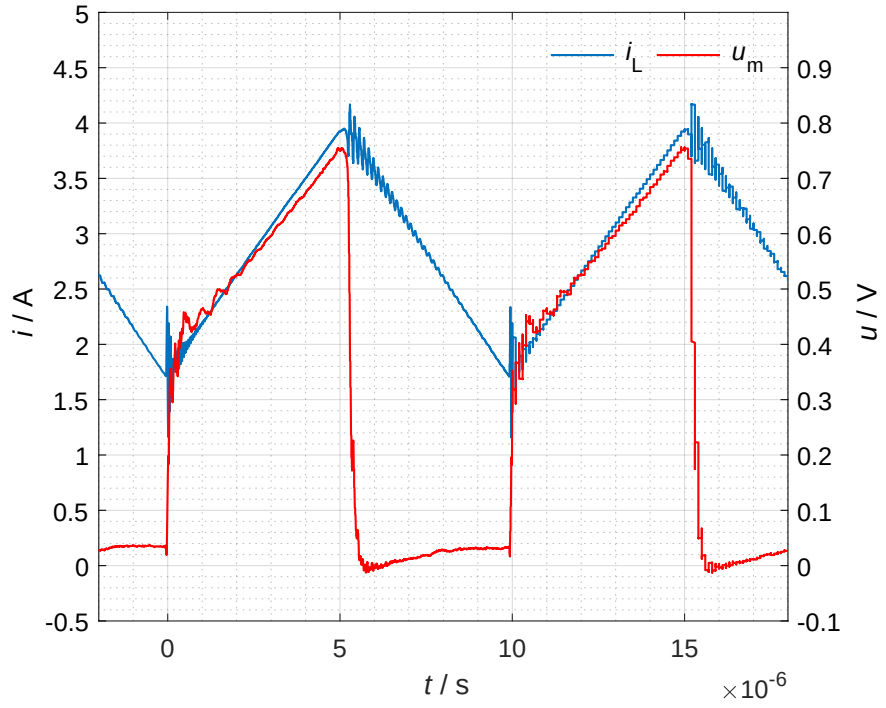
The CT sensor for the boost HPFC rectifier is composed of the ferrite core $(N30)$ from EPCOS TDK electronics. The primary winding is composed of a single turn that carries the current through the bidirectional switch. There are two secondary windings to sense the current for both of the positive and the negative switch currents. Each secondary winding has 70 turns and an analog circuit consisting of a diode and a MOSFET. It is further connected to the burden resistor [c.fig. 6.8]. The burden resistor is selected such that for the maximum and the minimum limits of the physical inductor current the voltage u_{m} does not exceed 3.3 V. As it is directly connected to the analog ADC input pin of the digital processor. The physical inductor current and the burden resistor voltage are recorded from the oscilloscope

and then plotted with MATLAB to analyze the measurement setup. The curves for the two switching intervals during the positive and the negative mains half cycle are shown in Figure 6.26. It shows that the voltage u_{m} is remains positive for the positive and the negative switch current.

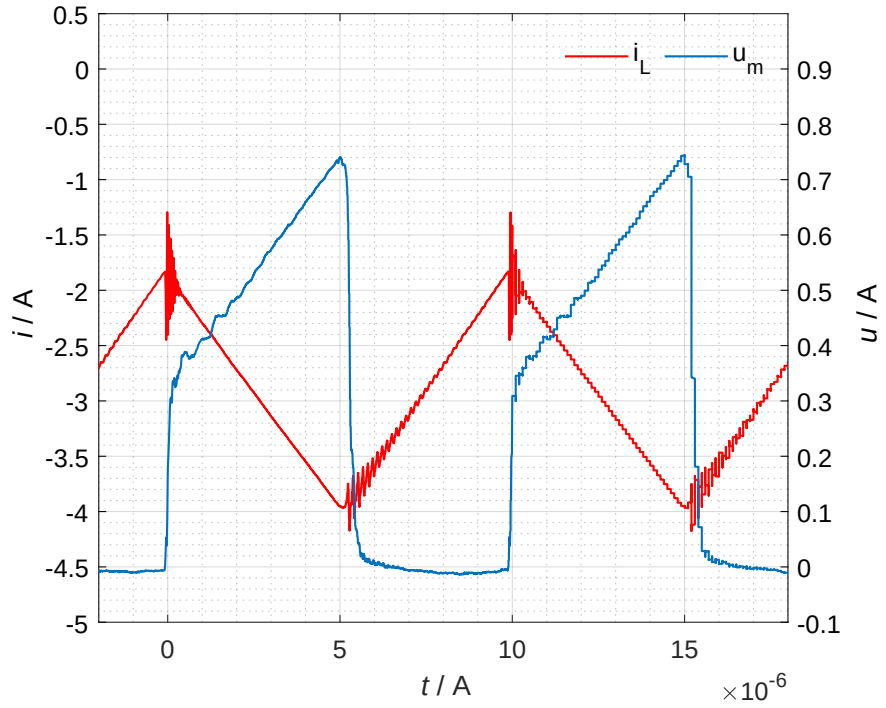
Further, for the validation of the implemented digital current observer, the digital outputs are visualized on the oscilloscope with the help of a SPI-based hardware monitor. The output of the current observer from the scope is recorded and scaled proportionally to the physical inductor current that is measured with the current probe as shown in Figure 6.27. The figure shows the maximum, medium and the minimum values of the estimated inductor current for one switching cycle.

The curves shown in figures 6.26 and 6.27 are obtained for the boost HPFC operating with the AC input voltage $u_{\mathrm{AC}} = 70\,\mathrm{V}$ RMS. Tthe DC output voltage U_2 is 200 V and the switching interval is around the vicinity of the peak voltage u_{AC}. The ripple of the inductor current can be analytically calculated as 2.28 A for the switching frequency of 100 kHz and the inductance of 219 µH. Whereas, the estimated inductor current ripple from the digital current observer comes out to be 2.306 A, it shows an acceptable relative error of 1.18%.

In summary, this chapter has first presented the concept and the digtial equations of the current observer for the three power factor correction rectifiers. It also showed how the inductor current is differently measured in each topology based on the position of the current transformer sensor. Moreover, the digital current observer equations are generalized for the totem-pole rectifier. Because in this rectifier the current through the CT sensor flows in both intervals of DT_{S} and $(1-D)T_{\mathrm{S}}$. Later in the experimental results, a bipolar current in the bridgeless boost HPFC rectifier is estimated with one physical CT sensor and the auxiliary windings over the boost inductor. This measurement setup has shown the acceptable range of relative error. Therefore, it validates the new digital current measurement concept for the power factor correction rectifiers.



(a) during positive mains half cycle



(b) during negative mains half cycle

Figure 6.26: Physical inductor current i_L (red) and the voltage across burden resistor u_m (blue) for two switching intervals

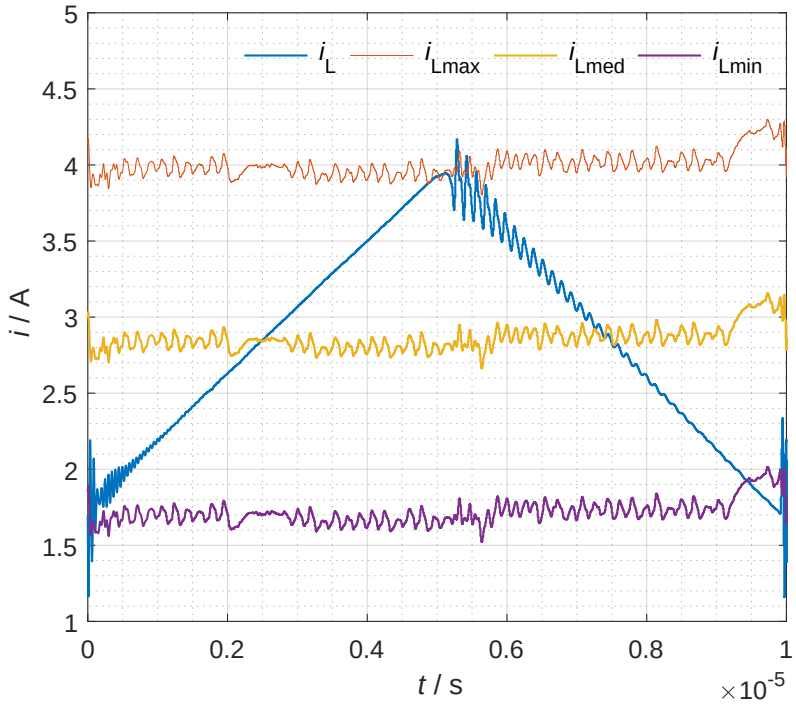


Figure 6.27: Physical inductor current (blue) vs. digital current observer output for one switching interval

7

RESULTS AND ACCURACY ASSESSMENT

In this thesis, the digital current observer for the half-bridge based topologies is proposed and implemented for the DC-DC converters and the AC-DC rectifiers. The implementation of this novel technique requires one current transformer CT sensor and auxiliary windings over the power inductor. The CT based sensor is chosen because it has low power losses, is compact and easy to implement. Moreover, the output of the sensor is isolated from the power stage. The output of the sensor is further sampled by the ADC input pin of the digital signal processor and utilized in the digital control. The voltage signals from the auxiliary windings are the input to the analog-to-digital conversion and the time capture module input pins of the DSP. The analog pins sample the stepped-down voltage across the inductor, and the capture modules estimate the time duration of the switching intervals. Thus, the outputs of the secondary windings are used for the digital estimation of the voltage-time product of the physical voltage across the inductor.

The digital current observer equations for the topologies discussed in the previous chapters are summarized in Table 9. The subscript k indicates the computation at the discrete-time instant k. Furthermore, the frequency of the clock of the DSP or the capture modules is represented with f_{clk} and the switching frequency of the power transistors is represented with f_{S}. Moreover, K_{m} is the proportionality constant between the current sensor output voltage u_{m} and the physical current flowing through the primary turn and has the unit $\frac{V}{A}$. K_{S} is the proportionality constant between the physical inductor voltage u_{L} and the auxiliary winding outputs u_{LADC1} and u_{LADC2} and it is a unit less quantity. The stepped-down voltage signals u_{LADC1} and u_{LADC2} of the secondary windings are sampled at the middle of the switching state. Similarly, the current measurement output voltage u_{m} or $u_{\mathrm{m,D}}$ is sampled at the center of DT_{S} interval, and $u_{\mathrm{m,1-D}}$ is sampled at the center of $(1-D)T_{\mathrm{S}}$ interval. In each topology, two of the time capture modules u_{LCAP1} and u_{LCAP2} are

utilized to estimate the switching intervals in terms of the number clock cycles of the DSP. The outputs of these capture modules are indicated with C_1 and C_2 respectively.

The output of the current observer is scaled with the proportionality constant K_m and it estimates the maximum, mean and minimum value of the inductor current for each switching period. The digital equations for the boost converter represent the simplest case where the inductor current is positive and the converter is operating in CCM. The sample of u_m for a switching interval k gives the mean value $K_m I_{Lmed}$. The maximum value $K_m I_{Lmax}$ for the interval k is determined with the sum of half of the estimated ripple and sampled value of u_m. The ripple is calculated from the product of the sample of u_{LADC1} and the number of DSP clocks C_1 estimated with u_{LCAP1} signal. Whereas, to determine $K_m I_{Lmin}$, the ripple is estimated from the product of the sample of u_{LADC2} and the number of DSP clocks C_2 estimated with u_{LCAP2} signal and it is further subtracted from $K_m I_{Lmax}$. These equations are same for the boost PFC in CCM operation. While for the DCM operation, $K_m I_{Lmax}$ value is twice the sampled value of u_m and $K_m I_{Lmed}$ is estimated by correcting the sampled u_m as in the Table 9.

The current observer equations are further implemented for the topologies where the inductor current is bipolar. For the boost HPFC, the digital equations for the CCM and DCM operation in positive mains half cycle are same as of boost PFC. But for the CCM operation in negative mains half cycle, the estimation of the voltage-time product is changed as documented in section 6.2.2. The digital current observer algorithm is further extended to the totem-pole PFC. The equations for the CCM operation in the positive and negative mains half cycle and the DCM operation in the positive mains half cycle are similar to boost HPFC. The only difference is the sampling instant of the current transformer output signal. For the DCM operation in the negative mains half cycle, $K_m I_{Lmax}$ is determined by estimating the ripple using the sample of u_{LADC2} and the number of DSP clocks C_2 estimated with u_{LCAP2} signal. Furthermore, $K_m I_{Lmed}$ is estimated by finding the average value using $K_m I_{Lmax}$. It can be seen from the Table 9 that the equations for the digital current observer concept can be implemented for various half-bridge based topologies.

Table 9: Digital current observer equations for the half-bridge topologies

Topology	Digital current observer outputs			Mains polarity
	$K_\mathrm{m} I_\mathrm{Lmax,k}$	$K_\mathrm{m} I_\mathrm{Lmed,k}$	$K_\mathrm{m} I_\mathrm{Lmin,k}$	
Boost converter	$\frac{1}{2}\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC1,k}}{L}\frac{C_\mathrm{1,k}}{f_\mathrm{clk}} + u_\mathrm{m,k}$	$u_\mathrm{m,k}$	$-\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC2,k}}{L}\frac{C_\mathrm{2,k}}{f_\mathrm{clk}} + K_\mathrm{m} I_\mathrm{Lmax,k}$	positive, CCM
Boost PFC	$\frac{1}{2}\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC1,k}}{L}\frac{C_\mathrm{1,k}}{f_\mathrm{clk}} + u_\mathrm{m,k}$	$u_\mathrm{m,k}$	$-\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC2,k}}{L}\frac{C_2}{f_\mathrm{clk}} + K_\mathrm{m} I_\mathrm{Lmax,k}$	positive, CCM
	$2 \cdot u_\mathrm{m,k}$	$u_\mathrm{m,k} \cdot (\frac{C_\mathrm{1,k}}{f_\mathrm{clk}} + \frac{C_\mathrm{2,k}}{f_\mathrm{clk}}) \cdot f_\mathrm{S}$	0	positive, DCM
Boost HPFC	$\frac{1}{2}\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC1,k}}{L}\frac{C_\mathrm{1,k}}{f_\mathrm{clk}} + u_\mathrm{m,k}$	$u_\mathrm{m,k}$	$-\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC2,k}}{L}\frac{C_\mathrm{2,k}}{f_\mathrm{clk}} + K_\mathrm{m} I_\mathrm{Lmax,k}$	positive, CCM
	$\frac{1}{2}\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC2,k}}{L}\frac{C_\mathrm{2,k}}{f_\mathrm{clk}} + u_\mathrm{m,k}$	$u_\mathrm{m,k}$	$-\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC1,k}}{L}\frac{C_\mathrm{1,k}}{f_\mathrm{clk}} + K_\mathrm{m} I_\mathrm{Lmax,k}$	negative, CCM
	$2 \cdot u_\mathrm{m,k}$	$u_\mathrm{m,k} \cdot (\frac{C_\mathrm{1,k}}{f_\mathrm{clk}} + \frac{C_\mathrm{2,k}}{f_\mathrm{clk}}) \cdot f_\mathrm{S}$	0	DCM
Totem-pole PFC	$\frac{1}{2}\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC1,k}}{L}\frac{C_\mathrm{1,k}}{f_\mathrm{clk}} + u_\mathrm{m,D,k}$	$u_\mathrm{m,D,k}$	$-\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC2,k}}{L}\frac{C_\mathrm{2,k}}{f_\mathrm{clk}} + K_\mathrm{m} I_\mathrm{Lmax,k}$	positive, CCM
	$2 \cdot u_\mathrm{m,D,k}$	$u_\mathrm{m,D,k} \cdot (\frac{C_\mathrm{1,k}}{f_\mathrm{clk}} + \frac{C_\mathrm{2,k}}{f_\mathrm{clk}}) \cdot f_\mathrm{S}$	0	positive, DCM
	$\frac{1}{2}\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC2,k}}{L}\frac{C_\mathrm{2,k}}{f_\mathrm{clk}} + u_\mathrm{m,1-D,k}$	$u_\mathrm{m,1-D,k}$	$-\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC1,k}}{L}\frac{C_\mathrm{1,k}}{f_\mathrm{clk}} + K_\mathrm{m} I_\mathrm{Lmax,k}$	negative, CCM
	$\frac{K_\mathrm{m}}{K_\mathrm{S}}\frac{u_\mathrm{LADC2,k}}{L}\frac{C_\mathrm{2,k}}{f_\mathrm{clk}}$	$\frac{K_\mathrm{m} I_\mathrm{Lmax,k}}{2} \cdot (\frac{C_\mathrm{1,k}}{f_\mathrm{clk}} + \frac{C_\mathrm{2,k}}{f_\mathrm{clk}}) \cdot f_\mathrm{S}$	0	negative, DCM

The implementation of the digital current observer is validated by computing the relative error of the estimated inductor current ripple Δi_L with the measured physical inductor current ripple with LeCory $CP031A$ current probe. It can measure 30 A RMS up to 1 kHz and at higher frequencies the current measurement capability decreases as shown in Figure 7.1. Moreover, the accuracy in the frequency range of 45 Hz to 65 Hz is $\pm 1.0\%$ and it is determined by measuring the current through a loop of 100 turns which is connected to a function generator [1]. In the experiments, the local frequency of the inductor current is kept 100 kHz and the RMS value lower than 10 A. Therefore, it can be measured with good accuracy with this current probe.

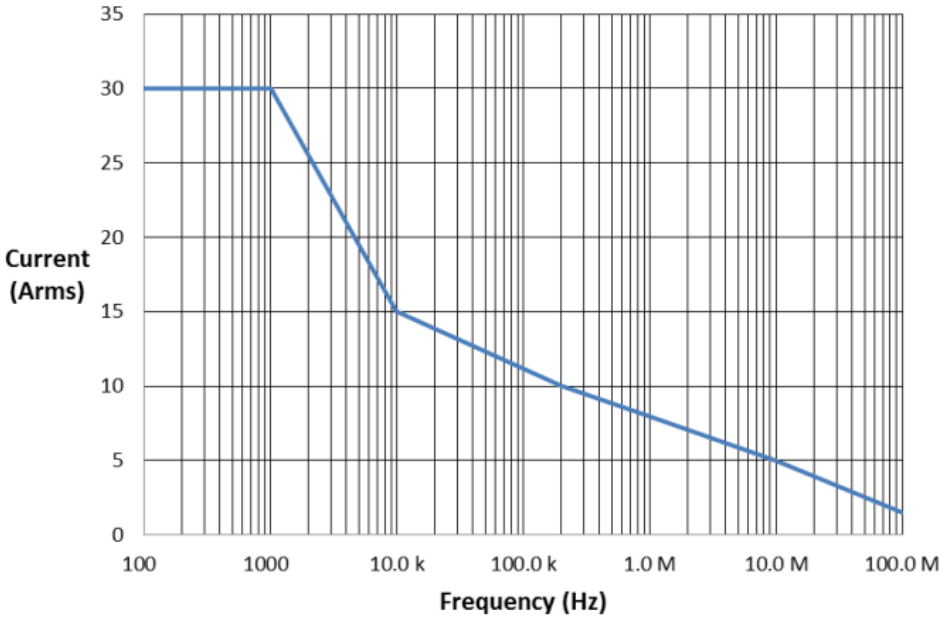


Figure 7.1: Derating curve of the current probe $CP031$ [1]

The boost converter that is discussed in Section 5.3.2 is operated at different loads (i.e., 500 W and 750 W). The input voltage U_1 is varied and the output voltage U_2 is kept constant. This results in a varying inductor current ripple as the duty cycle changes by changing the input voltage. The curves in Figure 7.2 show the results from the experiments. The normalized inductor current ripple (on left vertical-axis) and the relative error (on right vertical-axis) are represented against the normalized input voltage (on horizontal-axis). The curve

of $\frac{\Delta i_L}{i_2}$ is maximum for $\frac{U_1}{U_2} = 0.5$ and the current ripple decreases as the voltage ratio increases or decreases. It is the typical behavior of the boost converter. The black curves (solid and dotted) are representing the relative error in percentage present in the ripple current estimated by the digital current observer for various operations. For all operations the error stays below **1.15** % and it is minimum for the maximum current ripple operation.

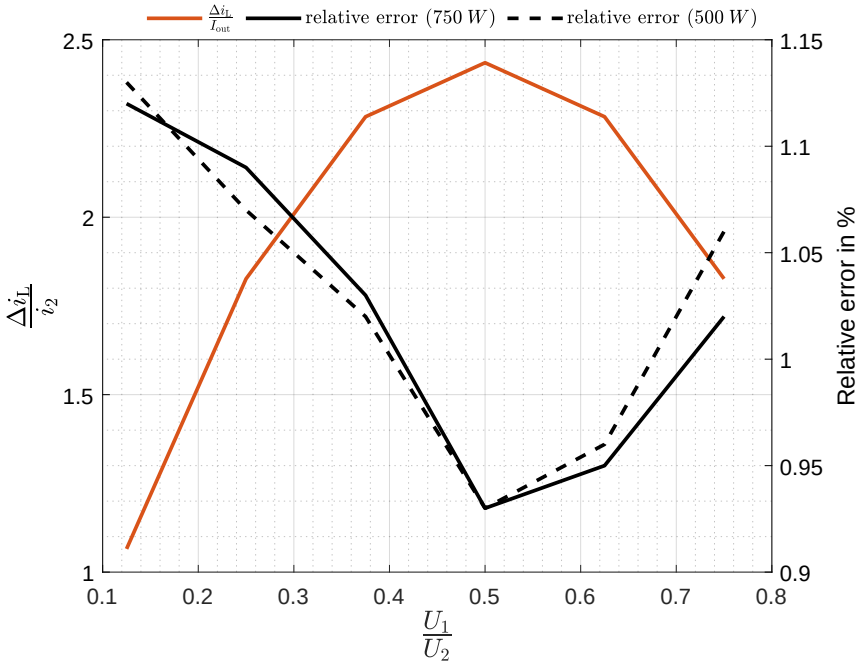


Figure 7.2: Curves of the normalized inductor current ripple and the relative error of the digital current observer implemented for the boost converter

Similarly, the relative error calculated for the bridgeless boost HPFC in Section 6.6 is around **1.18** % for one switching interval. The relative error for one mains half cycle for the bridgeless boost HPFC is also computed. The oscilloscope data is recorded and then plotted in MATLAB for the analysis as shown in Figure 7.3. The mean value of the physical inductor current measured with current probe and the mean value of the digital current observer are computed with MATLAB over 100 Hz cycle. The final relative error between the

current probe measured and the estimated mean remains below **1.2**%.

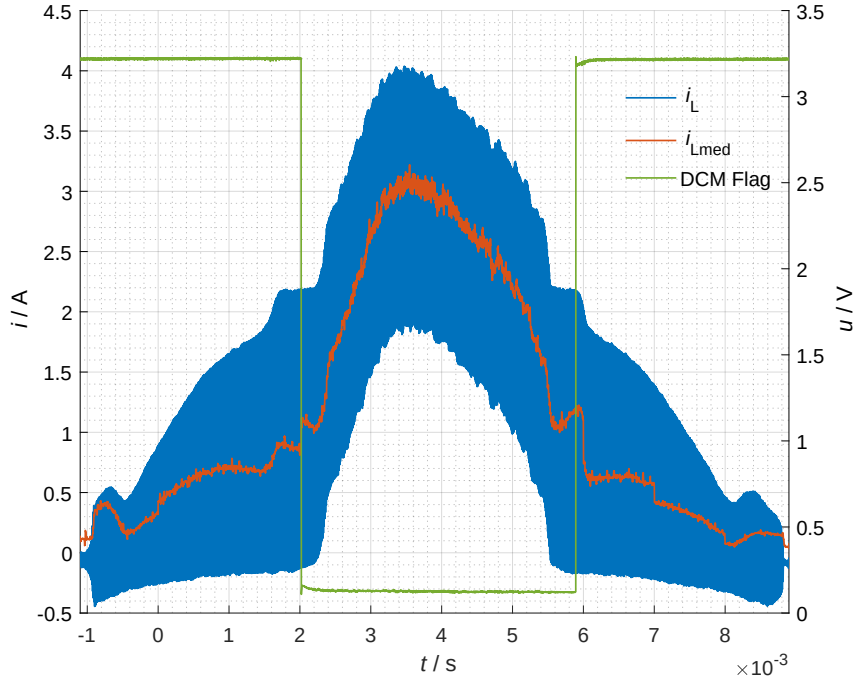


Figure 7.3: Physical inductor current i_{L}, estimated mean from digital current observer i_{Lmed} and DCM detection flag over positive mains half cycle

The possible sources of the relative error are discussed further for the assessment of the measurement data from the self-developed prototype. The accuracy of the implemented digital current observer is mainly depending on its essential components, which are the current transformer CT sensor and power inductor. Therefore, any disturbance on these components will lead to the error in the measurements. The current transformer sensor in the prototype is self-developed on the toroid ring core ($N30$) from EPCOS TDK electronics ($B64290L0652$) [47]. The number of turns of the secondary winding are 70. Hence, for the maximum output voltage of 3 V and $d_{\mathrm{max}} = 0.85$, the maximum magnetic flux density, as determined from equation 5.20, is calculated approximately to 20 mT. This value

is lower than the saturation magnetic flux density of the $N30$ material under the operating switching frequency $(100\,\text{kHz})$ [48]. Therefore, the influence of the disturbances from the saturation of the core of the CT sensor on the output of the digital current observer are low.

The inductor used for the prototype is a standard power coil from KEMET ($SHBC24N\text{-}2R0A0219V$). It has a rated current of 15 A and inductance of 219 µH at zero ampere current. It has a DC resistance of 19.5 mΩ. Further, for such coil inductors, the value of inductance decreases with the increasing current. In this work, for the implementation of the digital current observer equations, the inductance L is assumed constant which is a major shortcoming of the implementation and it is the main cause for the error. Moreover, the effect of the temperature on the inductance and DC resistance are also not considered. Hence, in case of non-ideal conditions, the relative error might increase further. This error can be compensated by the on-line estimation of the inductance L but it is not implemented for the digital current observer algorithm in this work.

The inductance L can be written as $L = u_\text{L}\frac{\Delta t}{\Delta i_\text{L}}$ with the physical inductor voltage u_L and current i_L. This equation can be implemented and estimated in the digital domain. The part $\frac{\Delta t}{\Delta i_\text{L}}$ can be estimated by sampling the current transformer output signal at two know instants. Further, the voltage across the inductor can be ascertained by sampling the auxiliary winding output for the respective switching interval. In this way, the parameter L can be corrected and used in the digital current observer equations.

With the foundational assumptions the relative errors occurring in the measurements are in the acceptable range for both DC-DC converter and AC-DC rectifier. Therefore, these results validate the concept presented in this work. Furthermore, the output of the digital current observer can also be used in the digital control as shown for the totem pole PFC.

8

CONCLUSIONS

At present, the industrial converters and rectifiers mainly utilize either non-isolated shunt-based current sensors or two current transformer sensors in the commutation leg to sense the complete inductor current. These both sensing methods have negative influence on the efficiency and switching behavior of the power transistor. In this dissertation, a simple-to-implement digital current observer for DC-DC converters and AC-DC rectifier is presented. In the proposed scheme, the conventional current measurement with two current transformer sensors in the commutation leg is reduced to one CT sensor. Additionally, auxiliary windings are used over the power inductor to estimate the switching time intervals and to measure the voltage across the inductor.

The scientific progress that this work offers is documented in summary below.

- The measurement of the inductor current has effects on the half-bridge circuit. Moreover, it needs some place on the PCB and also adds cost to the system. This negative influence is reduced first by selecting a low cost and low power loss current sensor i.e., current transformer sensor. Further, it is placed in series with any of the power switches of the half-bridge leg. The output of the CT sensor carries the information of the DC content and the inductor current ripple. The DC content can be obtained by regular sampling of the output of the CT sensor. To estimate the AC content in the inductor current, auxiliary windings are used. Thus, this measurement scheme requires only one physical current sensor.

- The estimation of the voltage-time area of the inductor voltage for the current observer can be implemented in the analog or digital domain. For this work, the digital based solution is investigated. The dedicated time capture modules present in the digital signal processor are configured. The switching time

intervals are estimated in terms of number of DSP clocks from the output voltage signals from the auxiliary windings. Further, the inductor voltage is obtained by regular sampling of the stepped-down voltage from the auxiliary windings. Hence, the product of voltage and time is obtained in the digital domain.

- The digital current observer equations are implemented in the digital domain and verified with the self-developed prototype. The measurement concept is implemented for boost converter and PFC rectifiers. Further, the experimental results have shown an acceptable relative error of **1.2**%.
- The output of the digital current observer can be further used in the digital control of the converter. It is shown in the simulation results of totem-pole PFC, where i_{Lmed} is used during the DCM in the negative mains half cycle. Further, the output of the digital observer can be used to implement other control algorithms such as peak current control. Hence, the use of the current observer can also be extended to the digital control.

Moreover, this concept will be relevant for the converters based on the modern fast switching devices (SiC and GaN) as one of the inductive component is reduced from the commutation leg and this leads to less parasitic inductance and hence offers the opportunity to increase the power density by increasing the switching frequency.

A

APPENDIX

A.1 COMPARISON OF SPACE VECTOR MODULATION SCHEMES

The space vector diagram for the three-level inverter is shown in Figure 1.1. It can be divided into various sectors and smaller triangles. In SVM, the reference voltage signal is generated with the time weighted vectors of the hexagon [24]. Here for simplicity the weighted values are ignored and just vector combination is compared. Moreover, -1,0 or 1 represent the state of the switch for the inverter shown in Figure 3.1.

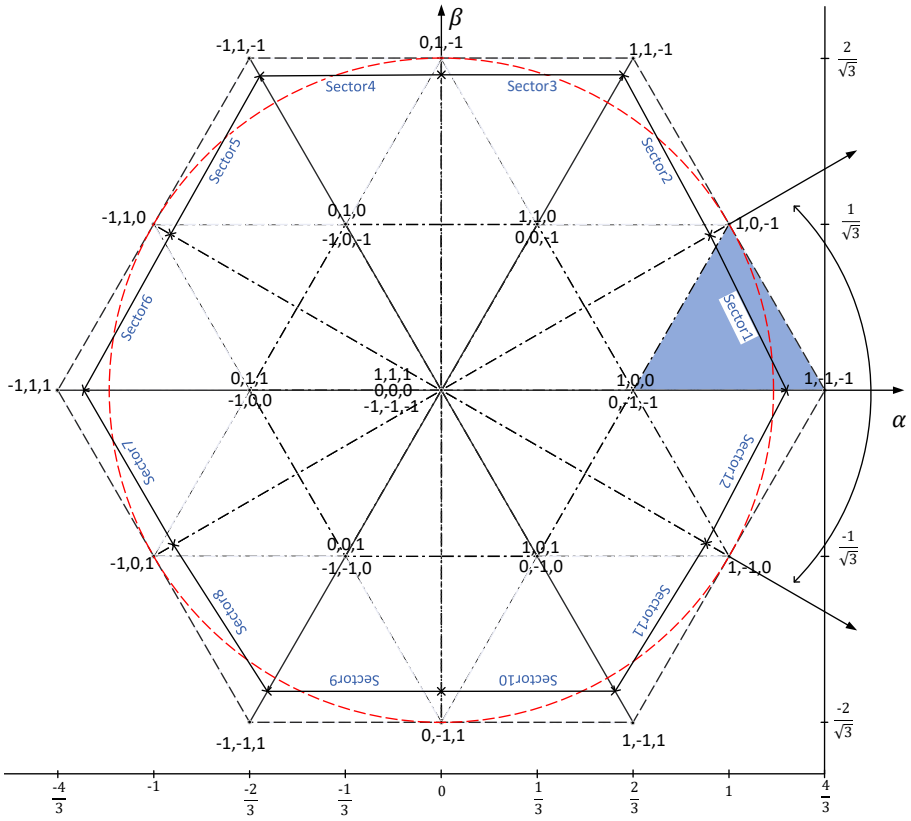


Figure 1.1: Space vector diagram of a three level inverter

For three level inverter, the required reference vector u_{ref} is generated by first finding a new reference vector $u_{\text{ref,new}}$ with respect to the smaller hexagon as shown in Figure 1.2.

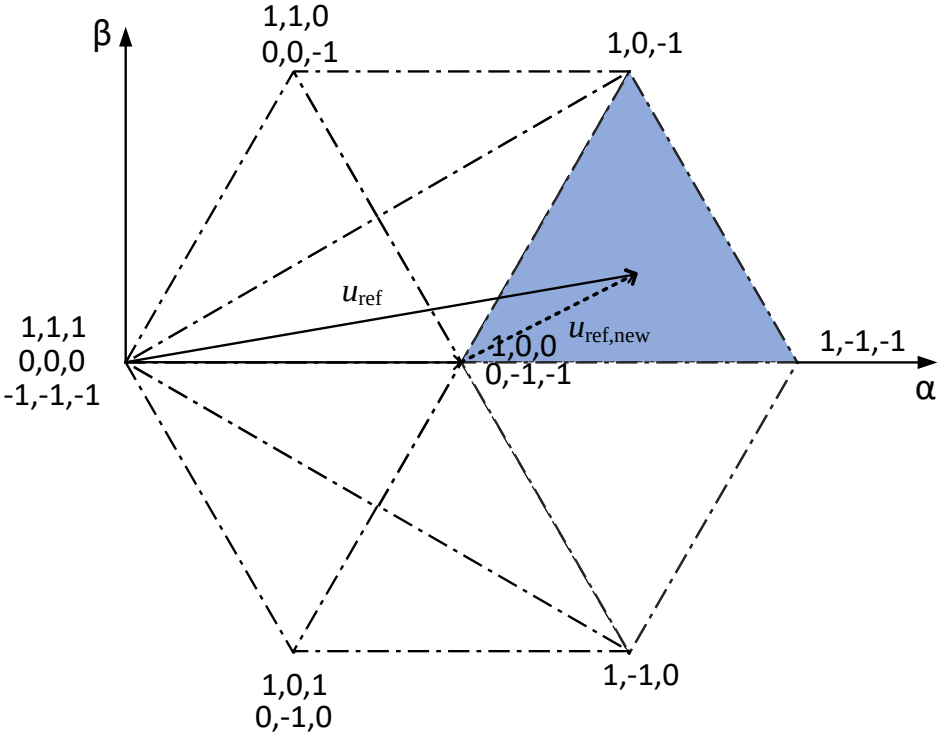
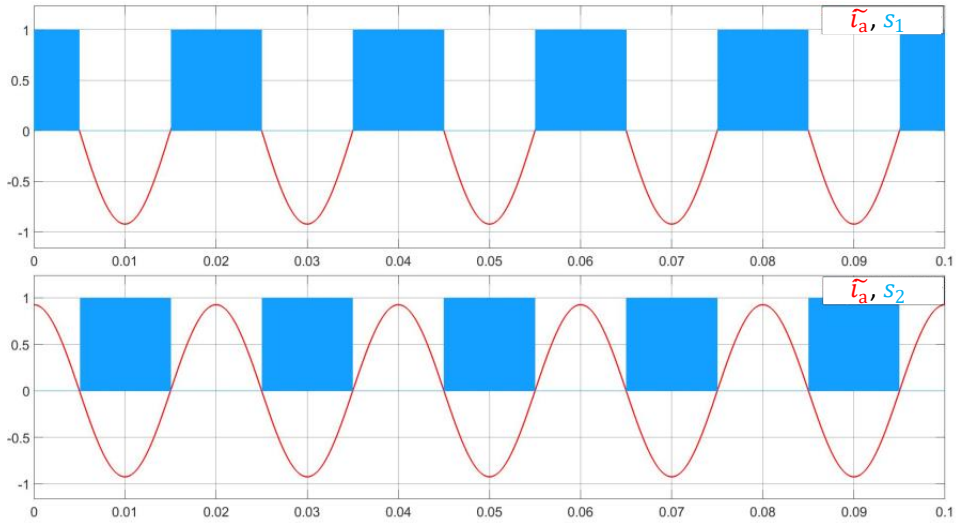


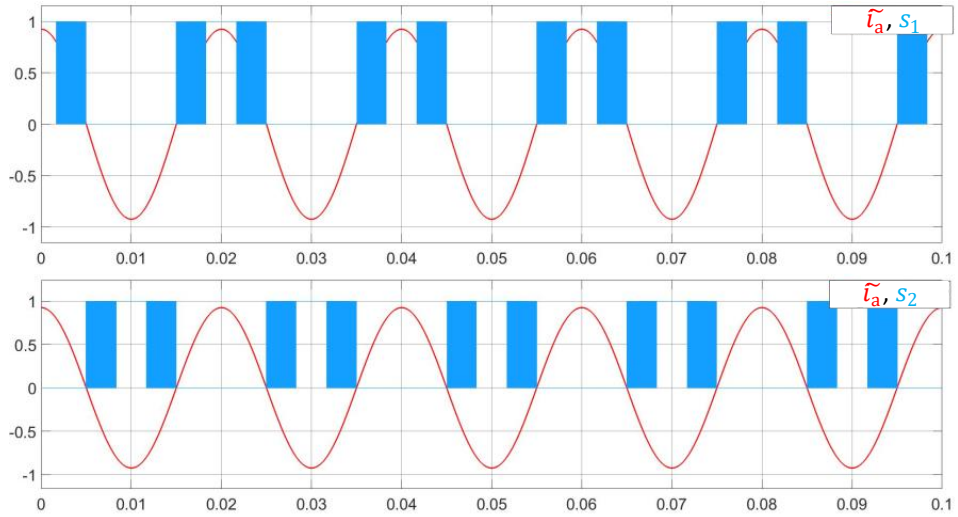
Figure 1.2: Smaller hexagon with center vector $1,0,0$ and $0,-1,-1$

The goal of SVM is to generate the minimum number of switchings in one period. With the standard SVM, the new reference vector $u_{\text{ref,new}}$ can be generated with the vectors as $0,-1,-1 \rightarrow 1,-1,-1 \rightarrow 1,0,-1 \rightarrow 1,0,0 \rightarrow 1,0,-1 \rightarrow 1,-1,-1$. Each vector is applied for a certain time during one period. This shows that the center vectors of the hexagon are occurring twice in one switching period.

With the clamped version of SVM, the new reference vector $u_{\text{ref,new}}$ can be generated with the vectors as $1,-1,-1 \rightarrow 1,0,-1 \rightarrow 1,0,0 \rightarrow 1,0,-1 \rightarrow 1,-1,-1$. Each vector is applied for a certain time during one period. Here only one center vector $1,0,0$ is used. Moreover, the first switch is always clamped to the positive DC rail as it remains 1 for the complete switching period.



(a)



(b)

Figure 1.3: Switching signals s_1, s_2 w.r.t normalized phase current i_a (a) standard SVM (b) 60° clamped SVM

The RMS of the current ripple in case of the 60° clamped SVM is almost twice as compared to the standard version as shown in Figure 1.4. This also implies that the DC-link capacitors have larger voltage ripple in case of the clamped version as compared to the standard space vector modulation.

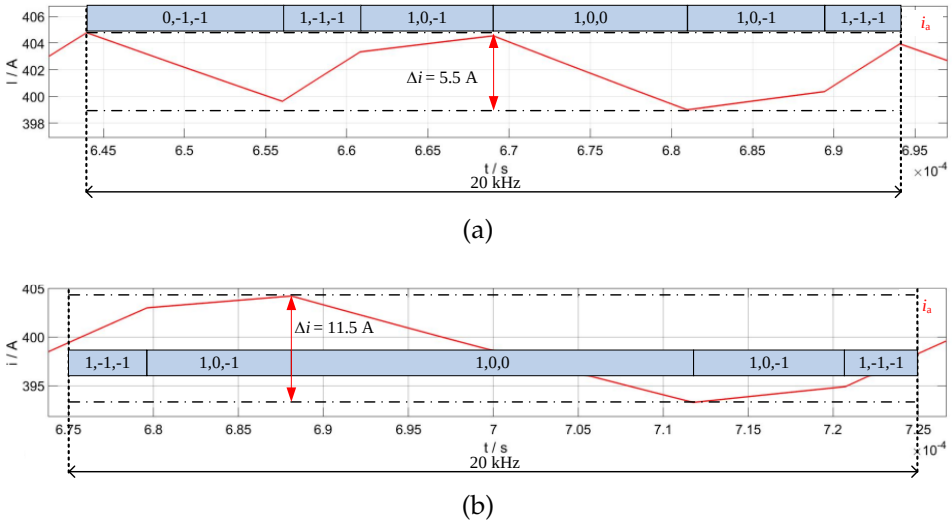


Figure 1.4: Current ripple comparison (a) standard SVM (b) 60° clamped SVM

Moreover, the power losses consisting of the switching and conduction losses can also be compared with simulations. Here the simulation model is developed for a 250 kW three-level inverter with 800 V DC voltage. The comparison of power losses at 10 kHz, 16 kHz and 20 kHz switching frequencies is shown in Figure 1.5. Furthermore, the power losses at multiple modulation index are shown in Figure 1.6. From the simulations, it can be concluded that the power losses due to the conduction and the switching losses for the power stage are reduced by 29 % by utilizing the 60° clamped space vector modulation.

This shows that the switching sequences have a significant effect on the power losses of the inverter.

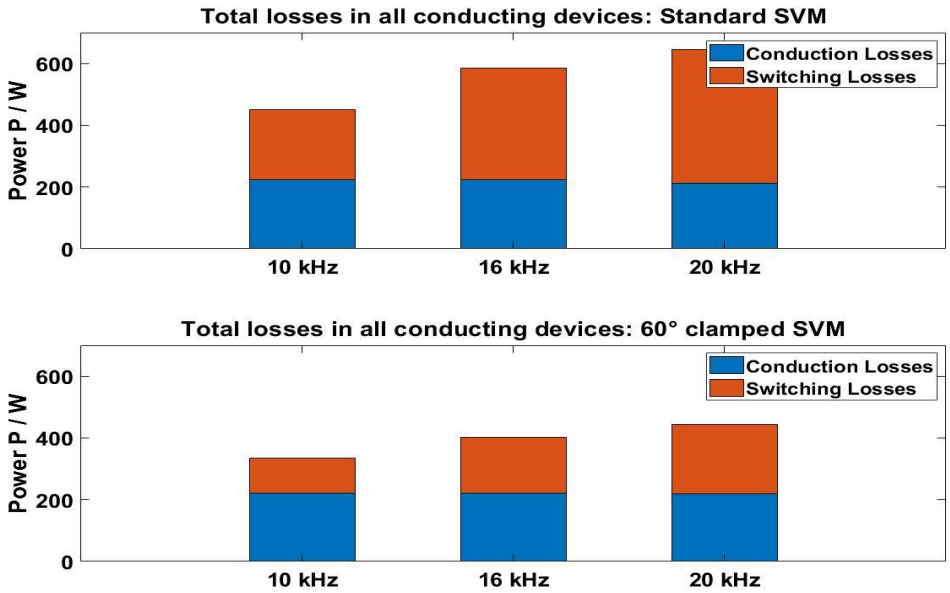


Figure 1.5: Power losses comparison at different switching frequencies

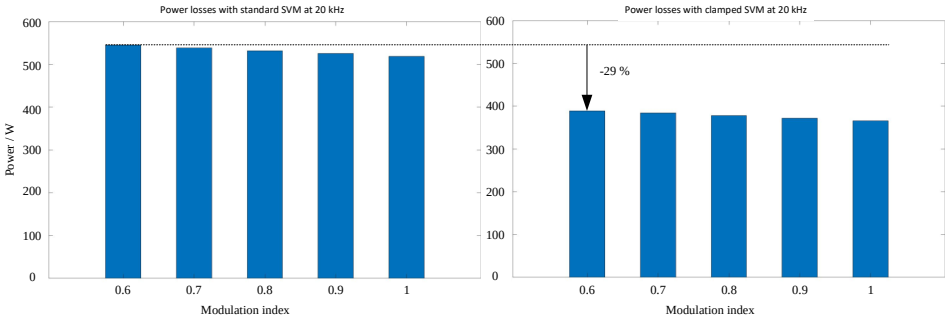


Figure 1.6: Power losses comparison at various modulation index

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