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High-Speed Clock and Data Recovery: Theory and Implementation

DOCTORAL THESIS

**High-Speed Clock and Data Recovery:
Theory and Implementation**

**Takt- und
Datenrückgewinnungsschaltung:
Theorie und Implementierung**

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High-Speed Clock and Data Recovery: Theory and Implementation

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OpenAI	ChatGPT	GPT-5	Spelling, grammar, and language refinement.
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Vorwort

In modernen Kommunikationssystemen wirft eine scheinbar einfache Frage ein grundlegendes Problem auf: Wann wird ein physikalisches Signal zu Information? Ein Signal ist im Grunde nur eine Wellenform. Doch sobald ihr ein sinnvoller Inhalt aufgeprägt wird, muss der Empfänger diesen korrekt interpretieren. Eine zentrale technische Herausforderung besteht darin, dies auch dann zuverlässig zu erreichen, wenn das Signal durch Rauschen, Verzerrungen oder zeitliche Schwankungen der Signalübergänge, oft als Jitter bezeichnet, beeinträchtigt ist.

Diese Dissertation untersucht diese Herausforderung im Kontext einer schnellen Takt- und Datenrückgewinnungsschaltung (engl.: clock and data recovery, CDR) für optische Kommunikationssysteme. Eine CDR muss die Zeitinformation direkt aus dem eingehenden Datenstrom rekonstruieren, selbst wenn die Signalqualität schwankt. Mit steigenden Datenraten wächst daher die Bedeutung stabiler Takt- und Datenrückgewinnungsschaltungen, die die richtige Betriebsfrequenz zuverlässig erfassen können.

Ein wesentlicher Aspekt dieser Arbeit beleuchtet, wie CDRs die korrekte Frequenz besser erkennen und sich darauf synchronisieren können, ohne an Effizienz oder Robustheit einzubüßen. Mithilfe umfangreicher Design-Iterationen, Simulationen und Labormessungen wurde ein Ansatz entwickelt, der den Arbeitsbereich für eine zuverlässige Frequenzakquisition erweitert, bei gleichzeitig minimalem zusätzlichem Schaltungsaufwand und geringerer Leistungsaufnahme. Diese Forschung entstand in enger Zusammenarbeit mit Kolleginnen, Kollegen und Projektpartnern und führte zu mehreren begutachteten Veröffentlichungen.

Ich hoffe, dass die Ergebnisse dieser Arbeit zu einem besseren Verständnis der praktischen Herausforderungen beim Entwurf von schnellen CDR-Schaltungen beitragen und künftige Entwicklungen präziser und energieeffizienter Mixed-Signal-Kommunikationsschaltungen unterstützen.

— Mohammed Iftexhar
Januar 2026
Paderborn

Preface

In modern communication systems, a seemingly simple question reveals a deeper challenge: When does a physical signal become information? A signal is fundamentally just a waveform, but once meaningful content is encoded onto it, the receiver must interpret that content correctly. A central engineering challenge is to achieve this reliably when the signal is impaired by noise, distortion, and variations in the timing of its transitions, often referred to as ‘jitter’.

This thesis investigates these challenges in the context of a high-speed Clock and Data Recovery (CDR) circuit used in optical communication systems. A CDR must extract timing information directly from the incoming data stream, even when the signal quality fluctuates. As data rates continue to increase, the need for stable timing-recovery circuits that can acquire the correct operating frequency reliably becomes increasingly important.

A central focus of this study is the improvement of the frequency-acquisition capability of CDRs without compromising efficiency or robustness. Through extensive design iterations, simulations, and laboratory measurements, an approach was developed to broaden the conditions under which reliable acquisition is achieved while minimizing additional circuit complexity and power consumption. This research was conducted in close collaboration with colleagues and project partners, resulting in several peer-reviewed publications.

I hope that the insights and results presented in this thesis help clarify the practical design challenges of high-speed CDR circuits and support future developments in precise and energy-efficient mixed-signal communication circuits.

— *Mohammed Iftekhar*
January 2026
Paderborn

List of Publications

Conference Publications

- M. Iftekhar, S. Gudyriev, and J. C. Scheytt, "28 Gbps Bang-Bang CDR for 100G PSM4 with Independently Tunable Proportional and Integral Parameters of the Loop Filter in 0.25 μm Photonic BiCMOS Technology," in *2020 IEEE 20th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2020, pp. 26–29. DOI: [10.1109/SIRF46766.2020.9040190](https://doi.org/10.1109/SIRF46766.2020.9040190)
- M. Iftekhar, S. Gudyriev, and J. C. Scheytt, "Reference-less Bang-bang CDR with Enhanced Frequency Acquisition Range Using Static and Modulated Integral Branch Offset Currents," in *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2021, pp. 1–4. DOI: [10.1109/BCICTS50416.2021.9682207](https://doi.org/10.1109/BCICTS50416.2021.9682207)
- M. Iftekhar, H. Gowda, P. Kneuper, B. Sadiye, W. Mueller, and J. C. Scheytt, "A 28-Gb/s 27.2mW NRZ Full-Rate Bang-Bang Clock and Data Recovery in 22 nm FD-SOI CMOS Technology," in *2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2023, pp. 191–194. DOI: [10.1109/BCICTS54660.2023.10310954](https://doi.org/10.1109/BCICTS54660.2023.10310954)
- M. Iftekhar, B. Sadiye, W. Mueller, and J. C. Scheytt, "A 50 Gbps Reference-Less NRZ Full-Rate Bang-Bang CDR with Automatic Frequency Acquisition in 130nm SiGe:C BiCMOS Technology," in *2025 IEEE Nordic Circuits and Systems Conference (NorCAS)*, 2025, pp. 1–7. DOI: [10.1109/NorCAS66540.2025.11231203](https://doi.org/10.1109/NorCAS66540.2025.11231203)

Patent

- M. Iftekhar and J. C. Scheytt, "Enhanced pll circuit," Patent LU000000500939B1, 2023

Other Publications

- B. Sadiye, M. Iftekhar, W. Mueller, and J. C. Scheytt, "60-Gb/s 1:4 Demultiplexer in 22-nm FD-SOI Technology Using TSPC Logic: A Circuit-to-System-Level Analysis and Design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, pp. 1–13, 2025. DOI: [10.1109/TVLSI.2025.3625787](https://doi.org/10.1109/TVLSI.2025.3625787)

Zusammenfassung

Takt- und Datenrückgewinnungsschaltung: Theorie und Implementierung

Diese Arbeit behandelt die Theorie und Implementierung einer referenzlosen Full-Rate Non-Return-to-Zero (NRZ) Bang-Bang Clock and Data Recovery (BBCDR), die für optische Hochgeschwindigkeits-Transceiver in hybrider und Electronic-Photonic Integrated Circuits (EPIC)-Integration entwickelt wurde. Basierend auf dem nichtlinearen Alexander-Phasendetektor (PD) zur inhärenten Taktrückgewinnung und Neutaktung der Daten (Retiming) werden umfassende nichtlineare Modelle erstellt. Diese charakterisieren die Phase-Locked Loop (PLL) zweiter Ordnung mit getrenntem Proportional- und Integralzweig.

Zur Überwindung des durch strenge Jitter-Anforderungen limitierten Akquisitionsbereichs wird ein neuartiges Verfahren zur Frequenzakquisition vorgestellt. Dabei wird die nominelle Frequenz des spannungsgesteuerten Oszillators (engl.: Voltage Controlled Oscillator, VCO) während des PLL-Betriebs gezielt verstimmt. Dies erfolgt entweder durch eine extern angelegte modulierte Offsetspannung oder durch einen modulierten Offsetstrom, der in den Integralzweig injiziert wird. Diese kontrollierte Verstimmung erweitert den Akquisitionsbereich über den einer herkömmlichen BBCDR-Architektur hinaus, bei nur geringfügig höherer Komplexität und Leistungsaufnahme. Darüber hinaus ermöglicht eine permanente Offsetmodulation eine Automatisierung des Akquisitionsprozesses.

Die theoretischen Grundlagen der vorgeschlagenen Techniken sowie deren Betriebsbedingungen und Grenzen werden ausführlich diskutiert. Während die Modulation des Offsetstroms eine Akquisition über den gesamten Abstimmbereich des VCO ermöglicht, deckt die externe Offsetspannungsmodulation etwa ein Drittel dieses Bereichs ab. Die vorgeschlagenen Techniken wurden anhand von Messungen an Full-Rate NRZ-BBCDR-Schaltungen validiert, die in verschiedenen Halbleitertechnologien gefertigt wurden, von 250 nm Silicon Germanium (SiGe)-Bipolar CMOS (BiCMOS) bis 22 nm Fully Depleted Silicon On Insulator (FD-SOI) CMOS. Die Ergebnisse zeigen eine effektive Erweiterung des Akquisitionsbereichs, ein energieeffizientes Design und die Eignung für optische Hochgeschwindigkeits-Kommunikationssysteme der nächsten Generation.

Abstract

High-Speed Clock and Data Recovery: Theory and Implementation

This work presents the theory and implementation of a reference-less, full-rate Non-Return-to-Zero (NRZ) Bang-Bang Clock and Data Recovery (BBCDR) designed for high-speed optical transceivers in hybrid and Electronic-Photonic Integrated Circuits (EPIC) integration. Utilizing the transition-based nonlinear Alexander Phase Detector (PD) for inherent clock recovery and data retiming, comprehensive nonlinear models are developed to characterize the second-order Phase-Locked Loop (PLL) with distinct proportional and integral branches.

To overcome the limited acquisition range constrained by stringent jitter requirements, a novel frequency acquisition technique is introduced. The technique employs either a modulated offset voltage applied externally to the Voltage Controlled Oscillator (VCO) or a modulated offset current applied within the integral branch to deliberately detune the nominal VCO frequency during PLL operation. This controlled detuning extends the acquisition range beyond that of a conventional BBCDR architectures, while only marginally increasing complexity and power dissipation. Moreover, permanent offset modulation automates the acquisition process.

Theoretical foundations of the proposed techniques, along with their operating conditions and limitations, are discussed in detail. Offset current modulation enables full acquisition across the entire VCO tuning range, whereas external offset voltage modulation achieves approximately one-third coverage. The proposed techniques are validated through measurements on full-rate NRZ BBCDR chips fabricated across diverse technology nodes, ranging from 250 nm Silicon Germanium (SiGe) Bipolar CMOS (BiCMOS) to 22 nm Fully Depleted Silicon On Insulator (FD-SOI) CMOS. The results demonstrate effective acquisition range extension, power-efficient design, and suitability for next-generation high-speed optical communication systems.

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I am deeply grateful to my first mentor, M.Sc. Sergiy Gudyriev, who introduced me to the art of chip design—from schematic creation and tapeout to measurement and debugging of fabricated chips. His insightful guidance, constant support, and constructive feedback have been instrumental throughout my research journey. Special thanks to my colleagues—Christian, Saed, Abdul, Maxim, Pascal, Meysam, Harshan, Vijaylakshmi, Uwe, and Rita—for their invaluable support and collaboration. I also sincerely appreciate Babak Sadiye’s dedication, often spending nights and weekends in the lab, providing critical reviews and insightful feedback. I am thankful to all my coauthors, whose collaboration enriched this work. Likewise, I appreciate the master’s students I had the privilege to supervise; their enthusiasm and inquiries also contributed to my own learning. I would also like to thank Birgit for her invaluable administrative support, which greatly facilitated the smooth progress of my research. Additionally, I am grateful to the reviewers of my publications for their thoughtful comments and constructive criticism, which helped improve the quality of this work.

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List of Abbreviations

ADC	Analog-to-Digital Converter.
BBCDR	Bang-Bang Clock and Data Recovery.
BBPD	Bang-Bang Phase Detector.
BEOL	Back End Of Line.
BER	Bit Error Rate.
BiCMOS	Bipolar CMOS.
BPD	Balanced Photodiode.
CDR	Clock and Data Recovery.
CML	Current Mode Logic.
CMOS	Complementary Metal-Oxide-Semiconductor.
CP	Charge Pump.
DAC	Digital-to-Analog Converter.
DJ	Deterministic Jitter.
DP-IQM	Double Polarization - IQ Modulator.
DSP	Digital Signal Processor.
ECL	Emitter Coupled Logic.
EIC	Electronic Integrated Circuits.
EPIC	Electronic-Photonic Integrated Circuits.
FBB	Forward Body Bias.
FD	Frequency Detector.
FD-SOI	Fully Depleted Silicon On Insulator.
FEOL	Front End Of Line.
FLL	Frequency-Locked Loop.
FoM	Figure of Merit.
GF	GlobalFoundries.
HBT	Heterojunction Bipolar Transistor.
HF	High Frequency.
IHP	Innovations for High Performance Microelectronics.
IMDD	Intensity Modulation with Direct Detection.
ISI	Inter Symbol Interference.
JGEN	Jitter Generation.
JTF	Jitter Transfer Function.
JTOL	Jitter Tolerance.

LD	Lock Detector.
LF	Loop Filter.
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor.
NMOS	Negative Channel Metal Oxide Semiconductor.
NRZ	Non-Return-to-Zero.
PAM	Pulse-Amplitude-Modulation.
PD	Phase Detector.
PDF	Probability Density Function.
PFD	Phase Frequency Detector.
PIC	Photonic Integrated Circuit.
PLL	Phase-Locked Loop.
PMOS	Positive Channel Metal Oxide Semiconductor.
PR	Phase Roller.
PRBS	Pseudorandom Binary Sequence.
PSD	Power Spectral Density.
PSM4	Parallel Single-Mode four-channel.
PVT	Process, Voltage, and Temperature.
QAM	Quadrature Amplitude Modulation.
RBB	Reverse Body Bias.
RJ	Random Jitter.
RPFD	Rotational Phase Frequency Detector.
RX	Receiver.
SAW	Surface Acoustic Wave.
SCL	Source Coupled Logic.
SiGe	Silicon Germanium.
SiGe:C	Silicon Germanium:Carbon.
SNR	Signal-to-Noise Ratio.
TIA	Transimpedance Amplifier.
TIE	Time Interval Error.
TX	Transmitter.
UI	Unit Interval.
VCO	Voltage Controlled Oscillator.

Chapter 1

Introduction

Cloud and internet service providers are continually expanding global data center capacity. This expansion is a main driver of increasing data communication within and outside of the data centers. Ethernet plays a central role in supporting this growth in communication capacity. Ethernet's utilization across various sectors is driving significant technological advancements, as shown in Fig. 1.1 [1]. Data centers currently account for approximately 1–1.5 % of worldwide electricity consumption. Between 2010 and 2022, the data center switch bandwidth increased nearly 80-fold to nearly 50 Tbps, while network equipment power consumption rose by a factor of about 22.

Major companies face sustainability challenges and opportunities that drive demand for higher link speeds and improved energy efficiency in Ethernet technology. Wireline transmission occurs over various physical mediums, such as copper wires or optical fibers, depending on the communication range. However, optical fiber transmits data using light at frequencies far higher than those of electrical signals in copper wire, enabling substantially greater data rates and making it an increasingly preferred transmission medium [2]. Cost-effective optical solutions such as pluggable, on-board, and co-packaged optics are driving significant innovation in the market, as shown in Fig. 1.2a. Pluggable optics connect the switch chip (electronic components) to external optical engines (photonic components), while on-board optics place photonic elements within the switch package. Co-packaged optics integrate the switch chip and optical engines into a common package, thereby improving

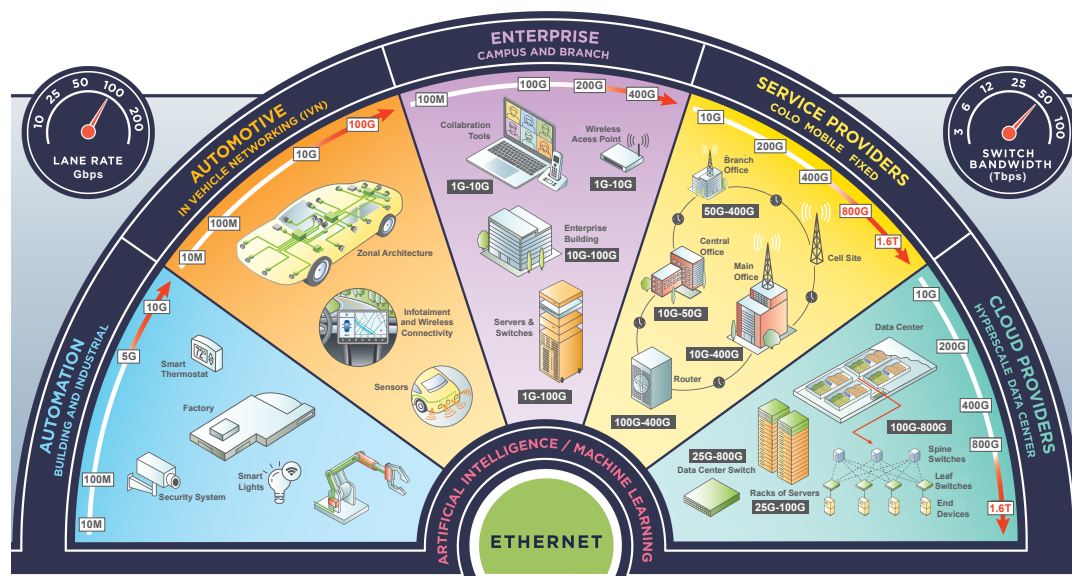


FIGURE 1.1: Ethernet roadmap [1].

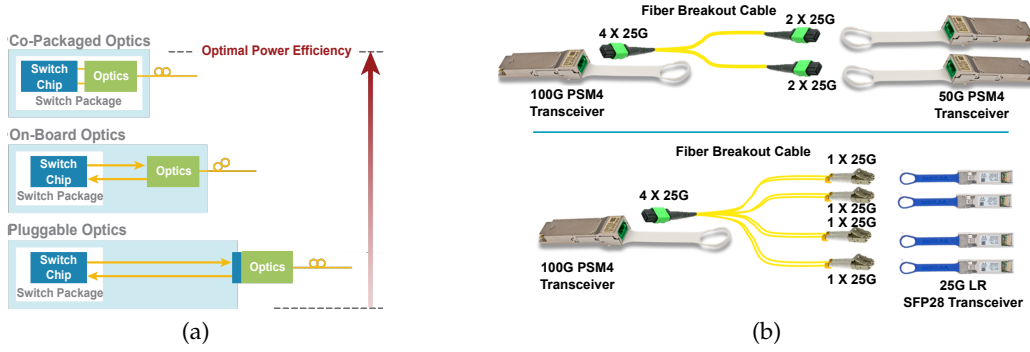


FIGURE 1.2: (a) Optical evolution [1] (b) 100G PSM4 transceiver [4].

power efficiency, reducing size and cost. Advances in Electronic-Photonic Integrated Circuits (EPIC) technology have enabled the integration of electronic and photonic components on a silicon platform, reducing interconnect parasitics, packaging complexity, and interface losses while improving bandwidth and power efficiency.

Data transmission links over optical media can be broadly categorized as either Intensity Modulation with Direct Detection (IMDD) or coherent systems. For short-reach links, IMDD transceivers are traditionally been favored due to their low cost and simplicity, while coherent systems are predominantly used for long-reach applications [3]. The 100G Parallel Single-Mode four-channel (PSM4) transceiver is an IMDD device designed to increase data throughput in modern data center networks, as shown in Fig. 1.2b [4]. By enabling parallel transmission over multiple fibers, it supports 100 Gigabit Ethernet applications. The PSM4 transceiver uses eight fibers—four for transmitting and four for receiving—allowing 100 Gbps point-to-point links over distances up to 2 km. This configuration also supports breakout options, such as dual 50 Gbps or quad 25 Gbps connections, offering flexibility for linking servers, storage, and other systems.

1.1 IMDD vs Coherent transceiver

In the exemplary IMDD transceiver shown in Fig. 1.3a, digital data to be transmitted is first converted to an analog format (either Non-Return-to-Zero (NRZ) or Pulse-Amplitude-Modulation (PAM)) using the Transmitter (TX) Digital Signal Processor (DSP). A serializer is then used to aggregate multiple parallel data streams into a single high-speed stream, allowing the transceiver to leverage the greater bandwidth of the optical fiber. This data is often retimed to reduce jitter before being sent to the laser driver or modulator driver. The laser or optical modulator then encodes the analog data from the driver onto the light, producing an optical data signal. This signal is transmitted over the optical fiber to the receiver. At the other end of the optical fiber, the optical signal is detected by a photodiode, which converts it into an electrical current. This current is then transformed into a voltage and amplified by the Transimpedance Amplifier (TIA) before being passed to the Clock and Data Recovery (CDR). The CDR recovers the clock, retimes the data, and suppress most of the jitter accumulated during transmission. The recovered clock and data are then used to deserialize and convert the signal back to digital data in the Receiver (RX) DSP. Since the primary bottleneck in this transmission is within the electronic components, parallel channels are used to increase the overall throughput.

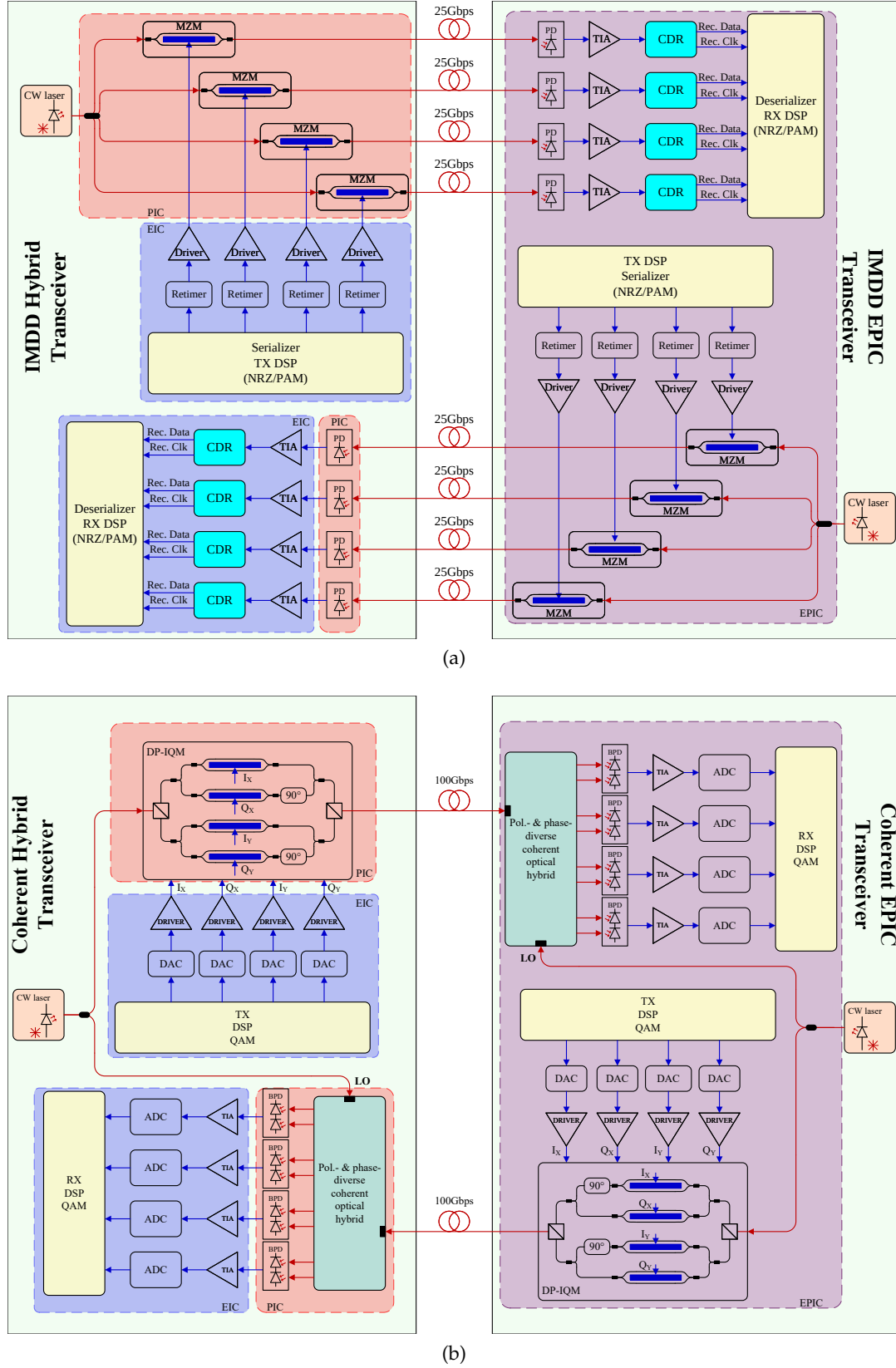


FIGURE 1.3: Exemplary optical transceiver implementations:
 (a) Intensity Modulation with Direct Detection (IMDD)
 (b) Coherent modulation and detection.

Similarly, the coherent transceiver shown in Fig. 1.3b uses Quadrature Amplitude Modulation (QAM) signaling to achieve comparable throughput [5]. In the transmitter, the TX DSP decomposes the data into quadrature components (I_x , I_y , Q_x & Q_y), which are then converted to analog signals using Digital-to-Analog Converters (DACs). These analog signals are subsequently combined and modulated onto the optical carrier by a Double Polarization - IQ Modulator (DP-IQM). The resulting optical data is transmitted over a single optical fiber. On the receiver side, a polarization- and phase-diverse coherent optical hybrid is used to demultiplex the received signal into its quadrature components. Balanced Photodiode (BPD) and TIA then convert the optical signals into electrical form, which are subsequently digitized by Analog-to-Digital Converters (ADCs). The resulting digital data is processed by the RX DSP. The use of a shared laser source for both the DP-IQM and polarization- and phase-diverse coherent optical hybrid adds significant complexity, with coherent systems generally requiring more sophisticated components, higher power consumption, and advanced DSP compared to simpler IMDD solutions [5].

Both systems can be implemented as either hybrid or EPIC transceivers, as discussed in [6]. In the hybrid approach (shown on the left in Figs. 1.3a–1.3b), the components are fabricated separately using the most suitable Electronic Integrated Circuits (EIC) and Photonic Integrated Circuit (PIC) technologies. Additional measures, such as interface matching or buffers, are needed to ensure integration and operation. In contrast, EPIC technology (shown on the right in Figs. 1.3a–1.3b) enables co-integration of electronic and photonic components on a single chip, thereby eliminating the need for external interface. Silicon photonics EPIC technologies have been demonstrated on both SiGe BiCMOS [7] and CMOS [8] platforms. Preez et al. [9] provide a comparative analysis of these platforms, with particular attention to critical transceiver circuit blocks. Clock recovery and data retiming are essential functions within the receiver. In IMDD system, these tasks are handled by dedicated CDR circuits, while in coherent systems, they are performed by the DSP. This thesis focuses on the design of high-speed CDRs for IMDD transceiver applications.

1.2 Types of CDRs

When an asynchronous data signal arrives at the receiver front-end without an accompanying clock (i.e., as a stream of random data bits), it may have experienced dispersion and accumulated jitter during transmission, degrading signal quality. Additional jitter and signal degradation can also be introduced during photo detection and amplification by the TIA. To reconstruct the original data, the clock information must be recovered from the received signal. The fundamental principle of CDR is illustrated in Fig. 1.4. The signal from the TIA, referred to as the input data to the CDR, drives a clock recovery circuit that generates a periodic clock signal,

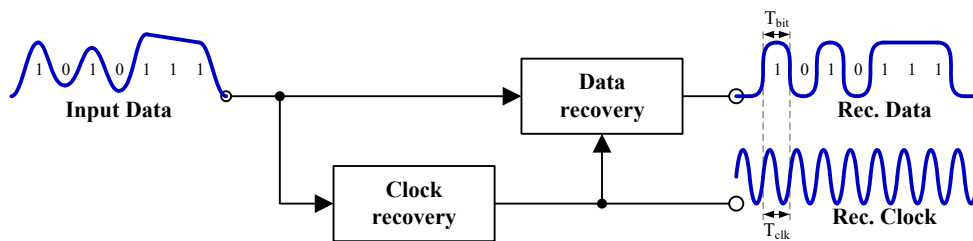


FIGURE 1.4: Basic CDR circuit principle.

known as the recovered clock. The data recovery circuit uses this clock to retiming the input data, now referred to as the recovered data. If the data recovery circuit is implemented as a simple D flip-flop, the recovered clock must have a frequency equal to the input data rate, that is, the clock period (T_{clk}) must match the bit period (T_{bit}) to ensure accurate retiming without data loss. Additionally, the sampling edge (or phase) of the recovered clock should be aligned with the center of each input data bit, maximizing the distance from data transitions that are most affected by jitter. This alignment ensures that the recovered data is minimally impacted by input jitter, effectively suppressing it.

Integrated CDR design for any transceiver involves systematic steps, as depicted in Fig. 1.5. First, the system requirement of the transceiver must be considered, including the system's data rate, data modulation format, jitter specifications as per the respective standard, power dissipation, the area required for the transceiver to fit within the form factor, and the technology that can be used to implement the transceiver. Once these requirements are defined, the topology of the CDR circuit can be selected. The topology can be classified based on the clock recovery techniques, and the architecture employed to retiming the data for further processing. After the topology is finalized, a behavioral model can be developed to verify whether the system requirements defined by the standards can be met.

With the behavioral model and the corresponding technology that aligns with the speed and power requirements, the CDR chip design can proceed to the schematic design phase. Following this, the designers need to create a layout, which will be used by the foundry for fabrication. The geometric structures introduced during the layout phase create parasitics, which are unintended resistive, capacitive, and inductive effects arising from the physical interconnects that reduce the circuit's performance compared to the schematic design. Designers must iterate between the schematic and layout designs to minimize the impact of parasitics, though complete elimination is not possible. Once the performance of the layout and schematic are close to the desired target, the chip can be sent for fabrication. After fabrication, the chip is mounted on a suitable package or printed circuit board for testing. With the test setup, the chip is characterized and compared to the simulation results to ensure the system requirements are met.

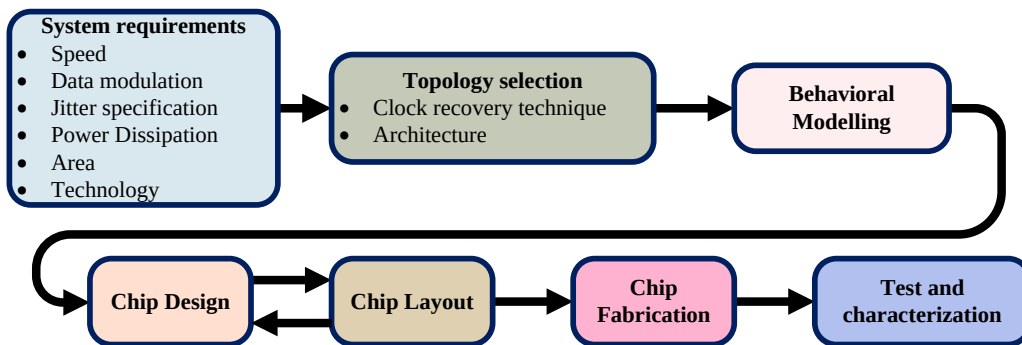


FIGURE 1.5: Integrated circuit design methodology.

1.2.1 Modulation formats for IMDD systems

For high-speed digital data transmission, the most common formats are NRZ and PAM4. To characterize CDR performance, a user may employ test patterns such as a Pseudorandom Binary Sequence (PRBS) with $N = 2^k - 1$, selected according to system

requirements. This pattern is distinguished by a periodic sequence with up to N bits and a maximum identical consecutive bits of length k , which is also referred to as the run length. For example, encoding PRBS $2^4 - 1$ data with ONES and ZEROS mapped to voltage levels "+1" and "-1" respectively yields a time-domain waveform as shown in Fig. 1.6a. For NRZ, the signal level remains constant for entire bit period T_{bit} (either +1 or -1). In contrast, each symbol in PAM4 encodes two bits over the symbol period T_{baud} using one of four discrete levels (+1, +1/3, -1/3, -1). The dashed lines illustrate the ideal signal behavior, while the solid lines show actual data, which may exhibit jitter, signal degradation, and bandwidth limitations. Superimposing multiple bit or symbol periods forms an eye diagram, which provides valuable insights into signal quality, as shown in Fig. 1.6b. The modulo of each bit or symbol period, known as a Unit Interval (UI), enables the measurement of key parameters such as jitter, Inter Symbol Interference (ISI), rise/fall times, and noise.

Examining the frequency-domain behavior of these signals, as shown in Fig. 1.6c, the power spectral density reveals that most signal energy is concentrated below $1/f_{bit}$

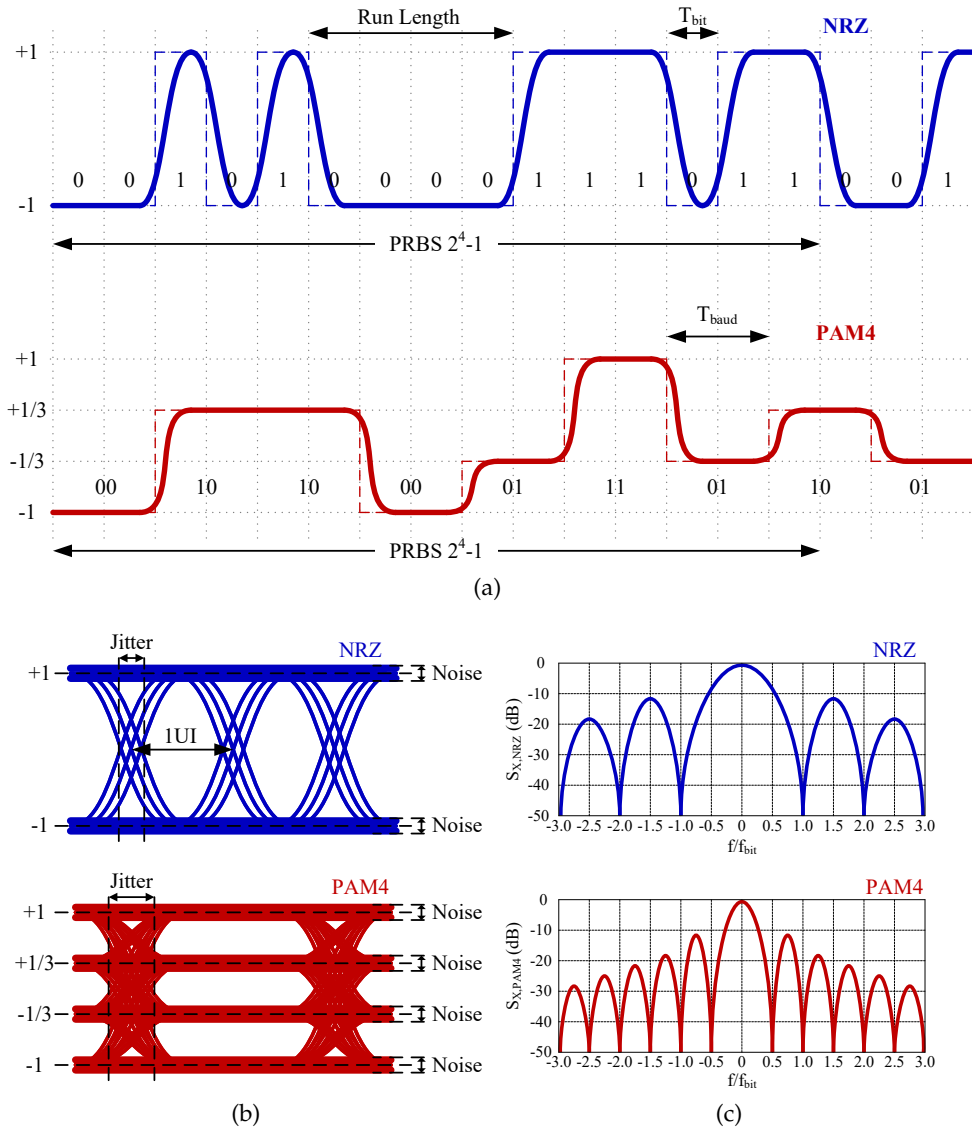


FIGURE 1.6: (a) NRZ(PAM2) and PAM4 coding, (b) eye diagrams of both formats with noise, and (c) corresponding power spectral densities.

for NRZ and below $0.5/f_{bit}$ for PAM4, with no significant components at integer multiples of the bit rate. For a data rate of 25 Gbps, the required receiver electrical bandwidth is approximately $0.75 f_{bit}$ for NRZ, while for 12.5 GBaud PAM4—providing the same throughput—the bandwidth is reduced to about $0.375 f_{bit}$ [10]. Although NRZ systems require higher bandwidth than PAM4 systems, NRZ signal generation and processing are much simpler. In contrast, PAM4 circuits must maintain high linearity to accurately process multi-level signals with reduced amplitude (down to one-third that of NRZ), making them more susceptible to noise and resulting in an Signal-to-Noise Ratio (SNR) penalty of approximately -9.5 dB ($\text{SNR}_{\text{loss}} = 20 \log_{10}(1/3)$) [11]. Furthermore, recent work by Forghani et al. [12] suggests that, to avoid additional ISI in PAM4 systems, the required bandwidth must be increased considerably to maintain signal quality. In addition, phase detection accuracy in PAM4 systems is reduced due to the presence of asymmetric intermediate transitions, which can worsen jitter in the recovered clock [13]. Filtering out these asymmetric transitions helps to reduce jitter, but this approach also lowers the tracking bandwidth and increases overall power consumption due to the additional transition detection circuitry.

1.2.2 Classification of CDR architectures

Clock recovery techniques for asynchronous data signals can be broadly classified, as shown in Fig. 1.7. One of the earlier approaches utilized a Surface Acoustic Wave (SAW) filter, as described in [14]. In this method, data and its complement are combined via a rectifier to generate pulses at each data transitions. These pulses are then amplified and passed through a high-Q SAW filter to produce a low-amplitude sine wave. Further amplification and squaring yield the recovered clock. However, delivering this clock to a separate data retiming path required an additional phase alignment circuit to ensure optimal sampling at the eye center, a challenging task due to variations in Process, Voltage, and Temperature (PVT) in integrated circuits. Moreover, SAW filters had limited or fixed frequency ranges because of their resonance properties and were sensitive to temperature and performance drift over time. Eventually, Phase-Locked Loop (PLL) replaced filter-based CDRs in modern technologies. However using PLLs for separate clock recovery and data regeneration paths (see Fig. 1.4) introduced the drawback of non-optimal sampling. As the phase difference between the recovered clock and data could be large due to systematic skew, making robust data sampling under PVT variations challenging [15].

To address the skew problem, integrated phase detection and data regeneration within a single circuit were developed. PLL-based CDR without reference

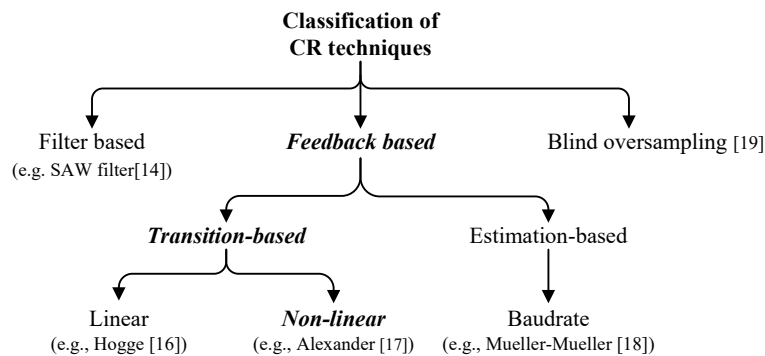


FIGURE 1.7: Classification of clock recovery techniques.

clock, also referred as feedback techniques, can be classified into transition-based or estimation-based methods, depending on the type of phase detector (PD) used. In transition-based PDs, linear or non-linear phase detection techniques are employed. For instance, linear PDs such as the Hogge PD [16], produce pulses with widths proportional to the phase difference between the recovered clock and the data transitions. However, as data transmission speed increases, timing skew and the narrow pulses produced by these detectors became limiting factors. Non-linear PDs, such as the Alexander PD [17], offer alternatives for overcoming these challenges. These detectors provide binary phase information when the data transitions occur, making the phase detector gain larger than that of linear PD, i.e., indicating whether the recovered clock phase is leading or lagging the data sampling point. In contrast to transition-based methods, in estimation-based PDs, as the modulation of the data changes to PAM, sampling the data at the center of the data bits leads to higher bit error rates. As multilevel PAM signals have many transitions and the highest data eye opening is no longer at the center of the data bit, estimation-based PD such as the Baud rate PD [18] are used. In this PD, the data signal is sampled and estimated at a particular signal level, reducing the minimum variance and allowing the data bits to be sampled at the point of the highest eye opening of the signal. Along with these, blind oversampling [19] clock recovery technique such as phase picking [20] is used. Here, multiple spaced clock phases are generated, and the sampling phase that most closely aligns with the center of the data eye is used to retime the incoming data.

Hogge PD and Alexander PD can inherently retime the data, avoiding the need for a separate data recovery circuit. Using these transition-based clock recovery techniques, CDR architectures can be further classified, as shown in Fig. 1.8. Both NRZ and PAM modulation schemes can be categorized based on the clock frequency used for phase detection relative to data rate. These categories include full-rate, half-rate, quarter-rate and octa-rate designs, corresponding to clock frequency equal to, one-half, one-quarter, or one-eighth of the data rate, respectively.

To better illustrate the operation of different CDR architectures, Fig. 1.9a presents a basic CDR circuit employing a full-rate NRZ PD. In this configuration, the PD detects the phase difference between the input data and the recovered clock when the bit period equals the clock period ($T_{bit} = T_{clk}$). This phase information-indicating whether the clock is early or late relative to the data sampling point- is passed to the Charge Pump (CP). The Loop Filter (LF) converts the current I_{cp} from CP into a control voltage V_c to adjust the Voltage Controlled Oscillator (VCO) frequency accordingly. As observed in the NRZ data spectrum (cf. Fig. 1.6c), there is no clock related component at integer multiples of f_{bit} where $f_{bit} = 1/T_{bit}$. Therefore, clock recovery based on data transitions (nonlinear process) requires an inverted clock with a 180° phase shift. This setup ensures that one clock samples the data at the center

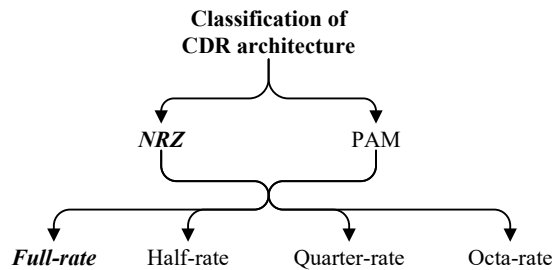


FIGURE 1.8: Classification of CDR architectures for transition-based clock recovery.

of the bit period while another samples at the data transitions. Consequently, the recovered data pattern closely resembles the input data pattern. For simplicity, only one recovered clock is shown in the figure.

In the half-rate NRZ PD shown in Fig. 1.9b, phase detection uses two clock phases (0° and 90°) at half the input data rate, with inverted clocks for transition detection. The recovered data is also half the input data rate and is asynchronously

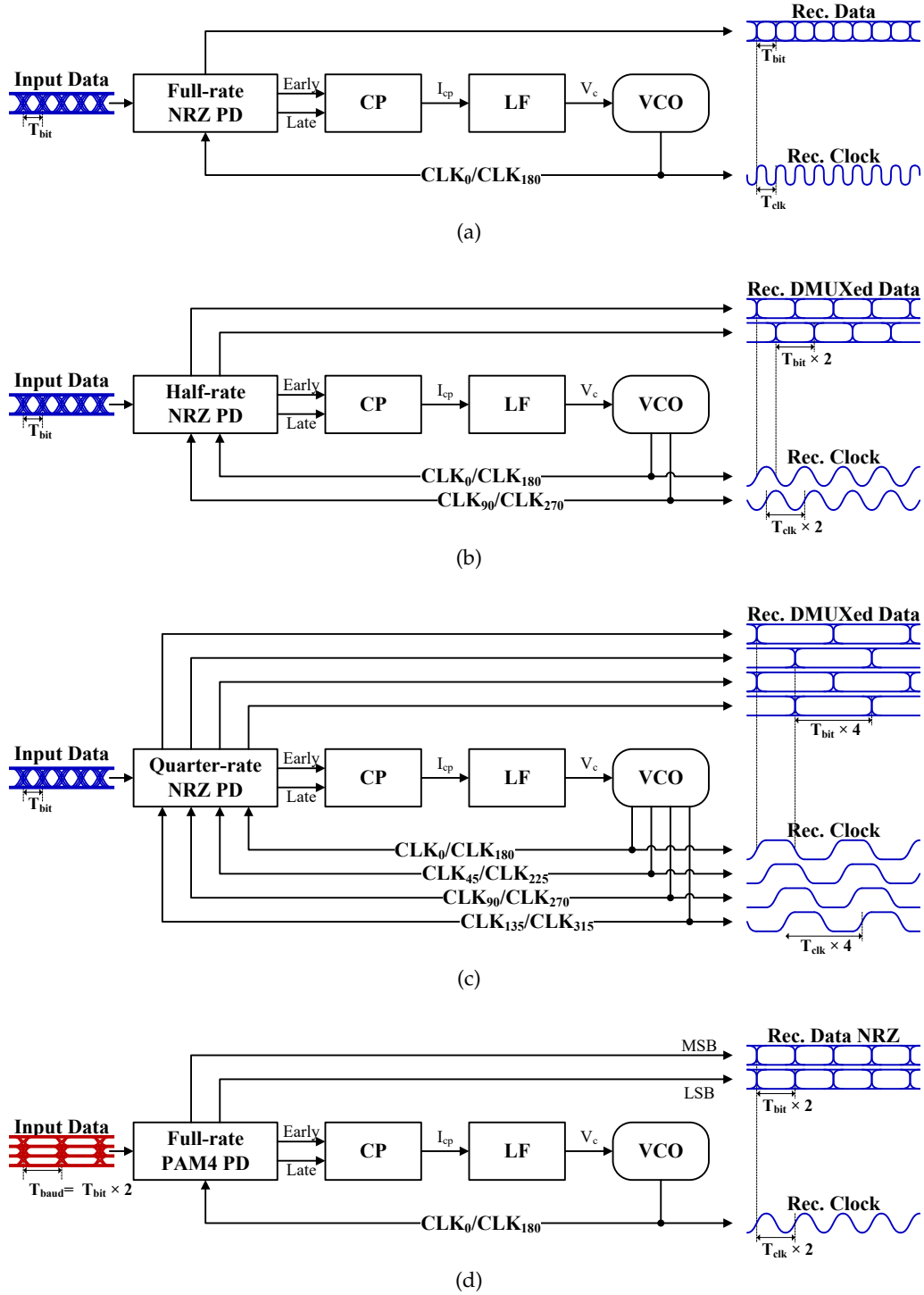


FIGURE 1.9: CDR using PLL for transition-based CR: (a) NRZ full-rate, (b) NRZ half-rate, (c) NRZ quarter-rate, and (d) PAM4 full-rate PD.

demultiplexed into two parallel streams, requiring additional circuitry to multiplex it back to full-rate, thereby increasing system complexity.

Similarly, the quarter-rate NRZ PD shown in Fig. 1.9c uses four clock phases (0° , 45° , 90° , and 135°), each running at one-fourth the input data rate. The recovered data is also at one-fourth the input data rate and is asynchronously demultiplexed into four parallel streams. Further multiplexing is required to reconstruct the full-rate data pattern, increasing design complexity.

When examining a full-rate PAM4 PD shown in Fig. 1.9d, and considering the same input data rate as NRZ ($T_{bit} = T_{baud}/2$), the required recovered clock frequency is half that of the NRZ case (i.e., clock period is $2 \times T_{clk}$). Unlike in half-rate or quarter-rate NRZ scenarios, the recovered data in this architecture is demultiplexed synchronously at the PD into NRZ data streams. This operation makes it easier to reconstruct the original data and enables more efficient system implementation.

1.3 Scope of the thesis

This thesis presents the design of high-speed full-rate NRZ Bang-Bang Clock and Data Recovery (BBCDR) circuits for IMDD transceivers. The Alexander PD is utilized for its inherent ability to perform data retiming of random data. The dissertation is organized as follows:

- Chapter 2: Develops the theoretical framework and behavioral modeling of Bang-Bang PLL. The model features an adaptable LF transfer function with independently tunable proportional and integral parameters. The chapter focuses on phase and frequency acquisition, as well as jitter characterization. It also demonstrates that stringent jitter requirements inherently limit the acquisition range of the BBCDR.
- Chapter 3: Reviews state-of-the-art frequency acquisition techniques. We introduce novel acquisition techniques employing either a permanently modulated offset voltage (applied externally to the VCO) or a permanently modulated offset current (applied within the integral branch of the PLLs). The chapter details the underlying theory, operational constraints, and limitations of these approaches.
- Chapter 4: Demonstrate the implementation of the proposed novel acquisition techniques in BBCDR circuits using two Innovations for High Performance Microelectronics (IHP) SiGe BiCMOS technology nodes. The 250 nm SiGe BiCMOS design targets IMDD EPIC transceiver applications, while the 130 nm technology addresses IMDD hybrid transceivers.
- Chapter 5: Explores the implementation of BBCDR circuits in GlobalFoundries (GF) 22 nm FD-SOI CMOS technology, focusing on IMDD hybrid transceiver. This design leverages backgate biasing to reduce the power consumption and improve sustainability.
- Chapter 6: Presents the measurement and characterization results for the fabricated BBCDR circuits described in Chapters 4 and 5.

The proposed acquisition techniques require minimal additional hardware and power, while meeting stringent system requirements. Key results have been published in IEEE conferences [21–24], and the technique has been granted a patent [25].

Chapter 2

Analysis and Design

An IMDD optical communication system, as illustrated in Fig. 2.1, consists of a Transmitter (TX), an optical fiber, and a Receiver (RX). Low-speed parallel input data generated by multiple users is provided to the TX. The serializer, such as a multiplexer, converts the low-speed parallel data to high-speed serial data. The serializer requires several clock signals with different frequencies and precise edge alignment generated by the PLL and state machine. The serializer output is affected by jitter and intersymbol interference, requiring a retimer to resample the signal using the transmitter clock (TX Clk) before reaching the laser driver. The driver then converts this data into large currents supplied to the laser. The laser transforms the electrical data signal into an optical data signal, i.e., it emits light for logical ONES and remains off for logical ZEROS. The light produced by the laser is transmitted to the receiver through the optical fiber.

In the RX, a photodiode such as a photodiode detects the light and converts it back into an electrical data signal (i.e., current). The TIA then amplifies the received data signal, converting it into a voltage with low noise and sufficient bandwidth. The clock recovery circuit re-synchronizes the recovered clock (Rec. Clk) to the transmitter clock (TX Clk) by extracting timing information from the received data transitions. The data recovery circuit then re-times the received data using the recovered clock. This combined operation is referred to as Clock and Data Recovery (CDR). Next, the deserializer, such as a demultiplexer, converts the high-speed re-timed data into low-speed parallel data using multiple clock signals with different frequencies and precisely aligned edges, generated by the state machine.

In the reference-less CDR, the circuit has functionalities beyond clock generation and data retiming, as illustrated in Fig. 2.2. The clock recovery circuit must generate

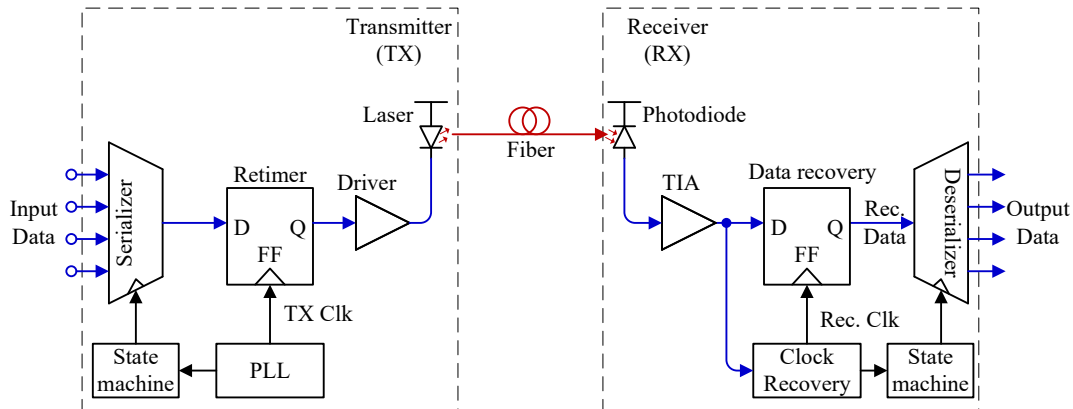


FIGURE 2.1: Simplified block diagram of an optical communication system using IMDD.

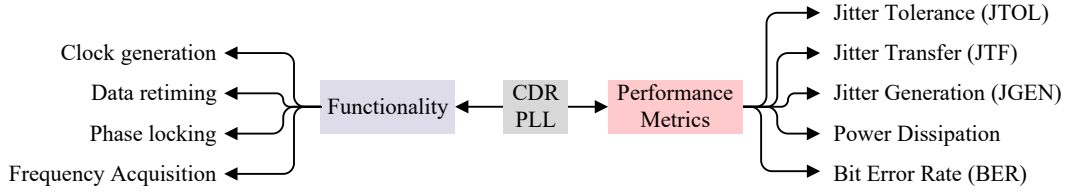


FIGURE 2.2: Reference-less CDR functionality and metrics.

a clock signal (Rec. Clk) with frequency, that instantly locks onto the input data rate or integer divisor of the data rate, a process known as frequency acquisition. There exists a phase offset between the input data signal and the internal clock which must be also locked so that the data recovery circuit samples the data precisely at the desired sampling point. Any phase drift due to jitter can lead to bit errors in the recovered data.

The entire communication system introduces various forms of distortion, including jitter in the data signal. At the input of the TX, data signal distortion occurs through the AC coupling, leading to amplitude drooping (AC coupling droop) or average voltage level drooping (baseline wander) when transmitting a long sequence of identical bits. Even after re-timing the serialized data to mitigate jitter at the cost of reducing speed due to the retimer [26], the TX Clk generated by the PLL still propagates clock jitter to the data edges. Additionally, distortions due to (1) random noise from the power supply or substrate, (2) electrical or optical crosstalk, (3) optical pulse dispersion, and (4) misalignment of fiber coupling to laser lead to signal distortion and increased Bit Error Rates (BERs). On the RX side, factors such as misalignment between the fiber and the photodiode, bandwidth limitation of the photodiode, and the input-referred noise contribution of the TIA further degrade to signal quality. Furthermore, random noise from the power supply or substrate in the receiver also contributes to the data signal distortion.

In summary, the data signal accumulates jitter, both Random Jitter (RJ) and Deterministic Jitter (DJ), before reaching the CDR circuit. Appendix A discusses the jitter terminology used in optical communication system. The CDR in lock or steady-state must tolerate (JTOL) the accumulated jitter while maintaining the specified BER as defined by the standards. Standards also specify the system's jitter transfer (JTF) characteristics, where low-frequency jitter can be transferred without amplification or attenuation, while high frequency jitter components are suppressed. Jitter peaking in the data is tolerated to a certain limit to prevent propagation or amplification when we use repeaters (same communication systems in series) for transmitting data over longer distances. The CDR circuit itself should generate (JGEN) only a low amount of jitter, as the recovered clock is used to deserialize the data. Power dissipation is also crucial to reduce the overall energy consumption of the transceiver.

2.1 Transition-based phase detectors

In high-speed CDRs, PDs are the most important blocks. Therefore, we begin our discussion with the different PDs used in transition-based CDR circuits for random data transitions, which simultaneously retime the data and detect the phase difference between the recovered clock and the input data. Additionally, in the absence of data transitions, the VCO control remains undisturbed, helping to suppress data-dependent jitter.

2.1.1 Linear PD

The Hogge PD [16] topology is most commonly used in self-correcting linear CDR circuit for extracting the clock from a NRZ random data signal. Fig. 2.3a shows the block diagram of a full-rate NRZ Hogge PD. The input data (D_{in}) is retimed to D_1 using the D flip-flop FF_1 , with a positive edge-triggered clock (Clk_0). The data D_1 is further retimed to D_2 using FF_2 , which is triggered by a negative edge clock (or inverted clock). The output of exclusive OR (X_1) of input data D_{in} and the retimed data D_1 generates the DN signal, which provides the pulses proportional to the phase error between input data transitions and rising edge of the clock (Clk_0). In contrast, the output of X_2 (UP signal) generated from D_1 and D_2 produces reference pulses with a width equal to half of the clock period ($t_{clk}/2$). It is assumed that all signal levels toggle between "0" and "1".

Fig. 2.3c illustrates the case when the falling edge of the clock is early relative to the middle of each data bit ($-\Delta\phi$). The XOR outputs are visible only when there is a data transition; when no data transition occurs, the PD output, $UP - DN$ remains zero. If we examine the average $UP - DN$ output (PD_{out}) during data transitions, it yields a negative value, corresponding to the phase difference. Fig. 2.3d illustrates the case when the falling edge of the clock is late relative to the middle of each data bit ($+\Delta\phi$). In this case, the PD_{out} is positive. As the phase difference changes, the widths of the proportional pulse change accordingly, which in turn alters the value

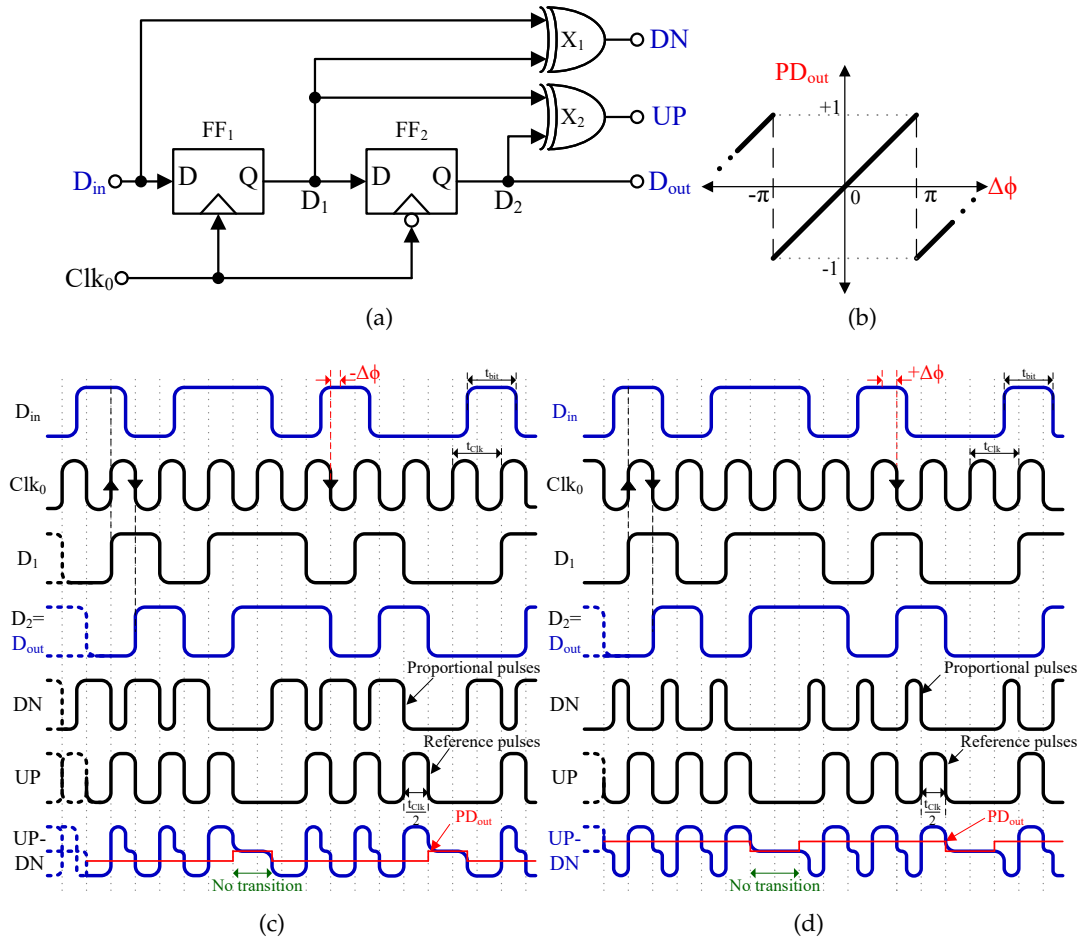


FIGURE 2.3: Hogge: (a) full-rate PD, (b) characteristics, (c) early clock, and (d) late clock.

of PD_{out} . This characteristic can be plotted as shown in Fig. 2.3b. In steady state, when the falling edge of the clock is at the middle of each data bit, the average value of UP equals the average value of DN , with each pulse time lasting for half clock period ($t_{Clk}/2$). However, the pulses are also separated by half clock period. The retimed output can be taken either from D_1 or its delayed version, D_2 . As the retimed data from FF_1 is applied to FF_2 , XOR_1 and XOR_2 , the fanout of FF_1 can be reduced by using the retimed data from FF_2 , i.e., the $D_{out} = D_2$ signal. The UP and DN signals are applied to the CP or a voltage to current converter.

As the data rate increases to tens of gigabits in modern technologies, the rise time, fall time, timing skews, and speed of flip-flops become limiting factors, which in turn makes the UP and DN signals narrower [15]. This results in insufficient signal widths to properly switch the CP, reducing the gain of the PD, and potentially causing it to vanish altogether. Additionally, the clock-to-Q delays from the flip-flops introduces offset in the data sampling point from the middle of data bit in the steady state [15]. Compensating for this offset by adding delay elements or offset currents in the CP can help mitigate the issue to some extent.

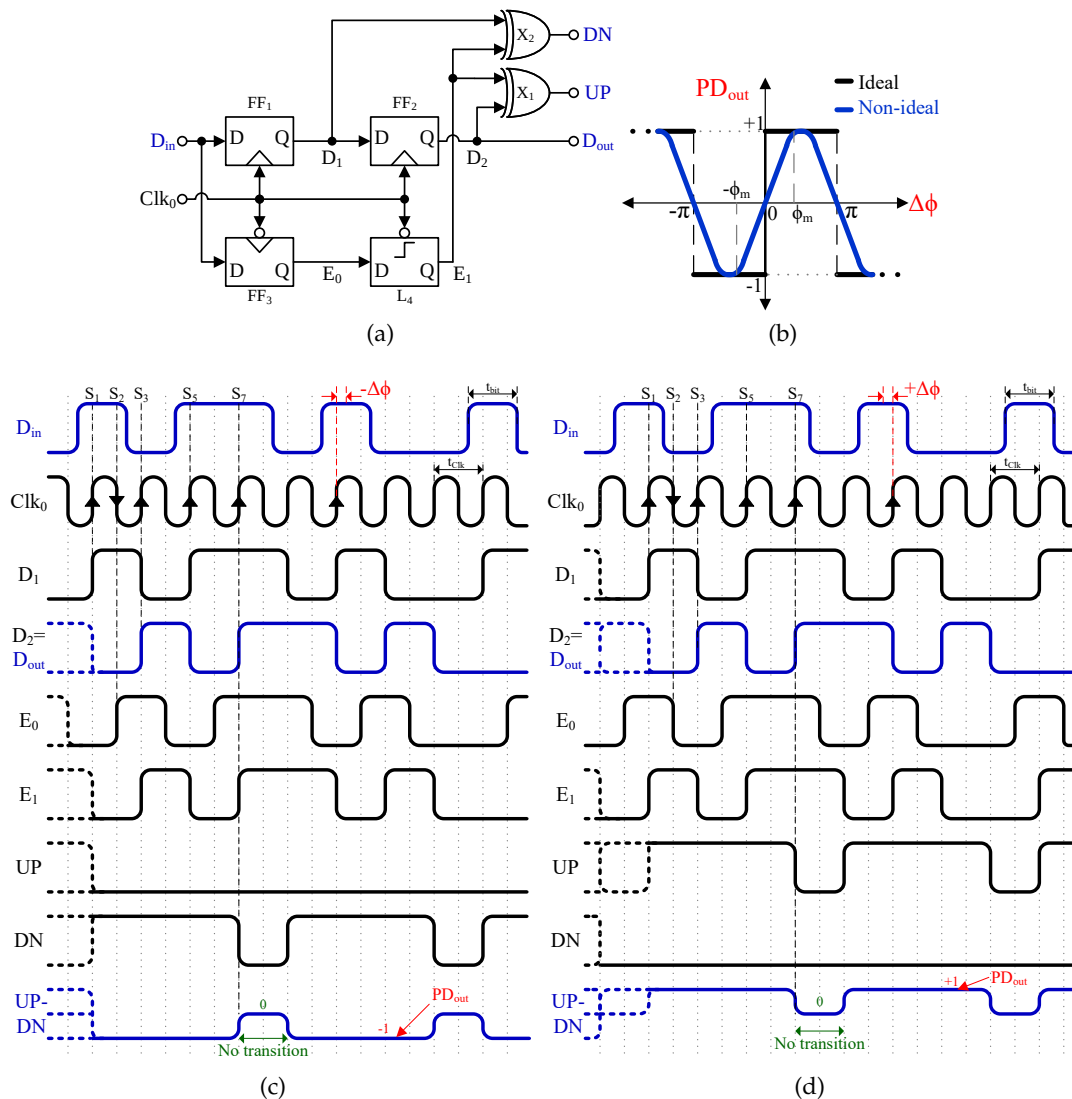
2.1.2 Nonlinear PD

Bang-Bang Phase Detectors (BBPDs) reduce the need for high speed and precision in flip-flops and other circuits within the CDR, thereby decreasing both complexity and power consumption [27]. As the name suggests, a BBPD ideally produces binary output signals for the phase difference. The Alexander PD [17] is a popular topology used for tristate realizations, i.e., it produces early, late, or no output in the absence of data transitions. Similar to the Hogge PD, the Alexander PD also requires the simple processing of the NRZ data using the D flip-flops.

Fig. 2.4a shows the block diagram of the modified full-rate Alexander PD [15]. The input data (D_{in}) is processed using D flip-flops FF_1 and FF_2 , with a positive edge clock Clk_0 to produce the retimed current bit D_1 and the retimed preceding bit D_2 , respectively. The input data transitions are sampled with the negative edge of the same clock Clk_0 to produce E_0 . The E_0 signal is delayed by an extra half bit period using latch L_4 to produce E_1 , allowing it to be compared for a full bit time with the bits D_1 and D_2 . The signals D_1 and E_1 are XORed using X_2 to produce the DN signal, whereas the signals D_2 and E_1 are XORed using X_1 to produce the UP signal. Therefore, incoming data bits are sampled and the decisions are made at every positive edge of the Clk_0 . It is assumed that all signal levels toggle between "0" and "1".

Fig. 2.4c illustrates the case when the rising edge of the clock is early relative to the middle of each data bit ($-\Delta\phi$). The phase difference information ($UP - DN$) is only visible when there is a data transition, resulting in a PD_{out} value of "-1". When there is no data transition, the value is equal to zero. Similarly, Fig. 2.4d illustrates the case when the rising edge of the clock is late relative to the middle of each data bit ($+\Delta\phi$). The PD_{out} value in this scenario is equal to "+1", during data transitions. If the phase difference between the rising edge of the clock and the middle of input data changes, either in the early or late case, the average value remains the same during data transitions, i.e., "-1" or "+1", respectively. Also, the widths of the UP and DN signals are independent of the phase difference. This results in nonlinear behavior, complicating the loop analysis and design. However, the PD gain is much higher compared to the Hogge PD gain, eliminating the need for amplifying very short pulses. This ideal characteristics can be plotted as shown in Fig. 2.4b. In steady state, the UP and DN signals are as wide as a full clock period.

A conventional reference-less full-rate CDR circuit using a transition-based PD with CP, LF and VCO, is shown in the Fig. 2.5a. Comparing the Hogge PD and the



Alexander PD in this implementation under continuous data transitions in a steady state or locked condition provides useful insights. Using the Hogge PD as shown in Fig. 2.5b, each transition generates both *UP* and *DN* pulses of equal width, separated by half the clock period $t_{clk}/2$. This behavior produces a corresponding CP current, which introduces ripple on the control voltage, V_c . When correctly aligned, the net charge deposited on the capacitor is zero, or the ripple effect can be mitigated by employing a higher-order LF.

In contrast, as shown in Fig. 2.5c, the Alexander PD produces either *UP* or *DN* signals for the entire clock period, t_{clk} . Regardless of how well-aligned the signals are, the PD deposits charge on the capacitor. As a result, the VCO control voltage alternates exclusively between $\pm V_{bb}$, with no intermediate values. In the absence of transitions, the control voltage remains undisturbed. However, the data is not sampled at a single fixed point but alternates between two points. This phenomenon, known as bang-bang jitter, requires careful consideration to ensure the alternating sampling positions are sufficiently narrow and within acceptable limits.

The architectures of the Alexander half-rate NRZ and full-rate PAM4 PDs are described in [29] and [30], respectively. Transitioning from a full-rate NRZ design to half-rate operation requires more flip-flops, XOR gates, and the generation of additional clock phases, which increases power dissipation and circuit complexity. Similarly, full-rate PAM4 PD require even more logic gates, including comparators and transition detector, to handle multi-level signals and to filter out jitter-inducing asymmetric transitions. Despite these challenges, the Alexander architecture remains highly adaptable for high-speed CDR circuits. The implementation details, circuit trade-offs, and power implications of these topologies are discussed in Appendix B.

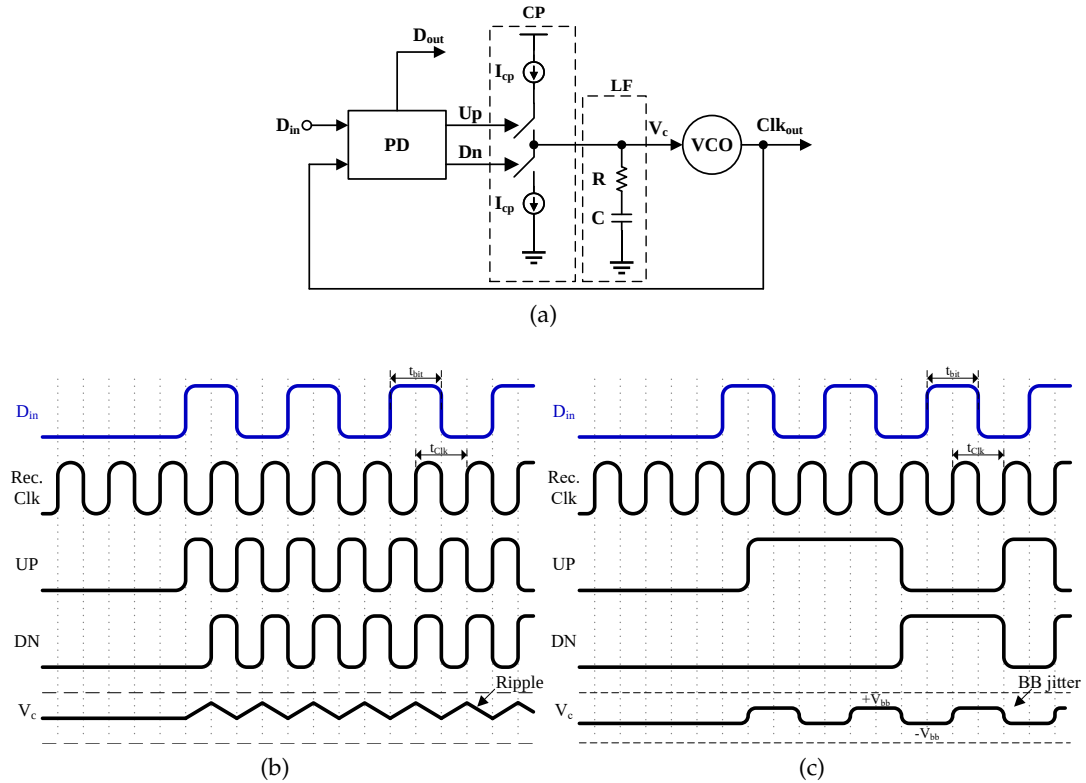


FIGURE 2.5: (a) Conventional reference-less full-rate CDR circuit (b) waveform with CDR locked using Hogge PD, and (c) waveform with CDR locked using Alexander PD.

2.2 Modeling of Bang-Bang PLL

Building on the Alexander PD, this section examines the operation and modeling of bang-bang PLL-based CDR circuits, commonly referred to as "Bang-Bang Clock and Data Recovery" (BBCDR). The inherent nonlinearity of the BBPD complicates analysis, making traditional linear PLL models insufficient. As a result, specialized nonlinear system modeling approaches have been developed to accurately describe the loop dynamics and performance limits of BBCDRs [15, 28, 31–35].

Conventional BBCDRs (cf. Fig. 2.5a) using a second-order PLL typically exhibit a tunable CP and a series RC LF. This can be modeled with two non-interacting loops: the proportional branch and the integral branch [15]. The proportional branch controls the jitter generation and jitter tolerance, whereas the integral branch extends the frequency acquisition range. In the conventional approach, the R and C are fixed, and tuning the CP current (I_{cp}) changes both the proportional and integral parameters simultaneously, thereby controlling the VCO. Ideally, the parameters of both branches should be independently tunable to optimize the dynamic behavior of the BBCDR. In addition to the main control input from the CDR loop, the VCO architecture typically includes auxiliary controls that use analog tuning via varactors for fine frequency adjustment and digital tuning via switched capacitor banks for coarse frequency band selection, allowing full utilization of the VCOs tuning range.

Utilizing a VCO design with separate varactor controls for proportional and integral branches, Fig. 2.6a shows the proposed architecture of a BBCDR with an adaptive dual-LF to optimize the CDR parameters independently, in a way that is similar to the frequency synthesizer PLL from [36, 37]. The proportional and integral branches are composed of separate tunable CP currents, $I_{cp,prop}$ and $I_{cp,int}$, fed into a resistor R_{prop} and a capacitor C_{int} , respectively.

2.2.1 Nonlinear time-domain modeling

To initiate the analysis, a simplified nonlinear phase-domain model of the PLL, based on [15] and illustrated in Fig. 2.6b, provides an efficient starting point for tuning the loop dynamics. This model primarily analyzes the transient response of the output to phase or frequency deviations at the input.

Consider a scenario with 100% probability of data transitions in full-rate BBCDR, where the data alternates between 0 and 1. In this case, the phase can be determined at every sampling instant; that is, each VCOs clock period ($t_{clk} = 1/f_{nom}$) is approximately equal to one bit period (t_{bit}). This data can be assumed to be generated by a pattern generator clocked on the rising edges of the signal, $\sin[2\pi f_{bit} t + \phi_j(t)]$, with jitter $\phi_j(t)$ which has a zero mean. If the frequency deviation between the incoming data (f_{bit}) and the nominal center frequency (f_{nom}) is denoted by δf , then:

$$f_{bit} = f_{nom} + \delta f \quad (2.1)$$

Accordingly, the data phase can be expressed as:

$$\phi_d(t) = 2\pi (f_{nom} + \delta f) t + \phi_j(t) \quad (2.2)$$

The VCO generates a periodic signal with frequency f_{clk} in response to the control voltages V_{prop} and V_{int} :

$$V_{clk}(t) = A_{clk} \sin(2\pi f_{clk} t + \phi_{clk}(0)) \quad (2.3)$$

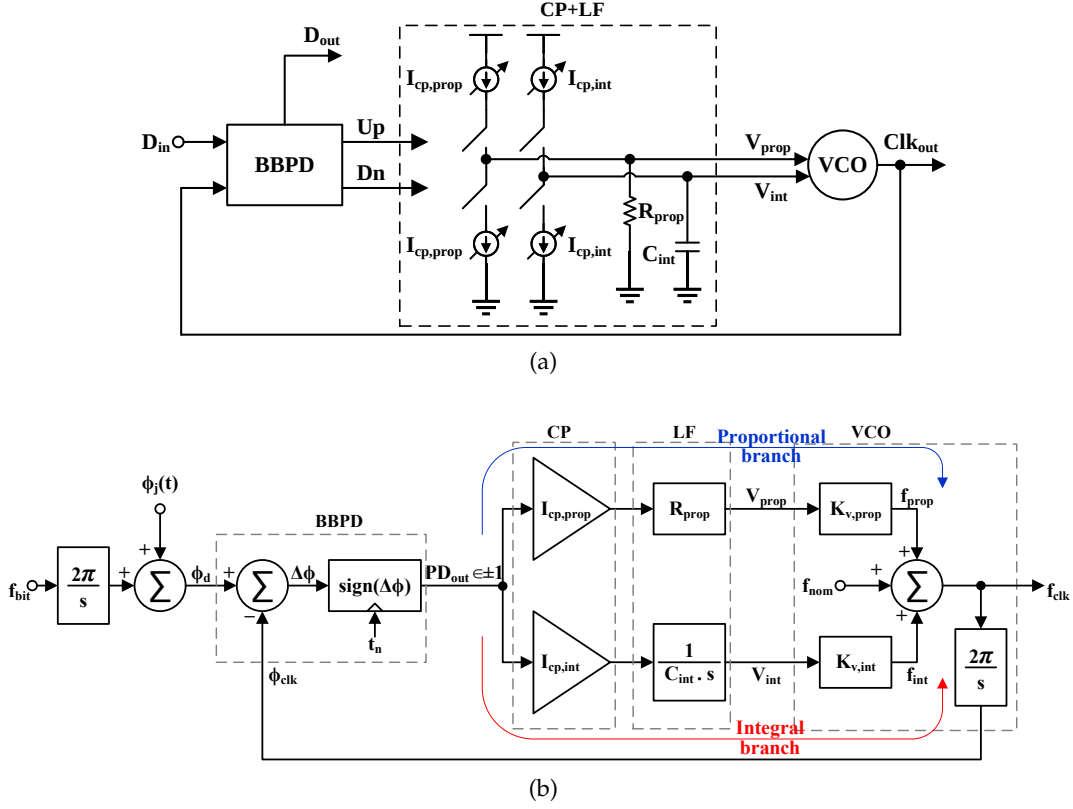


FIGURE 2.6: (a) Implemented reference-less full-rate BBBCDR circuit, and (b) Second-order Bang-Bang PLL nonlinear phase-domain model.

where $\phi_{clk}(0)$ is the initial phase. A_{clk} is the clock amplitude, chosen to reliably switch the PD logic gates.

The instantaneous VCO frequency with nominal center frequency (f_{nom}) and change due to proportional (f_{prop}) and integral (f_{int}) branches can be written as:

$$f_{clk}(t) = f_{nom} + f_{prop}(t) + f_{int}(t) \quad (2.4)$$

In particular, with the separate VCO sensitivities for proportional ($K_{v,prop}$) and integral ($K_{v,int}$) branches, the instantaneous frequency changes can be written as:

$$f_{prop}(t) = K_{v,prop} V_{prop}(t) \quad (2.5)$$

$$f_{int}(t) = K_{v,int} V_{int}(t) \quad (2.6)$$

Also the VCOs clock phase, which marks each branches phase change, can be computed by integration ($\phi = \int_0^t 2\pi f d\tau$) as,

$$\phi_{clk}(t) = 2\pi f_{nom} t + \phi_{prop}(t) + \phi_{int}(t) + \phi_{clk}(0) \quad (2.7)$$

At each sampling time ($t_n \approx n \times t_{bit}$), the phase error $\Delta\phi(t_n)$ due to the BBPD output is binary quantized to ± 1 , making it nonlinear. This quantization occurs at n discrete rising edges of the clock. The value of PD_{out} can be shown as:

$$PD_{out}(t_n) = sign(\Delta\phi) = sign(\phi_d(t_n) - \phi_{clk}(t_n)) \quad (2.8)$$

Therefore, the control voltages on the VCO can be written as:

$$V_{prop}(t_n) = PD_{out}(t_n) I_{cp,prop} R_{prop} \quad (2.9)$$

$$V_{int}(t_n) = \int_0^{t_n} PD_{out}(\tau) \frac{I_{cp,int}}{C_{int}} d\tau + V_{int}(0) = \overline{PD_{out}}(t_n) \frac{I_{cp,int}}{C_{int}} t_n + V_{int}(0) \quad (2.10)$$

Substituting (2.9) and (2.10) in (2.5) and (2.6) respectively gives us:

$$f_{prop}(t_n) = PD_{out}(t_n) \beta_{prop} \quad (2.11)$$

$$f_{int}(t_n) = \overline{PD_{out}}(t_n) \alpha_{int} t_n + f_{int}(0) \quad (2.12)$$

where,

$$\beta_{prop} = I_{cp,prop} R_{prop} K_{v,prop} \quad (2.13)$$

$$\alpha_{int} = \frac{I_{cp,int}}{C_{int}} K_{v,int} \quad (2.14)$$

Here, β_{prop} (Hz) characterizes the proportional branch gain, and α_{int} (Hz²) characterizes the rate of frequency change in the integral branch.

Additionally, the phase changes by both branches can be computed as:

$$\phi_{prop}(t_n) = 2\pi PD_{out}(t_n) \beta_{prop} t_n \quad (2.15)$$

$$\phi_{int}(t_n) = 2\pi \overline{PD_{out}}(t_n) \alpha_{int} \frac{t_n^2}{2} + \phi_{int}(0) \quad (2.16)$$

Similarly, if we compute the instantaneous frequency and phase change in each branch during each bit period, the result can be expressed as:

$$\Delta f_{prop}(t_n) = PD_{out}(t_n) \beta_{prop} \quad (2.17)$$

$$\Delta f_{int}(t_n) = PD_{out}(t_n) \alpha_{int} t_{bit} \quad (2.18)$$

$$\Delta \phi_{prop}(t_n) = 2\pi PD_{out}(t_n) \beta_{prop} t_{bit} \quad (2.19)$$

$$\Delta \phi_{int}(t_n) = 2\pi PD_{out}(t_n) \alpha_{int} \frac{t_{bit}^2}{2} \quad (2.20)$$

Fig. 2.7 shows a pictorial representation of the signals in the VCO, which updates its frequency and phase at each sample time (t_{bit}).

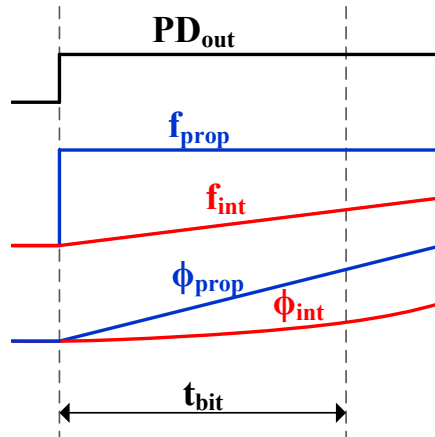


FIGURE 2.7: Response of the loop at each sample time.

In a typical BBCCR, the sum of Δf_{prop} and Δf_{int} is approximately 0.1% of f_{nom} [15]. This small change in frequency and phase within a bit period can be considered beneficial for loop performance. (2.11)-(2.16) are particularly useful during the frequency and phase acquisition mode, whereas (2.17)-(2.20) provide greater insight into the loop's behavior during the locked state, also known as the steady state.

Comparing (2.11) and (2.17), shows that the instantaneous frequency change due to proportional branch is dependent on the polarity of the phase error and is same over the entire bit period. During locked state, the VCO frequency due to this branch will be switching by $\pm f_{prop}$. The frequency change due to the integral branch will ramp up or down with a slope of $(I_{cp,int}/C_{int})$ as per (2.12) and (2.18).

If we examine the phase change during acquisition mode and locked state, the phase contribution due to the proportional branch increases linearly in both cases, as described by (2.15) for acquisition mode and (2.19) for the locked state. In contrast, the phase change due to the integral branch follows a parabolic or quadratic trajectory over time, as described by (2.16) during acquisition and (2.20) in the locked state.

The bang-bang jitter at the output of the PLL during locked or steady state without input jitter can be written as:

$$J_{pp} = 2(\Delta\phi_{prop} + \Delta\phi_{int}) = 4\pi(\beta_{prop} t_{bit} + \alpha_{int} \frac{t_{bit}^2}{2}) \quad (2.21)$$

2.2.2 Stability factor

The stability factor ξ , which quantifies the relative independence of the two feedback branches, is defined as the ratio of the phase change due to the proportional branch to the phase change due to the integral branch [15]:

$$\xi = \frac{\Delta\phi_{prop}}{\Delta\phi_{int}} = \frac{2\beta_{prop}}{t_{bit} \alpha_{int}} \quad (2.22)$$

To maintain loop stability, the phase change due to the proportional branch must be significantly greater than the phase change due to the integral branch within each bit period, resulting in the stability criterion $\xi \gg 1$.

2.2.3 Frequency acquisition

In a locked PLL without data jitter (i.e., $\phi_j(t) = 0$), the applied data may exhibit an initial frequency deviation δf and an initial phase deviation $\Delta\phi_{init}$ with respect to the clock, which are corrected after sometime by the PLL action. During this transient, the phases ϕ_d and ϕ_{clk} can deviate significantly without losing lock. Hence we call these phases excess phase of data ($\phi_{d,ex}$) and VCO ($\phi_{clk,ex}$). The instantaneous phase error $\Delta\phi(t_n)$ between $\phi_{d,ex}(t_n)$ and $\phi_{clk,ex}(t_n)$ can be expressed as:

$$\Delta\phi(t_n) = \phi_{d,ex}(t_n) - \phi_{clk,ex}(t_n) \quad (2.23)$$

where the excess phases are relative to $2\pi f_{nom}t$ from (2.2) and (2.7), with $\phi_{clk}(0)$ absorbed into $\Delta\phi_{init}$. Thus,

$$\phi_{d,ex}(t_n) = \phi_d(t_n) - 2\pi f_{nom} t_n = 2\pi \delta f t_n + \Delta\phi_{init} \quad (2.24)$$

$$\phi_{clk,ex}(t_n) = \phi_{clk}(t_n) - 2\pi f_{nom} t_n = \phi_{prop}(t_n) + \phi_{int}(t_n) \quad (2.25)$$

Assuming a positive δf and a positive $\Delta\phi_{init}$, the BBPD produces a series of UP pulses, resulting in $PD_{out} = +1$. The PLL then attempts to catch up with the excess data phase to minimize the error, as shown in Fig 2.8a. After $t_n = t_{acq}$, $\Delta\phi(t_n)$ becomes zero. Consequently, (2.23) can be rewritten using (2.24), (2.25), (2.15) and (2.16), for $t_n = t_{acq}$ as:

$$2\pi\delta f t_n + \Delta\phi_{init} = 2\pi\left(\beta_{prop} t_n + \alpha_{int} \frac{t_n^2}{2}\right) \quad \text{and} \quad (2.26)$$

$$2\pi\left(\frac{\alpha_{int}}{2}\right) t_n^2 - 2\pi(\delta f - \beta_{prop}) t_n - \Delta\phi_{init} = 0 \quad (2.27)$$

Solving for t_n yields two possible solutions:

$$t_n = \frac{2\pi(\delta f - \beta_{prop}) \pm \sqrt{(4\pi^2(\delta f - \beta_{prop})^2 + 4\pi\alpha_{int}\Delta\phi_{init})}}{2\pi\alpha_{int}} \quad (2.28)$$

A real-valued solution exists if the argument of the square root is non-negative:

$$4\pi^2(\delta f - \beta_{prop})^2 + 4\pi\alpha_{int}\Delta\phi_{init} \geq 0 \quad (2.29)$$

Following a similar approach as in [33], consider the worst case scenario where $\Delta\phi_{init} \approx \pi$. Substitute this value into (2.28) yields the acquisition time $t_{acq,bb}$, which is defined as the time when the excess clock phase and the excess data phase coincide, i.e., $\Delta\phi(t_n) = 0$. It can be expressed as:

$$t_{acq,bb} = \frac{(\delta f - \beta_{prop}) + \sqrt{(\delta f - \beta_{prop})^2 + \alpha_{int}}}{\alpha_{int}} \quad (2.30)$$

For random or long-pattern data, this result must be scaled by the appropriate data transition density and adjusted for the frequency deviation δf . Additionally, the stability factor ξ plays a significant role, as discussed in the following examples in subsection 2.2.4.

From (2.29), we can determine the maximum frequency deviation, δf_{max} , that the BBCCR can acquire before the phase error exceeds $\pm\pi$ during acquisition. When the

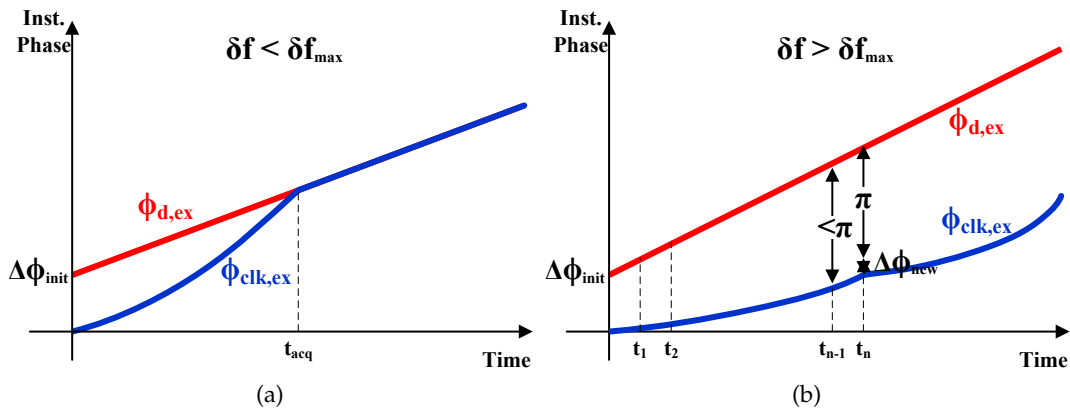


FIGURE 2.8: Bang-Bang PLL response illustrating: (a) successful acquisition when the frequency deviation is within the acquisition range, and (b) failed acquisition when the frequency deviation exceeds the acquisition range.

phase error exceeds $+\pi$ as shown in the Fig. 2.8b, the BBPD wraps the phase to $-\pi$ resulting in a polarity reversal in PD_{out} and the new phase deviation $\Delta\phi_{new}$. This reversal causes the loop to lose lock of the data phase, resulting in acquisition failure. Therefore, by replacing $\Delta\phi_{init} = -\pi$ in (2.29), the maximum allowable frequency deviation δf_{max} can be calculated as follows:

$$\delta f_{max} \leq |\beta_{prop} + \sqrt{\alpha_{int}}| \quad (2.31)$$

This result is consistent with the analysis presented in [32]. The overall inherent frequency acquisition range of the BBCDR can thus be expressed as:

$$\delta f_{acq,bb} = \pm \delta f_{max} \quad (2.32)$$

$\delta f_{acq,bb}$ is a key performance metric of a BBCDR, since it quantifies the PLLs ability to acquire a lock after being switched on when the VCO frequency f_{clk} deviates from f_{nom} and δf .

2.2.4 Extending frequency acquisition range via loop parameters

To gain an intuitive understanding of how loop parameters can influence the frequency acquisition range of a BBCDR, we now consider the effect of enabling and scaling the integral branch current. Consider a BBCDR operating around 25 Gbps NRZ data rate ($t_{bit} = 40$ ps). A VCO is designed with a nominal center frequency of $f_{nom} = 25$ GHz and a tuning range of approximately 10%. The proportional and integral branches are configured with VCO sensitivities $K_{v,prop} = 200$ MHz/V and $K_{v,int} = 1000$ MHz/V, respectively. The control voltages V_{prop} and V_{int} are allowed to vary within ± 1 V. The LF components are set to $R_{prop} = 50 \Omega$, and $C_{int} = 20$ pF. The proportional branch CP current is fixed at $I_{cp,prop} = 1$ mA, while the integral branch CP current is varied across cases.

Example 2.1 (Stability Factor $\xi = \infty$). *The integral branch is disabled. The proportional branch tracking range is $f_{prop} = \pm 10$ MHz.*

Fig. 2.9a shows the simulation of a first-order PLL, when the frequency deviation is $\delta f = 5$ MHz $< f_{prop}$, the loop remains locked, and the average VCO frequency matches the input frequency. However, when the frequency deviation increases to $\delta f = 20$ MHz $> f_{prop}$, as shown in Fig. 2.9b, the loop loses lock and begins to chase the phase, adjusting the VCO frequency in response to the phase error (in this case, the UP signal). When the phase error $\Delta\phi$ exceeds $\pm\pi$ (or 180 deg), the BBPD wraps the polarity of the error signal, causing the clock to change from lagging to leading the data, or vice versa (c.f. Fig 2.4b). When the phase error subsequently crosses zero, the loop attempts to reacquire lock; however, since the clock and data frequencies remain misaligned, the system continues to accumulate phase error, resulting in bit errors.

Example 2.2 (Stability Factor $\xi = 1000$). *The integral branch is enabled, with the CP current set to $I_{cp,int} = 10$ μ A. This results in a stability factor of $\xi = 1000$, calculated using (2.22), indicating strong proportional dominance. The maximum combined frequency deviation is $|\Delta f_{prop} + \Delta f_{int}| = 10.02$ MHz, which corresponds to only 0.04% of f_{nom} . From (2.13) and (2.14), the gains are calculated as $\beta_{prop} = 10$ MHz and $\alpha_{int} = 5 \times 10^{14}$ Hz². Using (2.31), the maximum acquisition range is $\delta f_{acq,bb} \approx \pm 32$ MHz with the corresponding acquisition time for $\delta f = \delta f_{max}$, obtained from (2.30) is $t_{acq,bb} \approx 108$ ns.*

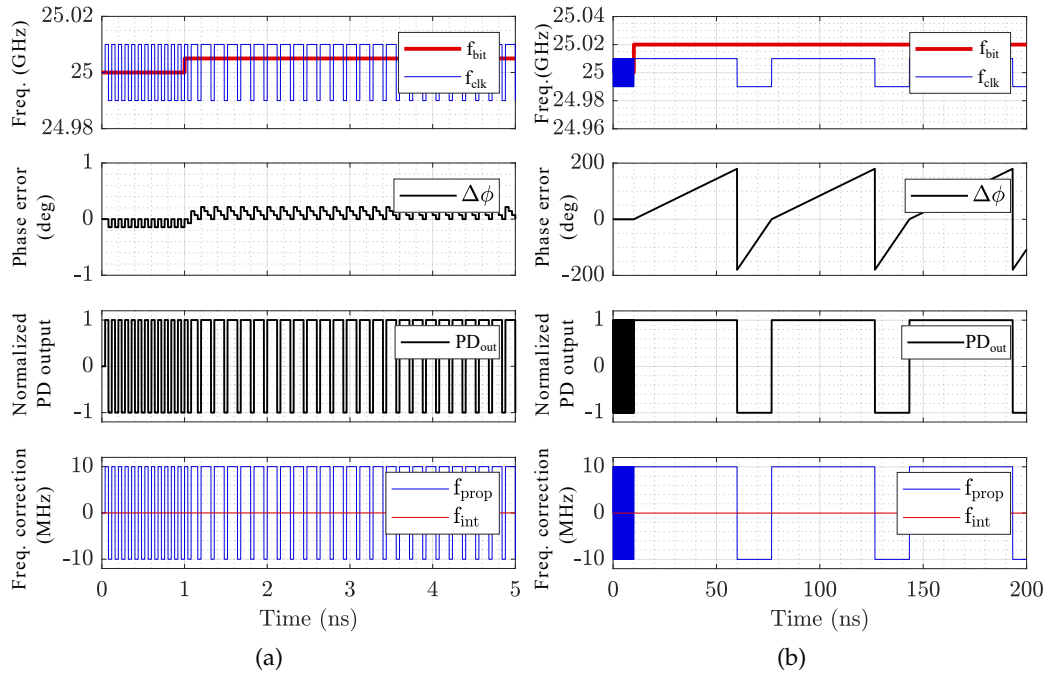


FIGURE 2.9: Simulated response of a first-order PLL with the integral branch disabled: (a) loop remains locked for $\delta f = 5$ MHz, within the proportional tracking range, and (b) loop loses lock for $\delta f = 20$ MHz, beyond the proportional tracking range.

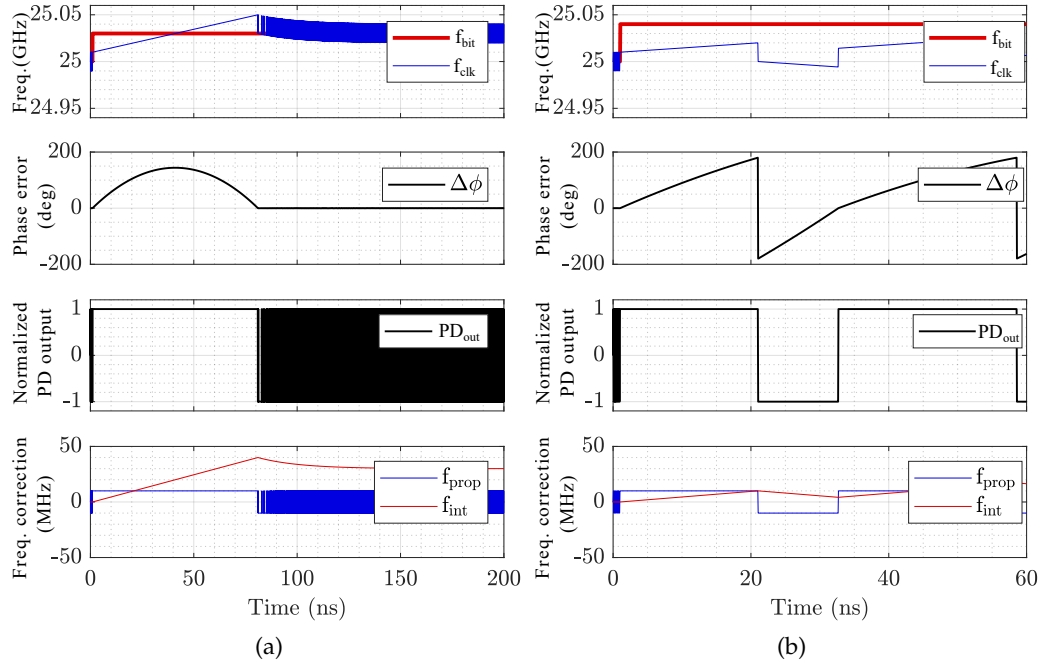


FIGURE 2.10: Simulated response of a second-order PLL with stability factor $\xi = 1000$ and maximum acquisition range $\delta f_{\text{acq},bb} \approx \pm 32$ MHz: (a) successful acquisition for $\delta f = 30$ MHz, and (b) acquisition failure for $\delta f = 40$ MHz.

When a frequency deviation of $\delta f = +30 \text{ MHz} < \delta f_{acq,bb}$ is present, the PLL successfully tracks this deviation, as shown in Fig. 2.10a. The acquisition is completed within 100 ns. The phase error $\Delta\phi$, remains below $+\pi$ (180 deg), with the integral branch frequency f_{int} gradually adjusting to the step and the proportional branch frequency alternating between $\pm f_{prop}$. This dynamic demonstrates the role of the integral branch in extending the acquisition range. On the other hand, when the frequency deviation exceeds the acquisition range, such as $\delta f = +40 \text{ MHz} > \delta f_{acq,bb}$, the loop fails to acquire lock, as shown in Fig. 2.10b. The phase error exceeds $+\pi$, causing the BBPD output PD_{out} to reverse polarity, leading to further divergence and eventual acquisition failure.

Example 2.3 (Stability Factor $\xi = 100$). To further extend the acquisition range, the integral branch CP current is increased to $I_{cp,int} = 100 \mu\text{A}$ - a tenfold increase from the previous setting - while all other parameters remain unchanged. The maximum combined frequency deviation increases slightly to $|\Delta f_{prop} + \Delta f_{int}| = 10.10 \text{ MHz}$, which is still about 0.04% of f_{nom} , similar to the previous case. The integral gain increases to $\alpha_{int} = 5 \times 10^{15} \text{ Hz}^2$, which reduces the stability factor to $\xi = 100$. As a result, the acquisition range improves to $\delta f_{acq,bb} \approx \pm 81 \text{ MHz}$, and the acquisition time for $\delta f = \delta f_{max}$ is reduced to be $t_{acq,bb} \approx 35 \text{ ns}$.

When a frequency deviation of $\delta f = 80 \text{ MHz}$ is present, the PLL successfully tracks this deviation, as shown in Fig. 2.11a. The phase error $\Delta\phi$, remains below $+\pi$ (180 deg), and the integral branch frequency f_{int} adjusts accordingly. Due to the more underdamped response at $\xi = 100$, the output clock frequency f_{clk} crosses the input frequency within 35 ns, but continues to oscillate before settling. The total

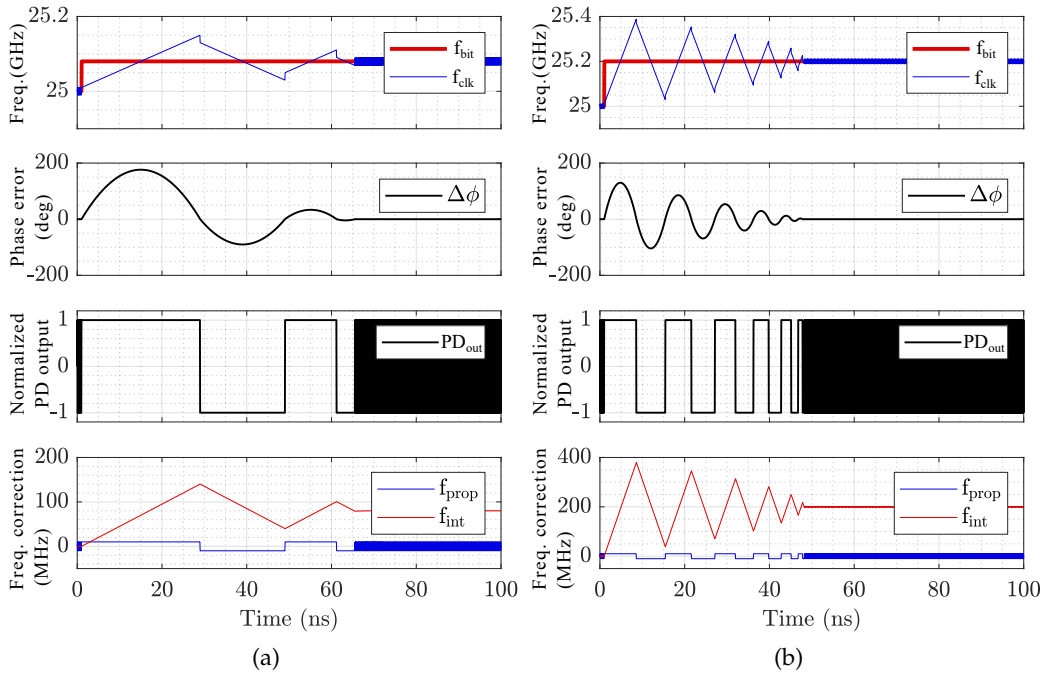


FIGURE 2.11: Simulated response of a second-order PLL for two stability factors: (a) $\xi = 100$ with the acquisition range $\delta f_{acq,bb} \approx \pm 81 \text{ MHz}$, showing successful acquisition for $\delta f = 80 \text{ MHz}$, and (b) $\xi = 10$ with the acquisition range $\delta f_{acq,bb} \approx \pm 233 \text{ MHz}$, showing successful acquisition for $\delta f = 200 \text{ MHz}$.

acquisition time, including overshoot and settling, is about twice the initial crossing time, i.e., around 70 ns.

Example 2.4 (Stability Factor $\xi = 10$). *To push the acquisition range even further, the integral branch CP current is increased significantly, trading off loop stability for faster response. In this case, $I_{cp,int} = 1000 \mu\text{A}$ is chosen, and the resulting maximum combined frequency deviation is $|\Delta f_{prop} + \Delta f_{int}| = 19.98 \text{ MHz}$, which is about 0.08% - still below 0.1%, but significantly higher than in the previous cases. The integral gain increases to $\alpha_{int} = 5 \times 10^{16} \text{ Hz}^2$, which reduces the stability factor to $\xi = 10$, indicating a highly underdamped loop. As a result, the acquisition range expands significantly to $\delta f_{acq,bb} \approx \pm 233 \text{ MHz}$, and the acquisition time for $\delta f = \delta f_{max}$ is further reduced to $t_{acq,bb} \approx 10.8 \text{ ns}$.*

Fig. 2.11b shows the response to a frequency deviation of $\delta f = 200 \text{ MHz}$, which is within the extended acquisition range. Due to the low stability factor, the PLL shows a much more pronounced underdamped response compared to the previous cases. The output clock frequency f_{clk} crosses the input frequency within about 10 ns, but then goes into oscillation with a much larger overshoot. The total acquisition time, including overshoot and settling, increases to about five times the initial crossing time, i.e., around 50 ns. This clearly illustrates the classic speed/stability trade-off: while the lock is achieved faster, the reduced damping results in less predictable and more oscillatory transient behavior.

The VCO in this design supports a tuning range of $\pm 1 \text{ GHz}$ via the control voltage V_{int} connected to the integral branch. However, in all cases only a fraction of this range was effectively used. Specifically, the acquisition range was limited to $\delta f_{acq,bb}$. This limitation is due to the stability constraints imposed by the loop dynamics. This inefficiency motivates the exploration of different frequency acquisition techniques, which are introduced in the next chapter 3. These methods aim to extend the usable VCOs tuning range without sacrificing loop stability or reliability. In addition to acquisition dynamics, the effect of input jitter on tracking performance also becomes critical - this will be the focus of the next section.

2.3 Jitter Characterization

Jitter characterization is essential in any transmission system, as jitter can cause bit errors and degrade the system performance. Jitter of data or clock shifts the decision point away from the optimal position. Many optical communication standards specify jitter requirements at both the optical and electrical interfaces, categorized into three main specifications which are associated with specific test methods: Jitter Transfer Function (JTF), Jitter Tolerance (JTOL) and Jitter Generation (JGEN).

The JTF test evaluates the jitter transmitted from the input to the recovered data or clock regeneration circuits, ensuring that the circuit does not add or amplify jitter to unacceptable levels. Conversely, the JTOL test measures the circuit's ability to handle incoming jitter without severe BER degradation. Standards define a template that specifies the range within which the circuit must maintain the required BER. Finally, intrinsic JGEN quantifies the jitter produced by the circuit itself, establishing an expected baseline when no input jitter is present.

2.3.1 Jitter transfer function

Focusing on the JTF and JTOL, which characterize the output jitter relative to the input jitter, the behavioral model previously shown in Fig. 2.6b is reformulated and

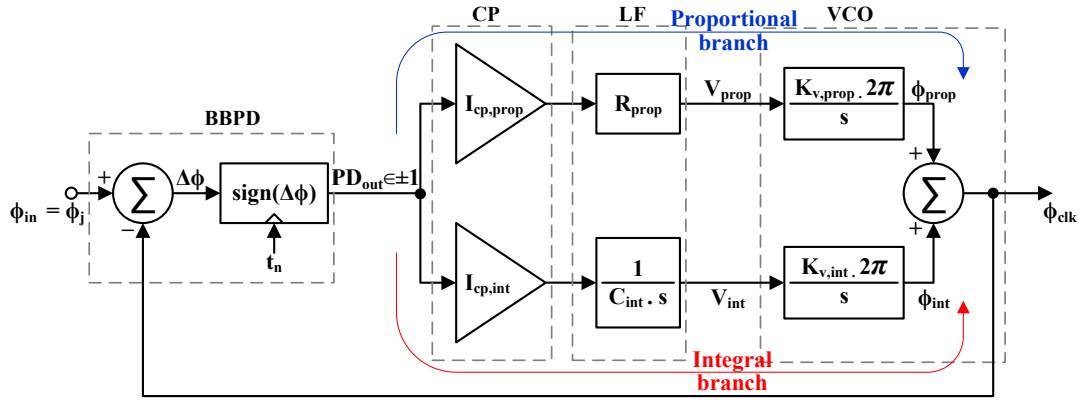


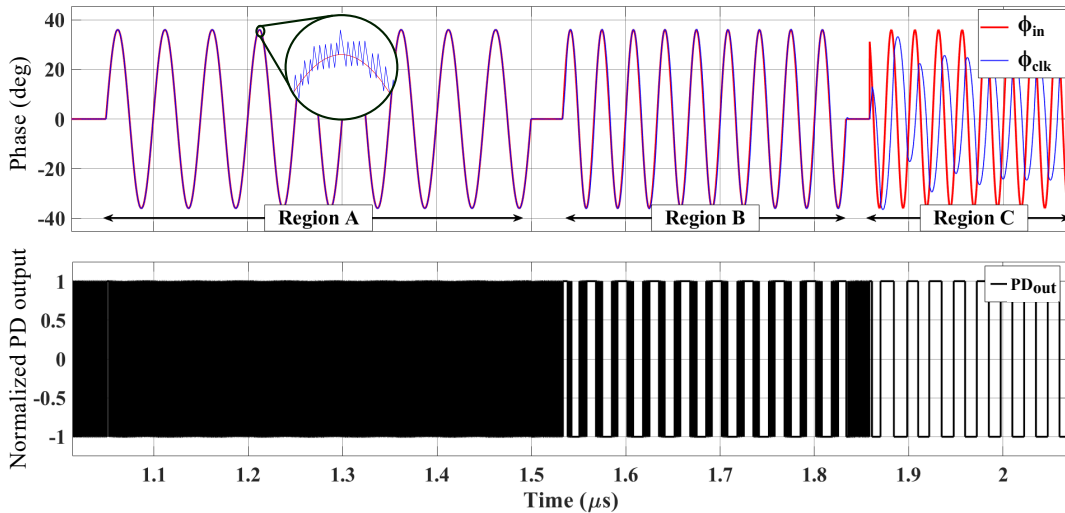
FIGURE 2.12: Phase domain behavior model for JTF and JTOL.

illustrated in Fig. 2.12. The PLL is assumed to be in lock, with frequency acquisition completed. As a result, there is only input jitter, and the clock phase at the output consists only of phase contributions from the proportional and integral branches of the PLL, as defined in (2.25).

The applied input jitter is modeled as a sinusoidal signal, where the jitter amplitude A_j is specified in unit intervals (UI) and the jitter frequency f_j in Hertz. The resulting input phase variation can be written as:

$$\phi_{in}(t_n) = 2\pi A_j \cos(2\pi f_j t_n) \quad (2.33)$$

Fig. 2.13 shows the behavior of the PLL as the applied jitter frequency is swept (i.e., gradually increased), while keeping the jitter amplitude constant. When the jitter frequency is low, the loop closely tracks the input phase. As a result, the jitter amplitude transfer ratio approaches unity, i.e., $|A_{j,clk}/A_j| \approx 1$, where $A_{j,clk}$ is the output clock jitter amplitude. In this regime, the BBPD output PD_{out} toggles quickly between ± 1 , ensuring accurate phase tracking. This behavior defines Region A. As the jitter frequency increases, the output phase begins to lag the input phase for longer periods, but continues to track it, advancing at a rate defined by (2.25). In

FIGURE 2.13: Jitter transfer behavior for a fixed input jitter amplitude A_j and varying jitter frequencies f_j .

this regime, PD_{out} exhibits extended durations of +1 or -1 in response to steeper input phase slopes, and more frequent toggling for gentler slopes. Despite this lag, the jitter amplitude transfer ratio remains close to unity. This behavior defines Region B. At even higher jitter frequencies, the output phase can no longer effectively follow the input, resulting in slewing behavior. In this regime, PD_{out} alternates between +1 and -1 with a period $T_j = 1/f_j$ and the jitter amplitude transfer ratio gradually decreases as f_j increases. This marks the onset of Region C. Importantly, the PLL remains locked and in steady state across all these regions. The jitter transfer function, denoted as H_j , is defined as the ratio of the output jitter amplitude, $A_{j,clk}$, to the input jitter amplitude, A_j , evaluated as a function of the jitter frequency, f_j , assuming sinusoidal input jitter [38]. These different operating regions and their respective characteristics are summarized in Fig. 2.14a.

Although the loop closely tracks the input at low jitter frequencies in Region A or Region B, the non-linearity introduced by the BBPD output PD_{out} results in jitter amplification. The output clock jitter in these regions consists of the input jitter superimposed with the bang-bang jitter J_{pp} , as defined in (2.21), which ensures that the loop remains locked. This combined effect is shown in the zoomed-in portion of Region A in Fig. 2.13. Consequently, the maximum jitter amplification, H_j in the tracking Region A or B can be written as:

$$\max |H_j| (dB) = 20 \log_{10} (1 + J_{pp}) . \quad (2.34)$$

In the slewing Region C, the jitter performance is analyzed using the large-signal piecewise linear model described in [28], as well as the Fourier series-based approach described in [34] and later extended in [35]. We use these approaches to predict key characteristics of the jitter transfer function, including the jitter peaking (JP) and the corner frequency (f_{jc}), and to formulate a mathematical model that captures the independent tunability of the proportional and integral parameters of the PLL. In parallel, behavioral simulations provide results that more closely reflect practical

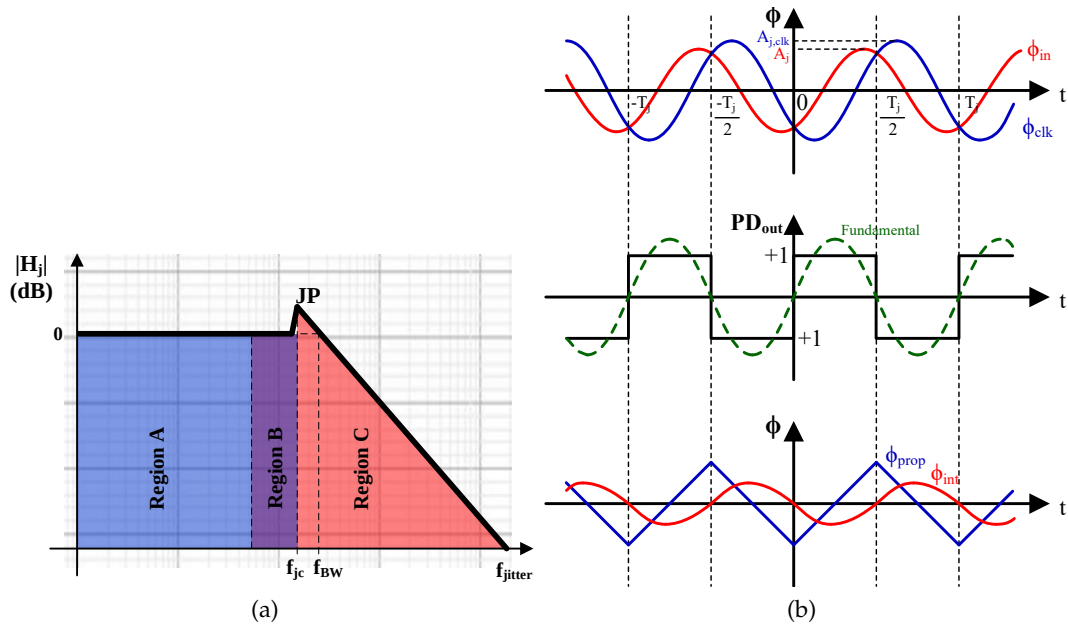


FIGURE 2.14: (a) Characteristics of JTF, and (b) Time-domain waveform in slewing Region C near f_{jc} .

circuit behavior, thereby improving both the accuracy and reliability of the analysis.

Fig. 2.14b shows the behavior of the loop in the slewing Region C for a jitter frequency near the corner frequency f_{jc} . The transfer function (c.f. Fig. 2.12), which relates the BBPD output PD_{out} to the clock phase ϕ_{clk} is given as:

$$H(s) = \frac{\Phi_{clk}}{PD_{out}}(s) = \left[I_{cp,prop} R_{prop} \frac{2\pi K_{v,prop}}{s} + \frac{I_{cp,int}}{C_{int}} \frac{2\pi K_{v,int}}{s} \right] \quad (2.35)$$

By performing the inverse Laplace transform of (2.35) and substituting the definitions of β_{prop} and α_{int} from (2.13) and (2.14), respectively, the resulting differential equation for the clock phase is:

$$\frac{d^2\phi_{clk}(t)}{dt^2} = 2\pi \left[\beta_{prop} \frac{dPD_{out}(t)}{dt} + \alpha_{int} PD_{out}(t) \right] \quad (2.36)$$

Using the Fourier series expansion, the periodic square wave signal $PD_{out}(t)$ can be expressed as:

$$PD_{out}(t) = a_0 + \sum_{n=1,3,5,\dots}^{+\infty} [a_n \cos(n\omega_j t) + b_n \sin(n\omega_j t)] \quad (2.37)$$

where the Fourier coefficients are given by:

$$a_0 = \frac{1}{T_j} \int_0^{T_j} PD_{out}(t) dt \quad (2.38)$$

$$a_n = \frac{2}{T_j} \int_0^{T_j} PD_{out}(t) \cos(n\omega_j t) dt \quad (2.39)$$

$$b_n = \frac{2}{T_j} \int_0^{T_j} PD_{out}(t) \sin(n\omega_j t) dt \quad (2.40)$$

Using the relation $\omega_j = 2\pi f_j = 2\pi/T_j$, the Fourier coefficients of square-wave signal $PD_{out}(t)$, can be given by $a_0 = 0$, $a_n = 0$ and $b_n = \frac{4}{\pi n}$ for odd n . Consequently, $PD_{out}(t)$ can be expressed as:

$$PD_{out}(t) = \sum_{n=1,3,5,\dots}^{+\infty} \left[\frac{4}{\pi n} \sin(n\omega_j t) \right] \quad (2.41)$$

Taking the derivative of PD_{out} with respect to time yields:

$$\begin{aligned} \frac{dPD_{out}}{dt} &= \sum_{n=1,3,5,\dots}^{+\infty} \left[\frac{4}{\pi n} \frac{d}{dt} \sin(n\omega_j t) \right] \\ &= \sum_{n=1,3,5,\dots}^{+\infty} \left[\frac{4\omega_j}{\pi} \cos(n\omega_j t) \right] \end{aligned} \quad (2.42)$$

Substituting the Fourier expansions from (2.41) and (2.42) into the differential equation (2.36), we obtain:

$$\frac{d^2\phi_{clk}}{dt^2} = 2\pi \sum_{n=1,3,5,\dots}^{+\infty} \left[\frac{4\omega_j \beta_{prop}}{\pi} \cos(n\omega_j t) + \frac{4\alpha_{int}}{\pi n} \sin(n\omega_j t) \right] \quad (2.43)$$

Integrating (2.43) twice with respect to time yields the Fourier series representation of the continuous-time clock phase $\phi_{clk}(t)$ as:

$$\phi_{clk}(t) = -8\omega_j \beta_{prop} \sum_{n=1,3,5,\dots}^{+\infty} \frac{\cos(n\omega_j t)}{(n\omega_j)^2} - 8\alpha_{int} \sum_{n=1,3,5,\dots}^{+\infty} \frac{\sin(n\omega_j t)}{n(n\omega_j)^2} \quad (2.44)$$

The loop response is primarily influenced by the fundamental harmonic, since the transfer function $H(s)$ in (2.35) exhibits a low-pass filtering behavior that attenuates higher order harmonics. Moreover, from (2.44), the magnitude of the n -th harmonic decreases with $1/n^2$ making its contribution negligible:

$$|\phi_{clk}(\omega_j t)| \gg |\phi_{clk}(n, \omega_j t)|, \quad \text{for } n = 3, 5, \dots \quad (2.45)$$

The output phase can therefore be approximated using only the fundamental component:

$$\phi_{clk}(t) \cong -a_1 \cos(\omega_j t) - b_1 \sin(\omega_j t) \quad (2.46)$$

Using an addition theorem, this expression can be rewritten as:

$$\phi_{clk}(t) = -\sqrt{a_1^2 + b_1^2} \cos\left(\omega_j t + \tan^{-1}\left(\frac{-b_1}{a_1}\right)\right) \quad (2.47)$$

where a_1 and b_1 depend on the jitter frequency:

$$a_1(f_j) = \frac{8\beta_{prop}}{\omega_j} \quad (2.48)$$

$$b_1(f_j) = \frac{8\alpha_{int}}{\omega_j^2} \quad (2.49)$$

From (2.46), the initial output phase is given by:

$$\phi_{clk}(0) = \theta_0 = \frac{-8\beta_{prop}}{\omega_j} \quad (2.50)$$

To simplify the analysis of the system dynamics and enable comparison with (2.47), the input phase expression in (2.33) can be reformulated by adjusting the time scale as shown in Fig. 2.14b:

$$\phi_{in}(t) = -2\pi A_j \cos(\omega_j t + \theta_0) \quad (2.51)$$

In the slewing Region C, when the jitter amplitude ratio approaches unity, i.e., $|A_{j,clk}/A_j| \approx 1$, and the jitter frequency is close to the frequency f_{BW} , we equate the amplitudes of the output and input phase expressions from (2.47) and (2.51). This yields:

$$\frac{\sqrt{a_1^2 + b_1^2}}{2\pi A_j} = \frac{\sqrt{(8\beta_{prop}\omega_j)^2 + (8\alpha_{int})^2}}{2\pi A_j \omega_j^2} = 1 \quad (2.52)$$

$$4\pi^2 A_j^2 \omega_j^4 - 64\beta_{prop}^2 \omega_j^2 - 64\alpha_{int}^2 = 0 \quad (2.53)$$

Simplifying (2.53) gives us an approximate value for the -3dB bandwidth with $\omega_{-3dB} \stackrel{!}{=} \omega_j$:

$$\omega_{-3dB} \approx \frac{2\beta_{prop}}{\pi A_j} \sqrt{2 + \sqrt{4 + \left(\frac{\phi_{in,p}^2 \alpha_{int}^2}{4\beta_{prop}^4}\right)}} \quad (2.54)$$

The bandwidth of the BBCCR is inversely proportional to the input jitter amplitude (A_j) and cannot be set as directly as the bandwidth in a standard PLL. Therefore, this characteristic frequency is also often referred to as the corner frequency, f_{jc} [38]. The bandwidth also increases with the integral gain α_{int} . For large stability factors ($\xi \gg 1$), where the proportional branch dominates, the bandwidth simplifies to:

$$\omega_{-3dB} \approx \frac{4\beta_{prop}}{\pi A_j} \quad (2.55)$$

indicating that the proportional branch and the input jitter amplitude primarily set the bandwidth or corner frequency.

Comparing (2.47) and (2.51) shows that the integral branch, through its dependence on b_1 , increases the clock jitter amplitude and introduces a phase shift of the recovered clock ($\tan^{-1}(-b_1/a_1)$). Larger $|b_1|$ values, regardless of sign, lead to greater phase deviation of ϕ_{clk} relative to ϕ_{in} .

From another perspective, the BBPD output PD_{out} produces a square-wave voltage V_{prop} in the proportional branch and a triangular voltage V_{int} in the integral branch. These result in triangular and parabolic phase trajectories, respectively, due to successive phase integration by the VCO. In the proportional branch, the triangular phase lags the square-wave voltage by 90 degrees, while in the integral branch, the parabolic phase introduces an additional 90 degree lag, resulting in a total phase lag of 180 degrees. At low jitter frequencies (Region A or B), the proportional branch dominates because the capacitor cannot respond effectively due to the bang-bang jitter. As the jitter frequency increases (in Region C), the proportional branch becomes less effective due to the limited response time before the BBPD output reverses, allowing the integral branch to become more influential. Although the phase amplitudes of both branches decrease as the jitter frequency continues to increase, the integral branch decays more slowly, and thus retains dominance in the high jitter frequency region.

Jitter peaking occurs near the lower edge of the slewing Region C, just below the -3dB bandwidth, at the corner frequency f_{jc} . It can be quantified as:

$$JP = 20 \log \left(\frac{2\pi A_{j,clk}}{2\pi A_j} \right) \leq JP_{max}(f_{jc}) \quad (2.56)$$

where $JP_{max}(f_{jc})$ denotes the maximum allowable jitter peaking at the corner frequency f_{jc} , as specified by the jitter transfer requirement. Substituting the amplitude of the clock phase from (2.47) into (2.56), we get the following condition:

$$\sqrt{a_1^2 + b_1^2} \leq 2\pi A_j 10^{\frac{JP_{max}}{20}} \quad (2.57)$$

This expression allows to determine a_1 and b_1 for a given A_j and JP_{max} , which is consistent with the result reported in [34].

Jitter peaking results from the combined contribution of the proportional and integral branches. To meet the jitter transfer specifications defined by the standard, the

loop parameters can be appropriately selected to minimize the peaking introduced by the integral branch.

Fig. 2.15a shows the simulated JTF for two stability factors, $\xi = 1000$ ($I_{cp,int} = 10 \mu A$) and $\xi = 100$ ($I_{cp,int} = 100 \mu A$), corresponding to Examples 2.2 and 2.3. As the input jitter amplitude A_j increases, the 3dB bandwidth decreases (refer to (2.54)), consistent with the analytical prediction. In the slewing region C, increasing the integral branch (larger $I_{cp,int}$, i.e., smaller ξ) causes the simulated jitter peaking (JP) near the corner frequency f_{jc} to increase, as described by (2.57). This demonstrates the impact of b_1 (refer to (2.47)): as $|b_1|$ increases, both the amplitude and the phase deviation of the clock (ϕ_{clk}) grow, with the phase shift given by $\tan^{-1}(-b_1/a_1)$ relative to the input. Time-domain waveforms near f_{jc} are shown in Fig. 2.15b and Fig. 2.15c, for proportional ($\xi = 1000$) and integral ($\xi = 100$) branch dominance, respectively. These figures illustrate that higher b_1 —i.e., stronger integral action—leads to greater phase deviation and increased jitter peaking in the recovered clock.

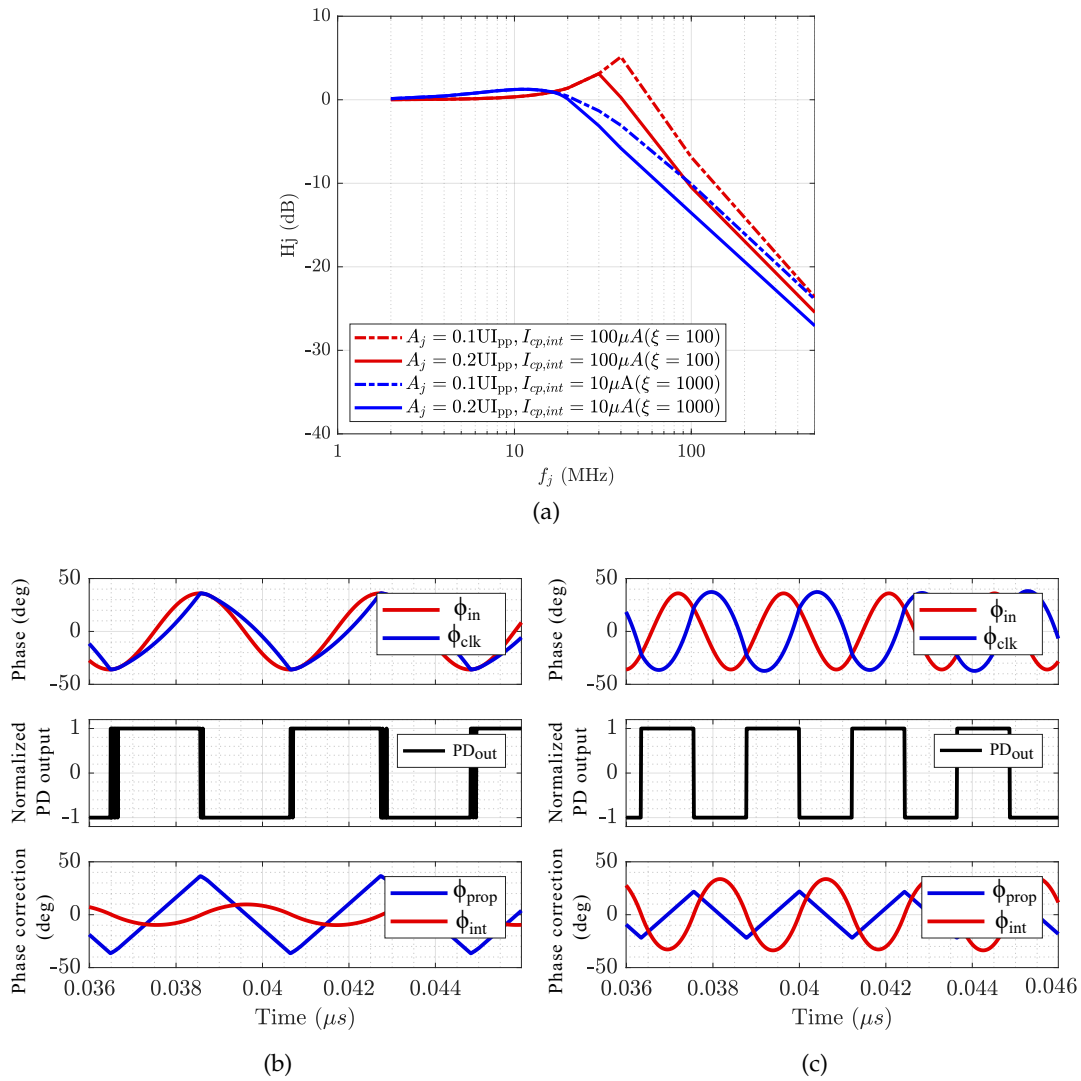


FIGURE 2.15: Simulated (a) JTF characteristics for different jitter amplitudes A_j and integral branch CP currents $I_{cp,int}$, (b) time-domain response of the bang-bang PLL near the corner frequency f_{jc} with proportional branch dominant ($\xi = 1000$) (c) response with integral branch dominant ($\xi = 100$).

2.3.2 Jitter tolerance

The Jitter Tolerance (JTOL) mask, shown in Fig. 2.16a, defines the maximum sinusoidal input jitter amplitude A_j , expressed in UI, that a CDR can tolerate at a given jitter frequency f_j without exceeding the BER beyond a specified limit. In the JTOL test, jitter is applied to the input data, and the recovered data stream is monitored to determine if the BER meets the standards. Specifically, for each jitter frequency f_j , a jitter amplitude is swept to evaluate the tolerance of the loop. In the tracking regions (Region A and B, as shown in 2.14a), the phase error, $\Delta\phi$, remains small (i.e., $\phi_m \ll \pi$; see Fig. 2.4b), resulting in correct data sampling and higher jitter tolerance [28]. In contrast, in the slewing Region C, bit errors begin to occur rapidly even at lower jitter amplitudes, resulting in reduced tolerance. Therefore, a maximum phase error of $\Delta\phi = \pi$ (equivalent to 0.5 UI) is commonly used as an upper bound on jitter tolerance. Note: This analysis neglects the effect of noise on the data and is only valid under well-controlled, low-noise test conditions. In practical systems, the presence of noise typically results in degraded jitter tolerance.

As shown in Fig. 2.16b, input jitter in the slewing Region C can be modeled as:

$$\begin{aligned}\phi_{in}(t) &= 2\pi A_j \sin(\omega_j t - \theta_0) \\ &= 2\pi A_j [\sin(\omega_j t) \cos \theta_0 - \cos(\omega_j t) \sin \theta_0].\end{aligned}\quad (2.58)$$

Here, θ_0 is the initial phase, derived from (2.50). In this analysis, ϕ_{clk} is treated as the recovered data phase, since jitter tolerance measures the deviation between the input and the output data. From Fig. 2.14b, we find $\phi_{in}(0) = \phi_{clk}(0)$. We obtain with (2.46) as:

$$\phi_{in}(0) = -2\pi A_j \sin \theta_0 = -a_1 \quad (2.59)$$

Applying the trigonometric identity,

$$2\pi A_j \cos \theta_0 = \sqrt{(2\pi A_j)^2 - a_1^2} \quad (2.60)$$

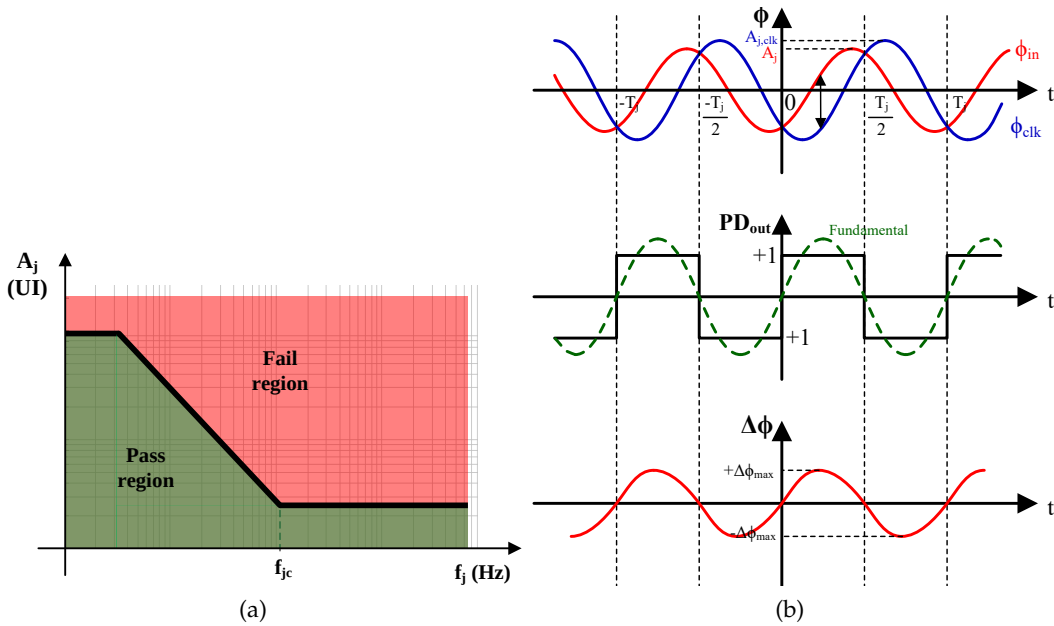


FIGURE 2.16: (a) Typical JTOL mask, and (b) Time-domain waveforms in slewing Region C.

and using (2.46), (2.59) and (2.58), the phase error becomes:

$$\begin{aligned}\Delta\phi &= \phi_{in}(t) - \phi_{clk}(t) \\ &= 2\pi A_j \sin(\omega_j t - \theta_0) + a_1 \cos(\omega_j t) + b_1 \sin(\omega_j t) \\ &= (\sqrt{(2\pi A_j)^2 - a_1^2} + b_1) \sin(\omega_j t)\end{aligned}\quad (2.61)$$

where the cosine terms cancel, leaving only the sine component in the final expression.

Hence, the maximum phase error can be calculated as:

$$\Delta\phi_{max} = \sqrt{(2\pi A_j)^2 - a_1^2} + b_1 \quad (2.62)$$

Rearranging gives the maximum tolerable input jitter amplitude ($JTOL_{max}$) at a given jitter frequency:

$$A_{j,max} = JTOL_{max} = \sqrt{(\Delta\phi_{max} - b_1)^2 + a_1^2} \quad (2.63)$$

Substituting $\Delta\phi_{max} = 0.5 UI$ and using (2.48) and (2.49), gives:

$$JTOL_{max} = \frac{\sqrt{\omega_j^4 + [(16\beta_{prop})^2 - 2(16\alpha_{int})]\omega_j^2 + (16\alpha_{int})^2}}{2\omega_j^2} \quad (2.64)$$

This expression is consistent with the result reported in [28]. In the high jitter frequency limit, as $\omega_j \rightarrow \infty$, the dominant term is ω_j^4 , and:

$$JTOL_{\omega_j \rightarrow \infty} \approx \frac{\sqrt{\omega_j^4}}{2\omega_j^2} \approx 0.5 UI \quad (2.65)$$

In the low jitter frequency limit, as $\omega_j \rightarrow 0$, the dominant term becomes $(16\alpha_{int})^2$, leading to,

$$JTOL_{\omega_j \rightarrow 0} \approx \frac{\sqrt{256\alpha_{int}^2}}{2\omega_j^2} \approx \frac{8\alpha_{int}}{\omega_j^2} \approx b_1 \quad (2.66)$$

From Example 2.2 with $I_{cp,int} = 10 \mu A$ (stability factor $\xi = 1000$) and Example 2.3 with $I_{cp,int} = 100 \mu A$ ($\xi = 100$), Fig. 2.17 shows the corresponding simulated jitter

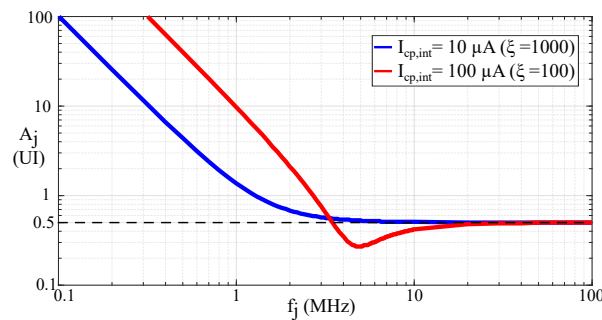


FIGURE 2.17: Simulated JTOL curves for different integral branch CP currents.

tolerance curves, assuming a maximum allowable phase error of $\Delta\phi_{max} = 0.5 \text{ UI}$. At low jitter frequencies, increasing the integral branch current enhances tolerance by making the loop more responsive to slower phase variations. However, this improvement comes at the expense of stability: a lower stability factor introduces jitter peaking near the corner frequency f_{jc} , resulting in a dip in the tolerance curve. At high jitter frequencies, the tolerance asymptotically approaches 0.5 UI in all cases, consistent with the slewing behavior predicted by the analytical model.

2.3.3 Jitter generation

Many sources contribute to the jitter generated by the CDR loop, including VCO phase noise, noise from the BBPD, ripple in the control voltages (V_{prop} & V_{int}), and disturbances from power supply and substrate noise [27]. When the Alexander PD operates within its linear range and no current is injected into the LF during long data runs, its impact on the control voltage ripple becomes negligible, leaving the VCO phase noise as the dominant source of jitter.

Fig. 2.18a shows the phase domain model used to quantify jitter generated intrinsically by the VCO, similar to the approach in [39]. When the BBPD operates within its linear region, defined by $\Delta\phi = \pm\phi_m$ (see Fig. 2.4b), its gain can be approximated as $K_{pd} = 1/\phi_m$. In this analysis, the input data to the PD is assumed to be free of phase deviation and jitter (i.e., $\phi_{in} = 0$). The phase noise of the VCO is also assumed to be sufficiently low such that the phase error remains within the linear range of the BBPD. The VCO phase noise, $\phi_{n,vco}$, is modeled as an additive phase noise component. The resulting closed-loop behavior of the PLL can be derived as follows.

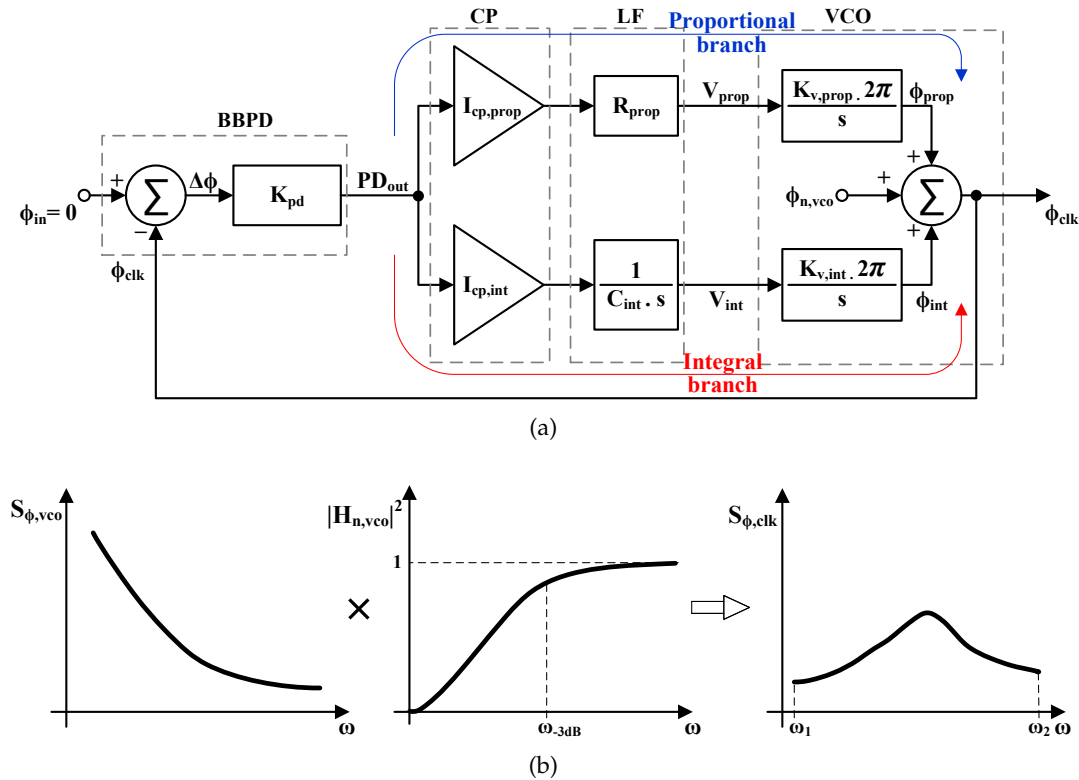


FIGURE 2.18: (a) Phase domain model of JGEN due to intrinsic VCO phase noise, and (b) the resulting phase noise shaping within the PLL.

For the analysis, the PLL is conceptually broken at the feedback path, and all quantities are expressed in the Laplace domain. The proportional and integral control voltages generated by the LF result from the CP currents driven by the BBPD output. These voltages can be expressed as:

$$V_{prop}(s) + V_{int}(s) = -\Phi_{clk}(s) K_{pd} \left(I_{cp,prop} R_{prop} + \frac{I_{cp,int}}{C_{int} s} \right) \quad (2.67)$$

where the BBPD output equals the phase error ($-\Phi_{clk}(s)$) scaled by gain (K_{pd}). The corresponding VCO phase contributions are:

$$\Phi_{prop}(s) + \Phi_{int}(s) = -\Phi_{clk}(s) K_{pd} \left(I_{cp,prop} R_{prop} \frac{K_{v,prop} 2\pi}{s} + \frac{I_{cp,int}}{C_{int} s} \frac{K_{v,int} 2\pi}{s} \right) \quad (2.68)$$

With β_{prop} and α_{int} from (2.13) and (2.14), this simplifies to:

$$\Phi_{prop}(s) + \Phi_{int}(s) = -\Phi_{clk}(s) K_{pd} \left(\beta_{prop} \frac{2\pi}{s} + \alpha_{int} \frac{2\pi}{s^2} \right) \quad (2.69)$$

The total excess clock phase of the VCO can then be written as:

$$\Phi_{clk}(s) = \Phi_{prop}(s) + \Phi_{int}(s) + \Phi_{n,vco}(s) \quad (2.70)$$

Substituting (2.69) into (2.70) gives the closed-loop transfer function:

$$H_{n,vco}(s) = \frac{\Phi_{clk}(s)}{\Phi_{n,vco}(s)} = \frac{s^2}{s^2 + 2\pi K_{pd} \beta_{prop} s + 2\pi K_{pd} \alpha_{int}} \quad (2.71)$$

This can be written in the standard second-order form [39]:

$$H_{n,vco}(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.72)$$

with natural frequency ω_n and damping factor ζ are:

$$\omega_n = \sqrt{2\pi K_{pd} \alpha_{int}} = \sqrt{\frac{2\pi \alpha_{int}}{\phi_m}} \quad (2.73)$$

$$\zeta = \frac{\pi K_{pd} \beta_{prop}}{\omega_n} = \beta_{prop} \sqrt{\frac{\pi}{2\alpha_{int} \phi_m}} \quad (2.74)$$

The magnitude of the transfer function in (2.72) is:

$$|H_{n,vco}(j\omega)| = \frac{\omega^2}{\sqrt{(\omega_n^2 - \omega^2)^2 + (2\zeta\omega_n \omega)^2}} \quad (2.75)$$

Setting this magnitude equal to $1/\sqrt{2}$ yields the -3 dB corner frequency of the high-pass response [39]:

$$\omega_{-3dB,HP} = \omega_n \sqrt{[2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}]} \quad (2.76)$$

Fig. 2.18b shows how the PLL shapes the free running VCO phase-noise Power Spectral Density (PSD) $S_{\phi,vco}(f)$ (in rad^2/Hz) through the transfer function ($H_{n,vco}(s)$),

resulting in the recovered clock phase noise spectrum. As shown, the PLL strongly suppresses low frequency VCO phase noise up to its -3dB bandwidth $\omega_{-3dB,HP}$, while high frequency components pass through largely unattenuated. The resulting output phase-noise PSD of the recovered clock can be written as:

$$S_{\phi,clk}(f) = |H_{n,vco}(j2\pi f)|^2 S_{\phi,vco}(f) \quad (2.77)$$

Expressed in logarithmic form (dBc/Hz)¹, this becomes:

$$L_{clk}(f) = L_{vco}(f) + 20 \log_{10} |H_{n,vco}(j2\pi f)| \quad (2.78)$$

The rms jitter of the recovered clock, integrated over a frequency range $[f_1, f_2]$, is:

$$\sigma_{rms}(f_1 - f_2) = \frac{1}{2\pi f_{clk}} \sqrt{\int_{f_1}^{f_2} S_{\phi,clk}(f) df} \quad (2.79)$$

From Example 2.2 with $I_{cp,int} = 10 \mu A$ (stability factor $\xi = 1000$) and Example 2.3 with $I_{cp,int} = 100 \mu A$ ($\xi = 100$), Fig. 2.19 shows the simulated phase transfer function ($H_{n,vco}$) for various BBPD gains, φ_m . As φ_m increases, the BBPD gain decreases, reducing the loop bandwidth $\omega_{-3dB,jgen}$ and thereby weakening suppression of low frequency VCO phase noise. Increasing the integral branch current $I_{cp,int}$ (i.e., lowering ξ) simultaneously decreases the damping factor and increases the natural frequency ω_n , producing a larger noise-peaking region near the loop bandwidth. Consequently, the worst-case jitter generation occurs when both the BBPD gain is low (large φ_m) and the stability factor is low (large $I_{cp,int}$).

In this section, the analysis focuses exclusively on jitter generation arising from the VCOs phase noise. Further analysis of jitter contributions from the CP, LF, and supply can be found in [39], which exhibits the same high-pass noise-shaping behavior.

¹If the VCO phase noise is originally specified as single side band phase noise ($L_{vco}(f)$) (dBc/Hz), it converts to linear PSD via $S_{\phi,vco}(f) = 2 \cdot 10^{L_{vco}(f)/10}$.

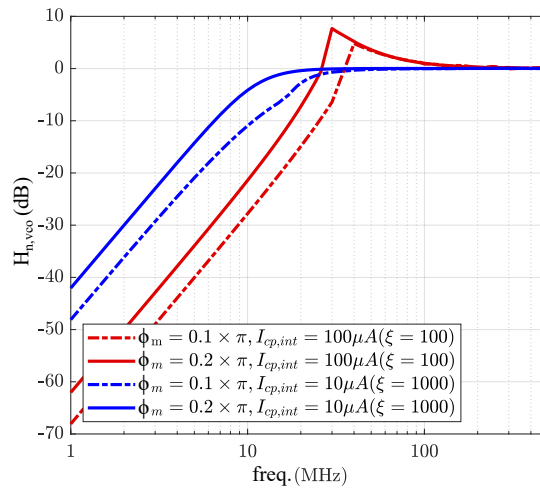


FIGURE 2.19: Simulated phase transfer function from the VCO phase noise to the recovered clock for different integral branch CP currents and BBPD gains.

2.4 Summary and conclusion

In this chapter, we compared two transition-based phase detectors, Hogge and Alexander. We selected the Alexander PD for its versatility and a higher PD gain with random data. Next, we introduced a bang-bang PLL modeling using a dual-LF with independently tunable proportional and integral branches. Our analysis, building on [15, 28, 31–35, 39], demonstrated that increasing the integral branch parameter $I_{cp,int}$ expands the inherent acquisition range $\delta_{acq,bb}$, but at the cost of reduced stability factor ξ .

Simulations revealed that a lower stability factor increases jitter peaking JP near the corner frequency f_{jc} , whose value is set by the input jitter amplitude A_j —making it difficult to tune the bandwidth as in the conventional PLLs. In JTOL, higher $I_{cp,int}$ improves tolerance at low jitter frequencies but leads to a dip (worsened tolerance) near f_{jc} . JGEN is also degraded with a lower stability factor and reduced BBPD gain, resulting in less effective VCO phase noise suppression. This increases the rms jitter of the recovered clock.

Overall, increasing the integral branch parameter improves acquisition range, but degrades jitter performance and introduces unwanted side effects. Additionally, the full VCO tuning range remains underutilized. These limitations motivate the exploration of enhanced acquisition techniques, which is the focus of the following chapter.

Chapter 3

Automatic Frequency Acquisition using BBPD

In CDR architectures using BBPD, the inherent frequency acquisition range $\delta f_{acq,bb}$ is typically narrow. This constraint results from the stringent jitter transfer and jitter tolerance requirements imposed by many wireline communication standards, which necessitate a low loop bandwidth and thus restrict acquisition range. Consequently, most practical PLL-based CDRs require additional acquisition circuitry to guarantee robust lock over wider frequency deviations δf . To address this challenge, numerous techniques have been reported in the literature.

3.1 State-of-the-art acquisition techniques

During power-up or extended idle periods, the input data rate (f_{bit}) may deviate significantly from VCO frequency (f_{clk}). If the data rate lies outside the acquisition range but still within the VCO sensitivity range, the VCO can respond to the frequency deviation; however, the control voltage (V_c) settles to an incorrect value (see Fig. 2.5). This condition results in acquisition failure and leads to the appearance of two different spectral tones in the recovered clock, as shown in Fig. 3.1a. Conversely, when the data rate remains within the acquisition range, the loop successfully locks to the input data rate. Consequently, the control voltage V_c converges to a valid operating point, and a single spectral tone appears in the recovered clock ($f_{clk} = f_{bit}$), as shown in Fig. 3.1b.

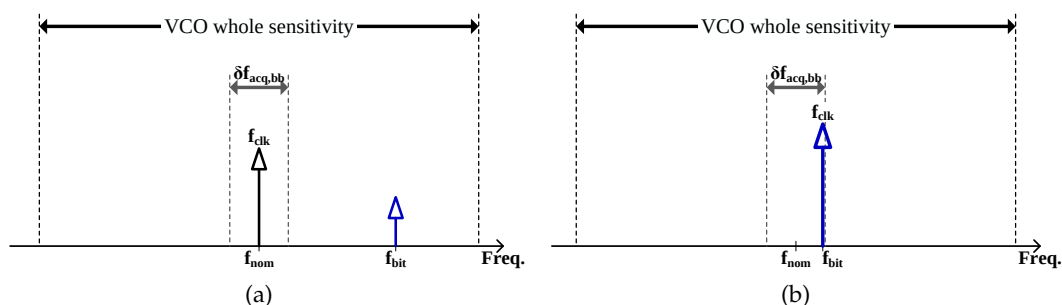


FIGURE 3.1: Recovered clock spectrum without frequency acquisition: (a) input data outside acquisition range—lock failure indicated by two tones, and (b) input data within acquisition range—loop locks, yielding a single tone.

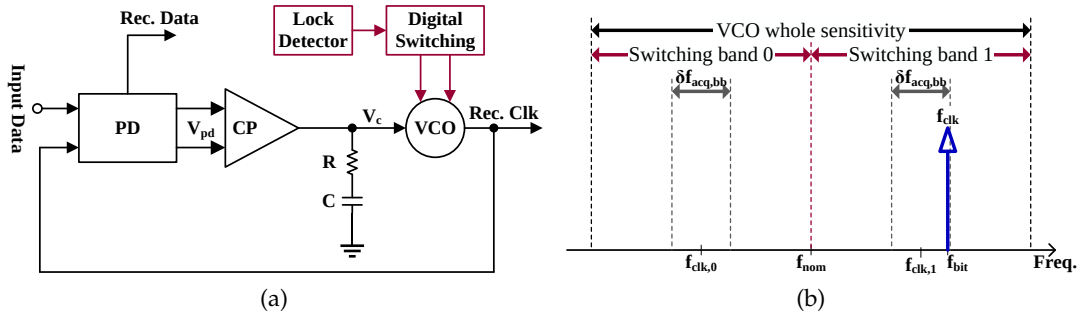


FIGURE 3.2: (a) CDR with digital VCO band switching; (b) Recovered clock spectrum showing successful acquisition in the second band.

An effective approach to extend the acquisition range is to digitally switch the VCO frequency bands using switched capacitor banks, as shown in Fig. 3.2a. In addition, integrating a Lock Detector (LD) can improve acquisition reliability and enable automation, but at the cost of increased power consumption. Fig. 3.2b shows the VCO spectrum when 1-bit resolution digital switching is implemented. The frequencies $f_{clk,0}$ and $f_{clk,1}$ correspond to the center frequencies of each digital switching band. In this configuration, the CDR successfully acquires lock in the second switching band, where it previously failed in Fig. 3.1a. Overlapping the switching bands ensures that the PLL acquisition range covers transitions between bands; however, the acquisition range itself cannot span the entire width of each band.

The dual-loop CDR architecture, as shown in Fig. 3.3a, integrates a PLL and a Frequency-Locked Loop (FLL), which contain a PD for phase alignment and a Frequency Detector (FD) for frequency acquisition, respectively [40]. In the event of a loss of lock, the FD generates a control voltage to steer the VCO frequency toward the input data rate. Once the frequency error falls within the acquisition range of the PLL, the PD takes control and aligns the clock with the incoming data. However, simultaneous operation of both loops leads to interaction, as the FD modulates the shared VCO control voltage (V_c), injecting phase noise and causing ripple on the recovered clock. During random data transmission, short-term spectral components near the nominal data rate can mislead the FLL, causing it to shift the clock frequency away from the input data and potentially resulting in lock loss or increased bit errors. To mitigate this, the bandwidth of the FLL is typically designed to be narrower than that of the PLL, thereby limiting the noise contribution of the FD.

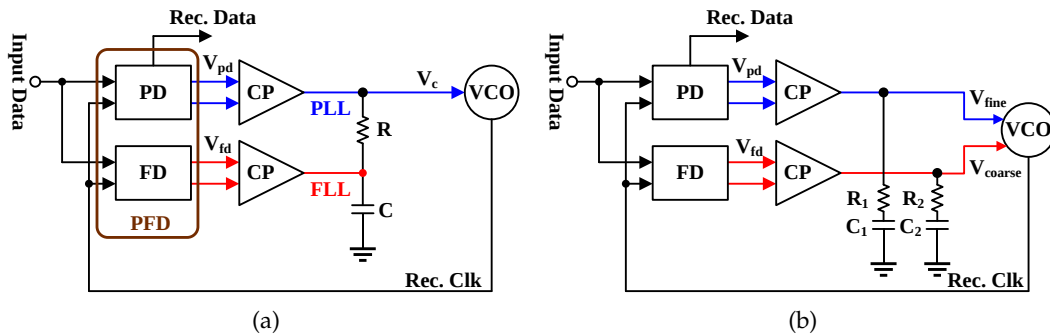


FIGURE 3.3: Frequency acquisition techniques in CDR architectures: (a) Dual-loop PLL/FLL, (b) Modified dual-loop with separate coarse/fine control.

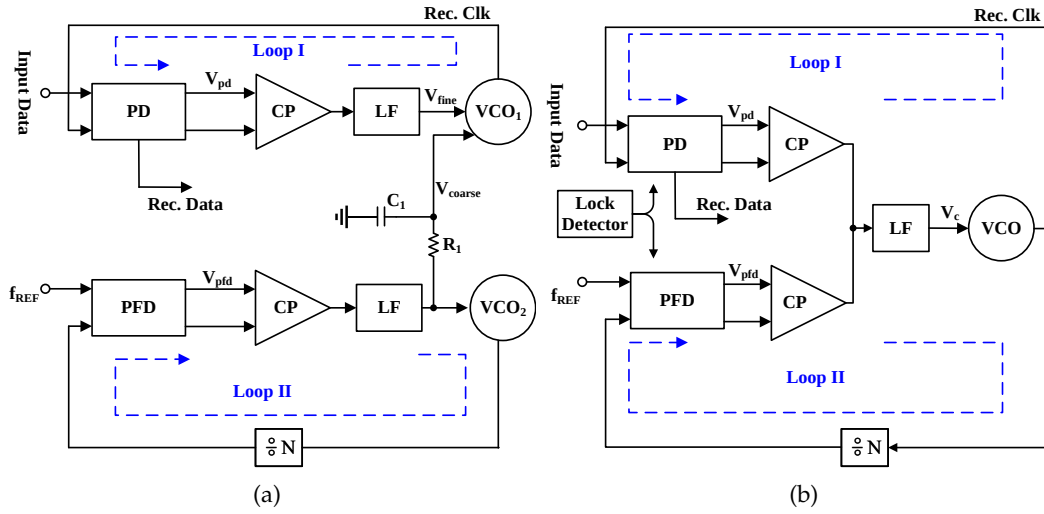


FIGURE 3.5: Frequency acquisition techniques in synchronous CDR architectures: (a) Dual-loop with phase frequency detector, and (b) modified with a single shared VCO.

and disable them as needed. However, this loop-switching mechanism can introduce ripple into the control voltage, which can degrade performance.

Different acquisition architectures can be adapted to suit specific system requirements. In this thesis, we propose a novel and simplified architecture that effectively addresses the limitations discussed above.

3.2 Novel acquisition technique

Our proposed automatic frequency acquisition architecture [22], shown in Fig. 3.6a introduces a permanently modulated offset current within the integral branch of the PLL. In another proposal of ours [24], shown in Fig. 3.6b, offset voltage modulation can be applied externally to the VCO (i.e., outside the PLL). In both cases, the VCO center frequency is deliberately detuned during PLL operation to steer the loop toward frequency acquisition. These methods simplify the design by eliminating the need for additional complex circuitry and extend the frequency acquisition capability beyond the inherent acquisition range of the BBCDR.

3.2.1 Varactor voltage modulation applied externally to the VCO

The second-order bang-bang PLL of Fig. 3.6b is modeled for frequency acquisition with an offset voltage V_{os} as shown in Fig. 3.7, using the framework of Fig. 2.6b. Since the analysis focuses on the frequency deviation $\delta f(t)$, the model omits the nominal center frequency f_{nom} and the jitter $\phi_j(t)$.

The instantaneous VCO excess frequency can be expressed as:

$$f_{clk,ex}(t) = f_{prop}(t) + f_{int}(t) + f_{os}(t) \quad (3.1)$$

where $f_{prop}(t)$ is the bang-bang frequency change, switching between $\pm f_{prop}$. It is tightly bounded (within $\pm 0.1\%$ of f_{nom}), as discussed in Section 2.2.1, and its time-average value can be approximated as zero in both acquisition and locked states. The VCO offset frequency $f_{os}(t)$, arising from the PVT variations relative to its center

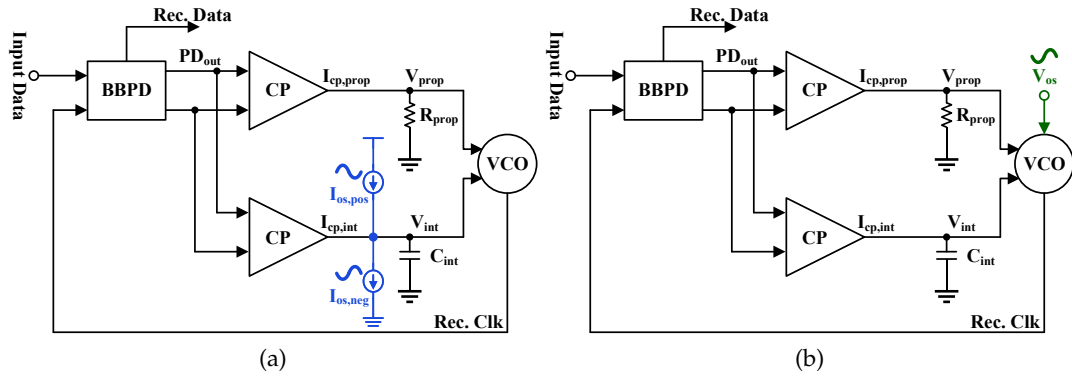


FIGURE 3.6: Novel BBCDR architecture with static or modulated: (a) offset current within the integral branch of the PLL (b) offset voltage outside the PLL.

frequency, can be manually adjusted through V_{os} . The integral term $f_{int}(t)$ then tracks both the input frequency deviation $\delta f(t)$ and the offset frequency $f_{os}(t)$. This relationship can be expressed as:

$$f_{int}(t) \cong \delta f(t) - f_{os}(t) \quad (3.2)$$

$$V_{int}(t) K_{v,int} \cong \delta f(t) - V_{os}(t) K_{v,os} \quad (3.3)$$

where $K_{v,int}$ and $K_{v,os}$ denote the VCO sensitivities to the integral control voltage $V_{int}(t)$ and offset voltage $V_{os}(t)$, respectively.

If no offset voltage is applied and the input frequency deviation $\delta f(t)$ is within the inherent acquisition range $\delta f_{acq,bb}$ (defined by (2.32)), the integral branch control voltage $V_{int}(t)$ adjusts to maintain lock with $\delta f(t)$.

When a static offset voltage ($V_{os,DC}$) is applied, the integral branch generates a compensating frequency contribution in the opposite direction, thereby maintaining lock to $\delta f(t)$. If the static offset shifts the VCO center frequency beyond the acquisition range, the acquisition range itself shifts accordingly, allowing the CDR to lock around the new center frequency.

Example 3.1 (Acquisition range shift using static offset voltage). *Using PLL parameters similar to Example 2.2, a VCO with a total tuning range of ± 1 GHz around a center frequency of 25 GHz is considered. This range is equally divided between the integral branch and the*

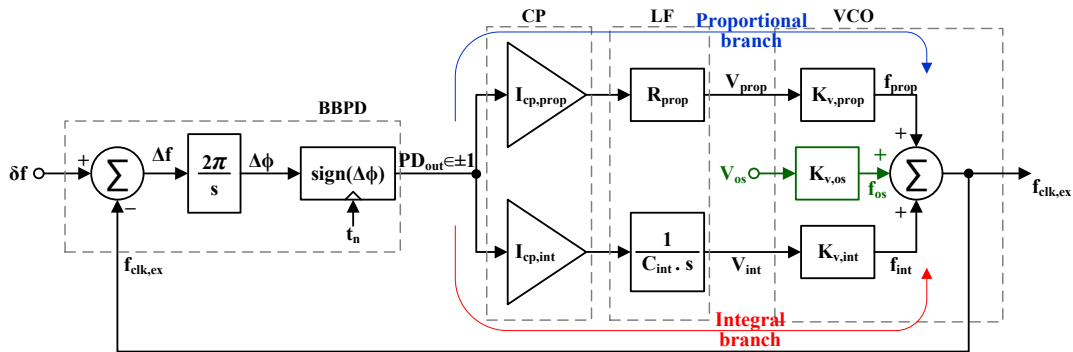


FIGURE 3.7: Second-order Bang-Bang PLL nonlinear frequency-domain model with frequency acquisition using offset voltage.

offset voltage, with each providing a tuning range of ± 500 MHz. Although the control voltage range is ± 1 V, the tuning range is limited to ± 500 mV. Thus, the sensitivities are $K_{v,os} = K_{v,int} = 1000$ MHz/V. For $I_{cp,int} = 10$ μ A, the inherent acquisition range is limited to $\delta f_{acq,bb} \approx \pm 32$ MHz. The nominal data rate is close to the VCO center frequency, with deviations captured by $\delta f(t)$. When a static offset voltage of $V_{os,DC} = +200$ mV is applied, the VCO center frequency shifts by $+200$ MHz, and the acquisition range moves to $\approx +200$ MHz ± 32 MHz around this new center frequency.

Fig. 3.8a shows the simulated BBCDR response to a frequency deviation of $\delta f = +30$ MHz with no static offset voltage applied. The input data is enabled at 5 μ s, while the system operates as a free-running VCO prior to this point. The integral branch then adjusts its control voltage to acquire lock with δf .

Fig. 3.8b shows the simulated BBCDR response to a frequency deviation of $\delta f = +170$ MHz with static offset voltage of $V_{os,DC} = +200$ mV is applied. This frequency deviation now falls within the shifted acquisition range, allowing the PLL to acquire lock. In this case, the integral branch generates a compensating voltage (and corresponding frequency contribution) in opposition to the applied offset, thereby maintaining lock to δf .

The offset voltage can be modulated with amplitude $V_{os,p}$ and frequency $f_{os,m}$ and is expressed as:

$$V_{os}(t) = V_{os,p} \cos(2\pi f_{os,m} t) \quad (3.4)$$

This modulation results in a peak-to-peak sweep of the VCO frequency from its center frequency, expressed as:

$$f_{vos,pp} = \pm V_{os,p} K_{v,os} \quad (3.5)$$

The derivative of (3.4) gives the rate at which the offset voltage changes and can be expressed as follows:

$$\frac{dV_{os}(t)}{dt} = -2\pi V_{os,p} f_{os,m} \sin(2\pi f_{os,m} t) \quad (3.6)$$

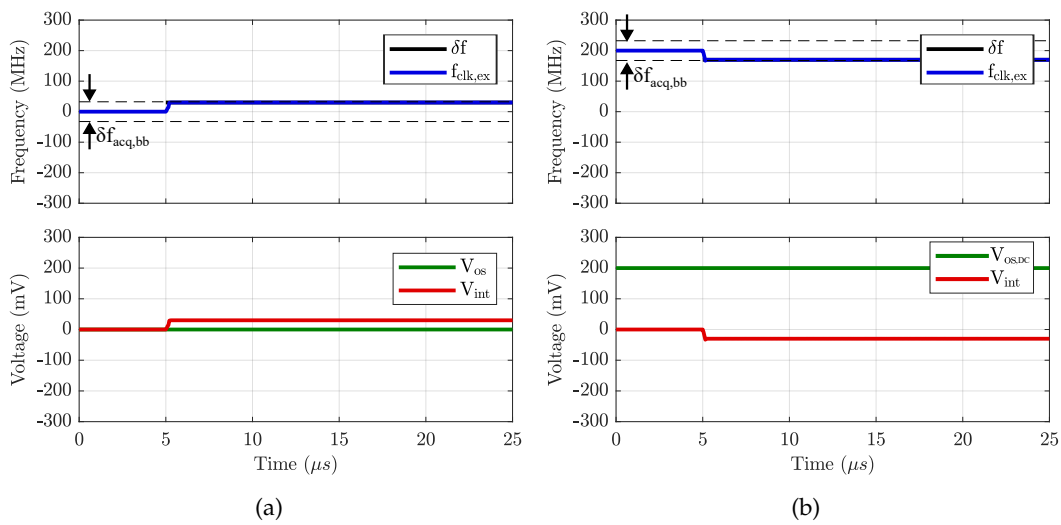


FIGURE 3.8: Simulated BBCDRs response to: (a) $\delta f = +30$ MHz with no static offset voltage, and (b) $\delta f = +170$ MHz with a static offset voltage applied shifting the acquisition range. (Input data enabled at 5 μ s)

Conversely, the integral control voltage ramps up or down with a slope of $I_{cp,int}/C_{int}$. Comparing this to the maximum slope of the offset voltage modulation in (3.6) gives the following condition, which ensures that the loop can efficiently track the modulation without losing lock:

$$|2\pi V_{os,p} f_{os,m} K_{v,os}| \leq \left| \frac{I_{cp,int} K_{v,int}}{C_{int}} \right| \quad (3.7)$$

Note: The sensitivity coefficients, $K_{v,os}$ and $K_{v,int}$ are included to convert control voltage changes into frequency changes. This enables a direct comparison of the modulation rate and the PLLs tracking capability. With offset voltage modulation, the extended acquisition range can be expressed as:

$$\begin{aligned} \delta f_{acq,vos} &\leq f_{vos,pp} + \delta f_{acq,bb} \\ &\leq \pm \left(V_{os,p} K_{v,os} + I_{cp,prop} R_{prop} K_{v,prop} + \sqrt{\frac{I_{cp,int}}{C_{int}}} K_{v,int} \right) \end{aligned} \quad (3.8)$$

Under the condition in (3.7), the peak-to-peak VCO frequency modulation $f_{vos,pp}$ can be set beyond the inherent acquisition range $\delta f_{acq,bb}$ (defined by (2.32)), thereby extending the total acquisition range of the BBCDR to $\delta f_{acq,vos}$.

For successful acquisition, the bang-bang PLL must lock to the data rate within a single period of the offset modulation, so the acquisition time is given by:

$$t_{acq,os} \leq \frac{1}{f_{os,m}} \quad (3.9)$$

Notably, this acquisition time is independent of the intrinsic BBCDR acquisition time $t_{acq,bb}$, (defined in 2.30), which depends on both the frequency deviation δf and the stability factor ξ . In contrast, $t_{acq,os}$ is determined solely by the modulated offset frequency $f_{os,m}$.

Example 3.2 (Acquisition range extension using modulated offset voltage). *Building on Example 3.1, the offset voltage is modulated with an amplitude of $V_{os,p} = 200$ mV and a frequency of $f_{os,m} = 200$ kHz, resulting in a free-running VCO frequency sweep of $f_{vos,pp} = \pm 200$ MHz around the center frequency, as shown in Fig. 3.9. With inherent acquisition range, only frequency deviations upto $\delta f = 32$ MHz can be acquired, corresponding to an acquisition time of $t_{acq,bb} \approx 108$ ns. In contrast, offset modulation extends the acquisition range to $\delta f_{acq,vos} \approx \pm 232$ MHz, with an acquisition time of $t_{acq,os} \leq 5$ μ s.*

When the input data is enabled at 5 μ s and the positive frequency deviation of $\delta f = +230$ MHz lies outside the inherent acquisition range of the BBCDR, but within the extended acquisition range enabled by the offset modulation, the PLL successfully acquires lock, as shown in Fig. 3.9a. The PLL actively searches for the frequency deviation and minimizes the phase error. Once δf falls within the acquisition range, the proportional branch becomes dominant and locks the clock to the input data rate. In the steady state, the integral control voltage modulates in opposition to the offset voltage modulation, thereby ensuring that the sum of f_{os} and f_{int} achieves the required frequency deviation, as described in (3.3). Similarly, Fig. 3.9b shows the response to a negative frequency deviation of $\delta f = -230$ MHz. For these examples, we observe that the integral branch control voltage V_{int} operates near the edge of its tuning range. Further increasing the acquisition range using $f_{vos,pp}$ and increasing the input frequency deviation pushes the integral control voltage beyond its linear

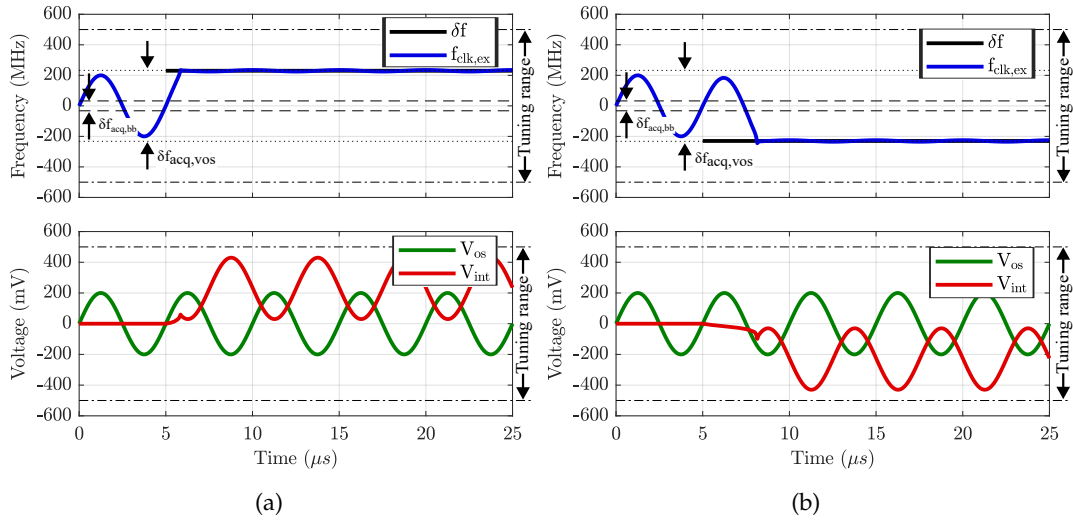


FIGURE 3.9: Simulated BBDRs response with offset voltage modulation ($V_{os,p} = 200$ mV and $f_{os,m} = 200$ kHz) and frequency deviation beyond inherent acquisition range: (a) positive frequency deviation ($\delta f = +230$ MHz); (b) negative frequency deviation ($\delta f = -230$ MHz). (Input data enabled at $5 \mu s$)

range. Therefore, the upper bound of the frequency acquisition can be expressed as:

$$\delta f_{acq,vos,max} \leq 3 \times (f_{vos,pp} + \delta f_{acq,bb}) \leq f_{int,lin} \quad (3.10)$$

where $f_{int,lin}$ represents the linear tuning range of the VCO with respect to the integral control voltage. This limit is reached when the integral control voltage hits the boundary of its linear tuning range. Example 3.5 shows the practical effect of this limit.

Example 3.3 (Acquisition range upper bound due to offset voltage modulation slope). In Example 3.2, if the modulating offset voltage amplitude is fixed at $V_{os,p} = 200$ mV, the maximum modulated offset frequency can be calculated from (3.7) as $f_{os,m,max} \approx 400$ kHz. Conversely, if $f_{os,m}$ is fixed at 200 kHz, the maximum modulated offset amplitude is $V_{os,p,max} \approx 400$ mV.

Fig. 3.10a shows the results of increasing the offset slope by raising $f_{os,m}$. When the data is enabled at $5 \mu s$, the frequency deviation of $\delta f = 20$ MHz is within the inherent acquisition range of the BBDR. For $V_{os,p} = 200$ mV and $f_{os,m} = 325$ kHz, the PLL successfully acquires the lock. However, when $f_{os,m}$ is increased to 425 kHz (beyond $f_{os,m,max} \approx 400$ kHz), acquisition fails. Similarly, Fig. 3.10b shows the effect of increasing $V_{os,p}$ at a fixed $f_{os,m} = 200$ kHz. For $V_{os,p} = 350$ mV, the PLL acquires lock, with an extended acquisition range of $\delta f_{acq,vos} = \pm 382$ MHz. When $V_{os,p}$ is increased to 450 mV, the acquisition range extends to ± 482 MHz, but acquisition fails as this exceeds $V_{os,p,max} \approx 400$ mV.

Example 3.4 (Acquisition range upper bound due to offset control voltage tuning range). If the peak-to-peak modulation of the VCO frequency ($f_{vos,pp}$), exceeds the tuning range set by the offset control voltage, (3.7) is no longer invalid. As PLL cannot acquire frequency deviations beyond the tuning range. Thus, VCOs tuning range defines the upper bound of the extended acquisition range.

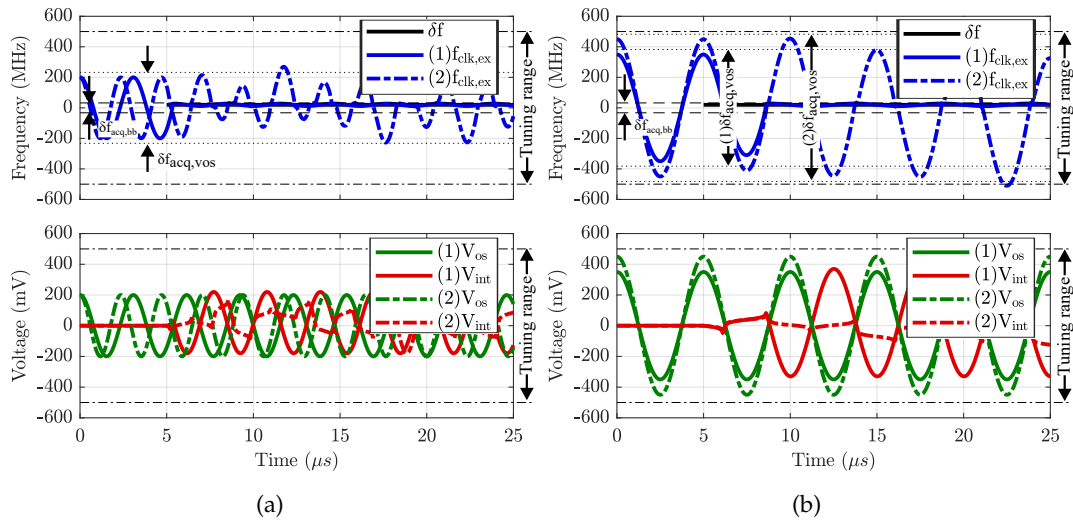


FIGURE 3.10: Simulated BBCDRs response with frequency deviation of $\delta f = +20$ MHz: (a) varying modulated offset voltage frequencies ((1) $f_{os,m} = 325$ kHz and (2) $f_{os,m} = 425$ kHz); (b) varying modulated offset voltage amplitudes ((1) $V_{os,p} = 350$ mV and (2) $V_{os,p} = 450$ mV). (Input data enabled at 5 μs)

Continuing with Example 3.2, we set $f_{os,m} = 100$ kHz and increase $V_{os,p}$ to 550 mV, resulting in $f_{vos,pp} = \pm 550$ MHz, which exceeds the tuning range of the VCO (± 500 MHz). Fig. 3.11a shows the result, when the data is enabled at 10 μs , the frequency deviation of $\delta f = 20$ MHz lies within the inherent acquisition range of the BBCDR. The PLL acquires lock and remains locked as long as the offset control voltage stays within the linear range. However, at time t_1 , the offset voltage reaches the end of the tuning range, and the integral branch can no longer track the offset voltage, causing the PLL to lose lock.

Example 3.5 (Acquisition range upper bound due to integral control voltage tuning range). Building on Example 3.2, the offset voltage is modulated with an amplitude of $V_{os,p} = 350$ mV and a frequency of $f_{os,m} = 200$ kHz, resulting in a free-running VCO frequency sweep of $f_{vos,pp} = \pm 350$ MHz around the center frequency. The acquisition range is $\delta f_{acq,vos} \approx \pm 382$ MHz, and the linearity range is $f_{int,lin} = \pm 500$ MHz. This violates the upper bound defined in (3.10). Accordingly, this bound restricts the maximum frequency acquisition range $\delta f_{acq,vos,max}$ to approximately one third of $f_{int,lin}$. In this case, around 166 MHz.

Fig. 3.11b shows the simulated response for different frequency deviations. When the input data is enable at 5 μs and the frequency deviation is $\delta f = 125$ MHz, the PLL acquires lock successfully. As the frequency deviation increases to $\delta f = 175$ MHz, the integral branch control voltage is pushed beyond the tuning range at time t_2 , causing the PLL to lose lock.

In other words, the maximum extension of the frequency acquisition range $\delta f_{acq,vos,max}$ using externally applied offset voltage modulation (i.e., outside the PLL) is approximately one third of the VCOs tuning range ($f_{int,lin}$) with respect to the integral branch control voltage. This condition, defined in (3.10), can be achieved by controlling either the offset voltage amplitude $V_{os,p}$ or the VCO sensitivity $k_{v,os}$. Alternatively, this upper bound on frequency acquisition can be overcome by implementing offset current modulation within the integral branch.

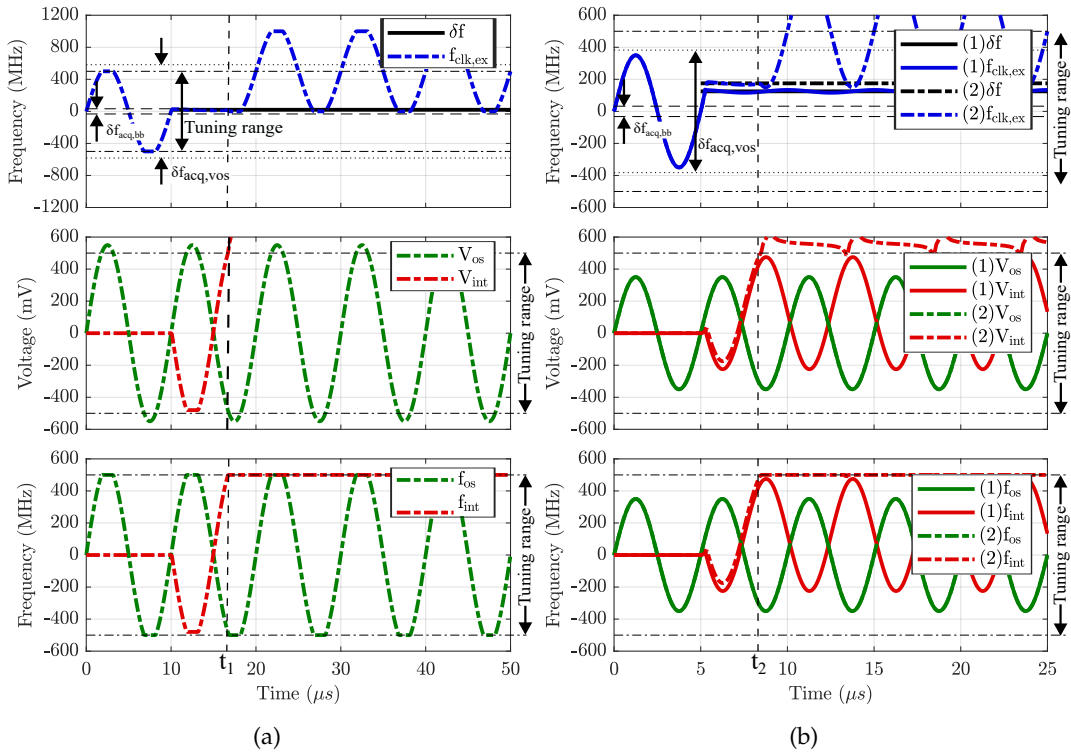


FIGURE 3.11: Simulated BBPDRs response with: (a) frequency deviation of $\delta f = +20$ MHz and $V_{os,p} = 550$ mV beyond VCO tuning linearity range (Input data enabled at $10 \mu\text{s}$); (b) varying frequency deviations, (1) $\delta f = 125$ MHz and (2) $\delta f = 175$ MHz. (Input data enabled at $5 \mu\text{s}$)

3.2.2 Offset current modulation applied within the integral branch

Using a current source, the same principle can be applied to modulate the integral control voltage as shown in Fig. 3.6a. A simple CP can be constructed using switches and Positive Channel Metal Oxide Semiconductor (PMOS) and Negative Channel Metal Oxide Semiconductor (NMOS) transistors as seen in Fig. 3.12. The output impedances of the transistors P_1 (PMOS) and N_1 (NMOS) form a resistive divider ($R_{out,int}$) and are always different due to the operating point, PVT, and PMOS vs. NMOS device sizing. Therefore the integral control voltage would tend to charge the capacitor towards VCC or discharge it towards VEE over time, depending on the device parameters and operating conditions of P_1 and N_1 , inevitably leading to CP leakage. The offset currents, $I_{os,pos}$ and $I_{os,neg}$ can be used to compensate for this leakage effect.

Alternatively, the offset currents can also be used to control the DC value of V_{int} , thereby setting the VCO center frequency. The VCO control voltage due to the integral branch based on (2.10), can be rewritten as:

$$V_{iL}(t_n) = \int_0^{t_n} V_{pd}(\tau) \frac{I_{cp,int}}{C_{int}} d\tau + V_{os}(t) + V_{int}(0) \quad (3.11)$$

where the first term can be denoted as V_{int} . The corresponding offset voltage $V_{os}(t)$ can be expressed as:

$$V_{os}(t) = I_{os}(t) R_{out,int} \quad (3.12)$$

shifted to $\approx +200 \text{ MHz} \pm 32 \text{ MHz}$.

Fig. 3.14a shows the simulated BBCDR response to a frequency deviation of $\delta f = +230 \text{ MHz}$ with a positive static offset current applied. This frequency deviation now falls within the shifted acquisition range, allowing the PLL to acquire lock. The input data is enable at $5 \mu\text{s}$. This activated the integral branch CP current $I_{cp,int}$, which toggles continuously due to the operation of BBPD. As a result, the circuit compensates for both the offset current $I_{os,DC}$ and the frequency deviation δf . The corresponding voltages V_{int} , $V_{os,DC}$ and V_{iL} further illustrate this behavior.

Similar to the offset voltage modulation, the offset current can be modulated with amplitude $I_{os,p}$ and frequency $f_{os,m}$, as described by:

$$I_{os}(t) = I_{os,p} \cos(2\pi f_{os,m} t) \quad (3.15)$$

This modulation results in a peak-to-peak sweep of the VCO frequency from its center frequency, given by:

$$f_{ios,pp} = \pm I_{os,p} R_{out,int} K_{v,int} \quad (3.16)$$

Substituting (3.15) and (3.12) into (3.7) gives us the relationship of the offset current to the integral current for which the loop will track efficiently:

$$|2\pi I_{os,p} R_{out,int} f_{os,m}| \leq \frac{I_{cp,int}}{C_{int}} \quad (3.17)$$

Note: Since the modulation occurs in the integral branch, the sensitivity coefficient

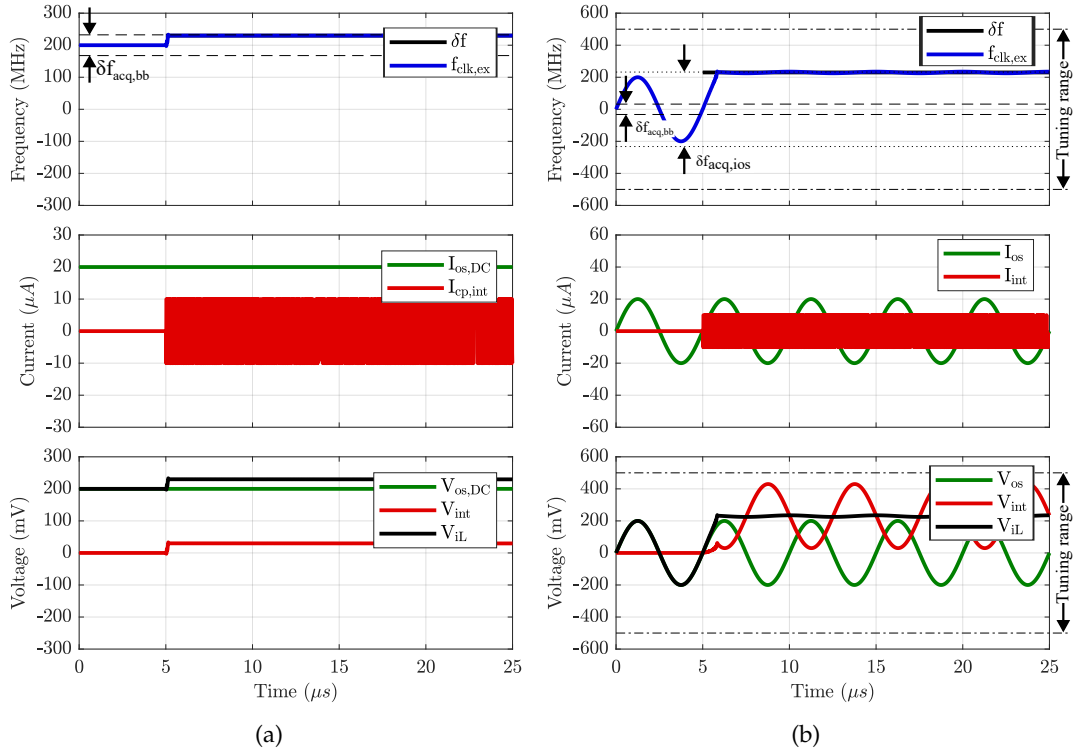


FIGURE 3.14: Simulated BBCDRs response to $\delta f = +230 \text{ MHz}$: (a) with a static offset current applied shifting the acquisition range, and (b) with modulated offset current ($I_{os,p} = 20 \mu\text{A}$ and $f_{os,m} = 200 \text{ kHz}$). (Input data enabled at $5 \mu\text{s}$)

$K_{v,int}$ is shared. This allows for a direct comparison between the modulation rate and the PLLs tracking capability.

The extended acquisition range with the offset current modulation in the integral branch can be expressed as:

$$\begin{aligned} \delta f_{acq,ios} &\leq f_{ios,pp} + \delta f_{acq,bb} \\ &\leq \pm \left(I_{os,p} R_{out,int} K_{v,int} + I_{cp,prop} R_{prop} K_{v,prop} + \sqrt{\frac{I_{cp,int}}{C_{int}}} K_{v,int} \right) \end{aligned} \quad (3.18)$$

Under the constraint in (3.17), the peak-to-peak offset VCO frequency modulation $f_{ios,pp}$ can be set beyond the inherent acquisition range $\delta f_{acq,bb}$ (defined by (2.32)), thereby extending the total acquisition range of the BBCDR to $\delta f_{acq,ios}$.

For successful acquisition, the PLL must lock to the data rate within a single period of the offset current modulation. Thus, the acquisition time remains as defined in (3.9).

Example 3.7 (Acquisition range extension using modulated offset current). *Building on Example 3.6, the offset current is modulated with an amplitude of $I_{os,p} = 20 \mu\text{A}$ and a frequency of $f_{os,m} = 200 \text{ kHz}$, resulting in a free-running VCO frequency sweep of $f_{ios,pp} = \pm 200 \text{ MHz}$ around the center frequency, as shown in Fig. 3.14b. With inherent acquisition range, only frequency deviations upto $\delta f = 32 \text{ MHz}$ can be acquired, corresponding to an acquisition time of $t_{acq,bb} \approx 108 \text{ ns}$. In contrast, offset modulation extends the acquisition range to $\delta f_{acq,ios} \approx \pm 232 \text{ MHz}$, with an acquisition time of $t_{acq,os} \leq 5 \mu\text{s}$.*

When the input data is enabled at $5 \mu\text{s}$ and the positive frequency deviation of $\delta f = +230 \text{ MHz}$ lies outside the inherent acquisition range of the BBCDR, but within the extended acquisition range enabled by the offset modulation, the PLL successfully acquires lock, as shown in Fig. 3.14b. The integral branch CP current $I_{cp,int}$, toggles continuously due to the operation of BBPD. As stated earlier, the circuit compensates for both the offset current I_{os} and the frequency deviation δf . The corresponding voltages V_{int} , V_{os} and V_{iL} further illustrate this behavior.

We also observe that, although V_{int} approaches the edge of the tuning range of the VCO, the control voltage V_{iL} remains within this range. As a result, frequency deviations near the VCO tuning limit caused by the integral branch can still be reliably acquired. Therefore, the upper bound given for the modulated offset voltage in (3.10) can be rewritten for the case of modulated offset current as:

$$\delta f_{acq,ios,max} \leq (f_{ios,pp} + \delta f_{acq,bb}) \leq f_{int,lin} \quad (3.19)$$

The practical implications of this condition is demonstrated in Example 3.10.

Example 3.8 (Acquisition range upper bound due to offset current modulation slope). *In Example 3.7, if the modulating offset current amplitude is fixed at $I_{os,p} = 20 \mu\text{A}$, the maximum modulated offset frequency can be calculated from (3.17) as $f_{os,m,max} \approx 400 \text{ kHz}$. Conversely, if $f_{os,m}$ is fixed at 200 kHz , the maximum modulated offset current amplitude is $I_{os,p,max} \approx 40 \mu\text{A}$.*

Fig. 3.15a shows the results of increasing the offset slope by raising $f_{os,m}$. The input data is enabled at $5 \mu\text{s}$, with a frequency deviation of $\delta f = 50 \text{ MHz}$. For $I_{os,p} = 20 \mu\text{A}$ and $f_{os,m} = 325 \text{ kHz}$, the PLL successfully acquires the lock. However, when $f_{os,m}$ is increased to 425 kHz (beyond $f_{os,m,max} \approx 400 \text{ kHz}$), acquisition fails. Similarly, Fig. 3.15b shows the results of increasing the offset slope by raising $I_{os,p}$.

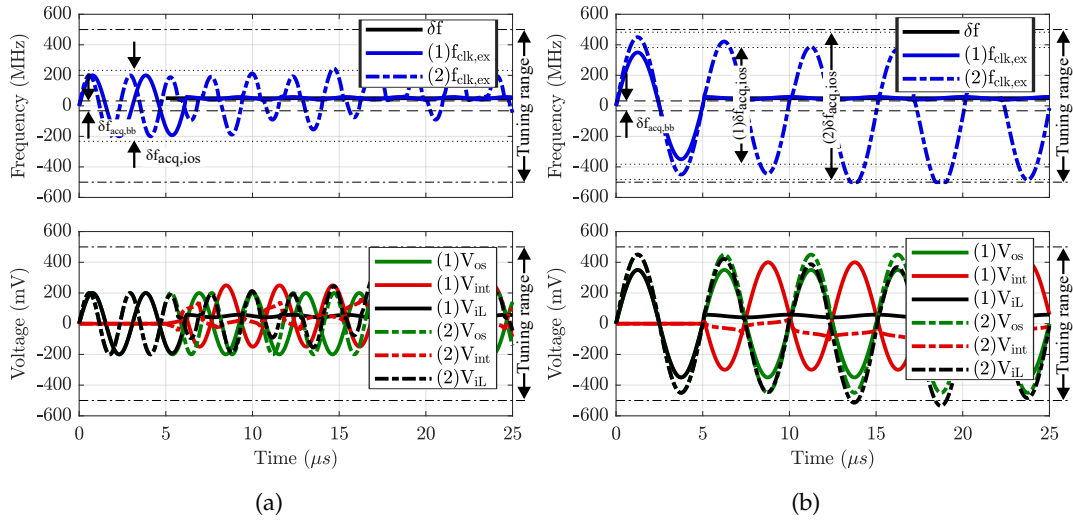


FIGURE 3.15: Simulated BBBCDRs response with frequency deviation of $\delta f = +50$ MHz: (a) varying modulated offset current frequencies ((1) $f_{os,m} = 325$ kHz and (2) $f_{os,m} = 425$ kHz); (b) varying modulated offset current amplitudes ((1) $I_{os,p} = 35$ μ A and (2) $I_{os,p} = 45$ μ A). (Input data enabled at 5 μ s)

For $f_{os,m} = 200$ kHz and $I_{os,p} = 35$ μ A, the PLL successfully acquires lock, with an extended acquisition range of $\delta f_{acq,ios} = \pm 382$ MHz. As $I_{os,p}$ is increased to 45 μ A, the acquisition range extends to $\delta f_{acq,ios} = \pm 482$ MHz; however, since this exceeds $I_{os,p,max} \approx 40$ μ A, acquisition fails.

Example 3.9 (Modulating beyond VCO tuning range). If the peak-to-peak modulation of the VCO frequency ($f_{ios,pp}$) exceeds the tuning range set by the offset control current, but the frequency deviation δf remains within the linear tuning range $f_{int,lin}$, the PLL can still successfully acquire the data rate. Therefore, modulating the VCO frequency beyond its linear range does not extend the acquisition range or affect the PLL dynamics.

Continuing with Example 3.7, we set $f_{os,m} = 100$ kHz and increase $I_{os,p}$ to 55 μ A, resulting in $f_{ios,pp} = \pm 550$ MHz, which exceeds the tuning range of the VCO (± 500 MHz). Fig. 3.16a shows the result, when the data is enabled at 10 μ s, with the frequency deviation of $\delta f = 50$ MHz. The PLL acquires lock and remains locked as long as the offset control voltage V_{iL} stays within the tuning range.

Example 3.10 (Acquisition range extension close to integral control voltage limits). Building on Example 3.7, the offset current is modulated with an amplitude of $I_{os,p} = 45$ μ A and a frequency of $f_{os,m} = 100$ kHz, resulting in a free-running VCO frequency sweep of $f_{ios,pp} = \pm 450$ MHz around the center frequency. The acquisition range is $\delta f_{acq,ios} \approx \pm 482$ MHz, and the linear tuning range is $f_{int,lin} = \pm 500$ MHz. This does not violate the upper bound defined in (3.19). Thus, the maximum frequency deviation δf of approximately 482 MHz can be tracked successfully.

Fig. 3.16b shows the simulated BBBCDR response for a frequency deviation of $\delta f = +480$ MHz. When the input data is enable at 10 μ s, the PLL successfully acquires lock. Although the control voltages V_{int} and V_{os} appear to exceed the linear tuning range of the VCO (± 500 mV in this case), these are virtual values. In practice, the respective currents $I_{cp,int}$ and I_{os} are updated or tracked such that the final control voltage V_{iL} supplied to the VCO remains within the linear range.

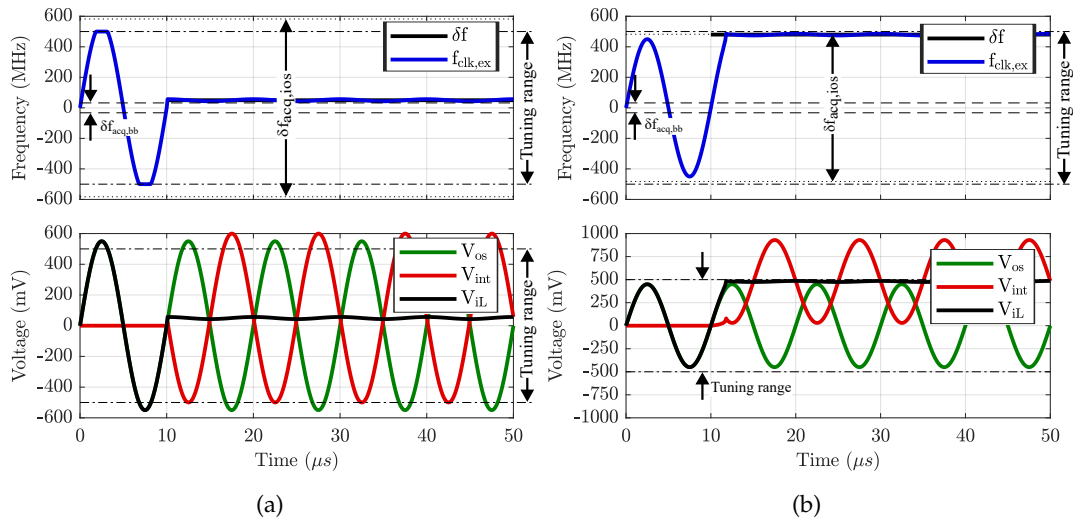


FIGURE 3.16: Simulated BBCDRs response with $f_{os,m} = 100$ kHz: (a) frequency deviation of $\delta f = +50$ MHz and $I_{os,p} = 55$ μ A beyond VCO tuning linearity range; (b) frequency deviation of $\delta f = +480$ MHz and $I_{os,p} = 45$ μ A. (Input data enabled at 10 μ s)

With varactor voltage modulation (i.e., applied outside the PLL), the maximum extended acquisition range is limited to one-third of the VCOs linear tuning range ($f_{int,lin}$). In contrast, offset current modulation within the integral branch utilizes the full VCO linear tuning range, making it a more effective approach. Another important observation is that the bang-bang PLL models in Fig. 3.7 and Fig. 3.13 closely resemble the phase-domain model used for jitter generation in Fig. 2.18a. This similarity indicates that offset modulation of the VCO center frequency is suppressed by the PLL dynamics. As the modulation frequency $f_{os,m}$ decreases, the PLL suppresses the modulation more effectively (see Fig. 2.19), but at the cost of increased acquisition time, as defined in (3.9). The next subsection discusses the impact of modulation on the phase noise of the recovered clock.

3.2.3 Spectrum of the recovered clock in steady state

In the steady state, the recovered clock signal from (2.3) with a permanently applied offset modulation of frequency $f_{os,m}$ and (PLL-suppressed) modulation amplitude A_{os} , can be expressed as:

$$V_{clk}(t) = A_{clk} \sin(2\pi f_{bit} t + A_{os} \sin(2\pi f_{os,m} t)) \quad (3.20)$$

Using the Jacobi-Anger expansion, the phase-modulated signal can be rewritten as:

$$V_{clk}(t) = A_{clk} \sum_{n=-\infty}^{n=\infty} J_n(A_{os}) \sin(2\pi (f_{bit} + n f_{os,m}) t) \quad (3.21)$$

where, $J_n(A_{os})$ are the Bessel functions of the first kind of order n . The resulting spectrum exhibits sidebands at $f_{bit} \pm n f_{os,m}$, with amplitudes proportional to $J_n(A_{os})$.

Fig. 3.17a and Fig. 3.17b show the recovered clock signal spectrum when a static positive or negative offset is applied, respectively, to shift the acquisition range. These results correspond to Examples 3.1 and 3.6. When the acquisition range is extended using permanently modulated offset, the steady-state spectrum of the recovered

clock is shown in Fig. 3.17c. As discussed earlier, the sidebands resulting from offset modulation are initially suppressed by the PLL, and higher-order sidebands are further reduced according to the Bessel function amplitudes.

During steady state, when sinusoidal jitter is applied to the input data, (3.21) can be adapted by substituting A_{os} with the jitter amplitude A_j (in UI) and $f_{os,m}$ with the jitter frequency f_j . Unlike offset modulation, input jitter at low frequencies is transferred through the loop, as shown in Fig. 2.15a. Notably, when the jitter amplitude exceeds 0.5 UI_{pp} , A_j approaches 1.57, causing $J_1(A_j) = 0.567$ to surpass $J_0(A_j) = 0.472$. This means the spectral component at the data rate becomes smaller than that of the first jitter sideband.

When both sinusoidal jitter and permanent offset modulation are applied, the PLL tracks both components. The resulting recovered clock can be expressed as:

$$V_{clk}(t) = A_{clk} \sin(2\pi f_{bit} t + A_{os} \sin(2\pi f_{os,m} t) + A_j \sin(2\pi f_j t)) \quad (3.22)$$

This phase-modulated signal can be expanded using Jacobi-Anger expansion as:

$$V_{clk}(t) = A_{clk} \sum_{n=-\infty}^{n=+\infty} \sum_{m=-\infty}^{m=+\infty} J_n(A_{os}) J_m(A_j) \sin(2\pi (f_{bit} + n f_{os,m} + m f_j) t) \quad (3.23)$$

This equation indicates that the steady-state recovered clock consists of a sinusoidal component with a fundamental frequency at f_{bit} , modulated by a offset term $n f_{os,m}$ and jitter applied to the input data $m f_j$. The amplitude of each spectral component is determined by the product of the Bessel functions, $J_n(A_{os}) J_m(A_j)$.

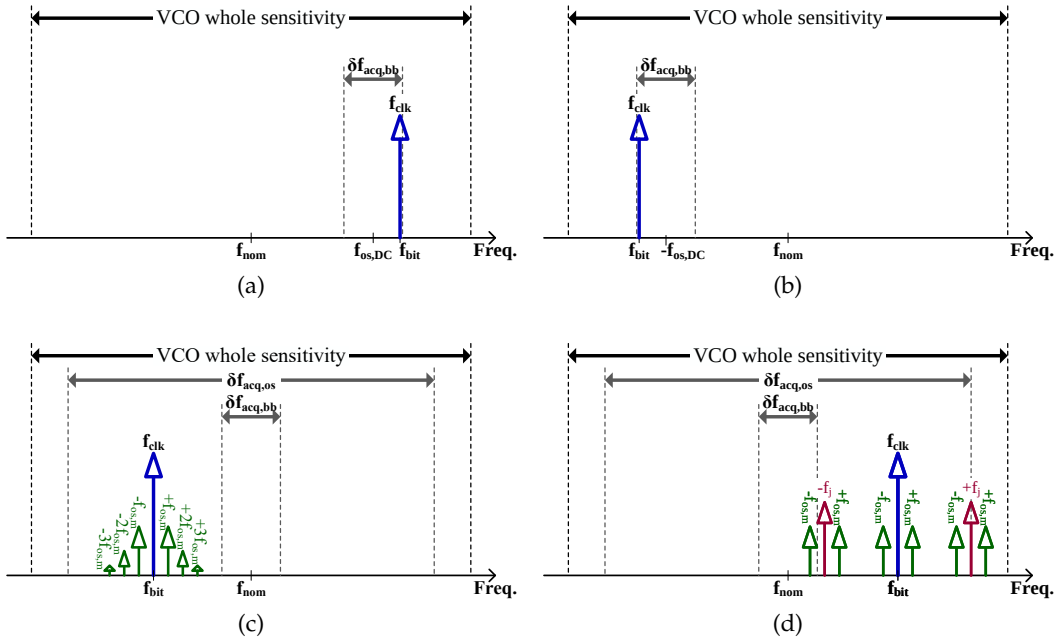


FIGURE 3.17: Recovered clock spectrum showing successful acquisition: (a) acquisition range shifted with positive static offset, (b) acquisition range shifted with negative static offset, (c) acquisition range extended with permanently modulated offset, and (d) jitter applied to input data with permanently modulated offset (only first-order displayed).

Fig. 3.17d shows the spectrum of the recovered clock in steady-state when both permanent offset modulation and jitter are applied. For simplicity, only the fundamental and first-order terms are displayed. The permanent offset modulation amplitude is suppressed by the PLL, while the jitter amplitude is tracked. As a result, the additional spectral lines introduced by offset modulation do not significantly degrade the recovered clock phase noise. Spectrum measurements in chapter 6 confirm that permanent offset modulation can be applied even during JTOL measurements.

3.3 Summary and conclusion

This chapter presented various frequency acquisition techniques for CDR circuits. A novel approach utilizing a modulated offset voltage (applied to the varactor of the VCO) or a modulated offset current (applied within the integral branch) was introduced. Unlike static offsets, which shift the acquisition range by changing the VCO center frequency, modulated offsets actively extend the inherent acquisition range from $\delta f_{acq,bb}$ to the values defined in (3.8) and (3.18). Key design conditions for effective acquisition were derived: modulated varactor voltage condition ((3.7) and modulated offset current condition (3.17)). These conditions show that the frequency sweep of the VCO caused by offset modulation must remain within the VCOs linear tuning range set by the integral branch. We also derived expressions for acquisition time ((3.9)) and upper bounds formulas ((3.10) and (3.19)). These results were illustrated through examples.

Using varactor voltage modulation, the acquisition range can be extended to approximately one third of the linear tuning range provided by the integral branch, as defined in (3.10). In contrast, with offset current modulation, the acquisition range can be expanded to utilize nearly the entire linear tuning range of the integral branch, as defined in (3.19).

This technique is particularly attractive due to its simplicity, minimal additional circuitry requirements, very slight increase in power dissipation and negligible impact on phase noise, as detailed in subsection 3.2.3. Chapter 4 discusses the circuit-level implementation of three frequency acquisition methods: digital VCO frequency band switching, offset current modulation, and offset voltage modulation. In contrast, Chapter 5 focuses solely on digital VCO frequency band switching, prioritizing designs with low power dissipation. Measurement results validating these methods are presented in Chapter 6. Partial results have been published in [22, 24], and the technique has also been granted a patent [25].

For automatic acquisition, a permanently modulated offset—using a sinusoidal or other suitable waveform such as triangular modulation—may be applied. However, to ensure robust acquisition, the primary design conditions outlined in this chapter must always be satisfied.

Chapter 4

Design of High-Speed BBCDRs in SiGe BiCMOS

In Chapter 1, the integration of photonic and electronic circuits was discussed, highlighting two methods: hybrid assembly, involving the combination of EIC and PIC technology chips, and monolithic integration using EPIC technology. This chapter presents the design of BBCDR circuits using two IHP SiGe BiCMOS technologies: the 250 nm node (SG25H4), representing the electronic version of EPIC, and the 130 nm node (SG13G3), providing the highest transistor performance in EIC technology. The adaptive dual-LF with independently tunable proportional and integral branches discussed in Chapter 2, as well as the frequency acquisition techniques described in Chapter 3, are implemented in these designs.

4.1 SiGe BiCMOS technology overview

Monolithic integration of photonic devices with electronics allows the shortest possible interconnects between photonic and electronic circuits [7]. IHP offers state-of-the-art BiCMOS silicon photonics platform, as shown in Fig. 4.1a. The Front End Of Line (FEOL) integrates photonic devices such as germanium (Ge) photodiode, waveguides and modulators at the same level as transistors, including HBTs and MOSFETs. The Ge photodiode is selectively grown on a silicon (Si) waveguide with a local buried oxide SOI substrate, while high power HBTs use a bulk Si wafer for efficient heat dissipation from high-speed circuits. Both the photonic and electronic circuits use the same Back End Of Line (BEOL) metal stack, providing a cost-effective approach that reduces integration parasitics. In this BiCMOS process, HBTs are integrated onto a common CMOS platform. Baseline CMOS features moderate speed transistors suitable for implementing on-chip control and tuning circuitry, reducing

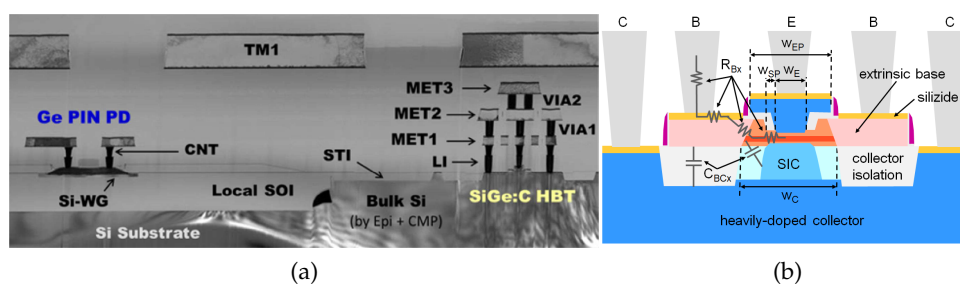


FIGURE 4.1: Cross-section of (a) Ge photodiode on SOI and a SiGe HBT fabricated in 250 nm EPIC technology [7] (b) high-speed SiGe HBT in 130 nm EIC technology [44].

subsystem assembly costs. Advanced SiGe HBTs offer high operating frequencies and breakdown voltage ($f_T \times BV$) for high-speed analog/mixed signal system-on-chip solutions. They also exhibit low $1/f$ noise corner frequencies and support cryogenic operation. In addition, the process includes integrated MIM capacitors, two types of poly-resistors, and symmetrical varicaps, the latter being essential for differential VCO design.

Fig. 4.1b shows the cross-section of the highest performance of HBT transistor in IHPs 130 nm BiCMOS process [44]. The low carbon concentration in the SiGe base region, as presented in [45], and the novel collector design for HBTs, as presented in [46], have improved the High Frequency (HF) performance of these bipolar transistors. The Silicon Germanium:Carbon (SiGe:C) HBT module, with its simplified BiCMOS integration scheme, enables easy migration across CMOS generations.

In SG25H4 technology, the HBT module integrated into a 250 nm CMOS platform delivers f_T up to 190 GHz [47], while in SG13G3 technology, the HBT module integrated into a 130 nm CMOS platform achieves f_T up to 470 GHz [44]. Furthermore, HBTs f_T is directly proportional to the transconductance (g_m), which is proportional to the collector current (I_C). Fig. 4.2 shows the simulated results for the two technologies as a function of the collector current density. The peak f_T is more than doubled, but this increase comes at the cost of additional current. In SG25H4 technology, the backend for routing includes three thin metal layers and two thick metal layers, while SG13G3 technology offers five thin metal layers and two thick metal layers. The thick metal layers are particularly advantageous for creating low-loss inductors.

Taking advantage of the superior performance of HBTs in this technology, high-speed building blocks are mainly realized using bipolar Current Mode Logic (CML) and Emitter Coupled Logic (ECL) circuits. These circuits use differential input and output signals, minimizing common-mode noise while operating with a low voltage swing, which is critical for high-speed operation. As highlighted in [48, 49], optimized design strategies for bipolar Current Mode Logic (CML) and Emitter Coupled Logic (ECL) circuits aim to minimize propagation delay by setting the appropriate bias current. Biasing transistors near their peak f_T provides an optimal operating range for high-speed circuits. However, the CML/ECL logic relies on continuously biased differential pairs, resulting in static power dissipation. In addition, the base-emitter diode drop ($V_{BE} \approx 0.9$ V) in the SiGe HBTs presents a significant challenge in reducing power dissipation [50]. ECL circuits typically operate on a positive or negative 3.3 V supply or higher voltage to provide the necessary voltage headroom [51].

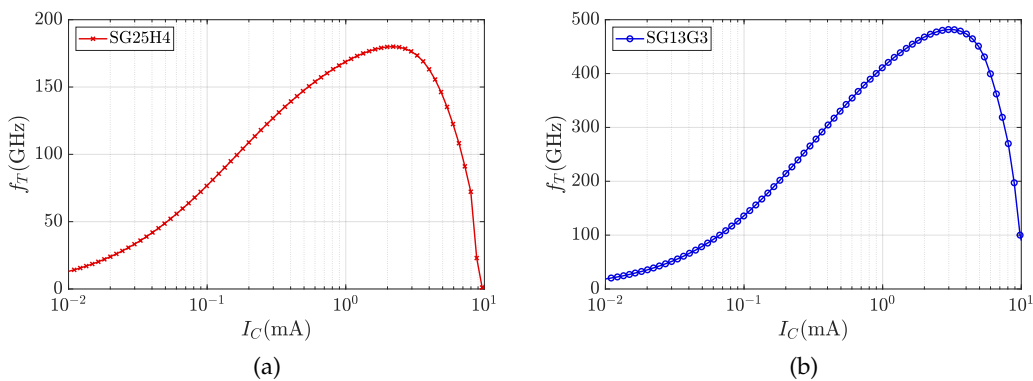


FIGURE 4.2: Simulated HBT f_T as a function of collector current in (a) SG25H4 and (b) SG13G3 technologies ($V_{CB}=0.25$ V).

4.2 Phase Detection

The Alexander PD was designed and implemented using D flip-flops and XOR gates (see Fig. 2.4a). Schematic of a clock edge-controlled master-slave D flip-flop implemented using ECL and consisting of two clocked D-latches in a push-pull configuration is shown in Fig. 4.3a. The push-pull operation facilitates efficient data latching by steering current between different paths based on clock transitions. The clock signal controls the latching of data at the input $D_p - D_n$. The transistors $Q_1 - Q_6$ are biased with stable current source I_{BIAS} , selected near the peak of f_T . The emitter follower pair, $Q_7 - Q_8$ with stable current source I_{EF} , acts as a driver for the slave latch. The base-emitter diode operates with a constant voltage drop ($V_{BE} \approx 0.9$ V), resulting in a minimum operating voltage of the D flip-flop of about 3.3 V. This accounts for three V_{BE} drops, the voltage headroom required for the current source (I_{BIAS}), typically > 200 mV, and the voltage drop across the load resistor R_L . The transistor pairs $Q_1 - Q_2$, $Q_3 - Q_4$ and $Q_5 - Q_6$ operate in the non-linear region to switch the bias current I_{BIAS} , requiring a logic switching voltage ΔV . ΔV is set between 200 mV and 300 mV to ensure reliable logic level switching across all PVT [52].

Fig. 4.3b shows the schematic of the CML XOR gate. The diodes in both the D flip-flop and XOR circuits are strategically placed to prevent the avalanche breakdown of the transistors by adding a DC voltage drop to reduce collector-emitter junction

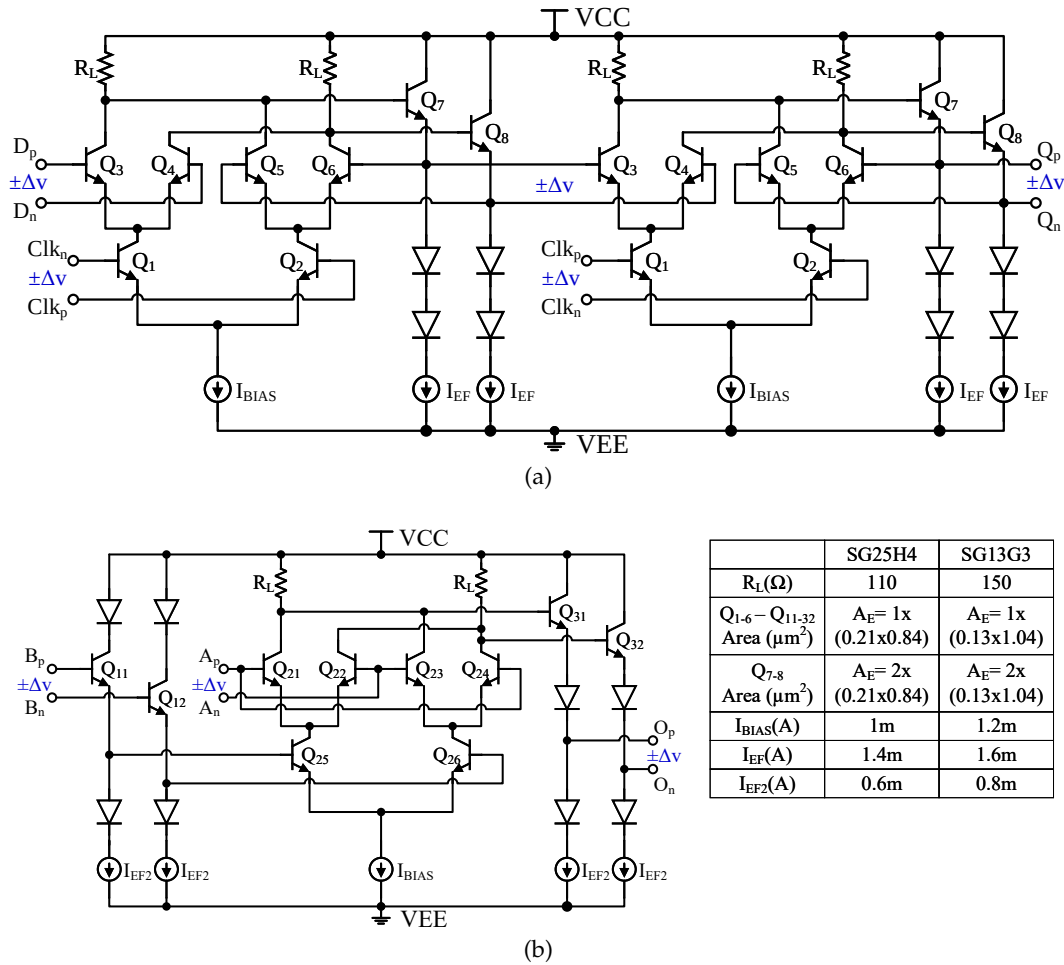


FIGURE 4.3: Schematic of (a) full-rate ECL master slave D flip-flop
(b) CML XOR.

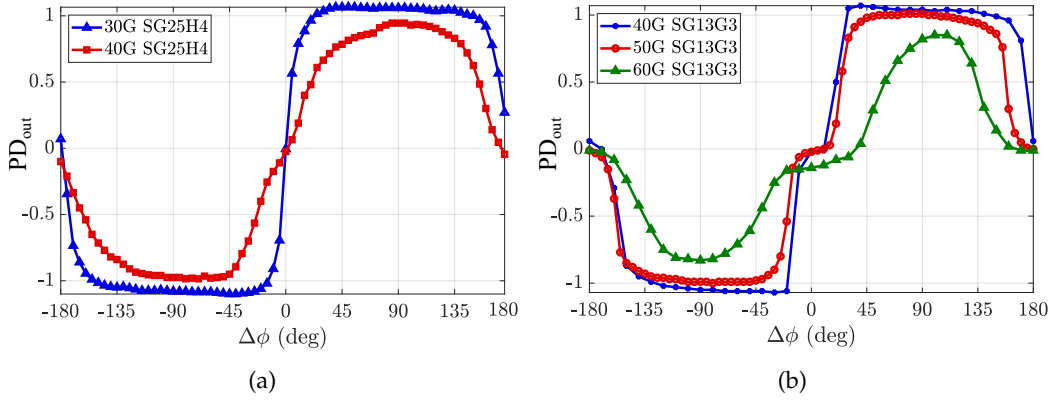


FIGURE 4.4: Simulated BBPD characteristics (a) RC extracted in SG25H4 (b) EM extracted in SG13G3.

voltages.

Considering the metastability discussed in 2.1.2, the speed of the BBPD is determined by the Clk-Q delay, the setup time in the D flip-flop, and the propagation delays in the XOR gate. The post-layout simulation of the BBPD characteristics can be performed by sweeping the phase of the clock signal with respect to the fixed input data signal. Fig. 4.4 shows a comparison of the characteristics in both SG25H4 and SG13G3 technologies. In the full-rate design, the data rate matches the clock frequency in all cases. In the SG25H4 technology, at a 30 GHz clock signal, the simulated RC-extracted results closely match the ideal behavior. However, as the clock frequency is increased to 40 GHz, the results indicate that the linear region is extended and the UP and DN signals do not fully switch to $\pm\Delta V$ in the saturation region. In the SG13G3 technology, which was evaluated using the EM-results, the circuit performs well up to 40 GHz clock signals due to the higher f_T . At 50 GHz, the propagation delay in the XOR gate creates a dead zone for $\Delta\phi$ of less than 45 deg. With a 60 GHz clock, this dead zone doubles, with $\Delta\phi$ approaching 90 deg. In addition, the UP and DN signals become significantly smaller (approximately halved) in the saturation region.

In summary, while SG13G3 shows superior performance at higher frequencies compared to SG25H4, both technologies reach their limits as the clock frequency increases, with maximum full-rate operation achievable up to $f_T/10$. The BBPD is the primary speed bottleneck in the CDR; therefore, the other CDR components were optimized for higher speeds. Full-rate BBDRs operating at 28 Gbps and 50 Gbps were studied in the SG25H4 and SG13G3 technologies, respectively.

4.3 Charge Pump + Loop Filter

A traditional CP combined with a LF (cf. 2.5a) using HBTs is discussed in [53]. The implemented CP with independently tunable proportional and integral branches is shown in Fig. 4.5. In the proportional branch, Fig. 4.5a, transistors $Q_1 - Q_4$ act as input current switches, directing current $I_{cp,prop}$ into R_{prop} to produce $\pm V_{prop}$ based on UP or DN signals, respectively. Emitter followers, using transistors $Q_5 - Q_6$ with stable current bias I_{EF} , act as drivers and improve the robustness of the circuit. Diodes are strategically placed to prevent avalanche breakdown of the transistors by introducing a DC voltage drop, thereby reducing the collector-emitter junction

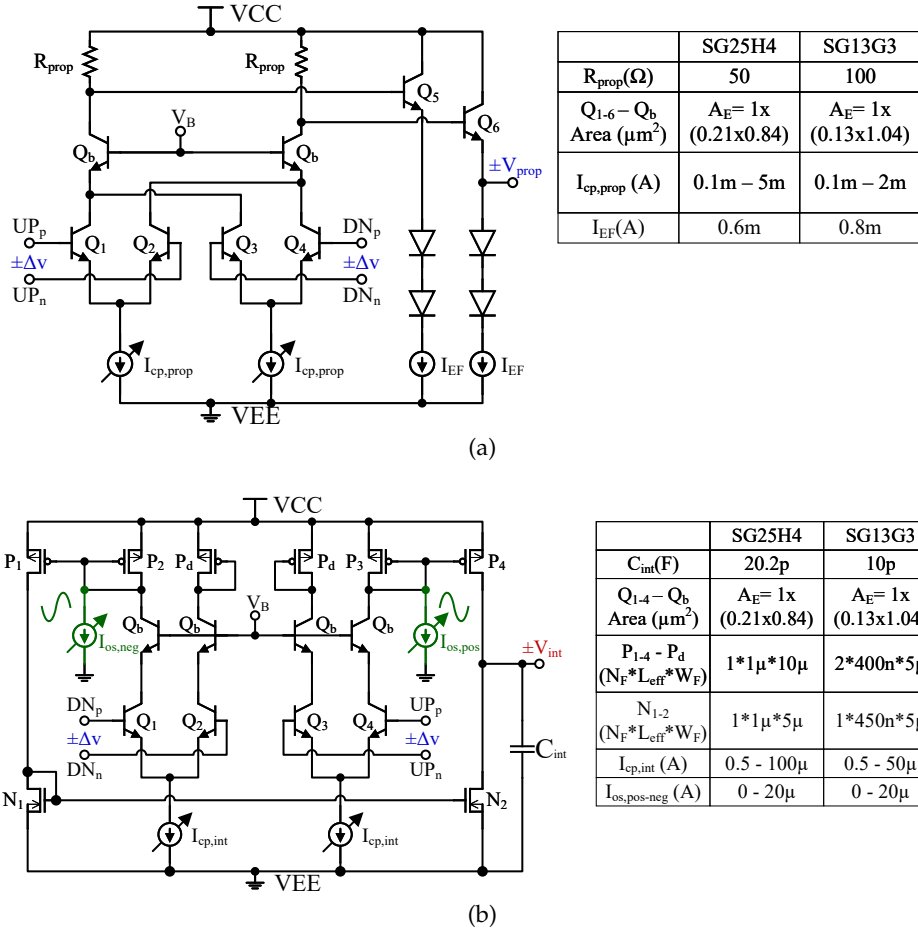


FIGURE 4.5: Schematic of the implemented CP+LF using HBTs with independently tunable (a) proportional branch (b) integral branch.

voltage. This arrangement also allows the control voltage V_{prop} to be set to discrete levels, ensuring operation within the linear tuning range and providing flexibility in the selection of the VCO topology.

In the BBPD with 100% transitions, a decision is made on each rising edge of the clock. The width of the UP or DN signal is equal to the period of the recovered clock signal t_{clk} . Therefore, the required bandwidth for the proportional branch is half of the clock frequency. For a 28 Gbps BBCDR in SG25H4, the required bandwidth is 14 GHz. The input base-collector capacitance C_{BC} of the input transistors Q_{1-4} contributes to the input pole, reducing the frequency response. Therefore, a cascode configuration realized by transistors Q_b , is used to improve the frequency response of the stages and to protect the input transistors Q_{1-4} from avalanche breakdown. By removing the cascode configuration and a diode in the emitter follower, the operating voltage can be reduced to 2.5 V, thereby reducing the power dissipation. In SG13G3 technology, for a 50 Gbps BBCDR, the required bandwidth for the CP was 25 GHz, and the circuit operating voltage was chosen to be 3.3 V, which is similar to the BBPD supply voltage. Fig. 4.6a show the simulated DC characteristics of V_{prop} as a function of changes in $I_{cp,prop}$ for the proportional branch circuits designed in SG25H4 and SG13G3 technologies. The $V_{prop,DC}$ have been set within the linear tuning range of the respective VCOs, details of which will be discussed in the following section.

In the integral branch, as shown in Fig. 4.5b, the transistors $Q_1 - Q_4$ control the current $I_{cp,int}$ to charge the capacitor C_{int} through the current mirror ($P_3 - P_4$) and

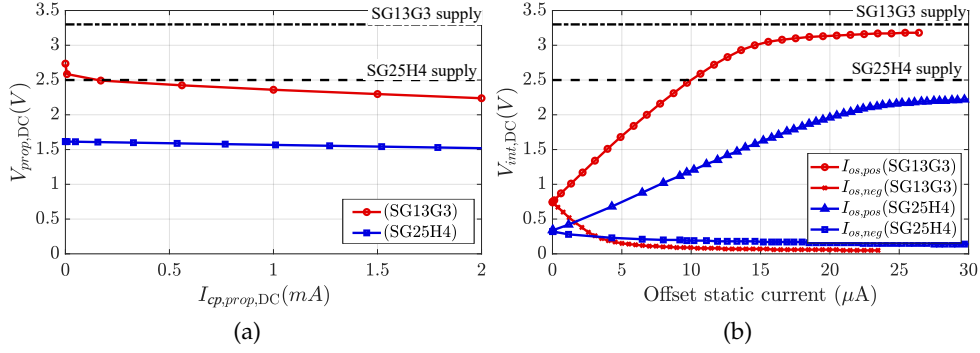


FIGURE 4.6: Simulated DC characteristics: (a) V_{prop} as a function of $I_{cp,prop}$, and (b) V_{int} as a function of offset current.

discharge it through the current mirrors ($P_1 - P_2$ and $N_1 - N_2$). Diode-connected PMOS transistors (P_d) are placed to ensure symmetry across the half-circuit. For the SG25H4 design with a 2.5 V supply, the common-base transistors Q_b are omitted. Conversely, in the SG13G3 design with a 3.3 V supply, common-base transistors were implemented to protect the input transistors Q_{1-4} from avalanche breakdown and to improve the frequency response of the stage.

As discussed in 3.2.2, the output impedances of the P4 (PMOS) and N2 (NMOS) form a resistive divider ($R_{out,int}$) and are always different due to operating point, temperature variations, process parameter mismatch, and PMOS vs. NMOS device sizing. The offset currents, $I_{os,pos}$ and $I_{os,neg}$ were used to compensate for this leakage effect and to extend the acquisition range by both static and modulated applications of these currents. Further details are discussed in the chapter 6. Fig. 4.6b show the simulated DC characteristics of V_{int} as a function of changes in static offset currents in integral branch circuits designed in SG25H4 and SG13G3 technologies. The DC value of V_{int} can be controlled as described in (3.12). In SG25H4 technology, the DC value of $V_{int,DC}$ can be adjusted in the range of 0.33 V to 2.1 V by varying the positive offset current ($I_{os,pos}$) from 0 to 23 μA. Similarly, $V_{int,DC}$ can be adjusted from 0.33 V to 0.2 V by varying the negative offset current ($I_{os,neg}$) from 0 to 10 μA. In SG13G3 technology, $V_{int,DC}$ can be adjusted from 0.74 V to 3 V by varying $I_{os,pos}$ from 0 to 15 μA, and from 0.74 V to 0.15 V by varying $I_{os,neg}$ from 0 to 5 μA.

4.4 Clock generation

In the full-rate CDR circuit, the recovered clock- being the highest frequency signal- must be reliably transferred from the VCO to the BBPD latches. We will first examine various VCO designs, followed by clock distribution using a high-bandwidth clock buffer designed to handle maximum fanout. This ensures efficient signal distribution while minimizing phase noise and jitter, thereby improving the overall performance and stability of the CDR system.

4.4.1 Voltage controlled oscillator

Several differential Colpitts VCOs with both fundamental and push-push topologies have been extensively studied in previous works [54–58]. These topologies are a

common choice for achieving HF operation, low-phase noise, and a wide tuning range in the SiGe BiCMOS process. The design methodologies are well detailed in [54, 59].

In the SG25H4 technology, the VCO core was implemented with Colpitts push-push topology as shown in Fig. 4.7. The core was designed for a nominal fundamental signal of 14 GHz, with the second harmonic clock signal of 28 GHz extracted using a transformer (T_1). A capacitive voltage divider, consisting of (i) a parallel combination of the external MIM capacitance (C_1) and the intrinsic base-emitter capacitance (C_μ), and (ii) a parallel combination of the MIM capacitance (C_2) and the varicap capacitances (C_{V1-4}), provides the necessary feedback to the tank circuit based on the Colpitts principle. The inductors L_B and L_E are symmetrical center-tapped inductors with a mutual coupling, providing additional magnetic base-emitter feedback [56]. Together with the capacitive voltage divider, the base resistance observed at the base of Q_1 , and parasitic components, inductor L_B forms the LC resonant tank, which determines the oscillation frequency. The VCO bias current is set by the bias voltage (V_B) and the tail resistor (R_E). In addition, the C_E act as bypass capacitor, providing an AC ground to the core circuit. The collector resistor (R_C) acts as a load resistor and helps set the DC operating point to the collector of Q_1 , ensuring stability. The capacitors C_C and C_3 , together with transformer T_1 , form a tuned resonant output network for second-harmonic signal extraction. The resistive dividers formed by R_1

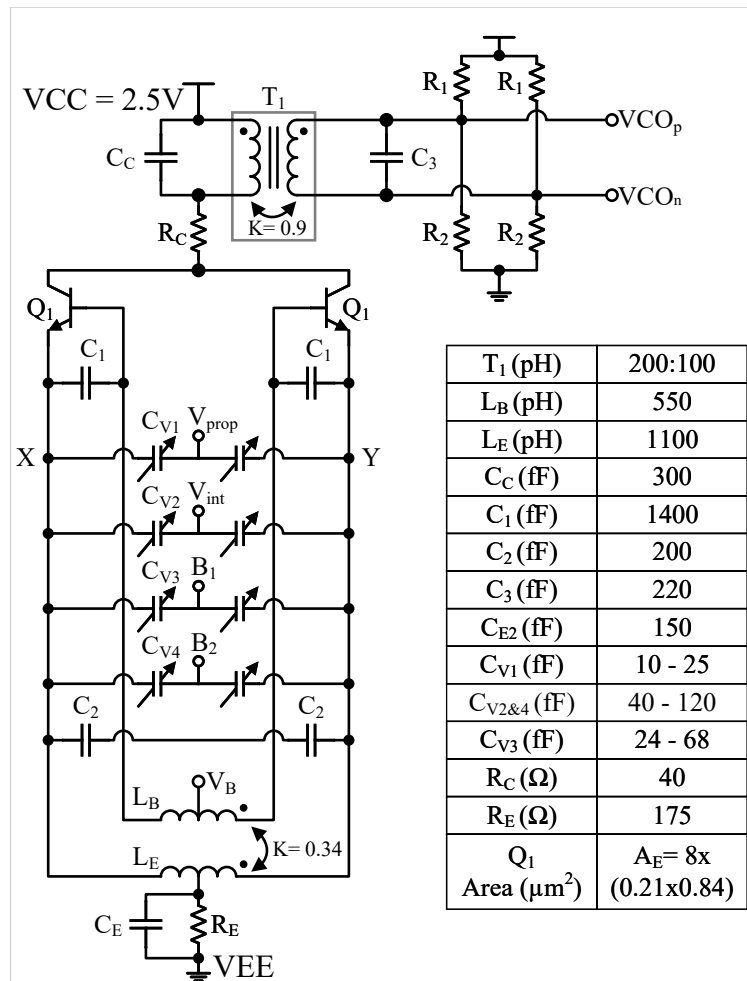


FIGURE 4.7: Schematic of push-push Colpitts VCO core in SG25H4 technology.

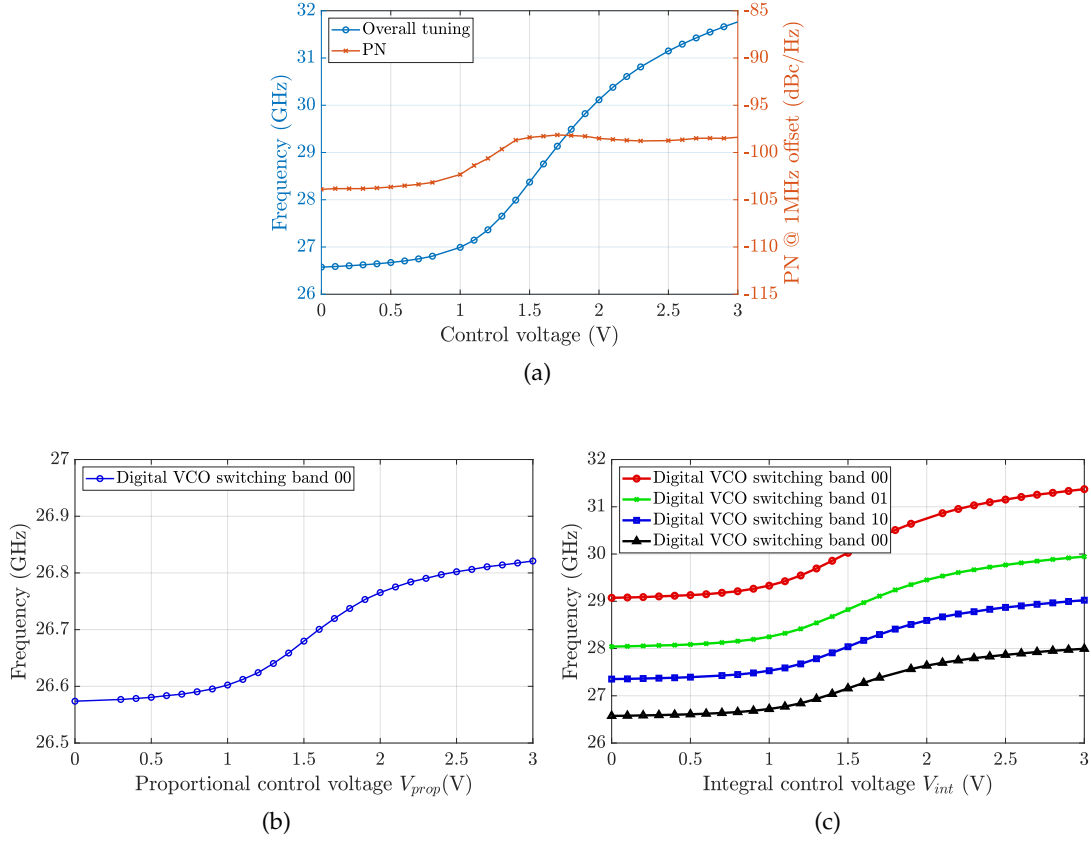


FIGURE 4.8: Simulated push-push VCO frequency tuning in SG25H4
 (a) whole sensitivity and phase noise (b) due to proportional branch
 (c) due to integral branch.

and R_2 set the DC bias points of the differential outputs (VCO_p and VCO_n).

The primary objective was to integrate multiple varicaps to control the VCO frequency. Specifically, one varicap was used for proportional control (V_{prop}), another for integral control (V_{int}), and two additional varicaps ($B_1 - B_2$) were digitally controlled to switch the VCO frequency sub-bands. The symmetric varicap, an n-channel MOS device, decreases the capacitance of the MOS structure as the control voltage applied to the n-well increases with respect to the gate, transitioning from accumulation to depletion. Accordingly, the quality factor of the parallel varicap varies from 7 to 18. The simulated sensitivity of the VCO is plotted in Fig. 4.8a. When the four controls (V_{prop} , V_{int} , B_1 , and B_2) were combined into a single analog control and tuned, the overall tuning range was from 26.57 GHz to 31.76 GHz, achieving a wide tuning range of 18 %. The phase remained below -98 dBc/Hz at 1 MHz offset frequency. In addition, the differential signal amplitude of the fundamental oscillation (at the X-Y node) was $2.3 V_{pp}$, while the differential signal amplitude at the $VCO_p - VCO_n$ node was $300 mV_{pp}$. Fig. 4.8b shows the tuning of the VCO with proportional control (V_{prop}) in switching band 00, where the digital control bits $B_1 - B_2$ were set to 00. The proportional VCO gain in the linear sensitivity range was approximately $K_{v,prop} = 230$ MHz/V. Fig. 4.8c shows the tuning of the VCO with integral control (V_{int}) over four switching bands, where the digital control bits $B_1 - B_2$ were varied from 00 to 11. The switching bands cover a total of 4.8 GHz and they overlap by more than 640 MHz to avoid dead zones during PLLs frequency acquisition. The integral VCO gain in the linear sensitivity range was approximately $K_{v,int} = 860$ MHz/V.

On the contrary in SG13G3 technology, the VCO core was implemented with a

Colpitts fundamental topology to extract a 50 GHz clock signal as shown in Fig. 4.9. The capacitive feedback is similar to the earlier approach, with a capacitive voltage divider consisting of (i) a parallel combination of the external MIM capacitance (C_1) and the intrinsic base-emitter capacitance (C_μ), and (ii) a parallel combination of the MIM capacitance (C_2) and the varicap capacitances (C_{V1-3}). The L_B and L_E are symmetric center-tapped inductors but are placed apart with shielding in the layout to eliminate coupling. Removing their interaction simplifies VCO optimization by minimizing design complexity, as cited in [56]. The quality factor of the inductor L_B was 21, with a self-resonance frequency (SRF) of 410 GHz, while the quality factor of the capacitor ranged from 3 to 5. This required a high negative resistance to sustain the oscillation, which was provided by the active circuit ($Q_1 - Q_2$), whose transconductance was increased by increasing the number of transistors or the emitter area. At the same time, as C_{BC} increases, the oscillation frequency decreases. Therefore, negative Miller capacitors C_3 are placed at the base-collector junctions to counteract this effect of C_{BC} , thereby increasing the oscillation frequency, as cited in [55]. Consequently, by adjusting the bias voltage V_B , the circuit can be operated in the forward active region while ensuring that the breakdown voltage remains within safe limits. The bias current source (I_{BIAS}) is used to reduce the sensitivity to supply variations and, together with the resistor R_1 , controls the oscillation amplitude. This arrangement is critical for maintaining stable signal integrity under varying operating conditions. The emitter follower pair $Q_3 - Q_4$, with diodes and a stable current bias I_{EF} acts as a driver. The common-collector configuration provides high bandwidth, and the outputs $VCO_p - VCO_n$ can be connected to the subsequent stage of the clock buffer at three DC levels.

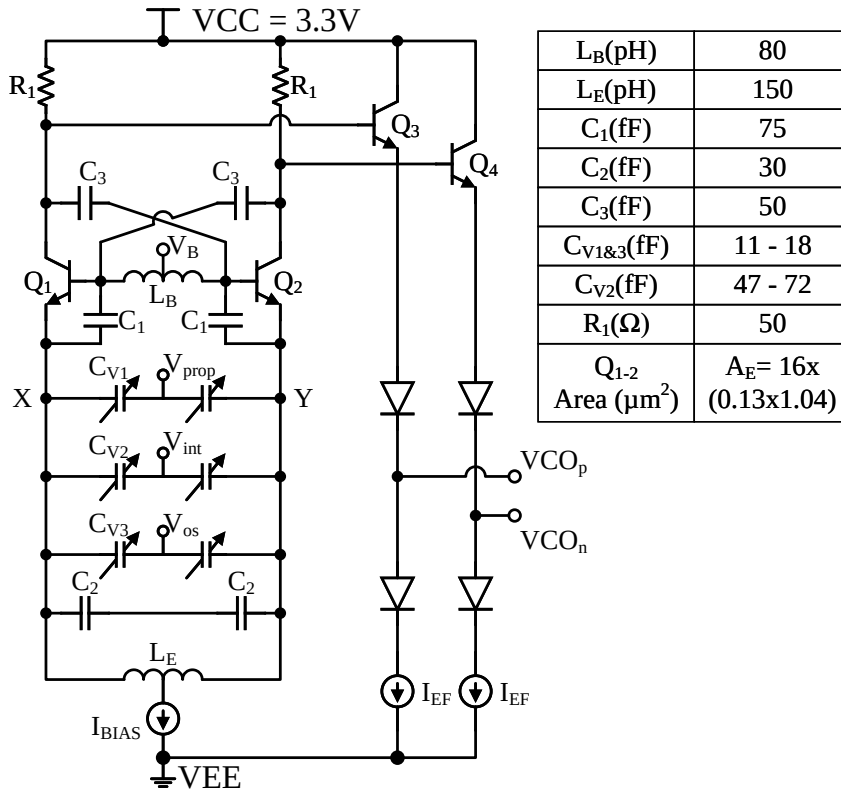


FIGURE 4.9: Schematic of fundamental Colpitts VCO in SG13G3 technology.

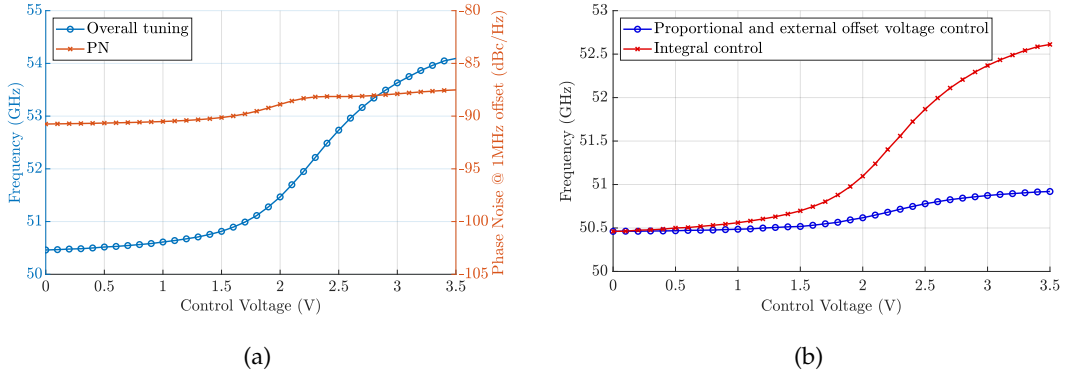


FIGURE 4.10: Simulated fundamental VCO frequency tuning in SG13G3 (a) whole sensitivity and phase noise (b) separate tuning controls used in CDR.

The goal of this design was to integrate three varicaps to control the VCO frequency. One varicap was used for proportional control (V_{prop}), another for integral control (V_{int}), and the third for external analog tuning V_{os} . Figure 4.10a shows the overall tuning range from 50.5 GHz to 54 GHz, achieving approximately 6.7 % tuning when all three varicaps were adjusted simultaneously. The phase noise remained below -87 dBc/Hz at 1 MHz offset frequency. The differential signal amplitude of the fundamental oscillation (at the X-Y node) was 1.2 Vpp, while the differential signal amplitude at the $VCO_p - VCO_n$ node was 1 Vpp. Fig. 4.10b shows the VCO tuning with separate V_{prop} & V_{int} controls used in the BBCDR and the external VCO control V_{os} . The proportional, integral and offset voltage VCO gains in the linear sensitivity range were approximately $K_{v,prop} = 310$ MHz/V, $K_{v,int} = 950$ MHz/V, and $K_{v,os} = 310$ MHz/V, respectively.

4.4.2 Clock buffer

A large VCO amplitude is essential to achieve low phase noise in clock generation circuits. However, the clock signal required to switch the ECL-based latches requires a minimum switching amplitude (ΔV). To ensure this, a cascode limiting amplifier was implemented for the clock buffer, as shown in Fig. 4.11. To suppress the effect of the base-collector capacitance C_{BC} of Q_{1-2} on the input pole, common-base transistors Q_b are stacked on top of transistor Q_{1-2} . This increases the bandwidth, improves input-to-output isolation, and distributes the collector-emitter voltage between Q_{1-2} and Q_b , preventing avalanche breakdown of Q_{1-2} . In addition, the cascode configuration provides a fast response time and improved timing accuracy, making it well suited for high-speed BBCDR applications. At high operating speeds, the drive capability of single emitter followers is limited due to the reduced effective current gain of the transistors [52]. Consequently, two emitter follower stages, Q_{5-6} and Q_{7-8} , have been implemented to better manage load requirements and mitigate layout parasitics, while maintaining signal integrity. However, this configuration results in increased power dissipation.

Fig. 4.12 shows the simulated transfer function of the clock buffer, demonstrating the variation of the amplitude of $Clkp - Clkn$ (delivered to the latches) as the input signal ($VCO_p - VCO_n$) frequency changes, while keeping the amplitude constant. This frequency sweep, conducted in the transient domain and plotted to analyze the dynamic response. In the design using SG25H4 technology, the push-push VCO

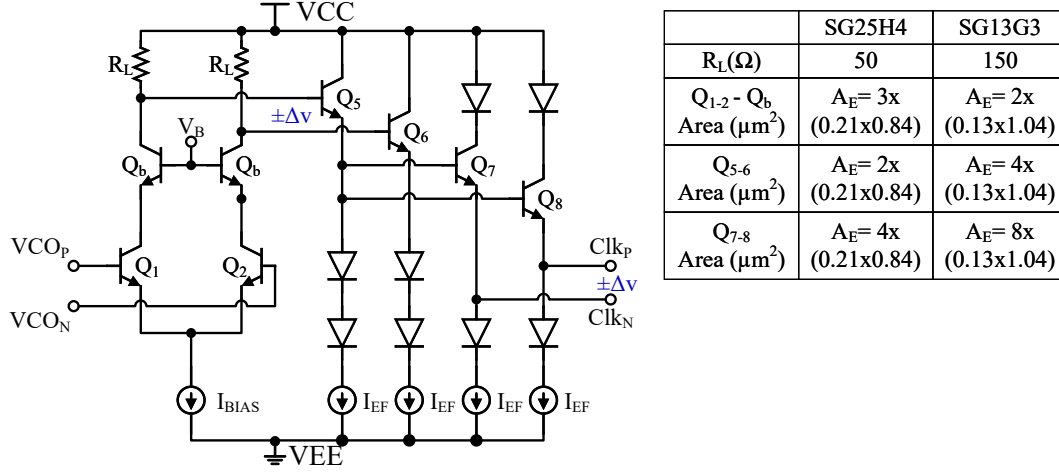


FIGURE 4.11: Implemented clock buffer.

output provides a differential signal amplitude of $VCO_p - VCO_n = 300 \text{ mV}_{pp}$. The latches required a minimum switching voltage of $\pm\Delta V = 200 \text{ mV}$. Therefore, the gain was kept at 3 dB up to a 30 GHz clock frequency. Conversely, in the design using SG13G3 technology, the fundamental VCO core output provides a differential signal amplitude of $VCO_p - VCO_n = 1V_{pp}$. To maintain the minimum switching voltage of $\pm\Delta V = 200 \text{ mV}$, the clock buffer can attenuate the signal amplitude by approximately $20 \times \log(0.4/1) \approx -8 \text{ dB}$ up to 56 GHz. Under these conditions, the cutoff frequency at -8 dB is about 60 GHz, providing sufficient bandwidth for high-speed switching operation.

Fig. 4.13a shows the core layout of the implemented 28 Gbps full-rate BBCDR in SG25H4 technology, with a core area of 0.3375 mm^2 . Similarly, Fig. 4.13b shows the core layout of the implemented 50 Gbps full-rate BBCDR in SG13G3 technology. Due to the use of smaller transistors and passive components, the core area is only 0.225 mm^2 . For high-speed operation, placement and routing were maintained as compact and symmetrical as possible to minimize parasitic effects and optimize signal integrity.

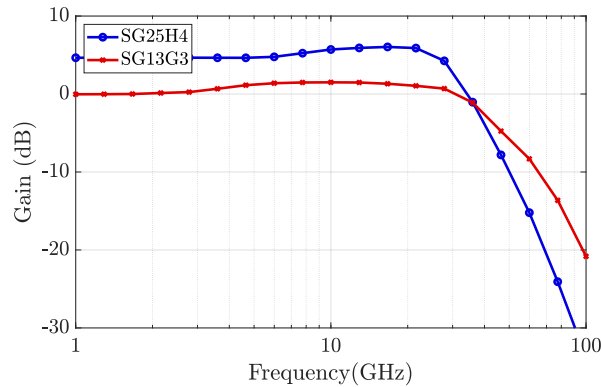


FIGURE 4.12: Clock buffer small-signal transfer function.

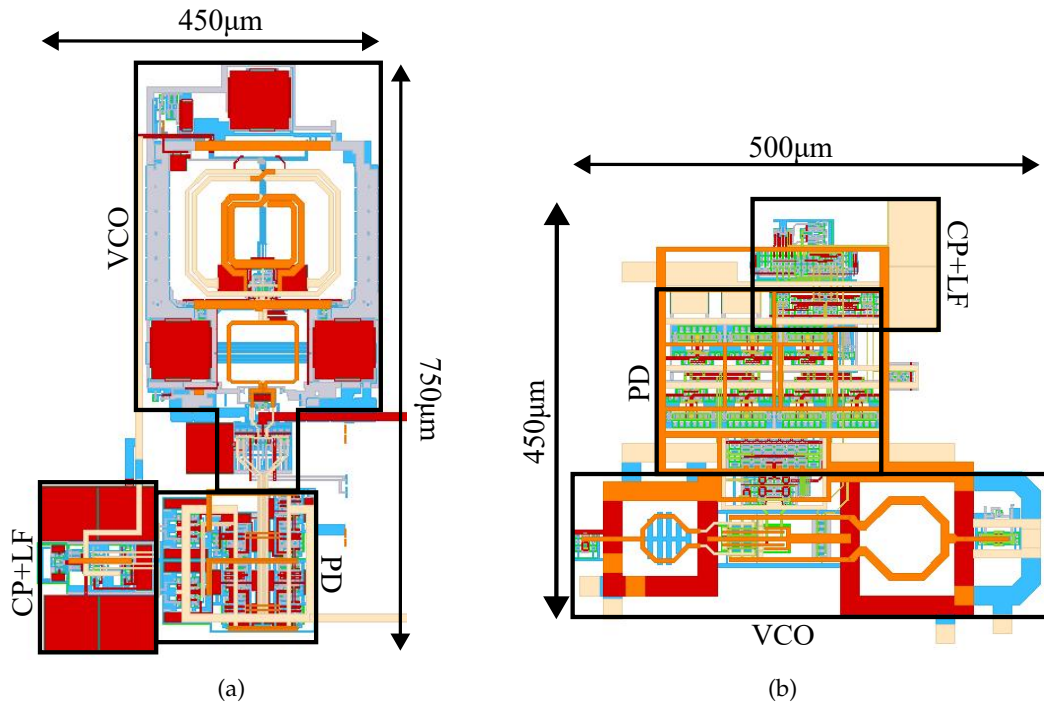


FIGURE 4.13: Core layout: (a) 28 Gbps BBICDR in SG25H4 (b) 50 Gbps BBICDR in SG13G3.

4.5 Summary and conclusion

In this chapter, an overview of SiGe BiCMOS technology is provided, focusing on the design of high-speed BBICDR circuits using IHPs 250 nm (SG25H4) for EPIC IMDD transceivers and 130 nm (SG13G3) SiGe BiCMOS technology for hybrid IMDD transceivers. Key components of the BBICDR, including the BBPD, dual-branch CP+LF, VCO, and clock buffer, are discussed. Given the critical role of the BBPD as the primary speed bottleneck, simulations were conducted first for the BBPD, with subsequent components optimized for similar operating frequencies. The integral branch CP includes offset current adjustments to control the integral control voltage V_{int} . Two VCOs, a Colpitts push-push oscillator in SG25H4 and a fundamental Colpitts topology in SG13G3, were designed with multiple varicaps to facilitate frequency control.

These circuits have been fabricated, and their measured results are presented in Chapter 6. Partial results using the SG25H4 technology have been published in [21, 22], and those using the SG13G3 technology have been published in [24].

FIGURE 5.1: Cross sectional view of the (a) NMOS with illustration of parasitic at the front-gate and back-gate [62] (b) metal stack [61].

transistors support back gate biasing (V_{BG}) to control the threshold voltage (V_T), improving transistor performance and supporting both flip-well and conventional well architectures. The coupling factor of $|dV_T/dV_{BG}|$ is approximately 75 mV/V, with a maximum V_{BG} of $|2\text{ V}|$. In conventional wells, regular V_T (RVT) and high V_T (HVT) devices have nFETs and pFETs located on p-type and n-type back-gates, respectively, allowing Reverse Body Bias (RBB) to reduce leakage current by increasing V_T . Conversely, in the flip-well architecture, super-low V_T (SLVT) and low V_T (LVT) devices have nFETs and pFETs located on n-type and p-type back-gates, respectively, allowing Forward Body Bias (FBB) to improve performance with faster switching capabilities and higher drive by lowering V_T .

As presented in [62], Fig. 5.1a shows the cross-sectional view of the n-type flipped-well transistor in 22FDXTM with parasitic components. Increasing the positive back gate voltage V_{BG} for the nFET shifts the peak values of f_T (350 GHz) and f_{MAX} (370 GHz), as well as their gain-efficiency products $f_T \times g_m/I_D$ and $f_{MAX} \times g_m/I_D$, towards lower front gate voltages V_G , while maintaining the same peak magnitudes (see Appendix C). On the other hand, the drawbacks of the advanced CMOS technologies are layout constraints such as local density rules and large metallization RC delay, which pose more implementation challenges to the layout designer, especially for high-speed circuits. 22FDXTM provides several BEOL stack options. [61, 64] discuss transistor performance, which is highly sensitive to the RF layout, including the number of fingers (N_F), finger width (W_F), effective finger gate length (L_{eff}), and distance between gates. In addition, the transistor Pcells and routing must carry high currents and meet electro-migration limits. Stack 19 with dual ultra-thick metal (UTM) and 11 level metal was chosen as shown in the Fig. 5.1b. In addition, passive components such as capacitors, inductors, and transmission lines benefit from thick metal layers, offering higher quality factors (Q) and reduced losses.

The peak f_T as a function of overdrive voltages ($V_{ov} = V_{GS} - V_T$) is difficult

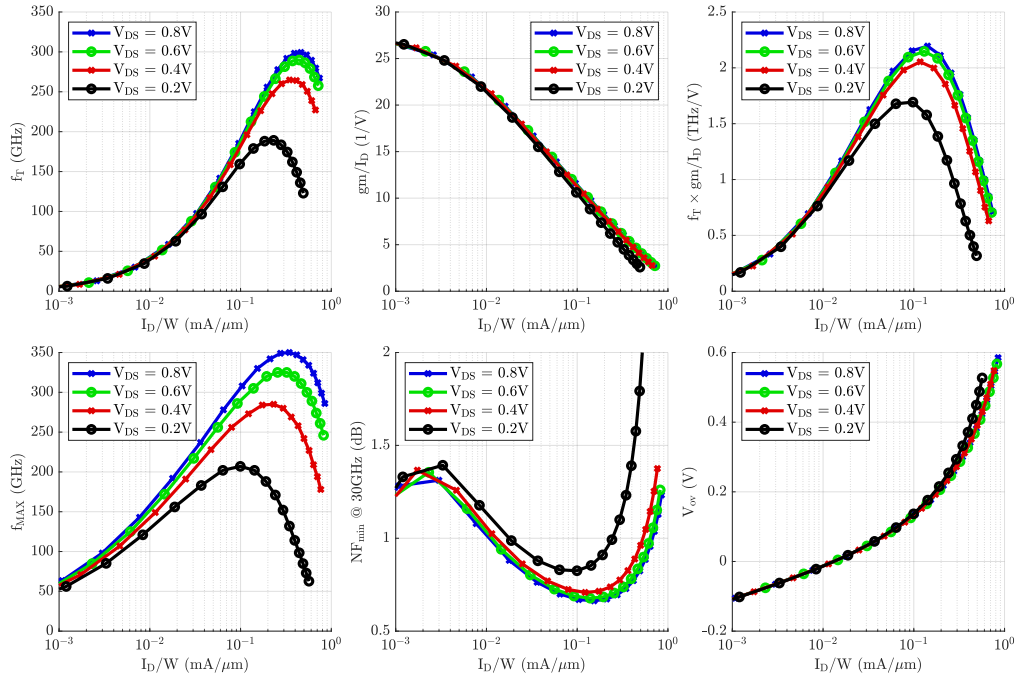


FIGURE 5.2: Simulated SLVT nFET mm-wave transistor parameters as a function of drain current density for various drain voltages.

to use in analytical circuit design [64]. However, the drain current per unit device width (I_D/W) at which the peak f_T occurs provide a more practical approach, allowing current-centered biasing techniques that simplify CMOS CML logic and mm-wave circuit design. Various simulated transistor parameters as a function of drain current for different drain voltages are shown in Fig. 5.2. The g_m/I_D methodology for transistor sizing, first proposed by Silveira et al. [65], uses the moderate inversion region to achieve an optimal speed-power tradeoff. In the weak inversion, the g_m/I_D ratio is high, allowing for efficient low-power operation, but at the cost of speed. Conversely, in strong inversion, g_m/I_D is low, resulting in higher speed but increased power consumption. It is also interesting to note that the peak f_T current density is typically $0.4 \text{ mA}/\mu\text{m}$, while the peak gain efficiency $f_T * g_m/I_D$ is around $0.1 \text{ mA}/\mu\text{m}$. In addition, the peak f_{MAX} current density is about $0.3 \text{ mA}/\mu\text{m}$, and the minimum noise figure NF_{min} @ 30 GHz for $V_{DS} > 0.2$ occurs at a current density of about $0.2 \text{ mA}/\mu\text{m}$. Despite these variations, V_{ov} shows a consistent trend for different V_{DS} . This methodology has been applied in this work. The BBCDR was designed to operate from supply voltage (VDD) of 0.8 V to 1.2 V. In the following, we call operation at VDD = 0.8 V as the low power (LP) mode and operation at VDD = 1.2 V as the high performance (HP) mode.

5.2 Phase Detection

Many techniques have been proposed to improve the speed and reduce the power consumption of the conventional CML D latches and flip-flops. To minimize voltage headroom and reduce the load on the clock buffer, Lee et al. [66] proposed a quarter-rate class-AB current switching D flip-flop topology that removes the tail current source. Building on this, Liao et al. [67] extended the design with shunt inductive peaking to achieve higher speed and full-rate class-AB switching. Guo et al. [68] further improved the topology by incorporating shunt peaking with FBB, reducing V_T and enabling operation at an ultra-low supply voltage of 0.6 V. Inductorless class-AB current switching D flip-flops operating up to 32 GHz have also been reported in frequency dividers using the same 22FDXTM technology [69, 70]. However, in full-rate BBPD designs, clocking becomes more challenging due to the increased number of latches (seven). In addition, the integration of inductors into full-rate BBPD increases the layout area and complicates routing in 22FDXTM technology, leading to parasitic effects that ultimately limit bandwidth.

Fig. 5.3a, shows the implemented architecture of the inductorless class-AB current-switching CML D flip-flop with FBB. The clock signal ($Clk_p - Clk_n$) is AC coupled through C_B and R_B . The current switching in the differential transistor pairs $N_3 - N_4$ and latch transistors $N_5 - N_6$ is controlled by the clock swing and gate control (V_B) instead of the conventional source-coupled current steering method. The clock transistors $N_1 - N_2$ operate in class-AB switching, drawing a large current at the peak of the clock swing, which enables larger voltage swings (ΔV) and enhances the signal in data path [66]. In contrast, the conventional Source Coupled Logic (SCL) D flip-flop is constrained by the bias tail current source, which limits its performance. When the clock is low ($Clk_p - Clk_n < 0$), the differential transistors in the master latch amplify the input ($D_p - D_n$) and store the result at nodes X and Y. When the clock becomes high ($Clk_p - Clk_n > 0$), the master latch is disabled, and the slave latch is enabled, regenerating the stored X-Y signals and passing them to the output. The narrow transistor sizing of the clock transistors reduces capacitance, minimizing the load on the clock buffer. As the supply is increased from LP mode to HP mode, the V_T

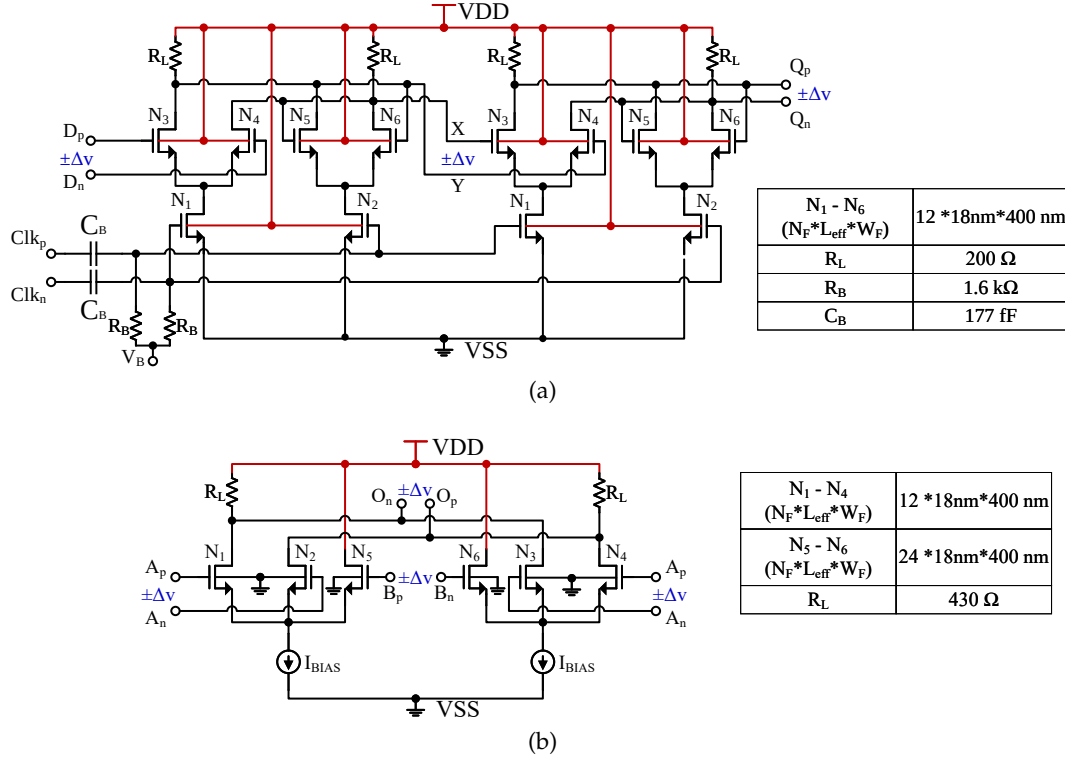


FIGURE 5.3: Schematic of: (a) full-rate class-AB current-switching CML D flip-flop with FBB and (b) CML XOR implemented in 22FDX™.

reduces from 205 mV to 170 mV due to FBB. Thus, V_{DSAT} reduces and overdrive (V_{ov}) of the transistors $N_1 - N_6$ increases, resulting in more drain current for the same input signals.

Razavi et al. [71] and Lee et al. [66] discuss high-speed, low voltage exclusive OR (XOR) gate that exhibit symmetry with respect to their two inputs. Fig. 5.3b shows a modified XOR gate based on the design presented in [71]. The differential transistor pairs $N_1 - N_2$ and $N_3 - N_4$ sense the input $A_p - A_n$, but with opposite polarity. Meanwhile, the clamp transistors $N_5 - N_6$, designed with different transistor sizes, are used to sense the input $B_p - B_n$. The circuit operates based on differential input and outputs, where $-\Delta V$ represents a logic 0 and $+\Delta V$ represents a logic 1. When both inputs are logic 0, the transistor pair $N_1 - N_2$ is enabled, producing an output of $O_p - O_n$ of logic 0. If $A_p - A_n$ is a logic 1 while $B_p - B_n$ remains a logic 0, the transistor pair $N_1 - N_2$ remains enabled and produces a logic 1 output. Conversely, if $A_p - A_n$ is a logic 0 and $B_p - B_n$ is a logic 1, the transistor pair $N_3 - N_4$ is enabled and produces a logic 1 output. Finally, if both inputs are logic 1, the transistor pair $N_3 - N_4$ remains enabled, but the output switches to logic 0. The circuit thus follows the XOR function, where $O = A \oplus B$.

Fig. 5.4 shows the simulated full-rate BBPD characteristics @ 30 GHz clock in both LP and HP modes. The speed of the BBPD is limited by layout constraints in advanced CMOS nodes, which dictate the placement of latches to properly receive input data and the recovered clock for phase information. In addition, factors such as Clk-Q delay, D-flip-flop setup time, and XOR gate propagation delays, as discussed in 2.1.2, further impact performance. Moreover, mismatched signal paths from the latches to the XOR gate (see 2.4a) introduce skew, resulting in asymmetry in the positive and negative phase difference information of the BBPD gain. The gain increases in HP mode due to the higher voltage headroom that allows faster transistors in the BBPD,

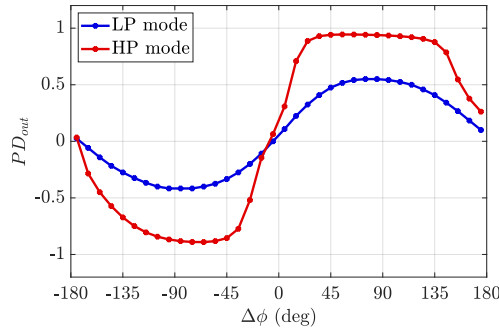


FIGURE 5.4: BBPD full-rate characteristics at 30 Gbps input data and 30 GHz clock (EM extracted).

along with the higher clock amplitude compared to LP mode, as will be discussed in 5.4. However, simulation results at a 30 GHz clock show that when switching from LP mode to HP mode, the data signal amplitude increased from $\pm\Delta V = \pm 300$ mV to ± 500 mV, while the clock signal amplitude increased from 400 mVpp to 1100 mVpp. It should be noted that the zero crossing of the PD characteristic is only marginally shifted between HP and LP mode which lets us expect a similar BER performance in both modes.

5.3 Charge Pump + Loop Filter

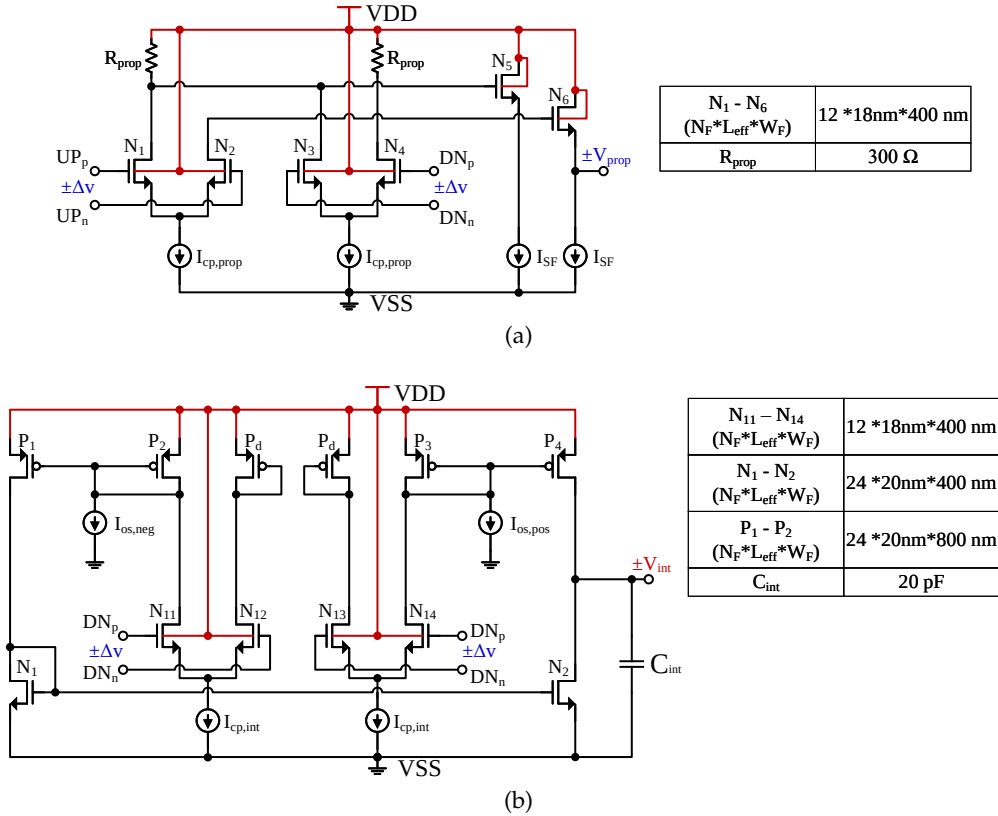


FIGURE 5.5: Schematic of the implemented CP+LF in 22FDX™ with independently tunable: (a) proportional branch and (b) integral branch.

A low-voltage CP implementation using MOSFET is discussed in [72]. However, the CP combined with a LF with proportional and integral branches, is similar to the design presented in 4.3, as shown in Fig. 5.5. In the proportional branch shown in Fig. 5.5a, transistors $N_1 - N_4$ act as input current switches, steering the current $I_{cp,prop}$ into R_{prop} to generate $\pm V_{prop}$ based on UP or DN signals. Source followers, consisting of transistors $N_5 - N_6$ with a stable current bias I_{SF} , act as driver and voltage shifter, ensuring that V_{prop} stays within the linear sensitivity range of the VCO. Fig. 5.6a shows the simulated DC characteristics of V_{prop} as a function of varying $I_{cp,prop}$ in both LP and HP modes.

In the integral branch as shown in Fig. 5.5b, the transistors $N_1 - N_4$ control the current $I_{cp,int}$ to charge the capacitor C_{int} through the current mirror ($P_3 - P_4$) and discharge it through the current mirrors ($P_1 - P_2$ and $N_1 - N_2$). The static offset currents, $I_{os,pos}$ and $I_{os,neg}$ can be used to compensate for the leakage effect in the CP, as discussed in 3.2.2. The simulated DC value of V_{int} as a function of different offset currents is presented in Fig. 5.6b for both LP and HP mode. In LP mode, $V_{int,DC}$ can be adjusted within the range of 0.12 V to 0.7 V by varying the positive offset current ($I_{os,pos}$) from 0 to 10 μ A and from 0.12 V to ≈ 0 V by varying the negative offset current ($I_{os,neg}$) from 0 to 10 μ A. In HP mode, $V_{int,DC}$ can be adjusted from 0.17 V to 1 V by varying $I_{os,pos}$ from 0 to 30 μ A, and from 0.17 V to ≈ 0 V by varying $I_{os,neg}$ from 0 to 15 μ A. The offset current was set to be $I_{os,pos} = 3 \mu$ A to achieve $V_{int,DC} \approx 0.4$ V in both modes, which corresponds to the center of the VCO sensitivity range, as discussed in the next section.

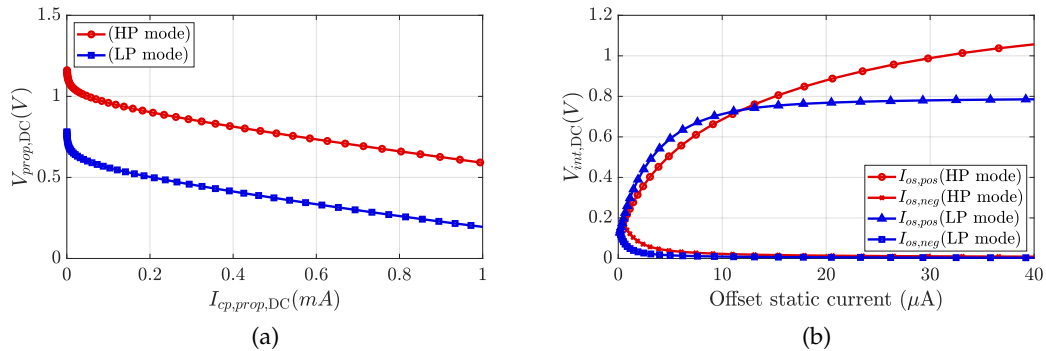


FIGURE 5.6: Simulated DC characteristics: (a) V_{prop} versus $I_{cp,prop}$, and (b) V_{int} versus offset currents, shown for both LP and HP modes.

5.4 Clock generation

Numerous topologies have been studied and proposed for low power and low voltage VCO designs. In this work, the NMOS class-B cross-coupled LC-tank oscillator was chosen over the Colpitts topology because of its superior startup conditions, which require lower gain, lower current consumption, and simpler implementation. However, this advantage comes at the cost of higher phase noise compared to the Colpitts oscillator, as discussed in a systematic comparison of differential Colpitts and differential cross-coupled LC VCOs in class-B operation presented in [73]. More insights and design methodology of the class-B cross coupled VCO design can be found in [74, 75]. In addition, Liao et al. [67] and Lee et al. [72] discuss the challenges in clock distribution from the VCO core to the high-speed sampling of the PD, with respect to the clock buffer circuit.

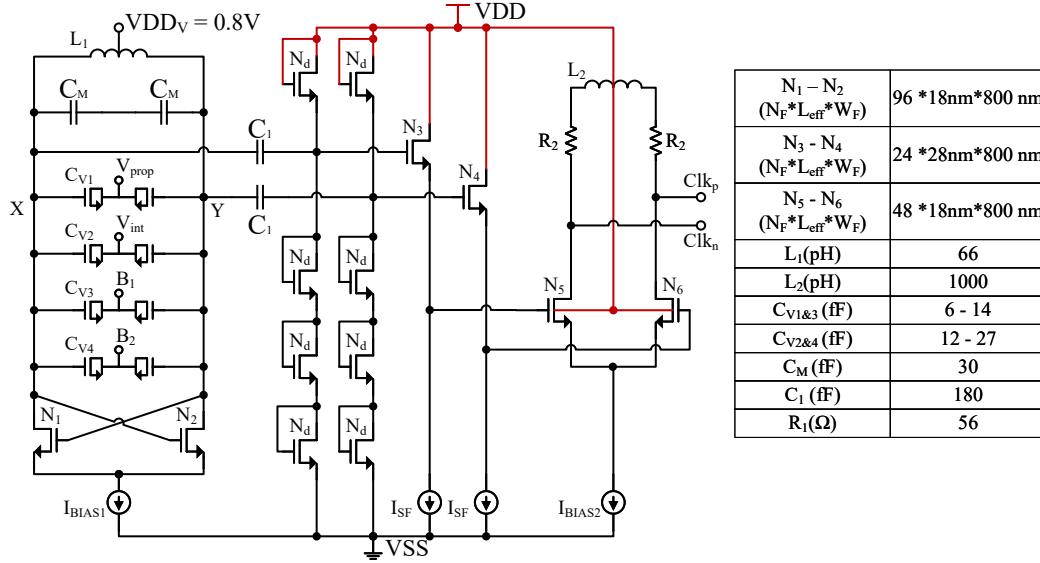


FIGURE 5.7: Schematic of class-B LC cross coupled VCO with clock buffer in 22FDX™.

The class-B LC cross coupled VCO with the clock buffer incorporated in this design is shown in Fig. 5.7. A symmetric center tapped inductor L_1 ($Q = 20$ @ 30 GHz and $SRF = 560$ GHz) in parallel with capacitor C_M , varactors C_{V1-4} and parasitic capacitance forms the resonant tank. The active circuit, consisting of transistors N_1-N_2 , provides negative resistance. A tail current source I_{BIAS1} is used to reduce supply sensitivity. Capacitor C_1 provides AC coupling between the oscillator core and the clock buffer. To deliver a large signal amplitude from the VCO to the latches (cf. Fig. 2.4a), directly loading the VCO output affects its frequency, tuning range and phase noise. To maintain signal integrity, a source follower cascaded with an underdamped peaking clock buffer [72] is used. The transistors N_d are used to bias the source follower transistors N_3-N_4 . The peaking inductor L_2 ($Q = 22$ @ 30 GHz, $SRF = 55$ GHz) compensates for the loading capacitance C_L seen by the buffer, including the parasitic capacitance from the routing to the latches. This configuration produces a voltage swing of $I_{BIAS2} \times R_{P2}$ at the resonant frequency $1/\sqrt{L_2 \times C_L}$, where I_{BIAS2} is the bias current source and R_{P2} represents the equivalent parallel resistance that accounts for the loss in L_2 . Since aligning the resonant frequencies of the VCO and the buffer is challenging, a resistive load R_2 is used to underdamp the buffer at low frequencies while enhancing the peaking within the VCO tuning range, ensuring large clock swings for the latches.

Similar to the VCO design in SG25H4 as described in 4.4.1, the primary goal was to integrate multiple varactors to control the VCO frequency. Specifically, one varactor was used for proportional control (V_{prop}), another for integral control (V_{int}), and two additional varactors ($B_1 - B_2$) were digitally controlled to switch the VCO frequency sub-bands. The simulated sensitivity and phase noise of the VCO is shown in Fig. 5.8a. When the four controls (V_{prop} , V_{int} , B_1 , and B_2) were combined into a single analog control and tuned, the overall tuning was from 28.42 GHz to 30.92 GHz, achieving a wide tuning range of 8.5%. The phase noise remained below -87 dBc/Hz at 1 MHz offset frequency. In addition, the differential signal amplitude (at the X-Y node) was $1 V_{pp}$. Fig. 5.8b shows the tuning of the VCO with proportional control (V_{prop}) in switching band 00, where the digital control bits B_1-B_2 were set to 00. The proportional VCO gain in the linear sensitivity range

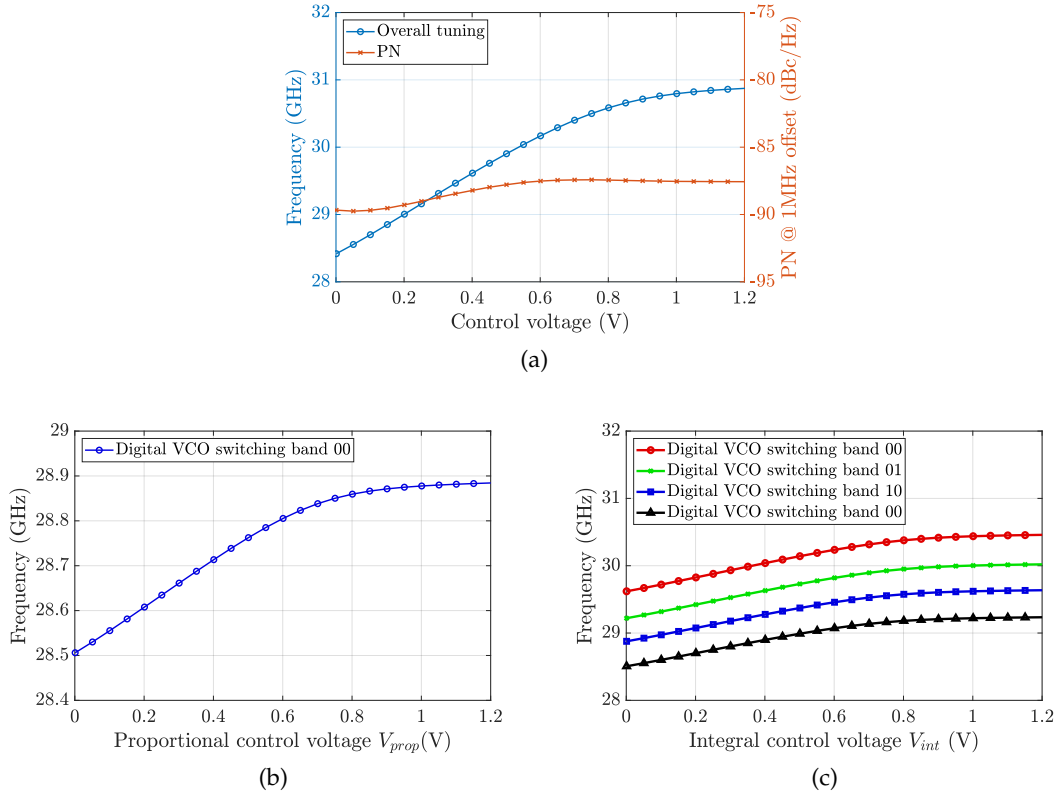


FIGURE 5.8: Simulated VCO frequency tuning in 22FDX™: (a) whole sensitivity and phase noise, (b) due to proportional branch, and (c) due to integral branch.

was approximately $K_{v,prop} = 400$ MHz/V. Fig. 5.8c shows the tuning of the VCO with integral control (V_{int}) over four switching bands, where the digital control bits $B_1 - B_2$ were varied from 00 to 11. The switching bands cover a total of 1.95 GHz and they overlap by about 400 MHz to avoid dead zones during PLLs frequency acquisition. The integral VCO gain in the linear sensitivity range was approximately $K_{v,int} = 900$ MHz/V.

Fig. 5.9 shows the simulated transfer function of the clock buffer from the VCO core nodes $X-Y$ to the input of the BBPD latches ($Clkp - Clkn$). This frequency sweep, conducted in the transient domain and plotted to analyze the dynamic response. The gain increases from LP mode to HP mode, due to the increased headroom of the current sources I_{SF} and I_{BIAS2} , resulting in increased current, and the reduced

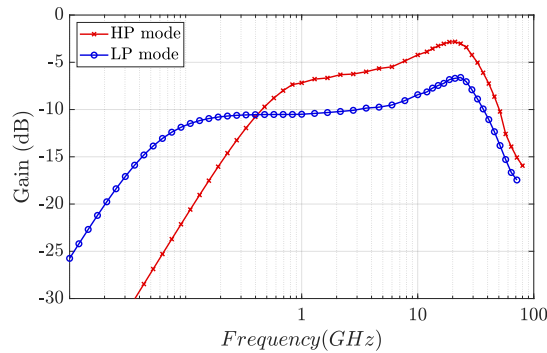


FIGURE 5.9: Clock buffer small-signal transfer function.

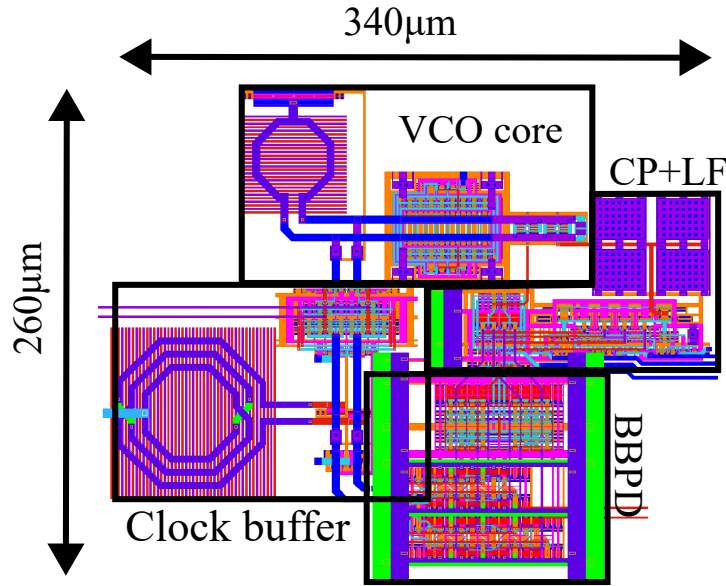


FIGURE 5.10: Core layout of 28 Gbps BBCDR in 22FDX™.

overdrive voltage V_{ov} due to FBB, resulting in faster transistors. In both modes, however, the peak occurs near the VCOs tuning frequency.

Fig. 5.10 shows the core layout of the implemented 28 Gbps full-rate BBCDR in 22FDX™ technology. The core area is 0.0884 mm^2 . Compared to the SG25H4 design (see Fig. 4.13a), using a lower technology node and improved passive components reduced the core area by a factor of four. Layout constraints, such as polysilicon gate alignment and limited pcell rotation, reduced the flexibility of the design. To minimize parasitic effects and maintain signal integrity, the placement and routing were kept compact and symmetrical. However this approach resulted in higher parasitic capacitance between closely spaced signal lines.

5.5 Summary and conclusion

In this chapter, an overview of FD-SOI CMOS technology is presented, emphasizing low power consumption through the application of a back-gate biasing technique. The back gate bias was tied directly to the supply voltage, resulting in 0.8 V for LP mode and 1.2 V for HP mode, extendable up to 2 V with respect to the source of the transistor for optimal performance [62]. The chapter details the design of high-speed BBCDR circuits using GFs 22 nm FD-SOI CMOS (22FDX™) for hybrid IMDD transceivers. The circuits employ a current-centered biasing approach, incorporating high-speed Class AB-current switching CML D flip-flops with FBB and low-voltage XOR gates, enabling BBPD operation at a 0.8 V supply (LP mode). Simulation results indicate that the full-rate BBPD operates effectively up to 30 GHz, with subsequent circuits optimized accordingly. A dual-branch CP+LF with independently tunable proportional and integral branches was implemented. Additionally, a Class-B LC cross-coupled VCO was designed with multiple varicaps to enable frequency tuning across multiple bands. Simulation results for both LP and HP modes are included. The fabricated chip and its measured performance are presented in Chapter 6. Partial results have been published in [23].

Chapter 6

Measurements results

This chapter presents the measurement results of the full-rate NRZ BBCDR chips discussed so far. Each BBCDR chip was characterized from a different application perspective. First, the 28 Gbps BBCDR in SG25H4 technology was characterized focusing on the independent tunability of the proportional and integral branches, as well as frequency acquisition using static and modulated offset current in the integral branch along with the digital switching of VCO frequency bands. Next, the 28 Gbps BBCDR in 22FDXTM technology was characterized focusing on the low-power design, with frequency acquisition solely by digital switching of VCO frequency bands. Finally, the 50 Gbps BBCDR in SG13G3 technology was characterized with a focus on extending frequency acquisition using offset current modulation in integral branch and external offset voltage modulation.

The measurement setup is shown in Fig. 6.1. Keysight's M8194A arbitrary waveform generator (AWG) has a built-in jitter source that can be embedded in the maximum length PRBS¹⁵-1 (PRBS15) pattern with a frequency content up to 50 GHz. The

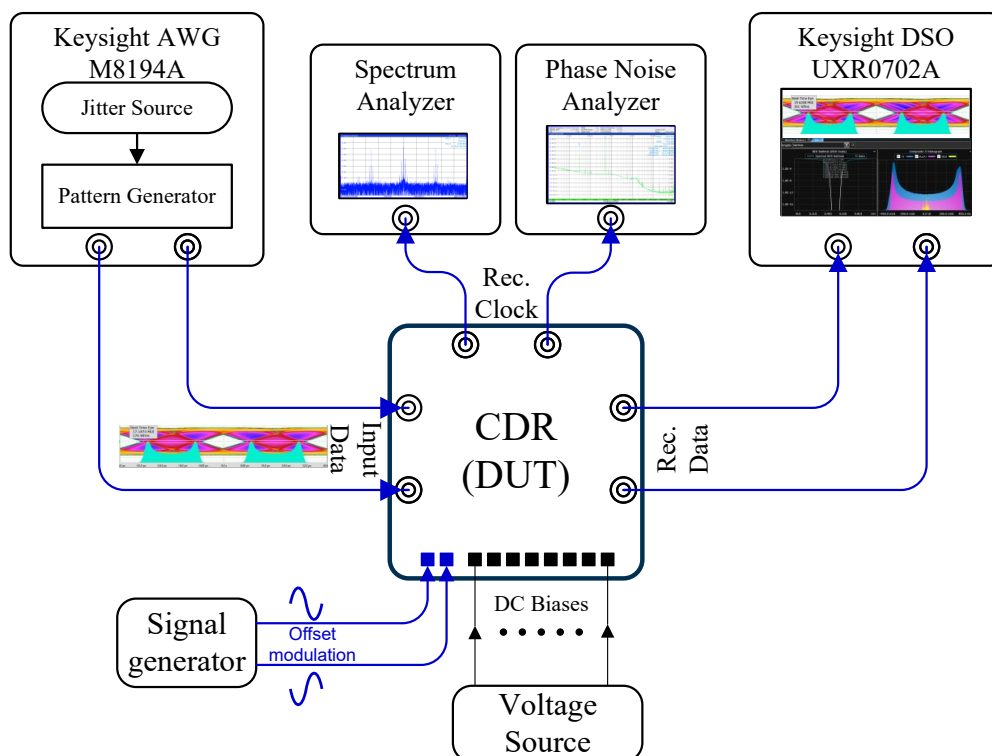


FIGURE 6.1: Measurement setup used for BBCDR chip characterization.

recovered data was measured using Keysight's advanced UXR0702A real-time oscilloscope, which offers a maximum sampling rate of 256 GSa/s and 70 GHz bandwidth, along with an advanced signal processing memory controller for jitter measurements, specifically Time Interval Error (TIE). In addition, the bathtub curve, which plots BER vs. timing margin (or sample position) in a data eye diagram, was used to measure BER according to the respective standards. The recovered clock was measured using the Anritsu MS2760A portable spectrum analyzer, which supports frequencies 9 kHz to 110 GHz, and the Rohde & Schwarz FSWP50 phase noise analyzer, which operates over a frequency range from 10 MHz to 50 GHz. DC voltage sources were used to power and bias the chip. To extend the acquisition range through offset modulation, an external signal generator with a frequency generation of up to 50 MHz was used. This approach enables precise control over the offset amplitude and frequency without integrating these functions within the current research scope.

6.1 28 Gbps BBCCR chip in SG25H4 technology

The implemented architecture and chip microphotograph, fabricated using IHPs SG25H4 technology to characterize the 28 Gbps NRZ full-rate BBCCR, are shown in Fig. 6.2a and Fig. 6.2b, respectively. The independent tunability of the proportional and integral branches was achieved by adjusting the CP currents, $I_{cp,prop} = 0.1\text{--}5\text{ mA}$ and $I_{cp,int} = 0.5\text{--}100\text{ }\mu\text{A}$, respectively, via external pads. Another set of external pads, B_1 and B_2 , was used to digitally switch the VCO over four frequency bands.

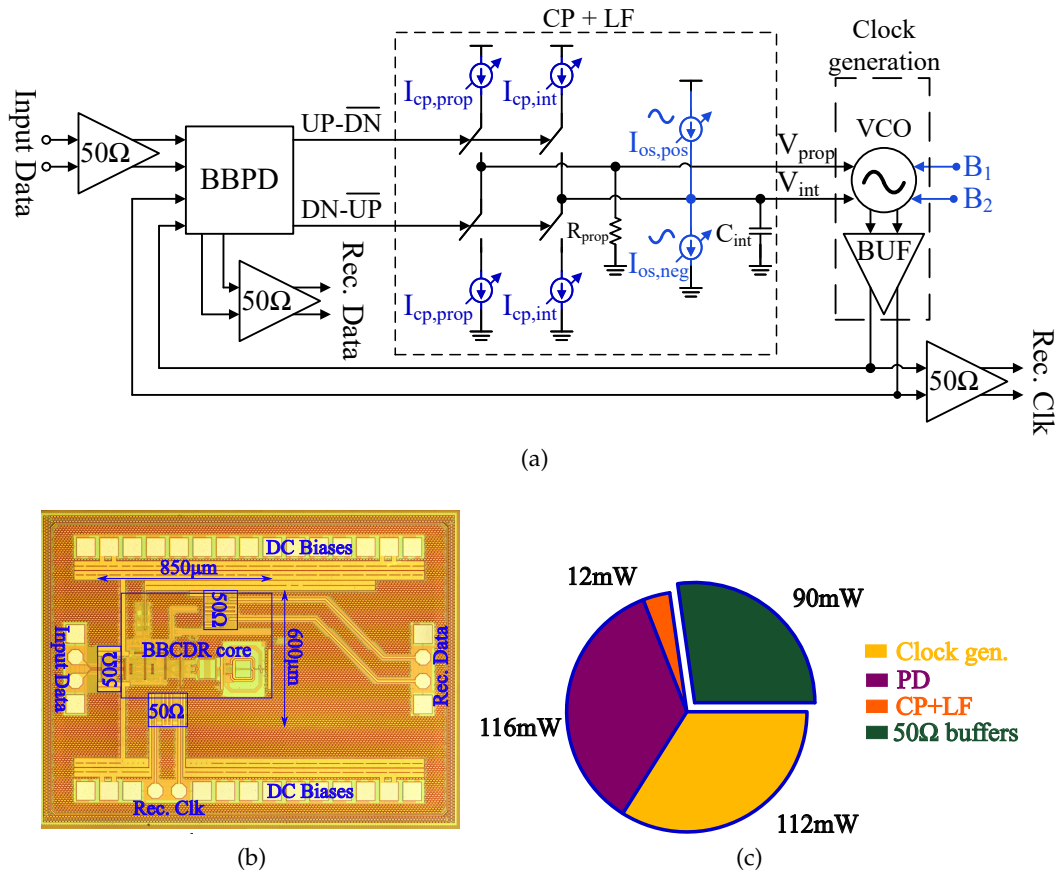


FIGURE 6.2: 28 Gbps NRZ full-rate BBCCR chip in SG25H4: (a) implemented architecture, (b) microphotograph, and (c) power breakdown.

The offset current, $I_{os,pos} = 0\text{--}20\ \mu\text{A}$, applied via an external pad, was used to automatically extend the acquisition range within each frequency band. The BBICDR core area is $0.3375\ \text{mm}^2$; including the $50\ \Omega$ buffers, the area increases to $0.51\ \text{mm}^2$, and the total chip area is $2.125\ \text{mm}^2$. The BBPD, clock buffer, $50\ \Omega$ input and output buffers were powered with a $3.3\ \text{V}$ supply, whereas the CP+LF and the VCO core were powered with a $2.5\ \text{V}$ supply. As shown in Fig. 6.2c, the BBICDR core had a power dissipation of $240\ \text{mW}$, while the buffers dissipated $90\ \text{mW}$. $50\ \Omega$ input and output buffers without inductive peaking have been implemented for testing purposes, similar to the circuits mentioned in [50, 52].

By applying a static offset current $I_{os,DC}$, the center frequency of the VCO can be tuned to any value within the frequency band, as discussed in sections 3.2.2 and 4.3. The output impedance of the N_2 transistor was designed to be smaller than that of the P_4 transistor (see Fig. 4.5b); therefore, V_{int} would discharge to VEE due to CP leakage. When no input data is applied, Fig. 6.3a shows the free running VCO frequency as a function of the positive static offset current $I_{os,pos,DC}$ across all the four VCO frequency bands. The offset current charges V_{int} from VEE to VCC, which in turn changes the VCO frequency. To set $V_{int} = \text{VCC}/2$, around $8\ \mu\text{A}$ of offset current must be injected to compensate for the output impedance mismatch of the CPs resistive divider ($R_{out,int}$). The overall VCO tuning range was measured from $24.6\ \text{GHz}$ to $28.5\ \text{GHz}$. Additionally, the frequency switching bands overlap with each other. Fig. 6.3b shows the measured phase noise plot of the free running VCO, with a phase noise of $-95\ \text{dBc}/\text{Hz}$ at a $1\ \text{MHz}$ offset. If the applied input data rate is outside the VCO band or acquisition range, the BBICDR fails to lock. However, the BBICDR can lock within the range of $24.6\text{--}28.5\ \text{Gbps}$ input data rate, resulting in a Figure of Merit (FoM) of $\approx 8.5\ \text{mW}/\text{Gbps}$.

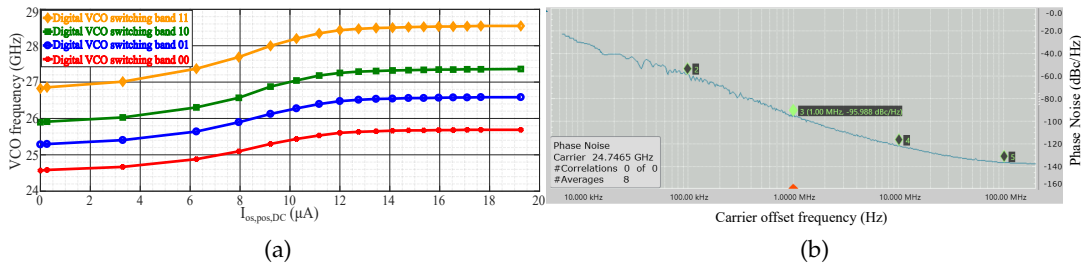


FIGURE 6.3: Measured free running VCO: (a) sensitivity due to positive static offset current, and (b) phase noise.

6.1.1 Frequency acquisition

For a particular VCO band, when the data rate lies within the acquisition range of the BBPD $\delta f_{acq,bb}$, the BBICDR locks onto the data. However, the VCO gain of the integral branch, $K_{v,int}$ varies for different offset currents (cf. Fig. 6.3a) which makes it difficult to calculate the exact locking range from (2.32).

Fig. 6.4a shows the measured frequency acquisition range for different values of integral branch CP currents $I_{cp,int}$ and positive static offset current $I_{os,pos}$. When no offset current ($I_{os,pos} = 0$) is applied, due to the CP leakage ($V_{int} = \text{VEE}$) and smaller $K_{vco,int}$, the measured acquisition range is less than half of the actual acquisition range of the BBICDR setting as per the calculations from (2.32). The acquisition range can be increased by shifting the V_{int} value closer to the center of the VCO switching band, where gain $K_{v,int}$ is at its maximum (similar to Example 3.6). For an offset

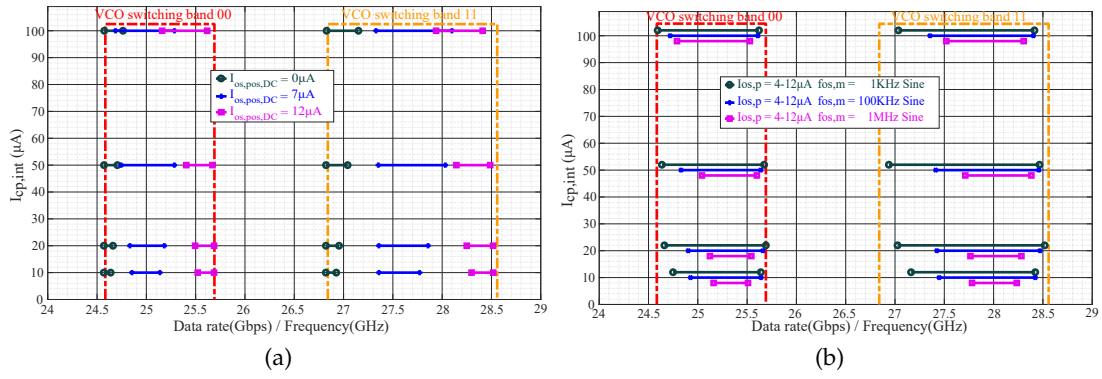


FIGURE 6.4: Acquisition range using (a) static offset current (b) modulated offset current. For improved readability only the lowest and highest VCO bands (00 and 11) are shown.

current $I_{os,pos} = 7 \mu\text{A}$, the maximum acquisition range is observed across all VCO bands. However, further increasing the offset current ($I_{os,pos} = 12 \mu\text{A}$) leads to lock the input data at upper limit of the VCO frequency band, where the $K_{v,int}$ gain is again minimized.

Next, as discussed in section 3.2.2, we can modulate the offset current so that the V_{int} value charges and discharges periodically between VCC and VEE. To ensure that the VCO gain remains large enough, the modulation current is varied within the range of $I_{os,p} = 4\text{--}12 \mu\text{A}$ (cf. Fig. 6.3). Outside of this range, the VCO gain decreases, limiting the VCO tunability and the integral branch is driven into a region where it no longer contributes to the PLL dynamics.

Fig. 6.4b shows the frequency acquisition range for different CP currents $I_{cp,int}$ and different modulated offset current frequencies ($f_{os,m}$). The acquisition range decreases as the modulation frequency increases. In addition, if the offset modulation amplitude satisfies $I_{os,pos} < I_{cp,int}$, the acquisition range is mainly determined by the frequency $f_{os,m}$ and is independent from $I_{cp,int}$, as discussed in Example 3.8.

The single-ended eye diagrams of the input and recovered data for the BBCDR operating at 25.781 25 Gbps with a PRBS9 test pattern and static offset current are shown in Fig. 6.5a. Similarly, the eye diagrams for the BBCDR operating at 25.38 Gbps PRBS9 test pattern with permanently modulated offset current are shown in Fig. 6.5b.

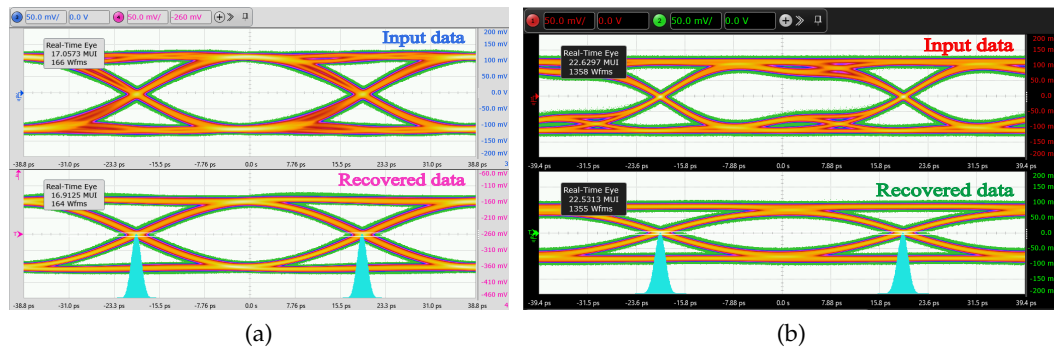


FIGURE 6.5: Measured single-ended input and recovered data eye diagrams at (a) 25.781 25 Gbps with static offset current, and (b) 25.38 Gbps with permanently modulated offset current amplitude $I_{os,p} = 4\text{--}12 \mu\text{A}$ and modulation frequency $f_{os,m} = 1 \text{ kHz}$ (sine wave).

The rms jitter generated by the BBCCR for no offset, static offset, and modulated offset currents are 334 fs, 336 fs and 342 fs, respectively. This indicates that permanent offset current modulation only marginally increases the clock phase error of the PLL in the locked state and could be used to increase the frequency acquisition range of BBCCR PLLs, without degrading JGEN.

6.1.2 Jitter characterization

First, the jitter characteristics using static offset current was conducted. Fig. 6.6a shows the measured and simulated JTF results for $I_{cp,prop} = 1.5$ mA, $I_{cp,int} = 5$ μ A and different input jitter amplitudes A_j . The measured maximum corner frequencies (f_{jc}), for which the output jitter follows the input jitter before it starts to decrease, is close to the simulated values. The simulated and measured transfer function peaking due to integral branch are 0.25 dB and 0.9 dB, respectively. The JTOL is measured, as proposed in OIF CEI-28G-VSR standard [76], by introducing a sinusoidal jitter to the input with PRBS9 test pattern while keeping the BER less than 10^{-7} . The results are shown in Fig. 6.6b-6.6c. At low jitter frequencies, as discussed in section 2.3.2, the jitter tolerance plot varies depending on the CP currents of both the proportional and integral branches, $I_{cp,prop}$ and $I_{cp,int}$ respectively. From Fig. 6.6c, at higher jitter frequencies the integral branch shows a small influence on the jitter tolerance.

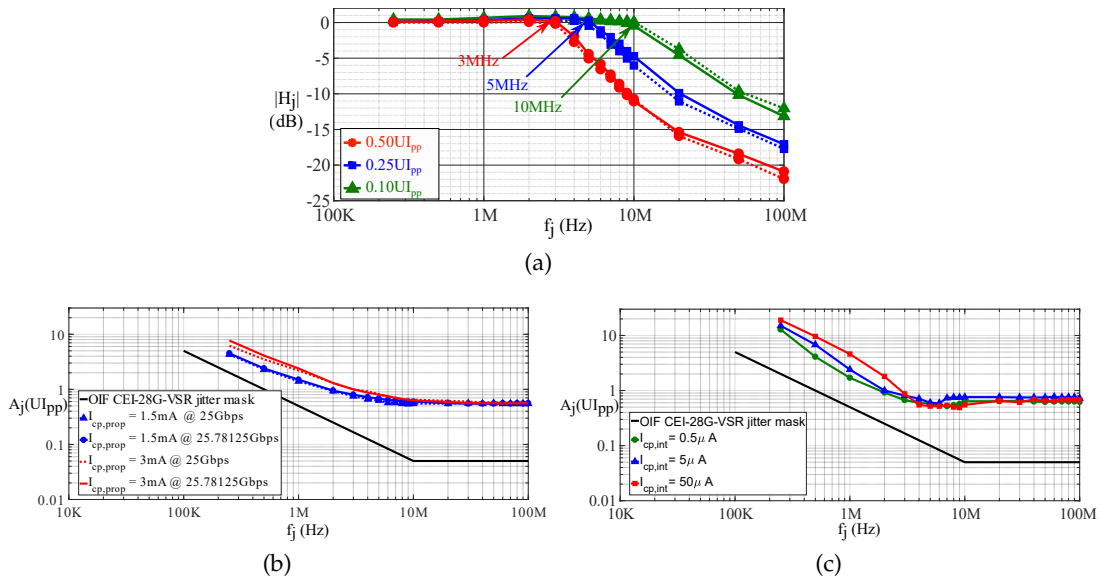


FIGURE 6.6: (a) MEASURED (solid lines) and simulated (dashed lines) JTF @ 25 Gbps with a PRBS9 test pattern for $I_{cp,prop} = 1.5$ mA, $I_{cp,int} = 5$ μ A and different A_j . Measured JTOL (b) with $I_{cp,int} \approx 0$, different $I_{cp,prop}$ values and data rates (c) At 25.78125 Gbps for $I_{cp,prop} = 1.5$ mA and different $I_{cp,int}$.

Next, the jitter characteristics is compared when the permanently modulated offset currents are used for acquisition. Fig. 6.7a shows the measured JTF characteristics for different CP integral current ($I_{cp,int}$). The jitter peaking increases with increase in the CP current ($I_{cp,int}$) and the maximum corner frequency is also shifted. The permanent low-frequency modulation of the offset current has only marginal influence. Fig. 6.7b shows the JTOL plots. The tolerance is better for the static offset current. However, with permanently modulated offset current the jitter tolerance specification is still satisfied.

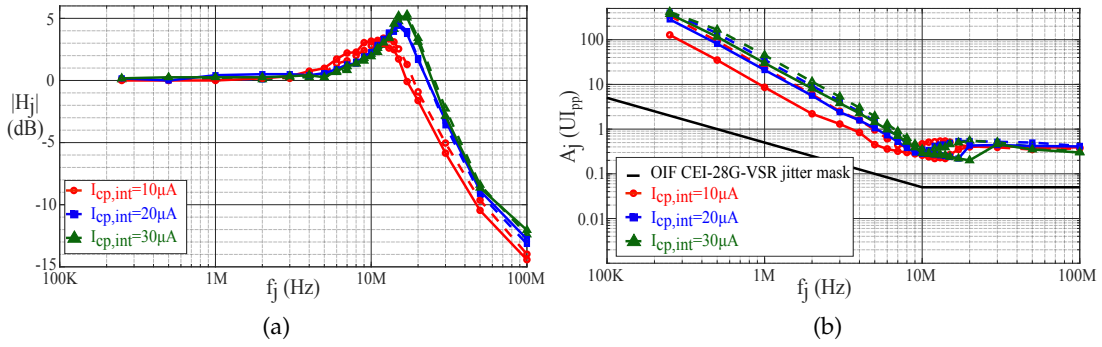


FIGURE 6.7: Measured @ 25.38 Gbps with a PRBS9 test pattern: (a) JTF for $A_j = 0.1 UI_{pp}$, and (b) JTOL. Both plots shown for a static offset current ($I_{os,pos,DC} = 10 \mu A$, dashed lines) and for a permanently modulated offset sine wave current ($I_{os,p} = 4\text{--}12 \mu A$, $f_{os,m} = 1 \text{ kHz}$, solid lines).

The spectrum and phase noise of the recovered clock with a static offset current are shown in Fig. 6.8a and Fig. 6.8c, respectively. The input data rate was set to 25 Gbps with an applied jitter of $A_j = 0.2 UI_{pp}$ and $f_j = 500 \text{ kHz}$. As a result, the recovered clock contains a fundamental frequency component at 25 GHz along with spectral components corresponding to the jitter frequency as described in (3.23). The measured peak-to-peak jitter of the recovered clock was 3.4 ps, while the rms jitter was 546 fs. When a modulated offset current with a frequency of $f_{os,m} = 70 \text{ kHz}$ is applied, additional spectral components associated with the modulation are also observed, as shown in Fig. 6.8b and Fig. 6.8d. A comparison of the phase noise plots for static and modulated offset currents reveals the presence of only one additional

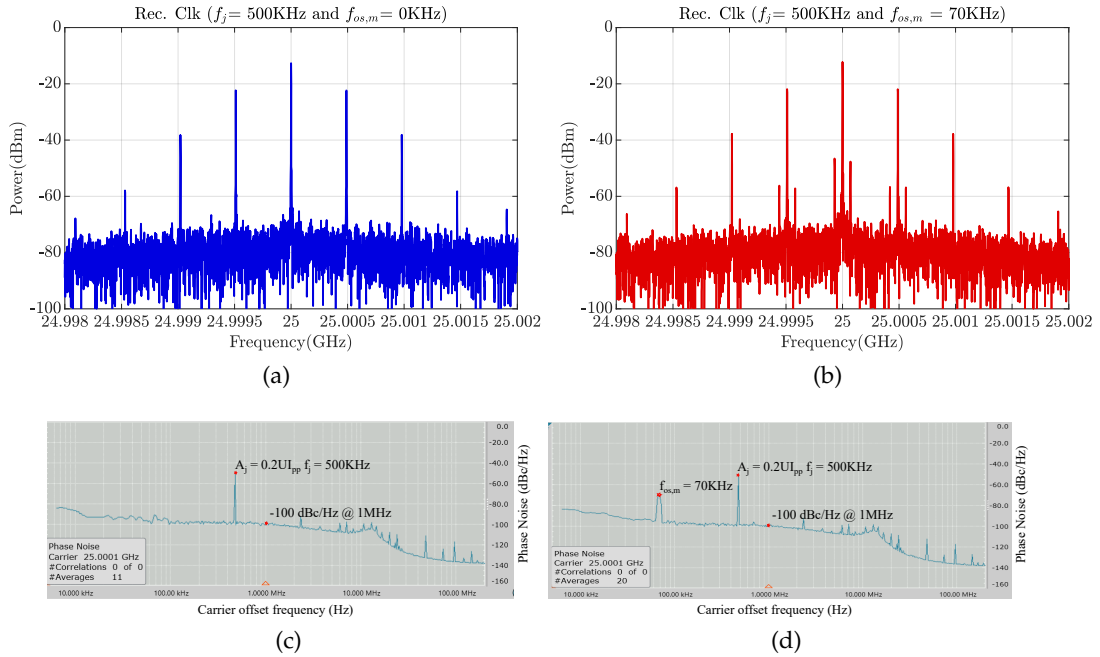


FIGURE 6.8: Measured recovered clock with static offset current: (a) spectrum, and (c) phase noise. With modulated offset current: (b) spectrum and (d) phase noise.

spectral component at a 70 kHz offset frequency. As discussed in section 3.2.3, the PLL also suppresses the magnitude of the modulation amplitude, A_{os} . The phase noise at a 1 MHz offset was measured at -100 dBc/Hz. The jitter introduced by the modulation frequency was negligible.

In summary, the acquisition range can be extended by subsequently shifting the VCO center frequency within a given VCO frequency band using static offset currents between 0 and $12 \mu\text{A}$, or by modulating the offset currents between $4 \mu\text{A}$ and $12 \mu\text{A}$ to cover the entire range within that band. The permanently modulated offset current used to increase the acquisition range had little impact on the phase noise of the recovered clock. In addition, digital switching of the VCO bands further extends the frequency acquisition range. This validates the novel acquisition technique used to enhance the acquisition range of the BBCDR by permanently modulating the offset current within the integral branch, as discussed in section 3.2.2.

6.2 28 Gbps BBCDR chip in 22FDXTM technology

The implemented architecture and chip microphotograph, fabricated using GFs 22FDXTM technology to characterize the 28 Gbps NRZ full-rate BBCDR, are shown in Fig. 6.9a and Fig. 6.9b, respectively. To digitally switch the VCO over four frequency bands, external pads, B_1 and B_2 were used. The BBCDR core area is 0.0884 mm^2 ;

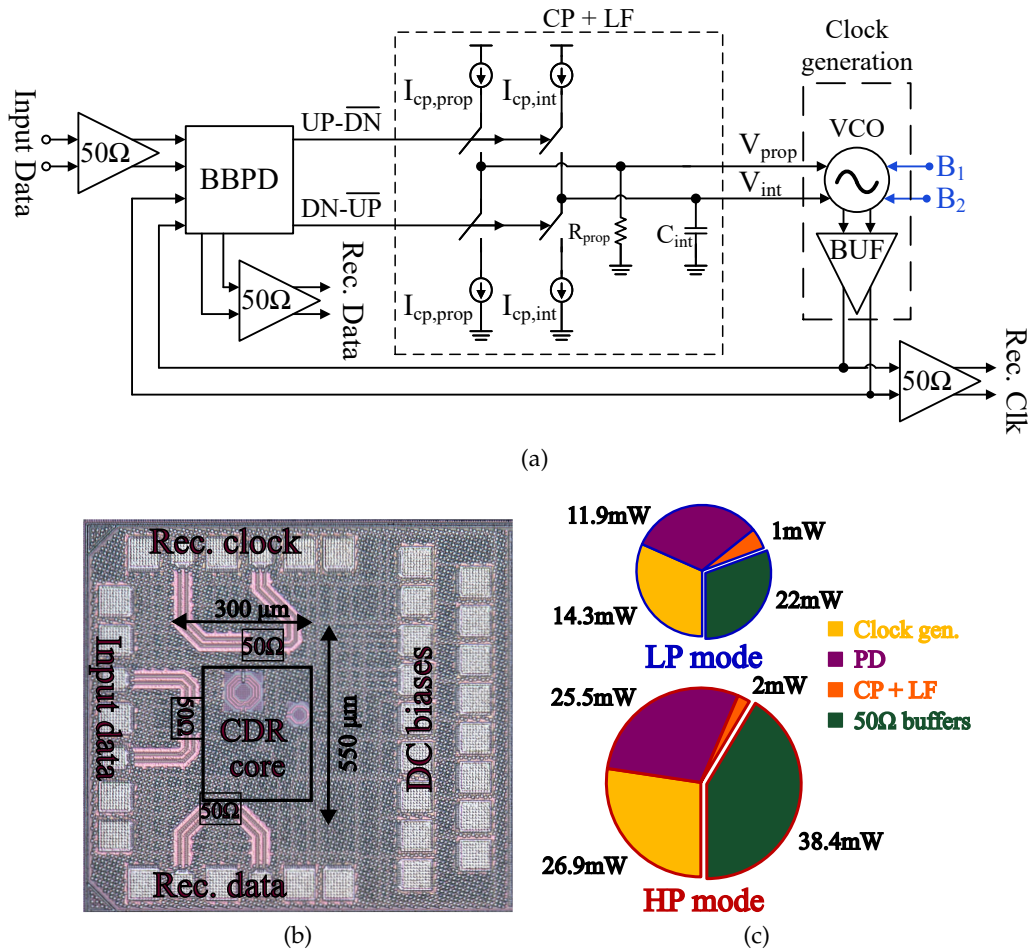


FIGURE 6.9: 28 Gbps NRZ full-rate BBCDR chip in 22FDXTM: (a) implemented architecture, (b) microphotograph, and (c) power breakdown.

including the 50Ω buffers, the area increases to 0.165 mm^2 , and the total chip area is 1 mm^2 . As shown in Fig. 6.9c, the core BBCDR dissipates 27.2 mW with 0.8 V supply (LP mode) and 54.4 mW with 1.2 V supply (HP mode). The 50Ω input and output buffers dissipate 22 mW and 38.4 mW in LP mode and HP mode, respectively.

In both modes, the VCO core supply was set to 0.8 V while the CP currents were set to $I_{cp,prop} = 400\text{ }\mu\text{A}$ for the proportional branch and $I_{cp,int} = 20\text{ }\mu\text{A}$ for the integral branch. The BBCDR can lock within the range of $26.9\text{--}28.2\text{ Gbps}$ input data rate, resulting in a FoM of $\approx 0.97\text{ mW/Gbps}$ in LP mode and $\approx 1.94\text{ mW/Gbps}$ in HP mode. The BBCDR was further characterized with a focus on the variation of the BBPD gain across both operating modes, as observed in Fig. 5.4.

6.2.1 Frequency acquisition

Fig. 6.10 shows the spectrum of the recovered clocks in different VCO bands in LP and HP modes. For clarity, markers are used to represent the inherent acquisition ranges ($\delta f_{acq,bb}$) of the BBCDR, rather than the overlapping frequency sensitivity bands of the VCO, which are not shown. The overlapping sensitivity can be found in the simulation results shown in Fig. 5.8c. In LP mode, markers $M1 - M2$, $M3 - M4$, $M5 - M6$, and $M7 - M8$ indicate the acquisition range when $B_1 - B_2$ are set to 00, 01, 10 and 11, respectively. Similarly, in HP mode, markers $M9 - M10$, $M11 - M12$, $M13 - M14$, and $M15 - M16$ indicate the acquisition range when $B_1 - B_2$ are set to 00, 01, 10 and 11 respectively. A spectrum of the recovered clock is provided for each band. Compared to LP mode, an increase in the acquisition range of each frequency band in HP mode is observed.

The recovered clock and data in both modes are shown in Fig. 6.11. In LP mode, the bandwidth limitation of the 50Ω output buffers and the 1 m measurement cables introduce 1 dB loss, resulting in reduced amplitude and increased intersymbol interference (ISI). At a recovered clock frequency of 27.6 GHz , the amplitude decreases from 150 mV_{pp} in HP mode to 90 mV_{pp} in LP mode, with the rms jitter increasing from 246 fs (HP mode) to 321 fs (LP mode). Similarly, at a recovered data rate of 27.6 Gbps , the amplitude decreased from 400 mV_{pp} (HP mode) to 300 mV_{pp} (LP mode), with the rms jitter increasing from 270 fs (HP mode) to 365 fs (LP mode). The ISI also doubles, increasing from 6.8 ps (HP mode) to 13.07 ps (LP mode).

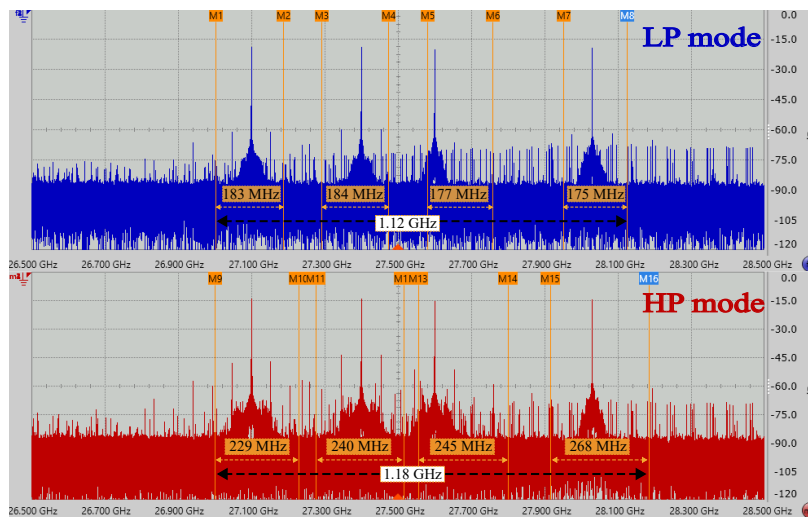


FIGURE 6.10: Measured acquisition ranges of BBCDR in LP and HP modes.

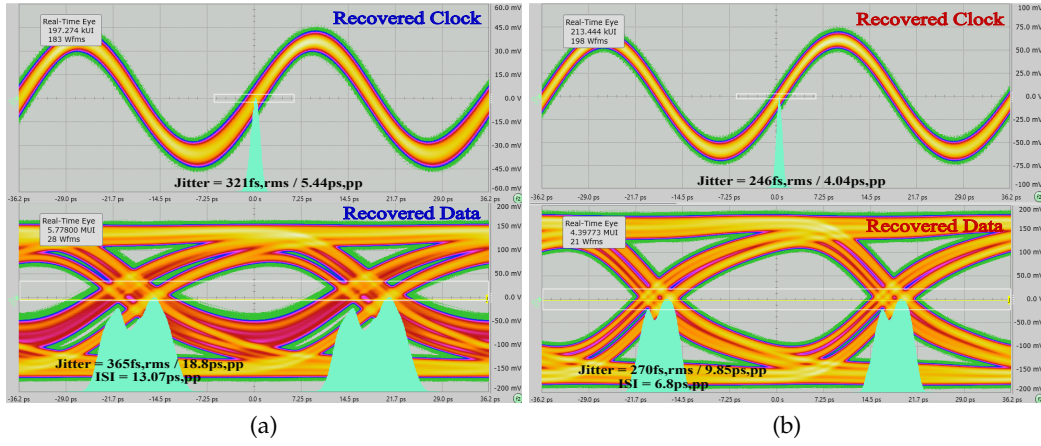


FIGURE 6.11: Recovered clock and data applying 27.6 Gbps PRBS15 input data in (a) LP mode (b) HP mode.

In a high-speed serial-link receiver, an equalizer is often used to receive the data with reasonable BER [67]. Therefore, incorporating an equalizer or using a bandwidth peaking technique in the 50 Ω output buffers would improve ISI.

6.2.2 Jitter characterization

The chip was characterized at 27.1 Gbps input data rate with PRBS9 test pattern. The measured JTF of the recovered data was evaluated as a function of the applied jitter frequency (f_j) for an input jitter amplitude of $A_j = 0.2 \text{ UI}_{pp}$, as shown in Fig. 6.12a. The corner frequency varied between 34 MHz in HP mode and 22 MHz in LP mode, which can be attributed to the variation in BBPD gain. In addition, the jitter peak increased from 3 dB in LP mode to 4 dB in HP mode. Fig. 6.12b shows the JTOL plots for both LP and HP modes, with the BER maintained below 10^{-12} . The tolerance is higher in HP mode due to the improved BBPD gain. Nevertheless, the jitter tolerance was still satisfied with a good margin for both modes.

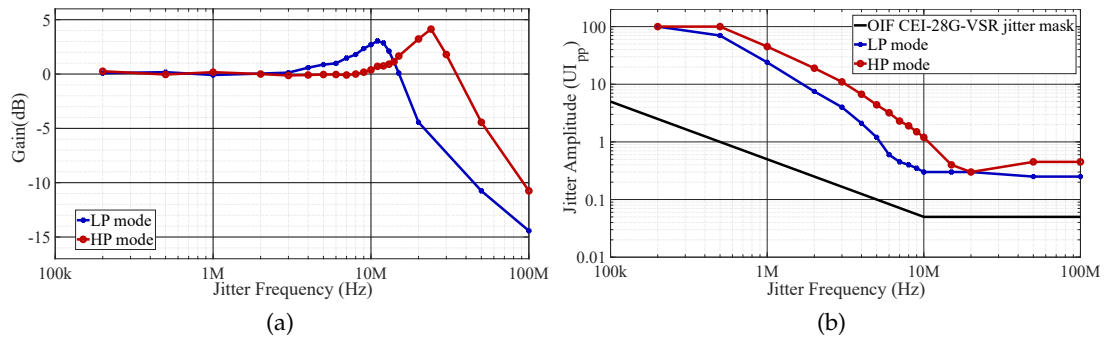


FIGURE 6.12: Measured jitter characteristics applying 27.1 Gbps PRBS9 input data in both modes: (a) JTF for $A_j = 0.2 \text{ UI}_{pp}$ (b) JTOL.

A sinusoidal input jitter ($A_j = 0.2 \text{ UI}_{pp}$, $f_j = 4 \text{ MHz}$) was applied to the input data at 28.03 Gbps. The phase noise of the recovered clocks at 28.03 GHz in both LP and HP modes is shown in Fig. 6.13. The integrated jitter (from 10 kHz to 1 GHz) of the recovered clock, without jitter applied to the input data, was measured to be 266.6 fs, rms and 211.4 fs, rms for LP and HP modes, respectively.

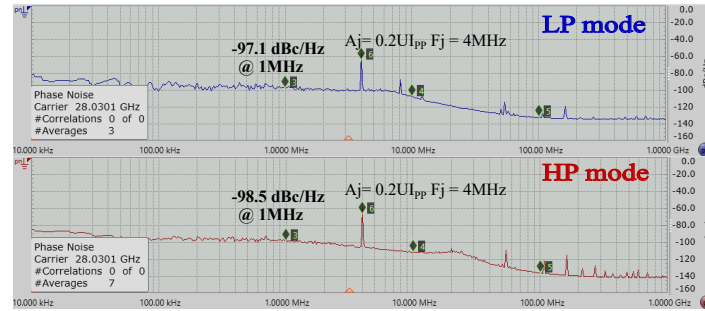


FIGURE 6.13: Phase noise of the recovered clock applying 28.03 Gbps PRBS9 input data with jitter.

In summary, the BBCDR measurements were conducted for LP mode and HP mode. The frequency acquisition was achieved through digital switching of the VCO frequency bands. The BBCDR was characterized in both modes, each demonstrating a good jitter tolerance margin. The FoM was reduced by half, from 1.96 mW/Gbps in HP mode to 0.97 mW/Gbps in LP mode. Furthermore, compared to the BBCDR designed in section 6.1, the FoM improved ninefold, from 8.5 mW/Gbps in SG25H4 to 0.97 mW/Gbps in 22FDXTM. In addition, the BBCDR core area, including 50 Ω buffers, was reduced threefold, from 0.51 μm^2 in SG25H4 to 0.165 μm^2 in 22FDXTM.

6.3 50 Gbps BBCDR chip in SG13G3 technology

The implemented architecture fabricated using IHPs SG13G3 technology to characterize the 50 Gbps NRZ full-rate BBCDR, is shown in Fig. 6.14a. The applied external offset voltage V_{os} , which controls the varactor, and an offset current $I_{os} = 0\text{--}20\text{ }\mu\text{A}$ were used to tune the VCO center frequency. In the CP, the output impedance of the N_2 transistor was designed to be smaller than that of the P_4 transistor (cf. Fig. 4.5b). Consequently, V_{int} tends to discharge towards VEE due to CP leakage, potentially pushing it out of the VCOs linear tuning range. Therefore, only a positive offset current is required. The modulation of both V_{os} and $I_{os,pos}$, applied via external pads, was used to extend the acquisition range and its effects were analyzed. The CP currents remained fixed - regardless of whether modulation was applied or not - at $I_{cp,prop} = 250\text{ }\mu\text{A}$ for the proportional branch and $I_{cp,int} = 10\text{ }\mu\text{A}$ for the integral branch. $R_{prop} = 100\text{ }\Omega$ and $C_{int} = 10\text{ pF}$ were chosen.

Fig. 6.14b shows the chip microphotograph. Input data, recovered clock and data were successfully probed. The BBCDR core area is 0.225 mm^2 ; including the 50 Ω buffers, the area increases to 0.25 mm^2 , and the total chip area is 1.5 mm^2 . As shown in Fig. 6.14c, the core BBCDR dissipates 245 mW from a 3.3 V supply, and the 50 Ω input and output buffers consume an additional 160 mW from the same supply. 50 Ω input and output buffers without inductive peaking have been implemented for testing purposes, similar to the circuits mentioned in [50, 52].

The frequency sensitivity of the free-running VCO was measured using the offset controls. Fig. 6.15a shows the analog tuning obtained by static control of the offset voltage $V_{os,DC}$, while Fig. 6.15b shows the tuning obtained by static control of the positive offset current $I_{os,pos,DC}$. The VCO sensitivity to the offset voltage ($k_{v,os}$) was deliberately set to be one-third of its sensitivity to the integral branch ($k_{v,int}$). This design choice ensures that the upper bound constraint defined in (3.10) is not violated while effectively utilizing the acquisition technique. Compared to the simulations, the measured tuning sensitivity range remained almost the same, while the nominal

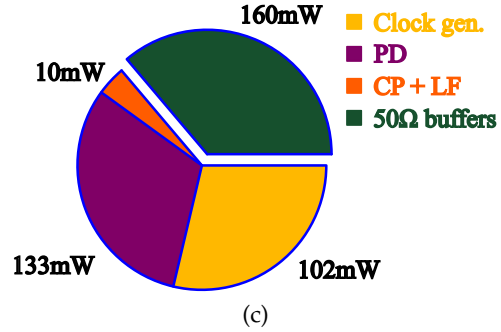
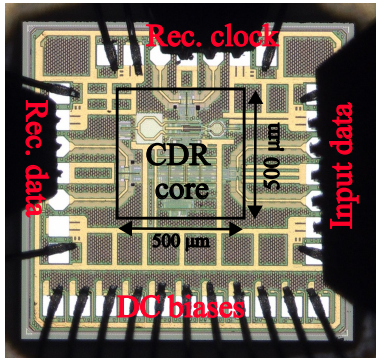
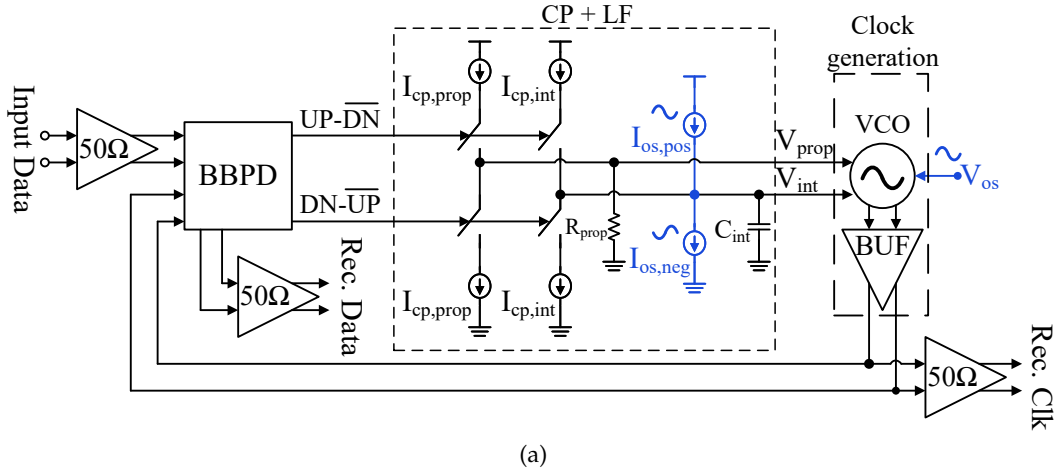


FIGURE 6.14: 50 Gbps NRZ full-rate BBCCR chip in SG13G3: (a) implemented architecture, (b) microphotograph, and (c) power breakdown.

VCO frequency shifted by approximately 1.5 GHz. The overall VCO tuning range was measured from 49 GHz to 52.3 GHz. The BBCCR successfully locked within an input data rate range from 49 Gbps to 52.3 Gbps, achieving a FoM of ≈ 4.68 mW/Gbps.

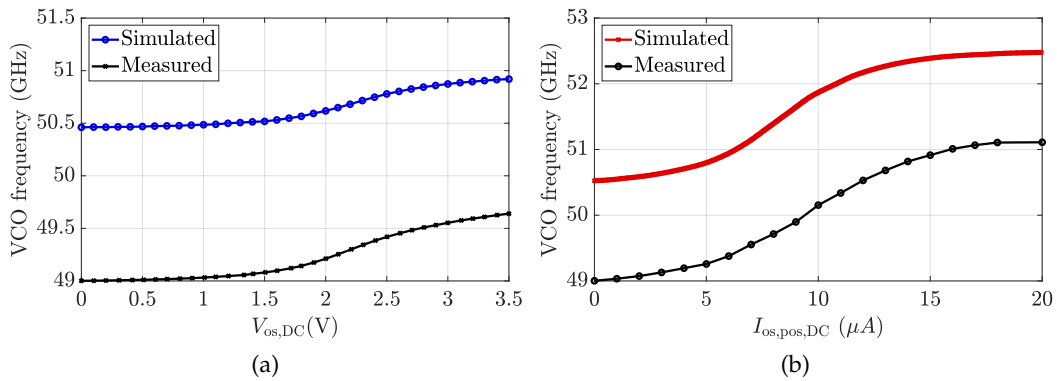


FIGURE 6.15: Simulated and measured free-running VCO sensitivity with static offset: (a) voltage (b) current.

6.3.1 Frequency acquisition

The acquisition range was measured under three conditions: without offset modulation, with permanent offset voltage (V_{os}) modulation, and with permanent offset current (I_{os}) modulation, as shown in Fig. 6.16. For simplicity, the spectra of the recovered clock are shown for the minimum and maximum acquisition of the input data rates for each case. Without offset modulation, the measured inherent acquisition range of the BBCDR was $\delta f_{acq,bb} = 270$ MHz, covering 49.05 GHz to 49.32 GHz. A permanent offset voltage modulation was applied with an amplitude $V_{os,p} = 1.5$ – 3.5 V and a frequency $f_{os,m} = 20$ kHz. This modulated the free-running VCO by $f_{vos,pp} = 700$ MHz. As a result, the measured acquisition range nearly quadrupled to $\delta f_{acq,vos} = 1$ GHz, acquiring from 49.25 GHz to 50.25 GHz. This result validates the derived equation in (3.8). For this $f_{vos,pp} = 700$ MHz setting, the maximum applicable $f_{os,m}$ that maintains the condition in (3.7) without reducing the acquisition range is 430 kHz, corresponding to an acquisition time of $t_{acq,os} = 2.3$ μ s, in accordance to (3.9). Similarly, a permanent offset current modulation was applied with an amplitude $I_{os,pos} = 5$ – 15 μ A and a frequency $f_{os,m} = 10$ kHz. This modulates the free-running VCO by $f_{ios,pp} = 2$ GHz. Consequently, the acquisition range was extended nearly eightfold to $\delta f_{acq,ios} = 2.27$ GHz, spanning from 49.3 GHz to 51.57 GHz. This result validates the derived equation in (3.18). For this $f_{ios,pp} = 2$ GHz setting, the maximum applicable $f_{os,m}$ that maintains the condition in (3.17) without reducing the acquisition range is 150 kHz, corresponding to $t_{acq,os} = 6.6$ μ s. Moreover, applying a static offset voltage of $V_{os,DC} = 3.5$ V together with permanent offset current modulation shifts the acquisition range, enabling clock recovery up to 52.3 GHz (corresponding to 52.3 Gbps data rate).

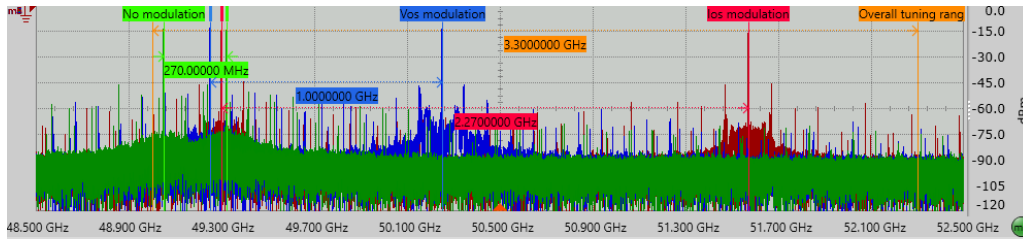


FIGURE 6.16: Measured acquisition ranges without modulation, with offset voltage (V_{os}) modulation, and with offset current (I_{os}) modulation.

6.3.2 Jitter characterization

The chip was characterized at a 49.7 GHz input data rate using a PRBS9 test pattern for the same three conditions. First, the JTF was evaluated as a function of different jitter frequencies with applied jitter amplitude of $A_j = 0.2$ UI_{pp}, as shown in Fig. 6.17a. Permanent offset voltage modulation increased the jitter peaking around the corner frequency by 1 dB, while permanent offset current modulation had negligible effect on the jitter peaking. Next, the JTOL was evaluated according to the OIF CEI-56G-VSR jitter specification [76]. The results are shown in Fig. 6.17b, ensuring a BER of less than 10^{-12} . The JTOL is better for the permanent offset current modulation. However, under all three conditions, the jitter tolerance remains unaffected and is above the jitter tolerance mask.

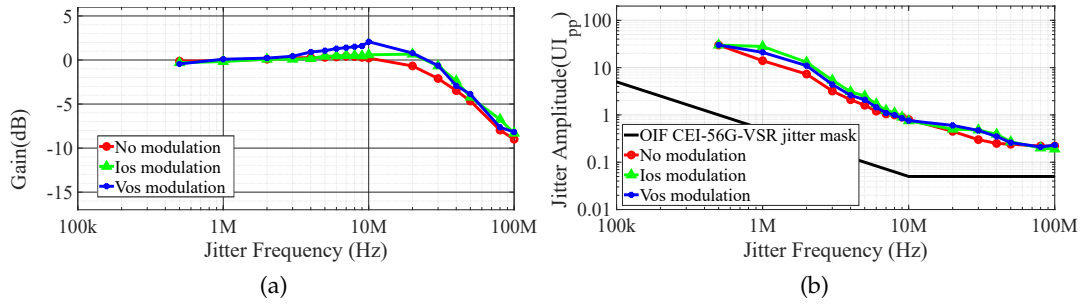


FIGURE 6.17: Measured jitter characteristics applying 49.7 Gbps PRBS9 input data: (a) JTF, and (b) JTOL.

Fig. 6.18a presents the applied jitter-free input data signal at 51.5625 Gbps with a PRBS9 test pattern along with the recovered data eye diagrams with permanent offset current modulation. The rms jitter of the recovered clock was measured to be 201 fs while the phase noise at a 1 MHz offset was -105 dBc/Hz. When sinusoidal jitter with an amplitude of $A_j = 0.2 \text{ UI}_{pp}$ and $f_j = 2$ MHz was embedded in the same input data, the corresponding eye diagrams are shown in Fig. 6.18b.

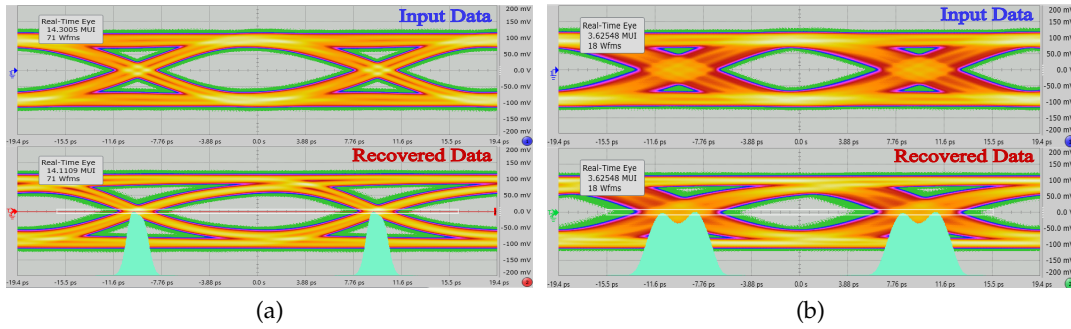


FIGURE 6.18: Eye diagrams with permanent offset current modulation and applying 51.5625 Gbps PRBS9: (a) no jitter applied, (b) $A_j = 0.2 \text{ UI}_{pp}$ and $f_j = 2$ MHz applied.

The spectrum of the recovered clock with a permanently modulated offset current with a frequency $f_{os,m} = 30$ kHz is shown in Fig. 6.19a. The input data rate was set to 49.5 Gbps, with an applied jitter of $A_j = 0.2 \text{ UI}_{pp}$ and $f_j = 607$ kHz. As a result, the recovered clock contains a fundamental frequency component at 49.5 GHz along with spectral components at $f_{os,m}$ and f_j as described by (3.23). This validates the claim that the PLL suppresses the magnitude of the modulation amplitude A_{os} , while the jitter amplitude A_j is preserved for this applied jitter frequency. Fig. 6.19b shows the phase noise plot when the applied data rate was changed to 49.7 Gbps, with $f_{os,m} = 150$ kHz and $f_j = 2$ MHz. Also shown is the phase noise of the free-running VCO is shown, where the phase noise at a 1 MHz offset was measured to be -85 dBc/Hz. The integer multiples of higher-order sideband spectral components resulting from the offset modulation are also clearly visible again in steady state.

In summary, the acquisition range can be extended by permanently modulating the offset currents within the integral branch or by permanently modulating the offset voltage of the VCO externally. This also confirms the novel acquisition technique discussed in section 3.2. The data rate was increased twice from 28 Gbps to 50 Gbps by changing the technology node. At the same time, the FoM was reduced half, from

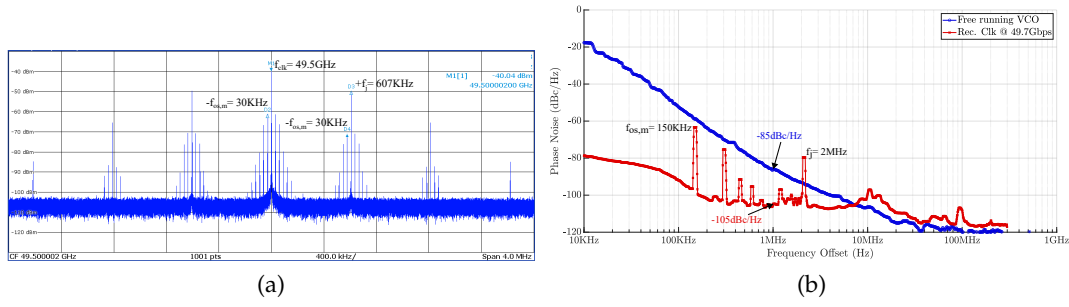


FIGURE 6.19: Measured recovered clock: (a) spectrum, and (b) phase noise with different modulation and jitter frequencies.

8.5 mW/Gbps in SG25H4 to 4.68 mW/Gbps in SG13G3. In addition, the BBCDR core area, including 50 Ω buffers, was reduced half, from 0.51 μm^2 in SG25H4 to 0.25 μm^2 in SG13G3.

6.4 Summary and conclusion

Measurements were performed on full-rate NRZ BBCDR chips fabricated in IHPs SG25H4, GFs 22FDXTM, and IHPs SG13G3. The presented results address diverse application perspectives while maintaining a high-speed design approach. The novel acquisition technique discussed in section 3.2 has been experimentally validated, demonstrating its effectiveness. This technique exhibits minimal impact on the BBCDR PLL, ensuring compliance with the stringent jitter specifications as defined by industry standards.

The permanently modulated offset automates the frequency acquisition process and contributes negligibly to the phase noise of the recovered clock. Additionally, its power consumption overhead is minimal, making it a power-efficient solution. Transitioning to the GFs 22FDXTM technology further targets low power dissipation by leveraging its back-gate biasing feature.

These measurement results underscore the scalability and adaptability of the proposed designs across different technology nodes, reinforcing their suitability for next-generation high-speed serial link applications. Partial results from this chapter have been published in [21–24].

Chapter 7

Conclusion and Outlook

In this thesis, we first discussed the need for Clock and Data Recovery (CDR) circuits in optical transceiver systems. We classified various CDR circuits and explained our choice of the Alexander Phase Detector (PD) topology for high-speed, full-rate operations to recover the clock and retune random data. We developed a behavioral model of the bang-bang Phase-Locked Loop (PLL), focusing on the independent tunability of the Loop Filter (LF) parameters using proportional and integral branch parameters. However, due to the insufficient acquisition range of the PLL, a novel frequency acquisition technique was introduced, along with derived conditions and limitations necessary for successfully increasing the acquisition range. In addition, three chips were designed using three different technologies tailored to different application perspectives. Each BBCDR chip has been characterized and the results have been published.

7.1 Comparison with the state of the art

Table 7.1 presents a comparison of the full-rate NRZ BBCDRs developed in this work against existing state-of-the-art designs operating above 20 Gbps using NRZ modulation. The 28 Gbps full-rate NRZ BBCDR implemented in 22FDXTM achieves the best FoM among all full-rate NRZ CDRs reported. Notably, its FoM approaches those of half-rate and quarter-rate NRZ CDR architectures but with significantly lower circuit complexity. Only publications with measurement results are considered here; for instance, [67] and [68] report full-rate designs with few measurement results but do not include jitter tolerance data.

The majority of prior designs are implemented using CMOS technology, where power consumption is primarily dynamic. In contrast, our design is based on CML circuits, leveraging the high-speed capabilities of HBTs in SiGe BiCMOS technology, where power consumption is dominated by static bias currents. This approach was chosen to facilitate the implementation of CDR circuits suitable for EPIC and hybrid IMDD transceivers, where both speed and minimal interconnect lengths are critical.

It is important to highlight that half-rate and quarter-rate approaches [77–79] achieve power savings primarily by reducing the number of flip-flops used in phase detection. However, this reduction leads to a loss of phase information during certain data transitions, thereby decreasing the phase detector gain and ultimately limiting the tracking bandwidth (see Appendix B for details).

References featuring PAM4 architectures with similar throughputs have been excluded from this comparison.

	[77]	[78]	[79]	[67]	[68]	22FDX TM [23]		SG25H4[21, 22]	SG13G3[24]
						LP mode	HP mode		
Technology	28 nm CMOS	65 nm CMOS	40 nm CMOS	90 nm CMOS	65 nm CMOS	22 nm FD-SOI CMOS		250 nm SiGe BiCMOS	130 nm SiGe BiCMOS
Clock architecture	Half-rate	Quarter-rate	Quarter-rate	Full-rate	Full-rate	Full-rate		Full-rate	Full-rate
PD type	Bang-Bang	Bang-Bang	Bang-Bang	Bang-Bang	Bang-Bang	Bang-Bang		Bang-Bang	Bang-Bang
Data Rate (Gbps)	56	34.2	32	40	25	28		28	50
Supply (V)	-	1	1.1	1.8/1.5	0.6	0.8	1.2	3.3/2.5	3.3
Rec. clock	28.5 GHz 500 fs, rms	9.15 GHz 957.7 fs, rms 19.76 ps, pp	8 GHz 1.99 ps, rms 15.4 ps, pp	300 fs, rms 4.3 ps, pp	25 GHz 230 fs, rms 4.62 ps, pp	28.03 GHz	28.03 GHz	28 GHz 546 fs, rms 3.4 ps, pp	51.5625 GHz 201 fs, rms
Phase noise Rec. clock	-110 dBc/Hz @1 MHz offset	-114 dBc/Hz @10 MHz offset	-	-	-119.49 dBc/Hz @10 MHz offset	-97.1 dBc/Hz @1 MHz offset	-98.5 dBc/Hz @1 MHz offset	-100 dBc/Hz @1 MHz offset	-105 dBc/Hz @1 MHz offset
Rec. data	14.25 Gbps	9.15 Gbps	8 Gbps	40 Gbps 9.6 ps, pp	25 Gbps 0.91 ps, pp 7.62 ps, pp	27.6 Gbps 365 fs, rms 18.8 ps, pp	27.6 Gbps 270 fs, rms 9.85 ps, pp	28.3 Gbps 342 fs, rms	51.5625 Gbps
Core area (mm ²)	0.06875	0.0827	0.041	-	0.39	0.0884		0.3375	0.225
Core power (mW)	33.3	45.65	30.8	57	39.9	27.2	54.4	240	245
FoM (mW/Gbps)	0.59	1.33	0.96	1.43	1.60	0.97	1.94	8.57	4.68
Jitter Tolerance	Yes	Yes	Yes	No	No	Yes	Yes	Yes	Yes

TABLE 7.1: CDR performance comparison.

7.2 Outlook

A promising subsequent step is the extension of the proposed offset-modulated acquisition techniques to higher data rates using half-rate or quarter-rate architectures, particularly for advanced IMDD formats. The application of offset-based acquisition to multi-level signaling, such as PAM-4, is particularly compelling, as the associated nonlinear detector behavior and complex error dynamics remain largely unexplored.

Further opportunities arise from circuit-level innovation. Recent demonstrations employing TSPC flip-flops have demonstrated the viability of substantial power savings and operation beyond 60 Gbps [80]. The integration of these flip-flop architectures with the proposed acquisition scheme has the potential to facilitate highly power-efficient design in 22FDXTM. Additionally, new device features in the 22FDXTM technology platform [63], most notably the availability of SiGe HBTs, has opened the door to hybrid CMOS–bipolar CDR designs. These designs have the potential to offer enhanced speed, gain, or noise performance.

Another significant direction in this field is system-level validation. The integration of the acquisition technique into a comprehensive optical transceiver chain, encompassing the driver, modulator, TIA, and photodiode co-design, will facilitate the quantification of its benefits in realistic short-reach or co-packaged optical systems.

Together, these paths highlight the potential of offset-modulated acquisition to enable future high-speed, low-power, and scalable CDR solutions, while motivating continued research into architectures tailored for next-generation optical interconnects.

Appendix A

Jitter terminology

Comprehensive mathematical models and detailed descriptions of jitter types are provided in [81]. In optical communication systems, observed jitter results from multiple contributing sources that collectively form the total jitter, as discussed in Chapter 2. Figure A.1 illustrates the classification of total jitter. Bounded jitter has a finite peak-to-peak amplitude and does not increase indefinitely with observation time. In contrast, unbounded jitter can theoretically grow without limit over time, typically following a Gaussian distribution. Jitter can be categorized based on the shape of its Probability Density Function (PDF) histogram into two main types:

- **Deterministic Jitter (DJ):** Bounded jitter with a finite peak-to-peak value. DJ can be further subdivided into:
 - *Data-Dependent Jitter (DDJ)*: Jitter that depends on the transmitted bit pattern. It is finite for specific patterns and run lengths. ISI caused by bandwidth limitations can be characterized or separated using mathematical models of the PDF.
 - *Duty Cycle Distortion Jitter (DCD)*: Arises from asymmetry between the rising and falling edges of the recovered clock. This jitter can also be characterized and separated via PDF-based models. In full-rate CDR architectures, where data is retimed only on rising edges, DCD can generally be neglected. However, half-rate or quarter-rate architectures require explicit consideration of DCD.
 - *Sinusoidal Jitter (SJ)*: Intentionally applied jitter with a sinusoidal waveform, often used for jitter tolerance testing.
 - *Bounded Uncorrelated Jitter (BUJ)*: Results from crosstalk with adjacent data links or on-chip random switching noise. When caused by independent

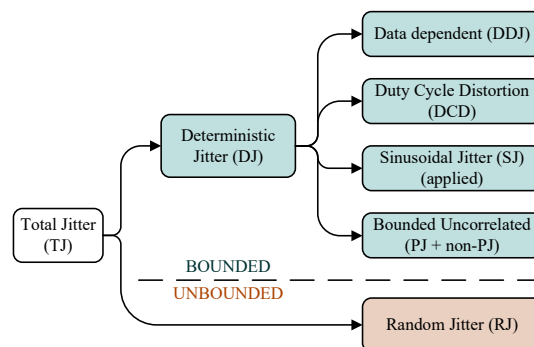


FIGURE A.1: Classification of jitter terminology and their interrelationships.

sources, BUJ can be modeled as a sum of independent PJs, which are deterministic jitters with periodic waveforms.

- **Random Jitter (RJ):** Unbounded jitter typically caused by device noise. Its PDF follows a Gaussian distribution, and its variance increases with observation time. RJ cannot be eliminated through design but must be accounted for to meet target BER.

As described in [81], when multiple uncorrelated components of RJ and DJ are present, the total RJ variance is the sum of the variances of the individual RJ components:

$$\sigma_{\text{total}}^2 = \sigma_{j1}^2 + \sigma_{j2}^2 + \dots + \sigma_{jn}^2 \quad (\text{A.1})$$

In contrast, the total DJ is the linear sum of the individual DJ components:

$$DJ_{\text{total}} = DJ_{j1} + DJ_{j2} + \dots + DJ_{jn} \quad (\text{A.2})$$

Decomposing the total jitter into its constituent components during measurement is essential for identifying dominant jitter sources and developing targeted mitigation strategies. One widely used approach for this decomposition is the *tail fitting method*. For further details, refer to [81]. The bathtub curve is a common visualization tool in jitter analysis, typically generated by real-time oscilloscopes or BER testers, as shown in Fig. A.2. The instrument records the received data and constructs an eye diagram along with a timing jitter histogram. By sweeping the sampling point across the UI, the BER is measured and plotted as a function of sampling time within the bit period. Near the edges of the UI, deterministic jitter tends to dominate the BER performance, whereas near the center of the eye, random jitter is the primary contributor. Due to memory limitations in measurement instruments, BER can only be recorded down to a certain threshold; beyond this, BER values are extrapolated based on the slope of the bathtub curve.

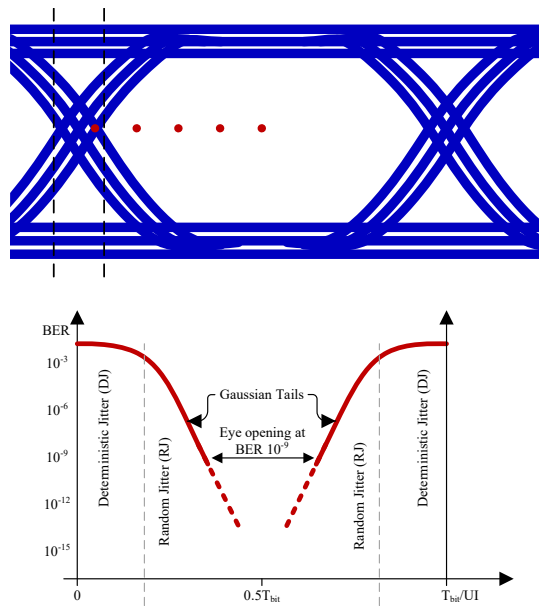


FIGURE A.2: Illustration of bathtub curve

Appendix B

Alexander half-rate NRZ PD and full-rate PAM4 PD

Half-rate Alexander NRZ PD

Fig. B.1 shows the modified Alexander half-rate NRZ PD. To replicate the phase detection behavior of the full-rate implementation (as in Fig. 2.4a), the half-rate design requires more flip-flops and XOR gates. While halving the clock speed reduces frequency demands, it also increases clock loading and routing complexity, since Clk_{90} must now drive additional flip-flops. The recovered data is asynchronously demultiplexed using both the rising and falling edges of Clk_0 .

Fan et al. [29] introduce two additional flip-flops to handle pipelined sampling. In contrast, other authors have proposed half-rate architectures with only six flip-flops, omitting the falling edge of the quadrature clock (responsible for sampling the transition at S_4). Atharav et al. [77] further reduce power by using only three flip-flops, though this comes at the cost of losing flip-flop output alignment for phase detection. However, these approaches may result in loss of phase information during certain transitions and reduce tracking bandwidth. Although such simplifications lower power consumption, generating the quadrature clock still incurs additional power overhead.

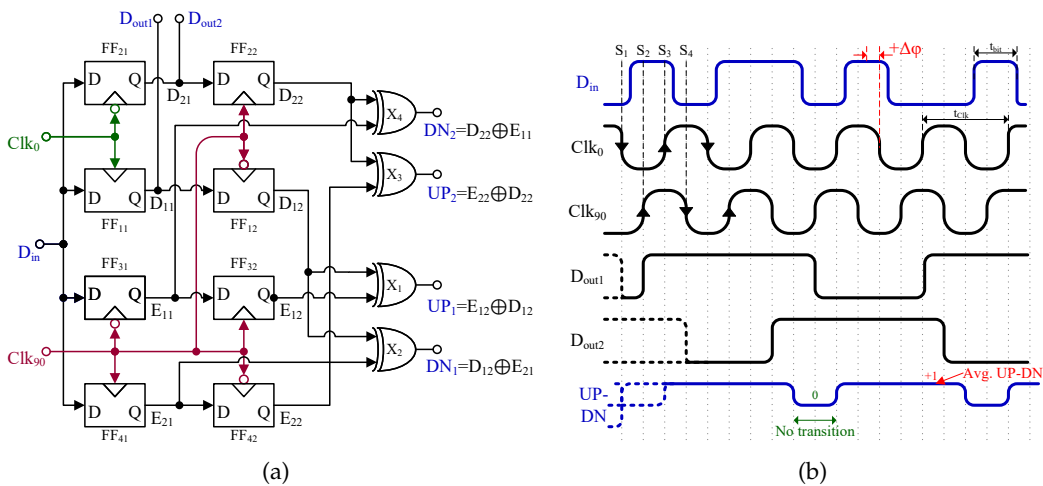


FIGURE B.1: Modified Alexander half-rate NRZ PD: (a) schematic and (b) waveform (clock late).

Full-rate Alexander PAM4 PD

One of the earlier implementations of the Alexander full-rate PAM4 PD is discussed by [30]. A modified version is shown in Fig.B.2. A PAM4 signal features four discrete levels, resulting in 12 possible transitions (e.g., $-1 \leftrightarrow +1$, $-1 \leftrightarrow -1/3$, etc.). Transitions between adjacent levels are considered symmetric and generally introduce less jitter, as they involve smaller voltage steps and faster slew rates, making them suitable for accurate clock recovery[13]. In contrast, transitions between non-adjacent levels are asymmetric, requiring larger amplitude changes and resulting in

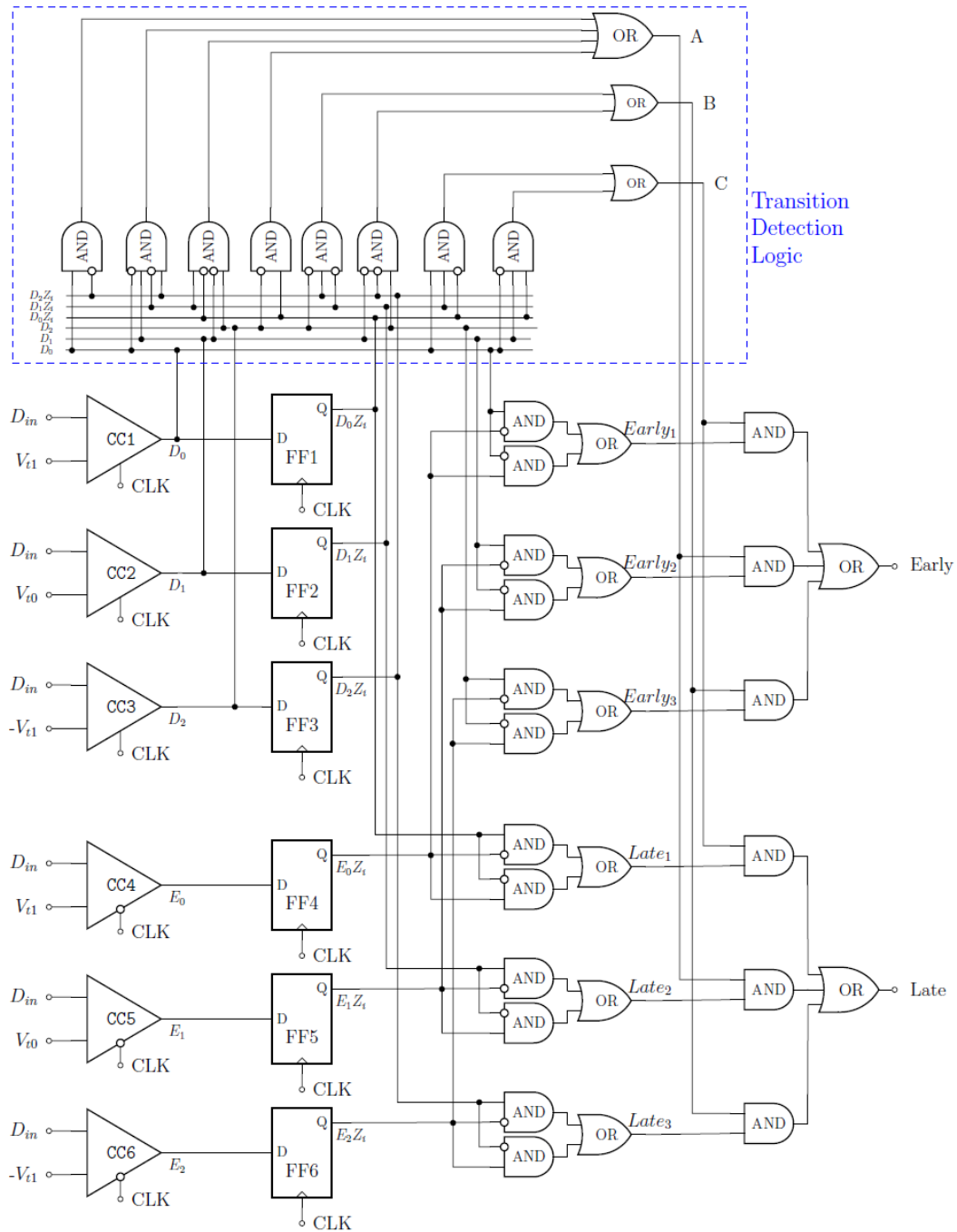


FIGURE B.2: Modified Alexander full-rate PAM4 PD schematic.

longer slew times. These asymmetric transitions increase timing uncertainty and contribute more jitter. Additionally, variations in signal edge shapes and slew rates can further worsen the overall jitter performance. Clocked comparators (CC) are used to quantize the multi-level PAM4 signal at well-defined thresholds, thereby reducing data-dependent jitter from asymmetric transitions and enabling reliable transition detection. A transition detector is required to filter out these asymmetric transitions. Furthermore, the propagation delays in the logic gate pipeline reduce the effective gain of the PD; therefore, multiple-input AND and OR gates are employed in this design to improve transition detection and processing.

When comparing the PD topologies for the Alexander full-rate NRZ (see Fig. 2.4a), half-rate NRZ (see Fig. B.1a), and full-rate PAM4 (see Fig. B.2), the number of required flip-flops, XOR gates, and logic components increases substantially. This comparison is summarized in Table B.1. It is important for the reader to consider that implementing these elements with CML circuits results in static power consumption, while CMOS-based implementations primarily contribute dynamic power, which depends on the transition activity, data rate, and clocking scheme.

Components		NRZ full-rate	NRZ half-rate	PAM4 full-rate
Phase Detector	FFs	4	8	6
	XORs	2	4	-
	CCs	-	-	6
	AND	-	-	26
	OR	-	-	11
Clock generation	VCO	1	1	1
	Divider	-	1	-
	Buffers	1	2	1

TABLE B.1: Component comparison of Alexander PD: full-rate NRZ, half-rate NRZ, and full-rate PAM4.

Appendix C

Transistor characterization and Figures of Merit in FD-SOI CMOS

In Chapter 5, we highlighted that analytical design approaches based on overdrive or gate voltage (V_{GS}) become challenging in advanced CMOS nodes. Fig. C.1a show how key parameters of an SLVT nFET for mm-wave operation vary with V_{GS} . For reference, $V_{GS} = 0.4$ V can be considered. As the backgate bias (V_{BG}) is increased from 0 V to 0.8 V, the threshold voltage (V_T) decreases, shifting the overdrive voltage and improving the transit frequency (f_T) from approximately 150 GHz to 220 GHz. Notably, this enhancement arises from a leftward shift in the f_T peak, rather than a uniform increase. The maxima of gain efficiency ($f_T \times g_m/I_D$), f_{MAX} , and the minimum noise figure (NF_{min} at 30 GHz) also shift to lower V_{GS} values. Therefore, targeting the optimum $f_T \cdot g_m/I_D$, f_{MAX} , or NF_{min} requires readjusting the gate voltage.

For high-speed designs, f_T represents the maximum frequency for current gain, while f_{MAX} sets the limit for power gain. The product $f_T \cdot g_m/I_D$ is a widely-used figure of merit that balances speed and power efficiency.

Alternatively, Fig. C.1b shows the transistor parameters plotted as a function of drain current density. The parameters are normalized to I_D/W . This current-centered biasing perspective is central to the g_m/I_D design methodology, which directly links device-level physics to circuit optimization. Using current density as the basis for parameter extraction standardizes design choices across technology nodes and streamlines transistor sizing for target performance. This approach greatly facilitates the sizing and biasing of transistors in CML and other high-speed circuit topologies.

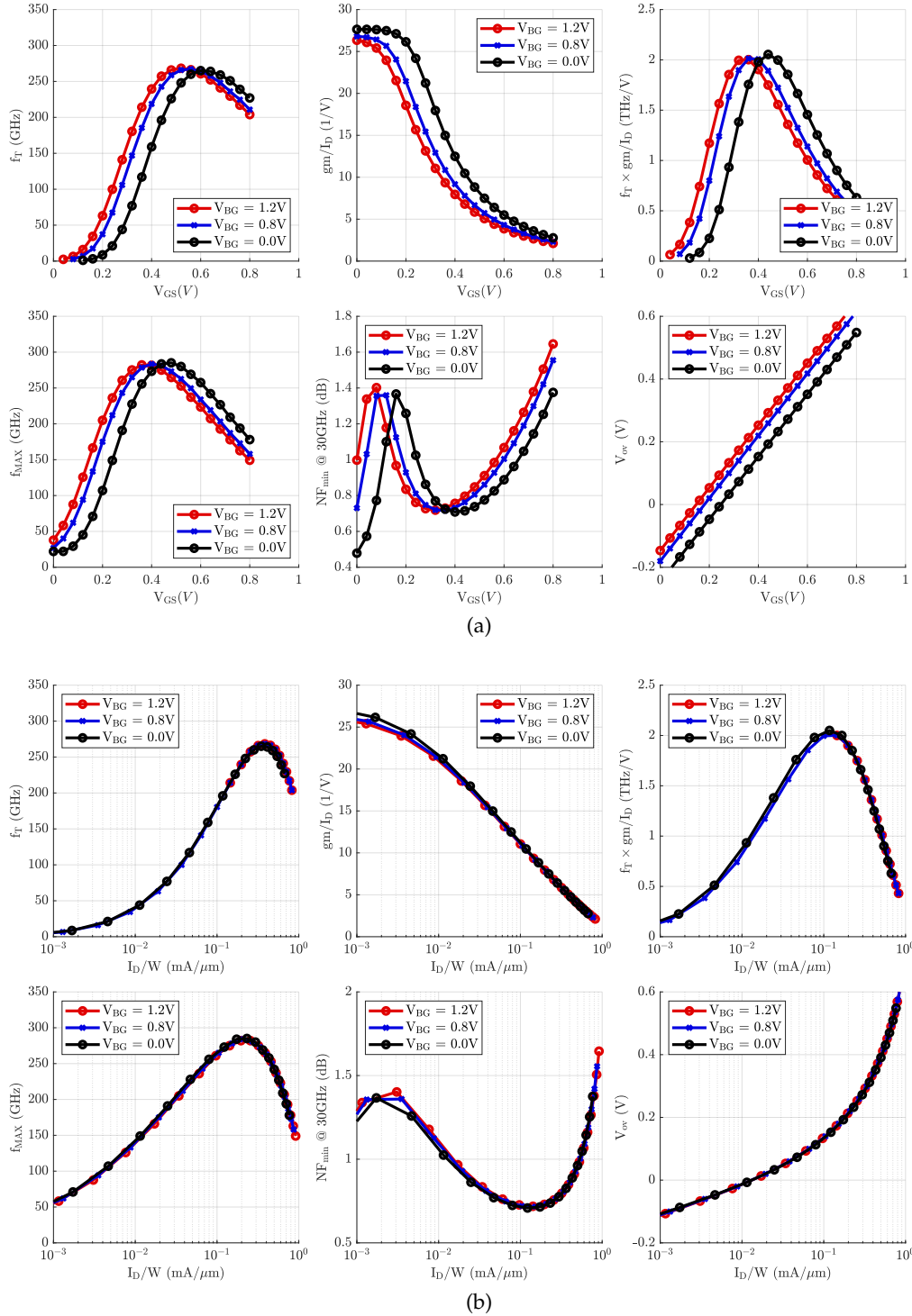


FIGURE C.1: Simulated SLVT nFET mm-wave transistor parameters as a function of: (a) gate voltage (V_{GS}), and (b) drain current density (I_D/W), for various backgate biases (V_{BG}). $V_{DS} = 0.4V$

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This work presents the theory and implementation of a reference-less, full-rate Non-Return-to-Zero (NRZ) Bang-Bang Clock and Data Recovery (BBCDR) designed for high-speed optical transceivers in hybrid and Electronic-Photonic Integrated Circuits (EPIC) integration. Utilizing the transition-based nonlinear Alexander Phase Detector (PD) for inherent clock recovery and data retiming, comprehensive nonlinear models are developed to characterize the second-order Phase-Locked Loop (PLL) with distinct proportional and integral branches.

To overcome the limited acquisition range constrained by stringent jitter requirements, a novel frequency acquisition technique is introduced. The technique employs either a modulated offset voltage applied externally to the Voltage Controlled Oscillator (VCO) or a modulated offset current applied within the integral branch to deliberately detune the nominal VCO frequency during PLL operation. This controlled detuning extends the acquisition range beyond that of conventional BBCDR architectures, while only marginally increasing complexity and power dissipation. Moreover, permanent offset modulation automates the acquisition process.

Theoretical foundations of the proposed techniques, along with their operating conditions and limitations, are discussed in detail. Offset current modulation enables full acquisition across the entire VCO tuning range, whereas external offset voltage modulation achieves approximately one-third coverage. The proposed techniques are validated through measurements on full-rate NRZ BBCDR chips fabricated across diverse technology nodes, ranging from 250nm Silicon Germanium (SiGe) Bipolar CMOS (BiCMOS) to 22nm Fully Depleted Silicon On Insulator (FDSOI) CMOS. The results demonstrate effective acquisition range extension, power-efficient design, and suitability for next-generation high-speed optical communication systems.