This thesis focuses on the resource-efficient design, ie area-efficient and energy-efficient design of pulse-coded neural networks and its technical implementation in current CMOS technologies.

The energy consumption used for information processing in a nerve cell is estimated by a state control based model of the ion transport through a cell membrane. This is used as a measure for the developed analog and digital implementations.

The transition from biological neurons to the technical implementation of neurons is supported by the derivation of essential properties of an electric neuron model. Subsequently, resource-efficient digital and analogue implementations of pulse-coded neurons in CMOS technologies with feature sizes of 130nm and smaller are designed and the required resources and the properties of the implementations are evaluated. The obtained results are set in relation to the biological model. It turns out that the analogue implementation of pulse-coded neurons in a 130nm CMOS technology is the most efficient realization.

It is shown that the design and use of specialized digital standard cell library elements, with particularly low supply voltage, can reduce the power dissipation of digital implementations by orders of magnitude compared to conventional approaches.