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Zusammenfassung der Dissertation:

Run-time Reconfigurable Multiprocessors

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The main advantage in multiprocessors is the performance speedup obtained with parallelism at processor-level. Similarly, the flexibility for application-specific adaptability is the advantage in reconfigurable architectures. To benefit from both these architectures, we present a reconfigurable multiprocessor template, which combines the benefits of parallelism in multiprocessors and flexibility in reconfigurable architectures. A fast, single cycle, resource-efficient, run-time reconfiguration scheme accelerates customisations in the reconfigurable multiprocessor template. Based on this methodology, a four-core multiprocessor called QuadroCore has been implemented on UMC's 90nm standard cells and on Xilinx's FPGA. QuadroCore is customisable and adapts to variations in the granularity of parallelism, the amount of communication between tasks, and the frequency of synchronisation. To validate the advantages of this approach, a diverse set of applications has been mapped onto the QuadroCore multiprocessor. Experimental results show speedups in the range of 3 to 11 in comparison to a single processor. In addition, energy savings of up to 30% were noted on account of reconfiguration. Furthermore, to steer application mapping based on power considerations, an instruction-level power model has been developed. Using this model, a power-driven instruction selection introduces energy savings of up to 70% in the QuadroCore multiprocessor.