Cubic AlGaN/GaN Hetero-Junction Field-Effect Transistors - Fabrication and Characterisation

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Abstract

Hetero-junction field-effect transistors made of metastable cubic AlGaN/GaN represent an alternative for devices made of stable hexagonal III-nitrides. Due to the absence of spontaneous and piezoelectric fields, cubic AlGaN/GaN provides an incentive for fabrication of hetero-junction field-effect transistors with both normally-on and normally-off characteristics.

In this work, field-effect transistors were fabricated of cubic AlGaN/GaN grown on carbonized silicon (3C-SiC/Si) and free standing Ar^+ implanted 3C-SiC substrates by molecular beam epitaxy. For electrical device isolation, a carbon doped GaN:C buffer was investigated. For this purpose, a new CBr_4 gas source was used and optimized.

Device structuring is performed by photolithography, liftoff process, reactive ion etching, and plasma enhanced chemical vapour deposition. Cubic AlGaN/GaN hetero-junction field-effect transistors with normally-on and normally-off output characteristics depending on the doping of the AlGaN barrier were demonstrated. The devices are characterized by electrical dc current-voltage and capacitance-voltage measurements. The measurement data were analysed using a 1D-Poisson solver and the ATLAS device simulation program. Finally, sample structures for improved cubic AlGaN/GaN field-effect transistor devices were developed.

1 Introduction

AlGaN/GaN hetero-junction field-effect transistors (HFETs) are presently of major interest for use in electronic devices, in particular for high-power and high-frequency amplifiers. This is motivated by their potential in commercial and military applications, e. g. in communication systems, radar, wireless stations, high-temperature electronics and high-power solid-state switching. Currently, state of the art HFETs are fabricated of the *c*-plane surface of wurzite (hexagonal) AlGaN/GaN hetero-structures. Their inherent spontaneous and piezoelectric polarization fields produce extraordinary large sheet carrier concentrations at the AlGaN/GaN hetero-interface. Therefore, all these devices are of the normally-on type [1]-[3].

However, for switching devices and digital electronics field-effect transistors (FET) with normally-off characteristics are desirable. Recently HFETs of *c*-plane AlGaN/GaN with normally-off operations have been reported [4], [5]. Some groups used non-polar *a*-plane AlGaN/GaN to fabricate HFETs [6], [7] and demonstrated that the electrical output characteristics of these devices are different for different gate finger orientations on *a*-plane layers. However, no field-effect transistors have been realized with non-polar cubic group III-nitrides to date, although it was discussed recently by Abe et al. [8] that they would offer to fabricate HFETs without undesirable parasitic piezoelectric and spontaneous polarization fields and with equal electrical properties for all gate orientations. Furthermore, the cubic nitrides would allow using the same technology for normally-on and normally-off devices.

The difference between the hexagonal and cubic AlGaN/GaN systems is demonstrated in Figure 1.1, which shows the conduction band edge and the electron concentration calculated for (a) hexagonal and (b) cubic AlGaN/GaN hetero-structures with the same parameters. An electron accumulation at the AlGaN/GaN hetero-interface is expected in both structures, but the electron channel in the hexagonal hetero-structure is highly conductive with sheet carrier density of 2×10^{13} cm^{-2} while the channel at the cubic hetero-interface is – with a carrier density that is two orders of magnitude lower – nearly depleted. However, it is possible to tune the charge sheet density of cubic AlGaN/GaN by intentional doping for fabrication of HFETs with normally-on characteristics.

The aim of this work was to realise HFETs based on cubic AlGaN/GaN, including the deposition of hetero layers by MBE, device structuring and their electrical characterization. However, to succeed with the realization of c-AlGaN/GaN HFETs certain conditions have to be fulfilled.

One of the most important conditions for such devices is a high insulating substrate or a semi-insulating layer between the substrate and the device to avoid buffer leakage. For

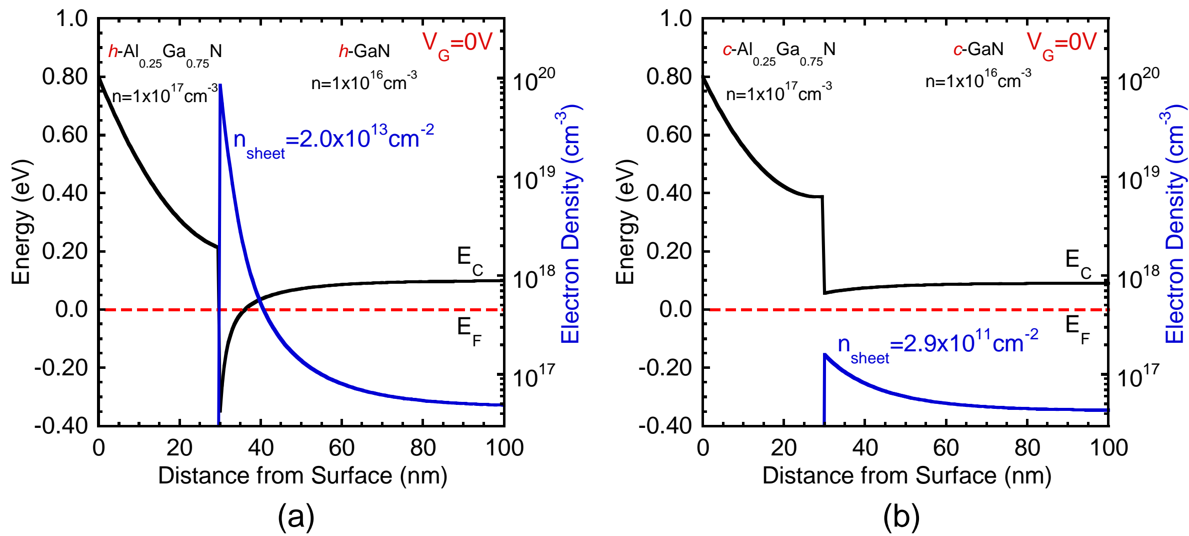


Figure 1.1 Calculated conduction band edge and electron concentration of (a) a hexagonal and (b) a cubic AlGaN/GaN hetero-layer structure.

this purpose, two different substrates, namely carbonised silicon and Ar^+ implanted free standing 3C-SiC were investigated. The properties of c-AlGaN/GaN hetero layers on these substrates are introduced in Chapter 4.

Then, low resistivity ohmic source and drain contacts are necessary to achieve high transconductance and a good Schottky gate contact to avoid gate leakage. Therefore, different metal contacts on c-GaN, c-AlGaN and c-AlN were investigated and described in Chapter 6. The measurement results were used to analyse the output characteristics of c-AlGaN/GaN HFETs and to model new optimized HFET structures, which are discussed in Chapter 7.

Additionally, the output characteristics of cubic AlGaN/GaN (c-AlGaN/GaN) HFETs depend on the thickness and doping of the c-AlGaN barrier layer and the lateral design of the device structure. Therefore the properties of the c-AlGaN/GaN hetero structures and HFETs were analysed with the aid of computer simulations.

The main part of this work is Chapter 5 in which cubic AlGaN/GaN HFETs are introduced and devices with both normally-on and normally-off output characteristics are demonstrated.

2 Fundamentals

In this work, hetero-junction field-effect transistors (HFETs) were fabricated of cubic AlGaN/GaN (c-AlGaN/GaN) and investigated concerning their output and transfer characteristics. To understand the electrical properties of the devices, model calculations were performed using a 1D-Poisson solver and the ATLAS device simulation software.

This chapter gives an introduction on the physical properties of cubic group-III nitrides, their epitaxial growth by molecular beam epitaxy and the characterization methods of their structural properties. A crucial part of this work was the design and fabrication of HFETs. Therefore, the device production process is described in detail in an extra subsection. Finally, a test assembly for current-voltage (IV) and capacitance-voltage (CV) measurements and basic parameters used for model calculations are introduced.

2.1 Properties of cubic III-Nitrides

Group III-nitrides crystallize in the stable hexagonal (wurzite) or in the metastable cubic (zincblende) structure. The challenge of this work was the realization of HFETs based on *cubic* AlGaN/GaN which as a non-polar material – comparable to AlGaAs/GaAs – is capable for fabrication of normally-off devices. Figure 2.1 shows the crystallographic structure of cubic group III-nitrides using the example of cubic GaN (c-GaN). The structure is based on a face-centred unit cell with a base of two atoms. In case of stoichiometric growth conditions the metal is incorporated on the (0,0,0) lattice point, and the nitrogen is placed on the $(\frac{1}{4},\frac{1}{4},\frac{1}{4})$ lattice site. In the direction of the basic vectors, the crystal consists of two alternating layers which contain only metal or nitrogen. The

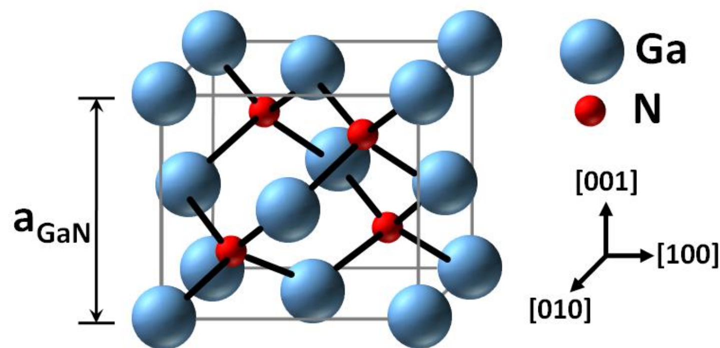


Figure 2.1 Zincblende structure of cubic GaN.

structure is very similar to that of a diamond with a strong covalent bond. This results in a high chemical inertness and thermodynamical stability. Based on the crystal symmetry cubic group III-nitrides exhibit isotropic electrical conductivity and no piezoelectric fields. These properties are important advantages of c-AlGaN/GaN which are used for HFET devices.

The c-AlGaN/GaN hetero-structures were deposited on cubic 3C-SiC substrate. Lattice constant a and band gap energies E_g of c-GaN, c-AlN, and 3C-SiC are summarized in Table 2.1. The lattice constant of c-$Al_xGa_{1-x}N$ is calculated by the linear interpolation of the c-GaN and c-AlN compounds called Vegard's law:

$$a(\mathrm{Al_xGa_{1\text{-}x}N}) = \mathrm{x} \cdot a(\mathrm{AlN}) + (1 - \mathrm{x}) \cdot a(\mathrm{GaN}). \tag{2.1}$$

For the band gap of $Al_xGa_{1-x}N$ alloys parabolic compositional dependence is traditionally assumed:

$$E_g(\mathrm{Al_xGa_{1\text{-}x}N}) = f(\mathrm{x}) - b\mathrm{x}(1 - \mathrm{x}), \tag{2.2}$$

where the bowing parameter b captures the magnitude of the parabolic nonlinearity, and where

$$f(\mathrm{x}) = x \cdot E_g(\mathrm{AlN}) + (1 - \mathrm{x}) \cdot E_g(\mathrm{GaN}) \tag{2.3}$$

is simply the linear compositional dependence of the band gap in the absence of bowing [9]. The dispersion of the bowing parameter of hexagonal $Al_xGa_{1-x}N$ reported by various researchers extends from b=-0.8 eV (upward bowing) to b=2.6 eV (downward bowing), most likely emanating from $Al_xGa_{1-x}N$ alloys prepared by different techniques with varying quality [10]. However, there are no investigations for band gap parameters of cubic $Al_xGa_{1-x}N$ alloys grown by molecular beam epitaxy to date. Therefore, only the linear component from Equation (2.3) was used for the estimation of the band gap of c-$Al_xGa_{1-x}N$ in this work.

Table 2.1 Material parameter of c-GaN, c-AlN and 3C-SiC.

Semiconductor Material	Lattice Constant a	Band Gap E_g
c-GaN	4.53 Å [11]	3.26 eV (direct) [11]
c-AlN	4.37 Å [12]	5.3 eV (indirect) [13] 5.93 eV (direct) [13]
3C-SiC	4.359 Å [14]	2.4 eV (indirect) [15] 6.7 eV (direct) [15]

2.2 Molecular Beam Epitaxy (MBE)

Cubic GaN layers and AlGaN/GaN hetero-structures were deposited by molecular beam epitaxy (MBE) [16] in a RIBER MBE 32 system with a HD-25 radio frequency (rf) activated plasma source by Oxford Applied Research. The sketch of the interior of the MBE UHV-chamber can be seen in Figure 2.2 which shows the sample holder facing the effusion cells. The growth position of the samples is the crossover point of the various molecular and atomic beams from the effusion sources. All effusion cells have an orifice of 2.5 cm in diameter and are located 12 cm from the substrate. To improve the uniformity of deposition, the sample holder can be rotated by the substrate manipulator. A liquid-nitrogen cooled shroud is used to enclose the entire growth area in order to minimize residual water vapour and carbon-containing gases in the vacuum chamber during epitaxial growth.

The loading of a sample holder is done via a load lock in order to avoid deterioration of the vacuum in the MBE chamber. To avoid unintentional doping (UID) of semiconductors, the MBE system and the source materials have to conform to stringent purity levels.

The MBE chamber is equipped with three RIBER ABN35 standard elemental sources which are used for the evaporation of Ga, Al and In for group III-nitride epitaxy. One additional standard cell is filled with Si and is used for silicon doping. The temperature of these effusion cells is measured at the bottom of the pyrolytic boron nitride (PBN) crucible by a thermocouple. The elemental source materials are of 99,9999 % (6N) purity.

Additionally, a self-made carbon tetra bromide (CBr_4) source is connected directly to

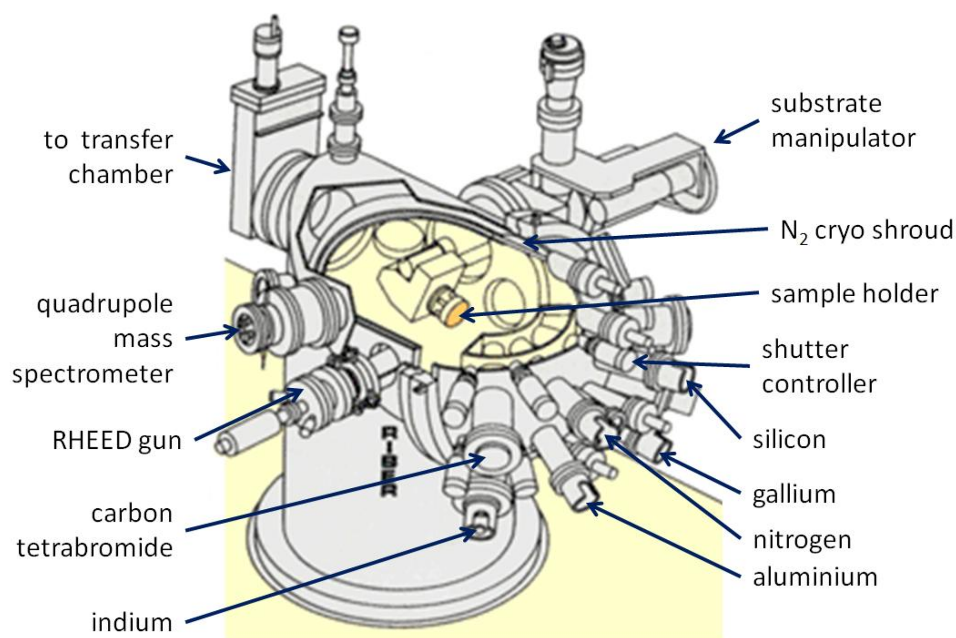


Figure 2.2 Sketch of the interior of the MBE UHV-chamber which shows the sample holder facing to the effusion cells.

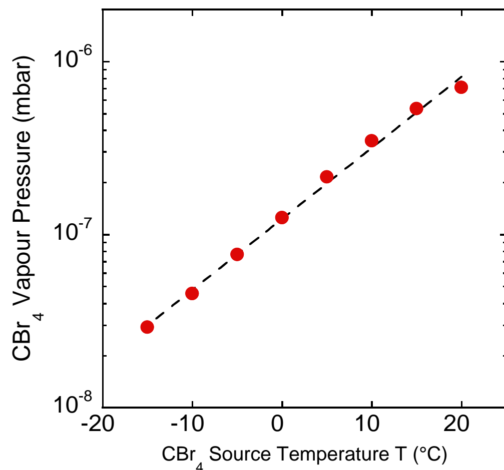


Figure 2.3 Temperature dependent vapour pressure curve of the CBr_4 source measured at maximum valve opening.

the MBE chamber. It is used for doping of c-GaN with carbon (c-GaN:C). The CBr_4 is a colourless solid which sublimates already at room temperature. The CBr_4 flux is controlled by a needle valve and/or the source temperature. The source temperature can be varied between -15 °C and +50 °C. The temperature-dependent vapour pressure curve of the CBr_4 source measured at the sample position at maximum valve opening is depicted in Figure 2.3. The black dashed curve is an exponential fit of the measurement data. The gas supply line is heated to 80 °C to avoid CBr_4 resublimation. The gas injector is heated to 120 °C during the c-GaN:C growth. During the doping process, the CBr_4 molecules are cracked on the sample surface of 720 °C to carbon which is incorporated into c-GaN and other volatile bromine compounds which are pumped out.

As nitrogen source the Oxford Applied Research HD-25 plasma source was operated with a rf energy of 300 W to produce the active atomic nitrogen flux. The PBN aperture disc used for the plasma source has 25 holes each with a diameter of 0.3 mm. The rf energy is inductively coupled to a PBN nozzle tube into which the commercial ultra-high purity nitrogen is led via a mass flow controller.

In order to minimize hexagonal inclusions in the c-GaN layers and to obtain an optimum surface roughness, coverage of one monolayer Ga was established during growth [17]. All samples were deposited at a substrate temperature of 720 °C with a c-GaN growth rate of 115-120 nm/h. Prior to the growth process, substrates were cleaned by acetone, propanol and deionized water and were chemically etched by a buffered oxide etching (BOE, NH_4F:H_2O:HF=4:6:1).

Reflection high energy electron diffraction (RHEED) [18] was used to monitor the crystalline nature of the sample surface during sample growth (in-situ control). This method uses a high energy electron beam (10-20 kV acceleration voltage) which hits the surface at an angle of 1°-3°. The electrons are diffracted at the crystal surface and are forward scattered to a fluorescence screen. The resulting diffraction pattern on this screen is a superposition of the contribution of electrons that have been scattered from atomically flat regions of the crystal and those that have been transmitted through asperities rising

above the surface. Thus, the formed diffraction pattern gives information about the symmetry and periodicity of ordered layers near the surface and the position of atoms within the unit cell. The observed RHEED pattern of cubic III-nitrides was used to control the surface stoichiometry such a c-(2×2) reconstruction during the growth interruption [19], to control the growth rate by measuring the c-AlGaN RHEED intensity oscillations [20] and to measure the Ga coverage of the c-GaN surface during growth [17].

2.3 Structural Characterisation Methods

2.3.1 High Resolution X-Ray Diffraction (HRXRD)

High resolution X-ray diffraction (HRXRD) was used to investigate c-GaN and c-AlGaN/GaN layers for their structural properties as dislocation density, hexagonal inclusions, Al mole fraction of c-$Al_xGa_{1-x}N$ and strain condition of c-AlGaN on c-GaN buffer. For this purpose, a Philips X'Pert materials research diffractometer was used with a copper anode emitting a $K_{\alpha 1}$ radiation of λ=1.54056 Å and a $K_{\alpha 2}$ radiation of λ=1.54444 Å. A schematic sketch of the diffractometer is shown in Figure 2.4. The X-ray tube is equipped with a line focus and a hybrid monochromator which guarantees a beam divergence of 47 arcsec. The monochromator consists of a graded parabolic mirror in connection with a (220) channel-cut germanium crystal. The mirror parallelises the beam and the germanium crystal blocks the $K_{\alpha 2}$ line. The sample is mounted onto an Euler cradle which allows an independent variation of the angle of incident ω, the diffraction angle 2θ, the rotation around the surface normal ϕ and the incident axis ψ, as well as a linear motion in the three directions x, y and z. A multichannel detector X'Celerator was used for measurements of ω- and ω-2θ-line scans and for measurements of reciprocal space maps (RSM) [21].

For a mono-crystal the diffraction of X-rays can be described by the Bragg equation [22]

$$\lambda = 2d_{hkl} \cdot \sin\theta. \tag{2.4}$$

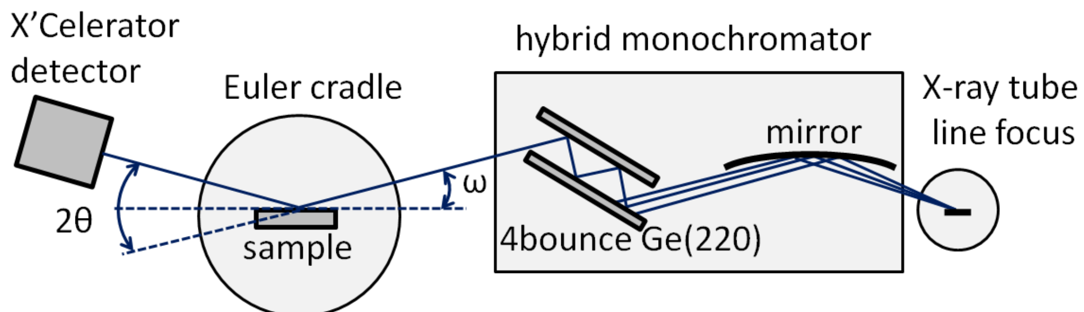


Figure 2.4 Schematic drawing of the Phillips X'Pert MDR HRXR diffractometer consisting of X-ray tube, hybrid monochromator, Euler cradle and X'Celerator detector.

The triplet (*hkl*) denotes the Miller indices and d_{hkl} for cubic structure is given by

$$d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \tag{2.5}$$

where d_{hkl} is the spacing of the lattice planes, a the lattice constant, λ the wavelength of the X-ray radiation and θ the incident angle of the radiation. More details of X-ray diffraction are given in [21].

Three different types of scans were performed to investigate the properties of the c-GaN and c-AlGaN/GaN layers, namely the ω-2θ-scans, the ω-scans and the reciprocal space maps (RSM).

The ω-2θ-scans allow measurements where the angular rotation speed of the detector is twice that of the incident angle. In case of scanning symmetrical lattice points, this is equal to the reflection from the lattice planes parallel to the sample surface. We get information with respect to vertically aligned properties, like the composition of ternary alloys and lattice mismatch.

The ω-scan or so-called rocking curve is a scan with the detector angle in a fixed position, while only the angle of incidence is changed. From the width of the reflex perpendicular to the surface the dislocation density D can be evaluated using the model by P. Gay [23] which is based on the formula

$$D = \frac{\Delta\theta^2}{9b^2} \tag{2.6}$$

where $\Delta\theta$ is the full width of half maximum (FWHM) of the rocking curve in radians and b the length of the Burgers vector. For a zincblende structure the Burgers vector of a 60° dislocation is calculated by

$$b = \frac{a}{\sqrt{2}} \tag{2.7}$$

where a is the lattice constant of c-GaN.

A combination of different ω-2θ-scans slightly displaced along the ω-direction results in an area map. This scanning method is known as RSM resulting in a two-dimensional intensity map. From the RSM it is possible to get the exact position of the reflection maximum and more information about the expansions in the different crystallographic directions.

From the RSM around the (002) reflex of c-GaN the hexagonal GaN inclusions grown on (111) facets can be estimated. The RSM of a c-AlGaN/GaN hetero structure deposited on Ar^+ implanted 3C-SiC (sample 1855) is shown in Figure 2.5 (a). In this measurement mode, only reflexes of 3C-SiC and c-GaN buffer layer are clearly detected. The reflex of c-AlGaN is superposed to the wide c-GaN reflex and is not resolvable. The position of the hexagonal (10-11) and (-1011) GaN reflex is indicated by blue arrows. From the intensity ratio of the hexagonal to the cubic reflex 0.6 % hexagonal inclusions were estimated in this sample.

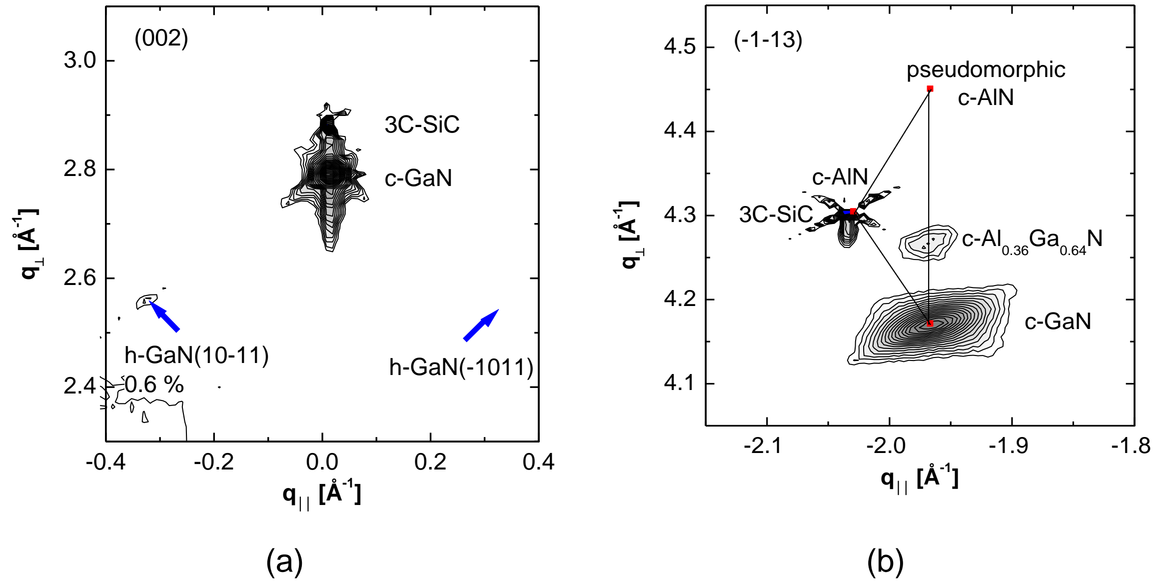


Figure 2.5 Reciprocal space map of a c-AlGaN/GaN hetero structure on free standing 3C-SiC around (a) (002) and (b) (-1-13) reflex of c-GaN.

The position of the c-AlGaN reflex relative to the (-1-13) reflex of c-GaN in the RSM gives information about the Al mole fraction and the strain of c-AlGaN. Figure 2.5 (b) shows asymmetrical RSM around the (-1-13) reflex of the same c-AlGaN/GaN hetero structure (sample 1855). In this measurement mode, the reflexes of 3C-SiC, c-GaN and c-AlGaN are distinguishable. The theoretical positions of relaxed c-AlN and c-AlN pseudomorphically strained on c-GaN are indicated by red squares. The reflexes of the c-GaN and the c-AlGaN have the same $q_{\parallel}$=-1.97 Å^{-1}. Therefore, the c-AlGaN layer is pseudomorphically strained on the c-GaN. Using Vegard's law (Equation 2.1) and the position of the c-$Al_xGa_{1-x}N$ and c-GaN reflexes an Al mole fraction of 36 % was established in the c-AlGaN layer.

2.3.2 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) offers a way to get information about the surface morphology of epitaxial layers. This method allows to measure the surface roughness on an atomic scale. Figure 2.6 shows the schematic diagram of an AFM setup. AFM works by bringing an atomically sharp tip close to a surface. There is an attractive force between the tip and the surface and this force is kept at the same level throughout the experiment. As the probe tip scans back and forth over the surface, the tip will rise and fall with the different features on the surface. A laser beam is pointed to the tip and is reflected to a 4 quadrant photo detector. As the tip goes up and down the laser beam hits different parts of the sensor. With the information the sensor collects an image of the surface can be recreated.

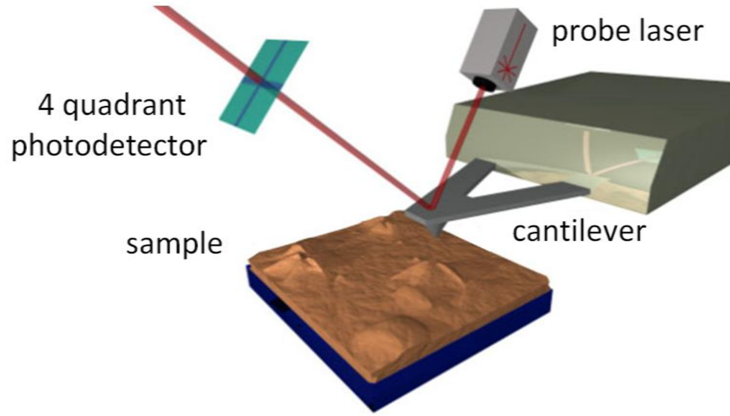


Figure 2.6 Schematic drawing of an AFM setup.

AFM was used to measure the root mean square (RMS) roughness of the sample's surface. The RMS in one dimension is defined as

$$RMS = \left[\frac{1}{L}\int_0^L (z(x) - \bar{z})^2 dx\right]^{\frac{1}{2}} \tag{2.8}$$

where L is the scan width, $z(x)$ the line profile and $\bar{z}$ is the median value of the height. However, the roughness is not determined in real space, it is determined via Fourier transformation in frequency space. In frequency space the RMS is

$$RMS = \left[\int_{f_1}^{f_2} P(f) df\right]^{\frac{1}{2}}. \tag{2.9}$$

P is the power spectral density which is defined as the square of the Fourier transformed line profile. For the line profile $z(x)$ follows

$$P(f) = \frac{1}{L}\left[\int_0^L e^{2\pi i f x} z(x) dx\right]^2. \tag{2.10}$$

As the topography of the scanned area is 2-dimensional and consists of discrete data points the spectral density power in two dimensions is calculated by the fast-fourier transformation (FFT) [24].

2.3.3 Photoluminescence Spectroscopy (PL)

Photoluminescence (PL) spectroscopy was used to investigate the carbon defects in c-GaN:C epilayers and for optical detection of the electron channel at the c-AlGaN/GaN hetero-interface. The setup used for PL measurements is shown schematically in Figure 2.7. The luminescence was excited by a *Kimmons cw* HeCd laser with an excitation line of λ=325 nm ($\hbar\omega$=3.815 eV) and an output power of about 4 mW. The laser plasma lines were suppressed by an interference filter. The laser light was then focussed onto the mirror reflecting the light onto the sample. The PL signal was dispersed by a grating monochromator and detected using a GaAs photomultiplier and a photon counting system. A computer system was used for data collection and visualization. A He bath cryostat allowed temperature-dependent measurements in the range from T=2 K…300 K.

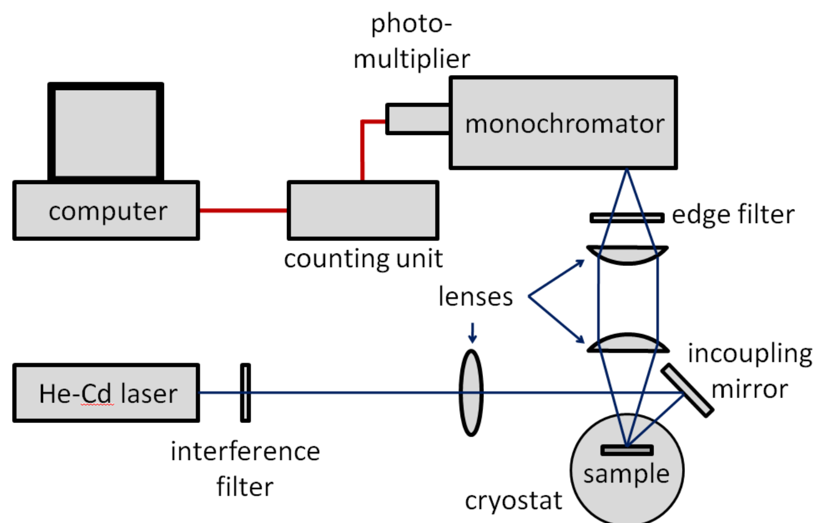


Figure 2.7 Schematic diagram of the photoluminescence (PL) setup.

2.4 Device Structuring

An important part of this work was the design and fabrication of HFET devices. The masks for the photolithography were drawn using a software *Solid Edge Design System* [25] and manufactured by the *Masken Lithographie & Consulting GmbH* (ML&C) [26]. Below, the HFET fabrication process by photolithography, thermal metallization, reactive ion etching (RIE) and plasma enhanced chemical vapour deposition (PECVD) is described in detail. Fundamentals of semiconductor processing technologies are given in [27].

2.4.1 Photolithography and Structuring

Photolithography is the most commonly used commercial technique to create lateral structures in semiconductor technology. The principle of photolithography is based on the transfer of lateral structures of a metal mask to the surface of a semiconductor. A mask for optical lithography consists of a transparent plate, called blank, covered with a patterned film of opaque material. The blank used in this work is made of fused quartz. The advantages of quartz is that it is transparent to deep UV (≤365 nm) and has a very low thermal expansion coefficient. The low expansion coefficient is important when the minimum feature size is less than ≃1.5 µm. The opaque material is typically a very thin (≤100 nm) film of chrome covered with an anti-reflective coating (ARC), such as chrome oxide, to suppress interferences at the wafer surface.

In order to guarantee an optimum structure transfer, the sample surface was cleaned with aceton, propanol and deionised water. The surface oxide was removed using a BOE solution (NH_4F:H_2O:HF=4:6:1). A positive photoresist *Allresist* AR-P 3510 was deposited on the sample surface using spin coating at 9000 rmp (rotations per minute) for 30 s and it was subsequently annealed at 100 °C for 2 min on a heating plate. The undiluted resist with a thickness of 2 µm was used for mesa etching with $SiCl_4$ and for large area contacts. For small sub-µm structures such as gate, source and drain contacts the resist was diluted with the thinner *Allresist* AR 300-12. The thickness of the thinned resist layer was 400 nm. The photoresist was exposed under the photomask in contact mode using a mask aligner *SÜSS KSM MJB3* for 20 s followed by the developing of the structure. The standard resist was developed in a developer/water (1:1) solution for 20 s and the thinned resist was developed in a developer/water (1:4) solution for 30 s. The developer type *Allresist* AR 300-35 was used. The patterned photoresist was used to structure sample layers by RIE or lift off. Finally, the resist was striped with the remover *Allresist* AR 300-70 at 70 °C. The substrate structuring using photolithography, etching and lift off is schematically shown in Figure 2.8.

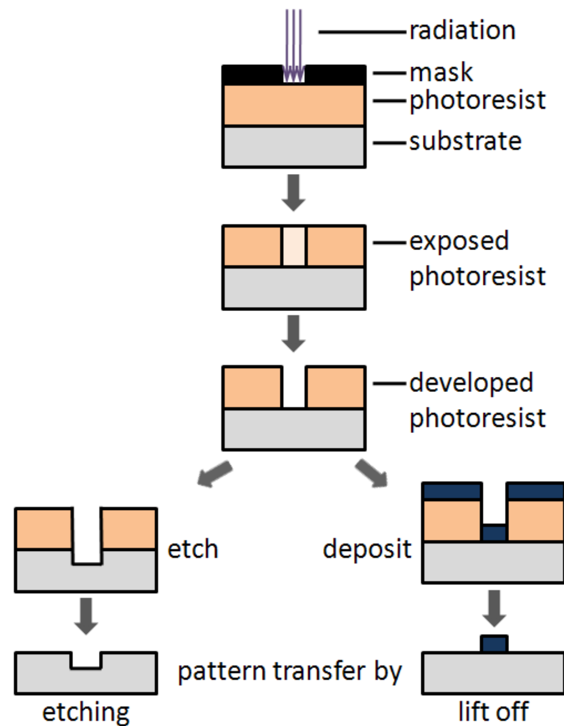


Figure 2.8 Transfer of a pattern to the photoresist for substrate structuring by etching and lift off.

2.4.2 FET Fabrication

The active device has a size of 25 µm×30 µm as shown in Figure 2.9 and is a c-AlGaN/GaN mesa on free standing 3C-SiC or 3C-SiC/Si substrate. The source and drain contacts are of 25 µm×11 µm with a spacing of 8 µm. The gate contact is 2 µm long and is centred between source and drain. The device is surrounded by a SiO_2 isolation layer. Due to the small size it is not possible to contact the device directly. Therefore, large contact pads are connected with source, drain and gate which lie on the SiO_2 isolation layer.

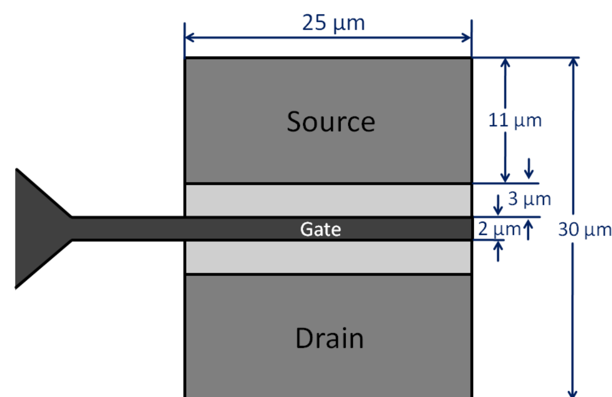


Figure 2.9 Dimensions of FET device structures fabricated using photolithography.

The fabrication of HFET devices is a complex process with six fabrication steps which are described below. The design of the photomasks used for the processing is shown in Figure 2.10 (a)-(e). The black parts in the design are transparent patterns in the mask and are regions on the sample used for etching or lift off process.

Step 1. After the cleaning of the sample with organic solvents and BOE solution, metal stacks shown in Figure 2.10 (a) were thermally evaporated and then annealed in a rapid thermal annealing (RTA) system *ULVAC-RIKO MILA-3000* for the source and drain contacts. For this process, the thinned photoresist was used. In the same step, alignment marks (two grid patterns) were evaporated which are used as the reference for the exact positioning subsequent patterns to the first pattern.

Step 2. The mesa isolation was performed by RIE with $SiCl_4$ using the mask from Figure 2.10 (b). The etching was performed in a RIE machine *OXFORD Instruments Plasmalab 80 Plus* without sample cooling at a $SiCl_4$ flux of 25 sccm, a chamber pressure of 10 mTorr, and a rf power of 300 W. The c-GaN etch rate was around 40 nm/min. The unthinned resist was used which was baked after the developing for 1 min at 100 °C on a hot plate.

Step 3. A 200-300 nm thick SiO_2 insulation layer was deposited on the whole sample surface by PECVD with 425 sccm SiH_4 and 710 sccm N_2O at a chamber pressure of 100 mTorr, a rf power of 20 W and a sample temperature of 300 °C in a PECVD machine *OXFORD Instruments Plasmalab 80 Plus*. The deposition rate was about 80 nm/min.

Step 4. The SiO_2 area over the FET device was etched by RIE with 10.5 sccm Ar and 10.5 sccm CHF_3 at a chamber pressure of 35 mTorr, a rf power of 150 W without sample heating in a RIE Machine *Plasma Technology Plasmalab U80P*. The etch rate was about 35 nm/min. For this process the thinned photoresist and the mask from Figure 2.10 (c) was used.

Step 5. The gate was evaporated using the thinned resist and the mask shown in Figure 2.10 (d). This contact was thermally annealed at 200 °C for 10 min on a heating plate.

Step 6. Finally, the mask from Figure 2.10 (e) was used to evaporate the contact pads. The unthinned photoresist is the most suitable for this process. The large metal pads contact the source and drain stacks and the gate finger and they lie on the SiO_2 isolation layer.

Figure 2.10 (f) shows a SEM diagraph of a fabricated sample structure with four identical FET devices. An enlarged SEM diagraph of a single FET device can be seen in Figure 5.4 (b).

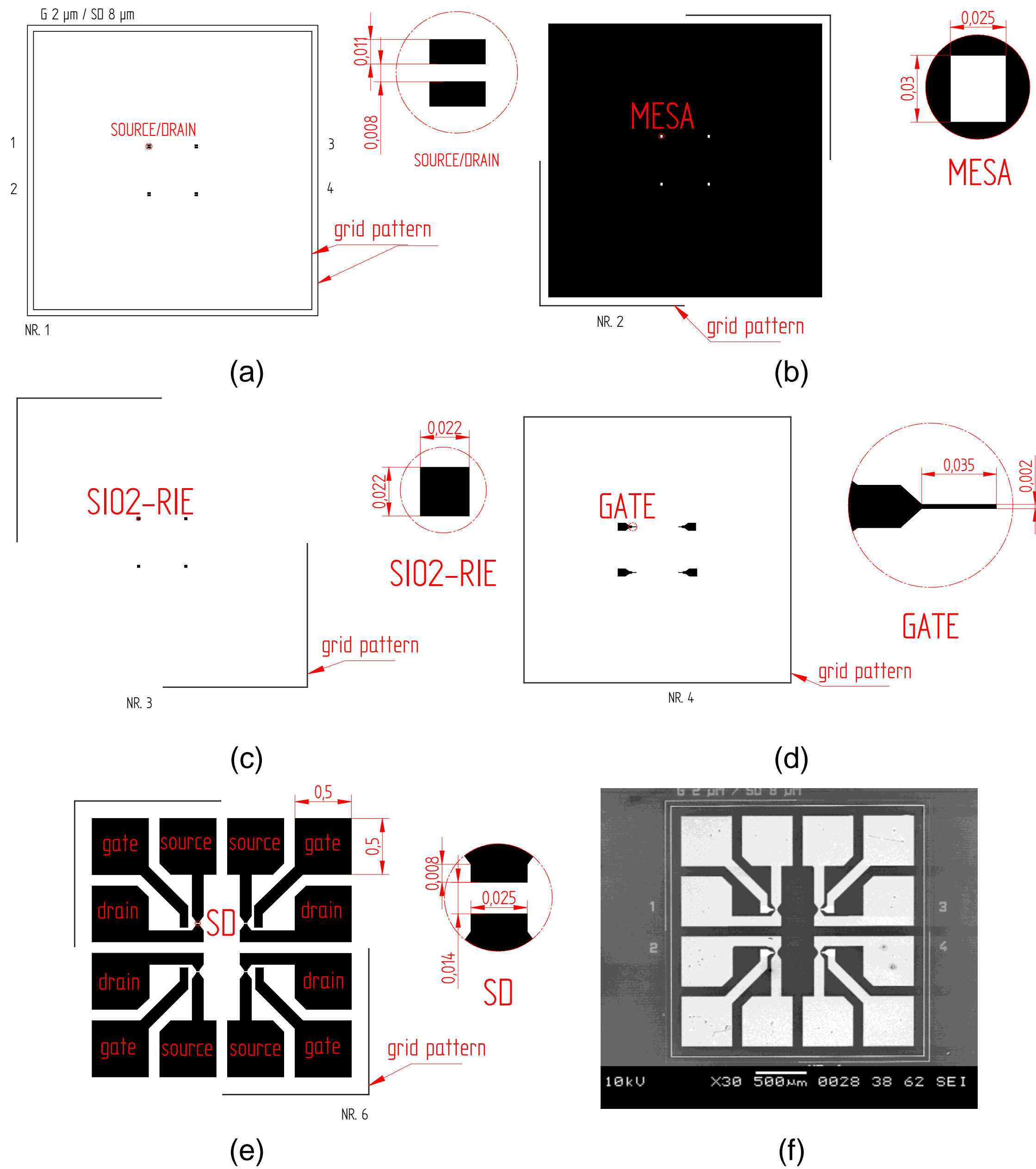


Figure 2.10 (a)-(e) Design of the photomasks used for fabrication of c-AlGaN/GaN HFETs. (a) Mask for source and drain contacts. (b) Mask for mesa etching. (c) Mask for opening of the devices after deposition of SiO_2 isolation layer. (d) Mask for gate contacts. (e) Mask for contact pads. The dimensions are given in mm. (f) SEM diagraph of a fabricated sample structure with four HFET devices.

2.5 Electrical Characterization Methods

For the electrical characterization of samples, current-voltage (IV) and capacitance-voltage (CV) measurements were done. For IV measurements an *Agilent Precision Semiconductor Parameter Analyzer 4156C* was used. CV measurements were performed by an *Agilent Precision LCR Meter E4980A*.

For temperature-dependent measurements a *Janis SHI* closed cycle refrigerator (CCR) system was used. A schematic drawing of the measurement setup for temperature-dependent IV and CV measurements is shown in Figure 2.11. This system can be used to perform electrical measurements between 7 K and 400 K. For cooling, a closed loop of helium gas is compressed and expanded, based on the Gifford-McMahon (G-M) thermodynamic cycle. A detailed description of the G-M cycle can be found in [28], [29]. The cold head is separated from the compressor by a couple of flexible high pressure tubes which transport the compressed helium into and out of the cold head. This enables easy handling of the cold head which weighs about 8 kg, while the 65 kg compressor is firmly positioned nearby. The cold head expands the helium gas to cool the sample. It is connected with a cooling finger and a sample mount. A heater and a thermocouple are installed on the cold finger and are used to precisely control the sample temperature by a *LakeShore 331* temperature controller. While the cold finger is cooled permanently, the heating power of the heater is varied according to the set temperature. The cooling finger is surrounded by a radiation shield (not shown here) and a vacuum jacket. To evacuate the

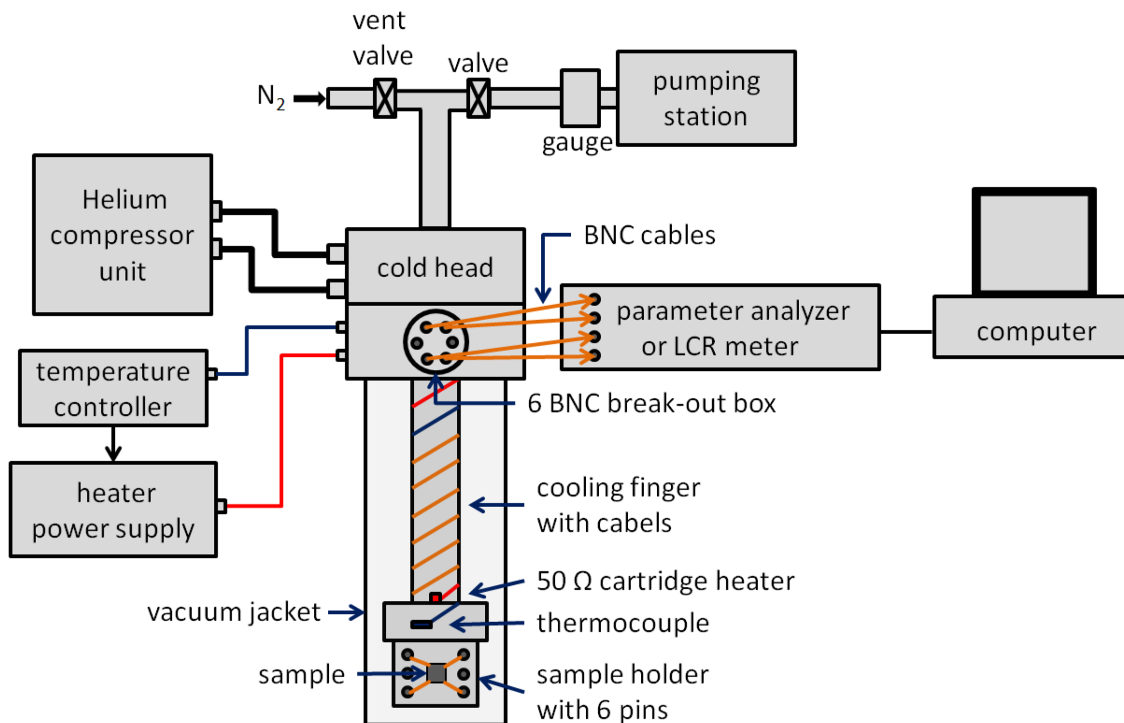


Figure 2.11 Schematic drawing of the measurement setup for temperature dependent IV and CV measurements.

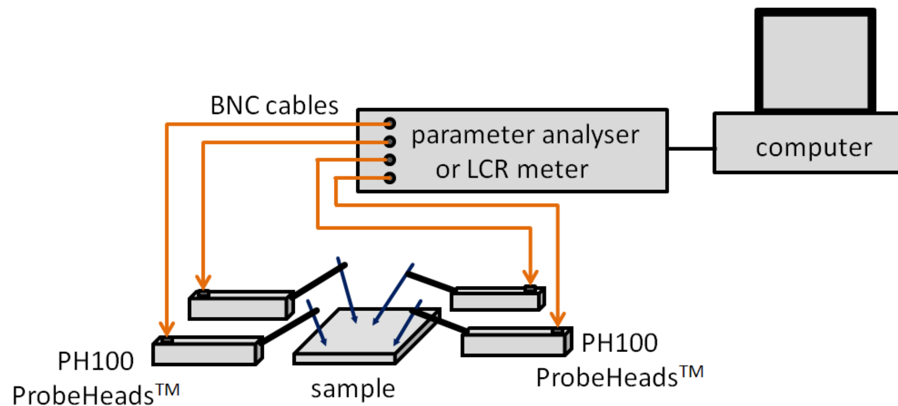


Figure 2.12 Schematic drawing of the measurement setup for room temperature IV and CV measurements.

sample space a pumping station *PFEIFFER Vacuum TSH 071E* is used. The vacuum is controlled by a compact full range gauge *PFEIFFER Vacuum PKR 251*. For the venting a nitrogen supply is used.

The sample is connected with the sample holder by brazing with indium. Six pins on the sample holder allow to connect six contacts of the sample with six BNC connectors in the BNC break-out box which are connected via BNC cables with the measurement instruments.

For room temperature measurements the samples were contacted using a *SüssMicroTec PM5* manual probe system schematically shown in Figure 2.12. In this setup *SüssMicroTec PH100 ProbeHeads* with tungsten carbide probe needles with a tip radius of 7 µm were used.

All electrical measurements were performed in darkness. Measurement data were stored in a computer.

2.6 Simulation Calculations

To understand the electrical measurement results of our cubic AlGaN/GaN hetero-layers and HFET devices, model calculations of their energy-band diagrams and output/transfer characteristics were performed using a 1D-Poisson solver [30], [31] and ATLAS device simulation software [32], respectively. The simulation programs are described in Appendix F.

The material parameters of c-GaN and c-AlN used for calculations are given in Table 2.2. Parameters of ternary c-$Al_xGa_{1-x}N$ were calculated by Vegard's law (Equation 2.1). Al mole fraction, thickness und donor concentration of the layers was varied according to the investigated samples. Therefore, more parameters are given in those sections describing calculation results.

Table 2.2 Material parameter of c-GaN and c-AlN used for calculation of energy-band diagrams.

Parameter	c-GaN	c-AlN
Energy Gap	3.2 eV	5.05 eV
Conduction Band Offset	---	1.33 eV
rel. Dielectric Constant	8.9	8.4
Electron Mobility	100 cm^2/Vs	100 cm^2/Vs
Polarization	1×10^{-8} C/cm^2	1×10^{-8} C/cm^2

3 Principals of Hetero-Junction Field-Effect Transistors

The hetero-junction field-effect transistor (HFET) is also known as the modulation-doped field-effect transistor (MODFET), high-electron-mobility transistor (HEMT), two-dimensional electron-gas field-effect transistor (TEGFET), and selectively doped hetero-junction transistor (SDHT) [33], [34]. The unique feature of the HFET is the hetero-structure, in which the wide-energy-gap material is doped and carriers diffuse to the undoped narrow-band gap layer at which hetero-interface a carrier channel is formed. The net result of this modulation doping is that the channel carriers in the undoped hetero-interface are spatially separated from the doped region and have high low-temperature mobilities because there is no impurity scattering. This phenomenon is demonstrated in Figure 3.1 where mobilities in the hexagonal bulk GaN are compared to those in the electron channel at the hexagonal $Al_{0.15}Ga_{0.85}N$/GaN interface.

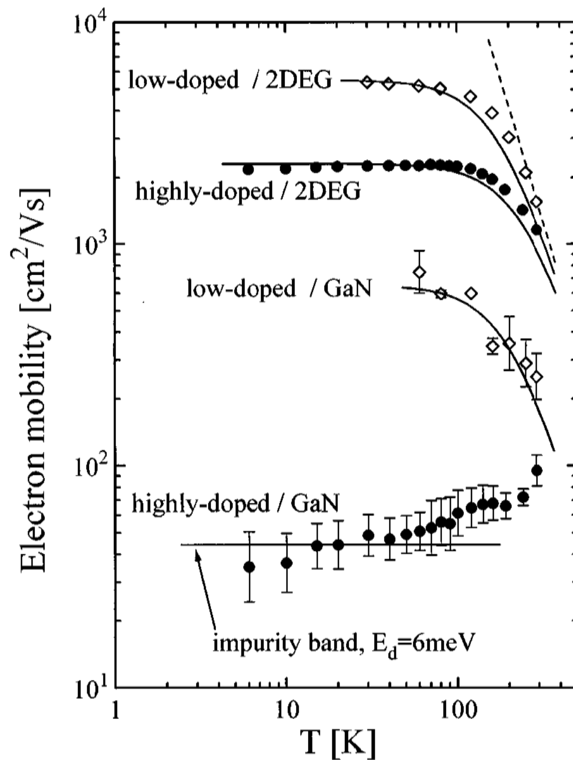


Figure 3.1 Temperature dependence of electron mobility for the 2-DEG in hexagonal AlGaN/GaN and the hexagonal GaN bulk layer with two different doping concentrations [35].

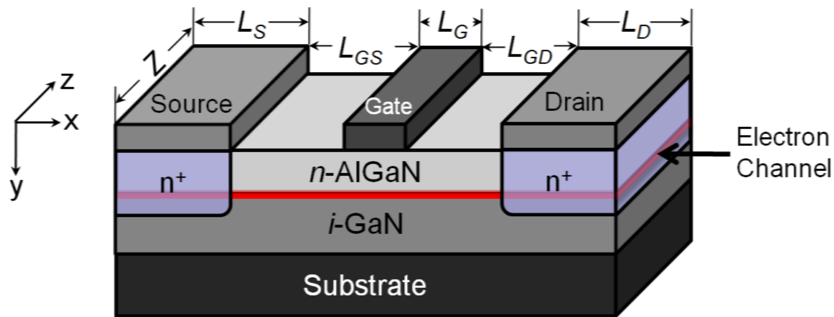


Figure 3.2 Typical structure of an AlGaN/GaN HFET.

3.1 Basic Device Structure

A basic HFET structure based on an AlGaN/GaN system is shown in Figure 3.2. It can be seen here that the barrier layer AlGaN under the gate is doped, while the GaN buffer layer is undoped. The doped barrier layer is typically around 30 nm thick. Very often, a δ-doped charge sheet is used within the barrier layer and placed close to the channel interface instead of uniform doping. The source and drain contacts are ohmic while the gate is a Schottky barrier. Sometimes, a top layer of n^+-GaN on AlGaN is used for better source and drain ohmic contacts. The deeper n^+-regions of source/drain are formed either by ion implantation or introduced during the alloying step to contact the electron channel. For low values of drain-to-source bias, a current flows from drain to source through the electron channel. The carrier sheet density and consequently the conductivity of the channel are controlled by the gate bias. Increasing of the positive bias applied to the gate increases the depth of the potential well at the AlGaN/GaN interface. This results in enhanced sheet carrier density of the electron channel and, therefore, increased current conduction. Increasing of the negative gate bias decreases the depth of the electron channel and the sheet carrier density decreases thereby lowering the channel conductivity.

The most important dimension that characterises the HFET physical structure is the gate length L_G. This dimension determines the maximum frequency limits for HFET devices. Typical gate lengths are in the 0.1..2 μm range. The gate width Z is another physical device dimension that is of primary importance to the determination of device behaviour. The device current is directly proportional to the gate width because the cross-section area available for the channel current is proportional to Z. For low-noise, low-current applications relatively small-gate-width devices are utilized. In contrast, large-gate-width devices are typically used for power applications. Other characteristic dimensions are the gate-to-source L_{GS} and gate-to-drain L_{GD} spacing and the drain L_D and source L_S length.

The actual layout of the HFET devices is more complex than implied by Figure 3.2. Connections must be made to all three terminals – source, gate and drain. These connections are large-area metal contact pads for probes or bond wires. The drawing of masks to use for the fabrication of HFET devices is shown in Chapter 2.4.2 and in Appendix E.

3.2 Current-Voltage Characteristics

In this work, *n*-channel devices of cubic AlGaN/GaN with the channel formed by electrons were investigated. There are two different types of FETs dependent on the state of the transistor with zero gate bias. Their energy-band diagrams at equilibrium (calculated for a cubic $Al_{0.25}Ga_{0.75}N$/GaN hetero-layer) and schematic output and transfer characteristics are compared in Figure 3.3. FETs are called enhancement-mode, or normally-*off* if at zero gate bias the channel is depleted and the Fermi level E_F is below the conduction band edge E_C. The conductance of the electron channel is very low and a positive gate voltage must be applied to fill the channel with carriers. The counterpart is called depletion-mode, or normally-*on*, if the channel is conductive with zero gate bias. The Fermi level E_F crosses the conduction band edge at the AlGaN/GaN hetero-interface. Negative gate voltage must be applied to turn the transistor off.

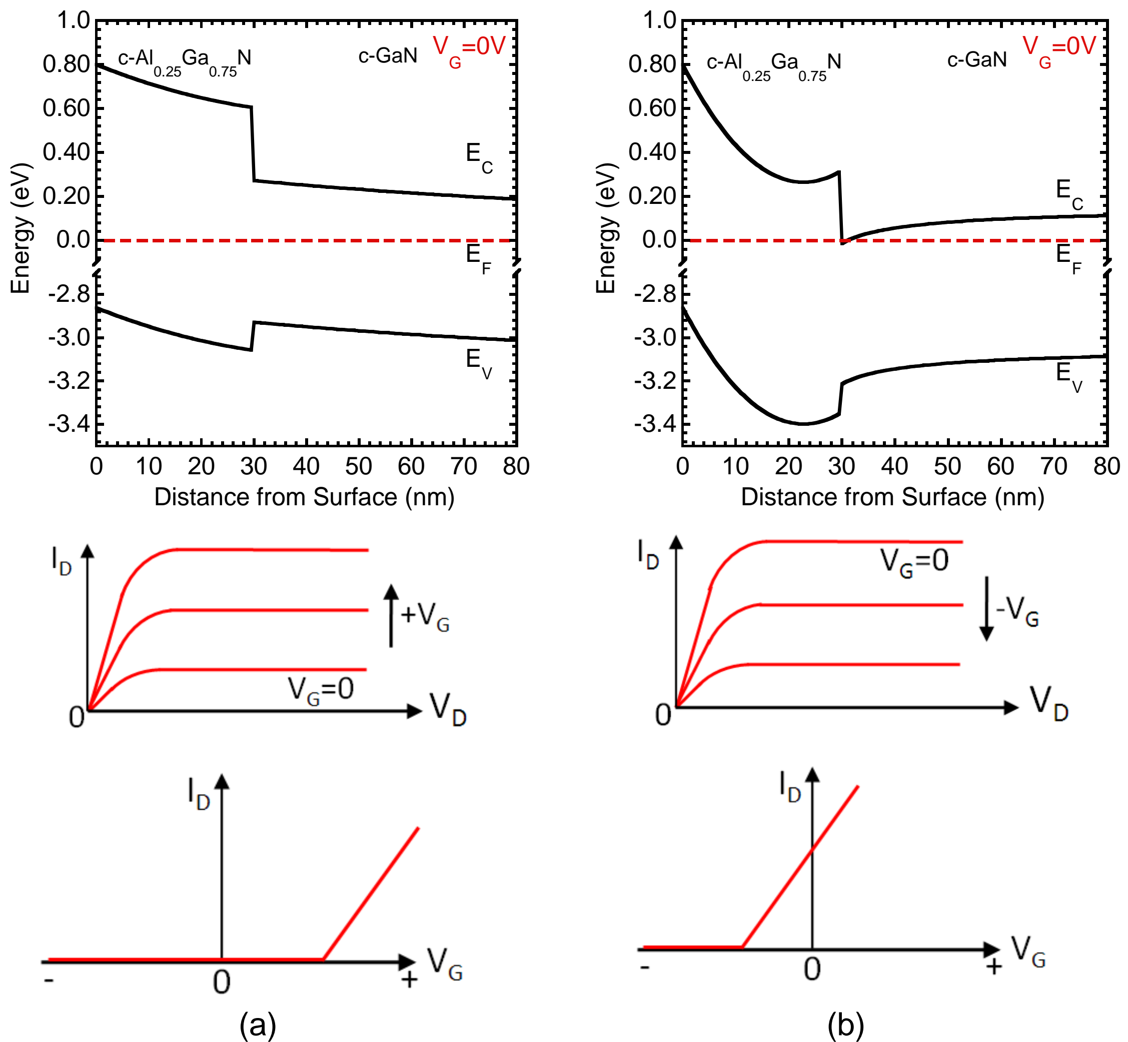


Figure 3.3 Band diagrams of c-AlGaN/GaN hetero-structures and schematic output and transfer characteristics of *n*-channel (a) normally-*off* and (b) normally-*on* HFETs.

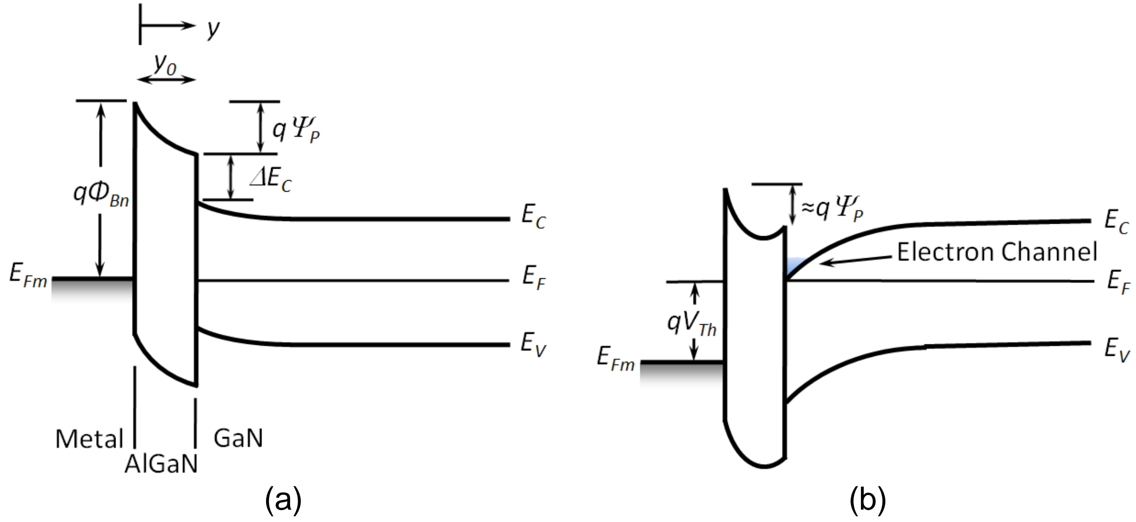


Figure 3.4 Room temperature energy-band diagrams for a normally-off HFET at (a) equilibrium and (b) onset of threshold.

Based on the principle of modulation doping, the impurities within the barrier layer are completely ionized and carriers depleted away. Referring to the energy-band diagrams of Figure 3.4, the potential variation ψ_P within the depleted region is given by

$$\psi_P = \frac{q}{\varepsilon_S}\int_0^{y_0} N_D(y)y\,dy \tag{3.1}$$

for a general doping profile. For uniform doping, this built-in potential becomes

$$\psi_P = \frac{qN_D y_0^2}{2\varepsilon_S}. \tag{3.2}$$

An important parameter for HFETs is the threshold voltage V_{th}, the gate bias at which the channel starts to form between the source and the drain. From Figure 3.4 (b), a first-order approximation shows that this occurs when the Fermi level E_F at the GaN surface coincides with the conduction band edge E_C. This corresponds to the bias condition of:

$$V_{th} \approx \phi_{Bn} - \psi_P - \frac{\Delta E_C}{q}. \tag{3.3}$$

It can be seen here that by choosing the doping profile and barrier height ϕ_{Bn}, V_{th} can be varied between positive and negative values. The example shown in Figure 3.4 has a positive V_{th}, and the transistor is called a normally-off device, which was the main objective of this work.

With a gate voltage larger than the threshold voltage, the charge sheet in the channel induced by the gate is capacitively coupled and is given by

$$Q_n = C_0(V_G - V_{th}), \tag{3.4}$$

where

$$C_0 = \frac{\varepsilon_S}{y_0 + \Delta y} \tag{3.5}$$

and Δy is the channel thickness of the electron channel estimated to be around 8-10 nm. When a drain bias is applied, the channel has a variable potential with distance and its value with respect to the source is designated as $\Delta\psi(x)$ (x is the direction from drain to source). It varies along the channel from 0 at the source to V_D at the drain. The channel charge $Q_n(x)$ as a function of position becomes

$$Q_n(x) = C_0[V_G - V_{th} - \Delta\psi(x)]. \tag{3.6}$$

The channel current at any location is given by

$$I_D(x) = ZQ_n(x)v(x). \tag{3.7}$$

Since the current is constant throughout the channel, integrating the above equation from source to drain (assuming L_{GS} =L_{GD}=0) gives

$$I_D = \frac{Z}{L}\int_0^L Q_n(x)v(x)\,dx. \tag{3.8}$$

With constant mobility, the drift velocity is simply given by

$$v(x) = \mu_n \mathscr{E}(x) = \mu_n \frac{d\Delta\psi}{dx}. \tag{3.9}$$

Substituting Equations (3.6) and (3.9) into Equation (3.8) we obtain after an integration

$$I_D = \frac{Z\mu_n C_0}{L}\left[(V_G - V_{th})V_D - \frac{V_D^2}{2}\right]. \tag{3.10}$$

The output characteristics for a normally-off HFET are shown in Figure 3.5. In the linear region where $V_D \ll (V_G - V_{th})$, Equation (3.10) is reduced to an ohmic relationship

$$I_{D,lin} = \frac{Z\mu_n C_0(V_G - V_{th})V_D}{L}. \tag{3.11}$$

At $V_{D,sat} = V_G - V_{th}$, $Q_n(L)$ at the drain is reduced to zero (Equation (3.6)) corresponding to the pinch-off condition, and the current saturates with V_D. This gives a saturation drain current of

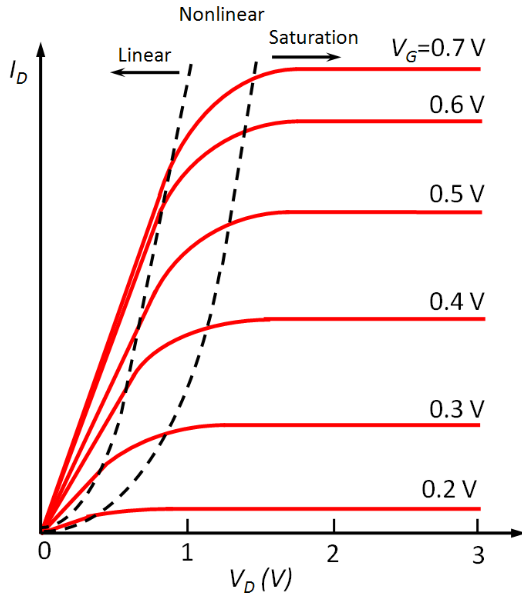


Figure 3.5 Output characteristics of a normally-off HFET.

$$I_{D,sat} = \frac{Z\mu_n C_0}{2L}(V_G - V_{th})^2. \tag{3.12}$$

From the above equation, the transconductance g_m can be obtained:

$$g_{m\equiv}\frac{dI_{D,sat}}{dV_G} = \frac{Z\mu_n C_0(V_G - V_{th})}{L}. \tag{3.13}$$

As the technology advances and pushes for device performance and density, the channel length gets shorter and shorter. The internal longitudinal field $\mathscr{E}_x$ in the channel also increases as a result. Figure 3.6 shows the electron velocity-field (v-$\mathscr{E}$) relationship where a two-piece linear approximation is also shown with a critical field $\mathscr{E}_c$. For low fields, the mobility is constant. This low-field mobility is used for the long-channel characteristics described before. In the extreme case of a very high field, the velocity approaches a value, saturation velocity v_s. In state-of-the art devices, the current becomes saturated with V_D before the pinch-off condition occurs, due to the fact that the carrier drift

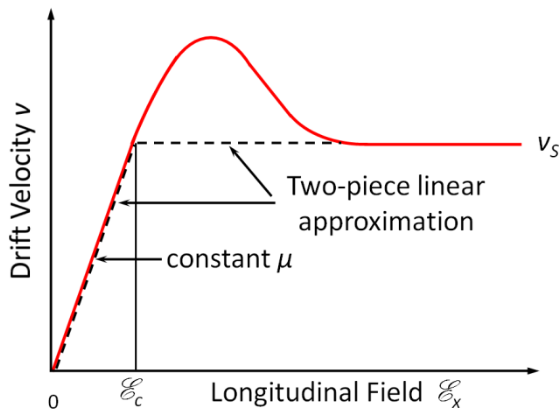


Figure 3.6 v-$\mathscr{E}$ relationship for the channel charge. Transfer/electron effect is shown for materials such as GaN. Two/piece linear approximation is indicated.

velocity is no longer linearly proportional to the electric field. In other words, in high fields the mobility μ, which is defined as $\mu = v/\mathscr{E}$ becomes field-dependent.
For devices with high mobilities such as HFETs this phenomenon is more severe. In case of a field dependent velocity $I_{D,sat}$ and $V_{D,sat}$ are given by

$$I_{D,sat} = \frac{ZC_0\mu_n}{L}\left(V_G - V_{th} - \frac{V_{D,sat}}{2}\right)V_{D,sat}, \tag{3.14}$$

$$V_{D,sat} = L\mathscr{E}_c + (V_G - V_{th}) - \sqrt{(L\mathscr{E}_c)^2 + (V_G - V_{th})^2}. \tag{3.15}$$

4 Separation between Substrate and HFET Device

A semi-insulating substrate or a GaN buffer layer is the fundament for many nitride-based device structures. Lateral conduction devices, such as the AlGaN/GaN HFET, require semi-insulating material beneath the device structure. A conductive buffer layer will not only lead to high leakage current and therefore poor pinch-off characteristics, but will also degrade the rf performance of the HFETs at high frequencies. Moreover, for electrical characterization test structures, e.g. Hall effect measurement or transmission line measurement (TLM) structures, the tested layer has to be insulated from the underlying conduction path. In this chapter, the necessity for isolation between the FET device and the substrate will be discussed first. Then, three possible insulating buffers for cubic nitrides will be introduced, namely the semi-insulating carbonised silicon 3C-SiC/Si, the Ar^{+} implanted free standing 3C-SiC, and the carbon doping of cubic GaN using a CBr_4 source.

4.1 Model Calculations of Cubic AlGaN/GaN FETs on Different Substrates

To clarify the necessity for buffer insulation, model calculations of cubic AlGaN/GaN FET devices on different substrates were performed by R. Granzner at the TU Ilmenau using the ATLAS simulation program. The hetero-structure from Figure 4.1 was used for the calculations. It was assumed that the ohmic source and drain contact were deposited on GaN contacting directly the electron channel. The Schottky gate contact was localised on top of c-AlGaN. Analogous to the real devices the gate length was 2 µm and the gate-to-source and the gate-to-drain space was 3 µm. For the calculations 30 nm cubic AlGaN with 36% Al mole fraction and a donor concentration of N_D(AlGaN)=5×10^{17} cm^{-3} on 600 nm cubic GaN with a donor concentration of N_D(GaN)=5×10^{16} cm^{-3} were used.

Figure 4.2 (a) shows the calculated I_D-V_{DS} characteristics of HFET on two different substrates with a donor concentration of N_D=2×10^{18} cm^{-3} (black curves) and an acceptor concentration of N_A=2×10^{12} cm^{-3} (red curves) for gate voltages of V_G=-5 V, 0 V and 5 V. The drain-to-source current through the device with the highly doped substrate is two orders of magnitude higher than through the high-insulating substrate. Moreover, due to the high shunt current the field-effect is not observable. These calculations demontrate, that a semi-insulating substrate is essential for the fabrication of FETs. Calculated I_D-V_{DS}

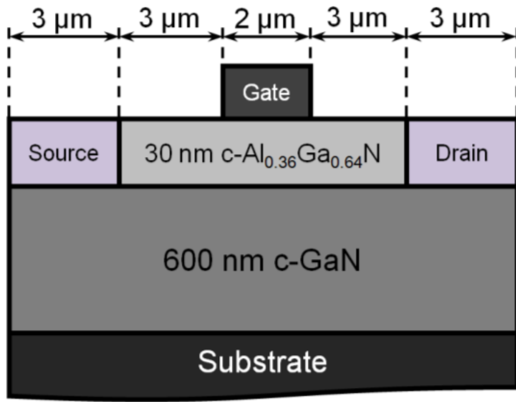


Figure 4.1 Schematic cross-section of a FET structure for model calculations.

characteristics of the same device on a substrate with N_A=2×10^{12} cm^{-3} and without substrate are shown in Figure 4.2 (b). In both cases, a current in the same order of magnitude as the calculated field-effect is available at a gate voltage of V_G=-5 V. This shunt current is caused by the leakage through the 600 nm thick c-GaN buffer layer with a high donor density of N_D(GaN)=5×10^{16} cm^{-3}. This is pointed out by the calculation of I_D-V_{DS} curves for devices on c-GaN with two different thicknesses of 100 nm and 600 nm and the same donor concentration of N_D(GaN)=5×10^{16} cm^{-3} shown in Figure 4.3 (a). The device with 100 nm c-GaN thickness is completely depleted at V_G=-5 V whereas the device with 600 nm c-GaN is conductive under the same conditions. Therefore, since the residual background carrier concentration of c-GaN is about 5×10^{16} cm^{-3}, the c-GaN buffer layer must not be thicker than 100 nm to avoid the parasitic shunt current.

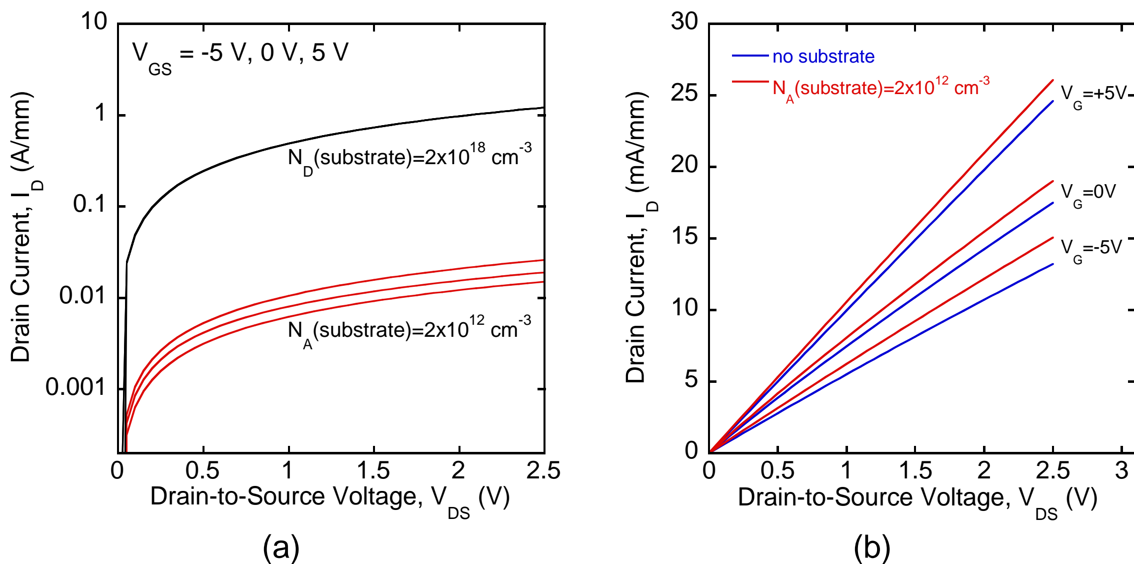


Figure 4.2 Simulated static output characteristics of the FET from Figure 4.1 for different substrate conductivity. The estimated donor density is N_D(c-GaN)=5×10^{16} cm^{-3} and N_D(c-AlGaN)=5×10^{17} cm^{-3}. (a) Comparison of FET on 3-SiC with N_D=2×10^{18} cm^{-3} (black curves) and N_A=2×10^{12} cm^{-3} (red curves). (b) Comparison of FET on 3-SiC with N_A=2×10^{12} cm^{-3} (red curves) and FET without substrate (blue curves).

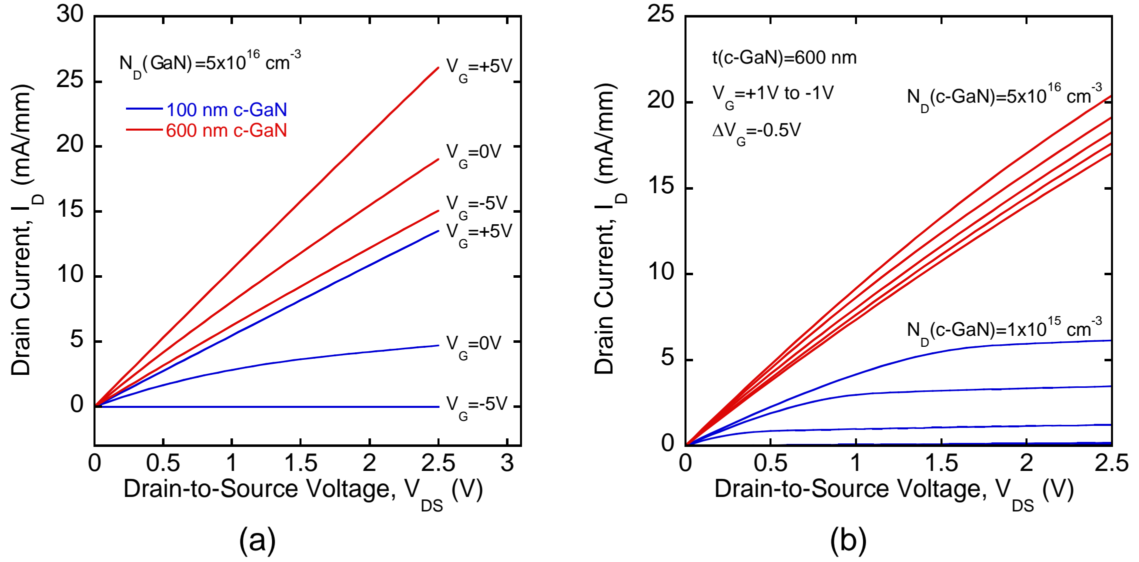


Figure 4.3 Simulated static output characteristics of the FET from Figure 4.1 for (a) 100 nm (blue curves) and 600 nm (red curves) GaN buffer layer with the same donor density of N_D=5×10^{16} cm^{-3} and (b) for different donor densities of N_D=5×10^{16} cm^{-3} (red curves) and N_D=1×10^{15} cm^{-3} (blue curves) and the same c-GaN thickness of t=600 mn.

The effect of the c-GaN doping on the shunt current is depicted in Figure 4.3 (b). The diagram shows calculated I_D-V_{DS} characteristics of two HFETs with a GaN donor concentration of N_D(GaN)=5×10^{16} cm^{-3} (red curves) and N_D=1×10^{15} cm^{-3} (blue curves) for V_G=-1V..1V. The GaN layer thickness was 600 nm for both samples. The device with N_D(GaN)=5×10^{16} cm^{-3} GaN layer exhibits a shunt current which is five times higher than the calculated field-effect. The device with N_D=1×10^{15} cm^{-3} features no shunt current and is completely depleted already at V_G=-0.5 V. In comparison with this HFET the same device on 100 nm GaN with N_D(GaN)=5×10^{16} cm^{-3} is depleted at a higher negative gate voltage of V_G=-5 V. This means that if the GaN buffer layer is conductive, the device is a combination of HFET and MESFET. After the electron channel at the AlGaN/GaN interface is depleted, negative gate voltages are necessary to deplete the GaN buffer layer. Therefore, the device shows normally-on behaviour.

In summary, for an efficient HFET a high resistant substrate is necessary. To avoid buffer leakage and to achieve a device with normally-off characteristics, a thin GaN buffer layer with a thickness of t<200 nm and a carrier concentration of n(GaN)<1×10^{16} cm^{-3} is an important precondition. In the following sections various alternatives for substrate insulation for epitaxy of cubic GaN and carbon doping of cubic GaN using a CBr_4 source as potential for the fabrication of compensated low-conductive epilayers will be discussed.

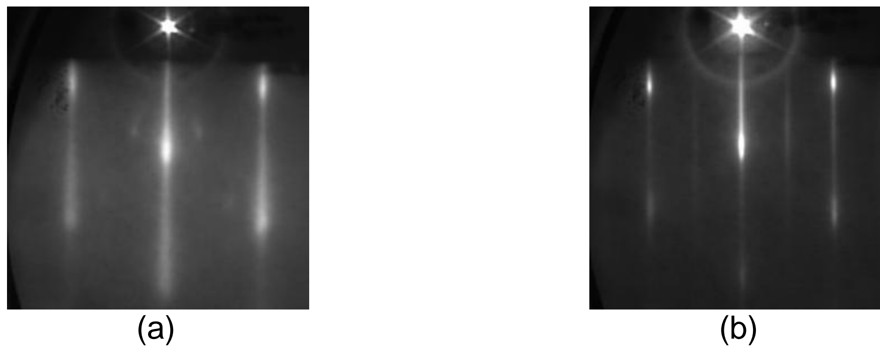


Figure 4.4 RHEED pattern in <110> direction at 720 °C of (a) carbonised Si (001) and (b) 600 nm thick cubic GaN on carbonised Si (001).

4.2 Carbonised Si (001)

One of the suitable substrates for epitaxy of cubic GaN is the so-called carbonised silicon (3C-SiC/Si) [36]. The 3C-SiC/Si substrates were fabricated by Dr. J. Pezoldt at the TU Ilmenau. For this substrate semi-insulating Si (001) with a resistivity of ρ=6 kΩ·cm was used. 34 nm 3C-SiC was deposited on the substrate using UHV-CVD with the gases SiH_4:C_2H_4:H_2=1.6:1.0:10 sccm at substrate temperature of 1050 °C. The deposition time was 60 min. The carrier concentration of the 3C-SiC/Si substrate was $p=7\times10^{11}$ cm^{-3} measured by Hall effect. The substrate resistivity was ρ=10 kΩ·cm measured by the four-point-method. One disadvantage of carbonised silicon is a high dislocation density of 3C-SiC due to a mismatch of 16.8 % between 3C-SiC and Si. The RMS roughness of the used 3C-SiC/Si was 1.6 nm.

Figure 4.4 shows the RHEED pattern of (a) 3C-SiC/Si and (b) 600 nm c-GaN grown on 3C-SiC/Si at 720 °C measured in <110> direction (sample 1747). The RHEED pattern of the substrate shows diffuse streaks overlaid with spotty reflexes. The RHEED pattern of the c-GaN shows sharper streaks and a (2×2)-reconstruction.

The RMS roughness of the 3C-SiC/Si was 1.6 nm and of the 600 nm GaN layer on the substrate it was 6 nm. The normalised high-resolution X-ray diffraction rocking curve of the symmetric (002) reflex of 3C-SiC/Si and 600 nm thick c-GaN is depicted in Figure 4.5 (a). The full width at half maximum (FWHM) of the ω-scans was 120 arcmin and 38 arcmin for the 3C-SiC and c-GaN, respectively. Since the FWHM is proportional to the dislocation density of a layer, the c-GaN epitaxy starts on the highly dislocation-rich 3C-SiC surface and the defects are released during the c-GaN growth. To investigate the hexagonal inclusions in c-GaN, the reciprocal space map (RSM) of the (002) reflex of c-GaN was measured as shown in Figure 4.5 (b). The hexagonal inclusions of this sample measured from the intensity ratio of the hexagonal (10-11) to the cubic (002) reflex were only 1 %.

Overall, the carbonised Si is a suitable semi-insulating substrate for cubic GaN epitaxy.

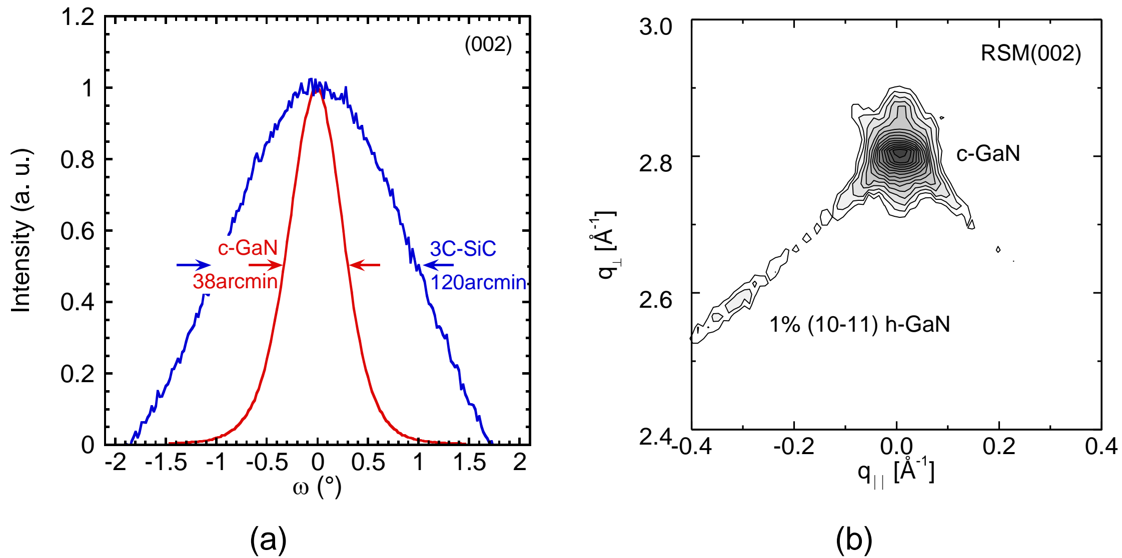


Figure 4.5 (a) Normalized high-resolution X-ray diffraction ω-scan of the symmetric (002) reflex of the 3C-SiC/Si and the 600 nm thick cubic GaN layer on the substrate. (b) Reciprocal space map of the (002) reflex of the 600 nm thick cubic GaN epilayer grown on 3C-SiC/Si (001).

4.3 Ar^+ Implanted 3C-SiC (001)

The most promising method for substrate insulation is up to now the Ar^+ implantation of 3C-SiC (001). For this process free standing 3C-SiC with a carrier concentration of $n=2\times10^{18}$ cm^{-3} was used and a three-fold energy implantation with Ar^+ ions at doses of 6×10^{14} cm^{-2} at 160 keV, 2.4×10^{14} cm^{-2} at 80 keV and 1.2×10^{14} cm^{-2} at 40 keV were performed by Prof. Dr. J.K.N. Lindner at the University of Augsburg. The idea was to induce a low-mobility insulating damage layer near the 3C-SiC surface.

Figure 4.6 (a) and (b) shows calculated Ar^+ density profiles in 3C-SiC and the calculated nuclear recoil energy profiles for the three implantation energies, respectively. The calculations were done using the simulation program SRIM2003.26 [37]. The total maximum Ar^+ density of $N_{Ar}=7\times10^{19}$ cm^{-3} is estimated to be between 30 and 130 nm below the surface. The amorphisation of a crystalline structure occurs around the maximum of the recoil energy profile curve. According to the calculation the strongest lattice damage is expected between 10 nm and 100 nm under the substrate surface.

Microstructures of the irradiated SiC were examined using cross-sectional transmission electron microscopy (TEM). The measurements were performed by Prof. Dr. J.K.N. Lindner at the University of Augsburg. The general cross-sectional view of the sample is shown in Figure 4.7 (a) where the crystalline, disordered and amorphised SiC layers are exhibited. The dotted lines are drawn to guide the eye. The thickness of the amorphised SiC layer is about 130 nm and correlates with the simulated data. Under Ar^+ implantation conditions a few top atomic layers at the surface of about 5 nm thickness are still crystalline as distinguishable in a high resolution TEM image in Figure 4.7 (b). A similar

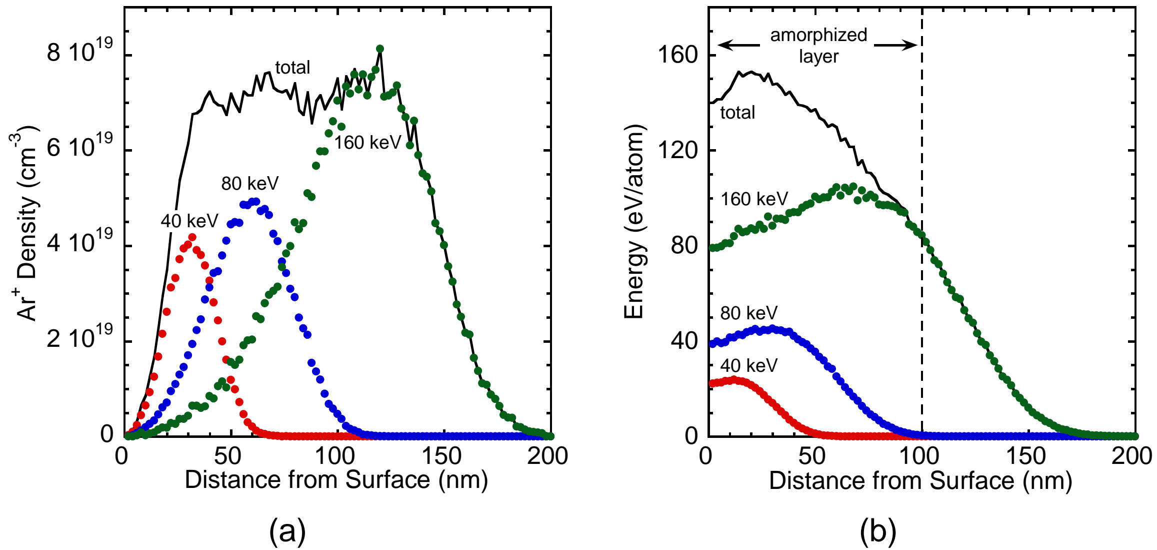


Figure 4.6 Calculated (a) Ar^+ density profiles and (b) nuclear recoil energy profiles of Ar^+ ions implanted at 40 keV, 80 keV and 160 keV.

layer structure was demonstrated of 6H-SiC after Au^+ ion implantation in [38]. However, in our samples the crystalline region at the substrate surface is not continuous and consists of crystalline 3C-SiC domains surrounded by amorphous SiC as depicted in the inset of Figure 4.7 (b).

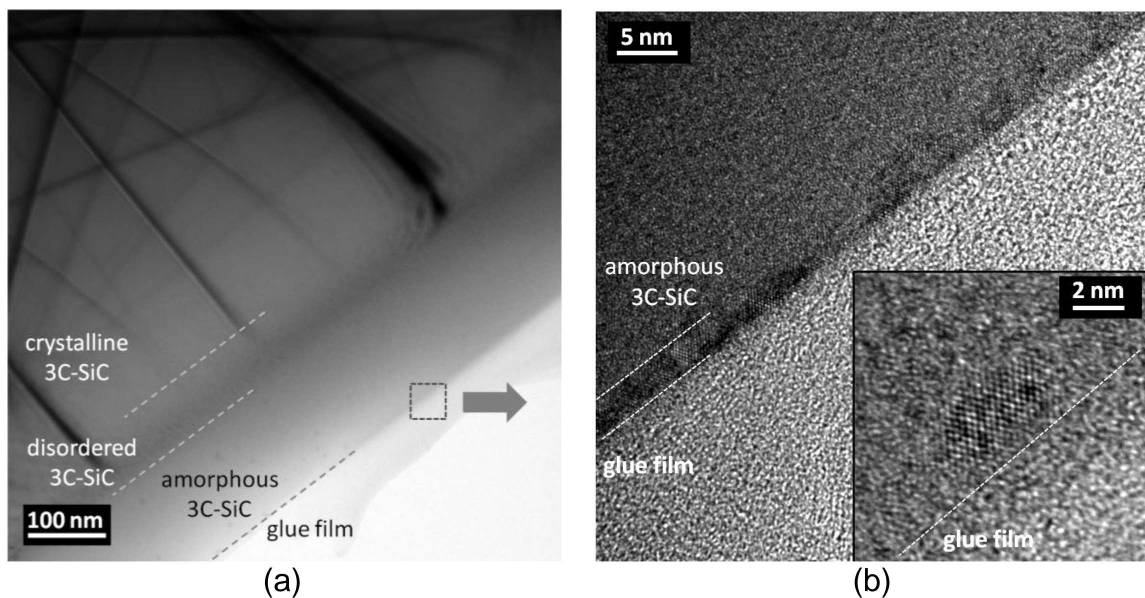


Figure 4.7 Cross-sectional TEM images of Ar^+ implanted 3C-SiC: (a) a general view at a low magnification, (b) shows a near surface region at a larger magnification; the inset in (b) shows a crystalline 3C-SiC domain in an amorphous SiC layer at the substrate surface.

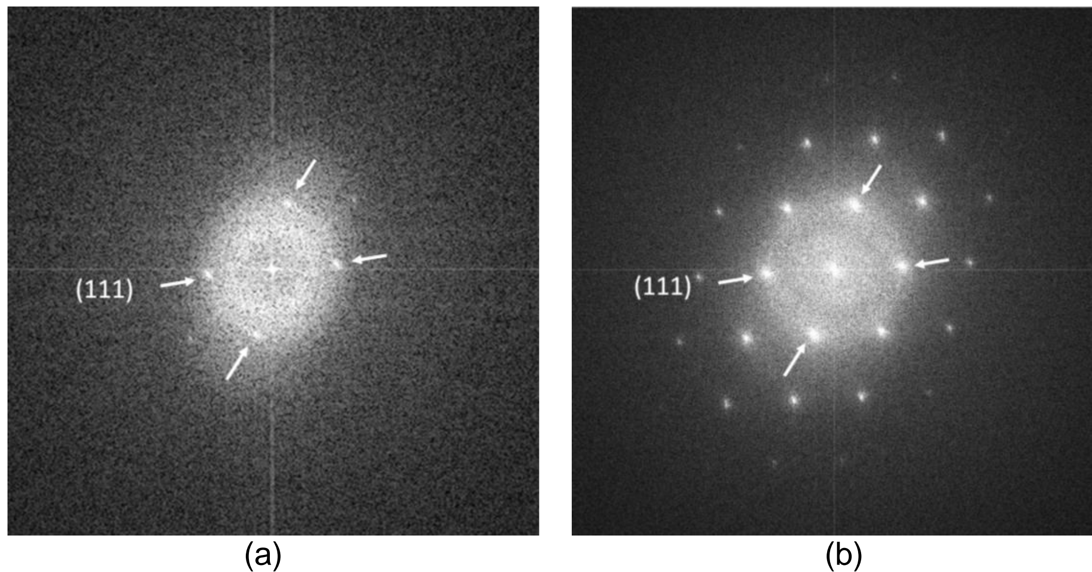


Figure 4.8 FFT image of (a) the inset in Figure 4.7 and (b) a mono crystalline 3C-SiC bulk substrate.

To verify the crystal orientation fast Fourier transformation (FFT) representing reflexes of the reciprocal crystal was performed of the inset of Figure 4.7 (b) and of a TEM image of a crystalline bulk 3C-SiC shown in Figure 4.8 (a) and (b), respectively. Four (111) reflexes are visible in the FFT image of the crystalline cluster at the substrate surface which are identical with the (111) reflexes of the 3C-SiC bulk material. This measurement shows that the thin crystalline 3C-SiC cluster layer exhibits the same crystal orientation as the bulk material and it has maintained its original orientation.

The formation of the amorphous SiC induces a colour change of the 3C-SiC. Free standing 3C-SiC is transparent yellow. After Ar^+ implantation the colour becomes opaque black as shown in Figure 4.9 (a) caused by the amorphous SiC and potentially by carbon clusters [39]. After thermal annealing at 800 °C for 30 min the SiC substrate becomes transparent as shown in Figure 4.9 (b), but it is still darker than the primary 3C-SiC.

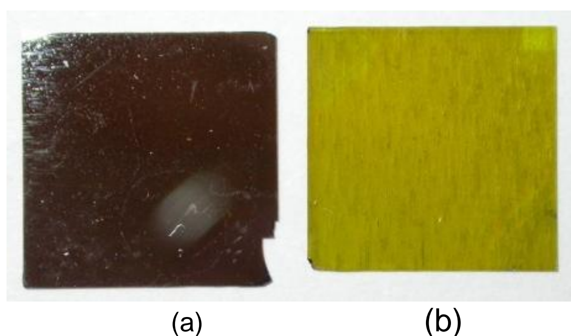


Figure 4.9 Ar^+ implanted 3C-SiC substrate (a) untreated and (b) after thermal annealing at 800 °C for 30 min.

The changes of the crystalline structure of the 3C-SiC substrate were controlled by high resolution X-ray diffraction (HRXRD). RSMs around the cubic (113) reflex of free standing 3C-SiC before Ar^+ implantation, after Ar^+ implantation and after Ar^+ implantation and subsequent thermal annealing are displayed in Figure 4.10 (a), (b) and (c), respectively. The RSM (113) of the untreated substrate features only a reflex of 3C-SiC (and a 3C-SiC twin reflex which is not typical and is observed only in wafer Nr. SFE14AT). After Ar^+ implantation a broadening below the 3C-SiC reflex in $q_\perp$ direction is observed. It can be explained by an expansion gradient of the 3C-SiC lattice constant in the disordered region due to additional Ar atoms. In addition it is known that amorphous SiC has an atomic density which is reduced by 20-30 % with respect to the crystalline state. One may therefore assume that damaged SiC exhibits an increased lattice constant.

Previous to c-GaN MBE the substrates are deoxidized at about 800 °C. Therefore, the Ar^+ implanted 3C-SiC was thermally annealed at 800 °C for 30 min. After the annealing process the broadening of the 3C-SiC reflex in the RSM has the shape of a separate reflex with a noticeable small FWHM. This is an evidence for a recrystallization of amorphous SiC by solid phase epitaxy studied in [40], [41] for 6H-SiC. For hexagonal SiC it was found that the recrystallization temperature varies between 750 °C and 1700 °C depending on different doses, ion species and the implantation temperature [42]. The volume increase of the 3C-SiC crystal after Ar^+ implantation and subsequent recrystallisation is 0.67 % calculated from the reflex positions of the both (113) 3C-SiC reflexes in Figure 4.10 (c). Thereafter, the lattice constant of the Ar^+ implanted 3C-SiC increases for 0.24 %. Additional Ar atoms in 3C-SiC crystal with a concentration of about 8×10^{19} cm^{-3} should cause a volume increase of only 0.16 %. This value is a factor of 4 lower than that measured from the reflexes in RSM (113). Therefore, the volume change of the Ar^+ implanted 3C-SiC is caused not only by the additional Ar atoms but also by lattice defects such as vacancies. For further analysis of the 3C-SiC recrystallisation investigations of Ar^+ implanted substrates after thermal annealing are necessary.

Figure 4.11 (a), (b) and (c) shows the RHEED patterns of a 3C-SiC, Ar^+ implanted 3C-SiC and 600 nm c-GaN grown on Ar^+ implanted 3C-SiC (sample 1855) measured at 720 °C in [110] direction. The RHEED pattern of both substrates was measured after the surface deoxidation at 800 °C. The RHEED pattern of the 3C-SiC offers a (2×4) reconstruction while a (1×1) reconstruction with diffuse streaks was observed in an Ar^+ implanted 3C-SiC surface. The RHEED pattern of the c-GaN shows sharper streaks and a (2×2)-reconstruction detecting two-dimensional surface.

The RMS roughness of the 600 nm c-GaN layer on the Ar^+ implanted 3C-SiC was 6 nm comparable with the roughness of c-GaN on 3C-SiC. The FWHM of the rocking curve of the 600 nm c-GaN was 25 arcmin. To investigate the hexagonal inclusions in c-GaN the RSMs of the (002) reflex of c-GaN were measured. The hexagonal inclusions of GaN measured on the intensity ratio of the hexagonal (10-11) to the cubic (002) reflex were of 0.6 % maximum in all samples. Herewith it was shown that Ar^+ implanted 3C-SiC is a suitable substrate for cubic GaN epitaxy.

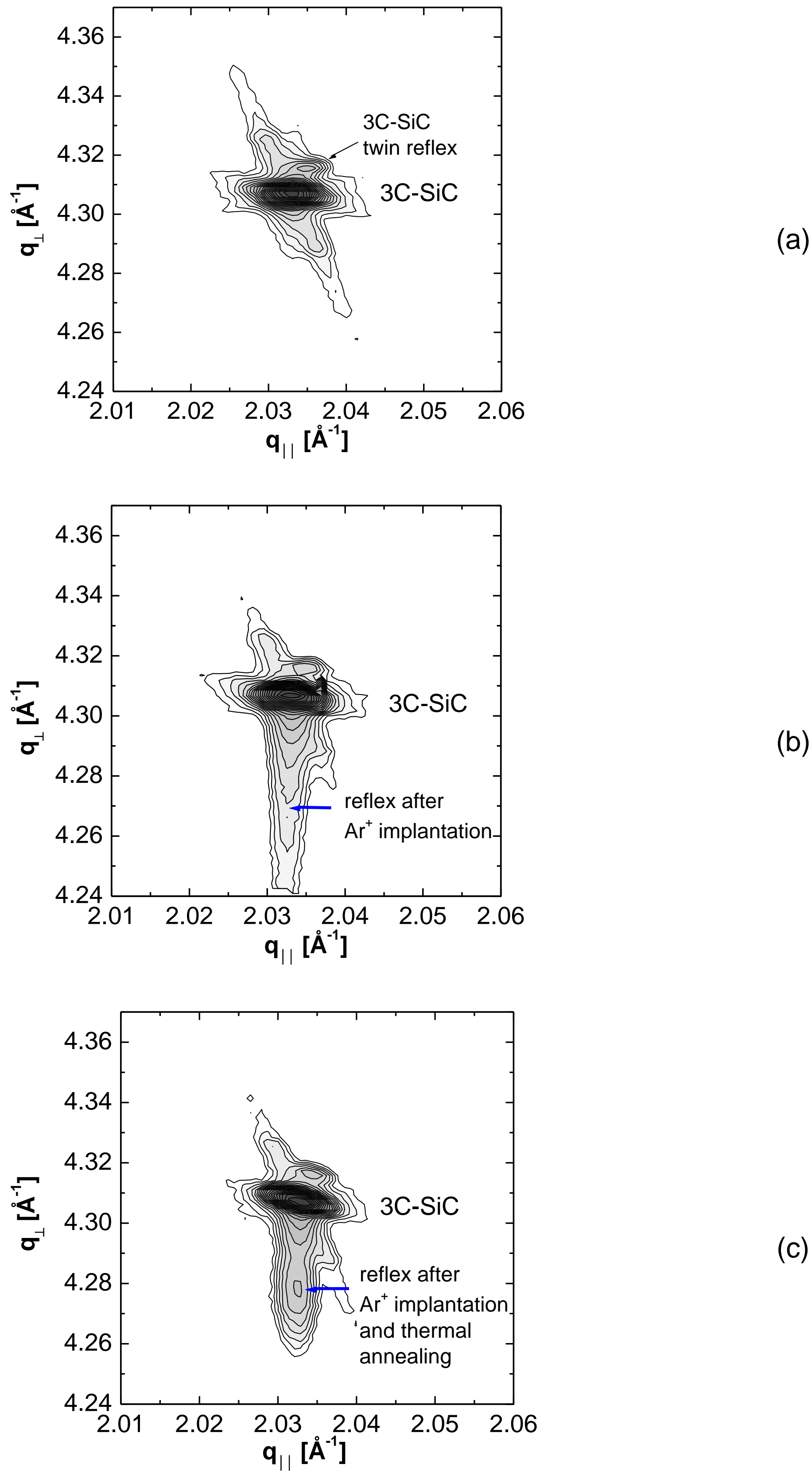


Figure 4.10 HRXRD-RSM around the cubic (113) reflex of free standing 3C-SiC (a) untreated, (b) after Ar^+ implantation, and (c) after Ar^+ implantation and thermal annealing at 800 °C for 30 min.

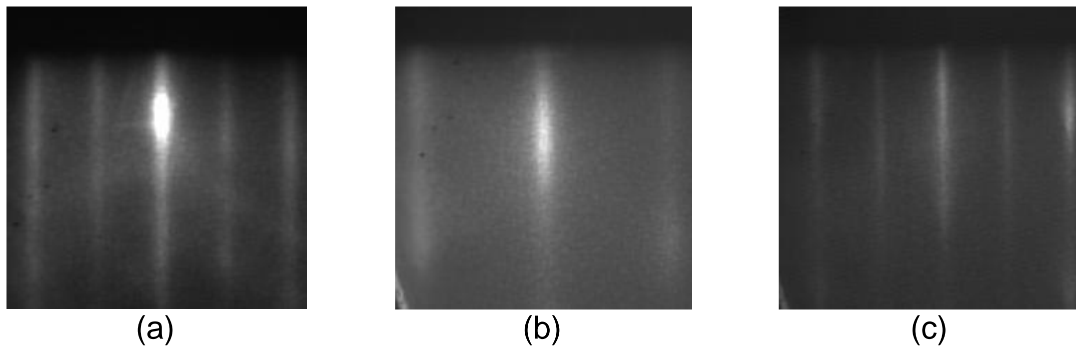


Figure 4.11 RHEED pattern measured in <110> direction at 720 °C of (a) 3C-SiC, (b) Ar^+ implanted 3C-SiC and (b) 600 nm thick cubic GaN on Ar^+ implanted 3C-SiC .

Electrical properties of Ar^+ implanted 3C-SiC before and after thermal annealing were investigated by IV measurements which were performed between a Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) contact on top and a large-area indium contact on the reverse side of the samples. The diameter of the top contact was 300 µm. Figure 4.12 (a) shows IV curves of Ar^+ implanted 3C-SiC before annealing and after thermal treatment at 800 °C for 30 min. The untreated substrate is highly conductive with a current density of I>35 A/cm^2 at V=1.5 V. After annealing the current is two orders of magnitude lower. Assuming that the thermal annealing induces a recrystallisation of an amorphised SiC layer, it can be concluded that the conductivity decrease of the 3C-SiC substrate is caused not by the amorphous SiC, but by residual defects remaining in the recrystallised layer.

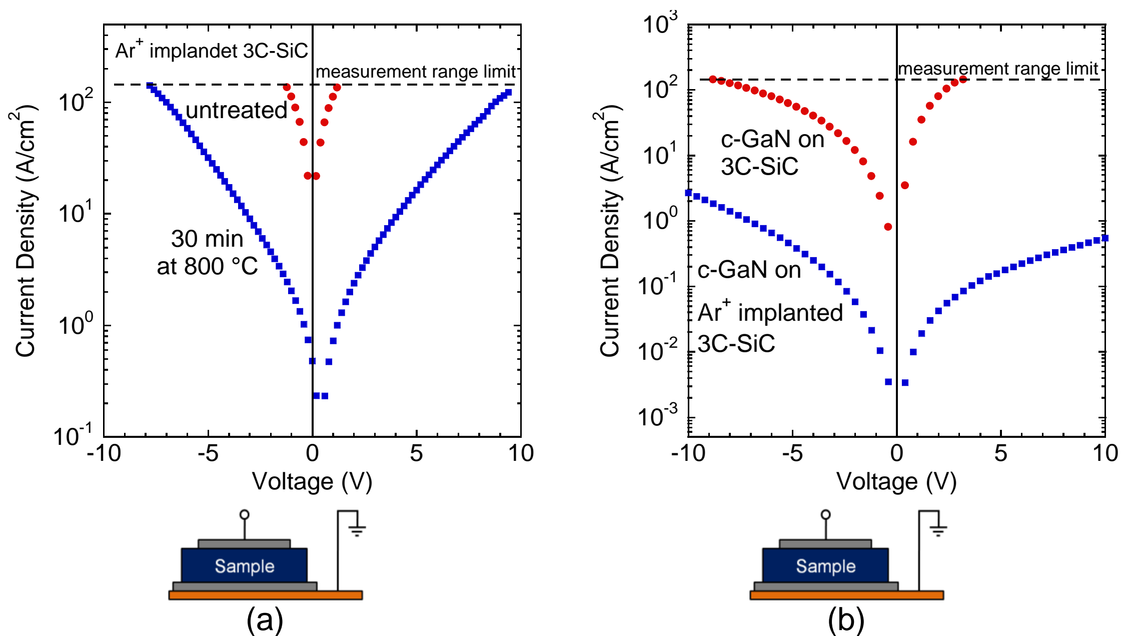


Figure 4.12 IV characteristics of (a) Ar^+ implanted 3C-SiC substrate before (red curve) and after thermal annealing (blue curves), and (b) c-GaN on free standing 3C-SiC without (red curve) and with Ar^+ implantation (blue curve).

Figure 4.12 (b) shows the IV curves of 600 nm c-GaN on 3C-SiC without and with Ar^+ implantation. These measurements were performed on Ti/Al/Ni/Au (15 nm/50 nm/ 15 nm/50 nm) contacts which were thermally annealed at 800 °C for 30 s. The current density through the c-GaN/3C-SiC is lower than through the 3C-SiC substrate caused by the low carrier density of c-GaN of $n \approx 5\times10^{16}$ cm^{-3}. The current through the c-GaN on Ar^+ implanted 3C-SiC is a factor 2000 lower than that through the c-GaN on the untreated substrate measured at 2 V forward bias.

Thus, it was demonstrated that Ar^+ implantation of 3C-SiC is an effective method to induce an isolating layer between the c-AlGaN/GaN HFET devices and the highly conductive substrate with only low degradation of crystalline properties of epitaxial c-GaN layers.

4.4 Carbon Doping of Cubic GaN

Another alternative for device isolation is the epitaxy of a semi-insulating c-GaN buffer layer. However, nominally undoped GaN typically shows *n*-type conductivity, presumably due to doping by residual oxygen impurities [43]. Therefore, achievement of a highly insulating GaN buffer prior to the deposition of AlGaN/GaN hetero structures has not been an easy task. To solve this problem, several approaches have been proposed. Using Fe [44], Be [45], and Zn [46] as acceptor-like point defects, semi-insulating hexagonal GaN films were also successfully grown by metal-organic chemical vapour deposition (MOCVD), MBE and hydride vapour phase epitaxy (HVPE) technique, respectively. Techniques incorporating carbon in hexagonal GaN buffer layers have been commonly used to obtain a highly resistive GaN buffer [47], [3], whereas the use of carbon tetra-bromide (CBr_4) as a carbon source shows great potential for doping of hexagonal GaN [48], [49]. The carbon doping of cubic GaN by CBr_4 was investigated in this work and the experimental results are summarized in this chapter.

The carbon source was a self-made CBr_4 sublimation source connected directly to the MBE chamber. The cylinder with solid CBr_4 powder is put into a heating jacket with a temperature controller. The source temperature can be varied from -15 °C and +50 °C. The gas line is permanently heated to 80 °C. The vapour pressure can be varied by the source temperature and by the opening the needle valve. Figure 2.3 shows the calibration curve of the CBr_4 source. For this calibration the needle valve of the CBr_4 source was fully opened (9-part), the source temperature was varied, and the beam equivalent pressure (BEP) was measured at the sample position.

Figure 4.13 shows the cross sectional view of carbon doped samples. For this investigation a free standing 3C-SiC (001) substrate with a carrier density of $n=2\times10^{18}$ cm^{-3} was used. A 65 nm thick UID c-GaN nucleation layer was deposited followed by a 530 nm c-GaN:C and a 130 nm UID c-GaN cap layer. The CBr_4 BEP of 2.5×10^{-7} mbar (sample 1832, A), 3.4×10^{-6} mbar (sample 1833, B) and 4.5×10^{-6} mbar (sample 1843, C) was preset. The undoped c-GaN cap layer was deposited to ensure similar electrical contacts on top of all samples. The reference sample was a 715 nm UID c-GaN layer (sample 1834, D).

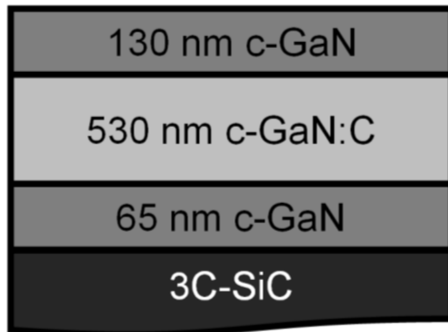


Figure 4.13 Cross-sectional view of investigated carbon doped C-GaN:C samples. The carbon BEP was set to 2.2×10^{-7} mbar, 3.4×10^{-6} mbar, and 4.5×10^{-6} mbar for three different samples, respectively.

The FWHM of the rocking curve of all c-GaN:C layers was about 25 arcmin. Thus, no deterioration in the structural quality is associated with carbon doping. This is supported by AFM scans which show a surface morphology typical of c-GaN MBE growth with a RMS roughness of 5-6 nm. To investigate the hexagonal inclusions in c-GaN:C RSMs around the (002) reflex of c-GaN were measured. The hexagonal inclusions of c-GaN:C measured on the intensity ratio of the hexagonal (10-11) to the cubic (002) reflex of c-GaN were comparable with those of the UID c-GaN sample. Thus no impact of carbon is seen on the structural or morphological properties of the films.

Time-of-flight secondary ion mass spectrometry (ToF-SIMS) was used to quantify the carbon incorporation behaviour. The measurements were performed by Dr. J.W. Gerlach at the IOM Leipzig. In Figure 4.14 (a) the measured depth profiles of $Ga^{69}N$, O, CN, and C of c-GaN:C sample C grown at CBr_4 BEP of 4.5×10^{-6} mbar are depicted. Whereas the GaN concentration is constant all over the c-GaN epilayer thickness, a clear region with higher carbon concentration in the distance between 130 nm and 660 nm from the surface can be identified in the C-profile. This region is detected in the CN signal with higher intensity. Therefore, the intensity of the CN signal will be used for further analysis. The bromine concentration was at the SIMS detection limit of $\sim10^{15}$ cm^{-3}. Additionally, the oxygen level did not appear to increase beyond the low unintentionally impurity level of $\sim10^{16}$ cm^{-3} typical of our c-GaN films.

For the calibration of the measurement data a SIMS measurement of a carbon ion (C^+) implanted 650 nm thick c-GaN layer (sample 1663) was done. The C^+ implantation was performed by Dr. H. Karl at the University of Augsburg. For room temperature C^+ implantation doses of 1×10^{15} cm^{-2} (sample I1) and of 1×10^{14} cm^{-2} (sample I2) at 60 keV were used. Figure 4.14 (b) shows the $CN/Ga^{69}N$ signal profiles of the calibration c-GaN layers (blue and black curves) and c-GaN:C layer sample C (green curve). For the calibration of the carbon concentration scale the integrated carbon concentration of sample I1 and I2 were calculated using the C implantation doses. The red dotted curve is the simulated C^+ implantation profile of the calibration sample I1 using the Monte-Carlo simulation software SRIM-2008. Thus, a maximum carbon concentration of 9×10^{19} cm^{-3} was achieved in the calibration sample I1 and a medium carbon concentration of 2.7×10^{19} cm^{-3} in the GaN:C sample C with the highest carbon doping density. In Figure 4.15 the incorporated carbon concentrations of samples A, B, and C are plotted vs. the

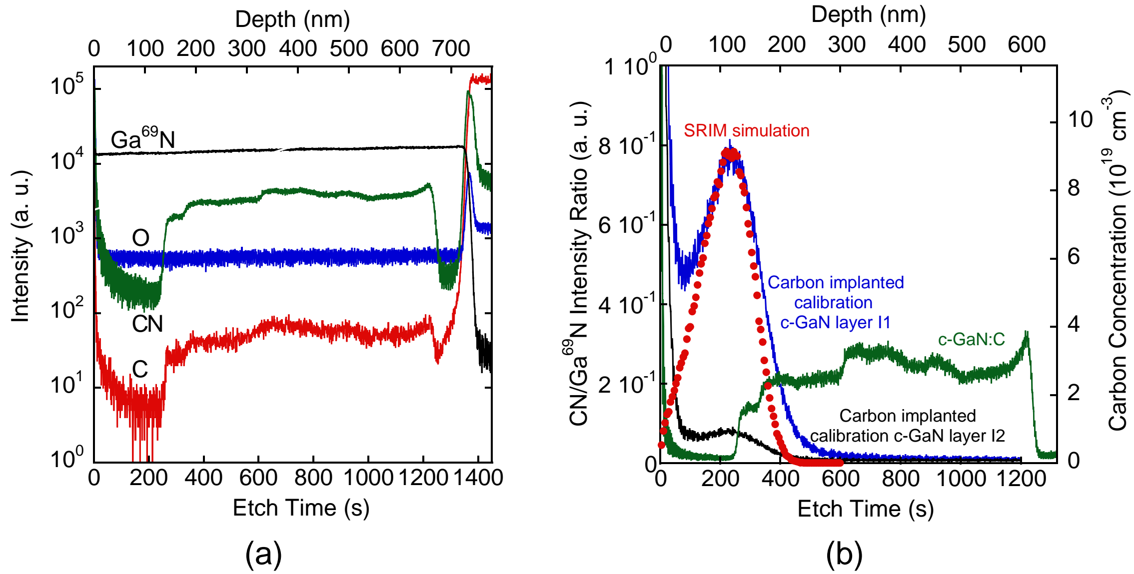


Figure 4.14 (a) SIMS depth profiles of $Ga^{69}N$, O, CN and C of a c-GaN:C epilayer grown with CBr_4 BEP of 4.5×10^{-6} mbar (sample C). (b) $CN/Ga^{69}N$ ratio profiles of the same c-GaN:C sample and of a carbon implanted c-GaN calibration sample with simulated carbon concentration.

CBr_4 BEP, respectively. This measurement shows that the amount of the incorporated carbon is linearly related to the incident CBr_4 flux. The carbon concentration of 3×10^{18} cm^{-3}, 1.6×10^{19} cm^{-3} and 2.7×10^{19} cm^{-3} was measured in samples A, B, and C, respectively.

The net donor N_D-N_A and acceptor N_A-N_D concentration was investigated by capacitance-voltage (C-V) measurements. Figure 4.16 (a), (b), and (c) show room temperature C^{-2}-V characteristics of the three carbon doped c-GaN samples A, B and C.

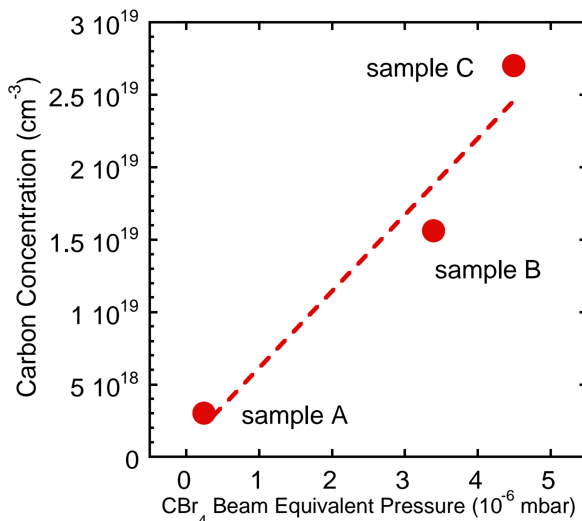


Figure 4.15 Incorporated carbon concentration measured by SIMS vs. CBr_4 BEP.

The measurements were performed at 1 MHz and 50 mV AC level. A noticeable difference of the measurement diagrams is the negative slope of the curves (a) and (b) and the positive slope of the curve (c). This behaviour points to a donor N_D surplus in samples A and B and to an acceptor N_A surplus in sample C. In order to investigate the doping profiles the model of parallel-plate capacitor was used with the abrupt approximation that the charge density $\rho \approx qN_D$ for $x < W_D$, $\rho \approx 0$ for $x > W_D$, where W_D is the depletion width. According to this approximation the non-compensated impurity concentration can be calculated from [33]

$$N_D - N_A = \frac{2}{q\varepsilon_s A^2}\left[-\frac{1}{dC^{-2}/dV}\right] \tag{4.1}$$

where A is the area of the contact and ε_s the dielectric constant of the semiconductor. The distance from the surface is given by

$$W_D = \frac{\varepsilon_s A}{C}. \tag{4.2}$$

The linear curve behaviour of C^{-2}-V measurement data points to homogeneous doping profiles of the samples in the measured depth section. Using Equation 4.1 the net doping density of N_D-N_A=8.7×10^{16} cm^{-3}, N_D-N_A=9.4×10^{16} cm^{-3} and N_A-N_D=2.8×10^{17} cm^{-3} was calculated in sample A, B and C, respectively. The depletion width W_D was calculated using Equation 4.2 at V=0 V and is 245 nm for sample A and 575 nm for sample B. Due to the complex layer structure Equation 4.2 is not appropriate to calculate the depletion width of sample C. The measured net doping density of sample B is higher than that of sample A, but the N_D of sample A was apparently measured on the c-GaN:C layer and the $N_D$of sample B was measured on the UID c-GaN buffer below the c-GaN:C layer.

For conductivity investigations of c-GaN:C IV measurements through the layers vertical to the surface were performed. The upper contacts were thermally evaporated Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) contacts with 300 µm diameter annealed at 850 °C for 30 s. The reverse side of the 3C-SiC substrates were contacted to a copper board using indium. The IV curves of three carbon doped c-GaN:C samples and an UID c-GaN layer are depicted in Figure 4.17 (a). The UID c-GaN reference layer of sample D has the highest conductivity. The electrical conductivity of sample A with a carbon concentration of N_C=3×10^{18} cm^{-3} is one order of magnitude and the conductivity of sample B with N_C=1.6×10^{19} cm^{-3} is two orders of magnitude lower than that of the reference c-GaN measured at 2 V forward bias. Sample C with the highest carbon concentration of N_C=2.7×10^{19} cm^{-3} exhibits a high electrical conductivity which is only three times lower than the conductivity of the undoped reference c-GaN measured at 2 V forward bias. The current density at 2 V forward bias of all four samples is compared in Figure 4.17 (b). These measurements show that the carbon doping of c-GaN using CBr_4 is a useful alternative for the fabrication of insulating c-GaN:C buffer layers whereas the optimum carbon density for this purpose has still to be found.

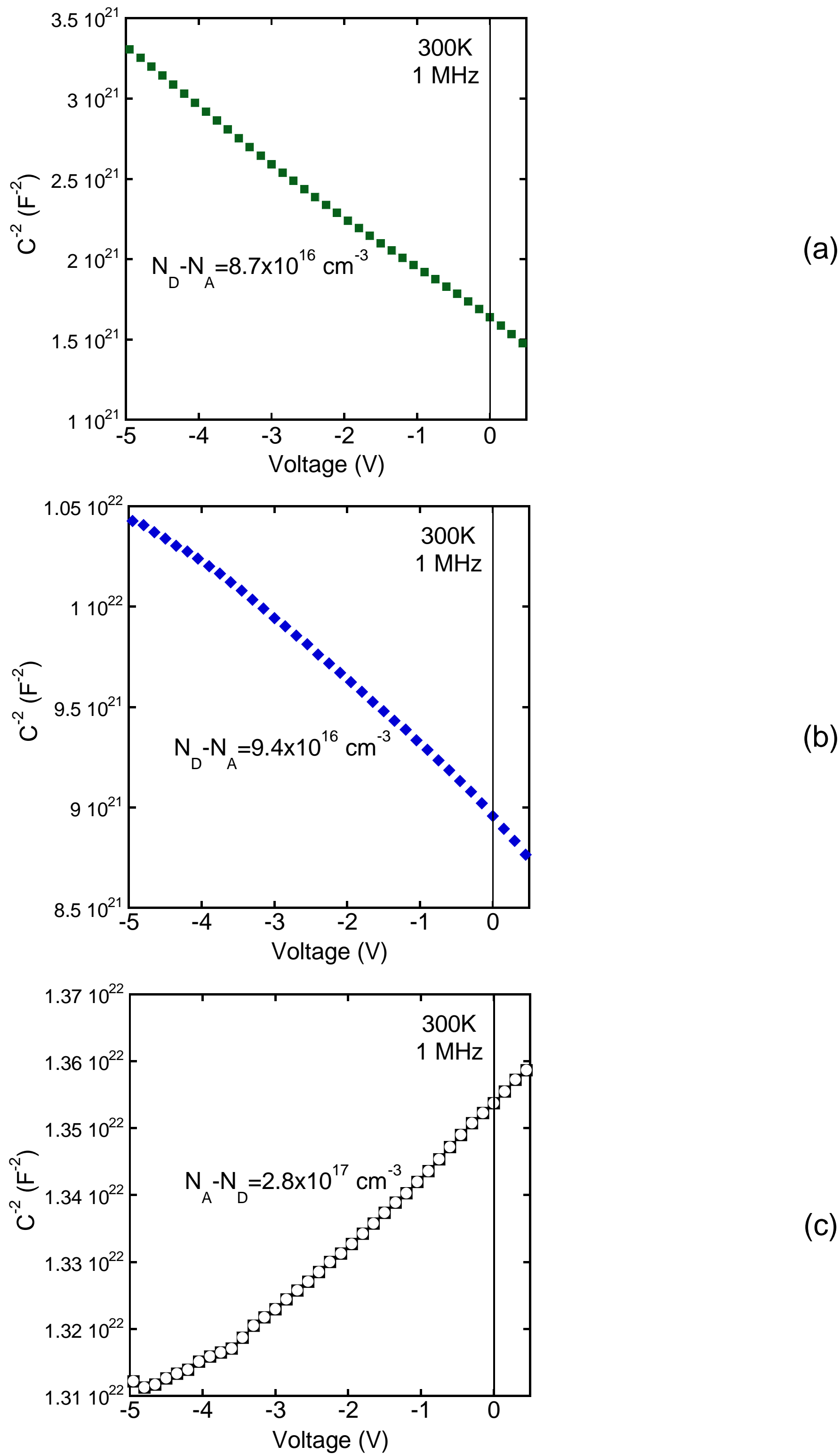


Figure 4.16 Room temperature C^{-2}-V characteristics of c-GaN:C with incorporated carbon concentration of (a) 3×10^{18} cm^{-3} (sample A), (b) 1.6×10^{19} cm^{-3} (sample B) and (c) 2.7×10^{19} cm^{-3} (sample C) measured at 1 MHz.

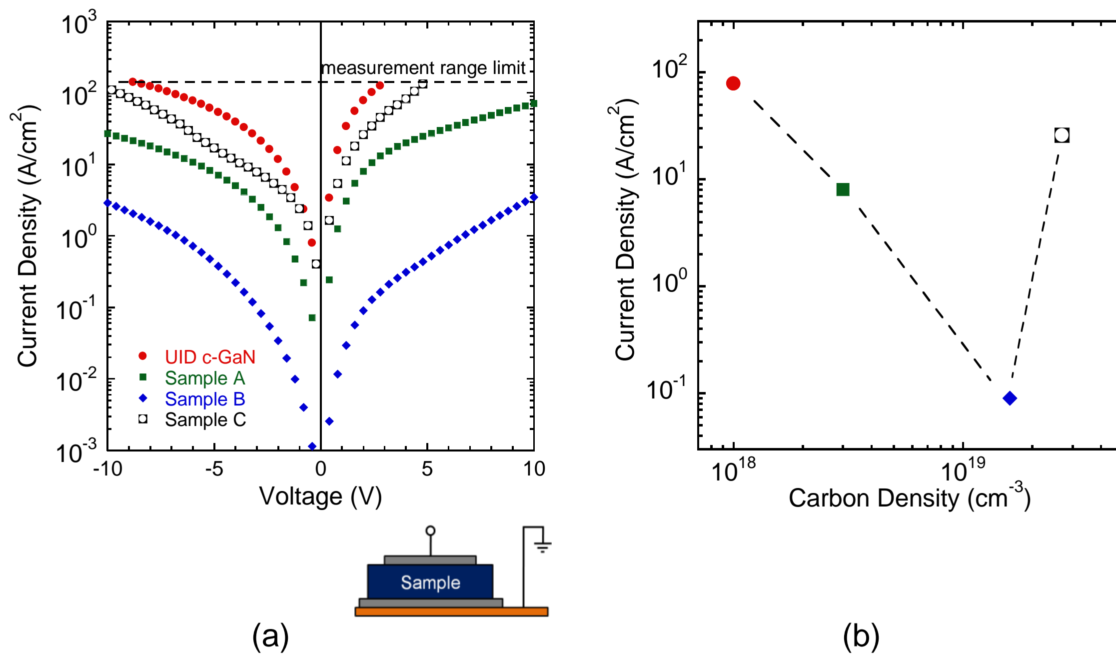


Figure 4.17 (a) IV characteristics of carbon doped c-GaN. (b) Current density at 2 V forward bias vs. carbon density.

For optical characterization photoluminescence (PL) measurements were performed on all carbon doped GaN:C epilayers. Figure 4.18 shows different photoluminescence transition energies of c-GaN:C at 2 K [50]. The typical PL transitions of UID c-GaN are the band-to-band (*e, h*) transition at 3.3 eV, the free exciton (*X*) transition at 3.26 eV and the donor-acceptor pair (D^0A^0) transition at 3.15 eV. The carbon related transitions in c-GaN:C are the band-carbon-acceptor (eA_C^0) recombination at 3.08 eV, the donor-carbon-

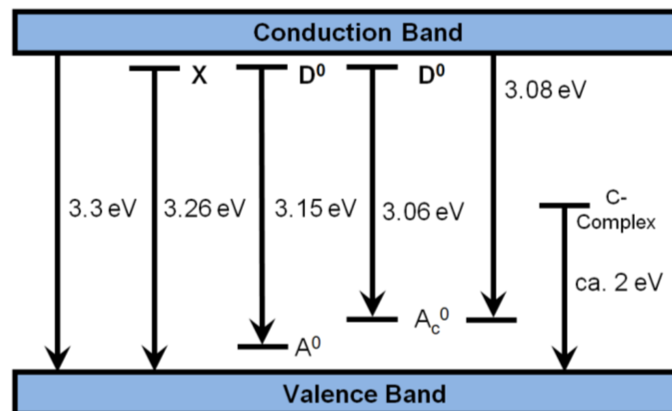


Figure 4.18 Potential photoluminescence transition energies of carbon doped c-GaN:C at 2 K [50]-[53].

acceptor ($D^0A_C{}^0$) transition and a deep level transition (*C-complex*) around 2 eV [51]-[53].

Figure 4.19 shows PL spectra of three c-GaN:C samples and of the reference c-GaN between 1.8 eV and 3.4 eV. The intensity of the X-transition is normalized to 1 and the spectra are offset against each other. Unlike in [52] and [53] only a weak deep luminescence centered around 2 eV was observed in c-GaN:C and this orange luminescence was most distinct in sample A with the lowest carbon concentration of 3×10^{18} cm^{-3}. This behavior indicates that by doping with CBr_4 under one mono layer Ga growth conditions carbon is not incorporated as a complex in contrast to earlier investigations using e-beam evaporated atomic carbon. High resolution PL spectra of the investigated c-GaN:C layers between 2.8 eV and 3.35 eV are depicted in Figure 4.20. Beside the well-known lines of UID c-GaN at 3.26 eV (*X*) and 3.15 eV (D^0A^0) a carbon related ($eA_C{}^0$) PL-band at 3.08 eV appears with increasing carbon concentration in c-GaN:C. The highest intensity of the ($eA_C{}^0$) transition was observed in sample C with the highest carbon concentration of 2.7×10^{19} cm^{-3}. In this sample an acceptor surplus N_A-N_D was measured by the CV method.

The doping of c-GaN with carbon using CBr_4 requires further investigations. The introduced investigations on c-GaN:C showed two different potential alternatives for the use of carbon doping for the growth of insulating c-GaN buffer layers. The first one is the compensation of negative background carriers as in sample B. The second possibility is the fabrication of e.g. a pn-junction of c-GaN as a buffer which would allow only lateral conduction through the electron channel at the c-AlGaN/GaN interface and would interrupt conductivity to the conductive substrate.

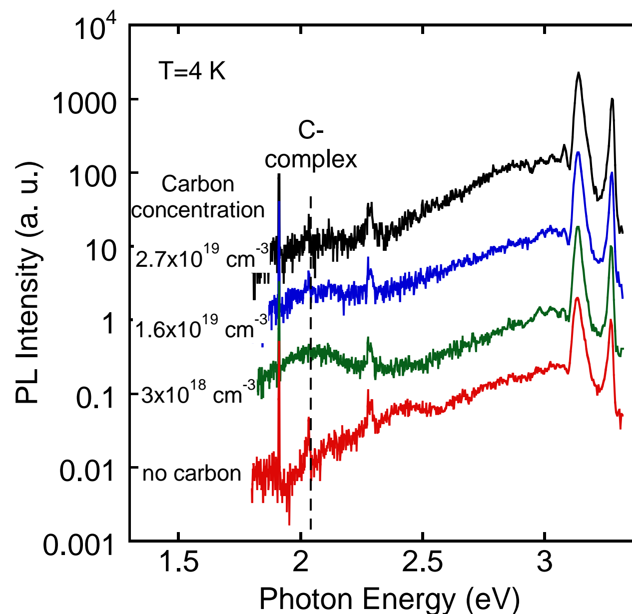


Figure 4.19 Low-temperature PL spectra of carbon doped c-GaN epilayers. The intensity of the X-transition at 3.27 eV is normalized to 1. The spectra are offset against each other for reasons of better clarity.

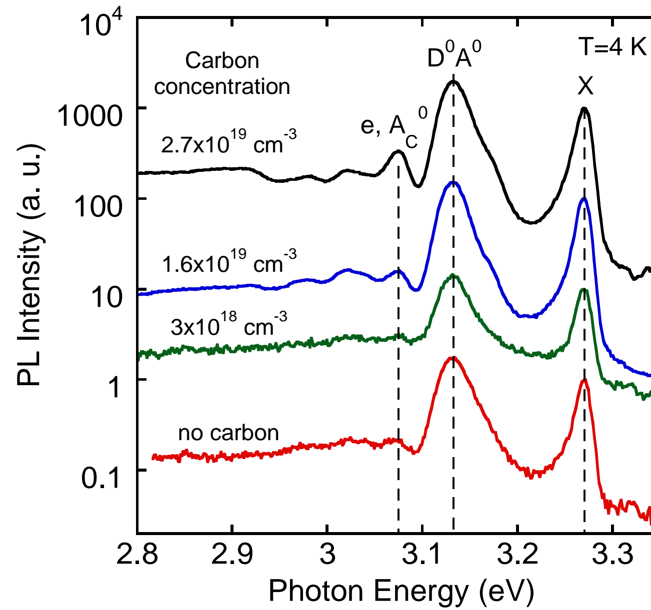


Figure 4.20 Low-temperature PL spectra of carbon doped c-GaN epilayers. The intensity of the X-transition at 3.27 eV is normalized to 1. The spectra are offset against each other for reasons of better clarity.

In this chapter, the necessity of an electrical isolation between the HFET devices and the substrate/buffer was demonstrated. It was shown that the shunt current through the c-GaN buffer layer can be reduced by reducing of the UID c-GaN thickness. It is also possible to decrease the conductivity of the c-GaN by carbon doping using CBr_4. The shunt current through the substrate can be avoided by use of the semi-insulating carbonised 3C-SiC/Si or by a damage layer near to the surface of the highly conductive 3C-SiC using Ar^+ implantation and subsequent thermal annealing.

5 Properties of Cubic AlGaN/GaN Field Effect Transistors

In this chapter, cubic AlGaN/GaN hetero-structures for fabrication of hetero-junction field-effect transistors (HFETs) will be presented. First the structural properties of cubic AlGaN/GaN samples and the analysis of the electron channel at the hetero-interface will be described. Then the output characteristics of the fabricated cubic HFETs on different substrates will be introduced.

5.1 Properties of Cubic $Al_xGa_{1-x}N$/GaN Hetero-Structures

Cubic AlGaN/GaN hetero-structures for HFETs were grown by plasma-assisted MBE. In order to minimize hexagonal inclusions in our layers and to obtain optimum interface roughness a coverage of one monolayer Ga was established during growth [17]. The substrate growth temperature was 720 °C. The growth rate of all samples was 115-120 nm/h.

The investigated c-AlGaN/GaN hetero-structures were deposited on free-standing 3C-SiC (HOYA), on Ar^+ implanted free-standing 3C-SiC, and on carbonized silicon (3C-SiC/Si) substrates. The properties of the different substrates are described in Chapter 4. The c-GaN buffer layer generally was about 600 nm thick. The c-AlGaN barrier layer was about 20-30 nm thick. The Al mole fraction of c-AlGaN was measured by the position of the c-AlGaN reflex in the reciprocal space map (RSM) around the asymmetrical (-1-13) reflex of cubic GaN shown in Figure 2.5 (b). The Al content of all samples varied between 33-36 %. In all samples, the c-AlGaN was pseudomorphically strained on the c-GaN, indicated by the position of the c-AlGaN reflex relative to the c-GaN reflex in the asymmetrical RSM depicted also in Figure 2.5 (b). The full width at half maximum (FWHM) of the c-GaN (002) rocking curve was between 22 arcmin on free standing 3C-SiC and 38 arcmin on carbonized Si. According to the model by Gay et al. [23] the dislocation density of the samples was between 4×10^9-1×10^{10} cm^{-2}, respectively. The RMS roughness of the sample's surface measured by AFM in a 5×5 μm^2 scan was 3-6 nm.

To detect the electron channel at the c-AlGaN/GaN interface electrical and optical measurements were performed. For the electrical characterization room temperature electrochemical capacitance-voltage (ECV) measurements [54] were done on a c-$Al_{0.35}Ga_{0.65}N$/GaN hetero-structure (sample 1865) and on a c-GaN reference layer (sample 1868) by Dr. S. Li at the University of Braunschweig. The advantage of ECV over CV measurement is that the DC bias of the semiconductor is set to 0 V during the whole

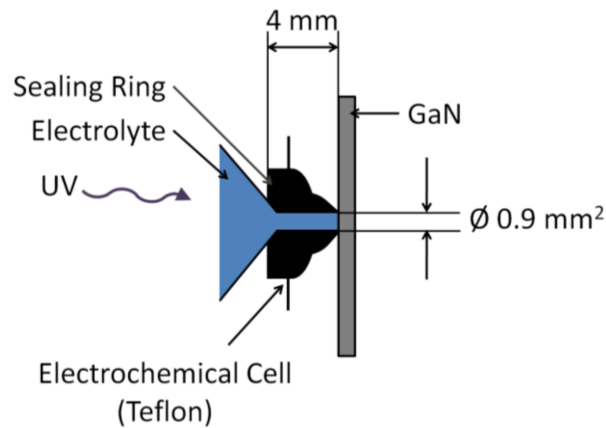


Figure 5.1 Cross-sectional view of an electrolyte/semiconductor interface area for electrochemical capacitance-voltage (ECV) measurements.

measurement and no parallel conductivity degrades the measured capacity. The essential part of the electrochemical setup is shown in Figure 5.1. For the ECV measurements, the electrochemical cell was filled with a 0.01 mole KOH aqueous solution (pH=12). Under a defined force the vertically hold semiconductor sample was pressed on the sealing ring defining an area of 0.9 mm². The electrolyte was used as a Schottky contact. The ohmic contact was performed by an InGa eutectic. To etch the *n*-type c-GaN and c-AlGaN material, UV illumination of a 100 W high pressure mercury lamp was focussed by a fused silica lens system through the electrolyte towards the interface. A PC-system was used to run the complete measurement in an automated mode. The automatically adjusted measurement frequency was 10-20 kHz.

The measured ECV data were used for the calculation of electron density profiles of the layers. Figure 5.2 shows the measurement data of the investigated c-AlGaN/GaN (red dots) and c-GaN (blue squares) layers. The apparent electron density profile of the c-GaN is nearly constant at c-GaN depth >120 nm with N_{ECV}=8×10^{17} cm^{-3} whereas the first measured electron density value is lower with N_{ECV}=5×10^{17}. This increase in the evaluated donor concentration with increasing etch depth is caused by a roughened etched area due to the relatively high dislocation density which was observed in all ECV samples. The carrier density measured on the same sample by CV with SiO_2/Ni/Au (6 nm/15 nm/50 nm) MOS contacts at 10 KHz-1 MHz was N_{CV}=2×10^{17} cm^{-3} in entire c-GaN layer thickness. Therefore, these ECV measurement data are not capable for measuring the absolute carrier density. They demonstrate simply that no significant changes in electron density were observed in the c-GaN layer. In contrast to the c-GaN layer the electron density of the c-AlGaN/GaN increases near the hetero-interface from 3×10^{17} cm^{-3} to 1×10^{19} cm^{-3}. The depth resolution of the ECV measurement is not suitable to detect the exact position of the electron channel. Taking the measuring error into account the maximum electron density is positioned 20-40 nm under the sample surface. This is in a good agreement with the thickness of the AlGaN layer of 30 nm. Therefore an electron accumulation building a channel at the c-AlGaN/GaN interface was verified by the electrochemical CV measurements.

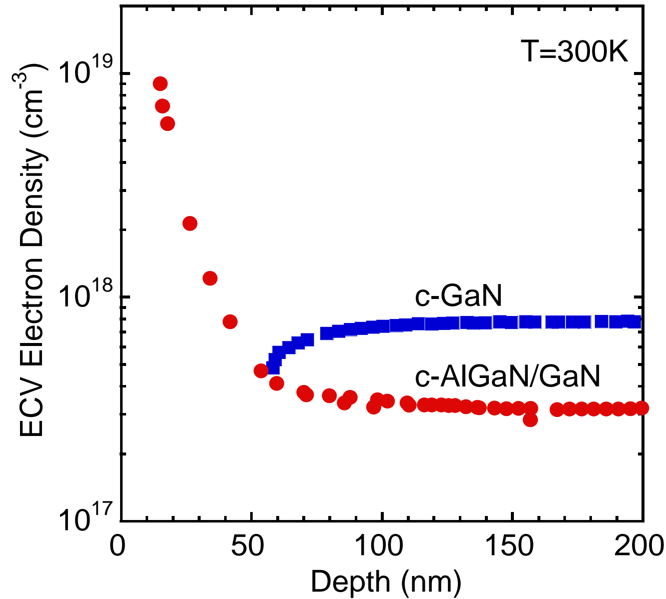


Figure 5.2 ECV electron density profile of the c-AlGaN/GaN hetero-structure (red dots) and the reference c-GaN layer (blue squares).

Unfortunately, the resistivity of all suitable substrates for the growth of c-AlGaN/GaN is with $\rho \approx 0.05\ \Omega\cdot$cm quite low and the substrates are highly conductive. Therefore, it was not possible to measure the Hall effect on cubic nitrides grown on these substrates and we do not have any data about the Hall mobility of the electron channel at the c-AlGaN/GaN hetero-interface.

The second method to detect the electron channel was photoluminescence (PL). The detailed theory for the optical characterization of cubic AlGaN/GaN hetero-structures is given in [20], [55]. Figure 5.3 shows a low temperature PL spectrum of a c-$Al_{0.33}Ga_{0.67}N$/GaN hetero-structure (sample 1793). The c-GaN buffer layer was 200 nm and the $Al_{0.33}Ga_{0.67}N$ cap layer was 20 nm thick. In this PL spectrum a clear peak at about 3.23 eV was observed in addition to the well known excitonic transition at 3.26 eV (X) and the donor-acceptor transition at 3.15 eV (D^0A^0) of cubic GaN [50]. This optical emission process, referred to as the H-band, has been related to the recombination of confined and free carriers near the interfacial band bending region and can be classified as an optical detection of 2-DEG.

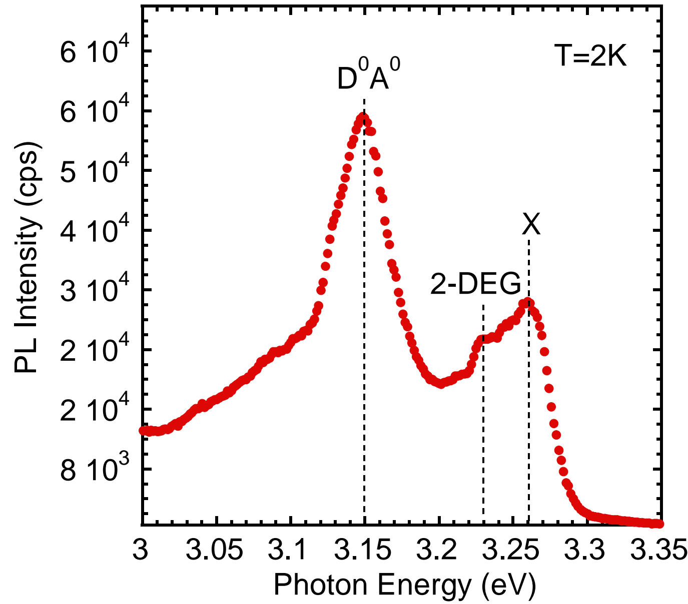


Figure 5.3 Photoluminescence (PL) spectrum of a c-AlGaN/GaN hetero-structure.

5.2 HFETs of Cubic $Al_xGa_{1-x}N/GaN$

Cubic $Al_xGa_{1-x}N$/GaN hetero-structures were used to perform hetero-junction field-effect transistors. A basic HFET structure based on an AlGaN/GaN system is shown in Figure 5.4 (a). It is seen here that the barrier layer AlGaN under the gate is doped, while the channel layer GaN is undoped. In our c-AlGaN/GaN hetero-structures the GaN buffer layer is unintentionally doped (UID) with a typical background doping concentration of n_{GaN}=1×10^{16}-1×10^{17} cm^{-3}. Due to the high affinity of Al to oxygen the aluminium forces the incorporation of oxygen into the c-AlGaN film. Oxygen acts as a shallow donor in the group-III nitrides if it occupies the N site, which is then responsible for the UID n-type doping. Therefore, the UID background concentration of c-AlGaN with Al mole fraction of 30-40 % is at least one order of magnitude higher than that of the c-GaN [20] and an additional doping of the c-AlGaN barrier is not necessary. In these HFETs carriers from the doped barrier layer are transferred to reside at the hetero-interface and are away from the doped region to avoid impurity scattering. The doped barrier is typically around 20-30 nm thick. Often, a δ-doped charge sheet is used within the barrier layer and placed close to the channel interface instead of uniform layer doping. The source/drain deeper n^+-regions are formed by an alloying step. The source and drain contacts are of ohmic and the gate contact of Schottky type.

Figure 5.4 (b) shows a scanning electron microscope (SEM) micrograph of a fabricated HFET of cubic AlGaN/GaN. The device has a gate length of 2 µm, a gate width of 25 µm and a source-to-drain spacing of 8 µm. The used mask drafts are shown in Chapter 2.4 and in Appendix E. First, Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) was thermally evaporated and annealed at 850 °C for 30 s in nitrogen atmosphere to form source and drain contacts with an ohmic characteristics. Then, c-AlGaN/GaN mesas were formed by $SiCl_4$ reactive

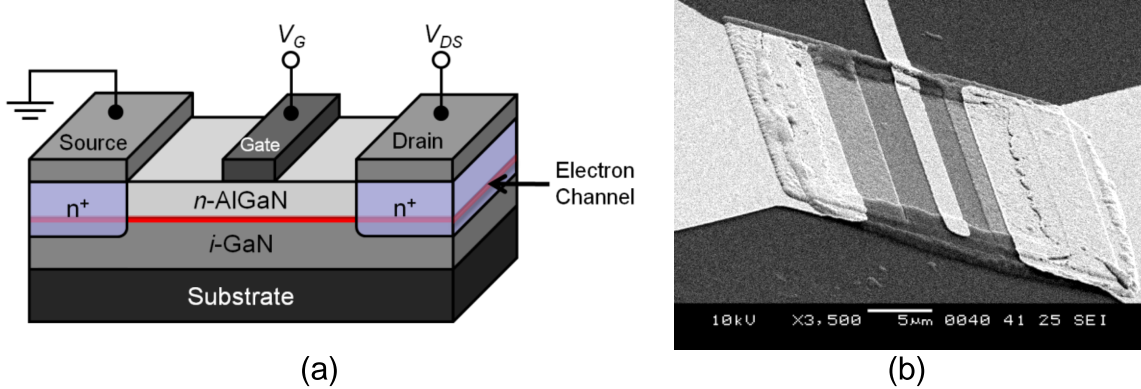


Figure 5.4 (a) Typical structure of a HFET, using the basic AlGaN/GaN system. (b) SEM diagraph of a fabricated HFET device of c-AlGaN/GaN.

ion etching (RIE) in order to separate single devices. A 250 nm thick SiO_2 layer was deposited on the sample surface and etched down over the mesa structures using Ar and CHF_3 to open the device surface. Gate fingers were fabricated by evaporating Pd/Ni/Au (15 nm/15 nm/50 nm) and subsequent annealing at 400 °C for 10 min in nitrogen atmosphere. Finally, contact pads of Ni/Au (15 nm/50 nm) were thermally evaporated.

To demonstrate the function of a HFET a Poisson-Schrödinger model [30] was used for the calculation of the band structure of a cubic AlGaN/GaN hetero-structure at three different gate voltages of V_G=-0.2 V, V_G=0 V and V_G=0.5 V shown in Figure 5.5 (a), (b) and (c), respectively. The calculation was performed for a typical c-AlGaN/GaN hetero-structure with 600 nm c-GaN buffer layer with n(c-GaN)=5×10^{16} cm^{-3} and 30 nm c-$Al_{0.36}Ga_{0.64}N$ with n(c-AlGaN)=5×10^{17} cm^{-3}. For the gate contact a Schottky barrier of 0.8 eV was assumed [56]. The sheet carrier concentration was calculated by formula

$$n_{sheet} = (n_{3D})^{\frac{2}{3}}. \quad (5.1)$$

At V_G=-0.2 V the maximum electron sheet concentration at the c-AlGaN/GaN interface is n_{sheet}=2.1×10^{11} cm^{-2} and the electron channel is depleted. At V_G=0 V an electron channel with n_{sheet}=6.2×10^{11} cm^{-2} is formed. However, the Fermi level is below the conduction band edge so that this device is of normally-off characteristics. At V_G=0.5 V the Fermi level is above the conduction band edge within the electron channel. The carriers inside the channel are degenerated, the carrier sheet concentration in the channel obtains n_{sheet}=2.0×10^{12} cm^{-2} and the channel is conductive. These calculations with typical parameters of UID c-AlGaN and UID c-GaN show the capability of a cubic AlGaN/GaN system for fabrication of normally-off HFETs. In the following chapters HFETs fabricated of c-AlGaN/GaN with different output characteristics will be introduced.

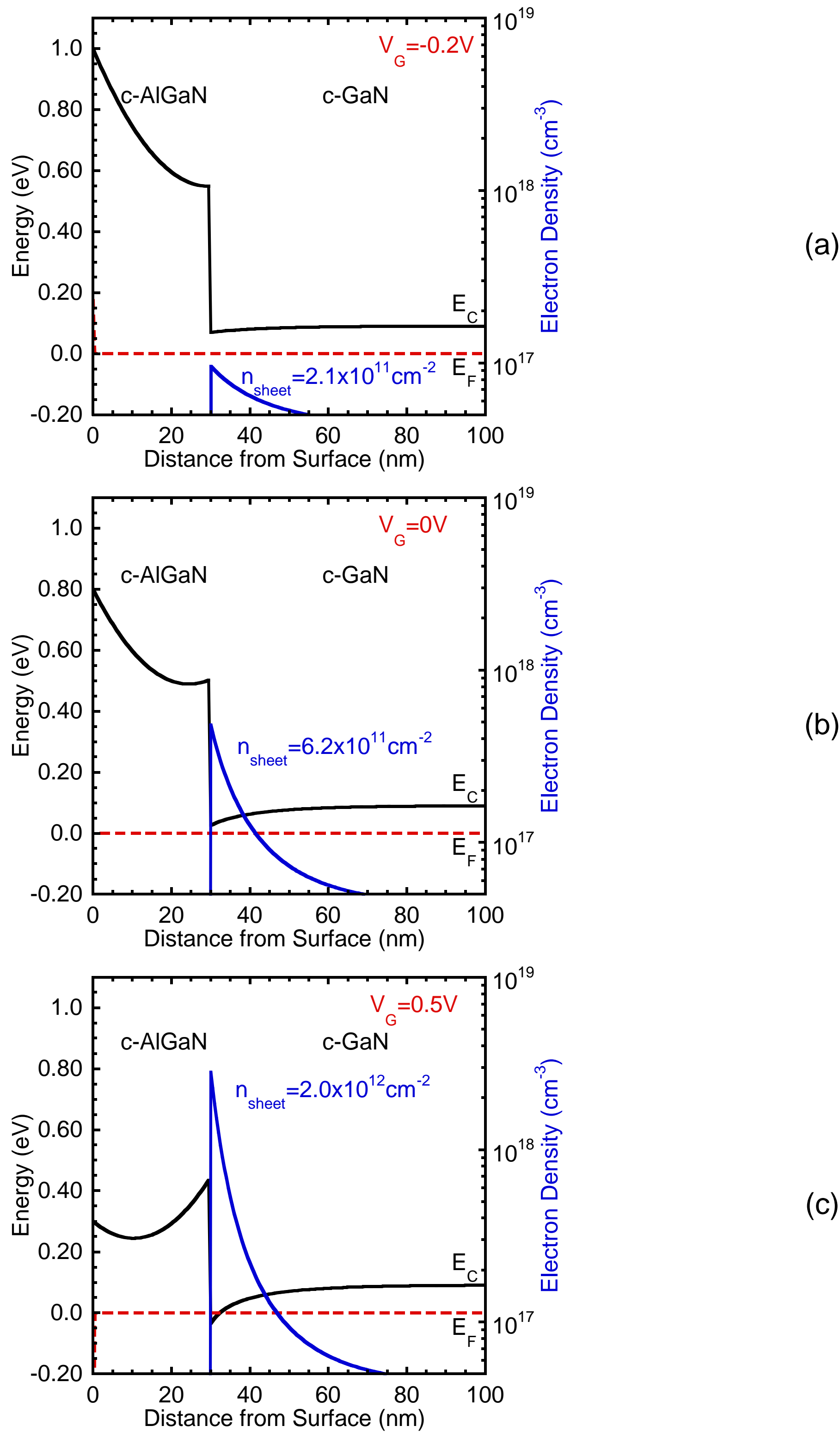


Figure 5.5 Calculated conduction band edge and electron concentration of c-$Al_{0.36}Ga_{0.64}N$/GaN vs. distance from surface at (a) V_G=-0.2 V, (b) V_G=0 V and (c) V_G=0.5 V.

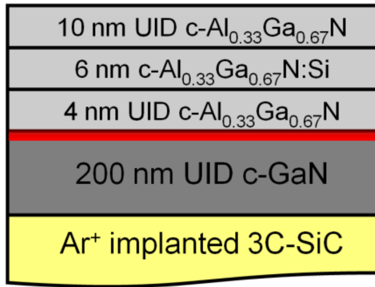


Figure 5.6 Schematic cross-sectional view of a c-AlGaN/GaN hetero-structure grown on Ar^+ implanted 3C-SiC for HFET *A*.

5.2.1 HFET with 200 nm c-GaN Buffer Layer on 3C-SiC (HFET A)

HEFT *A* (sample 1793) consists of 200 nm UID c-GaN on Ar^+ implanted 3C-SiC followed by 4 nm UID c-$Al_{0.33}Ga_{0.67}N$ spacer layer, 6 nm thick c-$Al_{0.33}Ga_{0.67}N$:Si doped with N_D=4×10^{18} cm^{-3} Si and 10 nm UID c-$Al_{0.33}Ga_{0.67}N$. A schematic cross-sectional view of the structure is shown in Figure 5.6. Due to the small c-GaN buffer thickness the RMS roughness of the sample's surface measured by AFM was 3 nm. The dislocation density of c-GaN was about 1×10^{10} cm^{-2} as estimated from the FWHM of the X-ray rocking curve of the (002) c-GaN reflex using a model by Gay et al. [23]. For the source and drain contacts of HEFT *A* 10 nm of the c-AlGaN top layer were removed by RIE with $SiCl_4$. The gate contact was evaporated directly on the c-AlGaN cap layer. The fabrication of the device was carried out according to the description in Chapter 5.2.

Figure 5.7 shows the room temperature DC drain IV curves of HFET *A*. A clear field-effect was measured with this device when the gate voltage was varied from V_G=-1 V to V_G=2 V. The negative source-drain current at V_{DS}=0 V and V_G>1 V is induced by gate

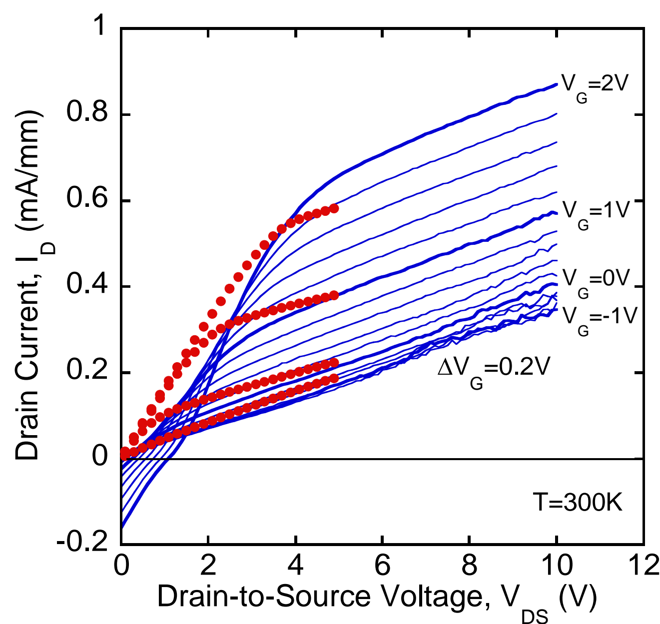


Figure 5.7 Static output characteristics of c-AlGaN/GaN HFET *A*. The red dotted lines represent calculated output characteristics at V_G=-1 V, 0 V, 1 V, and 2 V.

leakage in forward direction as will be explained in Chapter 6.1.1.

A parasitic shunt current was observed with I_{shunt}=0.34 mA/mm at V_{DS}=10 V which is caused by reverse gate leakage described in Chapter 6.1.1 and an insufficient isolation between the device and high conductive 3C-SiC introduced in Chapter 4.1. The source-to-drain current difference between V_G=-1 V and V_G=2 V was 0.5 mA/mm.

For the calculation of the output characteristics of HFET A a 2D device simulator ATLAS [32] was used. It was assumed that the c-GaN donor concentration was N_D=4×10^{16} cm^{-3} with mobility of μ=5 cm^2/Vs at the c-AlGaN/GaN interface and a linear decrease of donor concentration and mobility with increasing distance from the surface. The parameters of the c-$Al_{0.33}Ga_{0.67}N$ were 4 nm spacer layer with a doping concentration of N_D=4×10^{17} cm^{-3}, followed by a 6 nm c-$Al_{0.33}Ga_{0.67}N$ layer with N_D=4×10^{18} cm^{-3} and a 10 nm c-$Al_{0.33}Ga_{0.67}N$ cap layer with N_D=4×10^{17} cm^{-3}. For the Ar^+ implanted 3C-SiC substrate it was assumed that the insulating damage layer keeps the same carrier density as the bulk 3C-SiC of n=2×10^{18} cm^{-3} and the insulation effect is caused by low carrier mobility. Therefore three 3C-SiC layers with different mobilities were assumed in the simulation. The first 3C-SiC layer was 5 nm thick with μ=0.05 cm^2/Vs at the c-GaN/3C-SiC interface, followed by 95 nm 3C-SiC with μ=5×10^{-5} cm^2/Vs (ion damage region) and 40 µm bulk 3C-SiC with μ=500 cm^2/Vs. For the simulation the ohmic source and drain contacts with a contact resistivity of ρ_C=150 Ω·cm (measured by TLM) were assumed on the c-GaN layer contacting the electron channel directly. The Schottky gate contact with barrier height of 0.8 eV was localized on top of the c-$Al_{0.33}Ga_{0.67}N$ layer. Like in the realized HFET devices the gate length was 2 µm and the gate-to-source and gate-to-drain space was 3 µm. The red dotted lines in Figure 5.7 represent the calculated drain current I_D of HFET A at V_G=-1 V, 0 V, 1 V, and 2 V, respectively. The calculated data are in good agreement with the measured values.

The measured and calculated transfer characteristics of HFET A are shown in Figure 5.8. The threshold voltage of the device was V_{th}=0.6 V measured by extrapolation of the drain current I_{DS}-V_G curve at V_{DS}=10 V revealing that this device is of the normally-off type.

The electron concentration at the c-AlGaN/GaN interface was obtained from CV measurements which were performed on the gate contact of the device at 1 MHz. For this purpose, the gate contact was biased and the source and drain were connected in parallel and grounded. Figure 5.9 (a) shows measured (blue dots) and calculated (red dashed line) CV characteristics of HFET A confirming the presence of an electron channel at the c-AlGaN/GaN interface. The measured capacity has been corrected for the parasitic parallel capacity of the SiO_2 layer under the contact pads (C_p=20.6 pF). The resulting gate capacity is plotted at the right-hand scale. For the calculation a donor concentration of N_{Ga}=4×10^{16} cm^{-3} in c-GaN was assumed. The parameters of the c-$Al_{0.33}Ga_{0.67}N$ were 4 nm spacer layer with doping concentration of N_{AlGaN}=4×10^{17} cm^{-3}, followed by a 6 nm c-$Al_{0.33}Ga_{0.67}N$ layer with N_{AlGaN}=4×10^{18} cm^{-3} and a 10 nm c-$Al_{0.33}Ga_{0.67}N$ cap layer with N_{AlGaN}=4×10^{17} cm^{-3}. The CV curve increases at V>-1 V and depletes at positive voltage around 0.3 V. This is a typical CV behaviour of a normally-off HFET.

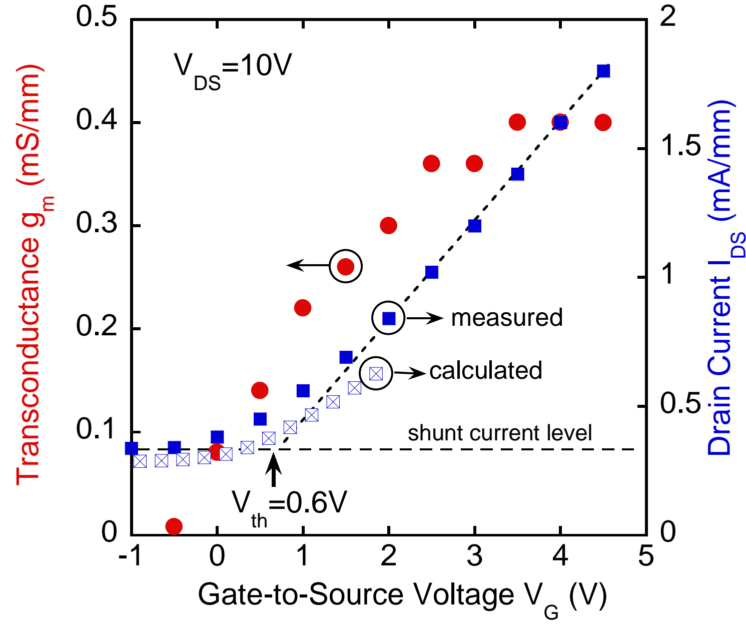


Figure 5.8 Measured (solid squares) and simulated (open squares) transfer characteristics of HFET *A* at drain-to-source voltage of V_{DS}=10 V. Also shown is the measured transconductance as function of the gate voltage (red solid circles).

The CV data were used to calculate the apparent carrier density N_{CV} in the sample using the following equations [57]:

$$N_{CV} = -\frac{C^3}{q\varepsilon_s A^2}\frac{dV}{dC} \tag{5.2}$$

$$W_D = \frac{\varepsilon_s A}{C} \tag{5.3}$$

where W_D is equal to the distance from the surface and A is the contact area. The derivation of the Equations (5.2) and (5.3) is shown in Appendix G. The calculated N_{CV} profiles of the simulated (red dashed line) and measured (blue dots) CV data are depicted in Figure 5.9 (b). An electron accumulation was observed in the c-GaN layer near the c-AlGaN/GaN hetero interface with a maximum sheet carrier concentration of n_{sheet}=3.4×10^{12} cm^{-2} at the c-AlGaN/GaN interface.

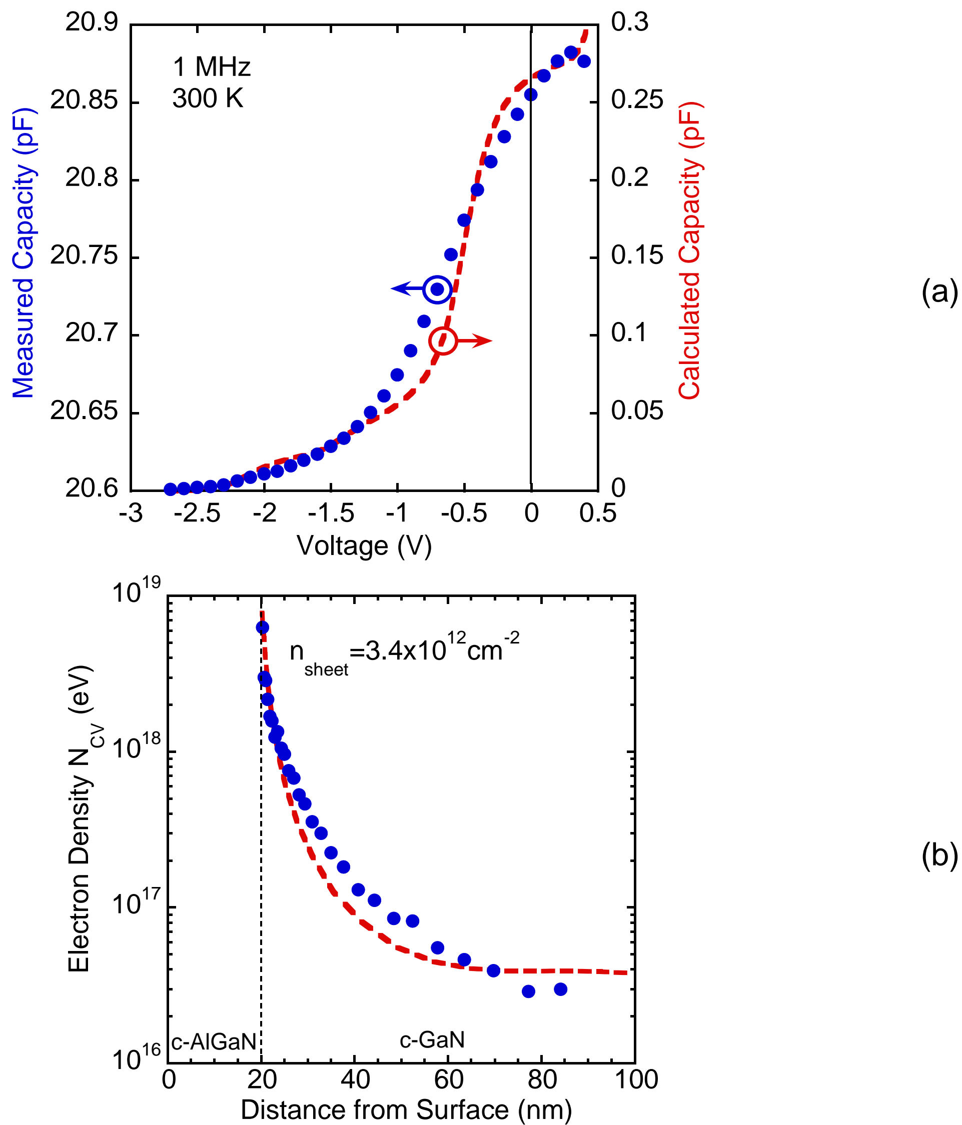


Figure 5.9 (a) Measured (blue dots) and calculated (red dashed line) CV characteristics of HFET *A*. (b) Calculated (red dashed line) and measured (blue dots) electron concentration N_{CV} vs. distance from surface.

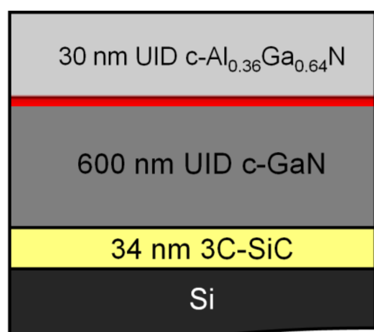


Figure 5.10 Schematic cross-sectional view of a c-AlGaN/GaN hetero-structure on 3C-SiC/Si substrate (HFET *B*).

5.2.2 HFET on 3C-SiC/Si (001) Substrate (HFET B)

A HFET of c-$Al_{0.36}Ga_{0.64}N$/GaN on carbonized Si substrate [36] will be introduced. Figure 5.10 shows a schematic cross-sectional view of the hetero-structure (sample 1747) consisting of 600 nm UID c-GaN on carbonized silicon with a 34 nm thick 3C-SiC layer followed by 30 nm UID c-AlGaN with Al mole fraction of 36 %. The HFET device fabrication was performed as described in Chapter 5.2. We denote the devices of this type HFET *B*.

Figure 5.11 (a) shows room temperature DC drain current-voltage (IV) curves of HFET *B* measured at gate-to-source voltages from V_G=0 V (red line) to V_G=1 V. The drain-to-source current at V_G=0 V (shunt current) is relatively large due to the reverse gate leakage and the high conductivity of the c-GaN buffer layer and potentially of the Si substrate. Apart from the shunt current a clear field effect was measured in HFET *B*. The drain-to-source current amplifier of ΔI_{DS}=28 μA/mm was measured at V_G=1 V and

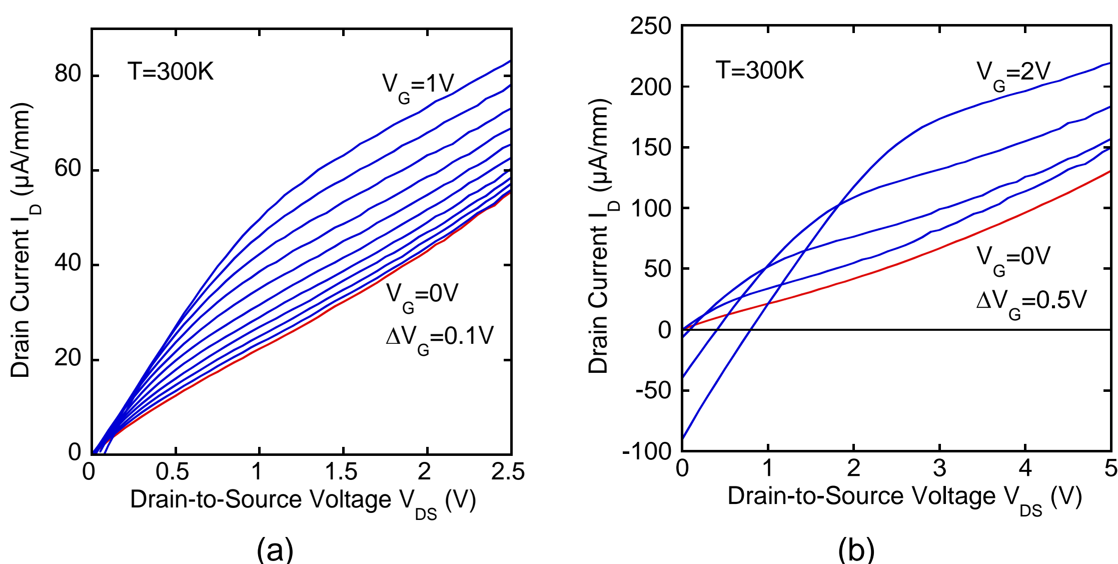


Figure 5.11 Static output characteristics of HFET *B* on 3C-SiC/Si substrate (a) at gate voltages from V_G=0 V (red line) to V_G=1 V and (b) at gate voltages from V_G=0 V (red line) to V_G=2 V.

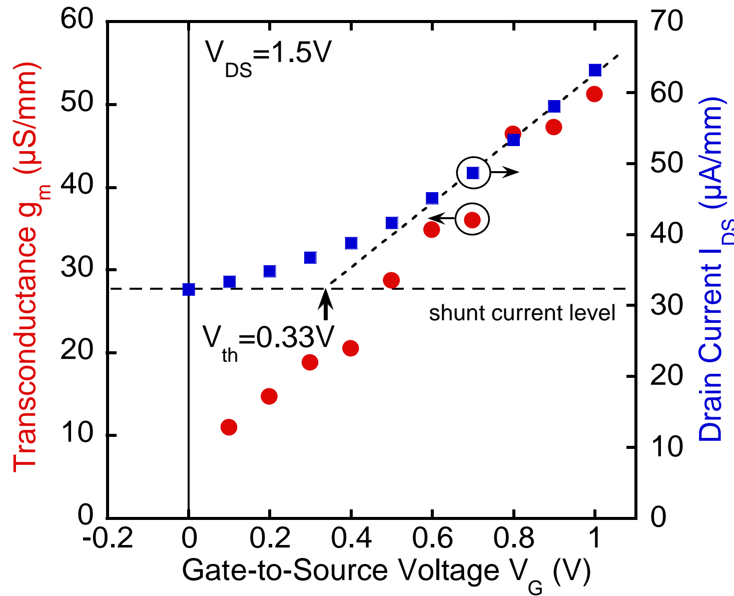


Figure 5.12 Transfer characteristics of the c-AlGaN/GaN HFET *B* at drain-to-source voltage of V_{DS}=1.5 V.

V_{DS}=2.5 V. The low drain current I_{DS} of this sample is probably caused by the relatively high resistivity of the source and drain contacts deposited directly on the c-AlGaN cap layer.

The output characteristics of the same device at gate voltages of V_G=0 V..2 V are shown in Figure 5.11 (b). The drain-to-source current amplifier in this measurement was ΔI_{DS}=90 µA/mm measured at V_G=2 V and V_{DS}=5 V. This value is three times higher than the measurement at V_G=1 V and V_{DS}=2.5 V. However, negative source-to-drain current appears at V_{DS}=0 V and V_G>1 V induced by forward gate leakage causing loss of power. At V_G=2 V and V_{DS}=0 V the gate leakage of 93 µA/mm was measured. This value is comparable with the gate-to source current in forward direction.

The transfer characteristics of HFET *B* are shown in Figure 5.12. The shunt current level is designated at I_{DS}=32.5 µA/mm. The threshold voltage of the device is V_{th}=0.33 V measured by extrapolation of the drain current I_{DS}-V_G curve at V_{DS}=1.5 V and its intersection with the shunt level. Therefore this device is of normally-off type.

5.2.3 Comparison of HFET with Normally-off (HFET C) and Normally-on Characteristics (HFET D) on Ar^+ Implanted 3C-SiC (001)

In this chapter, HFETs of non-polar cubic AlGaN/GaN hetero-structures with normally-off (HFET *C*, sample 1809) and normally-on (HFET *D*, sample 1855) operation are demonstrated and compared. Figure 5.13 shows a schematic cross-sectional view of HFET *C* and HFET *D*. Both samples were grown on Ar^+ implanted 3C-SiC.

HFET *C* consists of 600 nm UID c-GaN followed by 3 nm UID c-$Al_{0.25}Ga_{0.75}N$ spacer layer, 2 nm c-$Al_{0.25}Ga_{0.75}N$:Si and 15 nm UID c-$Al_{0.25}Ga_{0.75}N$. The carrier concentration of the Si doped c-AlGaN layer was n=4.5×10^{18} cm^{-3}. A 5 nm thick heavily silicon doped cubic c-GaN:Si cap layer with a carrier concentration on n=6×10^{19} cm^{-3} was grown on top of the sample. For HFET devices source and drain contacts were evaporated directly on the c-GaN:Si cap layer. For the gate contact the c-GaN:Si cap layer was removed using RIE with $SiCl_4$ followed by thermal annealing at 600 °C in air. The fabrication of the devices was carried out according to the description in Chapter 5.2.

HFET *D* consists of a 60 nm UID c-GaN nucleation layer followed by 580 nm carbon doped c-GaN used to minimize the shunt current through the c-GaN buffer layer. For the carbon doping a CBr_4 beam equivalent pressure of *BEP*=1×10^{-6} mbar was used. A 34 nm thick homogeneously silicon doped c-$Al_{0.36}Ga_{0.64}N$:Si cap layer with carrier concentration of n=1.5×10^{18} cm^{-3} was grown on top of the sample. For the source and drain contacts of HEFT *D* 10 nm of the c-AlGaN top layer were removed by RIE with $SiCl_4$. The gate contact was evaporated directly on the c-AlGaN cap layer after previous thermal annealing at 600 °C in air. The fabrication of the devices was carried out according to the description in Chapter 5.2.

The room temperature DC drain current voltage curves from V_G=-1 V to V_G=5 V of HFET *C* are displayed in Figure 5.14 (a). The threshold voltage of this device is V_{th}=1.2 V measured at V_{DS}=10 V by extrapolation of the drain current I_{DS}-V_G curve at V_{DS}=10 V shown in Figure 5.15 (a). This indicates normally-off device characteristics, however, the drain-to-source current at V_G=0 V is relatively large due to the gate and buffer leakage

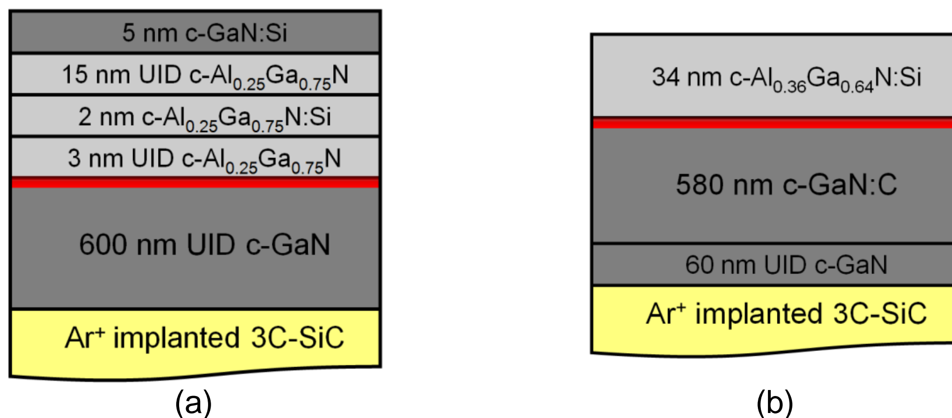


Figure 5.13 Schematic cross-sectional view of c-AlGaN/GaN hetero-structures grown on Ar^+ implanted 3C-SiC for (a) HFET *C* and (b) HFET *D*.

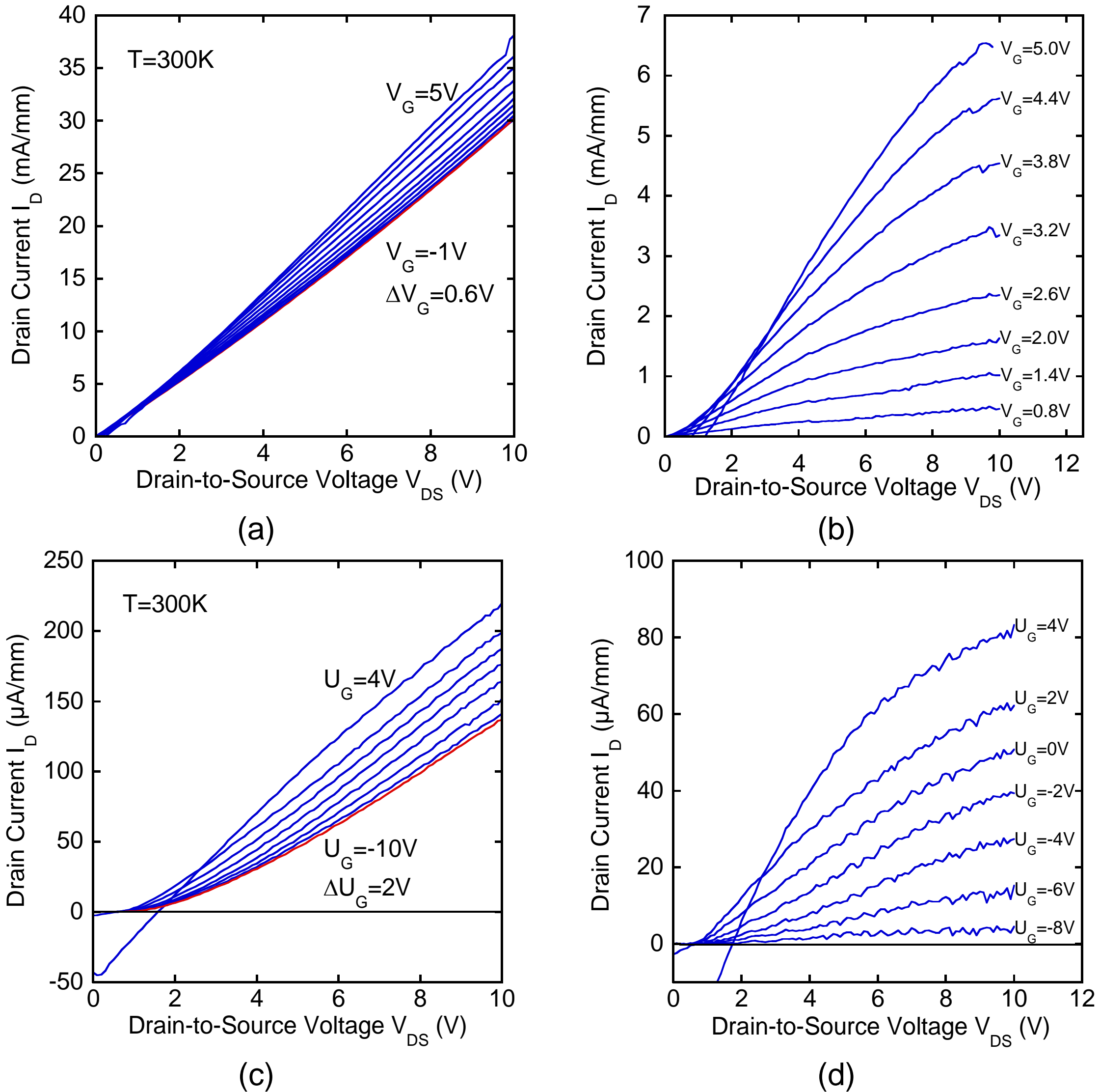


Figure 5.14 (a) Static output characteristics of HFET *C*. (b) The same measurement curves corrected for the drain current at V_{GS}=-1 V. (c) Static output characteristics of HFET *D*. (d) The same measurement curves corrected for the drain current at V_{GS}=-10 V.

current. Figure 5.14 (b) shows the measurement data adjusted by the shunt current. A maximum drain-to-source current of I_{DS}=6.5 mA/mm was observed when a gate voltage of V_G=5 V was applied.

The room temperature output characteristics of HFET *D* are depicted in Figure 5.14 (c). The gate voltage was varied between V_G=-10 V and V_G=4 V. Apart from the shunt current (red curve), a clear field effect with normally-on characteristics was measured in this sample. The threshold voltage of this device is V_{th}=-8.6 V measured at V_{DS}=10 V by extrapolation of the drain current curve I_{DS}-V_G curve at V_{DS}=10 V shown in Figure 5.15 (b) indicating normally-on behaviour of the device. Figure 5.14 (d) shows the I_D-V_{DS} curves of HFET *D* adjusted by the shunt current. The measurements of the source and drain contact resistance show a slight non-ohmic behaviour which limited the absolute current through the device. Therefore, the source-to-drain current difference between V_G=-10 V and

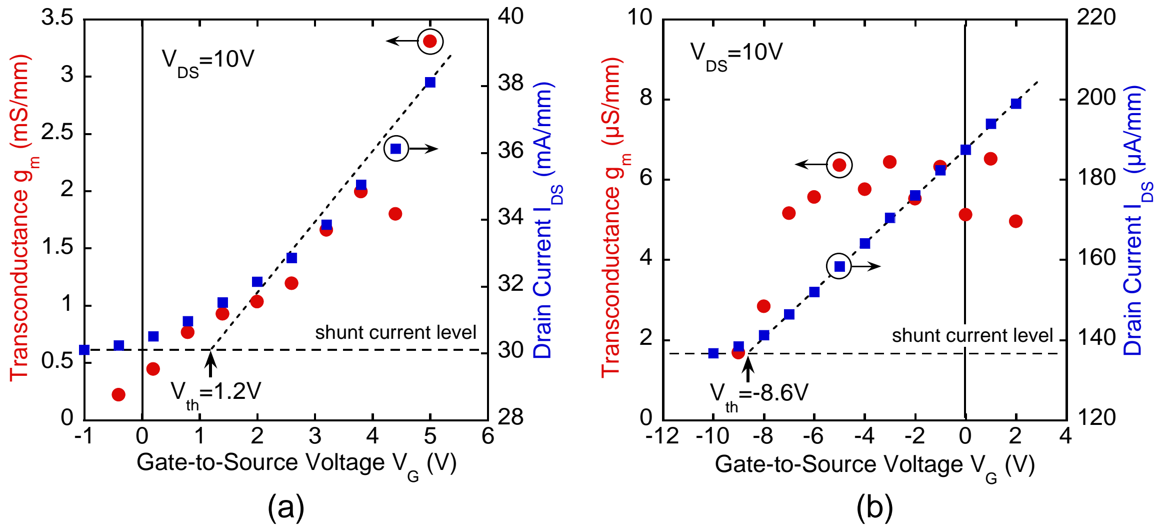


Figure 5.15 Transfer characteristics of the c-AlGaN/GaN (a) HFET *C* and (b) HFET D at drain-to-source voltage of V_{DS}=10 V.

V_G=4 V was only 80 µA/mm. At high positive gate voltages, an additional gate leakage was observed at low source-to-drain voltages. So, the drain current at V_G=4 V is reduced by the gate leakage.

The transconductance g_m of HFET C and HFET *D* is depicted in Figure 5.15 (a) and (b), respectively. A much larger transconductance was measured in HFET *C* than in HFET *D*. This can be explained by lower source and drain contact resistance of HFET *C* due to high silicon doping of the GaN:Si cap layer with n=6×10^{19} cm^{-3}. In HFET *D*, the same metal contacts were evaporated on $Al_{0.36}Ga_{0.64}N$:Si with only n=1.5×10^{18} cm^{-3}. As a result, the source-to-drain current and therewith the transconductance g_m of HFET *D* is limited by the contact resistance. More investigations of contact resistivity are introduced in Chapter 6.2.

To clarify the normally-off behaviour of HFET *C* and the normally-on behaviour of HFET *D*, band structures and electron density profiles were calculated for V_G=0 V using a Poisson-Schrödinger model. For the calculation a donor concentration of N_{AlGaN}=1.5×10^{18} cm^{-3} in UID c-$Al_{0.36}Ga_{0.64}N$ and N_{GaN}=1×10^{17} cm^{-3} in UID c-GaN was used. The simulation diagrams of both samples are shown in Figure 5.16. According to electrical measurements, the electron channel of HFET *C* is nearly depleted and the sheet carrier density of the electron channel is n_{sheet}=2.6×10^{11} cm^{-2}. To achieve a higher electron density at the c-AlGaN/GaN interface, a positive gate voltage has to be applied. In contrast to HFET *C*, the electron channel is already filled up and conductive in HFET *D* with one order of magnitude higher sheet carrier concentration of n_{sheet}=3.7×10^{12} cm^{-2}. A negative gate voltage has to be applied to deplete the channel.

CV measurements were performed on HFET *D* at 2 MHz to detect the electron channel at the c-AlGaN/GaN interface. For this purpose, the gate was biased and the source and drain were connected in parallel and grounded. Figure 5.17 (a) shows the measured room temperature CV profile of HFET *C* (blue dots). The typical shape was observed where the capacitance was found to be roughly constant (V=0..-1 V) when the electron channel was

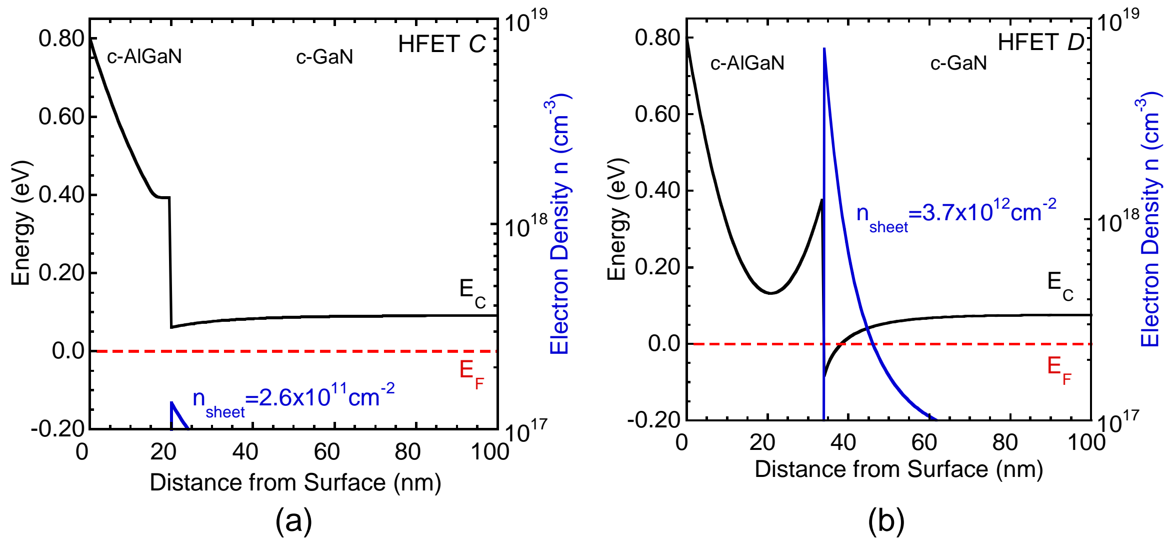


Figure 5.16 Calculated conduction band edge and the electron concentration vs. distance from surface at V_{GS}=0 V for (a) HFET *C* and (b) HFET *D*.

present, falling to smaller values once the electron channel had been depleted. In contrast to HFET A the CV curve HFET D saturates at negative voltage of V=-1V (see Figure 5.9 a). This is a typical CV curve behaviour of normally-on HFET devices. The left-hand scale is the measured capacity which has been corrected for the parasitic parallel capacity of the SiO_2 layer under the contact pads (C_p=19.8 pF). The resulting gate capacity is plotted at the right hand-scale. The red dashed curve depicts calculated CV data using the same Poisson-Schrödinger model as used for the calculations of band diagrams. For the calculation a donor concentration of N_{AlGaN}=1.5×10^{18} cm^{-3} in UID c-$Al_{0.36}Ga_{0.64}N$ and N_{GaN}=1×10^{17} cm^{-3} in UID c-GaN was used.

Figure 5.17 (b) shows the apparent carrier density N_{CV} of HFET *D* calculated from the CV characteristics using Equations 5.2 and 5.3 (blue dots). The resulting profile shows a carrier accumulation at the c-AlGaN/GaN interface building an electron channel. The red dashed curve is the carrier density calculated from the simulated CV data of HFET *D*.

In this chapter it was demonstrated that carbonized Si as well as Ar^+ implanted free standing 3C-SiC is suitable as substrate for cubic AlGaN/GaN HFETs. Additionally, a carbon doped GaN:C buffer layer can be used to reduce buffer leakage. However, the shunt current at V_G=0 V is most likely caused by buffer and reverse gate leakage. Therefore, a further improvement of the device isolation and Schottky gate contact characteristics are necessary.

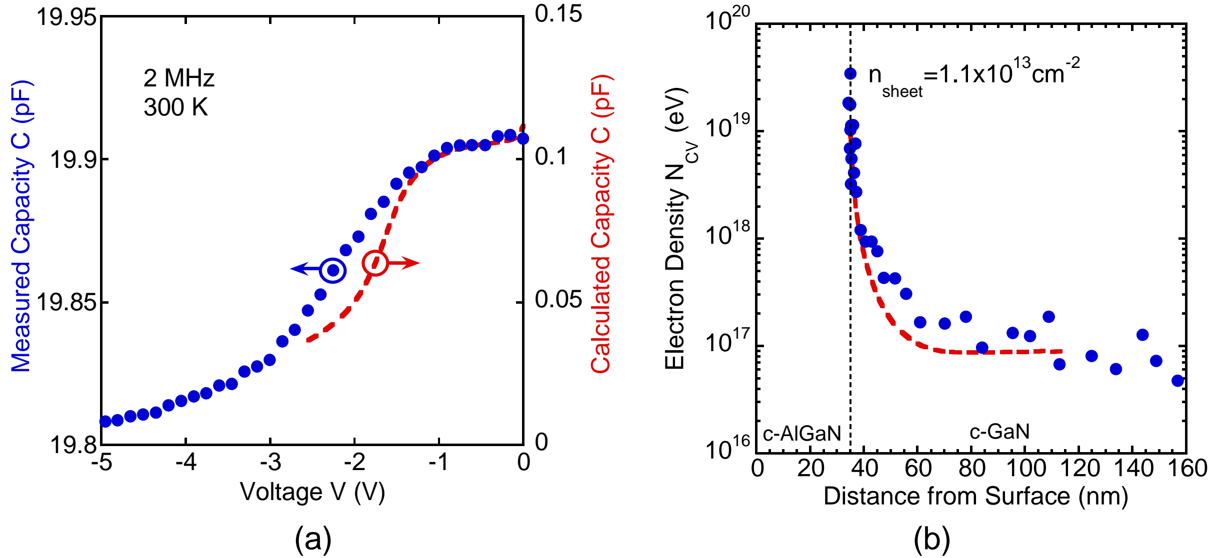


Figure 5.17 (a) Measured (blue dots) and calculated (red dashed line) CV characteristics of HFET *D* confirming the presence of an electron channel at the c-AlGaN/GaN interface. (b) Measured (blue dots) and calculated (red dashed line) carrier density profile N_{CV} of HFET *D*.

5.3 Comparison of Polar, Semi-polar and Non-polar AlGaN/GaN HFETs

In Table 5.1 the experimental data of cubic AlGaN/GaN HFETs are compared with hexagonal polar c-plane HFETs and semi-polar a-plane HFETs. Due to spontaneous and piezoelectric polarization fields state-of-the-art c-plane AlGaN/GaN HFETs are of normally-on characteristics [58]. The maximum source-to-drain current $I_{DS,max}$ of these devices is in the order of some hundred mA/mm. Therefore conventional AlGaN/GaN HFETs are applicable for high-power switching systems. In [59] it was shown that it is possible to fabricate normally-off HFETs of c-plane AlGaN/GaN with a thin InGaN cap layer. The polarization-induced field in the InGaN cap layer is expected to raise the conduction band of the AlGaN/GaN interface, which leads to a threshold voltage shift to the positive direction. However, one way to avoid undesirable polarization fields in HFET devices is the use of semi-polar and non-polar AlGaN/GaN. The first semi-polar HFET of a-plane AlGaN/GaN was published in [6]. Compared to c-plane HFET the transconductance of a-plane devices is a factor 20-30 lower. This is caused by the still inferior material quality of a-plane nitrides and high dislocation density, which reduces the carrier mobility μ and therefore the transconductance g_m. Up to now, the crystalline quality of non-polar cubic AlGaN/GaN is comparable with that of semi-polar a-plane hetero-structures. Therefore, the transconductance g_m of HFET *C* with the lowest source and drain contact resistance compares well with that of the a-plane devices. However, a positive threshold voltage V_{th} of 0.6 V, 0.33 V, and 1.2 V was measured on HFET *A*, *B* and *C*, respectively, whereas for the a-plane devices only “nearly positive” V_{th}=-0.5 V was observed. In addition, cubic HFETs show no dependence on the orientation of the gate as

observed in a-plane HFET ([1-100] and [0001] direction). In this work, both normally-on (HFET *D*) and normally-off (HFET *A*, *B* and *C*) c-AlGaN/GaN HFETs were demonstrated.

Table 5.1 Summary of device performance of polar c-plane, semi-polar a-plane and non-polar cubic AlGaN/GaN HFETs.

	L_G	L_{SG}	L_{DG}	V_{th}	$I_{DS,max}$	$g_{m,max}$
normally-on c-plane HFET [58]	2 µm	2 µm	5 µm	-3.5 V	460 mA/mm at V_G=1 V	125 mS/mm
normally-off c-plane HFET with InGaN cap layer [59]	1.9 µm	1.5 µm	2.4 µm	0.4 V	115 mA/mm at V_G=2 V	85 mS/mm
normally-off a-plane HFET in [1-100] [6]	1 µm	2 µm	2 µm	-0.5 V	19.5 mA/mm at V_G=1.6 V	6.7 mS/mm
normally-off a-plane HFET in [0001] [6]	1 µm	2 µm	2 µm	-0.5 V	13.5 mA/mm at V_G=1.6 V	3.6 mS/mm
normally-off HFET *A*	2 µm	3 µm	3 µm	0.6 V	1.4 mA/mm at V_G=4.5 V	0.4 mS/mm
normally-off HFET *B*	2 µm	3 µm	3 µm	0.33 V	88 µm/mm at V_G=2 V	70 µS/mm
normally-off HFET *C*	**2 µm**	**3 µm**	**3 µm**	**1.2 V**	**8 mA/mm at V_G=5 V**	**3.3 mS/mm**
normally-on HFET *D*	2 µm	3 µm	3 µm	-8.6 V	62 µA/mm at V_G=2 V	6.5 µS/mm

6 Role of Metal-Semiconductor Contacts for HFET Devices

In a hetero-junction field-effect transistor (HFET), three metal electrode contacts source, gate and drain are realised on the surface of the semiconductor structure. Ideally, source and drain contact the electron channel at the AlGaN/GaN interface directly and they should not reduce the conductivity of the device. Therefore, source and drain have to be of low-resistance ohmic behaviour. The charge density in the electron channel is controlled by the gate bias. So, the gate is a Schottky barrier and it must not be conductive in a wide voltage range to suppress the power loss in high power switching systems. Properties of the two different types of metal-semiconductor contacts on c-AlGaN and c-GaN will be introduced in this chapter.

6.1 Schottky Barrier Gate

When metal makes contact with a semiconductor, a barrier is formed at the metal-semiconductor interface. Figure 6.1 shows the electronic energy relations of a high work-function metal and an n-type semiconductor which are in contact. The theory of metal-semiconductor contacts is given in [33] in detail. The important parameters of metal-semiconductor contacts are the barrier height $q\phi_{Bn0}$ and the built-in potential ψ_{bi}. Because the electron affinity of semiconductor χ_s is higher than the metal work function ϕ_m (the usual case for a metal-semiconductor contact) the average total energy of electrons in the semiconductor is greater than in the metal, resulting in a transfer of electrons to the surface of the metal. The barrier height is simply the difference between the metal work function $q\phi_m$ and the electron affinity $q\chi_s$ of the semiconductor. The charge on the metal side resides on an infinitesimally thin layer, while the width of the positively charged transition region in the semiconductor is a function of the doping density. The barrier from semiconductor to metal varies with bias giving rise to the Schottky barrier IV characteristics. When the metal is positively biased with respect to the semiconductor, ψ_{bi} is lowered by the forward bias and the probability of an electron overcoming the barrier and moving to the metal is increased. If the applied forward bias $V \geq \psi_{bi}$, no barrier exists for the electrons and the forward current increases steeply. Under reverse bias, ψ_{bi} increases by V and, ideally, no electron moving into the metal occurs.

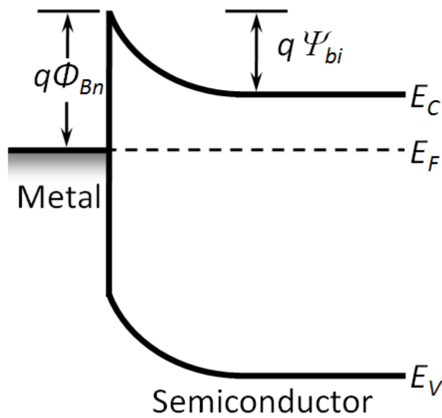


Figure 6.1 Energy-band diagram of metal-semiconductor contacts.

6.1.1 IV Characteristics of Schottky Contacts on c-GaN, c-AlGaN, and c-AlN

In [56] different metal contacts on cubic GaN were investigated and it was shown that Pd is the most suitable metal for fabrication of Schottky contacts on c-GaN with a barrier height of ϕ_{Bn}=0.8 V. For this reason, properties of Pd/Ni/Au (15 nm/15 nm/50 nm) on 600 nm bulk c-GaN (sample 1687), on c-$Al_{0.25}Ga_{0.75}N$/GaN (120 nm/200 nm) (sample 1824) and on c-AlN/$Al_{0.37}Ga_{0.63}N$/GaN (10 nm/30 nm/600 nm) (sample 1867) were studied by measuring the IV characteristics. The contact diameter was 300 µm. The evaporated contacts were thermally annealed at 200 °C for 10 min for mechanical stabilization. All samples were grown on highly conductive free standing 3C-SiC. The reverse side of the 3C-SiC substrates were contacted using In. Figure 6.2 shows a schematic cross-sectional view of the samples for which IV measurements on the upper Schottky contacts were performed.

IV curves measured on Pd/Ni/Au on c-GaN (Pd/c-GaN), c-$Al_{0.25}Ga_{0.75}N$ (Pd/c-AlGaN) and on c-AlN/$Al_{0.37}Ga_{0.63}N$ (Pd/c-AlN) are plotted in a semi-logarithmic scale in Figure 6.3. The IV curve of Pd/c-GaN shows the typical nonlinear behaviour of a Schottky contact on c-GaN. The current density in forward direction is I=140 A/cm^2 at V=3 V whereas in reverse direction a current density of I=-6 A/cm^2 at V=-5 V was observed. The forward current density of Pd/c-AlGaN is with I=14 A/cm^2 at V=3 V one order of magnitude lower

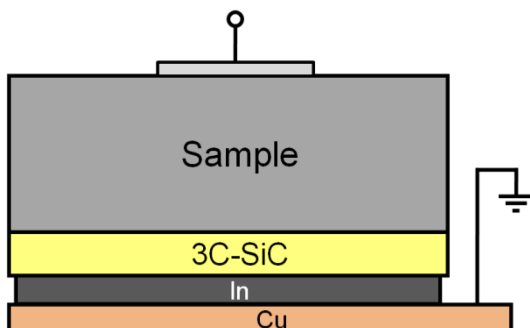


Figure 6.2 Schematic cross-sectional view of samples for IV measurements on Schottky contacts.

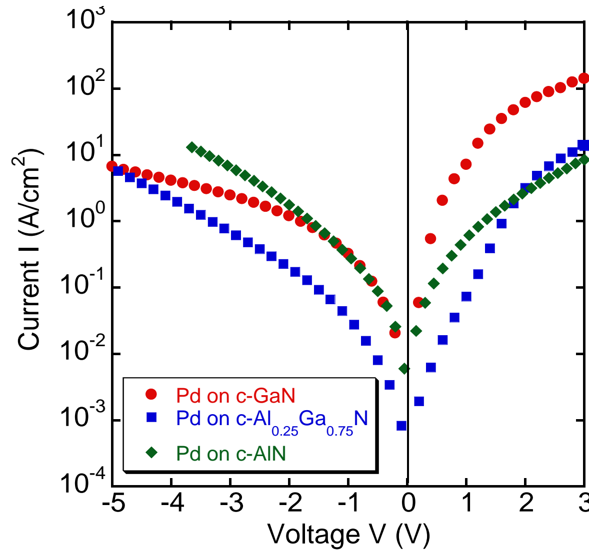


Figure 6.3 Room temperature IV curves of Pd/Ni/Au (15 nm/15 nm/50 nm) contacts on c-GaN (red dots), c-$Al_{0.25}Ga_{0.75}N$ (blue squares) and c-AlN/AlGaN (green diamonds) surfaces in a semi-logarithmic scale.

than the value of Pd/c-GaN. However, the reverse current density at V=-5 V is the same. The curve behaviour of Pd/c-AlN is symmetric with I=8 A/cm^2 at V=3 V and I=-7 A/cm^2 at V=3 V. These measurements show that the reverse current increases with higher Al mole fraction.

To explain the relatively high reverse conductivity of Pd contact on a c-AlN surface, energy-band diagrams were calculated using the Schrödinger-Poisson solver. For the calculation, electron affinities of $q\chi_{GaN}$=4.31 eV [20] and $q\chi_{AlN}$=0.6 eV [60] (values of hexagonal AlN) were assumed for c-GaN and c-AlN, respectively. Work function of $q\phi_{Pd}$=5.12 eV [61] was used to calculate the barrier height between Pd contact and the semiconductors. So, the estimated Pd Schottky barrier height is 0.81 eV for c-GaN and 4.52 eV for c-AlN. The same doping density of N_D=1×10^{17} cm^{-3} was assumed for both layers c-GaN and c-AlN. The calculated energy-band diagrams of Pd on c-GaN and c-AlN in thermal equilibrium are shown in Figure 6.4. A noticeable difference between the two systems is that the Fermi level E_F is close to the conduction band edge in c-GaN and it is close to the valence band edge in c-AlN at the Pd/c-AlN interface involving hole accumulation in c-AlN under the Pd contact as shown in Figure 6.5. If we apply a negative reverse bias on the Pd contact, electrons from the metal recombine with the holes in c-AlN. There is no barrier for holes in the valence band, so new holes can move up causing diffusion current.

If we apply a positive forward bias on the Pd contact, we would expect no current up to a voltage of about V>V_{bi}=4.5 V. However, the forward bias increases already at V>1.5 V as shown in Figure 6.6 (a), but it is one order of magnitude lower than the forward current through the c-GaN and can be explained with electron tunnelling through the Schottky barrier.

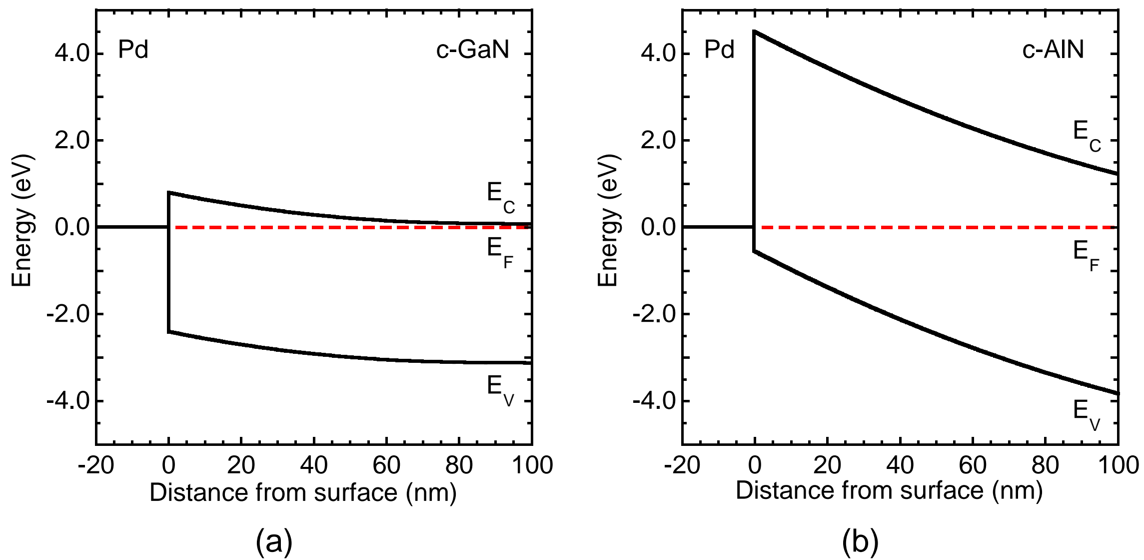


Figure 6.4 Calculated energy-band diagrams of Pd on (a) c-GaN and (b) c-AlN in thermal equilibrium.

Thus, Pd which forms a Schottky contact on c-GaN surface shows no Schottky behaviour on c-AlGaN and c-AlN and is hardly suitable for gate contacts of c-AlGaN/GaN HFETs. Therefore electrical properties of different contacts on the c-AlN sample were investigated by IV measurements to find an applicable metal for Schottky gate of c-AlGaN/GaN HFETs. Figure 6.6 shows IV curves of Pd/Ni/Au (15 nm/15 nm/50 nm) (Pd), In/Ni/Au (15 nm/15 nm/50 nm) (Ni), Ti/Al/Ti/Au (15 nm/50 nm/15 nm/50 nm) (Ti), Cu/Ni/Au (15 nm/15 nm/50 nm) (Cu) and Ni/Au (20 nm/50 nm) (Ni) on c-AlN/$Al_{0.37}Ga_{0.63}N$ (c-AlN) in a (a) linear and (b) semi-logarithmic scale. All measured IV

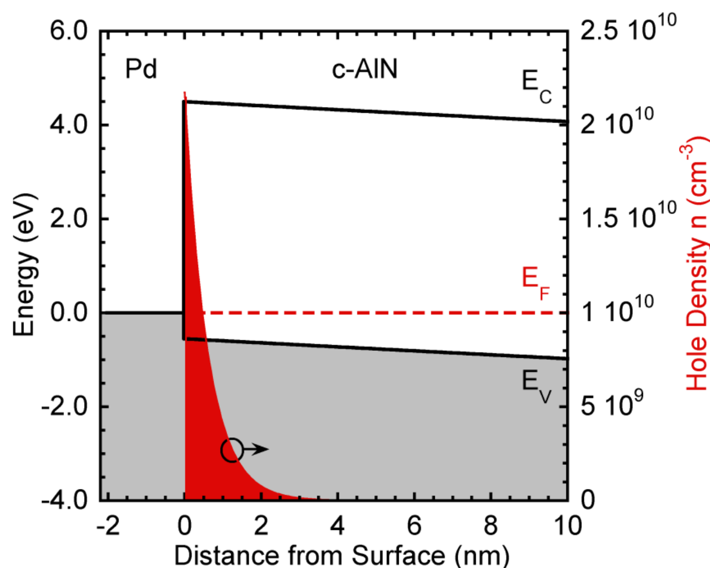


Figure 6.5 Calculated energy-band diagram of Pd on c-AlN and hole density in c-AlN.

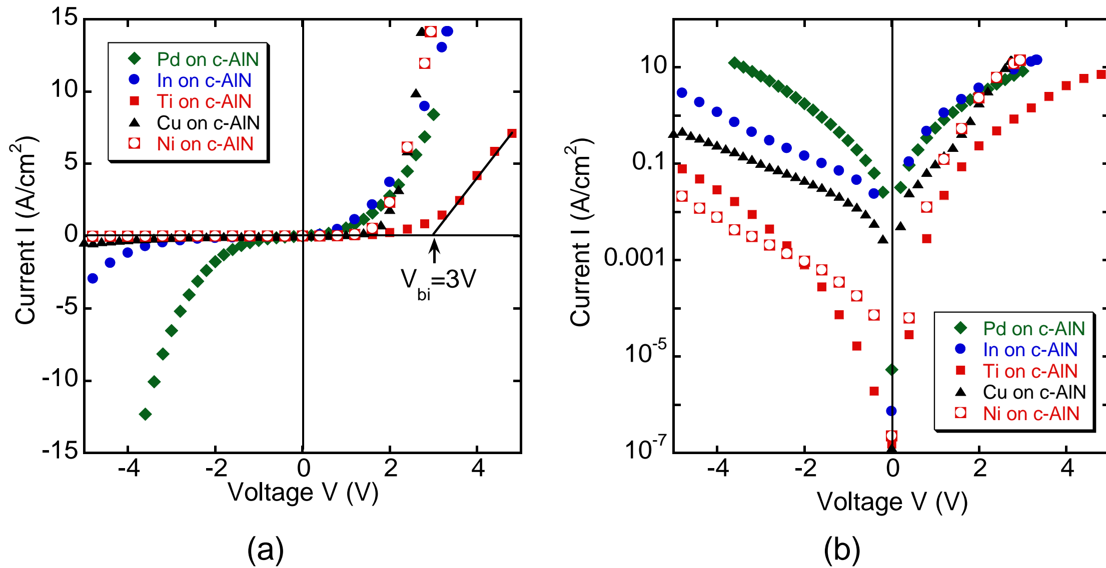


Figure 6.6 Room temperature IV curves with different contacts on a c-AlN/AlGaN surface in (a) linear and (b) semi-logarithmic scale.

curves exhibit nonlinear behaviour. The Schottky barrier height of all contacts was measured by extrapolation of the linear part of the IV curves in forward direction as indicated for the IV curve of the Ti contact in Figure 6.6 (a) and summarised in Table 6.1. Additionally, work functions of Pd, In, Ti, Cu, Ni and calculated barrier heights between the metals and AlN are shown in Table 6.1. It is noticeable that all measured barrier heights are smaller than their calculated values, which can be explained by electron tunnelling through the barrier. In forward direction, Ti is not conductive up to $V \approx 3$ V. Therefore, gate contacts of Ti on c-AlN/AlGaN/GaN HFETs would allow higher gate biases than used in devices described in Chapter 5. In reverse direction, the lowest current was observed with Ni and Ti contacts. The highest forward-to-reverse current ratio of 650 (I(3 V)/I(-5 V)) was measured on the Ni contact. Thus, Ti and Ni are the most suitable metals for Schottky gate contacts of c-AlGaN/GaN HFETs with a thin c-AlN cap layer.

Table 6.1 Measured and calculated barrier height of metals on c-AlN surface.

	Pd	**In**	**Ti**	**Cu**	**Ni**
$q\phi_m$ [61]	5.12 eV	4.12 eV	4.33 eV	4.65 eV	5.15 eV
calculated $q\phi_{Bn} = q(\phi_m - \chi_s)$	4.52 eV	3.52 eV	3.74 eV	4.05 eV	4.55 eV
measured barrier height $q\phi_{Bn} \approx qV_{bi}$	1.8 eV	1.7 eV	3.0 eV	2.1 eV	2.0 eV

6.1.2 Gate Leakage

The gate leakage current can interfere with output characteristics of HFET devices. Figure 6.7 (a) shows the output characteristics of HFET A introduced in Chapter 5.2.1. Two anomalies of the measurement curves are noticeable. The first one is the negative drain current at V_{DS}=0 V and V_G>1 V. This current - which causes loss of power - is induced by forward gate leakage explainable by IV characteristics of the gate contact shown in Figure 6.7 (b). If we apply a positive gate voltage the gate contact is biased in forward direction and at $V_G>V_{bi}$ the gate contact becomes conductive. At V_G=2 V a gate current of I_G=0.20 mA/mm was measured in this device which is comparable with the drain current of I_D=0.16 A at V_D=0 V and V_G=2 V.

The second difference to conventional FET output characteristics is the relatively high background drain current. Similar shunt conductance which was practically independent on the gate bias was observed in hexagonal c-plane AlGaN/GaN on sapphire substrate at temperatures above 200 °C [62]. In this case the shunt current was explained by the thermal activation of deep traps in the n-type GaN buffer layer. In our c-AlGaN/GaN HFETs the background current is probably caused by two different processes namely by the shunt current through the insufficiently insulating substrate and/or c-GaN buffer layer as described in Chapter 4.1 and by the gate leakage in reverse direction. If V_D>0 V is applied at V_G=0 V the gate contact is biased in reverse direction. Due to the high reverse conductance of the Schottky gate contact as demonstrated in Figure 6.7 (b), a reverse current flows from source to gate. Figure 6.8 shows the current measured on gate contact I_G vs. drain-to-source voltage V_{DS} at V_G=-1 V, 0 V, 1 V and 2 V. At V_G=0 and V_{DS}=10 V a gate current of I_G=-0.22 mA/mm was measured whereas the background drain current was I_D=0.4 mA/mm. Therefore, the shunt current of this HFET device can be divided by two

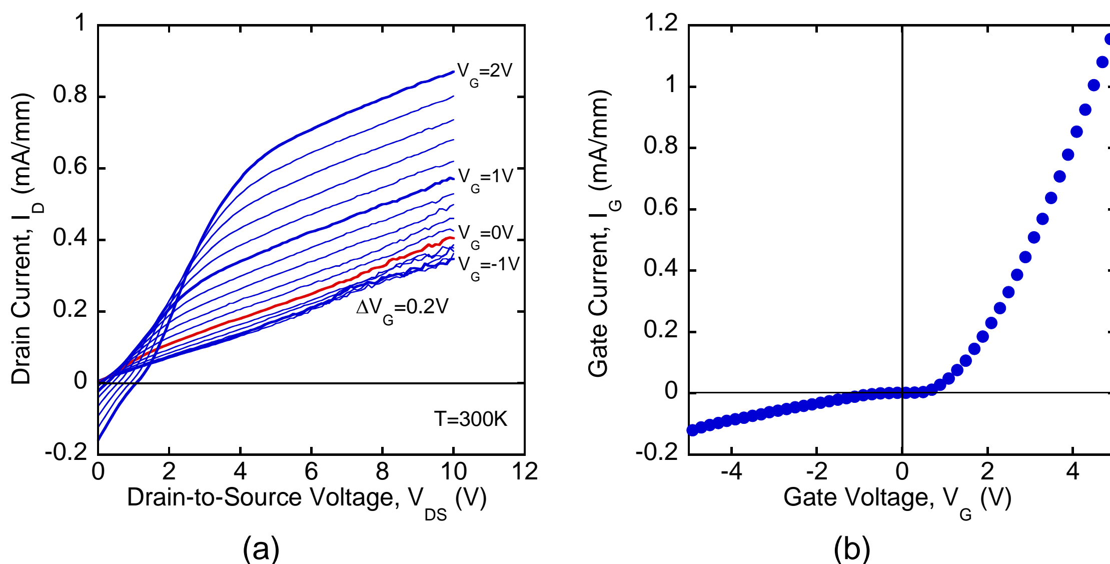


Figure 6.7 (a) Room temperature output characteristics of a c-AlGaN/GaN (HFET A). (b) Gate-to-Source and Drain-to-Source IV characteristics of HFET A.

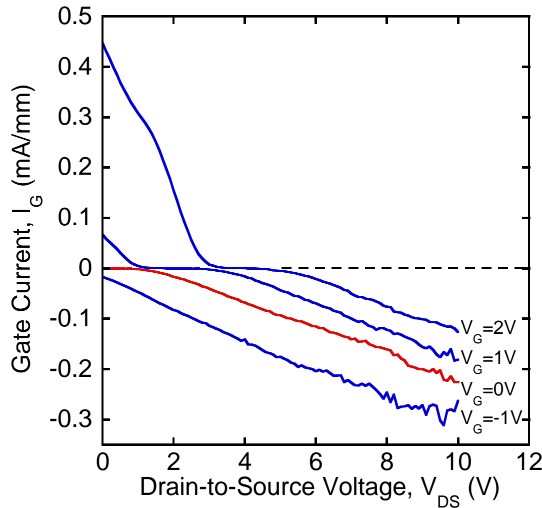


Figure 6.8 Gate current I_G vs. drain-to-source voltage V_{DS} of the c-AlGaN/GaN HFET.

by Schottky gate contacts with improved reverse current characteristics.

It is noticeable that the value of the gate current increases at V_G<0 V while the drain current decreases. At V_G=-1 V and V_{DS}=10 V the gate current is I_G=0.3 mA/mm and the drain current is I_D=0.34 mA/mm. That means that at negative gate voltages the reverse gate current decreases due to the decreased potential difference between drain and gate while the electron channel below the gate contact is more depleted than at V_G=0 V; therefore the drain current is reduced. In contrast, it was observed that in the defect c-AlGaN/GaN HFET devices which were overcharged, the drain current increases with increased negative gate voltage (not shown here).

If the gate leakage in reverse direction contributes to the background drain current direction it could be assumed that the drain current without gate bias should be lower than at V_G=0 V. Figure 6.9 (a) shows the drain-to-source IV characteristics of HFET A without gate voltage as depicted in Figure 6.9 (b) (red dots) and at V_G=0 V as depicted in Figure 6.9 (c) (blue squares). However, the drain current without gate bias and therewith without gate leakage is a factor of 5 higher than the drain current at V_G =0 V. The higher drain current observed without gate voltage can be explained by the positive surface potential of the c-AlGaN barrier layer causing high charge density in the electron channel. The electron channel is depleted when a gate voltage of V_G=0 V is applied. Additionally, the drain current measured without gate voltage is even higher than the drain current at V_G=2 V. Therefore the electron channel is not fully filled at V_G=2 V.

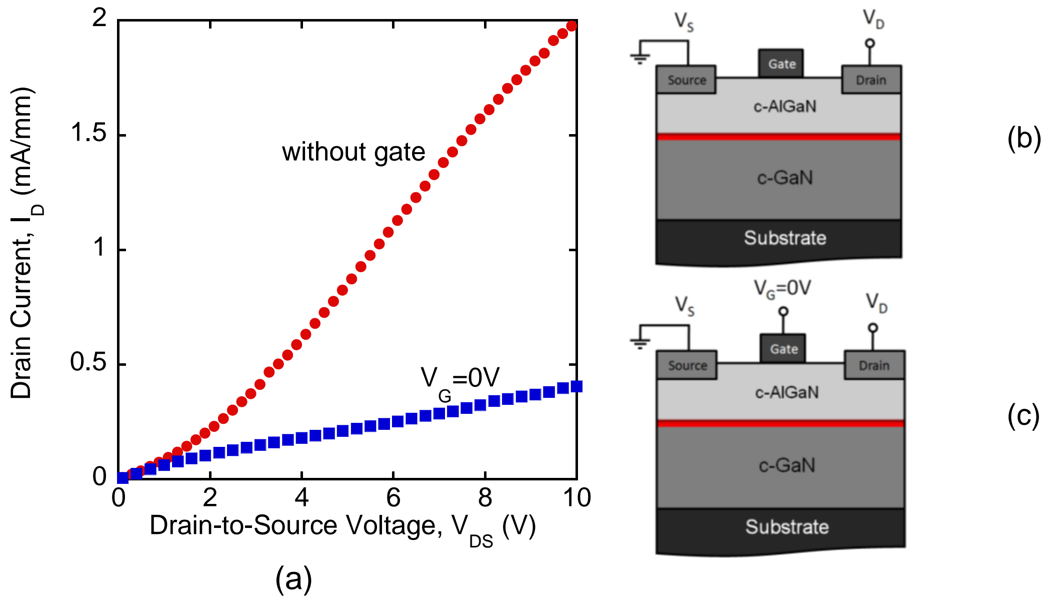


Figure 6.9 (a) Drain-to-source IV characteristics of HFET A without gate voltage (red dots, measurement setup is shown in (b)) and at V_G=0 V (blue squares, measurement setup is shown in (c)).

6.2 Role of Source and Drain Contact Resistance for HFET Devices

Good ohmic contacts of source and drain are essential for the realization of near-ideal HFET device performance. An ohmic contact is defined as a metal-semiconductor contact that has a negligible junction resistance relative to the total resistance of the semiconductor device. A satisfactory ohmic contact should not significantly perturb the device performance and can supply the required current with a voltage drop that is sufficiently small compared with the drop across the active region of the device. The active region of a HFET is the high conductive electron channel. Therefore, the source and drain contact resistance must be lower than the channel resistance.

For low to moderate doping levels and/or moderately high temperature, the specific contact resistance R_c is given by

$$R_c \propto \exp\left(\frac{q\phi_{Bn}}{kT}\right). \tag{6.1}$$

Equation 6.1 shows that a low barrier height should be used to obtain small R_c. The barrier between Ti and c-GaN is nearly 0 eV. Therefore Ti forms an ohmic contact on c-GaN [56].

For higher doping level thermionic electron field emission dominate and R_c is given by

$$R_c \propto \exp\left(\frac{q\phi_{Bn}}{\frac{q\hbar}{2}\sqrt{\frac{N}{m^*\varepsilon_s}}\coth\left(\frac{q\hbar}{2}\sqrt{\frac{N}{m^*\varepsilon_s}}\frac{1}{kT}\right)}\right). \tag{6.2}$$

This type of tunnelling occurs at an energy above the conduction band. With even higher doping level, field emission dominates and the specific contact resistance is given by

$$R_c \propto \exp\left(\frac{q\phi_{Bn}}{\frac{q\hbar}{2}\sqrt{\frac{N}{m^*\varepsilon_s}}}\right). \tag{6.3}$$

Provided that the barrier height cannot be made very small, a good ohmic contact should be operated in the regime of tunnelling.

It is quite obvious that to obtain low values of R_c, a high doping concentration or a low barrier height or both must be used. It is difficult to make good ohmic contacts on wide-gap semiconductors such as AlGaN. A metal does not generally exist with a low enough work function to yield a low barrier. In such cases, the general technique for making an ohmic contact involves the establishment of a more heavily doped surface layer. Another common technique is to add a hetero-junction with a layer of small band-gap material and with high-level doping of the same type. But this would render the semiconductor surface unusable for the realisation of Schottky contacts.

The importance of a low source and drain contact resistance was pointed out by model calculations of output characteristics of c-AlGaN/GaN HFETs using a 2D Simulator ATLAS [32] shown in Figure 6.10. The calculations were performed for a hetero-structure of 30 nm c-$Al_{0.36}Ga_{0.64}N$ with a donor concentration of N_D(c-AlGaN)=5×10^{17} cm^{-3} on 600 nm c-GaN with N_D(c-GaN)=1×10^{15} cm^{-3} and a semi-insulating substrate. For the mobility of the electron channel at the c-AlGaN/GaN hetero-interface μ=100 cm^2/Vs was assumed. Real device dimensions of 2 µm gate length, 25 µm gate width and 3 µm source-to-gate and drain-to-gate spacing were used for the calculation. Figure 6.10 (a) shows the output characteristics calculated for a device with ideal source and drain contact resistance of R_S=R_D=0 Ω and Figure 6.10 (b) shows the calculated output characteristics of the same device with R_S=R_D=400 kΩ what is comparable with real source and drain resistance. The gate voltage in both calculations was varied between V_G=-1V.. 1V. The main difference of the two diagrams is the dimension of the drain current I_D. In case of high contact resistance of R_S=R_D=400 kΩ the HFET transconductance decrease is about three orders of magnitude compared to the device with zero source and drain contact resistance. Thus, it is possible to increase the transconductance of c-AlGaN/GaN HFETs by improved low resistance source and drain contacts.

Below, two alternatives for the reduction of source and drain contact resistance of cubic AlGaN/GaN HFETs are described. Additionally, the temperature dependence of the contact resistance is demonstrated.

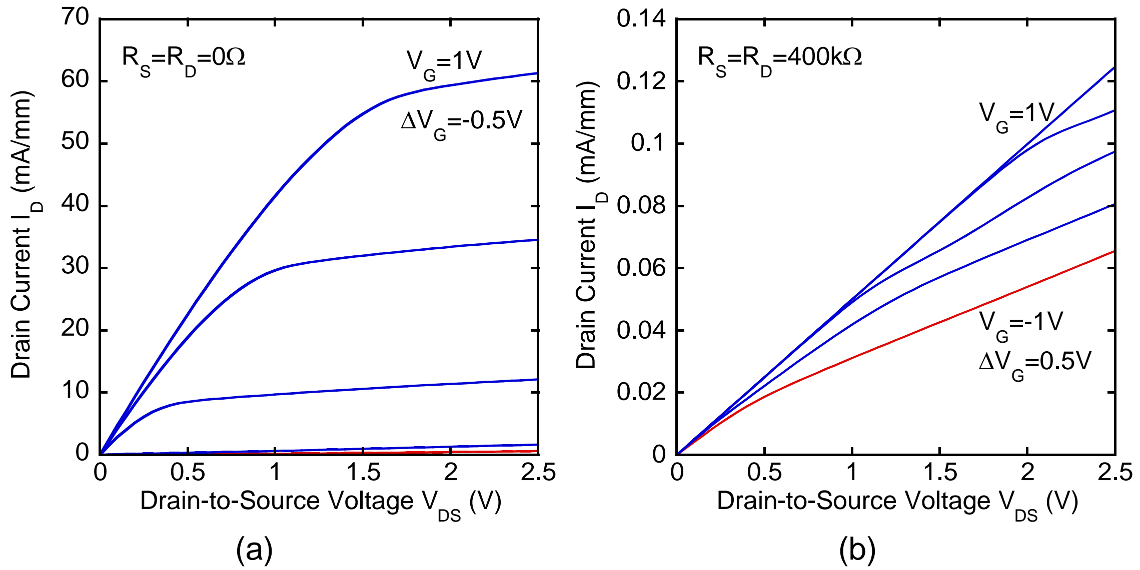


Figure 6.10 Calculated output characteristics of c-AlGaN/GaN HFETs with source and drain contact resistance of (a) 0 Ω and (b) 400 kΩ.

6.2.1 Reduction of Source and Drain Contact Resistance by n^+ GaN Cap Layer

The technique of doping the area underneath the ohmic contacts to reduce the contact resistance is a conventional method for semiconductors. Some groups also used an n^+ GaN cap layer structure to decrease the source and drain resistance of hexagonal AlGaN/GaN HFETs [63]-[65]. In this section, an investigation of the effect of the GaN:Si cap on the optimisation of ohmic contacts on cubic AlGaN/GaN hetero-structures will be presented.

For the investigation, two c-AlGaN/GaN hetero-structures grown on Ar^+ implanted 3C-SiC were used. A schematic cross-sectional view of the samples is shown in Figure 6.11. Sample A (sample 1793) consists of 200 nm UID c-GaN buffer layer followed by 4 nm UID c-$Al_{0.33}Ga_{0.67}N$, 6 nm c-$Al_{0.33}Ga_{0.67}N$:Si and 10 nm UID c-$Al_{0.33}Ga_{0.67}N$. No Si doped c-GaN cap layer was deposited on this sample. Sample B (sample 1809) was of 600 nm UID c-GaN buffer layer, 3 nm UID c-$Al_{0.25}Ga_{0.75}N$ spacer layer, 2 nm c-$Al_{0.25}Ga_{0.75}N$:Si and 15 nm UID c-$Al_{0.25}Ga_{0.75}N$. 5 nm Si doped c-GaN:Si cap layer with expected carrier concentration of n=6×10^{19} cm^{-3} was deposited on top of the sample.

Ohmic contact resistance of both samples was investigated by transmission line method (TLM) described in [66] in detail. For this measurement, Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) contacts were evaporated on the sample surfaces and subsequently thermal annealed at 850 °C for 30 s in nitrogen ambient. Contact pads of 100 μm×200 μm in dimension were linearly arranged with different inter-contact spacing l=5 μm, 10 μm, 15 μm, 20 μm, and 25 μm. The lateral isolation was done by reactive ion etching (RIE) with $SiCl_4$ down to the substrate.

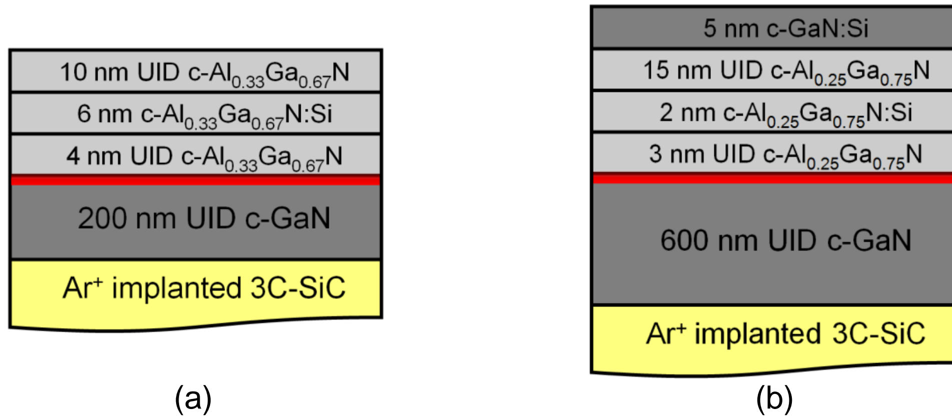


Figure 6.11 Schematic cross-sectional view of c-AlGaN/GaN hetero-structures (a) without (sample A) and (b) with a GaN:Si cap layer (sample B).

Room temperature current-voltage (IV) measurements were performed between contacts with different contact spacing. The total resistance $R = V/I$ was calculated from the IV curves and plotted vs. contact spacing l in Figure 6.12 for sample A (blue dots) and for sample B (red squares). The contact resistance R_c was obtained by the extrapolation of the linear $R(l)$ curves and their intercept with the R axis. A factor of 57 higher contact resistance of R_c=34 kΩ was measured on sample A without a GaN:Si cap layer in comparison to R_c=0.6 kΩ of sample B with a c-GaN:Si cap layer. The contact resistivity of sample A is ρ_c=3.6×10^{-1} Ωcm^2. It is a factor of 200 higher than the contact resistivity ρ_c=1.8×10^{-3} Ωcm^2 of sample B.

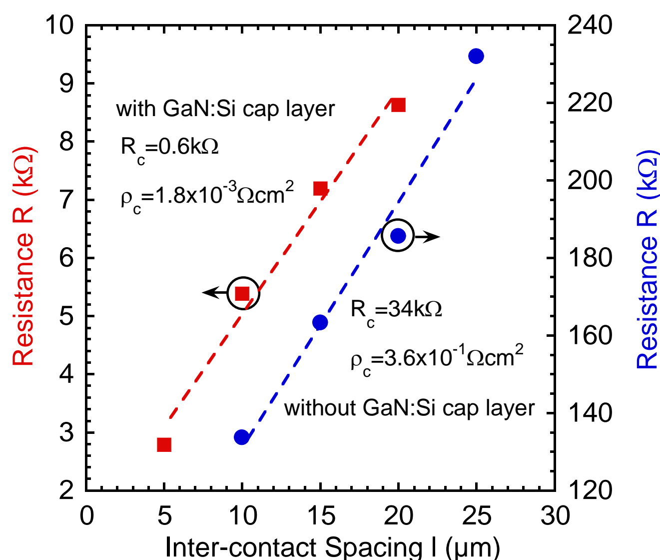


Figure 6.12 TLM resistance R as a function of contact spacing l measured on sample A (blue dots) and sample B (red squares).

The comparison of TLM measurement data of c-AlGaN/GaN hetero-structures of sample A and sample B shows that the contact resistance can be effective reduced by using a heavily doped c-GaN:Si cap layer. HFETs of both samples are introduced in Chapter 5. It was shown that the highest device transconductance was observed on c-AlGaN/GaN hetero-structures with a GaN:Si cap layer. However, for the fabrication of HFETs, the n^+-GaN cap layer has to be removed before gate formation to obtain a good Schottky gate contact with low reverse current and high barrier. This requires a complicated selective GaN etching process.

6.2.2 "Advancing Interface" Ohmic Contact to AlGaN/GaN Hetero-Structures

A metallisation scheme, termed "advancing interface contact" [67], was used to realize low resistance source and drain contacts of c-AlGaN/GaN HFETs. The "advancing interface" contact improves the carrier transport by tunnelling the AlGaN barrier layer in the source and drain regions using a method of thinning out of the AlGaN cap layer by solid state reactions as e.g. RIE. For these investigations, a c-AlGaN/GaN hetero-structure on 3C-SiC/Si substrate with 600 nm UID c-GaN buffer layer and 30 nm UID c-$Al_{0.36}Ga_{0.64}N$ cap layer (sample 1747) was used. HFETs with two different kinds of source and drain were fabricated of this sample as described in Chapter 5. Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) was thermally evaporated for source and drain and subsequently annealed at 850 °C for 30 s in nitrogen atmosphere. The standard contacts were deposited directly on the c-AlGaN surface (sample C). For the "advancing interface" contacts, the c-AlGaN layer was etched by RIE with $SiCl_4$ for 35 s before the metal deposition (sample D). The expected etch depth of c-AlGaN was 10 nm. Both sample structures are depicted in Figure 6.13.

Figure 6.14 shows the output characteristics of both HFET devices. The drain current I_D measured at V_G=0 V of sample D is a factor of 4 higher than the same current of sample

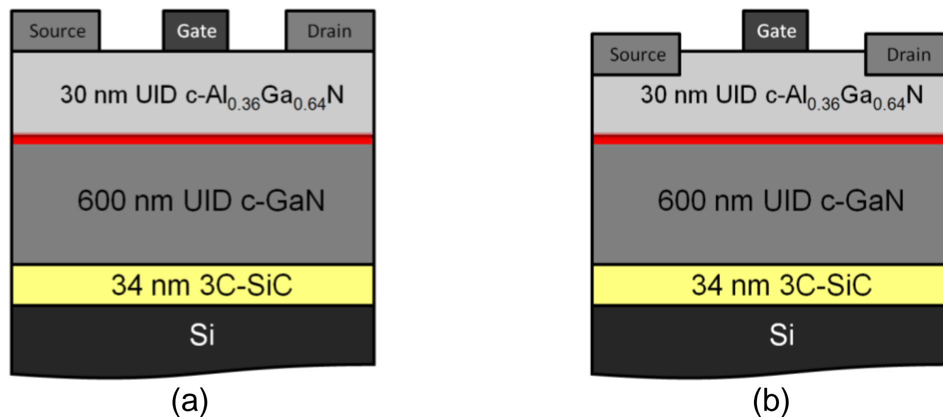


Figure 6.13 Schematic cross-sectional view of c-AlGaN/GaN HFETs (a) with standard source and drain (sample C) and (b) with "advancing interface" source and drain (sample D).

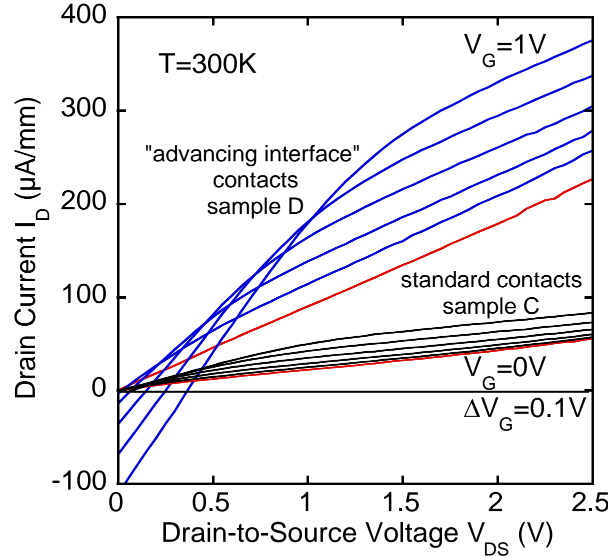


Figure 6.14 Output characteristics of c-AlGaN/GaN HFETs with standard (black curves) und "advancing interface" (blue curves) source and drain contacts.

C. Due to the same layer structure, the gate and buffer leakage must be the same. Therefore, the higher drain current of sample D can be explained by lower source and drain contact resistance. Additionally, as a result of lower contact resistance, a factor of 5.5 higher transconductance was measured on sample D with "advancing interface" contacts than on sample C with standard contacts. One disadvantage of this method is that the contacts are deposited on a low doped c-AlGaN surface and their resistance is still higher than the contact resistance of the same metals deposited on heavily doped c-GaN:Si cap layer.

6.2.3 Temperature Dependence of Source and Drain Contact Resistance

The two dimensional electron gas (2-DEG) sheet resistance R_{sheet} is determined by the 2-DEG density n_{sheet} and the mobility μ according to the formula

$$R_{sheet} = \frac{1}{q\mu n_{sheet}}. \tag{6.4}$$

Therewith high electron channel mobility μ is important for high power HFET devices. Options to improve the c-GaN surface roughness and therewith possible roughness at the c-AlGaN/GaN interface with a view to increase the electron channel mobility μ are described in Chapter 7.1.

From the literature it is well known that the electron mobility μ of a 2-DEG formed at the AlGaN/GaN hetero-interface increases significantly with decreasing temperature [35] so that the temperature-dependence of R_{sheet} is mainly determined by μ. Therefore temperature-dependent electrical measurements were performed on the c-AlGaN/GaN

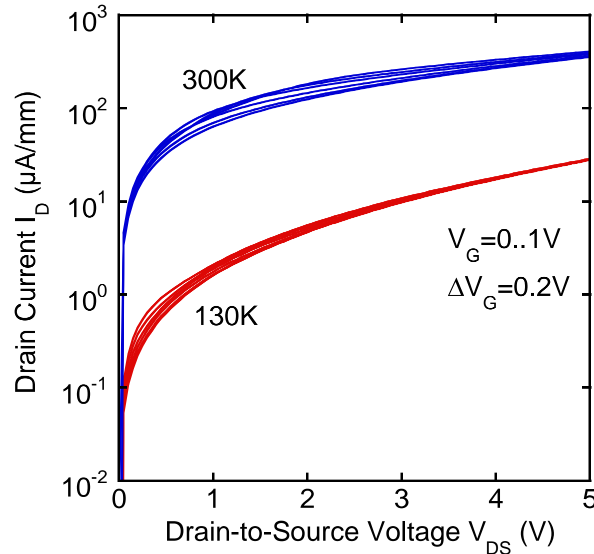


Figure 6.15 Output characteristics of c-AlGaN/GaN HFET sample D at room temperature and at 130 K.

HFET sample D (see Chapter 6.2.2) to obtain potentially higher transconductance than measured at room temperature. Figure 6.15 shows the output characteristics of sample D measured at T=300 K and T=130 K. Without detailed analysis of these measurement curves it is obvious that the room temperature device transconductance is about two orders of magnitude higher than the transconductance measured at T=130 K. A similar current decrease with decreasing temperature was observed in hexagonal AlGaN/GaN hetero-structures in [67] and [68]. It was found that with a lower temperature the contact resistance R_c increases rapidly and limits the current through the sample. It was concluded that the current transport process through the metal-AlGaN/GaN interface is dominated by tunnelling, mainly by the thermionic-field emission.

The measured transconductance, however, is less than the intrinsic transconductance due to the presence of parasitic source and drain resistance. Therefore, to achieve a high transconductance a temperature-independent low-resistance ohmic contact is needed. Low temperature output characteristics of c-AlGaN/GaN HFET sample D measured at T=7 K were analysed in detail. Figure 6.16 (a) shows output characteristics measured at negative gate voltages V_G=0 V..-6 V and Figure 6.16 (b) shows measurement curves at positive gate voltages V_G=0..6 V. The red curve is measured at V_G=0 V. A feature of these measurement data is that a current amplification was measured at negative gate voltages while no field effect is distinguishable at positive gate voltages. To understand these measurement data the following simple model was developed.

Figure 6.17 (a) shows a schematic cross-sectional view of the c-AlGaN/GaN HFET sample D. Due to very high resistance of all three contacts the resistance of the electron channel at the c-AlGaN/GaN interface is insignificant. Therefore, the device can be described by the equivalent circuit diagram depicted in Figure 6.17 (b) with source resistance R_S, gate resistance R_G and drain resistance R_D. In this model we assume

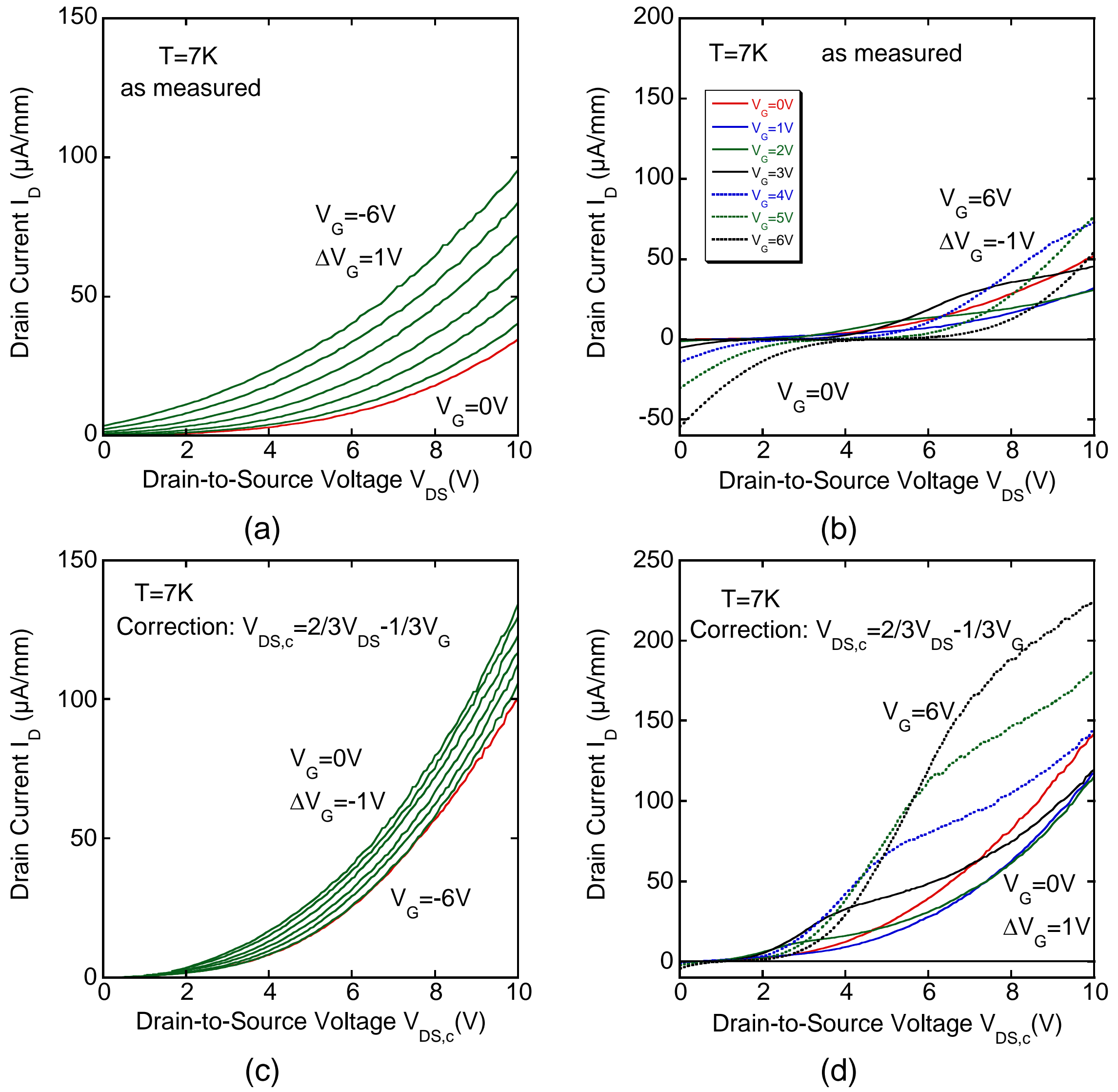


Figure 6.16 Output characteristics of the c-AlGaN/GaN HFET sample D (a) and (b) as measured, (c) and (d) with corrected drain-to-source voltage V_{DS}, measured at 7 K.

R_S=R_G=R_D=R. The source resistance is grounded and V_S=0 V. In first consideration, we set V_G=0 V and apply drain bias of $V_{D,tot}\neq$0 V. As R_S and R_G are connected in parallel the following voltage distribution arises:

$$V_{D,tot} = V_D + V_S = V_D + V_G = V_D + \frac{1}{2}V_D, \tag{6.5}$$

and after a transposition

$$V_D = \frac{2}{3}V_{D,tot}. \tag{6.6}$$

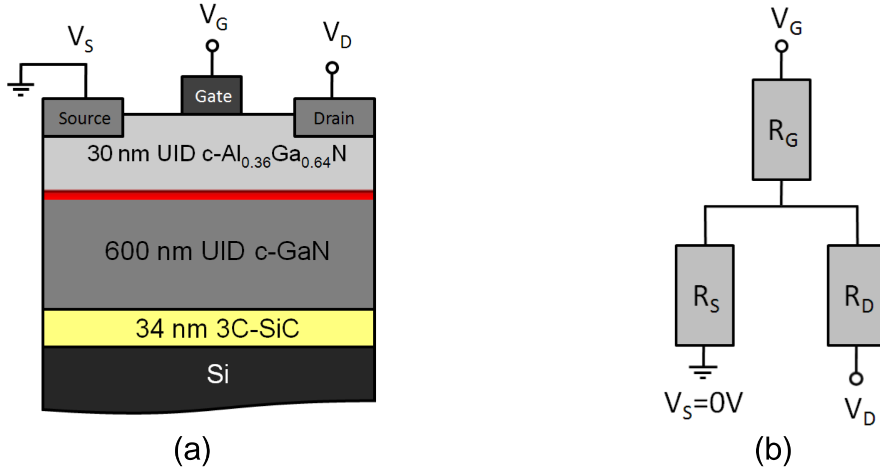


Figure 6.17 (a) Schematic cross-sectional view of the c-AlGaN/GaN HFET sample D. (b) Equivalent circuit diagram of sample D.

That means that only 2/3 of the applied drain voltage drops at the drain contact. With an analogue approach we obtain for V_D=0 V and for the applied gate voltage $V_{G,tot}$

$$V_{G,tot} = V_G + V_D = 3V_D \tag{6.7}$$

$$V_D = \frac{1}{3}V_{G,tot}. \tag{6.8}$$

If we apply both $V_{D,tot}$ and $V_{G,tot}$ the voltage which drops at the drain contact is given by the combination of (6.6) and (6.8):

$$V_D = \frac{2}{3}V_{D,tot} - \frac{1}{3}V_{G,tot}. \tag{6.9}$$

It was set $V_{D,tot}$=V_{DS}, $V_{G,tot}$=V_G and V_D=$V_{DS,c}$ and a new drain-to-source voltage was calculated using equation (6.9). Figure 6.16 (c) and (d) show the corrected output characteristics of the HFET sample D for negative and positive gate bias, respectively. After this correction, the current amplification at negative gate voltages is less distinctive than before and a clear field effect is in evidence at positive gate voltages. Additionally, the gate leakage disappears after the correction. At T=7 K the strong non-ohmic behaviour of source and drain is more noticeable after correction.

This model was applied to room temperature output characteristics of HFET sample D depicted in Figure 6.18 (a) and (b) before and after correction, respectively. After the calculation of the new source-to-drain voltage V_{DS} the gate leakage current caused by forward gate current disappears. However, the shunt current caused by the gate leakage in reversed direction is not corrected. Hereby the model with three equal resistances explains well only the resistances of source, drain and gate contacts.

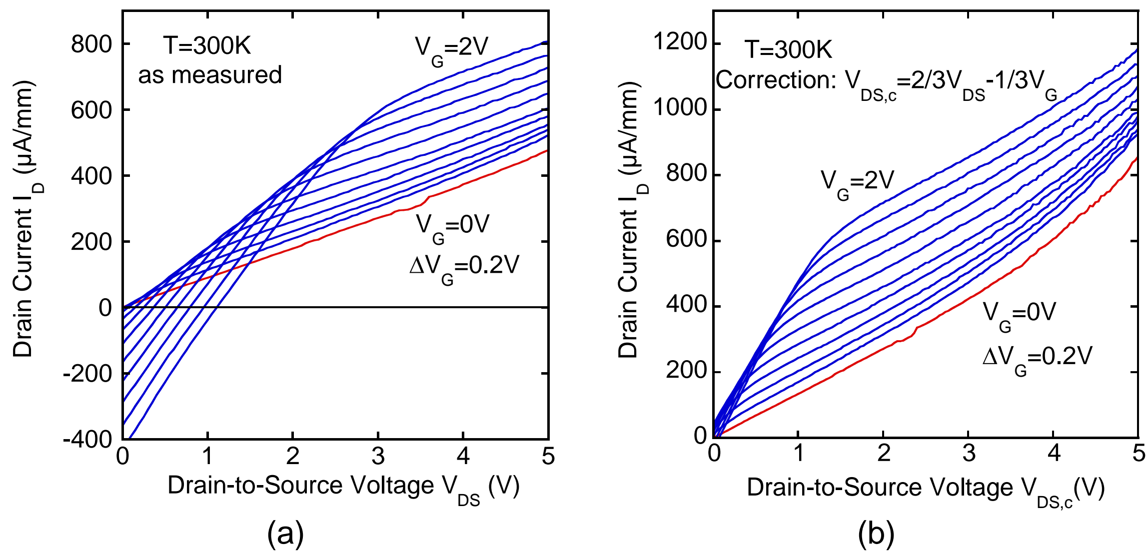


Figure 6.18 Room temperature output characteristics of the c-AlGaN/GaN HFET sample D (a) as measured and (b) with corrected drain-to-source voltage V_{DS}.

In this chapter the importance of good Schottky gate and ohmic Source/drain contacts were demonstrated. It was shown that the background drain current of the c-AlGaN/GaN HFETs is partly caused by the reverse gate current and can be reduced by decreased reverse gate current. This can be achieved by Pd or Ni deposited on a thin c-AlN cap layer. Additionally, the use of a c-AlN cap layer would increase the Schottky barrier and allow HFET performance at higher gate voltages. For high transconductance of the devices low resistance source and drain are necessary. It was demonstrated that the source and drain contact resistance can be reduced by use of a highly doped c-GaN:Si cap layer or so called “advancing interface” contacts.

7 Prospects for New HFET Structures

The output characteristics of non-polar cubic AlGaN/GaN hetero-junction filed-effect transistors are introduced in Chapters 5 and 6. It was shown that the device transconductance of the investigated cubic AlGaN/GaN HFETs is low in comparison to that of similar structures of polar and semi-polar AlGaN/GaN due to high contact resistance of ohmic source and drain, gate leakage or low mobility of charge in the electron channel. Additionally, the dimensions of the devices have an important influence on the output characteristics of HFETs. In this chapter, properties of the investigated transistors are analysed and possible improvements for new devices with normally-off characteristics are discussed.

7.1 Analysis of Crystalline Properties of c-GaN and c-AlGaN

An important parameter describing electron transport is the mobility μ. The most important scattering mechanisms limiting electron transport in 2-DEG at the AlGaN/GaN interface are impurity, dislocation and interface roughness scattering. In smooth hexagonal c-plane AlGaN/GaN with high 2-DEG densities, the 2-DEG mobility is limited by alloy and interface roughness scattering. At low 2-DEG densities, dislocation scattering from charge cores and strain fields are the dominant scattering mechanisms [69]. In [20] it was shown that in cubic AlGaN/GaN hetero-structures impurities and dislocations are not the limiting parameters for mobility. The scattering mechanism which causes the lowest mobility is the interface roughness. It was calculated that the RMS roughness at the c-AlGaN/GaN interface has to be reduced below 1 nm in order to reach the mobility limit due to dislocation scattering for a dislocation density of 10^{10} cm^{-2}.

In this work the RMS roughness and the dislocation density were investigated for c-GaN layers with different thickness. Four c-GaN layers were deposited on carbonized Si with 34 nm thick 3C-SiC (samples 1764, 1766, 1768, 1776). Figure 7.1 (a) shows the RMS roughness (red points) and dislocation density (blue squares) of four c-GaN layers with thicknesses between 200 nm and 1400 nm. The dislocation density was calculated from the FWHM of rocking curve around the (002) reflex of c-GaN using formula (2.6). It is evident that the surface roughness increases and the dislocation density decreases with the layer thickness. Therefore, a thin c-GaN buffer layer of t<100 nm is necessary to obtain high charge mobility at the c-AlGaN/GaN interface.

Assuming equal surface and interface roughness of c-GaN and c-AlGaN/GaN, respectively, even in the 200 nm thick c-GaN sample with RMS roughness of 3 nm and

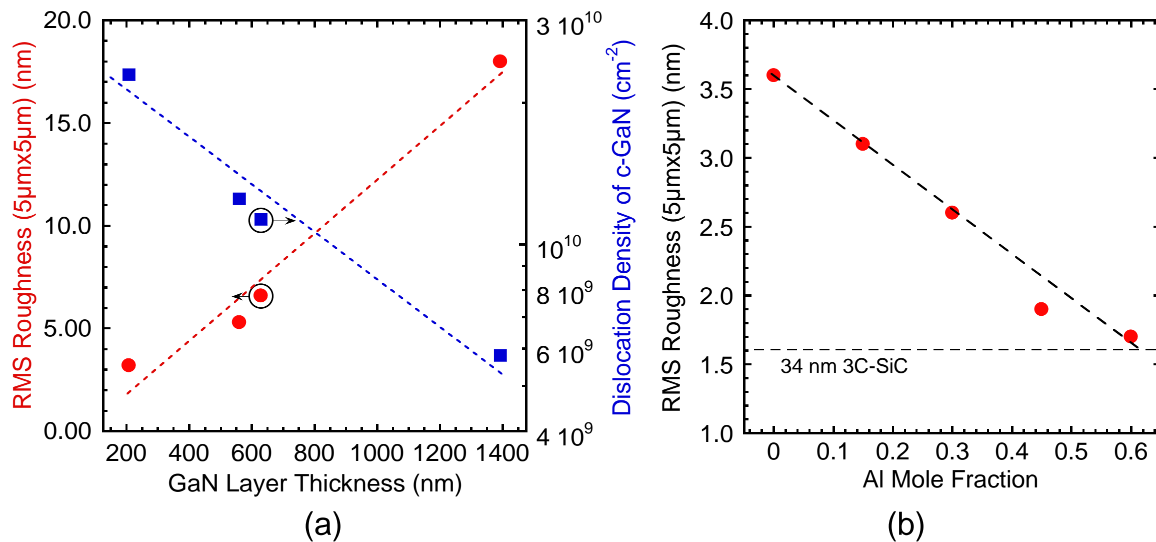


Figure 7.1 (a) RMS roughness (red points) and dislocation density (blue squares) versus c-GaN thickness. (b) RMS roughness of 30 nm c-$Al_xGa_{1-x}N$ on 200 nm c-GaN versus Al mole fraction.

dislocation density of 2×10^{10} cm^{-2} the electron mobility in the 2-DEG channel would be limited by the interface roughness [20]. Therefore another alternative to reduce the roughness at the c-AlGaN/GaN interface was investigated. For this purpose 30 nm c-$Al_xGa_{1-x}N$ with 15% (sample 1777), 30% (sample 1778), 45% (sample 1779) and 60% (sample 1780) Al mole fraction were deposited on a 200 nm thick c-GaN buffer layer. The RMS surface roughness of these samples is depicted in Figure 7.1 (b). In this measurement a surface roughness decrease with increasing Al content was established. RMS roughness of 1.7 nm was measured on c-$Al_{0.6}Ga_{0.4}N$ comparable to the RMS roughness of the 3C-SiC/Si substrate. These measurements show that Al of the c-AlGaN has a smoothing effect on surface. It is expected that the interface roughness of c-GaN/AlGaN with c-AlGaN as a buffer layer will be lower than the roughness of conventional c-AlGaN/GaN interface with c-GaN buffer. Therefore, the charge mobility at the c-GaN/AlGaN interface is expected to be higher than the charge mobility at c-AlGaN/GaN interface. Thus, c-GaN/AlGaN is a potential system for the fabrication of inverted HFETs with increased channel mobility.

7.2 Avoiding of Shunt Current

An isolating layer between the substrate and the device structure is indispensable for HFETs with normally-off output characteristics as demonstrated in Chapter 4.1. Ar^+ ion implantation of free standing 3C-SiC was successfully used to produce an insulation damage layer near the substrate surface. Therefore we prefer this substrate for further new c-AlGaN/GaN HFET devices. However, it is conceivable to skip the lowest implantation doses of 1.2×10^{14} cm^{-3} at 40 keV to conserve the good crystalline nature of 3C-SiC near the substrate surface.

To date, all fabricated HFET devices of cubic AlGaN/GaN feature a high shunt current which can be caused by leakage through the substrate or c-GaN buffer layer. Up to now, it was not possible to find a fully insulating substrate suitable for the epitaxy of cubic GaN, but it is possible to reduce the leakage current through the c-GaN buffer layer. The conductivity of UID c-GaN is presumably due to the background doping with oxygen which is typically about N_D(c-GaN)=1×10^{16}-1×10^{17} cm^{-3}. This conductivity can be decreased by the compensation of oxygen donors by doping of c-GaN with carbon (c-GaN:C) using CBr_4 as described in Chapter 4.4. However, this method is not yet optimized for cubic GaN.

Another simple possibility to reduce buffer leakage is to reduce the c-GaN layer thickness and therewith decrease the layer resistance. To demonstrate the contribution of the c-GaN buffer layer to the transfer charcteristics of HFETs, calculations were performed using ATLAS device simulation software [32]. A typical unintentional doping density of N_D(GaN)=4×10^{16} cm^{-3} was assumed for the c-GaN buffer layer. The gate length was set to L_G=2 µm and the source-to-gate and drain-to-gate spacing to L_{SG}=L_{DG}=3 µm as shown in Figure 7.2 (structure A). No source and drain contact resistance and no substrate were considered in these calculations.

Figure 7.3 shows calculated transfer characteristics at V_{DS}=10 V of c-AlGaN/GaN HFETs with 20 nm δ-doped c-$Al_{0.33}Ga_{0.67}N$ of 4 nm with N_D(c-AlGaN)=4×10^{17} cm^{-3}, 6 nm with N_D(c-AlGaN)=4×10^{18} cm^{-3} and 10 nm with N_D(c-AlGaN)=4×10^{17} cm^{-3} on c-GaN layers with different thicknesses of 50 nm (black dots), 100 nm (blue squares) and 200 nm (green diamonds), respectively. For comparison transfer characteristics of a reference HFET with 200 nm intrinsic c-GaN (red dashed line) is depicted in the diagram. From the transfer characteristics we see that the c-AlGaN/GaN HFET with 200 nm GaN is still not depleted at V_G=-2 V. The threshold voltage of the device with 100 nm c-GaN is lower with V_{th}=-0.7 V and the device with a 50 nm c-GaN buffer has the same threshold voltage as the reference HFET of only V_{th}=-0.3 V. Additionally, the device with 50 nm UID c-GaN is completely depleted at the same gate voltage of V_G=-0.6 V as the reference device with intrinsic c-GaN. Thus the use of an only 50 nm thick UID c-GaN layer would completely avoid the shunt current through the buffer. All introduced devices show normally-on behaviour which is caused by the relatively high δ-layer doping concentration of the c-$Al_{0.33}Ga_{0.67}N$ of N_D(AlGaN)=4×10^{18} cm^{-3} used in this calculation.

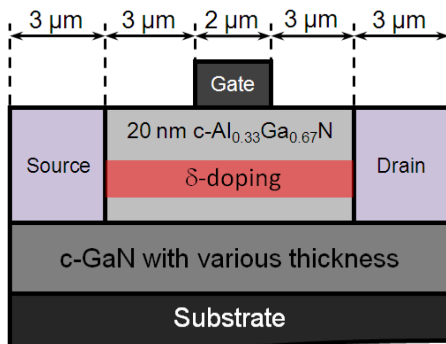


Figure 7.2 Cross sectional view of the c-AlGaN/GaN simulation structure A.

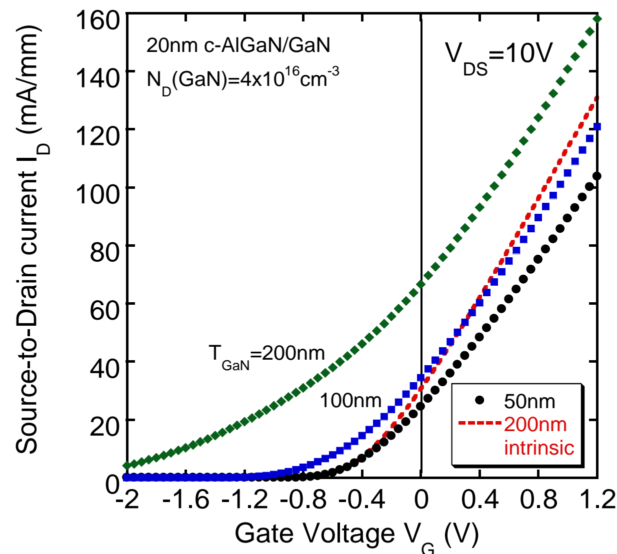


Figure 7.3 Calculated transfer characteristics of a c-AlGaN/GaN HFET with different thicknesses of the c-GaN buffer layer of 200 nm (green diamonds), 100 nm (blue squares), and 50 nm (black dots). The red dashed line shows transfer characteristics of a reference device on intrinsic c-GaN buffer layer.

7.3 Effect of c-AlGaN δ-Doping

The maximum transconductance of HFET devices depends on the maximum carrier sheet density in the channel at the AlGaN/GaN interface (see Equations 3.6 and 3.13). The carriers in the electron channel are generally transferred from the AlGaN barrier to the hetero-interface. Therefore, doping of the AlGaN barrier is necessary to achieve high electron sheet concentration and therewith high device transconductance. The use of a δ-doped layer within the AlGaN barrier placed close to the channel interface allows the local separation of electrons and donors thereby reducing impurity scattering and increasing electron mobility within the channel.

For the estimation of an ideal δ-doping concentration within the c-AlGaN barrier layer, model calculations were performed for c-AlGaN/GaN HFETs with 20 nm c-$Al_{0.25}Ga_{0.75}N$ on 200 nm intrinsic c-GaN as shown in Figure 7.4 using the ATLAS device simulation

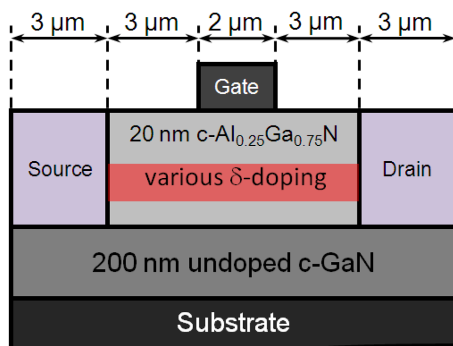


Figure 7.4 Cross sectional view of the c-AlGaN/GaN simulation structure B.

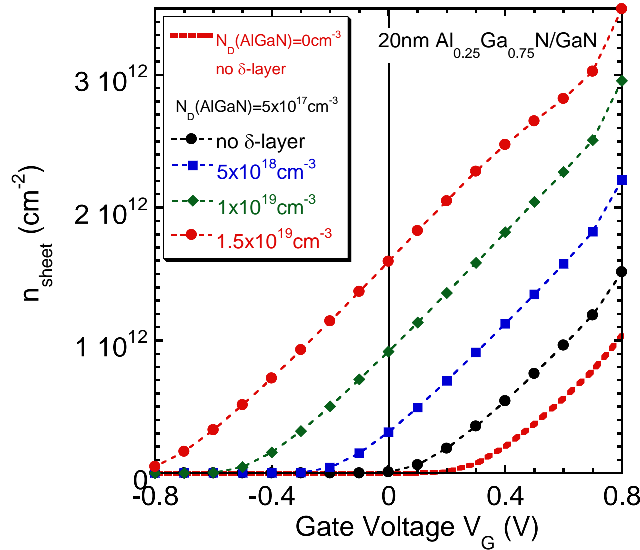


Figure 7.5 Calculated sheet carrier density at the c-$Al_{0.25}Ga_{0.75}N$/GaN hetero-interface vs. gate voltage for different doping of δ-AlGaN layer.

software. The UID concentration of the c-$Al_{0.25}Ga_{0.75}N$ was assumed to be N_D(AlGaN)=5×10^{17} cm^{-3}. A 2 nm thick δ-doped layer was simulated within the AlGaN layer with a spacing of 3 nm to the hetero-interface.

Figure 7.5 shows the calculated sheet carrier concentration n_{sheet} vs. the gate voltage V_G for different doping of the δ-layer N_D(δ) of 5×10^{18} cm^{-3} (blue squares), 1×10^{19} cm^{-3} (green diamonds) and 1.5×10^{19} cm^{-3} (red dots). Additionally, n_{sheet} of devices without δ-doping (black dots) and with intrinsic c- $Al_{0.25}Ga_{0.75}N$ (red dashed line) are depicted in the diagram. According to the calculated curves, both devices without δ-doping are fully depleted already at V_G=0 V. Thus, they are of normally-off characteristics. The other three devices with δ-doped c-AlGaN layers are of normally-on characteristics. However, the electron sheet density at V_G=0.8 V is minimum for the device without δ-doping within c-AlGaN and it increases with increased doping concentration of the δ-layer. The device with N_D(δ)=1.5×10^{19} cm^{-3} exhibits the highest maximum transconductance g_m, but is of normally-on behaviour. These calculated transfer characteristics visualise that intentional doping of the c-AlGaN barrier layer is essential to obtain high device transconductance.

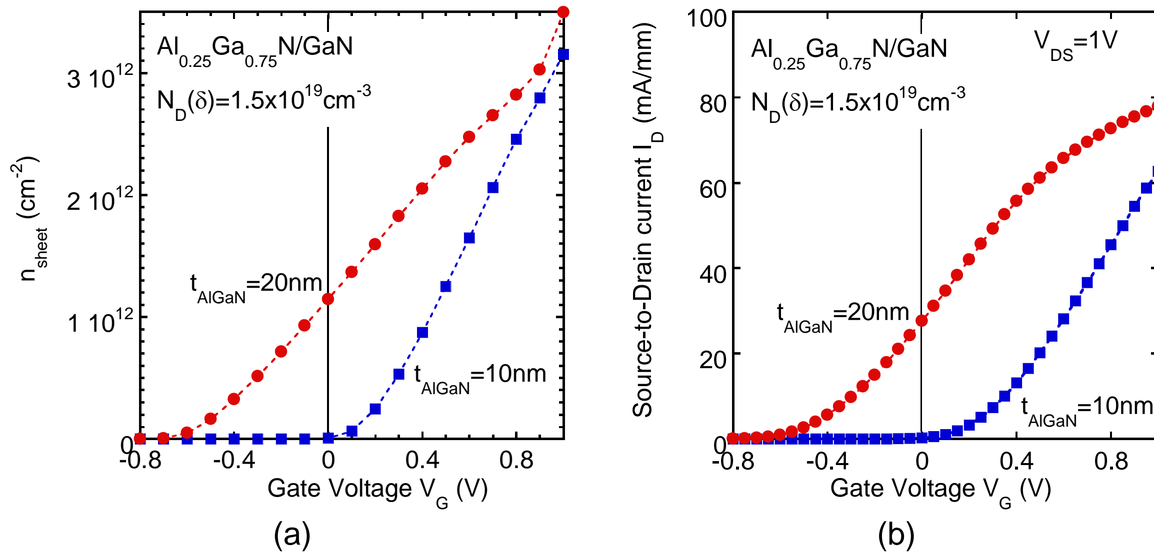


Figure 7.6 Calculated (a) sheet carrier density at the c-AlGaN/GaN hetero-interface vs. gate voltage and (b) transfer characteristics of c-AlGaN/GaN HFET with 20 nm (red dots) and 10 nm (blue squares) c-$Al_{0.25}Ga_{0.75}N$ barrier layer thickness.

7.4 Variation of the c-AlGaN Barrier Thickness

Parameters of the device with the highest δ-doping concentration of $N_D(\delta)=1.5\times10^{19}$ cm^{-3} were used to show the effect of thickness scaling of the c-AlGaN layer on the transfer characteristics of HFET devices. Figure 7.6 (a) shows the calculated sheet carrier density of the devices with 20 nm (red dots) and 10 nm (blue squares) thick c-$Al_{0.25}Ga_{0.75}N$ barrier layer vs. gate voltage. It is evident that the device with 10 nm c-AlGaN is depleted at V_G=0 V whereas its sheet carrier density at V_G=0.8 V is only 10 % lower than the electron sheet density of the device with 20 nm c-AlGaN. The source to drain current of the device with 20 nm c-AlGaN is only a factor of 1.3 higher than the drain current of the device with 10 nm c-AlGaN calculated for V_{DS}=1 V as shown in Figure 7.6 (b). These calculations clarify that it is possible to fabricate normally-off HFET devices of cubic AlGaN/GaN by scaling the c-AlGaN barrier thickness with low loss in transconductance.

7.5 Scaling of the HFET Device Dimensions

The following model calculations show that the HFET device characteristics can be even more improved by scaling the device dimensions. In Figure 7.7 (a) calculated transfer characteristics of c-AlGaN/GaN HFET devices with 10 nm δ-doped c-$Al_{0.25}Ga_{0.75}N$ with $N_D(\delta)=1.5\times10^{19}$ cm^{-3} on 200 nm intrinsic c-GaN at V_{SD}=1 V are shown. The red dotted curve is the source-to-drain current vs. gate voltage of a device with device scaling used for HFET fabrication in this work of L_G=2 µm and L_{SG}=L_{DG}=3 µm. The curve with green diamonds displays the same characteristics for a HFET device with L_G=L_{SG}=L_{DG}=0.5 µm. Smaller spacing between source and drain causes less scattering of charge and therewith

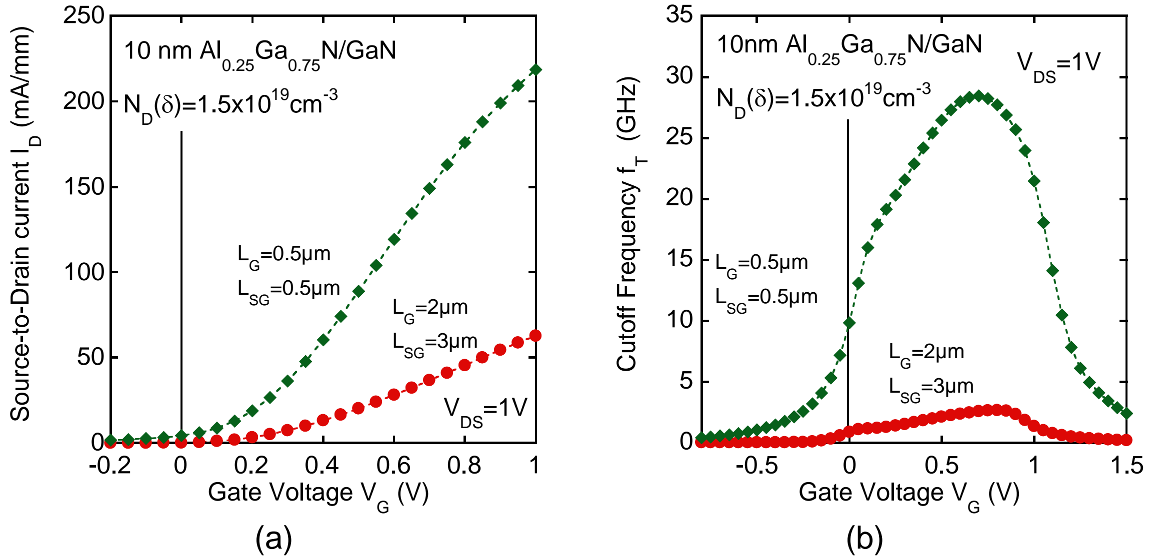


Figure 7.7 Calculated (a) transfer characteristics and (b) cutoff frequency vs. gate voltage for two different scalings of c-AlGaN/GaN HFET devices at V_{DS}=1 V.

higher electron mobility. Therefore, the calculated transconductance of the HFET with 1.5 µm source-to-drain spacing is a factor of three lower than the transconductance of the device with 8 µm source-to-drain spacing.

HFETs are useful for high-speed logic amplifications. As a key parameter for high-speed capability, the cutoff frequency f_T is commonly used. The f_T is defined as the frequency of unity gain at which the small-signal input gate current is equal to the drain current of the intrinsic FET [33]. It is a more appropriate figure-of-merit for digital circuits where speed is the primary concern. The speed limitation of HFETs are dependent on device geometry with the gate length L_G as the most important parameter with the relation $f_T \propto 1/L_G$. Therefore decreasing L_G will increase f_T.

Due to the poor performance of cubic AlGaN/GaN HFETs up to now, no frequency dependent measurements were done in this work. However, cutoff frequency f_T vs. gate voltage V_G was calculated for c-AlGaN/GaN HFETs with a device scaling of L_G=2 µm, L_{SG}=L_{DG}=3 µm and for device scaling of L_G=L_{SG}=L_{DG}=0.5 µm shown in Figure 7.7 (b). A peak cutoff frequency of f_T=30 GHz is calculated for cubic AlGaN/GaN HFET with shorter scaling. This value is a factor of 10 higher than that of the standard device and is comparable to measured cutoff frequencies of hexagonal AlGaN/GaN HEMTs with similar gate length L_G [63].

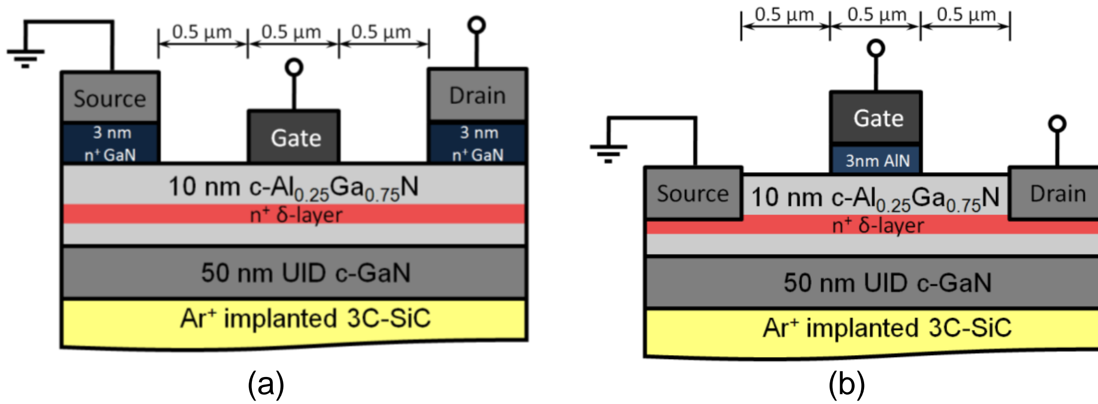


Figure 7.8 Cross sectional view of potential future c-AlGaN/GaN devices.

7.6 Design of Potential Future c-AlGaN/GaN HFETs

In this chapter it was demonstrated that the thickness of the c-GaN buffer layer of c-AlGaN/GaN HFETs has to be <100 nm to obtain a high electron channel mobility μ and to avoid the buffer leakage. Additionally, for high-power c-AlGaN/GaN HFET devices with normally-off characteristics a high δ-doping within a c-AlGaN barrier with t≈10 nm and device scaling are necessary.

Taking into account the above-mentioned calculations, two new designs for future c-AlGaN/GaN HFET devices with normally-off characteristics were modelled. Both devices have scaled contact spacing of L_{SG}=L_{DG}=L_G=0.5 µm and consist of 50 nm UID c-GaN on Ar^+ implanted 3C-SiC, followed by 10 nm δ-doped c-$Al_{0.25}Ga_{0.75}$:Si barrier layer with $N(\delta)=1.5\times10^{19}$ cm^{-3}. The first device shown in Figure 7.8 (a) has a 3 nm thick heavily doped c-GaN:Si cap layer for low resistance source and drain contacts. This cap layer has to be removed in the region between source and drain. The gate contact is positioned on top of the c-AlGaN layer.

The second HFET device structure is depicted in Figure 7.8 (b). It exhibits a 3 nm thick c-AlN cap layer instead of c-GaN:Si to improve the Schottky gate contact. In such devices metals Ti or Ni should be used for the gate (see Chapter 6.1.1). For source and drain, the c-AlN and c-AlGaN have to be etched down to the δ-doped c-AlGaN region.

Due to the small device dimensions of <1 µm the new structures pose new challenges for the fabrication process of c-AlGaN/GaN HFETs.

Summary

The main focus of this work was the fabrication and investigation of hetero-junction field-effect transistors (HFETs) based on cubic AlGaN/GaN. Although the molecular beam epitaxy of cubic GaN and AlGaN is already well investigated and optimized in previous works, the realisation of the HFET devices required solutions of several problems, such as establishing of device fabrication process, realisation of sufficient electrical device decoupling from substrate, and investigation of electrical properties of different metals for electrical source, drain and gate contacts.

For electrical HFET device isolation, substrates of two different types were investigated for the epitaxy of cubic AlGaN/GaN hetero layers. The first one was the carbonised silicon with a 34 nm thick 3C-SiC layer on semi-insulating Si (3C-SiC/SiC). This substrate is useful for the epitaxy of c-AlGaN/GaN and it was possible to fabricate HFETs of c-AlGaN/GaN with normally-off behaviour on this substrate, however the crystalline properties of the hetero-layers were quite poor.

More promising substrate for c-AlGaN/GaN HFET devices was the free-standing 3C-SiC with a surface treated by the Ar^+ ion implantation to induce an electrical isolating damage layer. It was shown that an amorphous layer is generated by the Ar^+ implantation, which epitaxially recrystallises during the thermal annealing. After the recrystallisation the substrate surface offers an insulating template suitable for the good quality c-GaN epitaxy. HFETs with normally-on and normally-off characteristics were realised on the Ar^+ implanted 3C-SiC.

Additionally, carbon doping of c-GaN using a CBr_4 source was investigated for fabrication of insulating c-GaN:C layers which would allow to decouple HFET devices from an electrically conductive substrate as already shown for hexagonal devices. It was found that the incorporated carbon concentration of c-GaN:C is linearly dependent on the BEP of the CBr_4 source. A maximum incorporated carbon concentration of N=2.7×10^{19} cm^{-3} was obtained causing an acceptor surplus of N_A-N_D=2.8×10^{17} cm^{-3} measured by CV. Such high carbon densities can be used for deposition of isolating p-n junction buffers. c-GaN:C layer with lower carbon concentration of N=1.6×10^{19} cm^{-3} showed a two orders of magnitude lower conductivity than the UID GaN layer. c-GaN:C with this density can be used for the device isolation. The advantage of the carbon doping of c-GaN is that the crystalline and optical properties of GaN:C layers are not degraded with higher carbon density. One c-AlGaN/GaN HFET was realized using a c-GaN:C buffer layer.

Cubic AlGaN/GaN hetero-structures were analysed by optical and electrical measurements. The electron channel which is built at the c-AlGaN/GaN hetero-interface

was detected by low temperature PL and room temperature CV measurements. A channel sheet density of about n_{sheet}=3×10^{12} cm^{-2} at the c-AlGaN/GaN interface was measured by CV investigations.

Cubic AlGaN/GaN HFETs were structured by liftoff, RIE and PECVD processes using photolithography. Room temperature output characteristics of both normally-on and normally-off type depending on the doping of the c-AlGaN barrier layer were successfully shown on c-AlGaN/GaN HFETs. A maximum transconductance of 3.3 mS/mm was obtained in the normally-off HFET grown on Ar^{+} implanted 3C-SiC. This value is comparable with the transconductance of AlGaN/GaN HFETs fabricated of semi-polar material.

The output characteristics of cubic AlGaN/GaN HFETs were analysed by model calculations using a 1D-Poisson band diagram calculator and ATLAS device simulation software. It was shown that the shunt current in c-AlGaN/GaN devices can be caused by the gate and/or buffer leakage. The gate leakage can be avoided by improved reverse characteristics of the Schottky gate contact. One way to reduce the buffer leakage is the decrease of c-GaN buffer layer thickness.

New layer and device structures for future c-AlGaN/GaN HFETs were designed. To improve the output and transfer characteristics of a cubic AlGaN/GaN normally-off HFET device, a 10 nm thick δ-doped $Al_{0.25}Ga_{0.75}N$ barrier layer on 50 nm UID c-GaN buffer was necessary. Additionally, the device must be scaled to L_G=L_{GS}= L_{GD}=0.5 µm.

In summary, it was demonstrated in this work that the cubic AlGaN/GaN system provides a basis for HFETs without undesirable parasitic piezoelectric and polarisation effects using the same technologies for normally-on and normally-off devices.

Appendix

Appendix A: List of Symbols

Symbol	Description	Unit
a	Lattice Constant	Å
A	Area	cm^{-2}
b	Burgers Vector	cm
C, C_0	Capacitance	F/cm^{-2}
d_{hkl}	Spacing of the Lattice Planes	cm
D	Dislocation Density	cm^{-2}
E_C	Bottom Edge of Conduction Band	eV
E_F	Fermi Level	eV
E_{Fm}	Metal Fermi Level	eV
E_g	Energy Gap	eV
E_V	Top Edge of Valence Band	eV
$\mathscr{E}$	Electric Field	V/cm
f_T	Cutoff Frequency	Hz
g_m	Transconductance	S
(hkl)	Miller Indices	---
I	Current	A
I_D	Drain-to-Source Current	A
I_G	Gate Current	A
I_{shunt}	Shunt Current	A
L	Length	cm
L_G	Gate Length	µm
L_{GD}	Gate-to-Drain Spacing	µm
L_{GS}	Gate-to-Source Spacing	µm
n	Concentration of free Electrons	cm^{-3}
n_{sheet}	Sheet Density	cm^{-2}
N	Doping Concentration	cm^{-3}
N_A	Acceptor Impurity Concentration	cm^{-3}
N_D	Donor Impurity Concentration	cm^{-3}
p	Concentration of free Holes	cm^{-3}
q	Unit Electronic Charge	C
Q_n	Channel Charge	C/cm^2
$q_{\parallel}, q_{\perp}$	Reciprocal Lattice Constants	$Å^{-1}$

Symbol	Description	Unit
R_C	Contact Resistance	Ω
R_{sheet}	Sheet Resistance	Ω
t	Layer Thickness	nm
T	Temperature	K
v	Carrier Velocity	cm/s
V	Applied Voltage	V
V_{DS}	Drain Voltage	V
V_G	Gate Voltage	V
V_{bi}	Build-in Voltage	V
V_{th}	Threshold Voltage	V
W	Depletion Width	cm
y	Layer Thickness	nm
Z	Width	µm
ε_s	Semiconductor Permittivity	F/cm, C/V·cm
θ	Incident Angle	radians
λ	Wavelength	Å
μ	Drift Mobility	$cm^2/V\cdot s$
ρ_C	Contact Resistivity	Ω·cm
ρ	Charge Density	cm^{-3}
ϕ_{Bn}	Schottky Barrier Height on n-type Semiconductor	V
ϕ_m	Metal Work Function	V
χ_s	Electron Affinity for Semiconductors	V
ψ_{bi}	Build-in Potential at Equilibrium	V
ψ_P	Potential Variation	V

Appendix B: List of Abbreviations

AFM	Atomic Force Microscope/Microscopy
BEP	Beam Equivalent Pressure
BOE	Buffered Oxide Etching
CV	Capacitance-Voltage
c-AlGaN	Cubic AlGaN
c-AlGaN/GAN	Cubic AlGaN/GaN Hetero Structure
c-GaN	Cubic GaN
D	Drain
2-DEG	Two Dimensional Electron Gas
ECV	Electro-Chemical Capacitance-Voltage
FET	Field Effect Transistor
FFT	Fast Fourier Transformation
FWHM	Full Width at Half Maximum
G	Gate
HFET	Hetero-Junction Field-Effect Transistor
HRXRD	High-Resolution X-Ray Diffraction
IV	Current-Voltage
MESFET	Metal-Semiconductor Field-Effect Transistor
MBE	Molecular Beam Epitaxy
PBN	Pyrolytic Boron Nitride
n-channel	Electron Channel
PECVD	Plasma Enhanced Chemical Vapour Deposition
PL	Photoluminescence
rf	Radio Frequency
RHEED	Reflection High Energy Electron Diffraction
RIE	Reactive Ion Etching
RMS	Root Mean Square
RSM	Reciprocal Space Map
S	Source
RTA	Rapid Thermal Annealing
SEM	Scanning Electron Microscope/Microscopy
SIMS	Secondary Ion Mass Spectroscopy
TEM	Transmission Electron Microscope/Microscopy
TLM	Transmission Line Method
UHV	Ultra-High Vacuum
UID	Unintentional Doping/Doped
UV	Ultraviolet

Appendix C: List of Room Temperature Parameters

Property	c-GaN [70]	c-AlN [70]	3C-SiC [70]
Energy Gap (eV)	3.26 (d) [11]	5.3 eV (i) [13] 5.93 eV (d) [13]	2.4 eV (i) [15] 6.7 eV (d) [15]
Lattice Constant (Å)	4.53 Å [11]	4.37 Å [12]	4.359 Å [14]
Atom Density (cm^{-3})	4.3×10^{22}	4.79×10^{22}	4.83×10^{22}
Density (g/cm^3)	6.09	3.26	3.21
Melting Point (K)		3273 (h)	3103
Dielectric Constant	9.7 (static) 5.3 (hf)	8.5-9.14 (static) (h) 4.6-4.84 (hf) (h)	9.72 (static) 6.52 (hf)
Debye Temperature Θ_D (K)	600	1150 (h)	1200
Effective Electron Mass m_e	$0.13m_0$	$0.19m_0$	$0.68m_0$
Effective h-Hole Mass m_{hh} $m_{[100]}$ $m_{[111]}$ Effective l-Hole Mass m_{lh} $m_{[100]}$ $m_{[111]}$	$1.3m_0$ $0.8m_0$ $1.7m_0$ $0.19m_0$ $0.21m_0$ $0.18m_0$	---	---
Electron Affinity (eV)	4.31 [20]	0.6 [60]	---
Elastic Coefficients (GPa) C_{11} C_{12} C_{44}	 293 159 155	 304 [71] 152 [71] 199 [71]	 290 235 55

(d): direct
(i): indirect
(h): hexagonal
(hf): high frequency

Appendix D: List of Samples

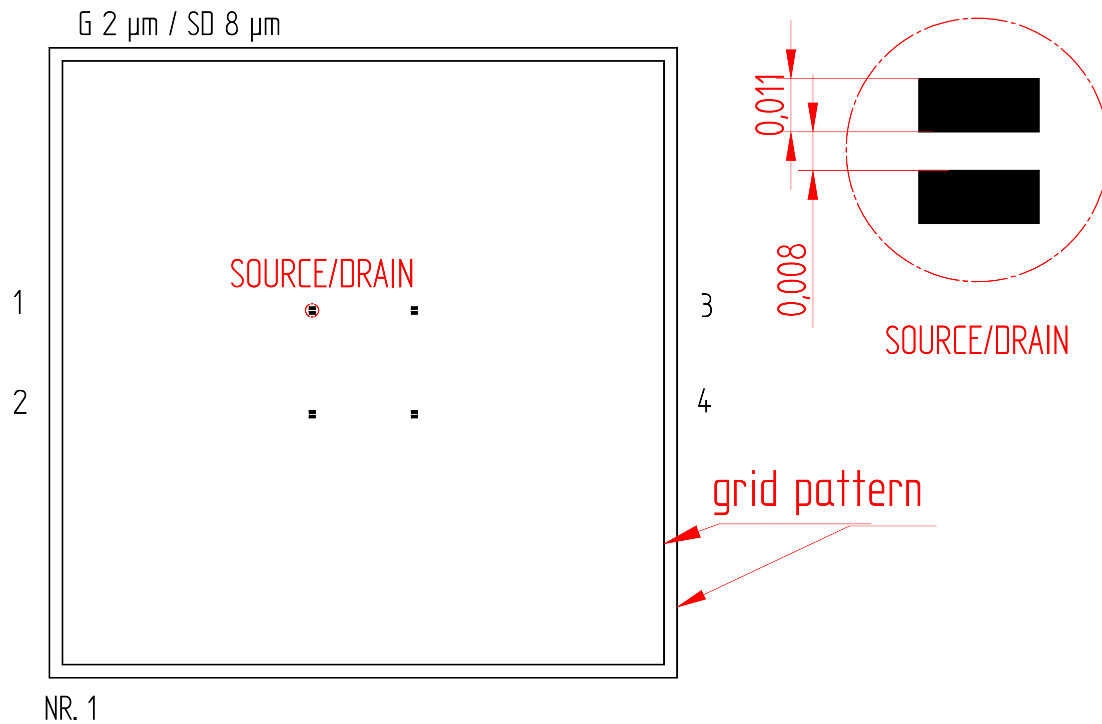
Sample Number	Substrate	Substrate Type	c-GaN Layer	c-AlGaN Layer	Comment
1663	SEK04AK	3C-SiC	650 nm UID GaN	---	---
1687	SEK04AK	3C-SiC	600 nm UID GaN	---	---
1747	PC575a	3C-SiC/Si	600 nm UID GaN (b)	30 nm UID $Al_{0.36}Ga_{0.67}N$ (t)	HFET B
1764	PC542a	3C-SiC/Si	210 nm UID GaN	---	---
1766	PC542a	3C-SiC/Si	630 nm UID GaN	---	---
1768	PC542a	3C-SiC/Si	1390 nm UID GaN	---	---
1776	PC542a	3C-SiC/Si	560 nm UID GaN	---	---
1777	PC542a	3C-SiC/Si	150 nm UID GaN (b)	30 nm UID $Al_{0.15}Ga_{0.85}N$ (t)	---
1778	PC542a	3C-SiC/Si	150 nm UID GaN (b)	30 nm UID $Al_{0.30}Ga_{0.70}N$ (t)	---
1779	PC542a	3C-SiC/Si	150 nm UID GaN (b)	30 nm UID $Al_{0.45}Ga_{0.55}N$ (t)	---
1780	PC542a	3C-SiC/Si	150 nm UID GaN (b)	30 nm UID $Al_{0.60}Ga_{0.30}N$ (t)	---
1793	SEK04AK	Ar^+ implanted 3C-SiC	200 nm UID GaN (b)	4 nm UID $Al_{0.33}Ga_{0.67}N$ 6 nm $Al_{0.33}Ga_{0.67}N$:Si, $\delta=4\times10^{18}$ cm^{-3} 10 nm UID $Al_{0.33}Ga_{0.67}N$ (t)	HFET A
1809	SEK04AK	Ar^+ implanted 3C-SiC	600 nm UID GaN (b) 5 nm GaN:Si cap, $n=6\times10^{19}$ cm^{-3}	3 nm UID $Al_{0.25}Ga_{0.75}N$ 2 nm $Al_{0.25}Ga_{0.75}N$:Si, $\delta=4.5\times10^{18}$ cm^{-3} 15 nm UID $Al_{0.33}Ga_{0.67}N$ (t)	HFET C
1824	SFE14AT	3C-SiC	200 nm UID GaN (b)	120 nm UID $Al_{0.25}Ga_{0.75}N$ (t)	---
1832	SFE14AT	3C-SiC	65 nm UID GaN (b) 530 nm GaN:C 130 nm UID GaN (t)	---	$N_C=3\times10^{19}$ cm^{-3}
1833	SFE14AT	3C-SiC	65 nm UID GaN (b) 530 nm GaN:C 130 nm UID GaN (t)	---	$N_C=1.6\times10^{19}$ cm^{-3}
1834	SFE14AT	3C-SiC	715 nm UID GaN	---	---
1843	SFE14AT	3C-SiC	65 nm UID GaN (b) 530 nm GaN:C 130 nm UID GaN (t)	---	$N_C=2.7\times10^{19}$ cm^{-3}
1855	SFE14AT	Ar^+ implanted 3C-SiC	60 nm UID GaN (b) 580 nm GaN:C	34 nm $Al_{0.36}Ga_{0.64}N$:Si, $n=1.5\times10^{18}$ cm^{-3}	HFET D
1865	SEJ19AK	3C-SiC	600 nm UID GaN (b)	30 nm $Al_{0.35}Ga_{0.65}N$	ECV
1867	SFE29AL	3C-SiC	600 nm UID GaN (b)	30 nm UID $Al_{0.37}Ga_{0.63}N$ 10 nm UID AlN	---
1868	SFE29AL	3C-SiC	650 nm UID GaN	---	ECV

3C-SiC/Si: carbonized Si substrate
3C-SiC: free standing 3C-SiC (HOYA)
(b): bottom
(t): top

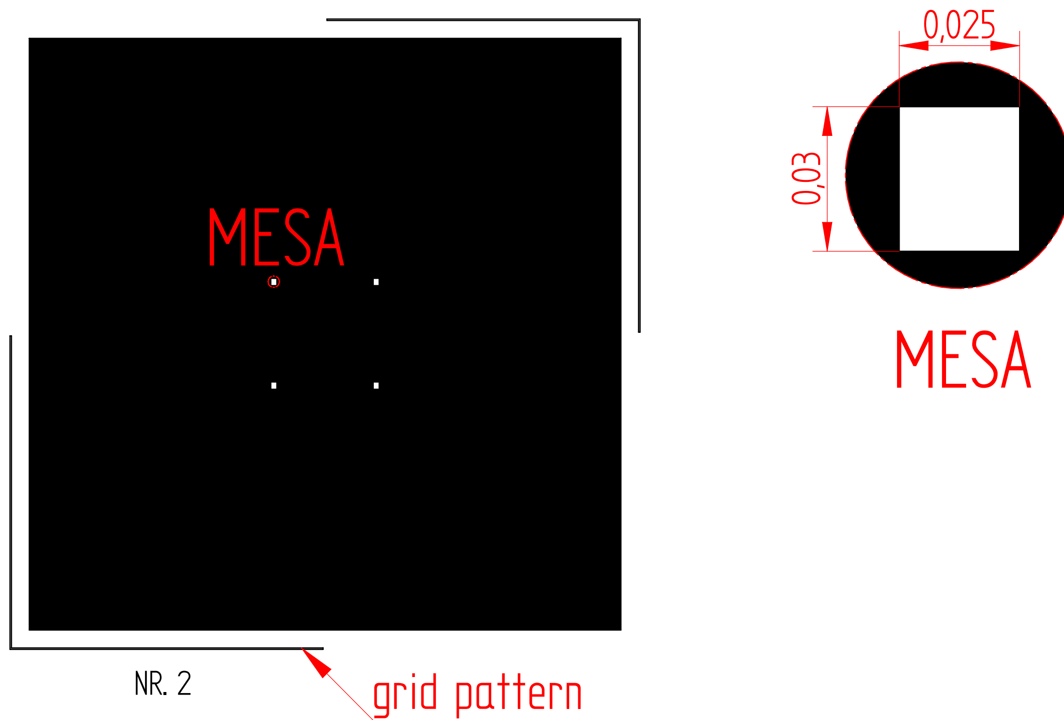
Appendix E: Drawing of Photomasks for FET Fabrication

The FET processing using the photomasks is described in Chapter 2.4.2.

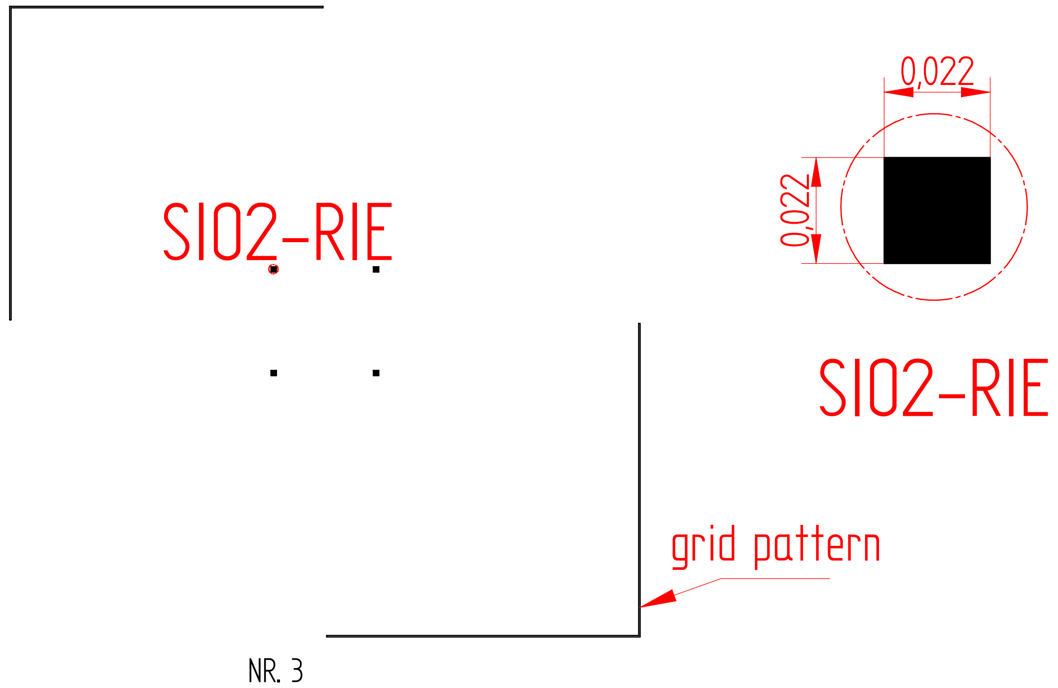
1. Source and drain stacks:



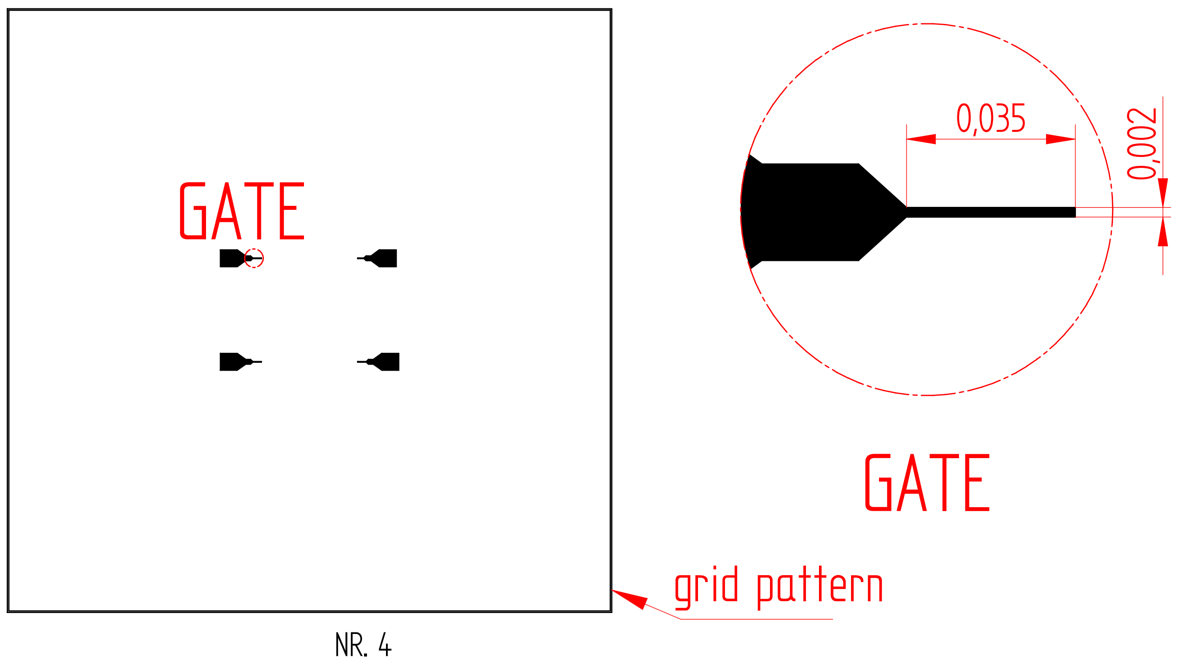
2. Mesa isolation:



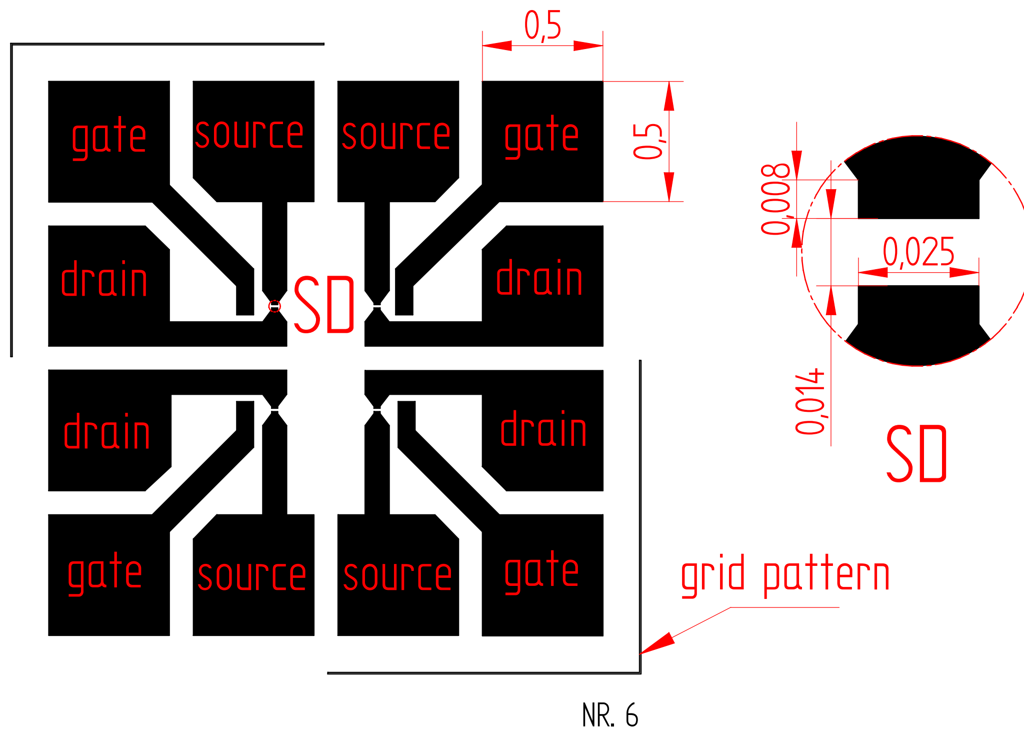
3. **Mesa opening by SiO_2 etching:**



4. **Gate finger:**



5. Contact pads:



6. RIE/PECVD Parameters:

	c-GaN RIE	SiO_2 PECVD	SiO_2 RIE
Gas	$SiCl_4$	SiH_4:N_2O	Ar:CHF_3
Flux (sccm)	25	425:710	10.5:10.5
Pressure (mTorr)	10	100	35
rf Power (W)	300	20	150
Temperature (°C)	20	300	20
etch/deposition rate (nm/min)	40	80	35

Appendix F: Simulation Software

a) Band Diagram Calculator "1D Poisson/Schrödinger"

The program "1D Poisson/Schrödinger" [31] was used for calculations of c-AlGaN/GaN energy-band diagrams and CV characteristics. This program uses the method of finite differences to find the one-dimensional band diagram of a semiconductor structure. The program is menu-driven through a pseudo-Mac interface but the user must provide separate text editing and plotting programs (a shareware text editing program is included in the 1D Poisson distribution).

In the input file semiconductors are called out by name, and the program automatically retrieves the physical parameters and even calculates the parameters for a ternary based on a given x value. Semiconductors within the materials file are organized into families so that parameters such as band offset are defined within a family and do not interfere with definitions in other families. The mobile charge concentrations are calculated using Boltzmann statistics with the addition of the Unger approximation for mild degeneracy and the Sommerfeld approximation for deep degeneracy and dopant ionization is also considered. If requested, the mobile charge can be calculated from a solution of Schrödinger's equation. The program calculates the conduction and valence bands and the hole and electron concentration. Dopant ionization is included for both shallow and deep level dopants. This allows to treat materials such as semi-isolating GaAs. The current flow is not calculated, so the structure can be simulated only in thermal equilibrium. In the used version of the program (*1D Poisson Win Beta8c*), three possible boundary conditions can be defined for surface and substrate, namely Schottky barrier, ohmic contact, and energy band slope = 0. If a Schottky barrier is used the program can simulate the effect of an applied bias which does not cause a significant current flow.

The input to the 1D Poisson program is a text file which contains the information necessary to simulate the structure. This file is created using a text editing program. An example file is shown below for the band structure of HFET A shown in Figure 5.8:

<table>
<tr><th>Example File</th><th>Comment</th></tr>
<tr><td><pre>surface schottky=0.8 v1
AlGaN t=10nm x=0.33 Nd=4e17
AlGaN t=6nm x=0.33 Nd=4e18
AlGaN t=4nm x=0.33 Nd=4e17
GaN t=200nm Nd=4e16
SiC t=100nm Nd=1e12
substrate ohmic v2
v1 0.3
v2 0

temp=300K
dy=5</pre></td><td>A Schottky contact with a barrier of 0.8 eV is set on the $Al_{0.33}Ga_{0.67}N$ surface and is biased with 0.3 V. The layer information is input between the delimiters "surface" and "substrate". The top $Al_{0.33}Ga_{0.67}N$ consists of three layers with a donor concentration of N_D=4×10^{17} cm^{-3}, 4×10^{18} cm^{-3} and 4×10^{17} cm^{-3}. The GaN layer is 200 nm thick with N_D=4×10^{16} cm^{-3}. The SiC layer is 100 nm thick with N_D=1×10^{12} cm^{-3}. The bottom contact is an ohmic contact at V=0 V. The simulation must be performed at room temperature.</td></tr>
</table>

The semiconductor parameters are defined in the “materials” file. The section for c-GaN is shown below:

Materials File	Comment
#c-GaN material parameters---------------------------------> Start GaN binary GaN cubic ← Line 1 +3.200E+00 +0.000E+00 +8.900E+00 +1.500E-01 +1.000E+00 +8.000E-01 +1.800E-01 +2.700E-02 +2.150E-01 +5.500E-02 +0.000E+00 +0.000E+00 ← Line 2 +0.000E+00 +0.000E+00 +0.000E+00 +0.000E+00 +1.000E+02 +1.000E+02 +1.000E-08 +1.000E-08 +0 ← Line 3 AlGaN ternary GaN cubic ← Line 1a 0.000E+00 0.000E+00 0.000E+00 0.000E+00 ← Line 2a eg 0.000 1.000 3.200E+00 1.850E+00 0.000E+00 ← Line 3a dec 0.000 1.000 0.000E+00 1.33E+00 0.000E+00 er 0.000 1.000 8.900E+00 -5.000E-01 0.000E+00 ed 0.000 1.000 2.700E-02 0.000E+00 0.000E+00 ea 0.000 1.000 2.150E-01 0.000E+00 0.000E+00 edd 0.000 1.000 5.500E-02 0.000E+00 0.000E+00 eda 0.000 1.000 0.000E+00 0.000E+00 0.000E+00 me 0.000 1.000 1.500E-01 4.000E-02 0.000E+00 val 0.000 1.000 1.000E+00 0.000E+00 0.000E+00 mh 0.000 1.000 8.000E-01 4.000E-01 0.000E+00 mlh 0.000 1.000 1.800E-01 1.500E-01 0.000E+00 bar 0.000 1.000 0.000E+00 0.000E+00 0.000E+00 emo 0.000 1.000 1.000E+02 0.000E+00 0.000E+00 hmo 0.000 1.000 1.000E+02 0.000E+00 0.000E+00 tn 0.000 1.000 1.000E-08 0.000E+00 0.000E+00 tp 0.000 1.000 1.000E-08 0.000E+00 0.000E+00 al 0.000 1.000 1.080E-07 0.000E+00 0.000E+00 ← Line 19a endAlGaN SiC binary GaN cubic +2.403E+00 -2.500E-01 +9.750E+00 +3.400E-01 +1.000E+00 +1.300E+00 +1.900E-01 +2.700E-02 +2.1500E-01 0.000E+00 0.000E+00 +1.000E+00 +1.000E+00 +1.000E+00 +1.000E+00 +4.500E+01 +4.000E+01 +1.000E-08 +1.000E-08 +0.000E-00 +2.500E-07 #c-GaN material parameters---------------------------------> End	The units are cm for length, and C/cm^2 for polarization. If a binary, the information is given as below: Line 1: Semiconductor name, "binary", semiconductor family, comment. Parameters of c-GaN: Line 2: Energy gap, band offset, rel. dielectric constant, electron eff. mass, cond. band valley degeneracy, heavy hole eff. mass, light hole eff. mass, donor ionization energy, acceptor ionization, deep donor ionization, deep acceptor ionization. Line 3: Donor concentration, acceptor conc., deep donor conc., deep acceptor conc., electron mobility, hole mobility, electron lifetime, hole lifetime, polarization, absorption coefficient There are 20 lines for Al$_x$Ga$_{1-x}$N: Line 1a: Semiconductor name, "ternary", semiconductor family, comment Line 2a: Donor concentration, acceptor conc., deep donor conc., deep acceptor conc., dummy number (optional, not used) Lines 3a-19a are one line for each parameter. On each line is a 2-3 letter descriptor, followed by 1 to 3 groups of 5 numbers defining the coefficients of the 2nd order polynomial describing the parameter, and defining the x interval over which it is valid. The order is as follows: x_{min}, x_{max}, constant, linear, quadratic. The parameter lines are in the order: Energy gap, band offset, rel. dielectric constant, donor ionization energy, acceptor ionization, deep donor ionization, deep acceptor ionization, electron eff. mass, cond. band valley degeneracy, heavy hole eff. mass, light hole eff. mass, electron mobility, hole mobility, electron lifetime, hole lifetime, absorption coefficient.

b) ATLAS Device Simulation Software

ATLAS device simulation software was used for calculations of output and transfer characteristics of c-AlGaN/GaN HFETs. ATLAS is a physically based device simulator which predicts the electrical characteristics that are associated with specified physical structures and biased conditions. This is achieved by approximating the operation of a device onto a two dimensional grid consisting of number of grid points called nodes. By applying a set of different equations onto this grid it is possible to simulate the transport of carriers through a structure. The performance of a device can be modelled in DC, AC or transient modes of operation.

ATLAS is based on a mathematical model of the operation of any semiconductor device. This model consists of a set of fundamental equations which link together the electrostatic potential and the carriers densities within some simulation domain. These equations which are solved inside any general purpose device simulator have been derived from Maxwell's laws and consist of Poisson's equation, the continuity equations and the transport equations. Poisson's equation relates variations in electrostatic potential to local charge densities. The continuity equations describe the way that the electron and hole densities evolve as a result of transport processes, generation processes and recombination processes. The mathematical model implemented into ATLAS is described in Chapter 3 of the ATLAS User's Manual [32].

Following parameter file was used for the simulation of output and transfer characteristics of HFET A shown in Figure 5.6 and 5.7:

```
### material Parameters for 1D cubic AlGaN/GaN structure on 3C-SiC
substrate (1793)            ###
### => same parameters as in 1D-SP-solver
##########################################################################
#
###############################
### 3C-SiC                  ###
###############################
#
# electron affinity [eV]:
set Chi_SiC = $Chi_Si - $dEc_SiC
# band gap [eV]:
set Eg_SiC = 2.36
# electron density of states effective mass [me0]:
set med_SiC = 0.72
# hole density of states effective mass [me0]:
set mhd_SiC = 0.6
# dielectric constant:
set eps_SiC = 9.72
#
###############################
### cubic GaN               ###
###############################
#
# conduction band offset cGaN/3C-SiC [eV]:
set dEc_GaN = -0.09
# electron affinity [eV]:
set Chi_GaN = $Chi_SiC - $dEc_GaN
# band gap [eV]:
```

```
set Eg_GaN = 3.07

# electron density of states effective mass [me0]:
set med_GaN = 0.193
# hole density of states effective mass [me0]:
set mhd_GaN = 0.908
# dielectric constant:
set eps_GaN = 9.5
#
###############################
### cubic AlGaN, x=0.33     ###
###############################
#
# Al-content:
set x_Al = 0.33
# conduction band offset cubic AlGaN/GaN [eV]:
set dEc_AlGaN = 0.580
# electron affinity [eV]:
set Chi_AlGaN = $Chi_GaN - $dEc_AlGaN
# band gap [eV]:
set Eg_AlGaN = 3.991
# electron density of states effective mass [me0]:
set med_AlGaN = 0.234
# hole density of states effective mass [me0]:
set mhd_AlGaN = 1.106
# dielectric constant:
set eps_AlGaN = 9.5
```

The HFET A was defined as followed:

```
####################################################################################
##### 2D cubic AlGaN/GaN HEMT structure on semi-insulating 3C-SiC substrate #####
##### with delta-doping in AlGaN barrier (FET 1793)                        #####
####################################################################################
---
#
# gate length:
set L_g = 2.0
# length of SD contacts:
set L_scont = 3.0
# S-G and G-D spacing:
set L_sg = 3.0
#
### 3C-SiC1 ###
# thickness:
set t_SiC1 = 40.0
# doping:
set Nd_SiC = 2e18
set Ed_SiC = 0.009
#
### 3C-SiC2 ###
# thickness:
set t_SiC2 = 0.095
# doping:
set Nd_SiC = 2e18
set Ed_SiC = 0.009
#set Na_SiC = 4.6e19
# Na > Ncrit(3.94e+18) => full ionization
#
### cAlGaN1 ###
# thickness:
set t_AlGaN1 = 0.004
# doping:
set Nd_AlGaN1 = 4e17
set Ed_AlGaN1 = 0.013
#
### cAlGaN2 ###
# thickness:
set t_AlGaN2 = 0.006
# doping:
set Nd_AlGaN2 = 4e18
# Nd > Ncrit(1.65e+18) => full ionization
#
### cAlGaN3 ###
# thickness:
set t_AlGaN3 = 0.010
# doping:
set Nd_AlGaN3 = 4e17
set Ed_AlGaN3 = 0.013
#
### Gate ###
```

<table>
<tr>
<td>
#
3C-SiC3
thickness:
set t_SiC3 = 0.005
doping:
set Nd_SiC = 2e18
set Ed_SiC = 0.009
#
cGaN
thickness:
set t_GaN = 0.2
doping:
set Nd_GaN = 4e16
set Ed_GaN = 0.018
#
</td>
<td>
Schottky barrier height [eV]:
set phi_barrier = 0.8
workfunction [eV]
set phi_G = $Chi_AlGaN + $phi_barrier
#

</td>
</tr>
</table>

Appendix G: Conventional Interpretation of CV Data

Doping profiles in semiconductors are commonly determined by a differential capacitance technique. In our measurements a metallic Schottky contact is formed at the surface of the semiconductors. This contact is placed in reverse bias and the capacitance of the transition layer is measured as a function of the bias voltage. The analysis of the CV relationship is conveniently done using the depletion-layer approximation in which the semiconductor is assumed to be divided in two distinct regions: a layer that is entirely depleted of charge carriers and an interior region of perfect charge neutrality as illustrated in Figure G.1 [57]. In this notation, x is the distance from the contact into the semiconductor, w the width of the depletion layer, $N(x)$ the net density of ionised impurity atoms and $n(x)$ the density of majority carriers. Specifically, the usual assumptions are that $n(x)$=0 for $0 < x < w$ and that for $x > w$ the semiconductor is electrically neutral with $n(x)$=$N(x)$. Minority carriers are neglected throughout.

Figure G.1 shows the assumed sharp edge of $n(x)$ for two bias voltages that differ by a small increment ΔV, thus producing an increment in width Δw. In effect, the majority-carrier increment

$$\Delta n(x) = n_1(x) - n_2(x), \tag{G.1}$$

shown shaded in Figure G.1, provides a sample of the doping profile $N(x)$ at $x = w$. The charge removed from the edge of the depletion layer is

$$\Delta Q = qN(w)\Delta w, \tag{G.2}$$

where q is the magnitude of the electronic charge. The charge ΔQ is passed through the external circuit, while within the depletion layer there is produced an increment of electric field

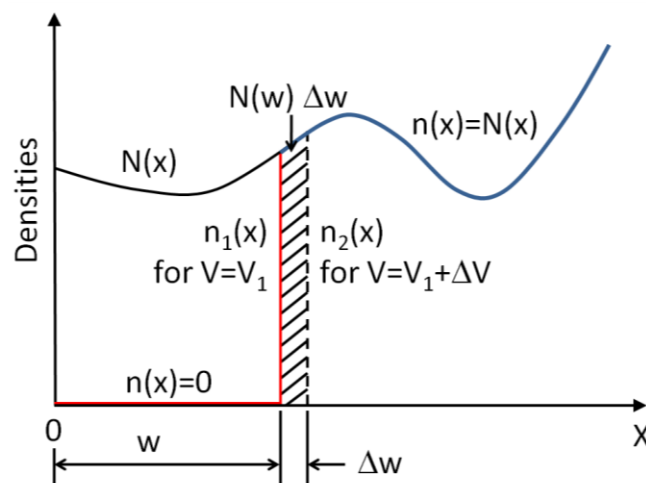


Figure G.1 Illustrating the usual assumption of a sharp-edged distribution of $n(x)$. The shaded ordinates represent the increment $\Delta n(x) = n_1(x) - n_2(x)$ [57].

$$\Delta E = \frac{\Delta Q}{\varepsilon_s}, \tag{G.3}$$

where ε_s is the dielectric permittivity of the semiconductor. The increment of voltage is given by

$$\Delta V = w\Delta E = \frac{QN(w)w\Delta w}{\varepsilon_s} \tag{G.4}$$

and the capacitance measured by external instruments is

$$C = \frac{\Delta Q}{\Delta V} = \frac{\varepsilon_s}{w}. \tag{G.5}$$

The lateral expression can be written as

$$w = \varepsilon_s C^{-1}. \tag{G.6}$$

Thus

$$\Delta w = -\varepsilon_s C^{-2} \Delta C, \tag{G.7}$$

and we can write the increment of voltage as

$$\Delta V = \frac{qN(w) \cdot (-\varepsilon_s C^{-2} \Delta C)(\varepsilon_s C^{-1})}{\varepsilon_s}, \tag{G.8}$$

from which we obtain the following conventional formulas:

$$N_{CV}(W_D) = -\frac{C^3}{q\varepsilon_s}\left(\frac{dC}{dV}\right)^{-1} \tag{G.9}$$

where

$$W_D = \frac{\varepsilon_s}{C}. \tag{G.10}$$

In semiconductors with large variations of the doping concentration and especially in semiconductors with quantum confinement, the CV-concentration N_{CV} does not have a direct physical meaning [72]. However, the CV-concentration corresponds approximately to the free carrier concentration

$$N_{CV} \cong n(W_D). \tag{G.11}$$

Nevertheless, Kroemer et al. [73] showed that charge conservation is fulfilled for CV-profiles, that is

$$\int_{-\infty}^{\infty} N_{CV}(W_D) dW_D = \int_{-\infty}^{\infty} n(w)\, dw. \tag{G.12}$$

The right-hand scale of Equation G.12 represents the 2-DEG carrier density of an electron system. Thus, the 2-DEG carrier density of doped quantum well structure, selectively doped hetero-structures, and similar structures can be precisely measured by CV-profiling technique.

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