Abstract of Dissertation:

Design of Multi-GHz Data Converter Components

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In the last few decades the communication bandwidth has evolved with an enormous speed and the requirement for high-speed data converters is directly dictated by that. In RF systems, the analog-digital interface is pushed towards the antenna, because the complex signal processing can be handled more efficiently in the digital domain. On the other hand it makes the design of these high-speed data converters more and more difficult.

In this dissertation the main design challenges in the field of multi-GHz data converters are discussed. The main research work is broadly divided into two parts. In the first part the different design techniques of multi-GHz analog to digital converters (ADC) are presented. In the other section the design of multi-GHz current steering digital to analog converters (DACs) have been discussed.

In the context of ADC design the front-end track and hold (THA) comes as the most critical part. This is because of the fact that any error introduced in this block cannot be compensated by the signal post-processing. In this research work an attempt has been made to improve the performance of the THA so that the stringent accuracy requirements of the quantization process can be relaxed. This is accomplished by enhancing the input range of the THA. Two different THAs are designed and measured successfully. In both the THAs, different techniques are used to enhance the input range up to 2Vpp differential at the sampling rate of 10GHz. According to the authors knowledge these THAs are the only published THAs which can work with 2Vpp input signal and achieve an accuracy of more than 6.5-bit at a sampling rate of 10GHz. A new double sampled technique is proposed for the open loop THA architectures which can be instrumental to double the sampling speed of the THA with a little overhead of power dissipation compared to conventional open loop THAs. As a design example a 20GHz 6-bit comparator has been designed and measured successfully.

An 8-bit segmented current steering DAC has already been designed. As a tread-off between the accuracy and power consumption 50% segmentation is used. The MSB sub-DAC is implemented with conventional unary weighted DAC architecture. In the context of high-speed DAC design the binary to thermometer decoder comes as the design bottleneck in terms of speed and power. In this unary sub-DAC design a novel thermometer decoder is proposed which is mainly based on an HBT ROM structure. In simulation the 8-bit DAC shows an accuracy of 7.83 effective number of bits (ENOB) with 9GHz of single tone input sinusoidal and a sampling rate of 20GHz. The 4-bit LSB sub-DAC is already implemented with a weighted resistive ladder network. A novel binary weighted resistive ladder network is proposed. The 4-bit DAC is found to be functional up to 30GHz of sampling rate which shows the second best performance in terms of sampling speed for published SiGe high-speed DACs.