

Abstract

The exponential increase of the integration density of integrated circuits in recent years has made it possible to manufacture information processing systems on a single chip (SoC, System-on-Chip). However, the trend to integrate millions of transistors has also led to higher requirements of electric power. The need for cooling as well as the relatively increasing weight and size of the batteries in embedded systems is a problem which is already a limiting constraint for portable and high performance systems.

There is also a problem on the development side: design methodologies for hardware synthesis are not yet on the same abstraction level as software design methodologies, where a paradigm shift happened with the introduction of object oriented programming. The common specification of hardware for synthesis on the register-transfer level often makes it necessary to transfer a higher level system description by hand what implies difficulties in the verification phase. Literature commonly refers to this as the "design-gap".

This work presents an approach to overcome the above problems by introducing a software framework which provides a design methodology across all abstraction levels from a high level specification of the system through architecture exploration up to the physical chip.

It has a high level of power optimization as a design goal which is achieved by three properties of the framework: Firstly, it uses commercially available, highly optimizing EDA tools as much as possible. Secondly, a module library was integrated into the framework which contains highly optimized digital signal processing modules. Thirdly, a quality measure is an integral part of the framework. The integrated measure allows a far better classification of the quality grade of the output concerning human hearing of the processing system than conventional signal-to-noise ratio based classification. This allows for an energy-saving quantization of the hardware operators.

The framework is evaluated using efficiency examinations for the embedded modules. Further, case studies implementing digital signal processing chains in real hardware are presented.