Abstract (englisch)

This thesis addresses implementations of the self-organizing map, an algorithm from the realm of artificial neural networks developed by Teuvo Kohonen. The algorithm is, just like its natural archetype, parallel in nature and thus well suited for parallel hardware implementation. The hardware option is useful in a range of applications dealing with huge amounts of data, real time requirements and a limited energy budget. An example with these requirements would be hyperspectral imaging of planetary surfaces on board of a satellite or drone. The research results regarding self-organizing maps in hardware are organized into several areas:

On the processing element level, usually a number of different hardware specific adaptations of the algorithm are introduced, aiming towards a more efficient implementation. The discretization of input and output data is one of the most important adaptations, allowing for exchanging expensive floating point operations for cheaper integer operations, resulting in an overall reduction of resource consumption. At the same time, the algorithms functionality is modified, too: primarily the precision of input and output data is reduced; secondary effects are a result of the internal modifications accumulating throughout the calculations. To be able to evaluate these effects, a new metric is developed which allows for a better comparability of different implementations. Using a number of different datasets, the new metric is used to evaluate a number of different modifications. As a result, a set of minimal requirements for hardware implementations of the self-organizing map could be found.

On the architectural level, an analysis discloses two independent degrees of parallelism which can be exploited independently. To be able to find a suitable hardware solution for a given task, a model for the estimation of the resource consumption of a hardware implementation (area, power, and latency) is developed on the basis of exemplary hardware implementations of the different architectures. Having acquired these values for a given task (for a given task an infinite number of hardware implementations can be evaluated), a method to find the best solution(s) has to be found. One way is to calculate the so called Pareto set, which consists of a number of points in the design space, which are not dominated by other points, meaning that no other implementation is better in all the characteristics (area, power, and latency). As this set can again be very large, a method for evaluating the points, the so called resource efficiency is introduced. Thus, an optimal implementation can be found for every task.

To be able to test parts of the design and to create a prototypical implementation, two tools are introduced which allow for comfortable analysis of digital circuits in a semi-automatic environment. The first tool called HiLDE is a bridge between a digital, FPGA-based hardware implementation and a simulation environment such as Matlab/Simulink or ModelSim. It allows for the verification of the correctness of the implemented circuit while disregarding timing issues such as the critical path. On behalf

of these, another tool called HiLDEGART is introduced to be able to observe and parameterize a hardware implementation running in its target environment in real time. As a number of hardware blocks have to be created for both of the tools, a versatile and powerful library for automatic code generation in VHDL called vMAGIC was created.

These tools are used to create a prototypical implementation of the self-organizing map hardware in FPGA technology, allowing for a reliable evaluation of the architecture. The resulting data is compared with software based implementations running on several processor architectures. This comparison shows that even with a comparably small and non-optimal implementation, a hardware solution is faster even in comparison to current multi-core processor architectures. An extrapolation for future technologies shows that on the long run hardware is a feasible solution for high performance, low energy calculation of self-organizing maps.