Abstract

We provide in this thesis our contribution in the area of reconfigurable system synthesis. We consider reconfigurable systems constructed from one or more general purpose processors (GPP) and a set of reconfigurable processing units (RPU). Given an application to be implemented on this architecture, a hardware/software partitioning step is used to differentiate between the part of the application to be executed on the hardware and the part to be executed in software. The synthesis of a reconfigurable system consists of the hardware/software partitioning process as well as the implementation of the software part on the GPP and the hardware part on the RPU. The part to be implemented on the RPU is provided as a dataflow graph (DFG). This thesis deals with the part of the application to be implemented on the RPUs. The RPUs targeted are field programmable gate arrays (FPGAs). Because the DFGs to be implemented in the FPGAs are usually too large to fit in a single FPGA, they must be partitioned in to blocks. These blocks are then successively downloaded in to the FPGA to compute the desired function. If the FPGA can not be partially reconfigured, then the blocks are used to configure the entire device. In this case, the partitioning process is called **temporal partitioning** otherwise it is a **temporal placement**. Our contribution consists of the development of various algorithms to solve the temporal partitioning and the temporal placement problems.