

The thesis combines interface synthesis techniques with reconfigurable computing concepts to create an interface adapter module called Interface Block (IFB), which affords the deterministic reconfiguration of tasks at runtime. Furthermore, it presents an integrated design flow that has been implemented by an EDA tool which supports the modeling and automated synthesis of an IFB. With the help of a worst-case-execution-time analysis and a succeeding schedulability analysis we can prove that an IFB performs a real-time conform protocol conversion. Finally, the thesis presents two optimization approaches for the minimization of the latency and the required chip area of the IFB circuit.