The concept of reconfigurable hardware provides a good trade-off between the flexibility of general purpose processors and the performance of application specific integrated circuits (ASICs). A reconfigurable architecture such as an FPGA (Field Programmable Gate Array) consists of an array of configurable processing elements that are connected by a programmable communication infrastructure. By interconnecting the processing elements, complex systems can be implemented on a single device. Partially reconfigurable architectures allow for adapting a part of the processing elements, while the other parts of the system continue to operate unaffectedly. Thus, system components can be realized that can be exchanged at run-time.

In this work the performance of various system approaches for partially reconfigurable hardware is analyzed. In order to evaluate the system approaches and the corresponding placement methods, the simulation framework for analyzing reconfigurable architectures (SARA) is introduced.

Since current FPGAs consist of several types of processing elements (e.g. logic cells, memory blocks), the placement of dynamic system components is subject to constraints imposed by the heterogeneity of the architecture. This work discusses, whether existing placement algorithms can be adapted to heterogeneous architectures. Moreover, suitable methods for resource allocation of heterogeneous reconfigurable architectures are introduced. A new placement approach is presented, which is able to deal with the constraints imposed by the heterogeneity of reconfigurable architectures.