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Identification and Simulation of Critical Interconnect Paths with Respect to Transient Noise on PCB-Level

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Abstract

In this thesis an efficient approach to identify and evaluate the critical transient noise paths on printed circuit board level is presented. This approach is based on the determination of the flow of the noise power induced into a system of interconnects and distributed to any sensitive integrated circuit device ports. The noise paths may result from all coupling mechanisms between the transmission structures. Moreover, the noise paths are extracted considering the entire printed circuit board.

Dominant and critical signal traces transferring significant noise from a specified noise source to digital device I/O ports can be determined in the frequency domain using advanced and efficient k shortest path algorithms. These are then combine with the signal flow graph circuit matrix to compute the transfer function of the individual weighted signal paths. The noise paths are evaluated in terms of the transmission coefficients over the frequency range of interest. The superimposition of several dominant signal paths delivers a good approximation to the total system response.

The associated coupling waveform can be computed by analyzing the whole dominant signal paths, including device drivers and receivers, in the time domain. This can be performed using a hybrid analysis like the harmonic balance technique or the S-parameter analysis. Depending on the component noise margin the path can be identified as critical or not. The approach proposed is able to predict the interconnects responsible for majority of signal degradations at the chip ports. Based on this information protection measure may be introduced to improve the printed circuit board design and develop more reliable circuits.

Contents

Abbreviations and Symbols

Abbreviations

2D, 2.5D, 3D	Two, two and a half, three dimensional
ASCII	American Standard Code for Information Interchange
BLT	Baum, Liu and Tesche
BTL	Bipolar Transistor
CAD	Computer-Aided-Design
CDM	Charged Device Model
CMOS	Complementary Metal Oxyd Semi-conductor
CST	Computer Simulation Technologies
CPU	Central Processor Unit
DC	Direct Current
DFT	Discrete Fourier Transform
EFT	Electrical Fast Transients
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FR4	Flame Retardant type 4
FFT	Fast Fourier Transform
GND	Ground
HB	Harmonic Balance
HBM	Human Body Model
HFSS	High Frequency Structure Simulation
HSPICE	Circuit Simulator of Synopsys
IBIS	IO Buffer Information Specification

IC	Integrated Circuit
IDFT	Inverse Discrete Fourier Transform
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input-Output Ports
LU	Lower-Upper decomposition of a matrix
LVTTL	Low Voltage Transistor Transistor Level
LVCMOS	Low Voltage CMOS
MATLAB	Matrix Laboratory
MM	Machine Model
MNA	Modified Nodal Analysis
MoM	Method of Moments
MOS	Metal Oxyd Semi-conductor
MTL	Multiconductor Transmission Lines
NC	Not Connect pin
PCB	Printed Circuit Board
RFI	Radio Frequency Interference
SFG	Signal Flow Graph
SI	Signal Integrity
SPICE	Simulation Program with Integrated Circuit Emphasis
STL	Standard Template Library
TEM	Transverse Electromagnetic Waves
TSTR	Transmission Structure
TTL	Transistor Transistor Logic

List of Symbols

$\mathbf{0}$	zero matrix
$\mathbb{1}$, $\mathbb{1}_{m-n}$	unitary matrices
A_n	Fourier coefficient of a periodic signal
$\boldsymbol{a}$	vector of input waves
a_i	input wave at port i
B_n	Fourier coefficient of a periodic signal
$\mathcal{B}(s', u')$	path bundle of branch (s', u')

$branchPath(u', v')$	path in G' representing branch (u', v') in $\mathcal{T}_i$
$\mathcal{B}_i$	block of vertices with index i
$block(u') = i$	position of vertex u' on the shortest path tree $\mathcal{X}$
$\boldsymbol{b}$	output wave vector
b_i	output wave at port i
$\boldsymbol{C}$	per unit length capacitance matrix
C	capacitance
C_{-comp}	*Die* capacitance
C_{-pkg}	package capacitance
C_j, C_{j0}	depletion capacitance of a diode
C_D	diffusion capacitance of a diode
$c(e')$	cost of edge e'
$c(u', v')$	cost of edge (u', v')
$\mathcal{C}(u')$	equivalence class associated to the node u'
$\mathcal{C}(u', t_{\mathcal{P}})$	equivalence class associated to the branch $(u', t_{\mathcal{P}})$
$\mathcal{C}(u', v')$	equivalence class associated to the branch (u', v')
$\boldsymbol{c}$	vector of independent generators
$\boldsymbol{c}_i$	subvector of independent generators for a multiport
$\mathbb{C}$	set of complex numbers
C_c	storage capacitor
C_d	DC blocking capacitor
C_s	charging capacitor
c_n	complex Fourier coefficient of a periodic signal
$d(u', v')$	distance between the vertices u' and v'
$d(v')$	distance from a source vertex s' to the vertex v'
dz	small section of a line
$d\omega$	differential frequency
det	determinant
$det_{\mathcal{P}}$	cofactor of a path $\mathcal{P}$
det_{SFG}	determinant of a signal flow graph
E'	set of edges in G'
E'_{cut}	edges crossing the cut $(\mathcal{V}_x, \mathcal{V}_y)$
E'_i	set of edges in $E' \backslash e'_i$

e'_i	edge with index i
$\mathfrak{F}$	diagonal matrix defined from the inverse of the square root of the normalization impedances
$\boldsymbol{G}$	per unit length conductance matrix
G	conductance
G'	graph
$H(v', u')$	transfer function relating the nodes u' and v'
$H_{\mathcal{P}_n}$	direct path gain associated to the path $\mathcal{P}_n$
$H_{v'}$	total transfer function at a node v' for multiple sources
$H_{\mathcal{P}}$	direct path gain associated to $\mathcal{P}$
$\mathfrak{G}$	diagonal matrix of the reference impedances
H', H'_i	subgraph of a circuit graph G'
I_s	saturation current of a diode
Im	imaginary part of a complex number
$\boldsymbol{I}_e$	current vector of external nodes
$\boldsymbol{I}_i$	current vector of internal nodes
I_p	current at the port p in a linear network
I'_p	current at the port p in a nonlinear network
$I_{p,q}$	current at the port p in a linear network at the q-th harmonic of the signal frequency
$I'_{p,q}$	current at the port p of nonlinear network at the q-th harmonic of the signal frequency
$\boldsymbol{I}$	vector of currents
$\boldsymbol{J}$	Jacobian matrix
κ	Boltzmann's constant
$\boldsymbol{L}$	per unit length inductance matrix
L	inductance
L_{-pkg}	package inductance
$\mathcal{L}(u', v')$	first edge in path (u', v')
l_i, l_{ij}	length of a line
$minblock(v')$	smallest index i for which $path(v', y)$ traverses $\mathcal{B}_i$
$\boldsymbol{P}$	connectivity matrix
$Path_{s't'}$	all paths connecting s' and t'
$\mathcal{P}_{u',v'}$	a path relating the nodes u' and v'

$\mathcal{P}_i$	dominant path of order i
P	total power available in a multiport
$path(s', t')$	shortest path connecting the vertices s' and t'
$\mathcal{P}$	simple directed Path
$\mathcal{P}(0)$	empty set of paths
$\mathcal{P}(k)$	set of first k shortest paths
$prefixPath(u')$	prefix path consisting of all the branches from s' to u'
q_e	electronic charge
$\boldsymbol{R}$	per unit length resistance matrix
$\mathcal{R}_i$	set of candidate paths connecting s' to t' at iteration i
Re	real part of a complex number
R	resistance
R_{-pkg}	package resistance
R_d	limiting resistor
R_c	charging resistor
R_m	impedance matching resistor
R_s	bulk resistance of a diode
R_{sh}	pulse duration shaping resistor
$\boldsymbol{S}, \boldsymbol{S}_i$	scattering matrix and submatrix
$s_{u'v'}(\mathcal{P}_n)$	scattering coefficient associated to the path $\mathcal{P}_n$
$s_{u',v'}$	scattering coefficient of the path or edge (u', v')
$\boldsymbol{T}$	transfer scattering matrix
$\mathcal{T}_i$	branching structure of first i shortest paths
$t_{\mathcal{P}}$	leaf node representing the path $\mathcal{P}$ in the branching structure
T_K	absolute temperature
T_{ij}	path transmittance for a path (i, j)
T_h	constant threshold value
T	period of a signal
$\boldsymbol{V}_e$	voltage vector of external nodes
$\boldsymbol{V}_i$	voltage vector of internal nodes
V_{cc}	common-collector voltage
V_T	thermal voltage

V'	set of vertices in G'
$\mathcal{V}_x$	set of vertices containing start vertex x
$\mathcal{V}_y$	set of vertices containing target vertex y
V_s	voltage source
$v(t)$	time voltage
V_p	voltage at the port p in a linear network
$V_{p,q}$	voltage at the port p and q-th harmonic of the periodic signal
$V_{t'}$	voltage at target load
$\boldsymbol{V}$	vector of voltages
w_{ik}	weight of edge (i, k)
$\mathcal{X}_i$	shortest path tree rooted at x and without edge e'_i
x_i	signal variable at node i
$\mathcal{X}$	shortest path tree with root start vertex x
$\boldsymbol{Y}$	admittance matrix
$\mathcal{Y}$	shortest path tree with root target vertex y
$\boldsymbol{Y}_L$	characteristic admittance of a line system
Z_N, Z_{Ni}	reference impedance of a port
Z_0	characteristic impedance of a line
$\boldsymbol{Z}$	impedance matrix
Z_L	load impedance of a line
α	attenuation constant
β	phase constant
$\boldsymbol{\Gamma}$	wave matrix of a multiconductor transmission lines
Γr	reflection coefficient
γ	propagation constant
$\Delta\mathcal{P}$	cofactor of the path $\mathcal{P}$
Δt	time sampling period
Δ	determinant of the circuit matrix
ε_r	relative permittivity constant
$\mathcal{E}$	error function
η	grading coefficient of a diode
$\boldsymbol{\Phi}$	chain matrix of a parallel coupled line system

ϕ	built-in potential of a diode
τ_D	transient time of a diode
ω	angular frequency
ω_0	fundamental frequency of a harmonic signal
$\omega_1, \omega_2, ...$	fundamental frequencies of a multitone excitation signal

Chapter 1

Introduction

1.1 Statement of The Problem

The recent trend in the electronic industry towards circuits of higher complexity with many conductor traces per unit area, faster signal transition rate, operating frequency and lower power consumption has made the signal integrity analysis (SI) of electronic systems with focus on these trends a challenging task. Many of these signal integrity problems derive from electromagnetic phenomena and hence are relate to the electromagnetic interference (EMI) and the electromagnetic compatibility (EMC). The performance of electronic systems is mainly affected by the design of the printed circuit board (PCB), the design of the integrated circuit (IC) and its package, as well as the characteristics of the signals for which the board is designed [1].

The continuous miniaturization combined with an increased integration density at the PCB level in today's PCBs have caused significant amount of crosstalk, reflections, and internal radiation. These three kinds of signal integrity problems have become critical issues in the design of modern electronic systems. PCB traces may act as unwanted emitting and receiving antennas, which cause a strong coupling between neighbouring structures [2]. In addition to this, technology trends at the chip level towards higher speed and higher density have pushed the package performance of digital devices to its limits. The space between integrated circuit pins continues to decrease leading to an increase of parasitic couplings. The clock rate of present digital systems is approaching several gigahertz. As the signal rise time decreases, the significant frequency content of digital signals extends up to some gigahertz. These issues lead to major ringing and crosstalk. On the other hand modern digital integrated circuits are characterized by low supply and input voltages and the corresponding noise margin is decreasing. Therefore the sensitivity of the digital components to EM perturbations increases dramatically.

In addition to the technology aspect, the performance of electronic systems is affected by the presence of transient impulses [3, 4, 5]. The effects caused by these transients are superimposed to the high frequency parasitic behaviour of the layout arrangement. Conducted transients are the typical kind of transients that may affect an electronic system. The transients' waveform contains high-frequency components ranging up to

several gigahertz. This makes their coupling with adjacent signal traces very easy. Since most digital devices are specified and designed to generate and respond to signals with fast rise times, comparable to electrostatic discharge (ESD) and electrical fast transients events (EFT), vulnerability towards these events should be expected. Fast transient impulses may be devided up into internal and external transient impulses. Internal transients are generated from the microprocessor, and couple to the rest of the system in question. External transients are generated from other systems, e.g. multiple PCBs, or may be of natural sources, e.g. ESD.

External noise impulses can be captured by cables connected to the peripheral equipment and propagate by conduction, inductive and capacitive coupling and is subject to distortion mechanisms on the board itself, like reflection. Typically the noise is distributed within the circuitry by a variety of interconnect paths to finally arrive at the individual sensitive digital integrated circuit component. The propagation impulses at the integrated circuit devices are superimposed on the nominal signal at their pins. The level of the incurred failure depends on the sensitivity of the integrated circuit devices. The induced impulses may cause errors in the operation of the IC or the overall system such as program reset, a logic state change or even data corruption in the memory. Moreover, in many situations, damage to the device is to be expected.

High frequency parasitics in conjunction with very fast transient signals lead to the perturbation or even destruction of sensitive IC. Therefore, an analysis of printed circuit boards with focus on these transients is required so as to provide sufficient information on the functionality and the reliability of the circuitry, and thus, to avoid poor printed circuit board design at early stage of the implementation.

1.2 State of The Art

The SI analysis of printed circuit boards with a focus on the propagation characteristics of transient interferences, namely conducting type, is required for providing sufficient information on functionality and reliability of the circuitry. Different protection measures towards transient impulses, depending on the application [6, 7, 8], are proposed. The susceptibility analysis of integrated circuits is usually carried out for several types of transients using numerical and measurement methods [4, 9, 10, 11, 5, 12, 13].

Numerical analysis methods which deal with the propagation of high-frequency transients within a circuit are based on the combination of the global EM field approach and the transmission line theory. In literature many numerical methods, or hybrid approaches, are combined for the simulation of specific problems [14, 15]. The distribution of noise including possible parasitic couplings can directly be determined by simulating the interconnect structures of the whole system. To achieve efficient computation with less computer memory storage, the system can be partitioned into subsystems in such a way that significant electrical interactions occur only through common physical ports [14, 16]. Derived parasitic models of the structures are used within a circuit simulator to perform a signal integrity analysis.

Recent investigations in the immunity of electronic systems towards fast conducted transients were made by using measurement procedures [13, 11, 10]. Tests regarding the effects of various types of noise impulses on the pins of digital devices are carried out [10]. Many articles present measurement concepts for the coupling noise impulses at specific IC pins using standard methods [17]. The impact of noise impulses on the protection elements of a variety of logic families is also investigated in order to select transient suppression components in regard to the optimal operating conditions [18]. Noise generators producing fast transients are also modeled in several contributions [19, 20, 21].

Typical circuit simulators are based on a nodal analysis. Microwave linear circuits are usually analyzed in the frequency domain. Transmission structures are modeled by lumped circuit elements or appropriate admittance matrices. For large circuits the nodal analysis leads to a very large matrix that renders the analysis process inefficient from the computation time and memory resources point of view. Alternatively, the multiport connection method which solves circuits iteratively can be used.

Nonlinear circuits containing IC drivers and receivers are usually analyzed in time domain. Conventional time domain analyzes are based on numerical integration techniques applied to the set of difference equations describing the system. Modern approaches, like the Harmonic Balance (HB) approach, which combines frequency and time domain techniques, are more efficient. Therefore, the use in analyzing signal integrity of electronic systems becomes of great interest. In most computer-aided-design (CAD) tools circuit simulators and EM field solvers are implemented together [22, 23]. This allows for the results of field solvers to be linked to circuit solvers in order to perform a complete analysis of the circuit considering the parasitic behaviour of the interconnect structures.

The common property of most existing computer-aided-design tools for electronic circuit analysis is to determine the physical quantities at the device pins. In literature, the propagation of noise power between two specified components is always determined within a simple interconnect structure by computing the parasitic elements or the transmission coefficient relating the corresponding ports [24]. Critical structures and single transmission lines are mainly defined by their dimensions, especially the length.

The aim of this thesis is to develop a signal tracing algorithm for the identification and characterization of the critical interconnect paths with respect to conducted transient impulses considering the global system of interconnects on a PCB. The critical or dominant propagation paths cause significant transfer of noise power from a noise source to a specific IC I/O pin. Because the PCB design becomes an interesting impact factor for the immunity of IC, the identification of the whole propagation path at PCB-level is of more importance. This methodology allows the extraction of the critical propagation paths by taking into account all coupling mechanisms which relate a given noise source to a target IC pin. Such functionality is not yet implemented in any circuit simulator. Moreover, there is no scientific literature at all published which addresses the determination of the whole signal propagation paths. The knowledge of these paths and their associated coupling noise can be used to optimize the layout's electrical and physical characteristics in order to keep the coupling noise at an acceptable level and thus meeting the requested specifications of the circuitry.

Chapter 2

Susceptibility and Immunity of Electronic Devices

This chapter presents the elements required for the description and analysis of an electromagnetic interference problem on printed circuit boards. Propagation, or coupling mechanisms for conducted fast transient interferences are described. Some examples of such transients are provided. The susceptibility of digital devices against electrostatic discharges is discussed.

2.1 EM Disturbances

Electromagnetic Interference is defined as the influence of unwanted signals on electronic devices and systems, making the operation of the device difficult or impossible. The noise signal may come from other electrical circuits or from a portion of the circuit itself. The electromagnetic energy is transmitted from one electronic device to another via radiation paths, conducting paths, or a combination of both. A system that does not become affected by its environment is said to be EM-compatible. The Electromagnetic Compatibility is defined as the capability of electrical and electronic systems, equipment, and devices to operate in their intended electromagnetic environment within a defined margin of safety, and at design levels or performance, without suffering or causing unacceptable degradation or interrupts as a result of electromagnetic interference. The immunity of an electronic system or device is its ability to function satisfactorily in its environment while maintaining a predefined performance level [25].

As high technology advances, so do the problems from electromagnetic interferences. EMI issues are increasingly problematic when designing systems. Systems are not performing to specifications to overcome all EMI problems, but satisfy certain conditions to avoid some particular EMI problems.

2.2 Electromagnetic Interference Model

A simple model to describe an interference problem consists of a noise source, a victim circuit, and a coupling path. The source of electromagnetic energy needs a coupling path to facilitate the transmission of the disturbance signal to the victim circuit. If one of these three elements is removed from the system, the disturbance problem is solved. The coupling path between source and victim does not have to be a conducting medium such as an electric conductor, but can also be a free space or any other material as well. In general the coupling path is a combination of conduction and radiation. A useful technique that can be used to minimize EMI-problems is to keep the disturbance signals from the source and across the coupling path below a certain level. Figure 2.2.1 illustrates the relationship between these three elements.

Figure 2.2.1: Elements of an electromagnetic interference model

2.2.1 Electromagnetic Interference Sources

The source of interference is the active element producing the original waveform of the disturbance. There exist two types of EMI sources depending on their creation. Artificial sources of EMI include microprocessors, microcontrollers, transmitters, transient power components, such as electromechanical relays, and switching power supplies. For instance within a microcontroller system, the digital clock circuitry represents a generator of wideband noise. Natural sources on the other hand include electrostatic discharges and lightning.

EMI sources can be also grouped into internal and external sources. Internal EMI sources are the result of signal degradation along a transmission path, including parasitic coupling between subcircuit elements, or devices, of the same system. More specifically, the problems are signal losses and reflections along the path, and crosstalk between adjacent signal traces. An example of such sources of disturbances are the noise impulses generated from a microprocessor and which may disturb other devices within the same equipment [26, 27, 28].

External sources are applied to the system from the outside. Examples of such external influences are electrostatic discharge and radio frequency interference (RFI). These can directly be coupled to the circuit components or indirectly via an interface to the outside of the circuit like I/O lines. The coupling waves are then transferred into the inside of the system.

2.2.2 Coupling Mechanisms

The EMI propagation path is the medium that carries the electromagnetic interference energy from the interference source to the victim circuit. The EM energy is propagating by conduction, radiation, or a combination of both. An obvious way noise can be conducted into a system is through interconnects. An example of this type of coupling is found when the noise enters a system through the power supply leads. The EM radiation does not however need a conducting medium. The radiated fields propagate in a free space and cause EM interaction with the system components.

There are four coupling paths for transmitting electromagnetic disturbances from an interference source to a victim circuit. The first belong to the radiated type, such as capacitive, inductive, and field coupling, and the last is of conductive nature like galvanic coupling.

2.2.2.1 Capacitive Coupling Paths

Capacitive coupling is caused by an electrical field. Two or more electronic circuits or subcircuits are coupled through their radiated electrical fields. The signal in the victim circuit is influenced by fast voltage transition of the interference signal by way of an interfering coupling parasitic capacitance. The influenced current can be modeled as a current source in the victim circuit according to

$$I = C \frac{dV}{dt},$$

where C is the parasitic capacitance relating both circuits.

For two signal traces with different electrical potential the value of the parasitic capacitance is depending on the ratio of their lengths and the distance between them. The coupling or parasitic capacitance leads not only to delay, but also causes potential logic malfunctions. This is a problem for designs with high clock frequencies, low supply voltages, and usage of dynamic logic with low noise margin.

2.2.2.2 Inductive Coupling Paths

Inductive coupling refers to the influence of a magnetic alternating field generated by the interference current on the victim circuit signal. By changing the flux an interference voltage, due to fast current transients, is inducted in the victim circuit. The inducted parasitic voltage is modeled as a voltage source in the victim circuit. For simple case where two conductors are inductively coupled the inducted voltage from the active conductor on the passive one is defined as

$$V = L \frac{dI}{dt},$$

where, L is the mutual inductance between the two conductors.

Inductive coupling can be reduced by increasing the space between the conductors, decreasing the length of parallel conductors, and using orthogonal arrangement during the placement.

2.2.2.3 Crosstalk

The combination of capacitive and inductive couplings simultaneously is named Crosstalk. Crosstalk occurs if the coupling path between parallel traces is very small. Consequently, the traces are coupled through the electric and the magnetic fields. The close coupling at the line start is called near-end crosstalk and the remote coupling at the line end is called far-end crosstalk. In general crosstalk noise modeling consists of determining of near- and far-end voltages, or currents at interconnect extremities.

The interconnect factors influencing crosstalk effect are those influencing capacitive and inductive paths, i.e. dimensions of the wires and distances separating them [29, 30, 14]. A crosstalk pulse generated on a victim line is depending also on the frequency of the signal and the nature of its transitions at the aggressor line. The slew rate of the transition signal depends on the frequency of signal. The current flow between two coupling wires increases as this slew rate increases. This causes the charge increase or decrease at the victim line.

Another effect which is usually implicitly analyzed when studying crosstalk are the reflections. Reflections, related to line terminations, result from impedance branches, which are caused by mismatching [31, 14]. On a printed circuit board, if a line is not matched, reflections occur and couple to the information signal on other signal lines. Thus, leading to undesirable effects that influence the nominal signals. Terminations of signal lines help to reduce these undesirable effects. A termination not only reduces signal reflection by matching the impedance of the coupling path, but can also slow down the fast rising and falling edge of the signals.

2.2.2.4 Galvanic Coupling Paths

A further coupling mechanism is the impedance coupling or galvanic coupling. It is the dominating coupling mechanism for low frequencies and occurs if common impedances are shared from two or more electronic circuits. In this case, a current of the interfering circuit flows through an impedance belonging to the agressor and the victim circuit. For instance, two circuits are sharing the conductor carrying the supply voltage and the conductor carrying the return path to ground. If one circuit creates a sudden demand in current, the other circuit's voltage supply will drop due to the common impedance both circuits share between the supply lines and the source impedance. This coupling effect can be reduced by decreasing the common impedance.

2.2.2.5 Radiation

Radiation or electromagnetic wave coupling is produced by the antenna effect of spatially extended circuits. The causes of this kind of interference are any sources which emit electromagnetic waves. These include all kinds of transmission systems, as well as lightning, etc.

Coupling can occur with radiated electric and magnetic fields which are common to all electrical circuits. Whenever current changes, electromagnetic waves are generated. These

waves can couple into the interface cables which provide a conductive path into the circuitry or they may be directly coupled onto the printed circuit wiring when the assembly is not shielded. When the amplitude of the radiated fields is sufficient, induced voltages and demodulated carriers can affect the operation of a device. The coupling noise is depending on the dimensions of the trace and the frequency of the applied signal [32, 33].

2.2.3 Victim Devices

All electronic circuits and devices are receptive to EMI transmissions. The coupling into a circuit can be done through connected cables or radiation. For a PCB with dimensions smaller than the interference wavelength, the interference collected by direct radio transmission is negligible compared with that transmitted by conduction [34]. The noise energy is transferred to devices susceptible to disruption. Due to their lower operating levels of voltages modern digital circuits are more sensitive to transient interferences [6].

2.3 Fast Transient Perturbations

Examples of EMI sources are fast transient noise impulses. These can be divided into single and repetitive impulses. Such kind of sources causes electrical overstress and leads to integrated circuit failures. The result of an electrical overstress event can range from no damage or degradation of the IC up to catastrophic damage where the IC is permanently non-functional. Electrical overstress covers a broad spectrum of events, including electrostatic discharge, power-up/power-down transients, and excessive DC current/voltage levels. ESD and burst are typically the most common form of electrical overstress, and consequently they are the focus of this subsection [20].

2.3.1 Electrostatic Discharge

The problem of static electricity accumulation and subsequent discharges becomes more relevant for uncontrolled environments and the widespread application of equipment and systems in a wide range of industrial plants. For instance ESD may affect many components such as diodes, transistors, integrated circuit devices, metal-oxide-semiconductors (MOS), and film passive components, etc. Device failures do not always occur immediately, often, the component is only slightly weakened or its parametric properties altered, and therefore is less able to withstand subsequent ESD exposure and may constitute a reliability problem [20, 21].

In particular, there are three general types of ESD events: the human body model (HBM), the machine model (MM) and the charged device model (CDM). The HBM and MM correspond to discharge current between any two pins on an IC as a result of a human body discharging through a chip, and a metal discharging through a chip respectively. In the CDM, the ESD event does not originate from outside the IC device itself, but instead represents the discharge of an IC device to ground. The IC device is charged for example

by an external field. The discharge leads to a high voltage pulse that may affect the susceptible devices. The effects of the operator discharge may be a simple malfunction of the equipment or damage of the electronic components. The dominant effects can be attributed to the parameters of the discharge current (rise time, duration, etc.). The general equivalent electrical model of an ESD simulator is depicted in Figure 2.3.1(a).

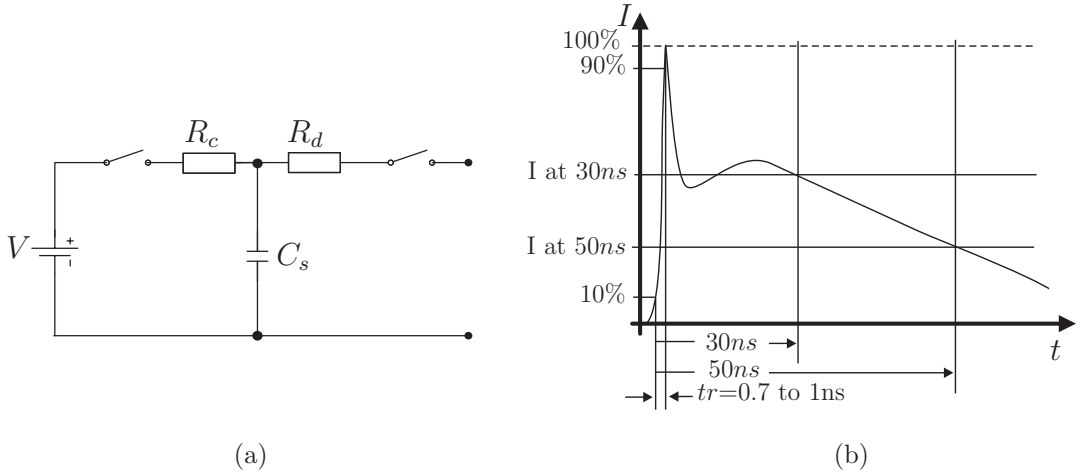


Figure 2.3.1: ESD discharge circuit: (a) electrical model, (b) typical waveform

First a source capacitor C_s is charged to a DC high voltage, then the high voltage power supply V is disconnected from the capacitor, and the capacitor is connected to the device under test through a limiting resistor R_d. The value of the test capacitor and the limiting resistor differ among the various test standards. The voltage source V defines the severity level of the test impulses.

The HBM uses a source capacitor of 100 pF and a discharge resistor of 1.5 $k\Omega$. The MM uses a source capacitor of 200 nF, but no discharge resistor. This causes the device under test to be subject to more voltage than the HBM testing. ESD test requirements are specified in the standard IEC61000-4-2. Typical values of the charging resistance R_c varies between 50 MΩ and 100 MΩ. The discharge resistance has a value of 330 Ω and the capacitance C_s has a value of 150 pF.

The form of an ESD impulse is represented in the right side of Figure 2.3.1(b). The waveform of the discharge current is characterized with an extremely short rise time of 0.7 to 1.0 ns and amplitudes of up to 45 A. Secondary effects caused by this edge steepness are high electrical and magnetic fields strengths.

The problem of protecting CMOS chips against ESD events has gained considerable importance for manufacturers and users. Protection circuits include ESD clamps configured to maintain the voltage at a power line to a value that is safe for the operating circuits, and that will also not interfere with the operating circuits under normal operating conditions [18].

2.3.2 Burst Impulses

Electrical fast transient noise impulses (EFT) are low-power high-voltage signals which occur as a result of bouncing contacts in switches and relays. The pulsed voltage arises several times and impulse packages, named Burst, are generated. These currents can couple and propagate over power and data lines and consequently lead to a disturbance or even destruction of attached devices or elements. IEC 61000-4-4 specifies the burst threat in both power and data lines [24].

The simplified circuit diagram of the burst generator is given in Figure 2.3.2. In this figure R_c is a charging resistor, C_s is an energy storage capacitor, R_s is a pulse duration shaping resistor, R_m is an impedance matching resistor, and C_d is a DC blocking capacitor. The values of the circuit elements C_s, R_s, R_m, and C_d differ among the various test standards. These are selected so that the generator delivers a fast transient under open circuit conditions and with a 50 Ω resistive load.

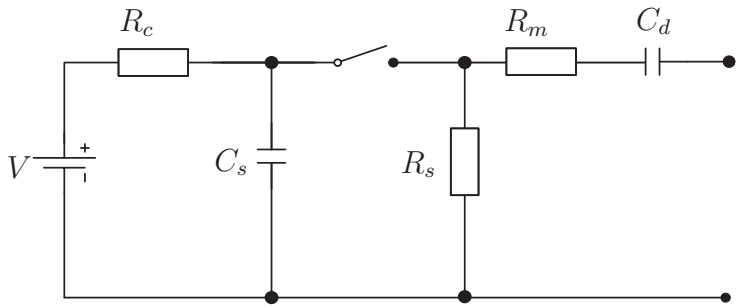


Figure 2.3.2: Circuit diagram of a burst generator according to IEC 61000-4-4

EFT impulses are described in terms of voltage across a 50 Ω load from a generator having a nominal dynamic source impedance of 50 Ω. The output occurs as a burst of high voltage spikes at repetition rates ranging from 2 kHz to 5 kHz. The burst duration is defined as 15 ms with bursts repeated every 300 ms. Each individual burst pulse is a double exponential waveform with a rise time of 5 ns and a total duration of 50 ns. EFT impulses are characterized by voltage amplitudes up to 5 kV and current amplitudes up to 30 A. The impulse waveform, the burst repetition rate, and a burst packet according to IEC 61000-4-4 are shown in Figure 2.3.3.

2.4 Electronic Device Sensitivity

The sensitivity of integrated circuits is defined by the noise margin, which represents the maximum value of noise that can be added to the input signal without affecting the signal state at the IC pin. In other words, that is, the difference between what the driver IC outputs as a valid logic voltage and what the receiver IC expects to see as a valid logic voltage. Any voltage that exceeds this noise margin causes a wrong output state.

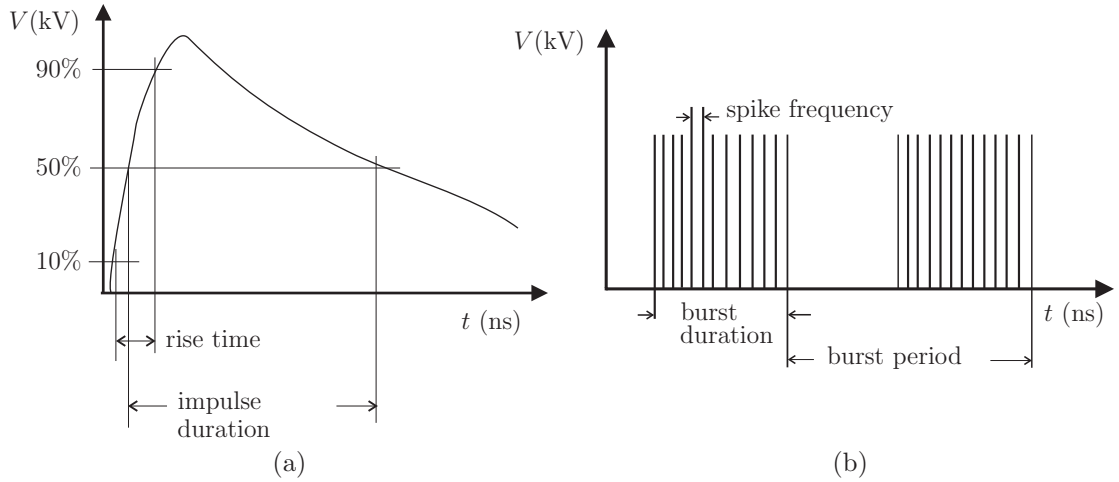


Figure 2.3.3: EFT impulse according to IEC 61000-4-4: (a) single impulse, (b) burst packet

There are two different types of noise margins, one for a logic high value and one for a logic low value. These are defined by

$$\begin{aligned} V_h &= V_{OH}\,[\text{driving device}] - V_{IH}\,[\text{receiving device}] \\ V_l &= V_{IL}\,[\text{receiving device}] - V_{OL}\,[\text{driving device}]\,, \end{aligned} \tag{2.4.1}$$

where V_h is the noise level immunity for the logic chip when the logic state is high, V_l is the noise level immunity for the logic chip when the logic state is low, V_{OH} is the minimum high output generated by the driving gate, V_{IH} is the minimum high input allowable for the driven gate, V_{OL} is the maximum low output generated by the driving gate, and V_{IL} is the maximum low input allowable for the driven gate.

In digital circuits, the most critical pins are that receiving significant EMI energy. These include reset, interrupt, and control line signals. The coupling energy to a victim digital device depends on the operating frequency of the circuit, the edge rate transition of digital components switching logic states, and transfer mechanisms. Table 2.4.1 shows typical noise margins for various logic families [35].

Logic	V_{OH} (V)	V_{IH} (V)	Noise Margin (mV)	V_{IL} (V)	V_{OL} (V)	Noise Margin (mV)
TTL [5volt]	2.4	2.0	400	0.8	0.5	300
BTL [5 volt]	2.1	1.62	480	1.47	1.1	370
CMOS [5 volt]	4.9	3.85	1050	1.35	0.1	1340
LVTTL [3volt]	2.4	2.0	400	0.8	0.4	400
LVCMOS [3 volt]	2.8	2.0	800	0.8	0.2	600
CMOS [2.5v]	2.0	1.7	300	0.7	0.4	300
CMOS [1.8v]	1.35	1.1	250	0.66	0.45	210

Table 2.4.1: Typical noise margins for various logic families

2.5 EMI Influence Parameters

The parameters influencing the EMI analysis of a problem are divided into two categories. The first category adresses the interference signal and the second one describes the technology of the printed circuit board and its devices. Interference signal parameters include frequency, amplitude, rise, and fall times. A noise source signal having a high voltage amplitude and small rise time contains high frequencies in its spectrum and thus can easily disturb the operation of a sensitive device.

Technology aspects on the other hand include the materials and the dimensions of the interconnect traces on the PCB as well as on the chip level. Small dimensions of signal traces on the PCB level lead to high crosstalk between them. On the chip level the technology aspect is associated with low noise margins and therefore high sensitivity. The parameters influencing the susceptibility of PCBs against parasitic interferences, at each stage of the EMI model, are given in Table 2.5.1.

Noise Source	PCB Interconnects	Digital IC Pin
Noise waveform	Technology issues	Technology issues
Fast rise and fall times High amplitudes	Complex structures Small dimensions High-density	Sensitive digital devices
High frequency components	Conduction Reflections Emission Crosstalk	Small noise margins

Table 2.5.1: The parameters influencing EMI models at PCB

Crosstalk on printed circuit boards in conjunction with fast transient signals represent the most signal integrity problems in modern systems. Fast transient impulses are mainly induced into a PCB by conduction through a single or multiple traces which distribute the high frequency noise energy into the entire system, and thus affecting the sensitive digital devices. Within this thesis a methodology for identifying and analyzing of coupling signal paths considering the whole system of interconnects in a PCB is developed. The coupling paths may include conductive, crosstalk and reflections paths.

Chapter 3

Elements of a Noise Propagation Path at the PCB-Level

This chapter presents the physical elements belonging to a noise propagation path at the PCB-level. Some assumptions regarding the layout are made to reduce the complexity of the analysis of the signal paths. A brief description of the modeling methodologies of both linear and nonlinear components of the signal paths is presented.

3.1 Assumptions to Reduction of Complexity

This section presents the partitioning scheme of complex PCB structures usually used for efficient numerical field simulation purposes. The multiport representation of the transmission structures, which is useful for circuit analysis techniques, is described.

3.1.1 Circuit Partitioning

A traditional approach for the analysis of the high frequency parasitic behaviour of printed circuit boards is based on the simulation of the electronic devices and the connecting signal traces it consists of. The parasitic behaviour is obtained by combining the circuit simulation and the electromagnetic field simulation. Thus, the parasitic effects between signal traces, including crosstalk and reflections, can be incorporated into the overall simulation of the system.

The entire PCB consisting of complex microstrip structures is usually characterized using a partitioning procedure under the assumption that the modes propagating along the coupled microstrip lines are assumed to be quasi-TEM. The resulting substructures can be analyzed separately and their models can be easily added to a CAD system. This procedure is hierarchical since the models for elementary blocks can be used to generate circuit models of other structures created by a combination of those elementary blocks. These blocks are consisting of coupled parallel transmission lines which are generally accompanied by discontinuities of different types. The parasitic behaviour is modeled

using the transmission line theory and the electromagnetic field theory. Transmission structures interconnecting circuit devices may be modeled as piecewise interconnected conductors characterized by the per unit length matrices $\boldsymbol{R}$, $\boldsymbol{L}$, $\boldsymbol{G}$, and $\boldsymbol{C}$, or directly by their frequency domain parameters. At high frequencies the discontinuities are better parameterized using numerical full wave field solvers, which cover all electromagnetic phenomena encountered in modern PCBs, e.g. transmission line effects, reflections, skin effects, proximity effects, and couplings. The behaviour of the entire system is obtained by the combination of all models of the structures that build it [36, 14, 16]. Figure 3.1.1 shows an example of an interconnect structure and its partitioning.

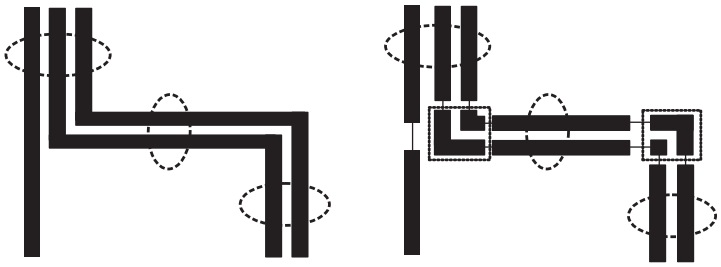


Figure 3.1.1: Principle of the decomposition of complex structures

The substructures are generated on the basis of their geometry. The structure in Figure 3.1.1 is divided into parallel lines and double bends discontinuities. This model shows that only the coupling between adjacent traces is considered. A circuit should be devided in places where coupling mechanism is at a minimum. Additional considerations such as the symmetry of interconnect structures and the wavelength need to be addressed. Using the adjacency aspect, only the coupling between neighboring traces is to be considered. This assumption may give a better approximation if the space between the transmission lines is constant. The symmetry may be used to decouple any structures that have some geometrical shape. This assumption may be a good approximation if the space between both partitions is many times bigger than the space between the transmission lines within a specified partition. Another assumption leads in neglecting the coupling between a signal trace and any other transmission line of small length.

Modeling a PCB as an assembly of predefined substructure elements which are connected to each others leads to efficient analysis. The number of these substructures is small and their characterization requires less computer resources rather than the original structures.

3.1.2 Multiport Representation

Circuit analysis techniques provide solution to the circuit equations in the frequency and time domains. The response of the circuit is computed in terms of the device parameters. At high frequencies electrical networks consist of lumped elements and distributed elements. Distributed elements model the transmission lines and high frequency structures present in the circuits. These are represented by multiports, characterized by some kind of

matrices. Multiports can be characterized in terms of its terminal currents and voltages. The impedance $\boldsymbol{Z}$ and the admittance $\boldsymbol{Y}$ of a multiport are defined by the equations

$$\boldsymbol{V} = \boldsymbol{Z}\,\boldsymbol{I} \tag{3.1.1}$$

$$\boldsymbol{I} = \boldsymbol{Y}\,\boldsymbol{V}, \tag{3.1.2}$$

where $\boldsymbol{I}$ and $\boldsymbol{V}$ are the vectors of terminal currents and voltages of the multiport respectively. For a multiport component with N ports the impedance and admittance matrices have the size $N \times N$. For reciprocal networks these matrices are symmetric. In addition, if the network is lossless, then the elements of $\boldsymbol{Z}$ and $\boldsymbol{Y}$ are pure imaginary.

A much more convenient form for the description of microwave circuits uses normalized wave variables and scattering matrix. It is the preferred description of microwave n-ports which uses the transfer of the power between the ports of a microwave structure by measuring of the incident and reflected waves a_i and b_i. The reason is that for some structures the voltage and current may not be well defined, or even defined at all. The specification of voltage and current in a distributed circuit requires a specification of the exact location, and these quantities vary with location in the circuit. The determination of the individual parameters of voltage and current equation sets requires short or open circuit loads, which are sensitive to the precise location [37, 31].

The scattering parameters relate the power variables a_i and b_i at the ports of a microwave multiport. The incident and reflected power waves at the i-th port of the network are defined in terms of the terminal voltage V_i, the terminal current I_i, and the reference impedance Z_{Ni}, as follows:

$$\begin{cases} a_i = \dfrac{1}{2\sqrt{\mathrm{Re}(Z_{Ni})}}(V_i + Z_{Ni} I_i) \\ b_i = \dfrac{1}{2\sqrt{\mathrm{Re}(Z_{Ni})}}(V_i - Z_{Ni}^{*} I_i) \end{cases}, \tag{3.1.3}$$

where the superscript $(^*)$ denotes the complex conjugate.

The scattering matrix for a multiport network with n-ports is defined by the equation

$$\boldsymbol{b} = \boldsymbol{S}\,\boldsymbol{a}, \tag{3.1.4}$$

where $\boldsymbol{S}$ is a square matrix of the order $n \times n$ and $\boldsymbol{a}$ and $\boldsymbol{b}$ are vectors, respectively, of the input and output power wave variables at the ports of the multiport.

The diagonal elements s_{ii} of the matrix $\boldsymbol{S}$ are the power wave reflection coefficients at the port i, and the off-diagonal elements s_{ik}, for $i \neq k$, are the power wave transmission coefficients between ports i and k.

The scattering parameters are physically interpreted by the power transfer between the ports of a multiport. The total power P delivered to all n ports of the circuit is the sum of the corresponding powers delivered to the individual ports. It is given by the relation

$$P = \sum_{i=1}^{n} \mid a_i \mid^2 - \sum_{i=1}^{n} \mid b_i \mid^2 = \boldsymbol{a}^{+}(\mathbb{1} - \boldsymbol{S}^{+}\boldsymbol{S})\boldsymbol{a}, \tag{3.1.5}$$

where $\mathbb{1}$ is a unit matrix of order n, and the superscript $(^+)$ indicates the complex conjugate transposed matrix or vector.

In a passive multiport, for which $P \geq 0$, the scattering matrix $\boldsymbol{S}$ satisfies the condition

$$\mathbb{1} - \boldsymbol{S}^+ \boldsymbol{S} \geq 0, \tag{3.1.6}$$

for all frequencies. Moreover, if the multiport is lossless, i.e. $P = 0$, (3.1.6) becomes

$$\mathbb{1} - \boldsymbol{S}^+ \boldsymbol{S} = 0. \tag{3.1.7}$$

Therefore, the scattering matrix of a passive lossless network is a unitary matrix. An important property of the $\boldsymbol{S}$ matrix for a reciprocal network is the symmetry, that is,

$$\boldsymbol{S} = \boldsymbol{S}^{\mathbf{T}}, \tag{3.1.8}$$

where $S^{\mathbf{T}}$ is the transpose of the matrix $\boldsymbol{S}$.

The scattering matrix of a multiport can be determined from the impedance and admittance matrices. It is computed from the impedance matrix as

$$\boldsymbol{S} = \mathfrak{F}(\boldsymbol{Z} - \mathfrak{G}^*)\,(\boldsymbol{Z} + \mathfrak{G})^{-1}\,\mathfrak{F}^{-1}\ , \tag{3.1.9}$$

where $\mathfrak{F}$ is a diagonal matrix defined in terms of the square root of the normalization impedance by

$$\mathfrak{F} = \begin{pmatrix} \frac{1}{2\sqrt{\mathrm{Re}(Z_{N1})}} & 0 & \dots & 0 \\ 0 & \frac{1}{2\sqrt{\mathrm{Re}(Z_{N2})}} & \dots & \vdots \\ \vdots & \dots & \ddots & 0 \\ 0 & \dots & 0 & \frac{1}{2\sqrt{\mathrm{Re}(Z_{Nn})}} \end{pmatrix}, \tag{3.1.10}$$

and $\mathfrak{G}$ is the diagonal matrix of the reference impedances Z_{Ni}

$$\mathfrak{G} = \begin{pmatrix} Z_{N1} & 0 & \dots & 0 \\ 0 & Z_{N2} & \dots & \vdots \\ \vdots & \dots & \ddots & 0 \\ 0 & \dots & 0 & Z_{Nn} \end{pmatrix}. \tag{3.1.11}$$

The inverse transformations of (3.1.3) give the voltage and currents in terms of power waves. Assuming the reference impedances of all the ports of a multiport are identical, the impedance matrix can be computed from the scattering matrix by

$$\boldsymbol{Z} = \mathfrak{F}^{-1}\,(\mathbb{1} - \boldsymbol{S})^{-1}\,(\boldsymbol{S}\,\mathfrak{G} + \mathfrak{G}^*)\,\mathfrak{F}\ . \tag{3.1.12}$$

The admittance matrix can also be derived from the scattering matrix $\boldsymbol{S}$ as

$$\boldsymbol{Y} = \mathfrak{F}\,(\mathbb{1} - \boldsymbol{S})\,(\boldsymbol{S}\,\mathfrak{G} + \mathfrak{G}^*)^{-1}\,\mathfrak{F}^{-1}\ . \tag{3.1.13}$$

3.2 Passive Component Modeling

Passive interconnected structures and terminating loads constitute the physical signal propagation paths in a PCB. High frequency parasitics of the transmission structures are described by both the transmission line theory [38, 31], and the field theory [31]. The topology in which the physical paths are connected is an important parameter for the prediction of the signal propagation between two specified devices.

3.2.1 Multiconductor Transmission Lines

At high frequencies a short section of length dz of a transmission line can be modeled as a lumped-element circuit. The electrical equivalent circuit representing this section of the line is depicted in Figure 3.2.1. The parameters R, L, G, and C modeling the line section are called the per unit length parameters.

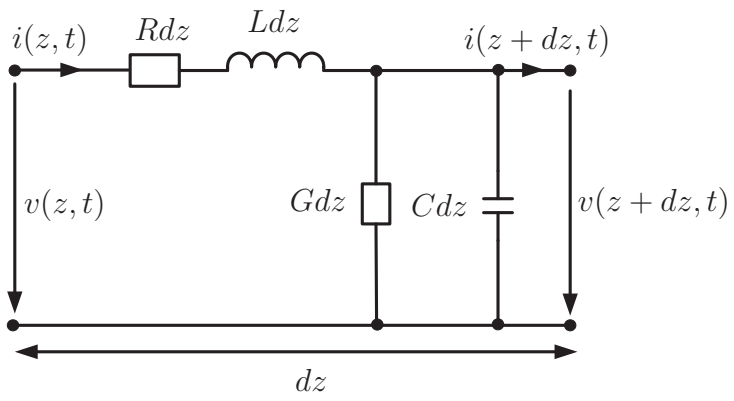


Figure 3.2.1: Lumped-element equivalent circuit of a transmission line section

In Figure 3.2.1 a small section, dz element, of a transmission line is represented. It consists of a series resistance Rdz, a series inductance Ldz, a shunt conductance Gdz, and a shunt capacitance Cdz. The parameters R, L, G, and C that are distributed along the entire line model the parasitic behaviour of the line at high frequencies. The series resistance R is due to the finite conductivity of the conductor, i.e. ohmic losses and skin effect. The series inductance L represents the total self inductance of the conductors, and the shunt capacitance C is due to the close proximity of the conductors. The shunt conductance G is due to the dielectric loss in the material between the conductors. The line is homogeneous if the per unit length parameters are constant along its expansions.

The two equations in the frequency domain describing the wave propagation for the voltages V and currents I on the line are given by

$$\begin{cases} -\dfrac{\partial V}{\partial z} = R\,I + L\dfrac{\partial I}{\partial t} \\ -\dfrac{\partial I}{\partial z} = G\,V + C\dfrac{\partial V}{\partial t} \end{cases} . \tag{3.2.1}$$

Under the steady state condition the equations in (3.2.1) can be transformed into differential equations, called also *Telegrapher*'s equations, in the frequency domain. These are given by

$$\begin{cases} \dfrac{\partial^2 V}{\partial z^2} - \gamma^2 V = 0 \\ \dfrac{\partial^2 I}{\partial z^2} - \gamma^2 I = 0 \end{cases}, \tag{3.2.2}$$

where γ is the complex propagation constant of the waves, and is defined as

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}. \tag{3.2.3}$$

The propagation constant depends on the frequency and the length of the line. Its real part α is the attenuation constant, and its imaginary part β is the phase constant. The characteristic impedance Z_0 of the line is defined as

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}. \tag{3.2.4}$$

The solution of equations (3.2.2) gives the wave equations for the voltages and currents at any locations of the transmission line. This solution is given by

$$\begin{cases} V(z) = V_0^+ \exp(-\gamma z) + V_0^- \exp(\gamma z) \\ I(z) = I_0^+ \exp(-\gamma z) + I_0^- \exp(\gamma z) \end{cases}. \tag{3.2.5}$$

The terms $\exp(-\gamma z)$ and $\exp(\gamma z)$ in (3.2.5) represent the wave propagation in the $+z$ and $-z$ directions respectively, and V_0^+, V_0^-, I_0^+, and I_0^- are constants which can be calculated from the voltage and current at the position $z = 0$.

In general the propagation constant and the characteristic impedance are complex. In the case where the line is losless, i.e. $R = G = 0$, the general expressions of the attenuation constant and the characteristic impedance can be simplified to give

$$\gamma = j\beta = j\omega\sqrt{LC}\ , \tag{3.2.6}$$

and

$$Z_0 = \sqrt{\frac{L}{C}}\ . \tag{3.2.7}$$

The frequency domain voltages and currents become

$$\begin{cases} V(z) = V^+ \exp(-j\beta z) + V^- \exp(j\beta z) \\ I(z) = I^+ \exp(-j\beta z) + I^- \exp(j\beta z) \end{cases}. \tag{3.2.8}$$

Due to the finite conductivity a transmission line has losses, which can be neglected in many practical cases. In high frequencies the losses can however depend on the frequency.

As an example, the per unit length resistance depends on the frequency according to the relation

$$R(\omega) = k_1 \sqrt{k_2\,\omega},$$

where k_1 and k_2 are constants.

At high frequencies a transmission line can be represented by its scattering parameters. The voltage and current and the associated incident and reflected waves in a transmission line terminated with a load Z_L are defined as shown in Figure 3.2.2.

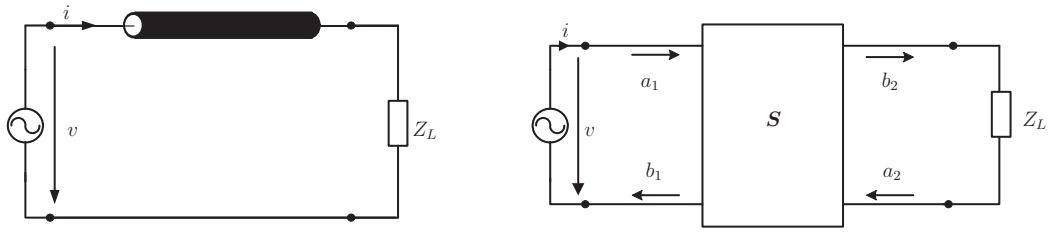


Figure 3.2.2: Two-port representation of a transmission line

If the characteristic impedance Z_0 of the line equals the load impedance Z_L, then no reflection of the power is produced and the line is said to be matched. If the characteristic impedance is different from the load impedance a portion of the incident power is reflected to the line. The reflection coefficient Γr is defined by

$$\Gamma r = \frac{Z_L - Z_0}{Z_L + Z_0}.$$

Reflections may also be produced at the generator side, if the generator presents mismatched impedance to the line. Consequently multiple reflections may occur at both ends of the line. Voltage and currents on the line consist of a superposition of the incident and reflected waves. The normalized wave phasors can be expressed as a function of voltage and current given by (3.2.5). A two-port network describing a single line represented by its scattering matrix $\boldsymbol{S}$ is shown in Figure 3.2.2.

If the single line is assumed to be lossless and has a characteristic impedance Z_0 and a length l, then its scattering matrix is given by

$$\boldsymbol{S} = \begin{pmatrix} 0 & \exp(-j\beta l) \\ \exp(-j\beta l) & 0 \end{pmatrix}.$$

The *Telegrapher*'s equations for a multiconductor transmission line system in the time domain are given by

$$\begin{cases} -\dfrac{\partial \boldsymbol{v}(z,t)}{\partial z} = \boldsymbol{R}\boldsymbol{i}(z,t) + \boldsymbol{L}\dfrac{\partial \boldsymbol{i}(z,t)}{\partial t} \\ -\dfrac{\partial \boldsymbol{i}(z,t)}{\partial z} = \boldsymbol{G}\boldsymbol{v}(z,t) + \boldsymbol{C}\dfrac{\partial \boldsymbol{v}(z,t)}{\partial t} \end{cases}, \tag{3.2.9}$$

where $\boldsymbol{R}, \boldsymbol{L}, \boldsymbol{G}$, and $\boldsymbol{C}$ are the matrices per unit length, $\boldsymbol{v}$, and $\boldsymbol{i}$ are vectors of voltages and currents on the conductors. The diagonal elements of the matrices represent the coupling of the lines to the reference conductor, the other elements represent the coupling of the conductors with each other. These matrices are of order $n \times n$, where n is the number of the coupled conductors. $\boldsymbol{L}$ and $\boldsymbol{C}$ are the inductance and capacitance matrices whose elements represent self and mutual parameters per unit length of the lines. In general $\boldsymbol{L}$ and $\boldsymbol{C}$ do not change heavily like $\boldsymbol{R}$. $\boldsymbol{G}$ increases proportionally with the frequency because of the dielectric losses.

Again, and assuming the steady state analysis, (3.2.9) can be written as

$$\begin{cases} \dfrac{\partial \boldsymbol{V}(z,\omega)}{\partial z} + (\boldsymbol{R}(\omega) + j\omega \boldsymbol{L}(\omega))\boldsymbol{I}(z,\omega) = 0 \\ \dfrac{\partial \boldsymbol{I}(z,\omega)}{\partial z} + (\boldsymbol{G}(\omega) + j\omega \boldsymbol{C}(\omega))\boldsymbol{V}(z,\omega) = 0 \end{cases} . \tag{3.2.10}$$

Introducing the impedance and admittance matrices defined by

$$\begin{cases} \boldsymbol{Z}(j\omega) = \boldsymbol{R}(\omega) + j\omega\ \boldsymbol{L}(\omega) \\ \boldsymbol{Y}(j\omega) = \boldsymbol{G}(\omega) + j\omega\ \boldsymbol{C}(\omega) \end{cases} ,$$

the equations (3.2.10) become

$$\begin{cases} \dfrac{\partial^2 \boldsymbol{V}(z,\omega)}{\partial z^2} - \boldsymbol{Z}(j\omega)\boldsymbol{Y}(j\omega)\boldsymbol{V}(z,\omega) = 0 \\ \dfrac{\partial^2 \boldsymbol{I}(z,\omega)}{\partial z^2} - \boldsymbol{Y}(j\omega)\boldsymbol{Z}(j\omega)\boldsymbol{I}(z,\omega) = 0 \end{cases} . \tag{3.2.11}$$

Similarly to the propagation constant γ of a single line, the complex wave matrix $\boldsymbol{\Gamma}$ can be defined for a multiconductor system as

$$\boldsymbol{\Gamma}(j\omega) = \sqrt{\boldsymbol{Z}(j\omega)\,\boldsymbol{Y}(j\omega)}.$$

The solution to voltage waves in (3.2.11) can be expressed in terms of the wave matrix $\boldsymbol{\Gamma}$ as

$$\boldsymbol{V}(z,\omega) = V_+ \exp(-\boldsymbol{\Gamma}(j\omega)\, z) + V_- \exp(\boldsymbol{\Gamma}(j\omega)\, z), \tag{3.2.12}$$

where V_+ and V_- are constant coefficients defining the conditions at the position $z = 0$ on the lines. The current waves can be obtained by substituting the voltage solution (3.2.12) in (3.2.10), and solving the resulting equation. The characteristic admittance matrix $\boldsymbol{Y}_L$ of the transmission line system is defined by

$$\boldsymbol{Y}_L(j\omega) = \boldsymbol{Z}(j\omega)^{-1} \sqrt{\boldsymbol{Z}(j\omega)\,\boldsymbol{Y}(j\omega)}\ .$$

The voltages and currents at any location z of a multiconductor transmission line are related by the chain, or transfer matrix $\boldsymbol{\Phi}$. It is a $n \times n$ matrix that can be partitioned into four submatrices $\boldsymbol{\Phi}_{11}$, $\boldsymbol{\Phi}_{12}$, $\boldsymbol{\Phi}_{21}$, and $\boldsymbol{\Phi}_{22}$, such that

$$\begin{pmatrix} \boldsymbol{V}(z,\omega) \\ \boldsymbol{I}(z,\omega) \end{pmatrix} = \begin{pmatrix} \boldsymbol{\Phi}_{11}(z,\omega) & \boldsymbol{\Phi}_{12}(z,\omega) \\ \boldsymbol{\Phi}_{21}(z,\omega) & \boldsymbol{\Phi}_{22}(z,\omega) \end{pmatrix} \begin{pmatrix} \boldsymbol{V}(0,\omega) \\ \boldsymbol{I}(0,\omega) \end{pmatrix}, \tag{3.2.13}$$

where the submatrices are defined by

$$\begin{aligned} \boldsymbol{\Phi}_{11}(z,\omega) &= \frac{1}{2}(\exp^{\boldsymbol{\Gamma}(j\omega)\,z} + \exp^{-\boldsymbol{\Gamma}(j\omega)\,z}) \\ \boldsymbol{\Phi}_{12}(z,\omega) &= -\frac{1}{2}(\exp^{\boldsymbol{\Gamma}(j\omega)\,z} + \exp^{-\boldsymbol{\Gamma}(j\omega)\,z})\boldsymbol{Y}_L^{-1}(j\omega) \\ \boldsymbol{\Phi}_{21}(z,\omega) &= -\frac{1}{2}(\exp^{\boldsymbol{\Gamma}(j\omega)\,z} + \exp^{-\boldsymbol{\Gamma}(j\omega)\,z}) \\ \boldsymbol{\Phi}_{22}(z,\omega) &= \frac{1}{2}(\exp^{\boldsymbol{\Gamma}(j\omega)\,z} + \exp^{-\boldsymbol{\Gamma}(j\omega)\,z})\boldsymbol{Y}_L^{-1}(j\omega) \end{aligned} \tag{3.2.14}$$

The impedance matrix $\boldsymbol{Z}$ can be computed from the chain matrix as

$$\mathbf{Z} = \begin{pmatrix} -\boldsymbol{\Phi}_{11}\,\boldsymbol{\Phi}_{21}^{-1} & -\boldsymbol{\Phi}_{21}^{-1} \\ -\boldsymbol{\Phi}_{21}^{-1} & -\boldsymbol{\Phi}_{21}^{-1}\,\boldsymbol{\Phi}_{22} \end{pmatrix}. \tag{3.2.15}$$

The chain matrix $\boldsymbol{\Phi}$ of a system of transmission lines can be determined from the per unit length parameters. The corresponding impedance matrix can be calculated from (3.2.15). Using (3.1.9) the scattering matrix relating the line ends can be computed.

3.2.2 Transmission Line Discontinuities

Discontinuities are present on PCBs due to layout necessities. These cause disturbances in the electric and magnetic fields which produce signal integrity effects like reflections and radiation. At the discontinuity regions many high order modes in addition to the propagating ones are produced. The accurate characterization of the EM behaviour of complex discontinuities occurring along printed circuit board signal paths represents one of the most important issues in the signal integrity analysis.

In a lumped equivalent circuit, disturbances in electric and magnetic fields are represented as an equivalent capacitance and an equivalent inductance respectively. Lumped element equivalent circuits of different types of discontinuities are provided in literature [37, 39, 40]. Many modeling techniques of complex discontinuities are based on the extraction of passive lumped equivalent circuits from numerical field solutions and measurement data [41, 42, 43]. For discontinuities with shorter longitudinal dimension one can model with shunt or series reactance, whereas for large longitudinal dimensions one can model by a T or Π network. The extraction of the $\boldsymbol{R}$, $\boldsymbol{L}$, $\boldsymbol{G}$, and $\boldsymbol{C}$ matrices of single and coupled transmission lines is carried out using 2D field solvers. For complex discontinuities 3D field solvers are needed to get accurate simulation.

Full wave numerical analysis, that allows to account for the non-TEM propagation mode occurring in proximity of a discontinuity, appears as the only reliable way of modeling accurately the electromagnetic behaviour of discontinuities. There are many field

solver tools for analyzing interconnect structures. All these are based on the solution of *Maxwell*'s equations in one form or another. The main differences between the tools are the equations solved, the numerical technique as well as the discretization procedure used. For instance, the frequency domain scattering parameters of a discontinuity structure can be obtained by the finite element software tool HFSS of Agilent [44], or by the finite integration technique tool Microwave Studio of CST [23]. These methods are very flexible in modeling complex geometries and suitable to account for the dispersive nature of the dielectric substrate. If necessary, the second tool provides the ability to synthesize an equivalent electrical model of the discontinuity from the simulation data.

3.2.3 Passive Discrete Components

Discrete passive components, R, L, and C, are two port devices that often appear in microwave networks as termination loads, or between the connection of many multiport elements. Like the transmission structures, these can also be represented by their impedance, admittance, or scattering matrices. Since microwave networks are better analyzed by means of the scattering parameters, it is also important to use this representation for discrete passive components [45]. The scattering matrices of a termination load, a series impedance, and a shunt admittance are given in Appendix B. For several parallel admittances or series impedances the scattering matrix can be derived from the equivalent admittance or impedance, respectively.

The scattering matrices for complex parallel and series connections, called also junctions, connecting more than three electronic elements can be derived from the fundamental matrices of the simple junctions given in Appendix B. In [46, 47], methods for the characterization of various junctions using voltage and current waves are provided.

The scattering matrices of both the structures and discrete components are normalized to a port reference impedance of $50\,\Omega$. Because of the passivity property of the circuit elements the symmetry of the matrices is fulffiled.

3.3 Nonlinear Component Modeling

In this thesis nonlinear devices are assumed only to appear at the terminations of the propagation paths. The first part of this section describes the general model of a diode which is frequently used in protection circuits of ICs against overvoltages. The second part provides some examples of efficient models of chip ports used in circuit simulation.

3.3.1 Passive Nonlinear Devices

The most common nonlinear element used in microwave circuits is the schottky diode. In signal integrity analysis the diode appears mainly in the protection circuits of digital

devices. The current-voltage characteristic of an ideal pn junction diode is described by the equation

$$I = I_s \left[\exp\left(\frac{q_e V}{\kappa T_K} \right) - 1 \right], \tag{3.3.1}$$

where $q_e = 1.6022 \times 10^{-19}$ C is the electronic charge, $\kappa = 1.3806 \times 10^{-23}$ J/°K is the *Boltzmann*'s constant, T_K is the absolute temperature in degrees *Kelvin*, I_s is the saturation current, which depends on the physical properties of the diode, and V is the voltage across the diode.

The dynamic conductance of a diode is defined as follows. When a constant voltage V_0 is applied to the diode, a constant current flows through it. The slope of the curve (I, V) at the operating point V_0 is called the dynamic conductance of the diode. It is determined as the derivative of I with respect to the voltage V by

$$g(V_0) = \left. \frac{dI}{dV} \right|_{V=V_0} = \frac{I_s}{V_T} \exp\left(\frac{V_0}{V_T} \right), \tag{3.3.2}$$

where $V_T = \kappa T_K / q_e$.

Equation (3.3.1) is sufficient to describe the DC behaviour of the diode. At higher frequencies additional parasitic effects have to be included into the diode model for more accurate description. Parallel capacitances come into the model which are dependent on the voltage across the diode [48, 49]. The dynamic model of the diode is depicted in Figure 3.3.1.

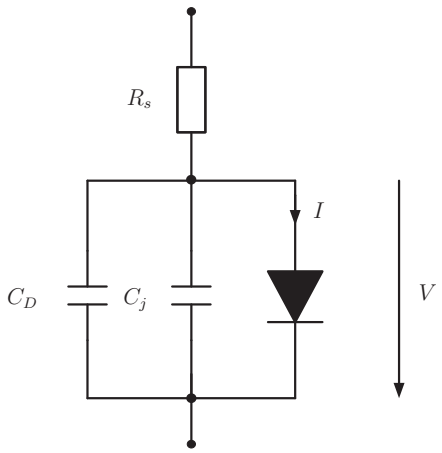


Figure 3.3.1: Dynamic model of the diode

In Figure 3.3.1, R_S represents the bulk resistance which is assumed to be constant. The capacitances C_j and C_D are called the depletion and diffusion capacitance, respectively. The depletion capacitance is defined as

$$C_j = \begin{cases} \dfrac{C_{j0}}{\left(1 - \dfrac{V}{\phi}\right)^{\eta}}, & \text{for } V \leq \phi - \phi_0 \\ K_1 V + K_2, & \text{for } V > \phi - \phi_0, \end{cases} \tag{3.3.3}$$

where η is the grading coefficient and is comprised between 0.33 and 0.5. A typical value of the built-in potential ϕ of the diode is 0.8. ϕ_0 is a constant value which depends on the material of the diode and is between 0.05 and 0.5. The constant C_{j0} is the capacity of the junction when $V = 0$ and depends on the physical construction of the diode. V_0 is the barrier voltage which depends on the material.

The parameters K_1 and K_2 in (3.3.3) are defined by

$$K_1 = \left.\frac{dC_j}{dV}\right|_{V=\phi-\phi_0}$$
$$K_2 = -K_1\left(\phi - \phi_0\right) + C_j|_{V=\phi-\phi_0}\,.$$

The diffusion capacitance is defined by

$$C_D = \begin{cases} \tau_D \dfrac{dI}{dV} & ,V > 0 \\ 0 & ,V \leq 0 \end{cases}, \tag{3.3.4}$$

where τ_D is the transient time.

The diode is one of the powerful devices for chip ESD protection due to its low trigger voltage, low turn-on resistance, and high ESD robustness. The function of the diodes is to clamp the ESD overstress and to transfer it to the ground. The basic approach to absorb the discharge is shown in Figure 3.3.2(a). The protection circuit must provide the required level without degrading the input signal or the characteristics of the internal circuit. There are different protection topologies depending on the type of the chip pin to be protected. An example of ESD protection structure constructed from double clamp diodes for I/O pin is shown in Figure 3.3.2(b). A negative ESD impulse will cause the lower diode to forward bias, thereby transferring discharge through the lower diode into ground. A positive impulse however, causes the upper diode to forward bias and the discharge is transferred into V_{cc}. The capacitance connecting V_{cc} to ground dissipates the discharge into ground. Instead of schottky diodes zener diodes can also be used. The capacitance of the zener diodes from the I/O pin to ground is higher. Therefore, they are not suitable to high-speed signals.

3.3.2 Active Device Models

Simulation of digital I/O buffers, together with their chip packages and printed circuit boards, can mainly be done by many approaches. The traditional approach is to use transistor level models, which is particularly useful when small circuits should be simulated. This approach would be very time consuming for simulations of a large number of buffers and their interconnections. As an alternative solution to this problem, behavioural models of devices such as I/O Buffer Information Specification (IBIS) are introduced [50]. The behavioural IBIS modeling data can be derived from measurements as well as circuit simulations. Simulations with behavioural models can be generally executed faster than the corresponding simulations with transistor level models.

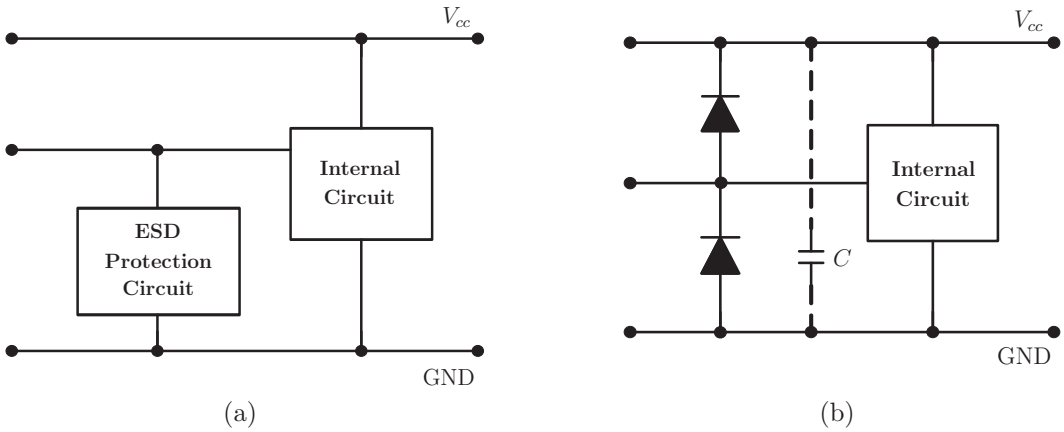


Figure 3.3.2: Typical I/O ESD protection circuit

SPICE transistor level models are single buffer centric. They often represent one of several inputs or outputs of a buffer. However, IBIS models are pin specific, the model describes all pins of the physical component. A complete IC contains different models, depending on the number of different driver and receiver types of the device [51]. A set of I/O pins that have the same characteristic behaviour can be grouped together into one model. The data are stored in forms of current-voltage tables, and switching and package information. The pins are classified as input, output, 3-state, I/O, open drain, power, GND, and NC pin. The model for an I/O buffer is represented in Figure 3.3.3.

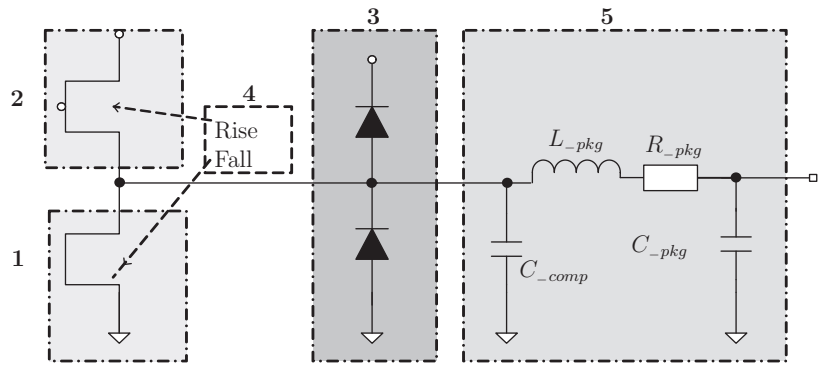


Figure 3.3.3: IBIS I/O buffer specification [50]

In this figure the blocks 1 and 2 represent the pulldown and pullup transistors of a digital device I/O buffer output stage. Block 3 consists of DC I/V-tables representing the ESD clamping diodes, power clamp and GND clamp. Block 4 represents the transition time of the output as it switches from one logic state to another. Rise and fall times are represented by the ratios of transition voltage to transition time dV/dt. Block 5 represents the `die` capacitance $C_{\_comp}$ of the input pin and the package parasitics of that pin. The package characteristic resistance, inductance and capacitance are denoted by $R_{\_pkg}$, $L_{\_pkg}$, and $C_{\_pkg}$, respectively. These represent the models of the bond wire and pin combination of the package. The model of the pin package is very important to make an accurate characterization of the input signal at high frequencies. The schematic

representing the input stage consists only of the blocks 3 and 5.

IBIS is a data format including typical curves in tabular form, which contains dynamic and static characteristics in three different conditions given as typical, minimum and maximum values. IBIS models offer higher numerical efficiency than SPICE models. In addition they are capable of maintaining suitable accuracy since the nonlinear aspects of I/O structures, as well as package parasitics and ESD structures, are considered in the model parameters.

Digital devices can be electrically described in time domain by accurate transistor level models, or IBIS behavioural models. In the frequency domain linear approximations must be made for the ports characteristics of nonlinear digital devices. Linear models are very efficient to simulate, but lumped element model of digital IC do not provide the accuracy needed for the signal integrity analysis. In [52] linear models representing the driver switching behaviour of an IC, and which consist of a shunt RC at the IC-ports to GND and a shunt capacitance C to V_{cc}, are presented. Figure 3.3.4 shows these linear models and their simple variants.

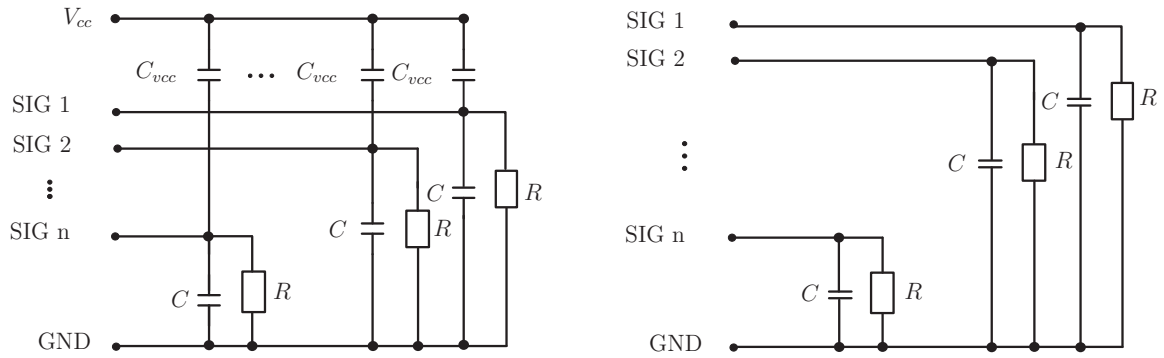


Figure 3.3.4: Linear IC-port model: (a) general model, (b) simple model

3.4 Analysis of a Complete Signal Propagation Path

Physical paths on a printed circuit board include all the interconnected transmission structures connecting present electronic devices. They contain connectors, cables, PCB tracks like microstrip and strip lines, discontinuities like vias, bends, and discrete linear and nonlinear components such as resistors, capacitors, diodes, etc. The elements belonging to a coupling path can be grouped into

- Linear elements: transmission lines, discontinuities, discrete components
- Nonlinear elements: diodes, IC I/O pins

Each of the components above can be considered as a small module. Discontinuities and nonlinear components can be represented by simplified equivalent circuit models.

These models can be derived in terms of lumped element circuit using resistors, inductors, capacitors, transmission lines, and dependent voltage and current sources. The resulting network from all these models generally produces an approximated model to the original network.

Usually linear elements are well modeled in the frequency domain. However the behaviour of nonlinear elements is analyzed in the time domain. A variety of circuit simulators use linearized models of nonlinear devices and then perform a transient simulation. Alternatively, there are also different hybrid approaches combining between both analysis.

The analysis of a complete signal propagation path from a noise source to a chip pin requires the characterization of all the circuit elements along this path. The main parts of a signal path at a circuit board level are the physical paths present in the system. IC Drivers and receivers may be present at the terminations of signal paths.

Interconnect structures with complex geometry are treated as lumped multiports described by passive macromodels or directly by their frequency domain data. In order to identify dominant propagation paths, all the substructures on the PCB must be characterized. Accurate and efficient models for each of these substructures lead to the reduction of the analysis complexity.

Discontinuities in the noise propagation paths can strongly affect the signal behaviour at the terminations of the paths. At the PCB level they constitute the critical parts which decide how and where the noise will flow to the victim device. A proper modeling of discontinuities should take into account geometry and material properties, thus requiring a complex full wave electromagnetic analysis. Instead of applying this costly analysis to the entire system, the subparts are analyzed separately. Each substructure is characterized via full wave analysis. It is very important to limit the set of the substructures that should be characterized small when partitioning the system. This can be reached by considering only coupling between neighbouring transmission lines which is called first level coupling before performing field simulation. As a result larger coupling effects are neglected and errors may be produced at high frequencies. More accurate simulation results can be obtained by taking into account higher order coupling, which requires more complex test structures.

Circuit drivers and receivers are usually buffers characterized by strong nonlinearities and relevant dynamic effects. Their intrinsic nonlinear and dynamic behaviour can significantly affect the shape of the noise impulses propagating. SPICE transistor level models and IBIS behavioural models of IC buffers are the most popular models used in the signal integrity analysis.

In conclusion the main steps usually used for the simulation of signal paths are:

1. Simulation of the parasitic behaviour of the transmission structures by the use of a 2D, 2.5D, or 3D field solver

2. Combination of these simulation parameters with the driver and receiver models of ICs as transistor based models or in the IBIS format.

3. Perform an electric simulation of the whole system

Chapter 4

Analysis Techniques of Large Circuits

This chapter provides an overview of the techniques mainly used for the simulation of microwave circuits. All these techniques are based on the formulation of the circuit equations using specific variables. The choice of a given technique depends on some features like the size, the topology, and the variables to be determined.

4.1 Basic Circuit Analysis Techniques

At low frequencies the analysis of electrical circuits is performed in terms of voltages and currents at the circuit terminals. The nodal admittance matrix is the most used method for computer-aided analysis of linear circuits in the frequency domain. When high frequency parasitics should be characterized, scattering matrix analysis are preferred [45]. Their derivation is based on introducing of power, voltage and current waves. In this section methods based on power waves are described. More details on analysis methods formulated in terms of voltage and current waves, known as Baum-Liu-Tesche (BLT) equations, can be found in [53, 54, 55].

4.1.1 Nodal Admittance Analysis

The nodal admittance matrix is derived on the basis of the *Kirchhoff*'s current law equations at the circuit nodes. The voltages at all nodes in the circuit are assumed to be known. The solution for the currents is given by

$$\boldsymbol{I} = \boldsymbol{Y}\,\boldsymbol{V}, \tag{4.1.1}$$

where $\boldsymbol{Y}$ is a square nodal admittance matrix, its degree equals the number of nodes in the circuit. $\boldsymbol{V}$ is a vector of node voltages, and $\boldsymbol{I}$ is a vector of terminal currents of the independent sources.

A more useful variant of the nodal admittance matrix is the indefinite admittance matrix. This method reduces the memory space and computation time requirements in the analysis of large circuits by deviding a circuit into subcircuits and separately computing the indefinite admittance matrices of the successive circuits connected to others. The reference node is located outside of the subcircuits. At each step a subcircuit is considered and its nodes are ordered into internal and external ones. For a subcircuit consisting of many multiports, the nodes connecting these multiports are the internal ports and the others are external nodes. The admittance matrix of the subcircuit can be written as

$$\begin{pmatrix} \boldsymbol{I}_e \\ \boldsymbol{I}_i \end{pmatrix} = \begin{pmatrix} \boldsymbol{Y}_{ee} & \boldsymbol{Y}_{ei} \\ \boldsymbol{Y}_{ie} & \boldsymbol{Y}_{ii} \end{pmatrix} \begin{pmatrix} \boldsymbol{V}_e \\ \boldsymbol{V}_i \end{pmatrix}, \tag{4.1.2}$$

where $\boldsymbol{I}_e$ and $\boldsymbol{V}_e$ are the vectors of the currents and voltages relative to the external nodes of the resultant circuit, $\boldsymbol{I}_i$ and $\boldsymbol{V}_i$ are the vectors of the currents and voltages relative to its internal nodes.

The resulting indefinite admittance matrix of this subcircuit, which relates voltages and currents at its external ports, can be derived from (4.1.2). It is given as

$$\boldsymbol{Y}_e = \boldsymbol{Y}_{ee} - \boldsymbol{Y}_{ei}\, \boldsymbol{Y}_{ii}^{-1}\, \boldsymbol{Y}_{ie}. \tag{4.1.3}$$

4.1.2 Connection Matrix Method

The connection matrix method is applicable when the network contains arbitrarily interconnected multiports and independent voltage or current sources. Its derivation is based on the formulation of the connectivity between the ports of the components that are connected with each other. All ports in the network are assumed to be connected [45, 37].

In a network with m multiport components, the incoming and outgoing wave variables $\boldsymbol{a}_i$ and $\boldsymbol{b}_i$ at the ports of the i-th component having n ports, are related by the scattering matrix $\boldsymbol{S}_i$ as

$$\boldsymbol{b}_i = \boldsymbol{S}_i\, \boldsymbol{a}_i. \tag{4.1.4}$$

Considering the waves impressed by the independent sources to the m multiport components, represented by the wave vector $\boldsymbol{c}$, the relation (4.1.4) becomes

$$\boldsymbol{b} = \boldsymbol{S}\, \boldsymbol{a} + \boldsymbol{c}. \tag{4.1.5}$$

In (4.1.5) the supervectors $\boldsymbol{a}, \boldsymbol{b}$, and $\boldsymbol{c}$ are defined by

$$\boldsymbol{a} = \begin{pmatrix} \boldsymbol{a}_1 \\ \boldsymbol{a}_2 \\ \vdots \\ \boldsymbol{a}_m \end{pmatrix}, \qquad \boldsymbol{b} = \begin{pmatrix} \boldsymbol{b}_1 \\ \boldsymbol{b}_2 \\ \vdots \\ \boldsymbol{b}_m \end{pmatrix}, \qquad \boldsymbol{c} = \begin{pmatrix} \boldsymbol{c}_1 \\ \boldsymbol{c}_2 \\ \vdots \\ \boldsymbol{c}_m \end{pmatrix},$$

where, $\boldsymbol{a}_i$, $\boldsymbol{b}_i$, and $\boldsymbol{c}_i$, for $i = 1, 2, ..., m$, are the subvectors representing the waves at the ports of the multiport component i.

The supermatrix $\boldsymbol{S}$ is defined by

$$\boldsymbol{S} = \begin{pmatrix} \boldsymbol{S}_1 & \cdots & 0 & \cdots & 0 \\ \vdots & \cdots & \vdots & \cdots & \vdots \\ 0 & \cdots & \boldsymbol{S}_i & \cdots & 0 \\ \vdots & \cdots & \vdots & \cdots & \vdots \\ 0 & \cdots & 0 & \cdots & \boldsymbol{S}_m \end{pmatrix} = diag(\boldsymbol{S}),$$

where, $\boldsymbol{S}_i$ for $i = 1, 2, ..., m$, are the scattering submatrices of the individual multiports.

The matrix $\boldsymbol{S}$ is a block matrix whose submatrices along the diagonal are the scattering matrices of various ports, and zeros represent null matrices. For a pair of connected ports, the outgoing wave variable at one port must be equal the incoming wave variable at the other, assuming that the wave variables at the two connected ports are similarly normalized. The connectivity between two ports is illustrated in the subnetwork of Figure 4.1.1.

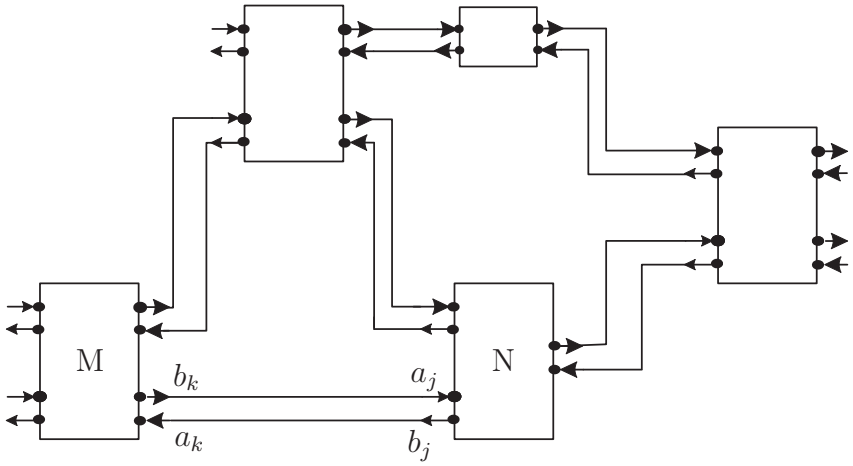


Figure 4.1.1: A subnetwork showing a connection between two ports

For example, if port j of one component is connected to port k of another component as shown in Figure 4.1.1, the incoming and outgoing waves satisfy

$$\begin{cases} a_j = b_k \\ a_k = b_j \end{cases}. \tag{4.1.6}$$

When the reference impedances of the two ports are equal, the two equations in (4.1.6) may be written in a matrix form like

$$\begin{pmatrix} b_k \\ b_j \end{pmatrix} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \begin{pmatrix} a_k \\ a_j \end{pmatrix}.$$

This matrix contains only 1's and 0's because the normalizing impedances for the two ports are assumed to be equal. Considering all the interconnections within a network, one gets an equation like

$$\boldsymbol{b} = \boldsymbol{P}\,\boldsymbol{a}, \tag{4.1.7}$$

where, $\boldsymbol{P}$ is a connection matrix describing the network topology. In each row of $\boldsymbol{P}$ all elements are zero except an entry 1 in the column indicating the interconnection. From (4.1.5) and (4.1.7), one can get

$$\boldsymbol{a} = (\boldsymbol{P} - \boldsymbol{S})^{-1}\, \boldsymbol{c}. \tag{4.1.8}$$

In this equation $\boldsymbol{c}$ is a vector of impressed wave variables and $(\boldsymbol{P} - \boldsymbol{S})$ is the connection scattering matrix. The solution of this equation gives the incoming waves $\boldsymbol{a}$ at all the component ports in the network, the outgoing waves $\boldsymbol{b}$ can be obtained from equation (4.1.7). The main diagonal elements in the matrix $(\boldsymbol{P} - \boldsymbol{S})$ are the negative values of the reflection coefficients at the various components ports. The elements corresponding to the ports of the same component are the negative of the transmission coefficients, and all other elements are zero except those corresponding to the two ports connected together.

The zero-nonzero pattern depends only on the topology and does not change with frequency. For a transmission line switched between nodes j and k with a length l_{jk}, the propagation equation in (4.1.7) becomes

$$\begin{pmatrix} b_k \\ b_j \end{pmatrix} = \begin{pmatrix} 0 & e^{-\gamma l_{jk}} \\ e^{-\gamma l_{jk}} & 0 \end{pmatrix} \begin{pmatrix} a_k \\ a_j \end{pmatrix},$$

where $\gamma = \alpha + j\beta$ is the propagation constant. α is the attenuation constant and β is the phase constant. If the transmission line is lossless, the last expression becomes

$$\begin{pmatrix} b_k \\ b_j \end{pmatrix} = \begin{pmatrix} 0 & e^{-j\beta l_{jk}} \\ e^{-j\beta l_{jk}} & 0 \end{pmatrix} \begin{pmatrix} a_k \\ a_j \end{pmatrix}.$$

Crosstalk Circuit Example

In this example, the connection matrix method is compared to the conventional SPICE frequency domain analysis. Figure 4.1.2 shows a circuit consisting of three pairs of parallel coupled microstrip transmission lines [56].

The lengths of the lines are: l_1=5 cm, l_2=4 cm, and l_3=3 cm. The per unit length matrices characterizing the coupled microstrips are given by the following matrices:

$$\boldsymbol{R} = \begin{pmatrix} 75 & 15 \\ 15 & 75 \end{pmatrix} \frac{\Omega}{\mathrm{m}}, \qquad \boldsymbol{L} = \begin{pmatrix} 494.6 & 63.3 \\ 63.3 & 494.6 \end{pmatrix} \frac{\mathrm{nH}}{\mathrm{m}},$$

$$\boldsymbol{G} = \begin{pmatrix} 0.1 & -0.01 \\ -0.01 & 0.1 \end{pmatrix} \frac{\mathrm{S}}{\mathrm{m}}, \quad \boldsymbol{C} = \begin{pmatrix} 62.8 & -4.9 \\ -4.9 & 62.8 \end{pmatrix} \frac{\mathrm{pF}}{\mathrm{m}},$$

The simulation results are given for the lossless and lossy cases in Figure 4.1.3. In the lossless case, the per unit length matrices $\boldsymbol{R}$ and $\boldsymbol{G}$ are not considered. The wave variables are computed at all the network ports and transformed into voltage ones. Then, the results are presented in the Figures 4.1.3(a) and 4.1.3(b) in terms of the voltage transfer

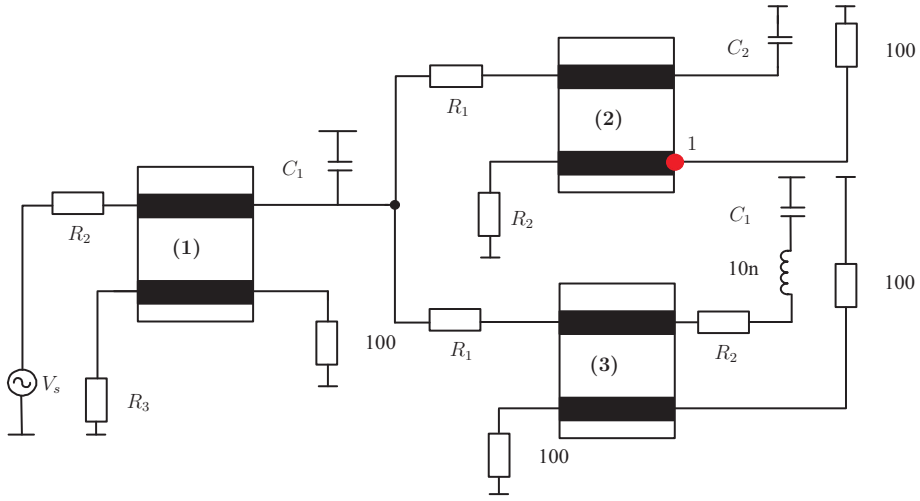


Figure 4.1.2: A transmission line circuit example (R_1=25Ω, R_2=50Ω, R_3=75Ω, R_4=100Ω, C_1=1 pF, C_2=2 pF, L=10 nH) [56]

function at the node t respectively. The curves of the responses are compared to the SPICE simulations.

In both cases the results of the connection matrix method are close to the ones provided by the SPICE simulations over the frequency range of 2 GHz. For the lossless case a small difference of the curves representing the connection matrix method and that of the SPICE model is observed above the frequency of 1.8 GHz.

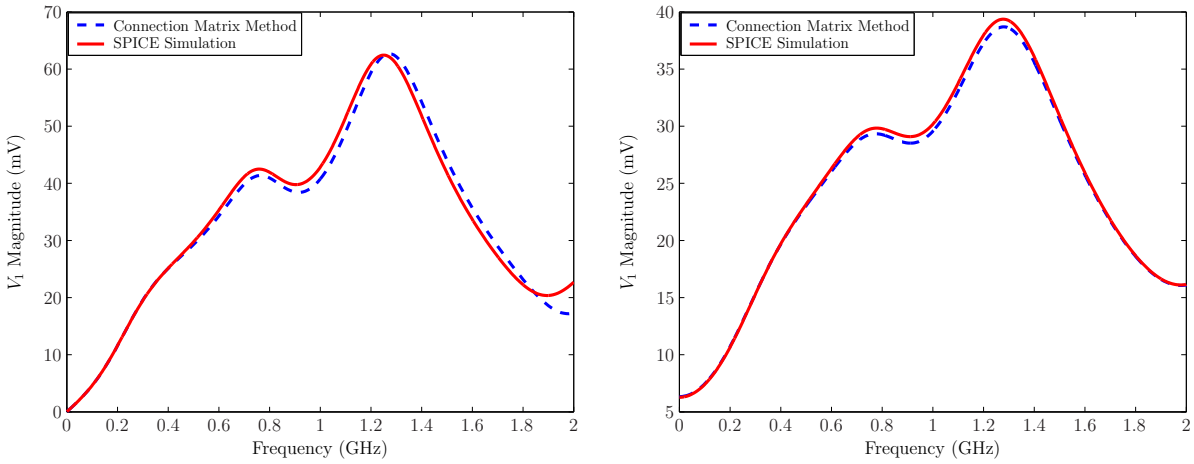


Figure 4.1.3: Voltage amplitude at the node 1

To conclude, the connection matrix method is an easy technique for the simulation of microwave circuits using the scattering parameters. The high frequency parasitic behavior of the circuit layout can be included into the analysis considering the scattering parameters of the transmission structures interconnecting the devices, and the connectivity information.

4.1.3 Transfer Scattering Matrix Method

The transfer scattering matrix in its classical form describes multiports with the same number of input and output ports. For a multiport with n input ports and n output ports, the scattering matrix is defined by

$$\begin{pmatrix} \boldsymbol{b}_{in} \\ \boldsymbol{b}_{out} \end{pmatrix} = \begin{pmatrix} \boldsymbol{S}_{11} & \boldsymbol{S}_{12} \\ \boldsymbol{S}_{21} & \boldsymbol{S}_{22} \end{pmatrix} \begin{pmatrix} \boldsymbol{a}_{in} \\ \boldsymbol{a}_{out} \end{pmatrix}, \tag{4.1.9}$$

where $\boldsymbol{S}_{11}$, $\boldsymbol{S}_{12}$, $\boldsymbol{S}_{21}$, and $\boldsymbol{S}_{22}$ are the scattering submatrices, $\boldsymbol{a}_{in}$, and $\boldsymbol{b}_{in}$ are the vectors of incoming and outgoing waves at the n input ports of the $2\,n$-multiport respectively, $\boldsymbol{a}_{out}$, and $\boldsymbol{b}_{out}$ are the vectors of incoming and outgoing waves at the n output ports of the $2\,n$-multiport.

The transfer scattering matrix $\boldsymbol{T}$ can be derived from (4.1.9) by ordering the input and output waves at both sides of the multiports as

$$\begin{pmatrix} \boldsymbol{b}_{in} \\ \\ \boldsymbol{a}_{in} \end{pmatrix} = \begin{pmatrix} \boldsymbol{S}_{12} - \boldsymbol{S}_{11}\boldsymbol{S}_{21}^{-1}\boldsymbol{S}_{22} & \boldsymbol{S}_{11}\boldsymbol{S}_{21}^{-1} \\ \\ \boldsymbol{S}_{21}^{-1}\boldsymbol{S}_{22} & \boldsymbol{S}_{21}^{-1} \end{pmatrix} \begin{pmatrix} \boldsymbol{a}_{out} \\ \\ \boldsymbol{b}_{out} \end{pmatrix} = \boldsymbol{T} \begin{pmatrix} \boldsymbol{a}_{out} \\ \\ \boldsymbol{b}_{out} \end{pmatrix} \tag{4.1.10}$$

If the number of the input and output ports is not equal, the submatrix $\boldsymbol{S}_{21}$ is not a square matrix and therefore its inverse does not exits. Consequently the transfer scattering matrix does not exist. To solve this problem, the scattering matrix is extended to have the following form

$$\begin{pmatrix} \boldsymbol{b}_{in} \\ \boldsymbol{b}_{out} \\ \boldsymbol{b}_{e} \end{pmatrix} = \begin{pmatrix} \boldsymbol{S}_{11} & \boldsymbol{0} & \boldsymbol{S}_{12} \\ \boldsymbol{S}_{21} & \boldsymbol{S}_{b} & \boldsymbol{S}_{22} \\ \boldsymbol{S}_{c} & \boldsymbol{S}_{d} & \boldsymbol{0} \end{pmatrix} \begin{pmatrix} \boldsymbol{a}_{in} \\ \boldsymbol{a}_{e} \\ \boldsymbol{a}_{out} \end{pmatrix}, \tag{4.1.11}$$

where $\boldsymbol{b}_e$ is a vector of additional virtual outgoing wave variables, $\boldsymbol{a}_e$ is a vector of additional virtual incoming wave variables, all equal zero by definition, $\boldsymbol{a}_e = \boldsymbol{0}$. Virtual waves $\boldsymbol{a}_e$ and $\boldsymbol{b}_e$ correspond to virtual input ports that do not really exist. $\boldsymbol{S}_b$, $\boldsymbol{S}_c$, and $\boldsymbol{S}_d$ are blocks of the extended square submatrix

$$\boldsymbol{S}_{21}^{e} = \begin{pmatrix} \boldsymbol{S}_{21} & \boldsymbol{S}_{b} \\ \boldsymbol{S}_{c} & \boldsymbol{S}_{d} \end{pmatrix}. \tag{4.1.12}$$

The number of columns in the submatrix $\boldsymbol{S}_b$ equals the number of the new added virtual incoming wave variables located in the vector $\boldsymbol{a}_e$. Similarly the number of rows in the submatrix $\boldsymbol{S}_c$ defines the number of the new added virtual outgoing wave variables $\boldsymbol{b}_e$. The equivalent circuit represented by the extended scattering matrix $\boldsymbol{S}$ is shown in Figure 4.1.4. The virtual ports do not exist physically.

Three different configurations of multiports may arise. If the number of input ports n is smaller than the number of output ports m, then

$$\boldsymbol{S}_{21}^{e} = \begin{pmatrix} \boldsymbol{S}_{1} & \boldsymbol{0} \\ \boldsymbol{S}_{3} & \mathbb{1}_{m-n} \end{pmatrix}, \tag{4.1.13}$$

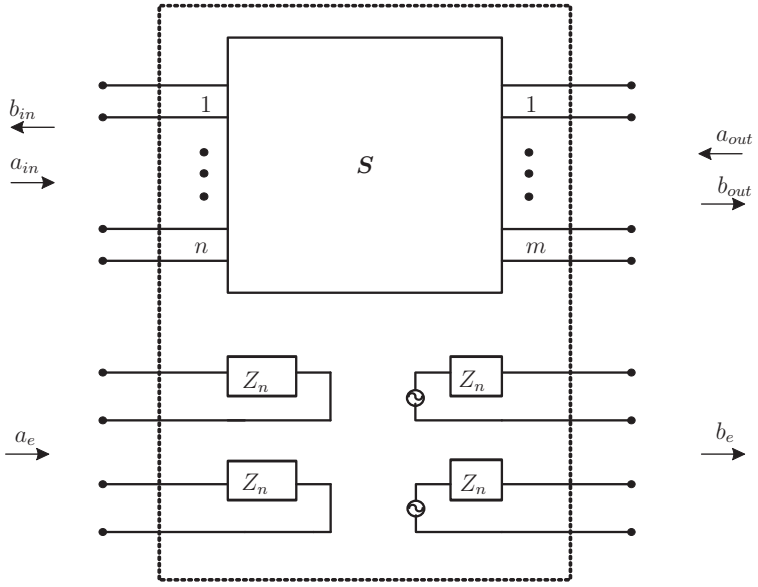


Figure 4.1.4: Extended network with virtual ports associated to the waves $\boldsymbol{a}_e$, and $\boldsymbol{b}_e$ [45]

where $\mathbb{1}_{m-n}$ is the $(m-n)\times(m-n)$ unit matrix, and the generalized transfer scattering matrix can be computed as

$$\begin{pmatrix} \boldsymbol{b}_{in} \\ \boldsymbol{a}_{in} \\ \boldsymbol{0} \end{pmatrix} = \begin{pmatrix} \boldsymbol{S}_{12} - \boldsymbol{S}_{11} \begin{pmatrix} \boldsymbol{S}_1^{-1} & \boldsymbol{0} \end{pmatrix} \boldsymbol{S}_{22} & \boldsymbol{S}_{11}\boldsymbol{S}_1^{-1} & \boldsymbol{0} \\ -\begin{pmatrix} \boldsymbol{S}_1^{-1} & \boldsymbol{0} \end{pmatrix} & \boldsymbol{S}_1^{-1} & \boldsymbol{0} \\ \begin{pmatrix} \boldsymbol{S}_3\boldsymbol{S}_1^{-1} & -\mathbb{1}_{n-m} \end{pmatrix} & -\boldsymbol{S}_3\boldsymbol{S}_1^{-1} & \mathbb{1} \end{pmatrix} \begin{pmatrix} \boldsymbol{a}_{out} \\ \boldsymbol{b}_{out} \end{pmatrix}. \tag{4.1.14}$$

In the case of equality, that's $n = m$, the submatrix does not need to be extended. If the number of input ports n is bigger than the number of output ports m, then

$$\boldsymbol{S}_{21}^e = \begin{pmatrix} \boldsymbol{S}_1 & \boldsymbol{S}_2 \\ \boldsymbol{0} & \mathbb{1}_{n-m} \end{pmatrix}, \tag{4.1.15}$$

and the generalized transfer scattering matrix is

$$\begin{pmatrix} \boldsymbol{b}_{in} \\ \boldsymbol{a}_{in} \end{pmatrix} = \begin{pmatrix} \boldsymbol{S}_{12} - \boldsymbol{S}_{11} \begin{pmatrix} \boldsymbol{S}_1^{-1} \\ \boldsymbol{0} \end{pmatrix} \boldsymbol{S}_{22} & \boldsymbol{S}_{11} \begin{pmatrix} \boldsymbol{S}_1^{-1} \\ \boldsymbol{0} \end{pmatrix} & \boldsymbol{S}_{11} \begin{pmatrix} \boldsymbol{S}_1^{-1}\boldsymbol{S}_2 \\ \mathbb{1} \end{pmatrix} \\ -\boldsymbol{S}_1^{-1}\boldsymbol{S}_{22} & \boldsymbol{S}_1^{-1} & -\boldsymbol{S}_1^{-1}\boldsymbol{S}_2 \\ \boldsymbol{0} & \boldsymbol{0} & \mathbb{1} \end{pmatrix} \begin{pmatrix} \boldsymbol{a}_{out} \\ \boldsymbol{b}_{out} \\ \boldsymbol{b}_e \end{pmatrix}. \tag{4.1.16}$$

For the analysis of cascaded microwave circuits composed of n-ports with the same port impedance, the input and output waves and the transfer scattering matrix may be re-

ordered to give

$$\begin{pmatrix} b_{in1} \\ a_{in1} \\ b_{in2} \\ a_{in2} \\ \vdots \\ 0 \end{pmatrix} = \boldsymbol{T} \begin{pmatrix} a_{out1} \\ b_{out1} \\ a_{out2} \\ b_{out2} \\ \vdots \\ b_{e1} \\ \vdots \\ b_{en-m} \end{pmatrix}.$$

The transfer scattering matrix method of a circuit with $2\,n$-ports is computed by the product of the transfer scattering matrices of the individual cascaded components it consists of. The generalized case of a cascaded connection of two multiports is shown in Figure 4.1.5.

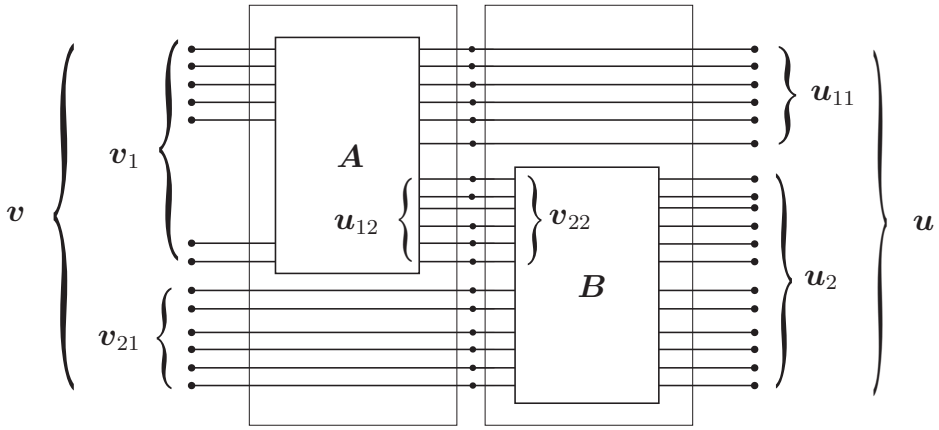


Figure 4.1.5: Generalized case of cascaded multiports [45]

In order to derive the transfer scattering matrix in the generalized case of cascaded two multiports, the following wave variables are introduced:

$\boldsymbol{v}_1 = (b_{in1}, a_{in1}, b_{in2}, a_{in2}, \ldots)^{\mathbf{T}}$: vector of wave variables at input ports of the first element,

$\boldsymbol{u}_{11} = (a_{out1}, b_{out1}, a_{out2}, b_{out2}, \ldots)^{\mathbf{T}}$: vector of wave variables at the first element output ports not connected with the input ports of the second element,

$\boldsymbol{u}_{12} = (a_{outn}, b_{outn}, a_{outn+1}, b_{outn+1}, \ldots)^{\mathbf{T}}$: vector of wave variables at the first element output ports connected with the appropriate input ports of the second element,

$\boldsymbol{v}_{22} = (a_{in1}, b_{in1}, a_{in2}, b_{in2}, \ldots)^{\mathbf{T}}$: vector of wave variables at the second element input ports connected with the appropriate output ports of the first element,

$\boldsymbol{v}_{21} = (a_{out1}, b_{in1}, a_{in1+1}, b_{in1+1}, \ldots)^{\mathbf{T}}$: vector of wave variables at the input ports of the second element,

$\boldsymbol{u}_2 = (a_{out1}, b_{out1}, a_{out1+1}, b_{in1+1}, \ldots)^{\mathbf{T}}$: vector of wave variables at output ports of the second element.

The transfer scattering matrix for the first element is

$$\begin{pmatrix} \boldsymbol{v}_1 \\ \mathbf{0}_1 \end{pmatrix} = \begin{pmatrix} \boldsymbol{A}_{11} & \boldsymbol{A}_{12} & \boldsymbol{A}_{1e} \\ \boldsymbol{A}_{01} & \boldsymbol{A}_{02} & \boldsymbol{A}_{0e} \end{pmatrix} \begin{pmatrix} \boldsymbol{u}_{11} \\ \boldsymbol{u}_{12} \\ \boldsymbol{b}_{e1} \end{pmatrix},$$

and for the second element

$$\begin{pmatrix} \boldsymbol{v}_{21} \\ \boldsymbol{v}_{22} \\ \mathbf{0}_2 \end{pmatrix} = \begin{pmatrix} \boldsymbol{B}_{11} & \boldsymbol{B}_{1e} \\ \boldsymbol{B}_{21} & \boldsymbol{B}_{2e} \\ \boldsymbol{B}_{01} & \boldsymbol{B}_{02} \end{pmatrix} \begin{pmatrix} \boldsymbol{u}_2 \\ \boldsymbol{b}_{e2} \end{pmatrix},$$

where $\mathbf{0}_1$, $\mathbf{0}_2$ are null vectors corresponding to the incoming waves at the additional virtual input ports, respectively, of the first and second elements, $\boldsymbol{b}_{e1}$, $\boldsymbol{b}_{e2}$ are vectors of the outgoing waves at the additional virtual output ports, respectively, of the first and second elements. The vectors of incoming and outgoing waves at input ports and output ports of the cascade are:

$\boldsymbol{v} = \left(\boldsymbol{v}_1^{\mathbf{T}}, \boldsymbol{v}_{21}^{\mathbf{T}}, \mathbf{0}_1^{\mathbf{T}}, \mathbf{0}_2^{\mathbf{T}}\right)^{\mathbf{T}}$

$\boldsymbol{u} = \left(\boldsymbol{u}_{11}^{\mathbf{T}}, \boldsymbol{u}_2^{\mathbf{T}}, \boldsymbol{b}_{e1}^{\mathbf{T}}, \boldsymbol{b}_{e2}^{\mathbf{T}}\right)^{\mathbf{T}}$

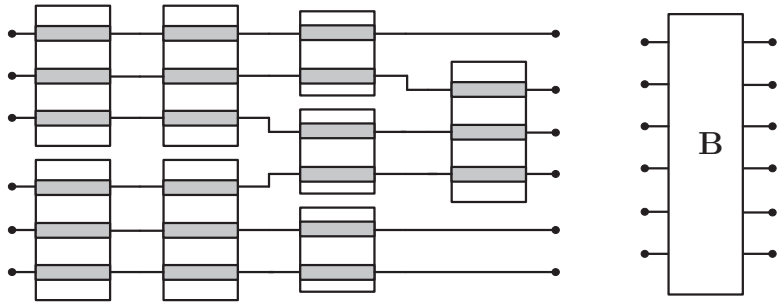
After reordering of the individual transfer scattering matrices and their multiplication, one gets the resulting transfer scattering matrix of the two cascaded multiports in Figure 4.1.5 as

$$\boldsymbol{T} = \begin{pmatrix} \boldsymbol{A}_{11} & \boldsymbol{A}_{12}\boldsymbol{B}_{21} & \boldsymbol{A}_{1e} & \boldsymbol{A}_{12}\boldsymbol{B}_{2e} \\ \mathbf{0} & \boldsymbol{B}_{11} & \mathbf{0} & \boldsymbol{B}_{1e} \\ \boldsymbol{A}_{01} & \boldsymbol{A}_{02}\boldsymbol{B}_{21} & \boldsymbol{A}_{0e} & \boldsymbol{A}_{02}\boldsymbol{B}_{2e} \\ \mathbf{0} & \boldsymbol{B}_{01} & \mathbf{0} & \boldsymbol{B}_{0e} \end{pmatrix}.$$

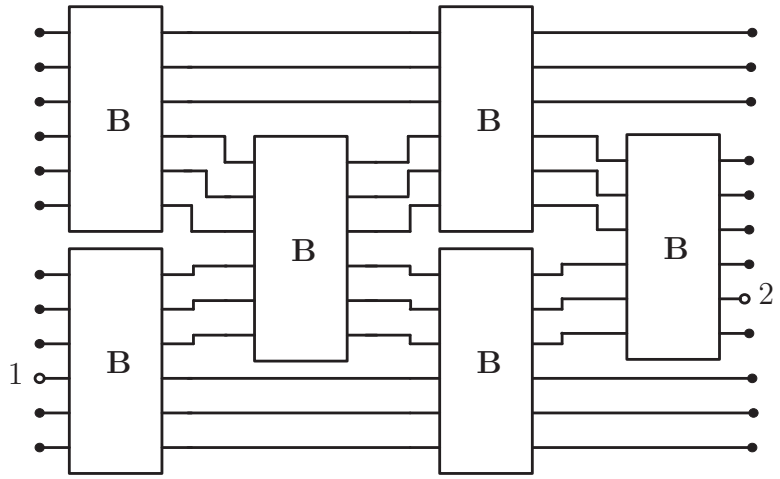
Application Example

The generalized transfer scattering matrix is applied to the single layer PCB shown in Figure 4.1.6. The subcircuit in Figure 4.1.6(a) consists of parallel microstrip lines mounted on a dielectric substrate of thickness 1 mm and with a relative permittivity of 4.3. This subcircuit, denoted **B**, is used to construct the cascaded circuit analyzed, which is depicted in Figure 4.1.6(b). The microstrip transmission lines and the ground plane, of finite thickness $100\,\mu m$, are assumed to be lossless. All the lines have the length l=4 cm. The widths of the microstrips and spacing between them have the same values within the individual structures. These values are 1 mm and 0.5 mm for the three and two coupled lines, respectively.

The microstrips structures are characterized using the HSPICE MoM solver. The parasitic coupling between the three-parallel lines is given by the following per unit length



(a)



(b)

Figure 4.1.6: Schematic of the studied cascaded structures: (a) subcircuit, (b) whole circuit

inductance and capacitance matrices

$$\boldsymbol{L} = \begin{pmatrix} 393.43 & 80.47 & 27.55 \\ 80.47 & 390.4 & 80.47 \\ 27.55 & 80.47 & 393.43 \end{pmatrix} \frac{\text{nH}}{\text{m}}, \quad \boldsymbol{C} = \begin{pmatrix} 85.26 & -9.39 & -0.73 \\ -9.39 & 86.64 & -9.39 \\ -0.73 & -9.39 & 85.26 \end{pmatrix} \frac{\text{pF}}{\text{m}},$$

whereas the two coupled lines are characterized by the parasitic inductance and capacitance matrices

$$\boldsymbol{L} = \begin{pmatrix} 499.70 & 176.91 \\ 176.91 & 499.70 \end{pmatrix} \frac{\text{nH}}{\text{m}}, \quad \boldsymbol{C} = \begin{pmatrix} 67.17 & -16.88 \\ -16.88 & 67.17 \end{pmatrix} \frac{\text{pF}}{\text{m}}.$$

The frequency domain response is determined in terms of the voltage transfer function between the terminals 1 and 2 specified in the circuit schematic. The transfer scattering matrix $\boldsymbol{T}$ of this circuit is computed and then converted into corresponding scattering matrix $\boldsymbol{S}$ in order to solve the voltage transfer function. The resulting response is compared with the frequency domain HSPICE circuit simulation. Figure 4.1.7 shows a good convergence between the results obtained by the generalized transfer scattering matrix and that of the HSPICE simulation.

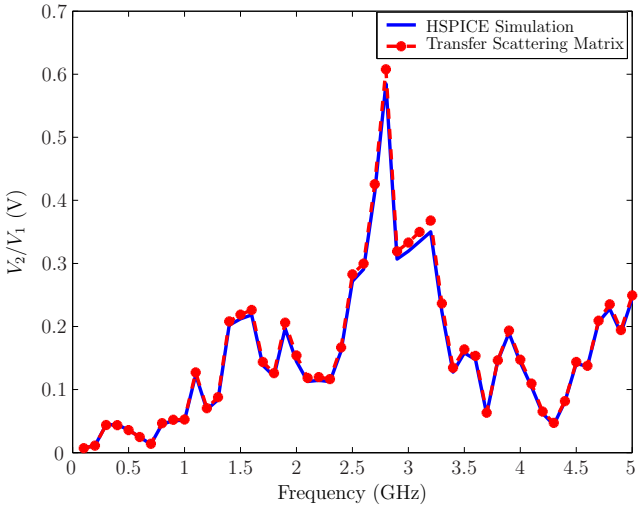


Figure 4.1.7: Far-end crosstalk voltage

4.1.4 Multiport Connection Method

The multiport connection method allows for the computation of large linear circuits using an iterative procedure. The circuit characteristics are computed considering at each step a part of the circuit. The size of the circuit decreases each step by the number of the internal ports in the subcircuit processed. Thus at the last step the number of the ports in resulting circuit equals the sum of the terminations and the number of the independent sources [45]. Figure 4.1.8 illustrates the concept of external and internal ports used by the multiport connection method.

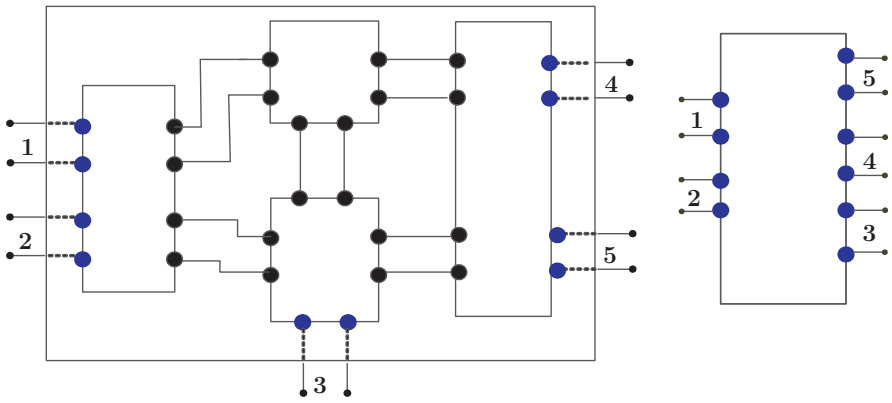


Figure 4.1.8: A subcircuit showing internal and external ports, and its equivalent multiport

When one or more independent generators are present in a network, these can be treated as existing outside the remaining network and the present method yields the scattering matrix for the network. This network contains i internal ports and e ports external to it. If there are m components in the network the governing relations for all components can be written together as

$$\boldsymbol{b} = \boldsymbol{S}\,\boldsymbol{a}. \tag{4.1.17}$$

The rows and columns in (4.1.17) can be reordered so that the wave variables are separated into two groups, the first corresponding to the e external ports, and the second to i internally connected ports. Equation (4.1.17) can now be written as

$$\begin{pmatrix} \boldsymbol{b}_e \\ \boldsymbol{b}_i \end{pmatrix} = \begin{pmatrix} \boldsymbol{S}_{ee} & \boldsymbol{S}_{ei} \\ \boldsymbol{S}_{ie} & \boldsymbol{S}_{ii} \end{pmatrix} \begin{pmatrix} \boldsymbol{a}_e \\ \boldsymbol{a}_i \end{pmatrix}, \tag{4.1.18}$$

where $\boldsymbol{b}_e$ and $\boldsymbol{a}_e$ are the vectors of the wave variables at the e external ports, and $\boldsymbol{b}_i$ and $\boldsymbol{a}_i$ are the the vectors of the wave variables at the internal ports. The interconnection constraints for the i internal ports can be written as

$$\boldsymbol{b}_i = \boldsymbol{P}\,\boldsymbol{a}_i, \tag{4.1.19}$$

where $\boldsymbol{P}$ is the connection matrix obtained in the same way as in Section 4.1.2. The manipulation of (4.1.18), and (4.1.19) gives the relation

$$\boldsymbol{P}\,\boldsymbol{a}_i = \boldsymbol{S}_{ie}\,\boldsymbol{a}_e + \boldsymbol{S}_{ii}\,\boldsymbol{a}_i.$$

The vector $\boldsymbol{a}_i$ can be computed as

$$\boldsymbol{a}_i = (\boldsymbol{P} - \boldsymbol{S}_{ii})^{-1}\ \boldsymbol{S}_{ie}\,\boldsymbol{a}_e. \tag{4.1.20}$$

The network scattering matrix $\boldsymbol{S}_e$ is then computed from (4.1.18) substituting the expression for $\boldsymbol{a}_i$ in (4.1.20). It is given by

$$\boldsymbol{S}_e = \boldsymbol{S}_{ee} + \boldsymbol{S}_{ei}\ (\boldsymbol{P} - \boldsymbol{S}_{ii})^{-1}\ \boldsymbol{S}_{ie}. \tag{4.1.21}$$

Equation (4.1.19) and (4.1.21) can be used to obtain the wave variables at the internal ports for any arbitrary excitation at the e external ports.

The multiport connection method, which uses the scattering parameters, is an analogous and iterative way to the indefinite admittance matrix described in Section 4.1.1. They differ only in the variable used. Both methods can be implemented to allow automatic computation of large circuits in the frequency domain. The pseudo-code of the algorithm developed is given by

Algorithm 4.1.1 MultiPort Connection Method

1: Compute circuit constraints: degree of nodes, adjacent components for each multiport
2: **repeat**
3: Select a multiport component with a maximum number of ports
4: Get its adjacent multiports and construct a current subcircuit
5: Compute the equivalent multiport matrix relating external ports of current
6: subcircuit
7: Update global netlist: remove components processed and update
8: connections
9: **until** number of multiports is 1

To make time domain simulation the resulting circuit matrix can be included in a HSPICE netlist.

Application Example

Figure 4.1.9 shows a microstrip line circuit analyzed using the multiport connection method. The microstrip traces (of width 200 μm and height 35 μm) are separated by a space of 200 μm above a FR4 ($\varepsilon_r = 4.2$) dielectric substrate of 365 μm height. The length of all the transmission lines is 3 cm. The microstrip lines are characterized over the frequency range of 1 GHz. The termination resistances $R_1, ..., R_{15}$ are chosen to be 50 Ω.

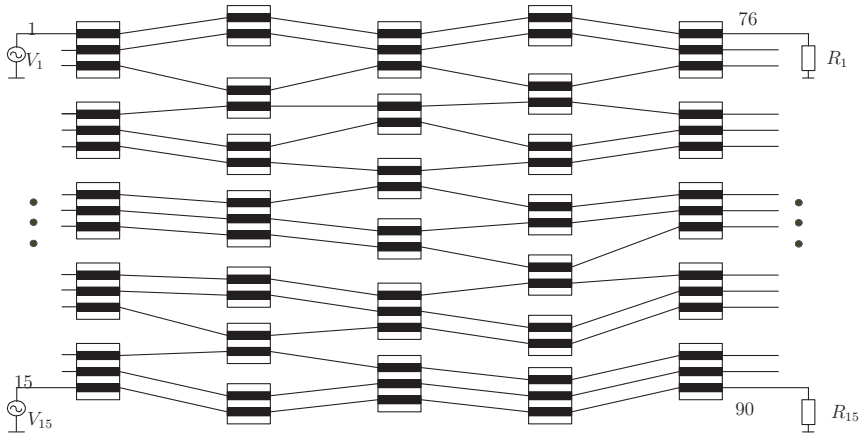


Figure 4.1.9: Example of interconnect circuit

The voltage phasor at the node 90 is computed over the frequency bandwidth of 1 GHz. That's the voltage response corresponding to a *Dirac* impulse response applied at the sources. Obviously, and as shown in Figure 4.1.10 the curves representing the magnitude and phase responses determined using the multiport connection method are identical to that provided by the circuit simulator HSPICE.

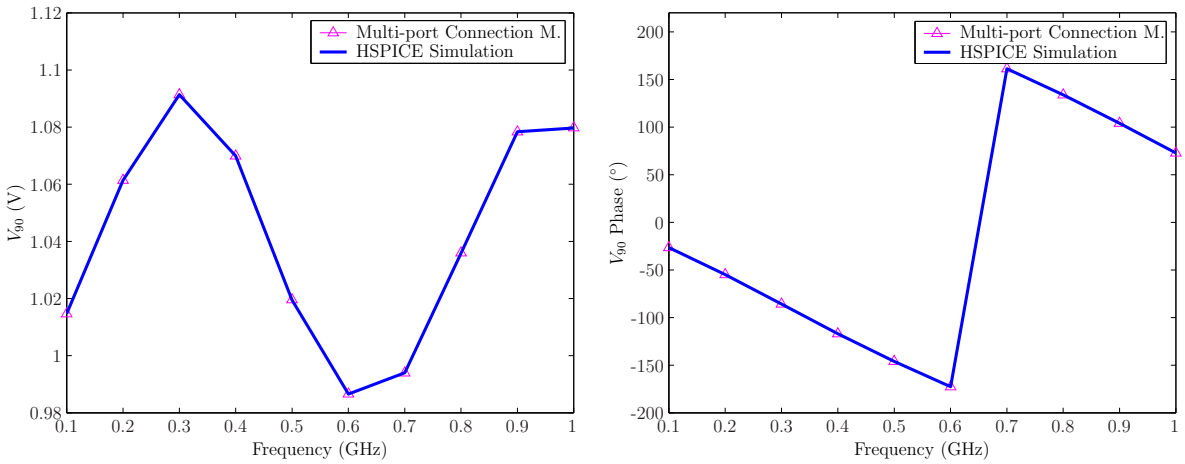


Figure 4.1.10: Magnitude and phase of the transfer function at node 90

To investigate in the time domain analysis of this circuit with digital components the resistive loads are replaced by 5 V CMOS inverters SN74LV04A of Texas Instruments [57]. The

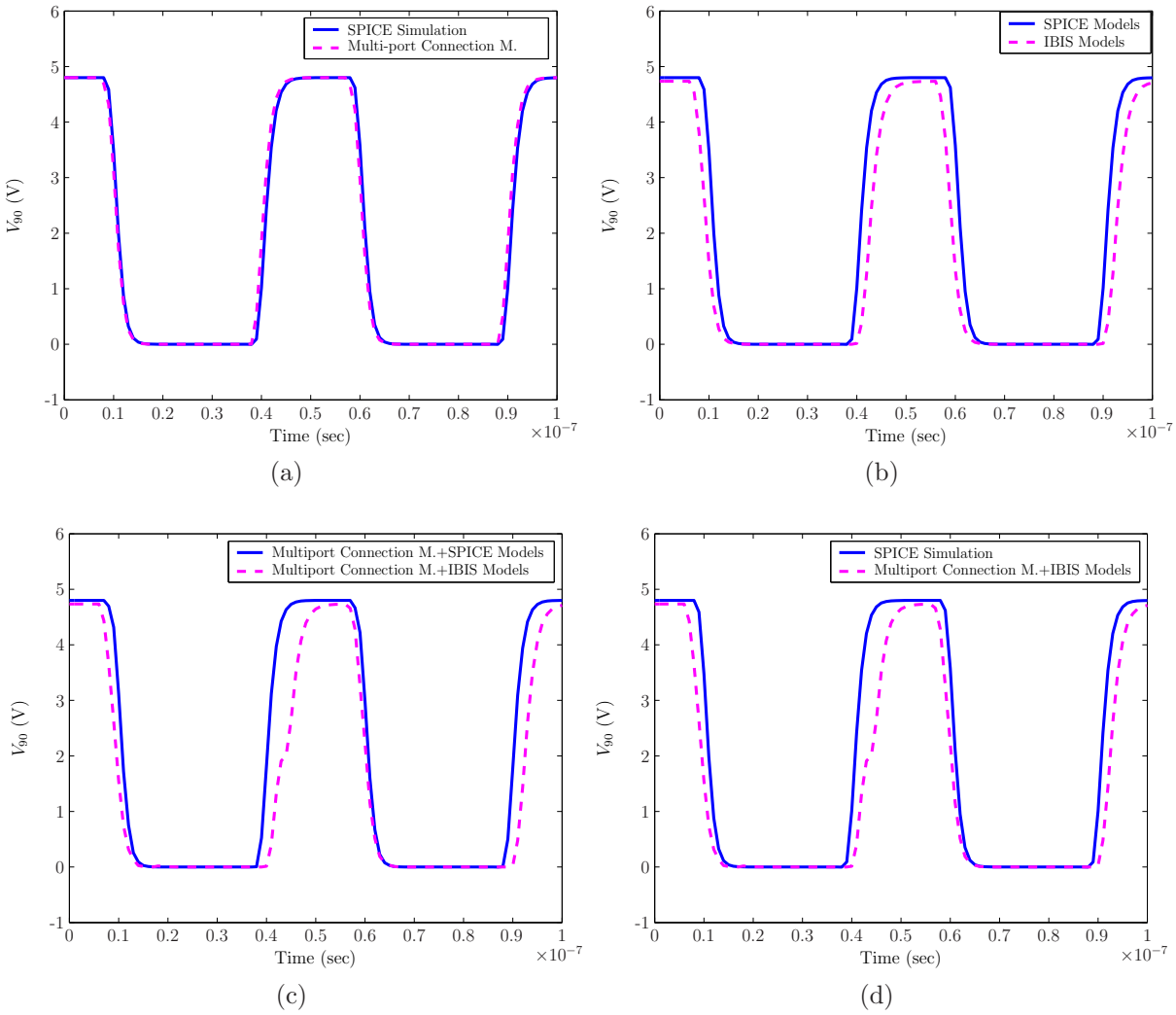


Figure 4.1.11: Time domain response at node 90

output ports of these inverters are loaded by parallel circuits RC (R= 500Ω , C=50 pF). The voltage sources are trapezoidal waves with transition times of 5 ns, widths of 25 ns, and periods of 50 ns. The frequency domain data characterizing the linear circuit part can be combined with SPICE or IBIS models of the inverter buffers. The time domain responses of combining the conventional SPICE circuit analysis, the multiport connection method, the SPICE and IBIS models of the inverter are depicted in Figure 4.1.11.

In Figure 4.1.11(a) the SPICE time domain analysis of the circuit is compared with the multiport connection method combined under the use of SPICE macromodels of the buffers. In Figure 4.1.11(b) the SPICE transient analysis is represented for both SPICE and IBIS models. In Figure 4.1.11(c) the results of the multiport connection method combined with SPICE and IBIS models are compared. In Figure 4.1.11(d) the SPICE analysis is compared to the multiport connection method combined with IBIS models. For all these cases the curves representing the results of all the combinations of the methods and models are close to each others.

An important factor in the choice of the simulation method is the efficiency. For this

purpose the speed of all the combinations analyzed in Figure 4.1.11 is computed on a Sun SPARC Station with 2 processors of 359 MHz. The run time required for each simulation is given in Table 4.1.1. It is clear that the simulation considering the whole circuit matrix and transistor level model requires not only large memory resources, but also more CPU time (110.5 sec), whereas the use of the multiport connection method in a preprocessing step can save a lot of memory resources. The use of IBIS behavioural models of the inverter buffers leads to significant efficiency increase with comparison to the conventional time domain analysis (21.3 sec).

	SPICE Transient Analysis	Multiport Connection Method
SPICE Macromodels	110.5 sec	51.2 sec
IBIS Models	33.2 sec	21.3 sec

Table 4.1.1: Average CPU time for different combinations of methods and models

4.2 Circuit Analysis by Signal Flow Graphs

Another way to represent an electrical network is the graph model. The behaviour of an electrical network can be analyzed by observing and solving the relevant properties of the corresponding graphs. There exist different types of graphs to model an electrical network depending on the physical quantities considered and the topology in which the components are connected. In this section basic concepts and terms in graph theory, that are of great importance for the derivation of a signal tracing approach, have been introduced and discussed [58, 59].

4.2.1 Basic Notions on Graphs

A graph $G' = (V', E')$ is a simple structure consisting of a finite set of vertices $V' = \{v'_1, v'_2, ...\}$ and a set of edges $E' = \{e'_1, e'_2, ...\}$, such that each edge e'_k is identified by an unordered pair (v'_i, v'_j) of vertices. The number of vertices is denoted by n and the number of edges is denoted by m. The vertices v'_i, and v'_j associated with the edge e'_k are called the end vertices of e'_k. An edge which has the same vertex as both its end vertices is called a self-loop. Each pair of vertices may be connected by many edges called parallel edges. A graph G' is said to be weighted if there is a real number associated with each edge of G'. A graph is named directed, or digraph, if the edges are assigned a direction. This is represented by their arrows in the graph. Throughout this thesis the terminology of directed graphs is defined.

In directed graphs an edge is incident into or incident out of a vertex. The vertex v'_i, which edge e'_k is incident out of, is called the initial vertex of e'_k. The vertex v'_j, which edge e'_k is incident into, is called the terminal vertex of e'_k. An edge for which the initial and terminal vertices are the same forms a self-loop. The number of edges incident out of a vertex v'_i is called the out-degree of v'_i. The number of edges incident into a vertex

v_i' is called the in-degree of v_i'. If the in-degree of every vertex v_i' equals its out-degree, the graph is called balanced. A digraph H' is said to be a subgraph, smaller portion, of a graph G' if all the vertices and all the edges of H' are in G', and each edge of H' has the same vertices in H' as in G'. Two subgraphs H_1' and H_2' of a graph G' are said to be edge disjoint if they do not have any edges in common, but they may have vertices in common. Subgraphs that do not have vertices in common are said to be vertex disjoint.

A walk is defined by a set of sequence of vertices and edges, beginning and ending with vertices, such that each edge is incident with the vertices preceding and following it. In a walk no edge appears more than once. A walk is named a simple path if no vertex appears more than once. That means a path does not intersect itself. The vertices with which a path begins and ends are called its terminal vertices. In digraphs the path is associated an orientation, such that each edge is oriented from the vertex preceding it to the vertex following it. In a weighted graph the length of a path is defined by the sum of the weights of all edges belonging to this path. A circuit is a walk in which the first and last vertices are the same. A directed graph which does not contain a circuit is called acyclic graph.

A graph G' is connected if we can reach any vertex from any other vertex by traveling along the edges. In other words there is at least one path between every pair of vertices in G'. In a connected graph the distance $d(v_i', v_j')$ between two of its vertices v_i', and v_j' is the length of the shortest path connecting them. A disconnected graph consists of many connected graphs each of these disjoint subgraphs is called a component.

An important term in graph theory is the notion of a tree. A tree is a simple connected graph without any circuits, i.e. having neither a self-loop nor parallel edges. There is only one path between every pair of vertices in a tree. In a graph that is not a tree, there are generally several paths between a pair of vertices. A special case of a tree is a rooted tree with a start vertex which is distinguished from the other vertices. A straightforward application of trees is in search procedures.

In many applications of graph theory, such as in electrical network analysis, matrices are used to store the topology of a graph and then analyze the problem. A matrix representation is a useful tool to investigate the properties of a graph by means of a digital computer. Examples of such matrices are the incidence and the adjacency matrices.

A special type of a directed graph is the signal flow graph (SFG). It is used in the past in control theory. In this thesis signal flow graphs are used to represent the parasitic coupling paths between the ports of the transmission structures in a passive linear network.

4.2.2 Signal Flow Graphs

The analysis of linear systems is eventually reduced to solving the corresponding set of simultaneous linear equations. Alternative methods to the matrix methods are based on SFGs that contain the same information as the equations from which it is derived. The analysis of such linear systems consists of generating of a corresponding SFG and then solving for the required dependent variable. By the construction vertices are labelled and edges $\{e_1', e_2', ..., e_m'\}$ are associated appropriate weights. Usually in a SFG, the vertices

$\{v'_1, v'_2, ..., v'_m\}$ are directly represented by signal variables $\{x_1, x_2, ..., x_m\}$ in the equations. An edge from x_i to x_j means that variable x_j depends on variable x_i. The dependency is expressed by the direction of the edges. The coefficients in the equations are assigned as the weights of the edges, such that the variable x_k is equal to the sum of all products $w_{ik}\, x_i$ where w_{ik} is the weight of the edge coming into x_k from x_i. Signals travel along the edges and are multiplied by the weights of the edges traversed. The variable x_j equals all incoming signals, and is the strength of the signal in each outgoing edge from x_j. The weights in signal flow graphs are called the edge gains, and independent vertices are referred to as sources. Each vertex x_k represents one equation of the system in which x_k is the sum of the products of the weights of all incoming edges and the labels of the initial vertices of these edges. A vertex x_i is a sink if no edges originate from x_i. A vertex x_i is a source if no edges terminates at x_i. A sink x_i is an input if only one edge originates from it. A source x_i is an output if only one edge terminates at x_i. It is in many applications very interesting to solve for one unknown variable as a function of another independent variable. In general this procedure requires the manipulation of the edges and vertices of the SFG so that a simplified graph is obtained. The four elementary rules to reduce a SFG are shown in Figure 4.2.1.

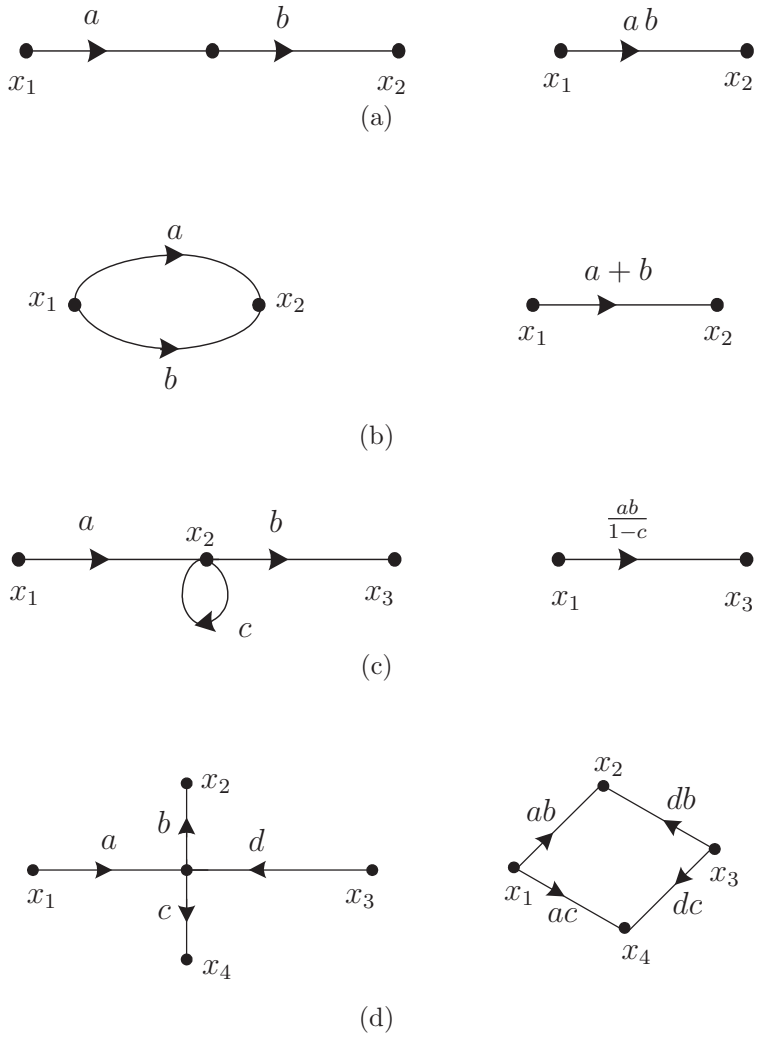


Figure 4.2.1: Signal flow graph reduction rules

By the series rule in Figure 4.2.1(a) the edge weights of two successive edges in series can be combined into one edge by multiplying their individual weights. When multiple edges connecting the same two vertices exist, the associated edge weights can be added as shown in Figure 4.2.1(b). A loop with the gain c, as shown in Figure 4.2.1(c), can be eliminated if all other edges into the vertices are devided by the factor $(1 - c)$. A vertex with multiple input or output edges can be split into multiple equivalent vertices with each of the separate input edges connected to the new vertices provided that each new vertex contains all of the output edges. Similarly, the vertices will be equivalent if each new vertex connects to each of the original output edges provided that each new vertex is connected to all of the original input edges as depicted in Figure 4.2.1(d).

To determine the transfer function from a SFG applying these reduction rules requires visual inspection on the graph. An alternative method which does not depend on visual inspection is the Matrix from of *Mason*'s gain rule. It is based on the determination of directed paths and their associated transfer functions.

Within this thesis the flow of parasitic noise is determined on the basis of signal propagation paths. These paths include all coupling subpaths relating the ports of the individual network structures. The electrical network, assumed to be linear, consisting of transmission lines and passive discrete components are represented by their SFGs. The individual subgraphs are concatenated to build the whole network. The network elements are represented by asymmetrical SFGs. That means vertices are joined by most one edge and there is no self-loop in the signal flow graph. The edges of the graph are associated real weights computed using a metric depending on electrical properties of the components. The vertices represent the electrical signals, like waves, and voltages, that have to be determined. For the analysis of microwave networks usually the flow of the power, expressed in terms of transmitted and reflected power waves, is used. A four-port network, characterized by its scattering parameter matrix $\boldsymbol{S}$, and the corresponding SFG are depicted in Figure 4.2.2.

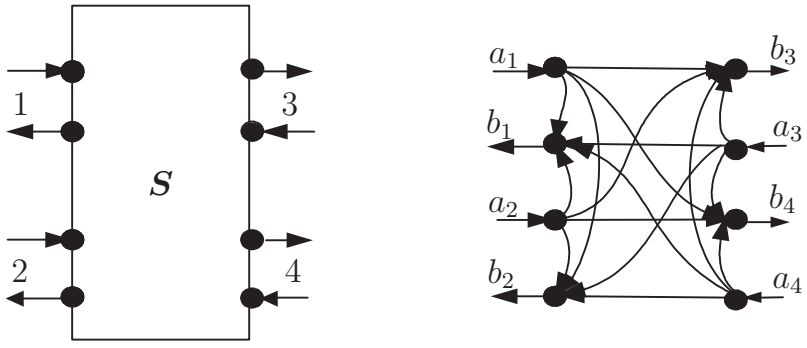


Figure 4.2.2: A four-port network and its associated signal flow graph

4.2.3 Transfer Function in Signal Flow Graphs

Mason's rule is a way to determine the transfer function between any input and any output vertices in a SFG. The transfer function can be derived by studying the features

of the SFG representing the microwave network. There are two variants of this formula. The first variant is based on the determination of the circuits, i.e. cycles, and the paths in the network graph. The second however, requires only the determination of the simple paths, which are sufficient to derive the transfer function using the associated network subgraphs, or submatrices [58].

Signal flow graphs representing a microwave network containing many transmission structures characterized by their multiports parameters consist of big number of cycles and paths. The determination and storage of all these features, using the first variant, seems to be a difficult task when analyzing large circuits with complex topology. In this section the second variant representing an alternative procedure, which requires only the knowledge of the paths, is described.

To derive the transfer function between two vertices in a SFG the set of linear equations describing the network should be written in a matrix. For this purpose consider a signal flow graph G' with vertices $x_1, ..., x_n$ and source vertices $y_1, ..., y_n$ representing the external signals at the vertices $x_i, i = 1, ..., n$. There exist different representations of the network equations depending on the order in which the variables x_i, and $y_i, i = 1, ..., n$ are written. A particular type of the set of linear equations representing the graph G' is defined by

$$\begin{array}{c} (1 - w_{11})x_1 - w_{12}x_2 - ... - w_{1n}x_n = y_1 \\ -w_{21}x_1 + (1 - w_{22})x_2 - ... - w_{2n}x_n = y_2 \\ \vdots \\ -w_{n1}x_1 - w_{n2}x_2 - ... + (1 - w_{nn})x_n = y_n \end{array} \tag{4.2.1}$$

In this equation the coefficients $w_{ij} \in \mathbb{C}, i, j = 1, ..., n$. Since the SFG of a microwave network does not consist of self-loops, w_{ii}=0, for $i = 1, ..., n$. Under this condition, the matrix corresponding to (4.2.1), which is named the structure matrix of the signal flow graph G', is given by

$$\begin{pmatrix} 1 & -w_{12} & \dots & -w_{1n} \\ -w_{21} & 1 & \dots & -w_{2n} \\ \dots & \dots & \ddots & \vdots \\ -w_{n1} & -w_{n2} & \dots & 1 \end{pmatrix}. \tag{4.2.2}$$

This matrix represents all states of the network. The solution of this system of equations provides the values of the waves at the corresponding vertices of the graph. A trivial solution can be obtained using the Gaussian elimination. In the case where the ratio of an output variable to an input one is required the *Cramer*'s method can be used. Another way to compute this ratio, keeping the information on signal flow, is the combination of graph and matrix approaches. The cofactor of each path $\mathcal{P}$ in the signal flow graph G' is defined by the determinant of the underlying subgraph without the vertices belonging to $\mathcal{P}$. It is denoted by

$$\Delta_{\mathcal{P}} = det(G', \mathcal{P}).$$

Each directed simple path $\mathcal{P}$ in a SFG is associated a gain denoted $H_{\mathcal{P}}$, which is the product of all edge gains, i.e. weights, belonging to this path. For a path $\mathcal{P}$ consisting of

the sequence of vertices $x_1, x_2, ..., x_N$ and connected by the edges with weights $w_{i,i+1}$, the path gain is defined as

$$H_{\mathcal{P}} = \prod_{i=1}^{N-1} w_{i,j+1}. \tag{4.2.3}$$

The transfer function between any input and output nodes of a SFG can be determined by computing of the directed paths and associated cycle gains. For an input vertex x_1 and for each other vertex $x_j, j = 2, ..., n$ in the graph G', the ratio of the signal variables at both vertices x_j and x_1 is expressed in terms of all directed paths $Path_{j1}$ relating these vertices. It is defined as

$$x_j = \sum_{\mathcal{P} \in Path_{j1}} \frac{H_{\mathcal{P}}\, \Delta_{\mathcal{P}}}{\Delta}\, x_1, \tag{4.2.4}$$

where Δ is the determinant of the structure matrix representing the signal flow graph.

Consequently, the solution of the system of equations consists of determining the determinant of the whole matrix, and for each path the path gain and the determinant of the modified network matrix after removing the vertices belonging to this path. In the case of multiple inputs $y_1, y_2, ..., y_k$, (4.2.4) can be applied for each input separately and the resulting expression for an output node x_j is then of the form

$$x_j = \sum_{i=1}^{k} T_{ji}\, y_i, \tag{4.2.5}$$

where

$$T_{ji} = \sum_{\mathcal{P} \in Path_{ji}} \frac{H_{\mathcal{P}}\, \Delta_{\mathcal{P}}}{\Delta}, \tag{4.2.6}$$

is the graph transmittance from the input y_i to the vertex x_j.

Throughout this thesis the transfer scattering matrix and multiport connection methods described in subsections 4.1.3 and 4.1.4 can be used as validation methods for the signal propagation paths. The transfer scattering matrix is preferred when the problem is characterized by a simple topology. However, the multiport connection method is able to analyze large interconnect circuits with complex topologies.

The expression of the transfer function given by (4.2.4) seems to complex if applied to large circuits with a big number of paths. In order to compute the transfer function between any two pair of vertices in a SFG all directed simple paths connecting these vertices have to be determined. The cycle gains of the subgraphs associated to these paths can be easily computed from the determinants of corresponding submatrices. The determination of all paths still represent a hard problem in graph theory. In the next section efficient algorithms are used to identify only the weighted simple paths, and therefore to compute an approximation of the transfer function.

Chapter 5

Approach to Noise Path Tracing

The *Mason*'s formula described in Section 4.2.3 for the analysis of an electrical network by its associating signal flow graph requires the determination of all signal paths connecting the input and output vertices, called also the source and target vertices respectively. As the computation of all paths in a graph is complex problem, shortest paths algorithms can be introduced to identify only a few weighted signal paths which give a good approximation to the total transfer function. In such a way the noise flow can be determined efficiently.

5.1 Shortest Paths Algorithms

Shortest paths algorithms are used in operation research and computer science to search for an optimal path in various applications [59]. The variant of algorithms used here is limited to the determination of simple shortest paths in directed graphs, i.e. without cycles of repeated vertices. The objective is to compute, for each vertex v' reachable from the source vertex s', the weight of a minimum-weight path from s' to v'. The weight of a path is the sum of the weights of its edges.

There exist a variety of simple shortest paths algorithms for specific applications. The first category allows the identification of the shortest paths from a single specified source vertex to another specified vertex, or to all vertices, in the graph. The second category deals with the determination of all shortest paths between any pair of vertices. The third category is the k-shortest paths algorithms which focus on the computation of many shortest paths connecting a given source-destination pair of vertices in the graph with minimum total lengths [60, 61, 62, 63]. In the next sections two examples of the most efficient algorithms belonging to the first and third categories are described. The first one is the single source shortest path algorithm of *Dijkstra*. The second one is the k-shortest paths algorithm of *Hershberger* et al. [63].

5.1.1 Single Source Shortest Path Algorithms

Different algorithms have been proposed in literature to solve shortest path problems in directed graphs. Most of these types are developed to deal with particular graphs depending on their structure and size. In this section single shortest path algorithm of *Dijkstra* is described. It is mainly used to solve routing problems for different applications [59].

Given a directed graph $G' = (V', E')$ with vertex set V' and edge set E'. Each edge $e' = (u', v') \in E'$ has a positive real edge weight or cost $c(u', v') \geq 0$. The number of vertices and edges in the graph G' are denoted n and m respectively. A source vertex s' and a destination vertex t', assumed to be different from s', are specified, for which the shortest path is to be defined. The shortest path between two vertices v'_1 and v'_q in G' is defined as the path $\mathcal{P} = \{v'_1, v'_2, ..., v'_q\}$ such that the sum over all $c(v'_i, v'_{i+1})$, for $i = 1, ..., q-1$, is minimum. Its length is denoted by $d(v'_1, v'_q)$.

Dijkstra's algorithm is based on labeling the vertices of the given graph. That means each vertex is associated a positive value d which represents its distance from the source s'. At each step of the algorithm some vertices have permanent labels and others temporary labels. The permanent labels indicate the shortest distance from the source s' to their associated vertices. The algorithm starts with an initialization step by assigning a permanent label 0 to the source vertex s', and a temporary label ∞, i.e. infinite distance, to the remaining vertices. In each iteration the adjacent vertices of the permanent label are updated according to the following rules:

1. Every vertex v' that is not yet permanently labeled gets a new temporary label whose value is given by

   $$min[d(s', v'), (d(s', u') + c(u', v'))],$$

   where, u' is the last vertex permanently labeled, in the previous iteration, and $c(u', v')$ is the weight of the edge constructed from the vertices u' and v'. If u' and v' are not joined by an edge, then $c(u', v') = \infty$.

2. The smallest value among all the temporary labels is found, and this becomes the permanent label of the corresponding vertex. In the case of many candidate labels, one of them is selected as permanent label.

The first vertex to be permanently labeled is at a distance of zero from s'. The second vertex to get a permanent label, from the set of remaining vertices, is the vertex closest to s'. The next vertex to be permanently labeled is the second closest vertex to s'. The permanent label of each vertex is the shortest distance of that vertex from the source s'. This procedure is repeated until the destination vertex t' gets a permanent label. As an illustration of *Dijkstra*'s algorithm the digraph in Figure 5.1.1 is considered.

The labeling procedure is applied to the directed graph in Figure 5.1.1 to compute the shortest distance from the source vertex A to the vertex F. Table 5.1.1 shows the algorithm steps needed to get the solution.

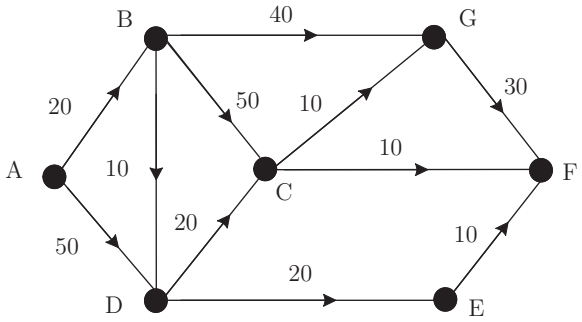


Figure 5.1.1: A directed graph example to illustrate *Dijkstra*'s single shortest path algorithm

The first line in this table represents the initialization step, where only the source vertex is reached. The vertex that gets permanent label at each step is indicated with a superscript (*) at its label. The distances to the remaining vertices are recomputed using the vertex permanently labeled.

The shortest path can be determined by recording the vertices from which each vertex was labeled permanently. If the shortest path from the starting vertex s' to each vertex is determined, then these paths may be represented by a rooted tree at s', called shortest-distance arborescence.

A	B	C	D	E	F	G
0	∞	∞	∞	∞	∞	∞
0^*	20	∞	50	∞	∞	∞
0	20^*	∞	50	∞	∞	∞
0	20	70	30^*	∞	∞	60
0	20	50^*	30	50	∞	60
0	20	50	30	50^*	60	60
0	20	50	30	50	60	60^*
0	20	50	30	50	60^*	60
0	20	50	30	50	60	60

Table 5.1.1: Steps for the determination of a shortest path by *Dijkstra*'s algorithm

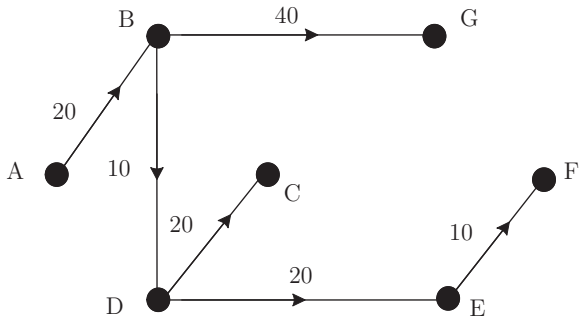


Figure 5.1.2: Shortest paths arborescence for the graph in Figure 5.1.1

There exist a variety of implementations of *Dijkstra*'s algorithm which uses different data

structures. The asymptotic time complexity of *Dijkstra*'s algorithm depends on the choice of the priority queue used for storing and handling the edges and vertices. Especially the time required to perform some operations like insertion and deletion for different heaps dominates this complexity. For general graphs, the use of Fibonacci heaps still provide the best theoretical worst-case time of $O(m+n \log n)$ using an adjacency list to represent the graph data structure. For sparse graphs, binary heaps are more efficient and result in the same asymptotic time complexity. A pseudo-code describing this algorithm is given bellow.

Algorithm 5.1.1 DIJKSTRA's Algorithm

Input: Graph $G' = (V', E', c)$, $c(u', v') > 0$, start and target nodes (s', t')
Initialization: $d(s') = 0$, $d(v') = \infty$ for each $v' \neq s'$, $Q = \{s'\}$
repeat:
    Select a node h' from Q with minimum $d(h')$
    for each adjacent vertex v' of h', with v' not yet visited **do**
        if $d(h') + c(h', v') < d(v')$ **then**
            $d(v') = d(h') + c(h', v')$
            $Q = Q \cup \{v'\}$
        end if
    end for
    $Q = Q \backslash \{h'\}$
until $Q = \emptyset$

5.1.2 K-Shortest Simple Paths Algorithms

In many applications a number of simple shortest paths is to be computed. That is, not only the shortest path is to be determined, but also the second shortest, the third shortest, and so up to the k-th shortest path. The paths are determined in increasing order of their lengths, i.e. distance from the source. A comparative study of the algorithms that solve the k-shortest path problems is provided in literature [61]. The recent algorithm used in this thesis is the most efficient one developed by *Hershberger* et al. [63].

Given a directed graph $G' = (V', E')$ with vertex set V' and edge set E'. Each edge $e' \in E'$ has a real positive weight $c(e') > 0$. The sizes of the sets V' and E' are m and n respectively. A start vertex s' and a target vertex t' are specified for which k simple shortest paths have to be determined. The shortest path between the vertices s' and t' is denoted here by $path(s', t')$.

The k-shortest path problem consists of the determination of a set $\mathcal{P}(k) = \{\mathcal{P}_1, ..., \mathcal{P}_k\}$ of simple paths, assuming at least one exists, between the vertices s' and t' when the objective function, i.e. the weight, of the shortest path problem is considered and in such a way that

$$d(\mathcal{P}_k) \leq d(\mathcal{P}), \text{for any } \mathcal{P} \in Path_{s't'} - \mathcal{P}(k-1),$$

where $Path_{s't'}$ is the set of all paths between s' and t', and $\mathcal{P}(0)$ is the empty set.

The algorithm in [63] is based on the application of single shortest path algorithms in subgraphs and an efficient best replacement path algorithm. The paths already determined are stored in a rooted tree called the path *branching structure*. The nodes and branches of this branching structure are associated *equivalence classes* which define the subgraphs in which the next candidate shortest paths should be determined.

For a set $\mathcal{P}(i) = \{\mathcal{P}_1, \mathcal{P}_2, ..., \mathcal{P}_i\}$ of first i generated shortest paths a set $\mathcal{R}_i$ of candidate paths connecting s' to t' is defined. The set $\mathcal{R}_i$ contains the remaining $k - i$ candidate shortest paths. This set is partitioned into equivalence classes in order to find the next shortest path in $\mathcal{R}_i$ efficiently. The first i shortest paths are encoded in a branching structure, denoted $\mathcal{T}_i$, that shows how these deviate from each other. The equivalence classes are related to this branching structure.

The branching structure $\mathcal{T}_i$ is constructed in a recursive way from the parameters $(s', \mathcal{P}(i))$, where s' is the fixed source and $\mathcal{P}(i) = \{\mathcal{P}_1, \mathcal{P}_2, ..., \mathcal{P}_i\}$ is the set of the first i shortest paths. $\mathcal{T}_i$ is initialized to the root node s'. At each step the longest prefix path of the paths in $\mathcal{P}(i)$ is considered. If $(s', a', b', ..., u')$ is the longest subpath that is a common prefix of all the paths in $\mathcal{P}(i)$, then the branching structure $\mathcal{T}_i$ is expanded by adding a node labeled u', which is the child of s', and creating the branch (s', u').

The set of paths $\{\mathcal{P}_1, \mathcal{P}_2, ..., \mathcal{P}_i\}$ is called the *path bundle* of the branch (s', u') and denoted by $\mathcal{B}(s', u')$. This path bundle $\mathcal{B}(s', u')$ will be partitioned into sets $\mathcal{S}_1, \mathcal{S}_2, ..., \mathcal{S}_n$ such that all paths in a given set $\mathcal{S}_j$, $j = 1, ..., n$, follow the same edge after u', and paths in different sets follow distinct edges. This procedure is illustrated in Figure 5.1.3.

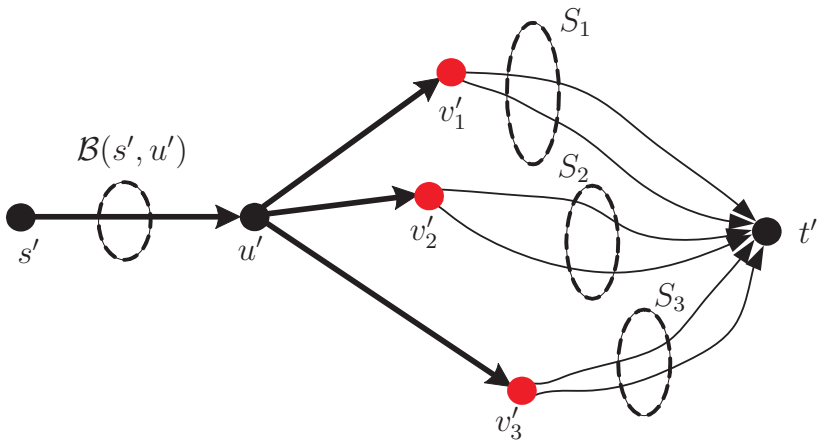


Figure 5.1.3: Path bundle of a branch (s',u')

The construction of the branching structure $\mathcal{T}_i$ is made by recursive calls $(u', \mathcal{S}_j)$, for $j = 1, ..., n$, until the path set $\mathcal{S}_j$ contains only a single path $\mathcal{P}$, i.e. $|\mathcal{S}_j| = 1$. This path is represented in the branching structure by a leaf node labeled $t_{\mathcal{P}}$.

For any given node u' in the branching structure $\mathcal{T}_i$ a prefix path $prefixPath(u')$ is defined. It is formed from the concatenation of all the branches from s' to u'. Therefore the shortest path $\mathcal{P}$ for a leaf node $t_{\mathcal{P}}$ is equal to $prefixPath(t_{\mathcal{P}})$. Each branch (u', v') in the branching structure $\mathcal{T}_i$ has a path bundle $\mathcal{B}(u', v')$ associated with it, and which consists of all the paths that terminate at leaf descendants of v'. For any branch (u', v')

in $\mathcal{T}_i$ there is a path in G' associated with it, and denoted by $branchPath(u', v')$. This is the path connecting the vertices u' and v' and which is shared by all the paths in $\mathcal{B}(u', v')$. The first edge of $branchPath(u', v')$ is called the lead edge of the path, denoted $\mathcal{L}(u', v')$.

The equivalence classes of candidate paths are associated with the nodes and branches of $\mathcal{T}_i$. Each non-leaf node $u' \in \mathcal{T}_i$ is associated an equivalence class $\mathcal{C}(u')$. If the node u' has n children in $\mathcal{T}_i$ labeled $v'_1, v'_2, ..., v'_n$, then an equivalence class $\mathcal{C}(u', v'_j)$ is associated with each branch out of u'. The class $\mathcal{C}(u')$ consists of the paths that overlap with each $prefixPath(v'_j)$ up to u', and branch off at u' using an other edge that is distinct from any of the lead edges $\mathcal{L}(u', v'_j)$, for $j = 1, 2, ..., n$. The class $\mathcal{C}(u', v'_j)$ consists of the candidate paths that coincide with the paths in $prefixPath(v'_j)$ up to and including the lead edge $\mathcal{L}(u', v'_j)$, but branch off before v'_j. That is, the paths of $\mathcal{C}(u', v'_j)$ diverges from $prefixPath(v'_j)$ between u' and v'_j. The equivalence partition associated with the path branching structure $\mathcal{T}_i$ is the collection of these sets over all branches and non-leaf nodes of $\mathcal{T}_i$. The notion of node and branch equivalence classes is illustrated in Figure 5.1.4.

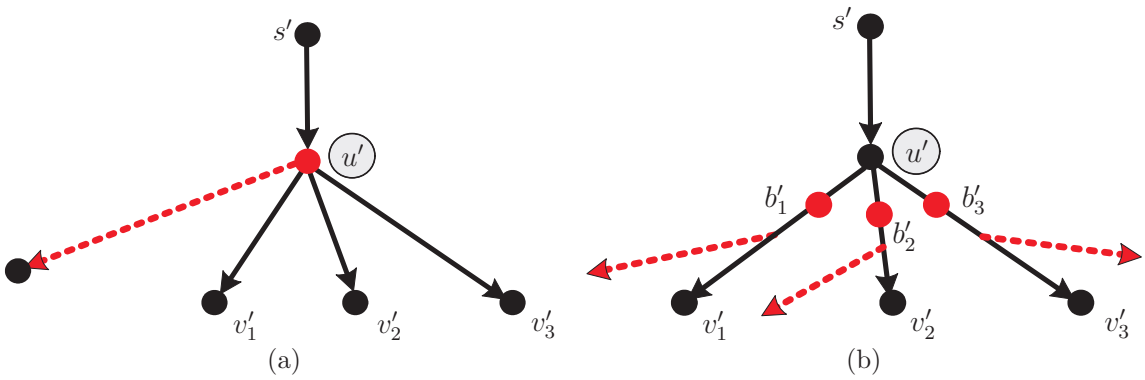


Figure 5.1.4: Equivalence classes: (a) node equivalence class, (b) branch equivalence classes

A graph example and the corresponding branching structure are shown in Figure 5.1.5. In this figure the node a has three equivalence classes associated with it and its children. The first class $\mathcal{C}(a)$ consists of the paths that overlap with $\mathcal{P}_1, ..., \mathcal{P}_5$ up to a, then branch off at a. The second class $\mathcal{C}(a, c)$ contains those paths that have the same subpath from s' to a with $\mathcal{P}_4, \mathcal{P}_5$, and diverge somewhere strictly between a and c. The third class $\mathcal{C}(a, b)$ includes the paths that share the subpath from s' to a with $\mathcal{P}_1, \mathcal{P}_2$, and $\mathcal{P}_3$ until a, then leave before b.

The problem of searching for many shortest paths between two vertices s' and t' can now be reduced to handling of the equivalence classes. There is an equivalence class for each non-leaf node and branch of the tree. To store the lengths of the shortest paths from each of the equivalence classes, a heap is used. For each class, one determines the minimum element, and then inserts it into the heap. The next shortest path corresponds to the smallest entry of the heap. This path is then chosen and deleted from the heap. Accordingly the path branching structure and the associated equivalence class partition are modified.

The node and branch equivalence classes are determined after a shortest path computation. There are two situations that may occur. In the first one the current shortest

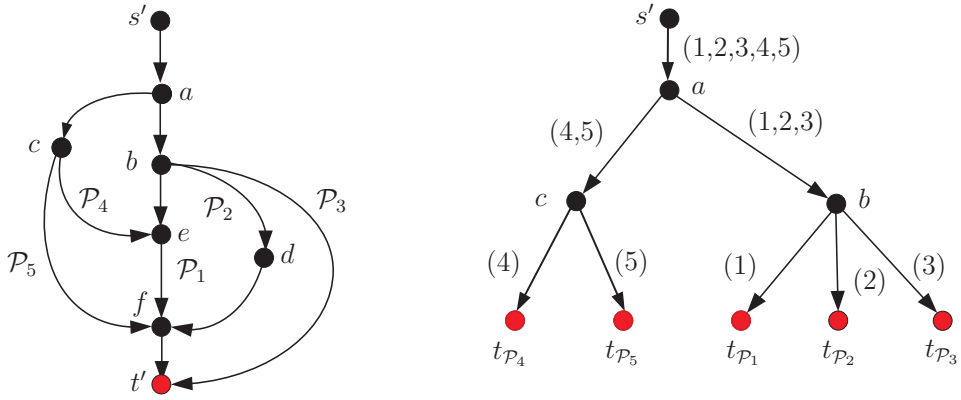


Figure 5.1.5: Five shortest paths and their path branching structure according to [63]

path $\mathcal{P}$ comes from a node u' in the branching structure. That is, this node is already contained in $\mathcal{T}_i$. Here the node class $\mathcal{C}(u')$ is modified and a new branch equivalence class $C(u', t_{\mathcal{P}})$ is created. In the second situation the current shortest path $\mathcal{P}$ comes from a branch (u', v') in the branching structure. That means, from some node w' between u' and v', and which is not yet inserted in branching structure. Here, and as in the first case, the classes $\mathcal{C}(w')$ and $C(w', t_{\mathcal{P}})$ corresponding to the new node w' are computed. In addition, two equivalence classes $\mathcal{C}(u', w')$ and $C(w', v')$ associated to the branches (u', w') and (w', v') are determined. This procedure involves refining one equivalence class into at most four classes. Both situations are shown in Figure 5.1.6.

Each of the four equivalence classes is associated a subgraph H' of G', in which the shortest path is determined. To solve the shortest path in an equivalence class $\mathcal{C}(u')$ *Dijkstra*'s algorithm is applied to compute the shortest suffix path from u' to t' in a subgraph H' of G' obtained by deleting from G' all the vertices in $prefixPath(u')$ except u', plus all the lead edges that leave from u'. This path is then appended to $prefixPath(u')$. This procedure is represented in Figure 5.1.6(a).

To solve the shortest path in a branch's equivalence class $\mathcal{C}(u', v')$ the lead edge of $\mathcal{L}(u', v') = (u', b')$ is considered. The paths in this class follow $prefixPath(v')$ up through the lead edge b', then branch off before v'. Thus the problem reduces to finding the shortest suffix starting at b', ending at t', which is vertex-disjoint from $prefixPath(u')$ and deviates from $branchPath(u', v')$ before v'. This path is determined using a replacement path algorithm, described later in this section, in a subgraph H' of G', defined by deleting from G' all the vertices on $prefixPath(u')$, including u'. Figure 5.1.6(b), 5.1.6(c), and 5.1.6(d) show this situation.

The overall complexity of the k-shortest paths algorithm is dominated by $O(k)$ invocations of the replacement paths subroutine. In the optimistic case, this takes $O(m + n \log n)$ time per invocation, which is equivalent to one *Dijkstra*'s call. In the pessimistic case, it takes $O(n\,(m+n \log n))$ time per invocation. The pseudo-code of the algorithm presented in [63] is given by Algorithm 5.1.2.

The computation of the shortest path in each branch equivalence class can be formulated as a replacement paths problem. Given a directed graph $H' = (V', E')$ with positive edge weights, a start vertex x and a target vertex y. Consider $\mathcal{P} = \{v'_1, v'_2, ..., v'_m\}$, where

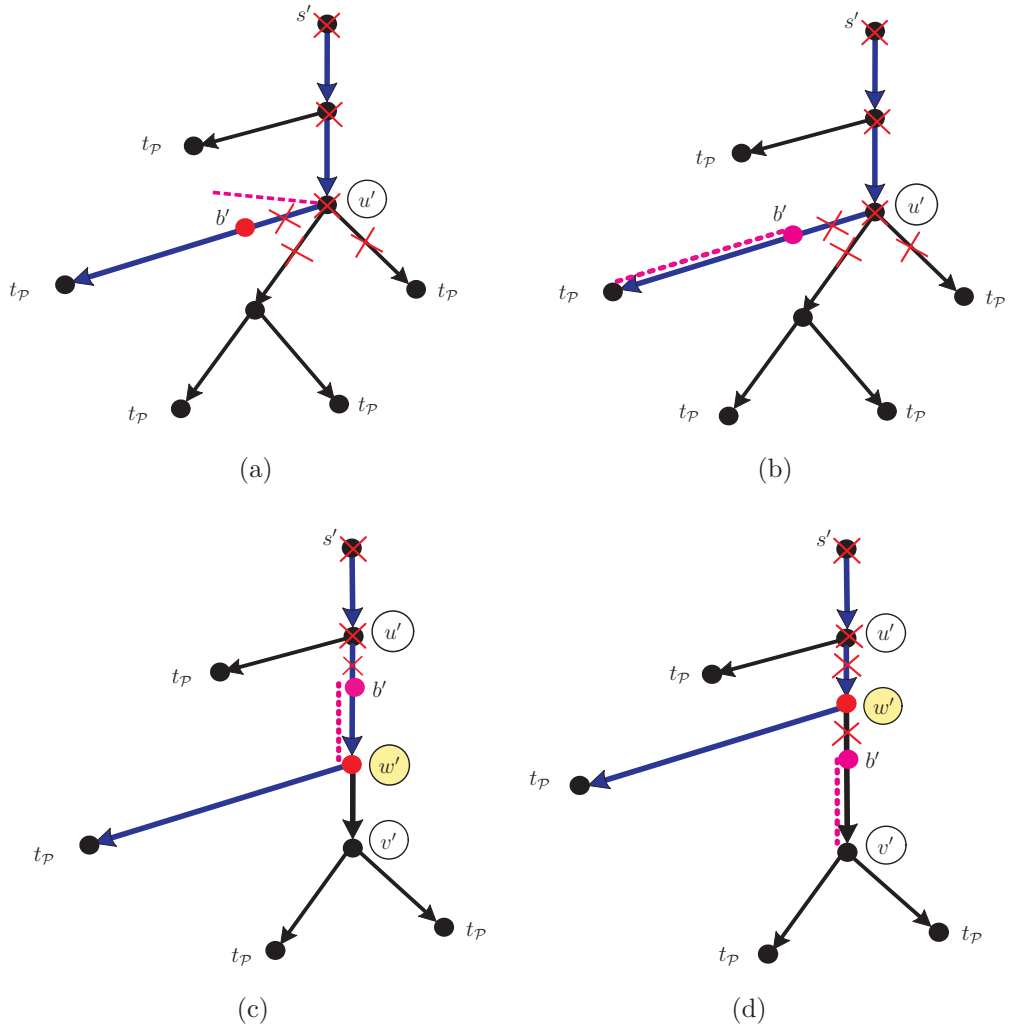


Figure 5.1.6: Equivalence classes associated to the nodes and branches of a branching structure: (a) node u', (b) branch $(u', t_{\mathcal{P}})$, (c) branch (u', w'), (d) branch (w', v')

$v'_1 = x$, and $v'_m = y$, the shortest path from x to y in H'. The best replacement path for the edge (v'_i, v'_{i+1}), for each $i \in \{1, 2, ..., m-1\}$, is the shortest path from x to y that does not include (v'_i, v'_{i+1}).

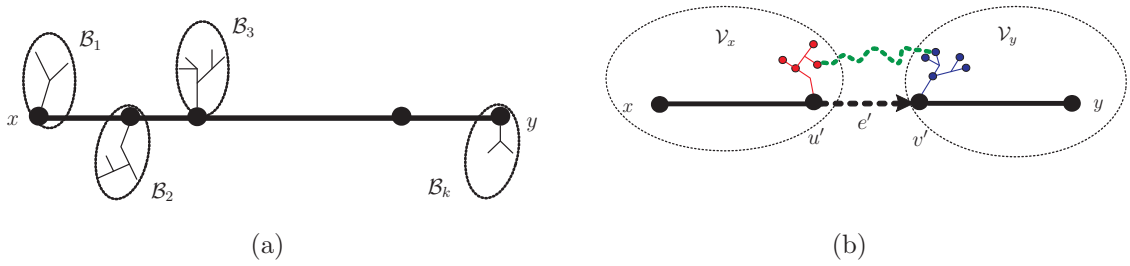
A trivial procedure requires $m-1$ invocations of the single source shortest path computation in the graph $H' \backslash (v'_i, v'_{i+1})$, and thus leads to a slower algorithm. An alternative is the efficient replacement paths algorithm presented in [64]. This algorithm computes all the replacement paths for each edge that belongs to the shortest path in $O(m + n\,logn)$ time. The replacement paths algorithm may fail for some directed graphs, but the failure can be detected and switch into the trivial procedure.

Given a shortest path $\mathcal{P}$ connecting two vertices x and y for which the best replacement path is to be determined. For each edge e' in $\mathcal{P}$ the replacement distance $d(x, y, G' \backslash e')$ can be computed by combining two shortest path trees $\mathcal{X}$ and $\mathcal{Y}$ constructed from the roots x and y respectively. The shortest path tree $\mathcal{Y}$ with root y can be computed after reversing the orientation of every edge in E'. These shortest path trees can be computed in $O(n \log n + m)$ time using *Dijkstra*'s algorithm and Fibonacci heaps.

Algorithm 5.1.2 Algorithm k-Shortest Simple Paths [63]

Initialize the path branching structure $\mathcal{T}_0$ to contain the source node s', and put $path(s', t')$ in the heap. There is one equivalence class $\mathcal{C}(s')$ initially, which corresponds to $Path_{s't'}$.
repeat
    Extract the minimum key from the heap. The key corresponds to
    some path $\mathcal{P}_i$.
    if $\mathcal{P}$ belongs to an equivalence class $\mathcal{C}(u')$ for some node u' **then**
        Add a new branch $(u', t_{\mathcal{P}_i})$ to $\mathcal{T}_i$ that represents the suffix of $\mathcal{P}_i$ after
        u'.
        Remove from $\mathcal{C}(u')$ the paths that share at least one edge with $\mathcal{P}_i$
        after u' and put all of them except $\mathcal{P}_i$ into the newly created
        equivalence class $\mathcal{C}(u', t_{\mathcal{P}_i})$.
    else if $\mathcal{P}_i$ belongs to an equivalence class $\mathcal{C}(u', v')$ for some branch (u', v') **then**
        Let w' be the vertex where $\mathcal{P}_i$ branches off from $branchPath(u', v')$.
        Insert a new node labeled w', and split the branch (u', v') into two
        new branches (u', w') and (w', v'). Add a second branch $(w, t_{\mathcal{P}_i})$ that
        represents the suffix of $\mathcal{P}_i$ after w'.
        Redistribute the paths of $\mathcal{C}(u', v')$ among the four new equivalence
        classes $\mathcal{C}(u', w'), \mathcal{C}(w', v'), C(w', t_{\mathcal{P}_i})$, and $\mathcal{C}(w')$, depending on where
        they branch from $branchPath(u', v')$ and /or $\mathcal{P}_i$.
        - Paths branching off $branchPath(u', v')$ before node w' belong to
        $\mathcal{C}(u', w')$.
        - Paths branching off $branchPath(w', v')$ after node w' belong to
        $\mathcal{C}(w', v')$.
        - Paths branching off $\mathcal{P}_i$ after node w' belong to $\mathcal{C}(w', t_{\mathcal{P}_i})$.
        - Paths branching off both $\mathcal{P}_i$ and $branchPath(u', v')$ at node w'
        belong to $\mathcal{C}(w')$.
    end if
    For each new or changed equivalence class, compute the
    shortest path from s' to t' that belongs to the class. Insert these paths
    into the heap.
until $i = k$

The algorithm is based on a partitioning of the vertices in V' into two sets $\mathcal{V}_x$ and $\mathcal{V}_y$ such that $x \in \mathcal{V}_x$ and $y \in \mathcal{V}_y$. These sets are easily obtained from the shortest path tree $\mathcal{X}$ by removing the edge $e'_i = (v'_i, v'_{i+1})$ in $path(x, y)$, for which the best replacement distance should be computed. For their determination the vertices of V' are assigned to blocks $\mathcal{B}_i$, which indicate their positions in the shortest path tree $\mathcal{X}$. That is, for each vertex $u' \in \mathcal{B}_i$, $block(u') = i$. Thus for a given edge $e'_i = (v'_i, v'_{i+1})$ to be removed in $path(x, y)$, $\mathcal{V}_x = \cup_{j=1}^{i} \mathcal{B}_j$, and $\mathcal{V}_y = \cup_{j=i+1}^{k} \mathcal{B}_j$. Figure 5.1.7 shows a shortest path tree and the associating blocks. As shown in Figure 5.1.7(a) the blocks of vertices are related to their predecessor nodes on the shortest path. Figure 5.1.7(b) illustrates the replacement paths procedure for the edge $e' = (u', v')$.



(a) (b)

Figure 5.1.7: Partitioning of vertices into blocks: (a) shortest path tree, (b) cut edges for the edge $e' = (u', v')$ [64]

The set of edges crossing the cut $(\mathcal{V}_x, \mathcal{V}_y)$, denoted E'_{cut}, is defined based on the shortest path tree $\mathcal{X}$. That are the edges (u', v') that have their start vertex $u' \in \mathcal{V}_x$ and their target vertex $v' \in \mathcal{V}_y$. Any path from x to y must include at least one edge from E'_{cut}. For a given edge $(u', v') \in E'_{cut}$ the shortest paths $path(x, u')$ and $path(v', y)$ are contained in $\mathcal{V}_x$ and $\mathcal{V}_y$ respectively. The corresponding distances are given by the shortest path trees $\mathcal{X}$ and $\mathcal{Y}$. Thus, for each edge $e'_i = (v'_i, v'_{i+1})$ in the shortest path $path(x, y)$ and for some cut $E'_{cut} = (V_x, V_y)$, the shortest distance is expressed by

$$d(x, y, G'\backslash e'_i) = \min_{\substack{(u', v') \in E'_{cut} \\ (u', v') \neq e'_i}} \left(d(x, u'; G'\backslash e'_i) + c(u', v') + d(v', y; G'\backslash e_i)\right). \qquad (5.1.1)$$

By evaluating (5.1.1) over all the edges $e'_i = (v'_i, v'_{i+1})$ of $path(x, y)$ in sequence from $i = 1$ to $n - 1$, the best replacement path can be obtained efficiently. It is the path with the minimum distance over all the cut edges. For some directed graphs the replacement path algorithm may fail. Figure 5.1.8 shows an example in which vertex v' belongs to the set $\mathcal{V}_x$ that contains y, but the shortest path $path(v', y)$ goes through the edge e', and leads to an incorrect path.

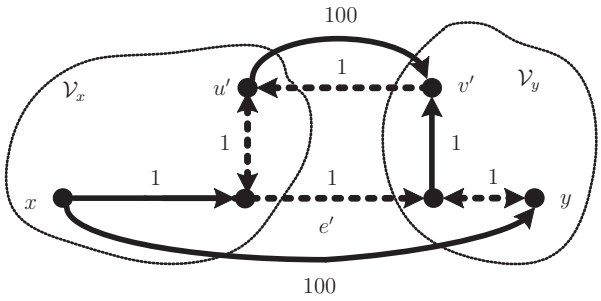


Figure 5.1.8: Example of incorrect replacement path [64]

In order to detect which edges cause incorrect replacement paths, the vertices $v' \in V'$ are labeled according to the lowest-indexed block of the tree $\mathcal{X}$, such that $path(v', y)$ passes through. The smallest index i for which $path(v', y)$ contains a vertex of block $\mathcal{B}_i$ is defined to be the minblock of v', denoted $minblock(v')$. That is, $minblock(v') = \min_{w' \in path(v', y)} block(w')$. For any edge (u', v'), $minblock(u')$ is just $min(block(u'), minblock(v'))$. Figure 5.1.9 shows the definition of the terms block and minblock for a path (v', y).

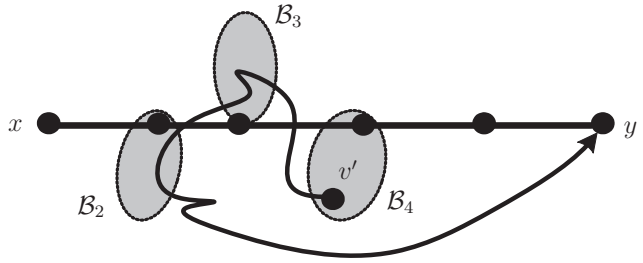


Figure 5.1.9: Notions of block and minblock: $block(v') = 4$, $minblock(v') = 2$ [64]

To formalize the condition for which the replacement path algorithm computes a correct path associated to a given edge $e' = (u', v') \notin path(x, y)$, the quantities $left(e') = block(u')$ and $right(e') = minblock(v')$ are defined. From these definitions, the set of edges e'_i for which (5.1.1) can be minimized satisfy $left(e') \leq i < right(e')$. Equation (5.1.1) can then be written as

$$d(x, y, G'\backslash e'_i) = \min_{\substack{(u', v') \in E'_{cut} \\ (u', v') \neq e'_i \\ path(v, y) \cap V_x = \emptyset}} \left(d(x, u'; G'\backslash e'_i) + c(u', v') + d(v', y; G'\backslash e_i)\right). \quad (5.1.2)$$

The pseudo-code of the replacement path algorithm described above is given by Algorithm 5.1.3.

Algorithm 5.1.3 Algorithm Replacement Path [63]

1: In the graph H', let $\mathcal{X}$ be a shortest path tree from the source x to all the remaining nodes, and let $\mathcal{Y}$ be a shortest path tree from all the nodes to the target y. The shortest path $\mathcal{P}$ from x to y belongs to both $\mathcal{X}$ and $\mathcal{Y}$.
2: **for** every edge $e'_i = (v'_i, v'_{i+1}) \in \mathcal{P}$ **do**
3: Let $\mathcal{X}_i = \mathcal{X}\backslash e'_i$. Let E'_i be the set of all edges $(a', b') \in E'\backslash e'_i$ such that a'
4: and b' are in different components of $\mathcal{X}_i$, with a' in the same component
5: as x.
6: **for** every edge $(a', b') \in E'_i$ **do**
7: let $d(a', b') = d(x, a') + c(a', b') + d(b', y)$. Observe that $d(x, a')$
8: and $d(b', y)$ can be computed in constant time from $\mathcal{X}$ and $\mathcal{Y}$.
9: **end for**
10: The replacement distance for e'_i is the minimum of $d(a', b')$
11: over all $(a', b') \in E'_i$.
12: **end for**

The k-shortest paths algorithms can be used with an appropriate metric to compute the weighted signal paths between any pair of nodes in a SFG representing an electronic network. Their evaluation provides an approximation of the total transfer function. The number of paths required can be determined using some given threshold value.

5.2 Approach to Dominant Signal Paths Analysis

The signal tracing approach presented in this section allows for the identification of weighted propagation paths connecting a noise source and a victim pin in a PCB. Thus, providing the ability to classify the interconnect paths into critical and less critical ones. Instead of analyzing the transmission substructures separately, the global system is considered. Dominant propagation paths connecting two ports are characterized by the amount of signal transmitted through them. The approach proposed to identify and evaluate such paths is based on a combination of graph shortest paths algorithms and the transfer function formulation in signal flow graphs. This approach is described in details in this section.

5.2.1 Illustration of A Dominant Signal Path

A direct solution to determine the signal propagation paths with respect to induced transient impulses within a printed circuit board is based on a separate analysis of all interconnection structures. Thus, critical structures with higher field coupling can be detected. For the simulation of the whole circuit, derived models are inserted into a circuit netlist and the whole network is analyzed by applying an interference source model.

In this thesis dominant propagation paths are determined considering the entire system. A dominant path is defined by a sequence of circuit nodes, or interconnects, transmitting significant noise power from a noise source to a device pin. It is said to be critical if the associated power transfer disturbs the function of the target device [65]. That is, the coupling impulses are comparable with the noise margin of the digital sensitive components. A dominant propagation path may contain galvanic paths as well as all possible parasitic coupling paths.

The identification of dominant paths is limited to linear circuits consisting mainly of transmission structures and passive linear components. Their evaluation is performed by computing the physical quantities representing the signal transfer between specified components. Particularly the wave quantities can be introduced to represent the signal or energy transfer between the ports of these components.

To illustrate the notion of a dominant signal path the system of interconnects in Figure 5.2.1 is considered. It consists of single and parallel coupled transmission lines. The signal path indicated by the dashed line in this figure is assumed to transmit high amount of power from port 1 to port 2, and thus becomes dominant over the remaining paths. It is composed of galvanic and coupling subpaths.

5.2.2 Mathematical Background of the Algorithm

This section will apply $k-$shortest simple paths algorithms to identify the dominant signal paths between two ports in a linear network. The approach is developed by deriving an approximation to the *Mason*'s formula given by (4.2.5). The total transfer function can

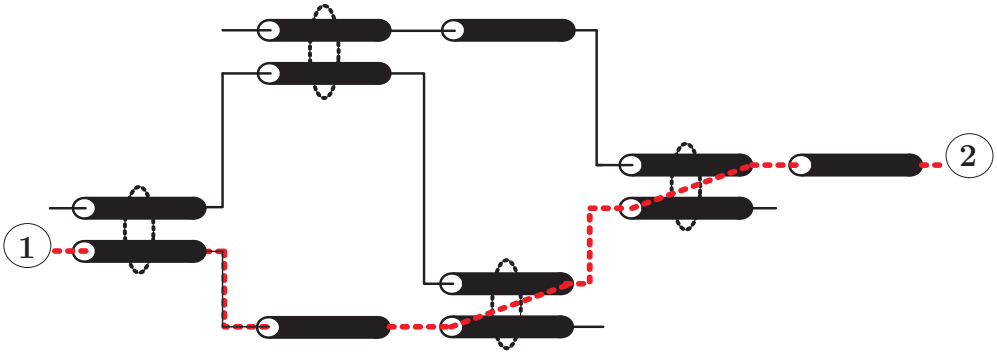


Figure 5.2.1: Illustration of a dominant signal path [66]

be seen as a superposition of many partial transfer functions, related to the signal paths connecting the input and output nodes in the circuit graph. Instead of computing the transfer function using all the existing signal paths, between a noise source and a device pin, shortest paths algorithms are applied to identify only the weighted terms of the transfer function that characterize some directed simple paths between the corresponding nodes. In Figure 5.2.2 the concept of weighted signal propagation paths between two nodes in a signal flow graph is illustrated by means of the interconnected transmission structures of Figure 5.2.1.

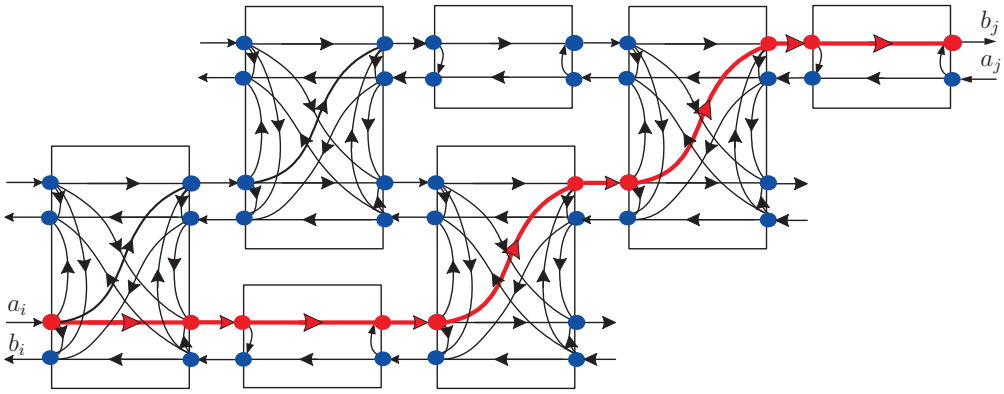


Figure 5.2.2: Signal transfer between two ports

The k-shortest simple paths algorithm described in Section 5.1.2 is applied to extract the required number of paths that are dominant. For validation purposes the number of signal paths which deliver a good approximation to the transfer function should be extracted. This algorithm is applied to signal flow graphs with additive metric, or weights, derived from the scattering parameters of the interconnection structures and their linear termination loads.

For a path $\mathcal{P}_{u',v'}$ relating two nodes u' and v' in a directed graph without cycles and passing through a sequence of nodes $u'_1, u'_2, \ldots, u'_n$, the transfer function associated to this path, also called direct path gain, is computed from the scattering parameters of the edges connecting these nodes by

$$H_{\mathcal{P}_{u',v'}} = s_{u'u'_1}.s_{u'_1u'_2} \ldots s_{u'_nv'}. \tag{5.2.1}$$

Figure 5.2.3 shows different directed simple paths connecting the vertices u' and v' in a graph. The magnitudes of the transfer functions $H_{\mathcal{P}_{u',v'}}$ associated to the paths are the main criteria considered to determine the weighted ones.

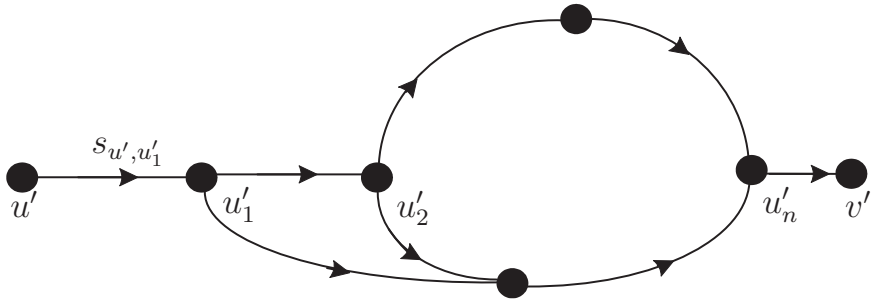


Figure 5.2.3: Directed simple paths between two vertices

The problem of computing dominant paths in a PCB is formulated as identifying some shortest paths in a representing SFG. For its construction a mapping of scattering parameters onto additive quantities is required. A logarithmic metric allowing the addition of the edge weights belonging to a direct path is defined. It is given by

$$c(u', v') = \log\left(\frac{1}{\|s_{u'\,v'}\|}\right). \tag{5.2.2}$$

The value of $c(u', v')$ is always positive, except if $s_{u'\,v'}$ equals zero, which does not occur in high frequencies. The use of such a positive metric is a condition to apply the most efficient *Dijkstra*'s algorithm. Figure 5.2.4 shows the curve representing the proposed metric derived from the scattering parameters having a magnitude in the interval $]0, 1]$.

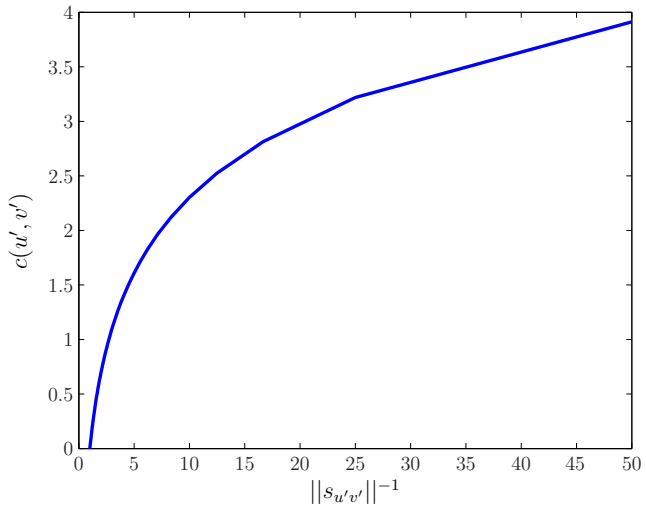


Figure 5.2.4: The function representing the edge metric in terms of scattering parameters

The algorithm to extract the dominant propagation paths starts with an initialization step where the start node (noise source), destination node (chip port), and the first shortest path is computed. In this thesis the number k of paths required to compute the transfer function is not specified, but determined automatically by the algorithm using a threshold

approach [66]. In other words, the ratio of the transmission coefficients associated to two successive signal paths is compared with a given threshold T_h. In the next step of the algorithm the second dominant path is extracted. The ratio of the transmission coefficient magnitudes associated to both paths is evaluated and compared with the threshold T_h. If this ratio is smaller than the threshold T_h, the algorithm stops else the next shortest path is extracted. This procedure is repeated for each new extracted path $\mathcal{P}_{i+1}$ and its predecessor $\mathcal{P}_i, i = 1, 2, \ldots$ until a ratio of transmission coefficients is reached, which forces the algorithm to stop. Thus the number of signal paths identified corresponds to the number k required. The pseudo-code of the k-shortest path algorithm extended with a threshold approach is given as

Algorithm 5.2.1 Algorithm Transmission Coefficient Threshold

1: Initialization:
2: - Set the start and target nodes u' and v'
3: - $i = 1$
4: - Extract the first path $\mathcal{P}_1$
5: - Set a threshold T_h (e.g. 10%)
6: **repeat**
7: $i = i + 1$
8: Extract the i-th path $\mathcal{P}_i$ using the k-shortest path algorithm
9: Compute $Q = \dfrac{\| s_{u'v'}(\mathcal{P}_i) \|}{\| s_{u'v'}(\mathcal{P}_{i-1}) \|}$
10: **until** $Q <= T_h$

Equation (4.2.4) which requires the extraction of all paths connecting two nodes u' and v' in a graph is modified. To compute the scattering parameter coefficients $s_{u',v'}$ between both nodes, a limited number k of weighted signal paths is considered. Its new expression is given as

$$s_{v',u'} \simeq \sum_{i=1,\mathcal{P}_i \in Path(v',u')}^{i=k} H_{\mathcal{P}_i} \left[\frac{det_{\mathcal{P}_i}}{det_{SFG}} \right], \tag{5.2.3}$$

where $H_{\mathcal{P}_i}$ is the transfer function associated to the path $\mathcal{P}_i$ and which can be computed by the use of (4.2.3), det_{SFG} is the determinant of the structure matrix associated to the scattering parameters signal flow graph, and $det_{\mathcal{P}_i}$ is the determinant of the one associated to the subgraph without the nodes belonging to the path $\mathcal{P}_i$. That is, the matrix after removing the rows and columns corresponding to the individual paths connecting the input and output nodes u' and v'.

This approach represents a combined method to compute the power wave scattering parameters, since the transfer functions $H_{\mathcal{P}_i}$ associated to the dominant paths extracted have to be multiplied by the associated cycle transfer functions computed from a matrix formulation. The transmission coefficients are formulated by identifying of dominant signal propagation paths relating a start and a target port of interest in an PCB. Using the transmission coefficient as transfer function, (5.2.3) can be written as

$$s_{u',v'} \simeq s_{u',v'}(\mathcal{P}_1) + s_{u',v'}(\mathcal{P}_2) + \ldots + s_{u',v'}(\mathcal{P}_k), \tag{5.2.4}$$

where

$$s_{u',v'}\left(\mathcal{P}_i\right) = H_{\mathcal{P}_i}\left[\frac{det_{\mathcal{P}_i}}{det_{SFG}}\right], \text{i=1,2,...,k.}$$

Here, $H_{\mathcal{P}_i}$ is the value of the gain associated to the path $\mathcal{P}_i$, and which is given by (5.2.3). The principle of determining the dominant noise paths is illustrated in Figure 5.2.5.

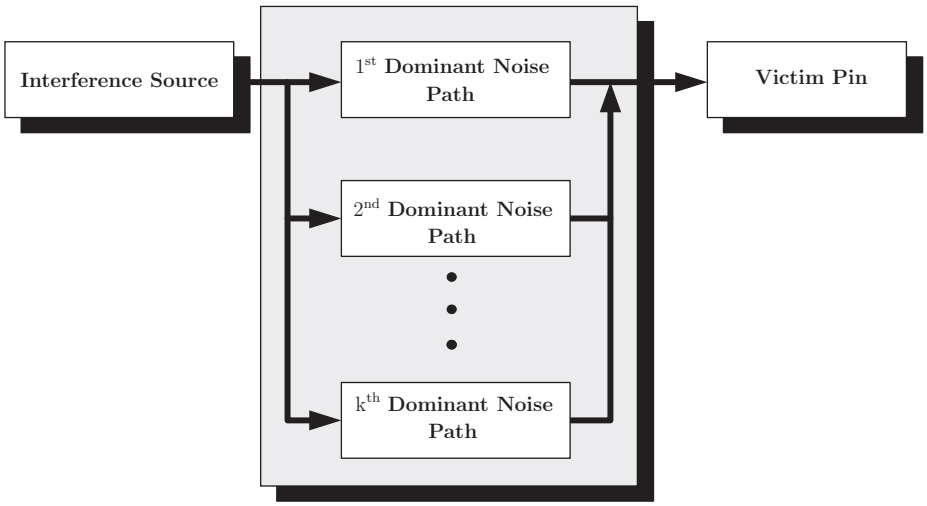


Figure 5.2.5: Principle of signal path extraction [67]

The reflection coefficients may also be obtained considering the dominant propagation paths. Their use is however useful only when a complete simulation of the system is required. If the nodes representing the reflected and the incident waves at the noise source and the target load ports, in a PCB, are denoted by u^r and v^i, the approximated two-port scattering matrix relating these ports is given as

$$\boldsymbol{S} \simeq \begin{pmatrix} \sum_{i=1}^{k1} s_{u'u^r}\left(\mathcal{P}_i\right) & \sum_{i=1}^{k} s_{u'v'}\left(\mathcal{P}_i\right) \\ \sum_{i=1}^{k} s_{v^iu^r}\left(\mathcal{P}_i\right) & \sum_{i=1}^{k2} s_{v^iv'}\left(\mathcal{P}_i\right) \end{pmatrix}, \tag{5.2.5}$$

where k is the number of the paths giving a good approximation to the transmission coefficients, and k_1, and k_2 are the numbers of the paths giving a good approximation to the reflection coefficients at the source and target ports respectively. For symmetrical networks, the off-diagonal elements of (5.2.5) are equal.

In the case where multiple noise sources exist, i.e. several input nodes in the signal flow graph, (4.2.6) can also be approximated using the notion of dominant signal paths. Each noise source is analyzed separately, then the results are superimposed.

5.2.3 Reciprocity of Dominant Signal Paths

In this subsection the reciprocity of dominant signal propagation paths is investigated. Up to now, only signal paths transmitting power from a noise source to a target load, also

called forward paths, are considered. To demonstrate the reciprocity property of signal paths for linear passive networks the noise source is applied at the target port and the load is placed at the start port. In other words the start and target nodes in the circuit are swapped. In the corresponding signal flow graph this is equivalent to considering the nodes associated to the incident and transmitted waves at the target and start ports respectively.

Due to the reciprocity of passive linear networks the matrices characterizing the individual interconnect and discrete elements are symmetric. As a result the signal propagation paths become also reciproc. Applying the k-shortest simple paths algorithm to the signal flow graph with swapped start and target nodes delivers reversal directed paths, called here backward paths, having same weights. These paths travel the same ports of the network as the corresponding forward paths. That means the same nodes in the circuit. Using the reciprocity property has the advantage to reduce the computation time when computing the scattering matrix of the entire system. That's, only the forward paths between every pair of vertices should be considered [66]. Figure 5.2.6 shows a forward and its associating backward signal path between two specified ports.

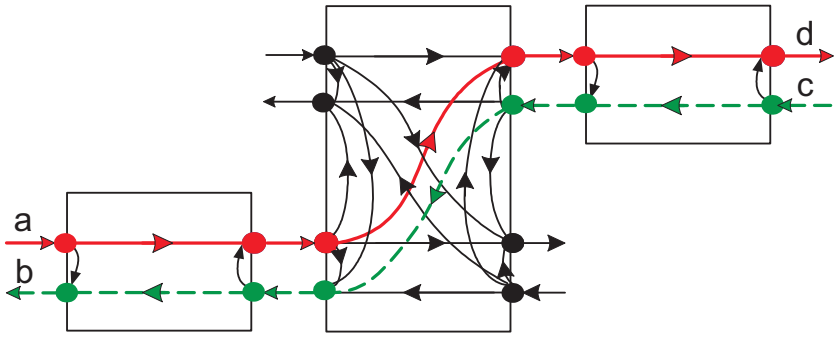


Figure 5.2.6: Illustration of the reciprocity of signal propagation paths for passive linear networks

5.2.4 Workflow of the Dominant Path Approach

A conventional approach to determine the distribution of transient noise within a printed circuit board consisting of complex transmission structures is based on the partitioning of the global system into simple interconnect structures and the simulation of all relevant structures including possible parasitic couplings using numerical methods. The simulation data can be provided in form of matrices or equivalent electrical macromodels. These data will be placed into the circuit matrix which can be solved using e.g. the nodal analysis technique.

Such an approach provides only the system response at the circuit nodes and branches, but no information on signal propagation paths. However the technique presented in this thesis allows the identification of dominant signal paths relating two specified ports in the circuit. The input and output ports correspond to the interference source and the target

load respectively. The work-flow of the proposed dominant path approach is depicted in Figure 5.2.7.

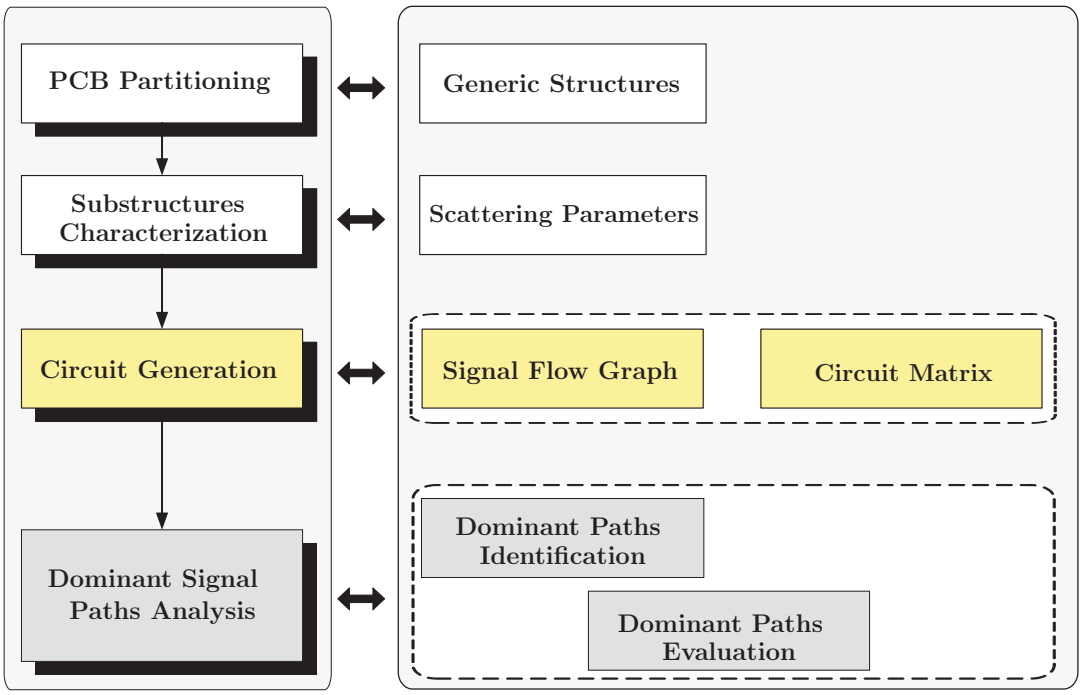


Figure 5.2.7: Path tracing analysis flow

The approach starts with partitioning of complex structures on the PCB into fundamental ones. In the nest step, the substructures are characterized in the frequency domain by their scattering matrices. Then, at each frequency point both the circuit signal flow graph and matrix are generated. The SFG is constructed by connecting the subgraphs of the structures in the circuit. Each port of the substructures is represented by two nodes associated to the transmitted and reflected waves. The edges are associated the weights defined by (5.2.2). By means of shortest paths algorithms the dominant propagation paths relating an impulse source and a destination target device pin can be extracted in the circuit SFG. These paths are then evaluated in terms of transmission coefficients using the circuit matrix formulation according to (5.2.3). The dominant signal paths may be extracted at all frequency points in the interval of the analysis. Alternatively, the coupling frequencies are determined in a preprocessing step and the signal paths are extracted at the resonant ones.

5.2.5 Analysis Example

The proposed approach to dominant paths analysis is applied to a circuit consisting of interconnects of parallel transmission lines and passive discrete components. The schematic of this circuit is shown in Figure 5.2.8. It consists of six blocks of coupled parallel microstrip line systems. The microstrips are assumed to be lossless. The microstrips of width 200 μm, thickness 30 μm are placed on a dielectric substrate of a permittivity ε_r=4.5 which

is placed on a conducting metal ground plane. The space between the microstrip lines is 300 μm. The blocks of two and three coupled traces are indicated by MTL 2 and MTL 1, respectively. The length of MTL 2 is 2 cm, whereas MTL 1 have a length of 3 cm. The lines which are not connected to each other are matched.

The three coupled microstrips are characterized by the per unit length inductance and capacitance matrices

$$\boldsymbol{L} = \begin{pmatrix} 512.71 & 136.11 & 56.26 \\ 136.11 & 509.61 & 136.11 \\ 56.26 & 136.11 & 512.71 \end{pmatrix} \frac{\text{nH}}{\text{m}}, \quad \boldsymbol{C} = \begin{pmatrix} 68.83 & -11.62 & -1.01 \\ -11.62 & 71.07 & -11.62 \\ -1.01 & -11.62 & 68.83 \end{pmatrix} \frac{\text{pF}}{\text{m}},$$

and the inductance and capacitance matrices per unit length of the two coupled lines are

$$\boldsymbol{L} = \begin{pmatrix} 513.07 & 137.21 \\ 137.21 & 513.07 \end{pmatrix} \frac{\text{nH}}{\text{m}}, \quad \boldsymbol{C} = \begin{pmatrix} 68.81 & -11.81 \\ -11.81 & 68.81 \end{pmatrix} \frac{\text{pF}}{\text{m}}.$$

A resistance $R_2 = 75\,\Omega$ and a capacitance $C_1 = 5\,\text{pF}$ are connected between some transmission lines of the circuit. The start node s' and the target node t' correspond to the voltage source and the load resistance $R_1 = 75\,\Omega$ respectively [65].

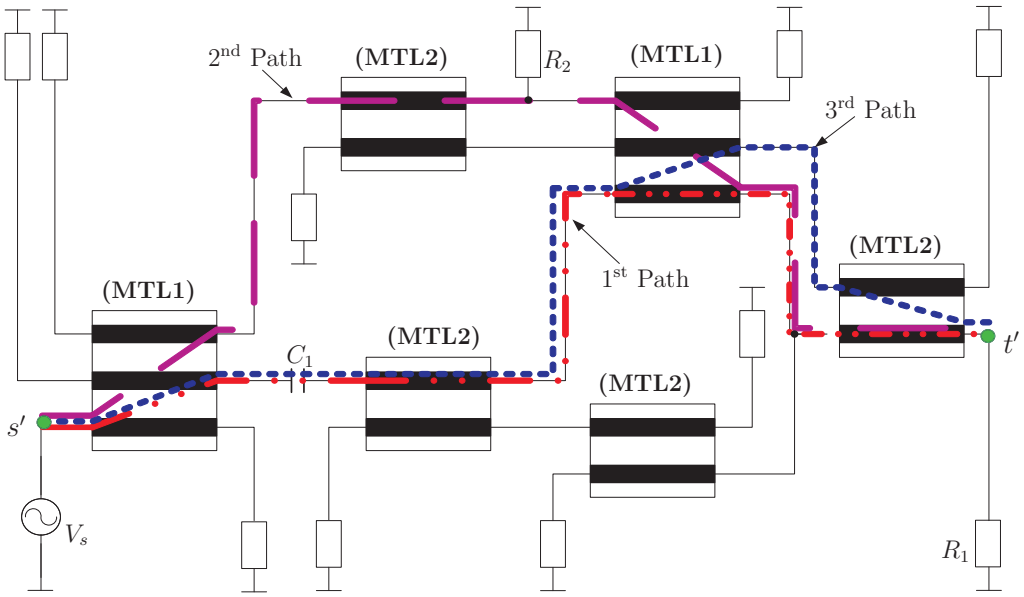


Figure 5.2.8: Example of a circuit showing the dominant crosstalk paths between the nodes s' and t' [65]

The scattering matrices, which are useful for the algorithm, are computed from the per unit length matrices $\boldsymbol{L}$ and $\boldsymbol{C}$. Because of the topology of this circuit all parasitic propagation paths relating the start and target nodes are due to the crosstalk between the transmission lines. That's, there are no conducting paths contributing to the signal transfer between both nodes.

The first three dominant paths relating the noise voltage V_s source and the target load R_1 are extracted. These are indicated in the schematic of Figure 5.2.8. These represent

the propagation ways that transmit significant noise power from the voltage source to the load R_1. The remaining signal paths are negligible, since they do not contribute to significant change in the total response. The magnitudes of the transmission coefficient s_{12} associated to these paths are depicted in Figure 5.2.9.

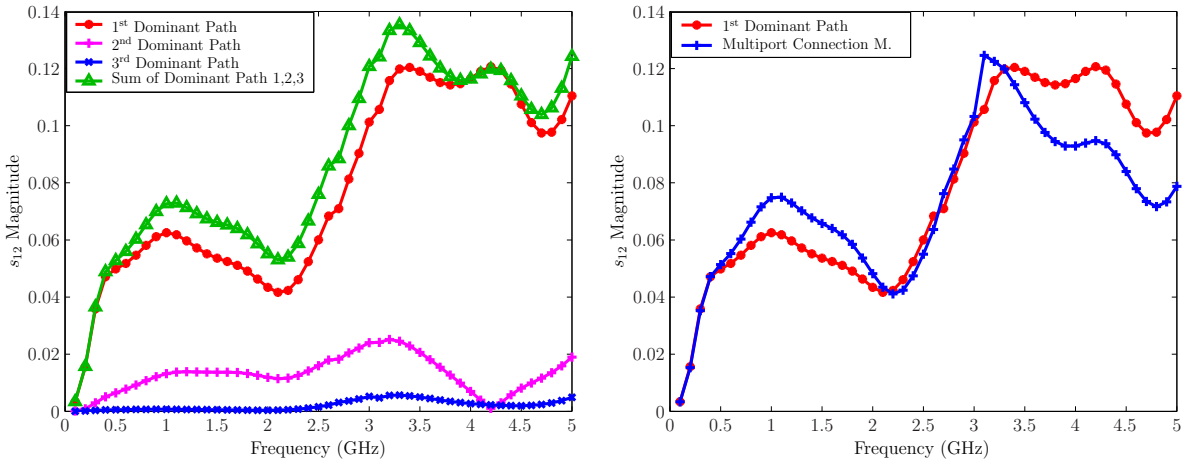


Figure 5.2.9: Transmission coefficient s_{12}: (a) the first three dominant signal paths, (b) comparison of $\mathcal{P}_1$ with the total response

Clearly all the three paths are resulting from the coupling between the transmission line ends. All coupling phenomena between the transmission lines are taken into account. Figure 5.2.9(a) compares the magnitudes of the transmission coefficients $s_{12}(\mathcal{P}_1)$, $s_{12}(\mathcal{P}_2)$, and $s_{12}(\mathcal{P}_3)$ associated to the three paths. The first dominant signal path shows significant transfer of power over the frequency range of 5 GHz. The second dominant path has a transfer function which is higher than the one of the third path up to the frequency of 4.2 GHz. The same figure compares the response from the superposition of the three dominant paths. In Figure 5.2.9(b) the magnitude of the most dominant path is compared with the one obtained by multiport connection method (4.1.21). A good convergence is achieved up to the frequency of 3.5 GHz. That means, the consideration of this path alone may be enough to model the transmission of power between the voltage source and the target load up to 3.5 GHz.

In order to compute the coupling voltage impulses at the target resistance R_1 an equivalent two-port of the circuit is synthesized. Its input and output ports correspond to the noise source V_s and target load R_1 respectively. The reflection coefficients at both ports are computed and an equivalent two-port scattering matrix of the linear circuit is obtained. Since the focus of interest is on the propagation of noise signal between the noise source and the target load, i.e. two different ports in the network, the propagation paths associated to the reflection coefficients are not indicated in the circuit schematic. Figure 5.2.10 shows the magnitude responses of the reflection coefficients at the input and output ports.

In this figure the reflection coefficients s_{11} and s_{22} are verified with the results of the multiport connection method over the frequency range of 5 GHz. For the coefficient s_{11}

identical results are obtained considering only the first two dominant paths. The curve of the coefficient s_{22} is obtained considering three dominant paths. The results can be improved by considering secondary paths. As a result a scattering matrix associated to the dominant signal paths is derived. It is given by

$$\boldsymbol{S} \simeq \begin{pmatrix} \sum_{r=1}^{2} s_{11}\left(\mathcal{P}_r\right) & s_{12}\left(\mathcal{P}_1\right) \\ s_{21}\left(\mathcal{P}_1\right) & \sum_{r=1}^{3} s_{22}\left(\mathcal{P}_r\right) \end{pmatrix}. \tag{5.2.6}$$

According to (5.2.5), $k = 1$, $k1 = 2$, and $k2 = 3$ are the number of signal paths required to approximate the coefficients s_{12}, s_{11}, and s_{22}, and thus the total system response.

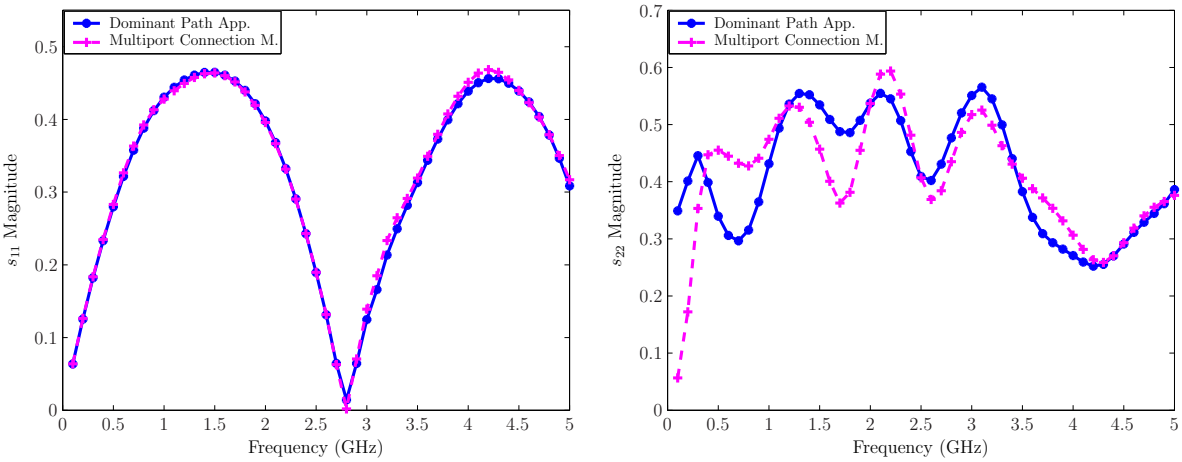


Figure 5.2.10: Magnitude of the reflection coefficients at : (a) noise source, (b) target load

The results in terms of the voltage transfer function $V_{t'}/V_{s'}$ are shown in Figure 5.2.11. The magnitude and phase responses obtained from the superposition of the individual responses of the first and second dominant signal paths are represented. An increase of crosstalk noise is observed with increasing operation frequency.

The resulting voltage responses, in term of magnitude (Figure 5.2.11a) and phase (Figure 5.2.11b), are compared with the total responses delivered by the HSPICE circuit simulator. The superposition of the first two dominant paths only delivers good results in terms of scattering coefficients and voltage phasor. Consequently only the first two dominant paths can approximate the total response of the system over the range of the frequency analyzed.

In order to study the reciprocity of the extracted dominant signal paths the transmission coefficient s_{21} is also computed using the same approach. In the schematic of Figure 5.2.12 the reciprocity is shown for each individual propagation path. The flow of the power between the voltage source and the target load is represented using forward and backward propagation paths. It is clear that each dominant signal path $\mathcal{P}_i$ from the target load to the noise source, for $i = 1, 2, 3$, traverses the same network ports like the one from the voltage source to the target load with the same order.

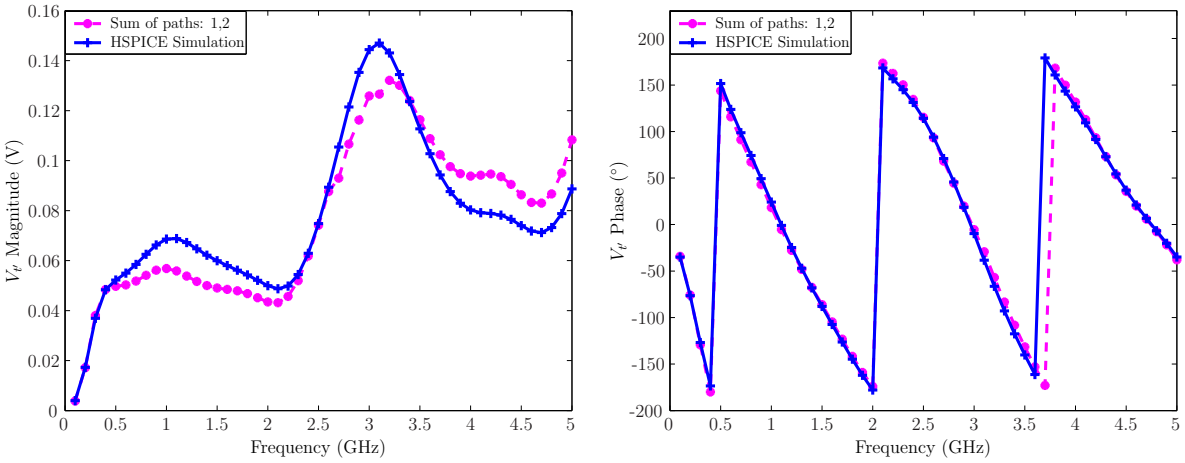


Figure 5.2.11: Coupling voltage impulses at the target load: (a) magnitude, (b) phase

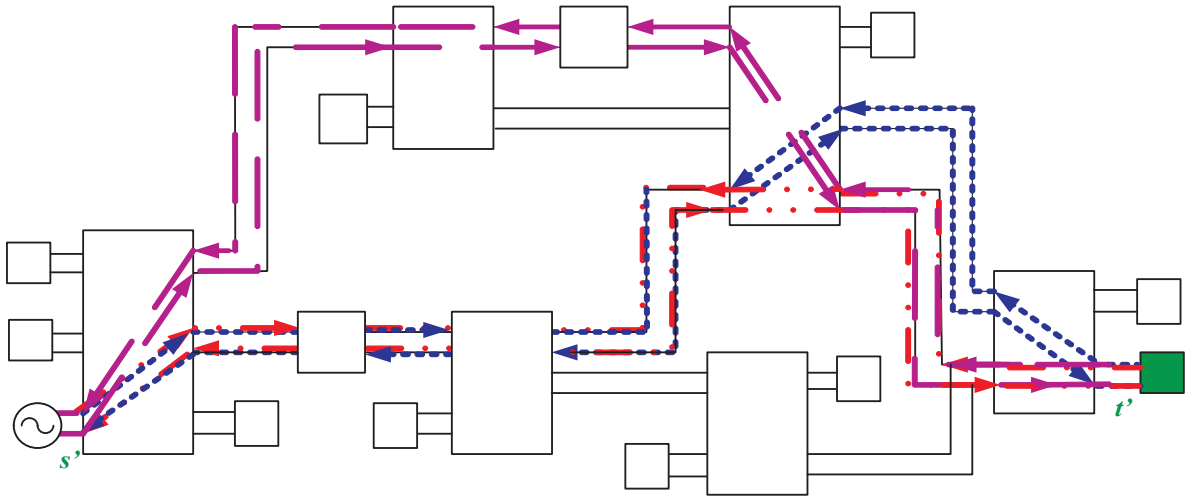


Figure 5.2.12: Forward and backward dominant propagation paths between two ports in a circuit

To conclude an approach for the extraction of dominant noise propagation paths relating two nodes in a linear circuit is presented. The dominant noise paths are extracted using k-shortest simple paths algorithms applied to the signal flow graph constructed from the scattering parameters of the circuit. The noise paths evaluation is performed by the computation of the corresponding transmission coefficients. The approach is illustrated by an interconnect circuit example.

Chapter 6

Time Domain Analysis of a Complete Signal Path

The dominant path approach presented in Section 5.2 is a frequency domain technique for describing the interactions between two specified ports in a linear circuit. These interactions are expressed in terms of the power flow through the weighted signal paths relating these ports. The corresponding voltage and current transfer functions can then be derived using appropriate transformations. The time domain analysis of signal paths is carried out in this chapter. The waveform of dominant noise propagation paths is investigated considering the characteristics of the excitation impulses and some features of the PCB.

6.1 Signal Path with a Linear Termination

Time domain signals can be represented by their frequency contents using the Fourier analysis. Periodic signals are often described by Fourier series while non-periodic signals are represented in the frequency domain by Fourier integral or transform.

6.1.1 Fourier Series

Every periodic signal, represented by a function f, with a period T can be represented in the time domain by the Fourier series expansion

$$f(t) = \frac{A_0}{2} + \sum_{n=1}^{\infty} \left(A_n \, cos(n\omega_0 t) + B_n \, sin(n\omega_0 t)\right), \tag{6.1.1}$$

where ω_0 is the fundamental angular frequency of the signal which is given by

$$\omega_0 = \frac{2\pi}{T}.$$

The coefficient A_0, A_n, and B_n are known as the Fourier coefficients. These are defined by

$$A_0 = \frac{2}{T}\int_{t=t_0}^{t_0+T} f(t)\,dt, \tag{6.1.2}$$

$$A_n = \frac{2}{T}\int_{t=t_0}^{t_0+T} f(t)\,cos(n\omega_0 t)\,dt, \tag{6.1.3}$$

$$B_n = \frac{2}{T}\int_{t=t_0}^{t_0+T} f(t)\,sin(n\omega_0 t)\,dt, \tag{6.1.4}$$

where t_0 can be any value of time.

Equation (6.1.1) means that a periodic signal is a summation of sinusoidal signals, referred to the harmonics of multiple frequencies and amplitudes. The frequency of each sinusoid in the series is an integer multiple of the fundamental frequency of the signal. The more sinusoids included in the sum, the better the approximation.

A more practical form of (6.1.1) is the discrete Fourier series, which approximates the signal value at a sampling point of time using a limit number M of discrete coefficients. It is defined by

$$f(t_k) = \frac{A_0}{2} + \sum_{n=1}^{M}\left(A_n\,cos(\frac{2\pi\,n\,k}{N}) + B_n\,sin(\frac{2\pi\,n\,k}{N})\right), \tag{6.1.5}$$

where N is the number of sampled signal values in the period T and $t_k = k\,\Delta t$ are the discrete time samples. The coefficients A_0, A_n, and B_n can be determined as for the continous Fourier series, but by replacing the integral by a sum.

Instead of using trigonometric functions the function f can be expressed as complex exponential terms. The definitions of complex Fourier series and coefficients are given in Appendix A.

The frequency spectrum of a periodic signal depends on the parameters and shape of the signal. An important parameter which influences the spectrum of a signal is the transition time. To show the influence of this parameter a periodic trapezoidal wave is considered. The signals and the corresponding frequency spectra are represented in Figure 6.1.1 for the transition times 5 ns and 10 ns.

The amplitudes of both signals in Figure 6.1.1(a) are maintained constant, namely 100 V. In Figure 6.1.1(b) the frequency spectum is represented. The common property is that both spectra are decreasing with the frequency. From the comparison of the curves, it is evident that an increase of the frequency content is resulted by a significant decrease of the signal transition time.

An other important parameter which may affect the frequency content of a signal is the amplitude. In Figure 6.1.1(c) two periodic trapezoidal waves having the same slope and the amplitudes 100 V and 60 V are represented. Their frequency spectra are compared in Figure 6.1.1(d). This figure shows the same values for the common frequencies. The difference in the spectrum comes only from the frequencies which are not shared by both

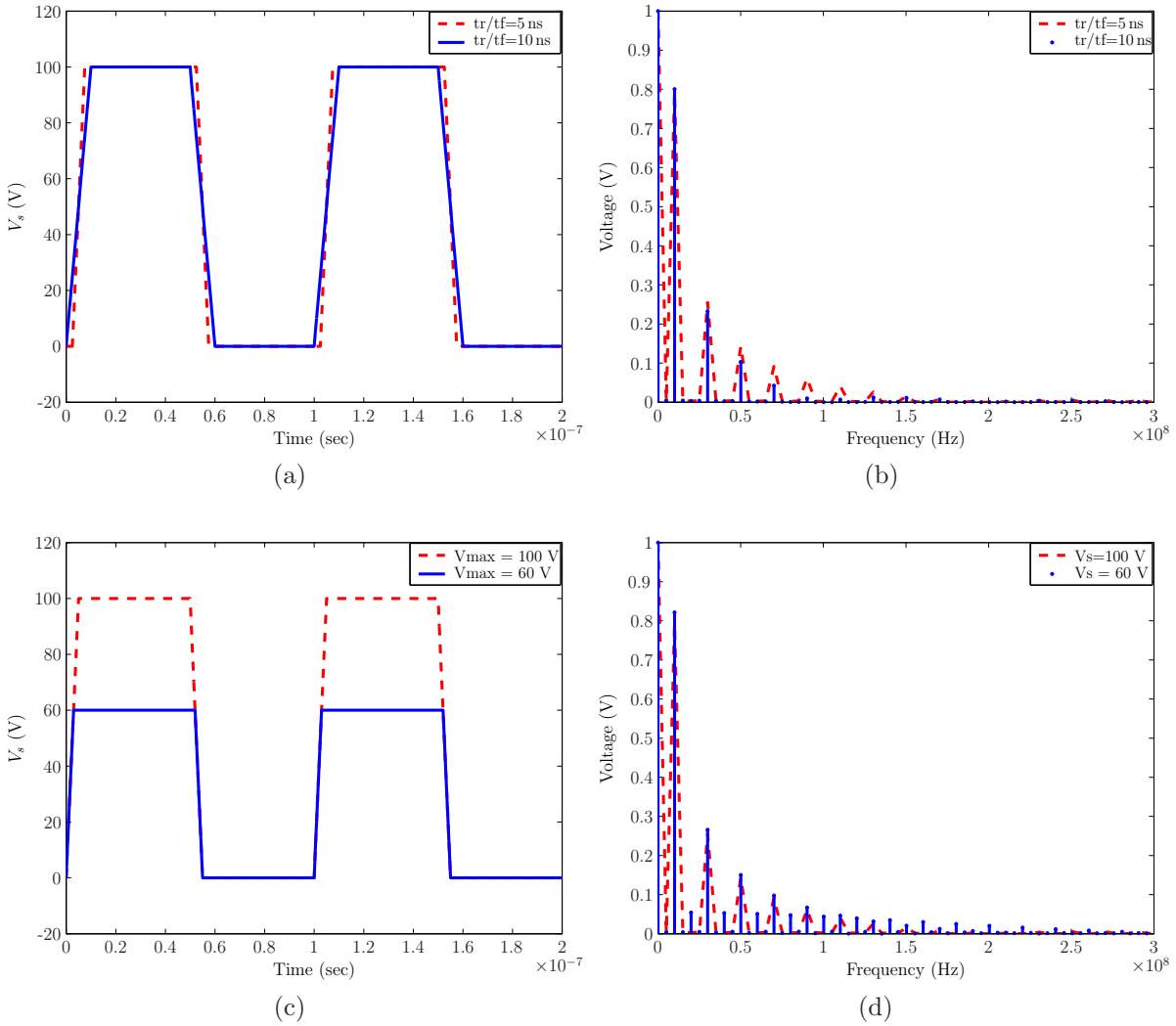


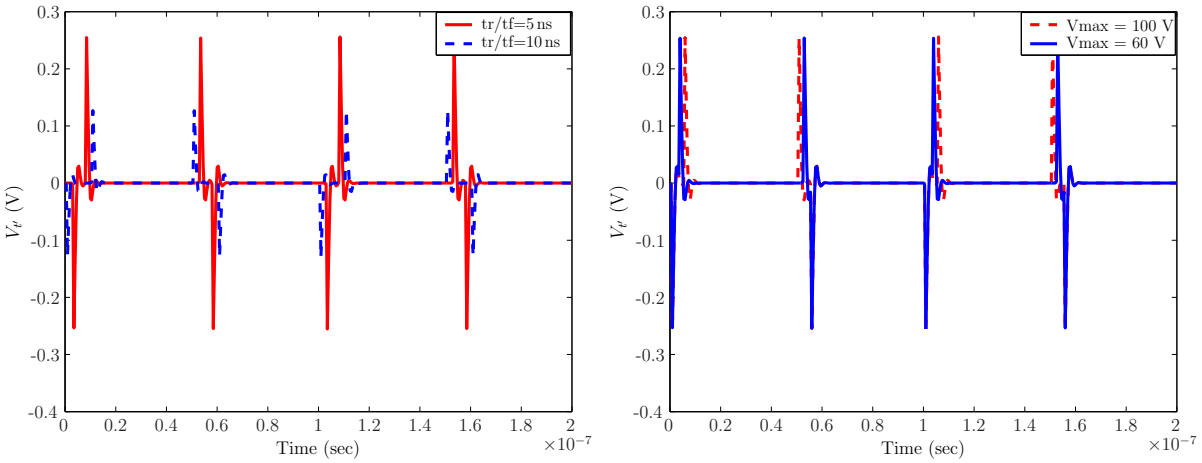
Figure 6.1.1: Frequency spectrum for different transition times and amplitudes for a trapezoidal wave

signals simultaneously. It is obvious that both spectra have no important frequency components above 200 MHz. Therfore the analysis of the dominant signal paths can be limited to the frequency range of the excitation impulses.

The transient analysis of the linear circuit in Figure 5.2.8 is carried out considering the excitation signals represented in Figure 6.1.1(a) and 6.1.1(c). The transition time of a trapezoidal can model approximately the slope of an ESD signal. The scattering parameter matrices computed in Section 5.2.5 are inserted in a HSPICE circuit netlist containing the impulse voltage sources and the transmission lines terminations. The transient analysis of this netlist is then performed to compute the coupling noise impulses at the target load R_1.

Figure 6.1.2 presents the time domain simulation results for the input signals in Figure 6.1.1. The Figure 6.1.2(a) shows the coupling transient impulses for two trapezoidal input waves with 5 ns and 10 ns transition times. As shown, a significant coupling can be observed for the wave with a transition time of 5 ns. Figure 6.1.2(b) shows the coupling

impulses for two trapezoidal input excitations with the same slope, but different amplitudes of the input voltage. For both voltage amplitudes similar peaks of the coupling impulses are obtained. As a result, the frequency content, or the signal transition time, of the excitation impulses is the parameter which affects essentially their propagation at the PCB-level.



(a) (b)

Figure 6.1.2: Coupling voltage impulses at the target resistance R_1 of the circuit in Figure 5.2.8 for various parameters of a trapezoidal excitation signal: (a) different signal transition times, (b) different amplitudes

6.1.2 Fourier Transformation

The Fourier transformation converts signals from the time domain to the frequency domain. The spectrum of a signal represented by a function f is defined by

$$F(\omega) = \int_{\infty}^{+\infty} f(t)\, e^{-j\omega t}\, dt. \tag{6.1.6}$$

A given signal occupies a frequency spectrum. The Inverse Fourier Transformation (IFT) is given by

$$f(t) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} F(\omega)\, e^{j\omega t}\, d\omega. \tag{6.1.7}$$

In digital systems the signal $f(t)$ and its spectrum $F(\omega)$, respectively, are sampled at discrete time and frequency points. The Discrete Fourier Transformation (DFT) is defined by

$$F(n) = \sum_{k=0}^{N-1} f(k)\, e^{-j\,\frac{2\pi k\, n}{N}}, \qquad n = 0, 1, \ldots, N-1 \tag{6.1.8}$$

where $F(n)$ is the nth coefficient of the DFT, and $f(k)$ denotes the kth sample of the time signal which consists of a number N of samples. The inverse operation (IDFT) is defined by

$$f(k) = \frac{1}{N} \sum_{n=0}^{N-1} F(n)\, e^{j\,\frac{2\pi\, k\, n}{N}}, \qquad k = 0, 1, \ldots, N-1. \tag{6.1.9}$$

These expressions depend on the sampling period Δt of the signal and the number of time samples N. The frequency spectrum is choosen at equally spaced frequencies

$$n\,\Delta f = \frac{n}{N\Delta t}, \qquad n = 0,\, \pm 1,\, \pm 2, \ldots,\, \pm\frac{N}{2}.$$

6.1.3 Simulation Example

A trivial time domain analysis method of linear circuits can be formulated by solving the transfer function in the frequency domain and converting back into time domain using Inverse Fourier Transformation (IFT). Then the response of the circuit at any time can be determined by convolving the impulse response with an input waveform in every iteration. The computational effort required with this type of methods is proportional to the square of the number of time points in simulation, because the convolution operation has to be extended over the entire past history. This makes the method computationally inefficient and limits its usability. Alternatively the product of the transfer function with the frequency spectrum of the input waveform can be determined. Time domain response is then obtained directly using IFT.

The transient analysis of the circuit in Figure 5.2.8is performed using the two-port scattering matix generated by the dominant paths approach. The transfer function relating the target resistance to the voltage source is determined. The time domain response is obtained using the Inverse Fast Fourier Transformation (IFFT) approach. Figure 6.1.3 presents the coupling voltage impulses $V_{t'}$ for a trapezoidal excitation signal with an amplitude of 100 V, a width of 50 ns, and a rise and fall times of 5 ns.

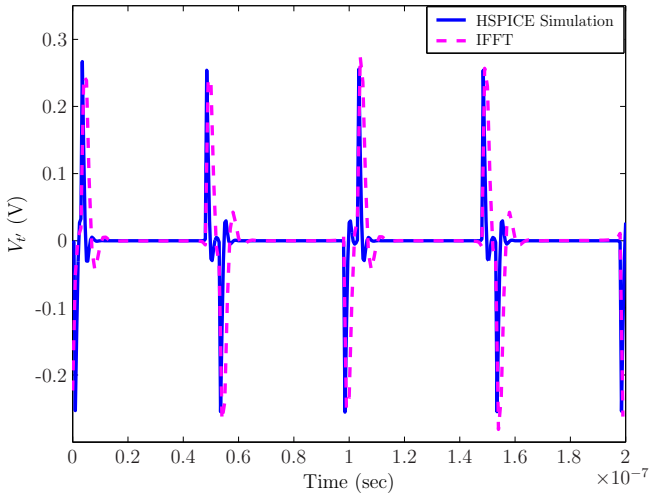


Figure 6.1.3: Time domain response of the dominant paths using the IFFT approach

The trapezoidal wave is synthesized using 40 harmonics of its fundamental frequency 10 MHz. For the validation the curve representing the conventional HSPICE transient

simulation is also represented in the same figure. Both curves are very close to each other. The accuracy of the time domain analysis depends on the characterization of the linear part of the circuit, i.e. the number of dominant signal paths extracted in the frequency domain, and the accurate synthesis of the harmonic signal applied to the system. More accuracy can be obtained by increasing the numbers of dominant signal paths considered and the harmonics in the input signal.

In order to compute the coupling voltage impulses associated to each of the three dominant paths in the schematic of Figure 5.2.8, time domain analysis of each of these paths is performed. Figure 6.1.4 shows the results in terms of coupling voltages. Figure 6.1.4(a) represents also the resulting curve obtained by superimposing all the three paths. The zoomed region around the first impulse is shown in Figure 6.1.4(b). It is clear that the amplitude of first dominant path $\mathcal{P}_1$ is very close to the one obtained by the superposition of all the three paths. Therefore the coupling voltages from the second and third paths, and their impact on the target device, can be neglected.

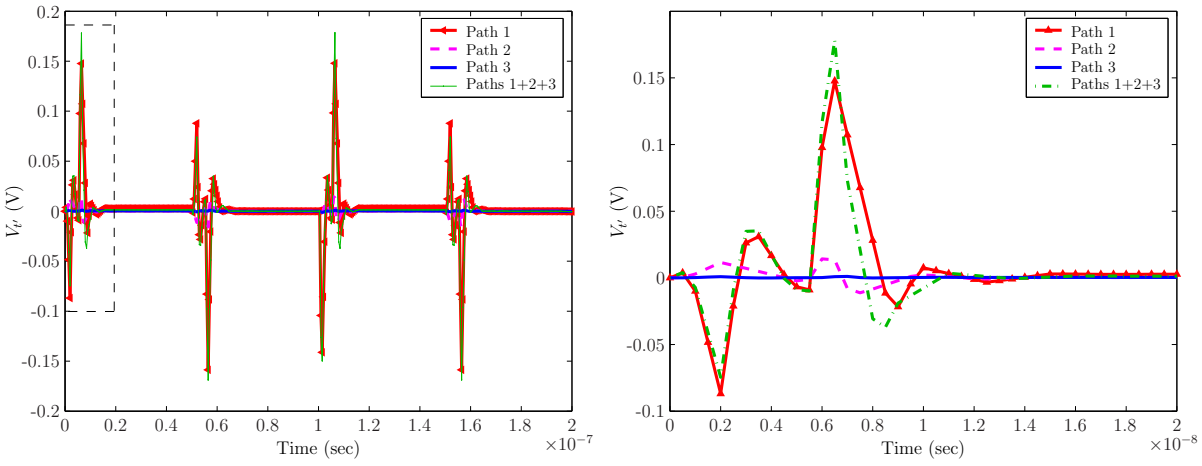


Figure 6.1.4: Time domain responses of the three dominant propagation paths indicated in the schematic in Figure 5.2.8

6.2 Signal Path with a Nonlinear Termination

Digital integrated circuit devices which appear onto the signal paths as terminations are characterized by nonlinear models. These models are described in the time domain. In this section some hybrid methods are used to simulate the transient behaviour of individual dominant signal paths. The Harmonic Balance technique and the HSPICE S-parameter simulation are applied for the analysis of many examples.

6.2.1 Conventional Nonlinear Methods

Conventional nonlinear circuit simulation techniques are based on the formulation of the system equations that can be generally written as a set of first order nonlinear differential

equations. The solution of these equations can be determined in the frequency domain or in the time domain. The domain of analysis depends on the nature of the circuit and the quantity to be solved.

The frequency domain steady state behavior of a microwave circuit is typically of great interest if some quantities, like frequency, power, noise, and transfer characteristics such as gain and impedance, should be determined. Therefore all these can only be determined accurately for linear circuits in the steady state. Time domain analysis is however of great importance when analyzing of nonlinear networks. Time domain methods generally use numerical integration to calculate the instantaneous value of the output of an element from the instantaneous value of its input. An example of such computed aided analysis technique using this approach is the popular circuit simulator SPICE. The transient analysis using this tool requires a long simulation time and integration over an excessive number of periods.

A more important class of nonlinear methods are the hybrid methods which combine the frequency and time domain techniques. An example of hybrid methods is the HB technique which is a more useful method for analyzing microwave circuits. Unfortunately, it is limited to systems having only harmonically related signal components [68, 69].

6.2.2 Harmonic Balance Technique

The Harmonic Balance is a technique for computing the steady state response of nonlinear circuits excited by single or multiple periodic sources. It is based on the assumption that for a given sinusoidal excitation there exists a steady state solution that can be approximated to satisfactory accuracy by means of a finite Fourier series. Therefore the solution can be expressed as a sum of steady state sinusoids that includes the input frequencies in addition to any significant harmonics or mixing terms. A circuit with a single input source will require a single tone HB simulation [70]. A solution waveform is approximated as follows:

$$v(t) = \mathrm{Re}\left\{\sum_{k=0}^{K} V_k e^{jk\,\omega_0\,t}\right\}, \tag{6.2.1}$$

where ω_0 is the fundamental radian frequency of the source, the V_k's are the complex Fourier coefficients that the HB analysis computes, and K is the order of truncation. A circuit with multiple input sources will require multitone HB simulation. In this case, the steady state solution waveforms are approximated with a multidimensional truncated Fourier series as follows:

$$v(t) = \mathrm{Re}\left\{\sum_{k_1=0}^{K_1}\sum_{k_2=0}^{K_2}\cdots\sum_{k_n=0}^{K_n} V_{k_1,k_2,\ldots,k_n} e^{j(k_1\omega_1+k_2\omega_2+\ldots+k_n\omega_n)\,t}\right\}, \tag{6.2.2}$$

where n is the number of tones, or sources, $\omega_1 \ldots \omega_n$ are the fundamental radian frequencies of each source, and $K_1 \ldots K_n$ are the number of harmonics for each tone.

Harmonic Balance technique divides a nonlinear system into a strictly linear and a strictly nonlinear network. In Figure 6.2.1 the separation of an electrical network into linear and

nonlinear parts is shown. The linear part in this figure is connected with K source generators and to the nonlinear part through an interface of M ports.

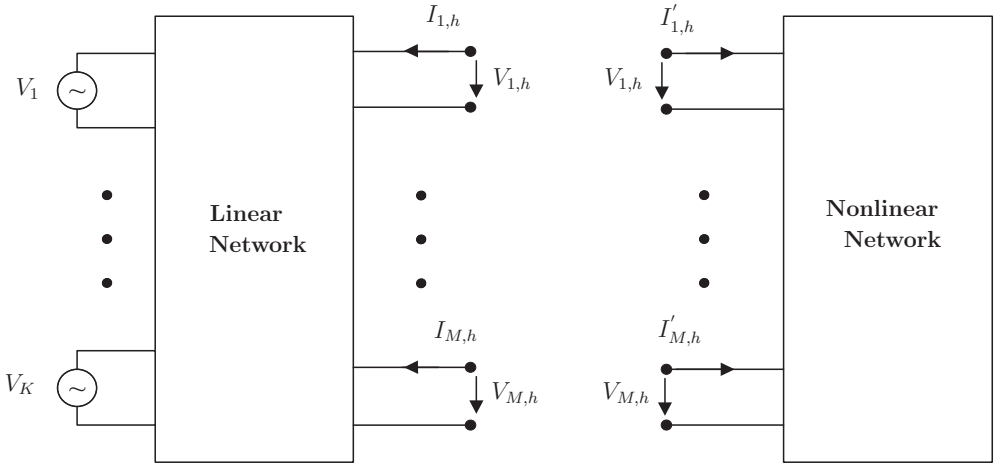


Figure 6.2.1: Hybrid analysis of circuits with nonlinear elements

The linear network is described in the frequency domain, e.g. through usage of admittance matrix $\boldsymbol{Y}$, and the nonlinear network is described in the time domain. The basic approach used to solve a system of nonlinear circuit equations is first to formulate an error function and then to perform a minimization by the use of an algorithms such as the *Newton* iteration scheme. A solution is found by optimizing voltages between the linear and nonlinear parts until both frequency and time domain analyzes agree sufficiently on the port voltages and currents. That means the port voltages and currents on all harmonics h must agree. This is done for a fixed set of frequency points, or harmonics, as dictated by the input parameters.

The currents flowing from nodes into linear elements including all distributed elements are calculated by means of straightforward frequency domain linear analysis method. The instantaneous currents for the nonlinear network can be described by the nonlinear functions of the voltages which describe the behaviour of the nonlinear devices. According to *Kirchhoff*'s Current Law in the frequency domain, the objective, or error function can be derived at all nodes at the interface ports. This error function should be minimized until acceptable convergence is achieved.

Assuming the nonlinear network has M nodes, the instantaneous current into the linear network at the p-th node is the sum of N frequency components such that

$$I_p = \sum_{q=1}^{N} \mathrm{Re}(I_{p,q} e^{j\omega_q t}). \tag{6.2.3}$$

Similarly, the current into the nonlinear network at the p-th node is

$$I'_p = \sum_{q=1}^{N} \mathrm{Re}(I'_{p,q} e^{j\omega_q t}). \tag{6.2.4}$$

In (6.2.3) and (6.2.4), $I_{p,q}$ and $I'_{p,q}$ are the phasors of the q-th frequency components of current flowing into the linear and nonlinear subcircuits, respectively. The instantaneous voltage at the p-th node is given by

$$V_p = \sum_{q=1}^{N} \mathrm{Re}(V_{p,q} e^{j\omega_q t}), \tag{6.2.5}$$

where $V_{p,q}$ is the phasor of the q-th frequency component of voltage at the p-th node. At the interface nodes *Kirchhoff*'s Current Law must be satisfied, so that $I_p + I'_p = 0$ for all p from 1 to M. Therefore, the steady state solution of the circuit can be found by minimizing the objective function

$$\mathcal{E} = \sum_{p=1}^{M} \sum_{q=1}^{N} \mid I_{p,q} + I'_{p,q} \mid^2 . \tag{6.2.6}$$

Since the current phasors I_p and I'_p are functions of all node voltage phasors at the interface ports, equation (6.2.6) can be written as

$$\mathcal{E} = \sum_{j=1}^{2} \sum_{p=1}^{M} \sum_{q=1}^{N} \Theta^2_{j,p,q}(\boldsymbol{V}) = \sum_{i=1}^{2MN} \Psi^2_i(\boldsymbol{V}), \tag{6.2.7}$$

where

$$\Theta_{1,p,q}(\boldsymbol{V}) = \mathrm{Re}(I_{p,q} + I'_{p,q}),$$

and

$$\Theta_{2,p,q}(\boldsymbol{V}) = \mathrm{Im}(I_{p,q} + I'_{p,q}).$$

In (6.2.7) the elements $\Psi_i(\boldsymbol{V})$ are equal to the elements $\Theta_{j,p,q}$, where the subscript i represents a unique choice for j, p, and q. $\boldsymbol{V}$ is a vector of real and imaginary parts of the phasors of the node voltages at the interface ports.

The evaluation of the objective function as a function of the node voltage phasors requires the calculation of the node current phasors given the node voltage phasors. Its minimization can be achieved using a variety of iteration techniques [68, 69, 48]. A suitable technique to minimize such a sum of squares is the *Newton*'s method [48]. This method finds the minimum of $\mathcal{E}$ with respect to $\boldsymbol{V}$ using the iterative procedure

$${}^{i+1}\boldsymbol{V} = {}^{i}\boldsymbol{V} - \boldsymbol{J}^{-1}({}^{i}\boldsymbol{V})\, \Psi({}^{i}\boldsymbol{V}), \tag{6.2.8}$$

where the leading superscripts i are the iteration numbers, and $\boldsymbol{J}$ is the *Jacobian* matrix of Ψ. For its determination the partial derivatives of the node current phasors with respect to the real and imaginary parts of the node voltage phasors for all interface nodes and frequencies computed.

The element of the matrix $\boldsymbol{J}$ in the $(2j-1)$-th row and k-th column at the i-th iteration is given by

$$\left[\boldsymbol{J}({}^{i}\boldsymbol{V})\right]_{2j-1,k} = \frac{\partial \Psi_{2j-1}({}^{i}\boldsymbol{V})}{\partial \mathrm{Re}({}^{i}\boldsymbol{V}_k)},$$

and the element in the $(2j)$-th row and k-th column is

$$\left[\boldsymbol{J}({}^{i}\boldsymbol{V})\right]_{2j,k} = \frac{\partial \Psi_{2j}({}^{i}\boldsymbol{V})}{\partial \mathrm{Im}({}^{i}\boldsymbol{V}_k)}.$$

The calculation of the *Jacobian* requires partial derivatives of the current phasors with respect to the real and imaginary parts of the node voltage phasors for all nodes of the nonlinear subcircuit and frequency components.

The diagram in Figure 6.2.2 illustrates the *Newton* method for the scalar case. A function f of a single variable v is considered for which a solution for the root v^* should be found. For this method the first step is to make an initial guess, $v^{(0)}$, then linearize about $v^{(0)}$. Then solve for the next guess $v^{(1)}$, and so on. As k becomes large, $v^{(k)}$ will asymptotically approach the exact solution v^*.

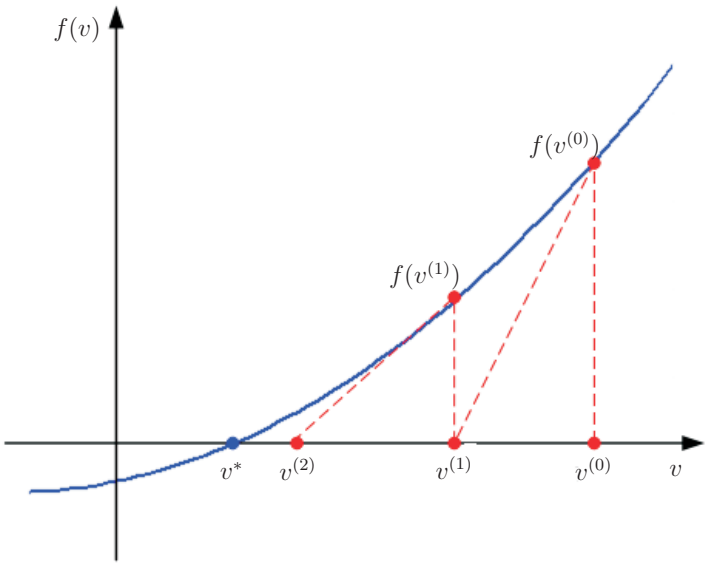


Figure 6.2.2: Illustration of the *Newton*'s method [70]

The steps used by the Harmonic Balance technique are described by Algorithm 6.2.1. For signals with small transitions a few number of frequency spectra may be sufficient for accurate analysis. Moreover, if a circuit contains weakly nonlinear devices, an efficient and accurate analysis will be obtained. In strongly nonlinear circuits containing waveforms with sharp transitions, the number of Fourier coefficients needed to describe the waveform accurately is large. In this case oversampling will help to get convergence.

Algorithm 6.2.1 Algorithm Harmonic Balance

1: Specify fundamental frequency, number of harmonics, voltage sources
2: Calculate the admittance matrix for the linear network
3: Assume an initial set of interface port currents
4: Calculate interface port voltage due to interface port current in the linear network
5: Convert interface port voltage from frequency domain to time domain
6: Using time domain port voltages, compute the time domain current in the nonlinear network
7: Convert time domain current to the frequency domain
8: Compare the linear port current to the nonlinear port current
9: **if** currents are almost the same at each frequency **then**
10: the solution is found
11: **else if** they are not almost the same **then**
12: using some optimization technique compute the new interface port current and go to line 4
13: **end if**

6.2.3 Example of a Linear Load

The Harmonic Balance technique is mainly used to analyze the steady state analysis of nonlinear circuit, but it can also be applied to solve linear circuits. As an example the circuit in Figure 5.2.8 is again analyzed using the HB technique. In Figure 6.2.3 the time domain response in terms of voltage impulses, obtained using the dominant path approach combined with the HB technique, is represented. The results of the dominant path approach combined with HB technique shows a good convergence to the curve obtained by the conventional HSPICE transient simulation. The small difference between these results may be related to the number of harmonics considered by the HB approach.

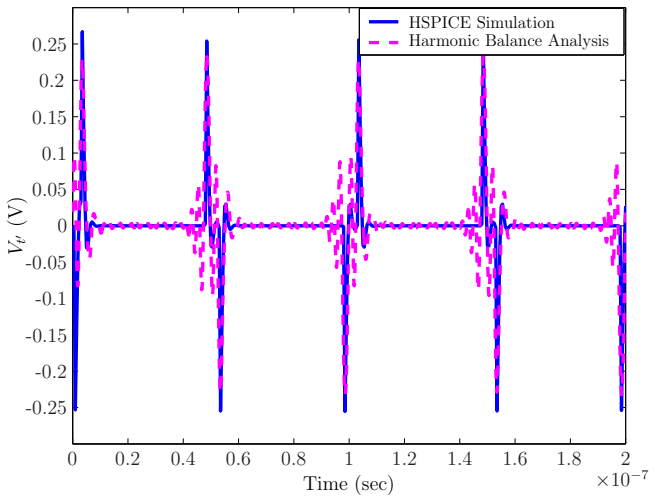


Figure 6.2.3: Time domain analysis of the circuit in Figure 5.2.8 by the Harmonic Balance technique

6.2.4 Example of a Passive Nonlinear Device

The Harmonic Balance technique is used to perform the time domain analysis of the circuit depicted in Figure 6.2.4, which was analyzed in [71]. It consists of two and three parallel coupled microstrip lines, and discrete components such as resistors and capacitors. The three coupled microstrips are the same like that of the schematic in Figure 5.2.8. All the lines have a length of 4 cm. The lines that are not connected to the others are terminated with 50 Ω loads. The capacitance C and the resistance R_1 have the values of 2 pF and 100 Ω, respectively. In this example all the propagation paths relating the voltage source V_s and the load impedance of R_2=75 Ω consist only of the coupling paths, i.e. crosstalk.

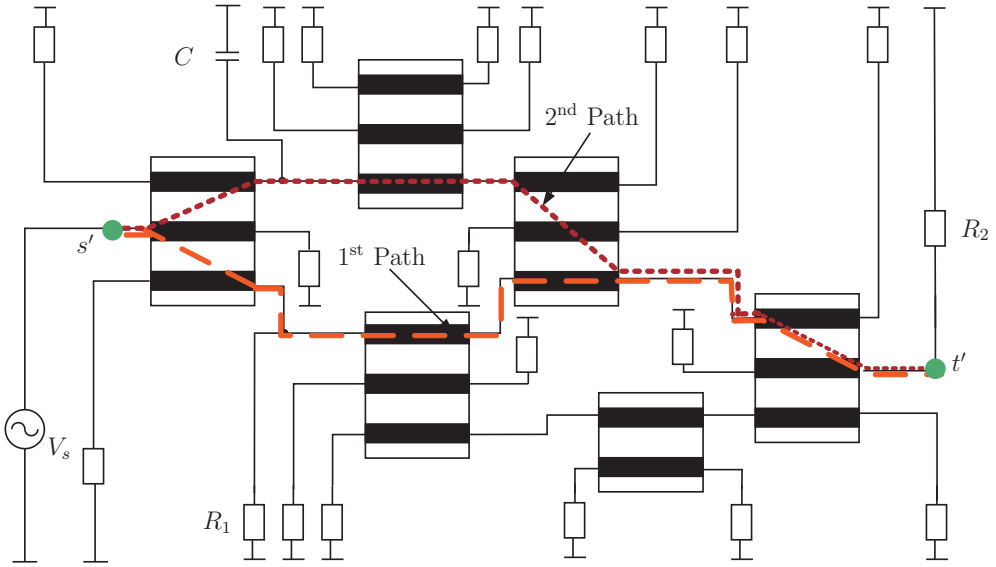


Figure 6.2.4: Interconnect circuit showing the noise propagation from the source V_s to the load R_2 [71]

Identification and Evaluation of The Dominant Paths

In the schematic of Figure 6.2.4 the circuit nodes representing the voltage source and the target load are indicated by s' and t', respectively. The first two dominant propagation paths relating the voltage source V_s and the load impedance R_2 are extracted. For this circuit the extraction is performed only at the single frequency of 1 GHz. This is sufficient because there is no change of the order of the first and second dominant paths over the frequency range of 5 GHz. In general the paths should be extracted at each discrete frequency point in the interval of analysis. The two dominant paths extracted are evaluated by their transmission coefficients. The results are shown in Figure 6.2.5.

The magnitudes of the transmission coefficient s_{12} corresponding to the first two dominant paths $\mathcal{P}_1$ and $\mathcal{P}_2$ are plotted in Figure 6.2.5(a). The remaining signal paths may be neglected over the whole frequency range considered. Clearly the most dominant path transmits the highest level of noise to the target load. Obviously the coupling noise associated to each of these paths increases with the frequency. This is due to the high frequency parasitic coupling between the transmission lines. In Figure 6.2.5(b) the response obtained from the superposition of the two paths is compared to the multiport

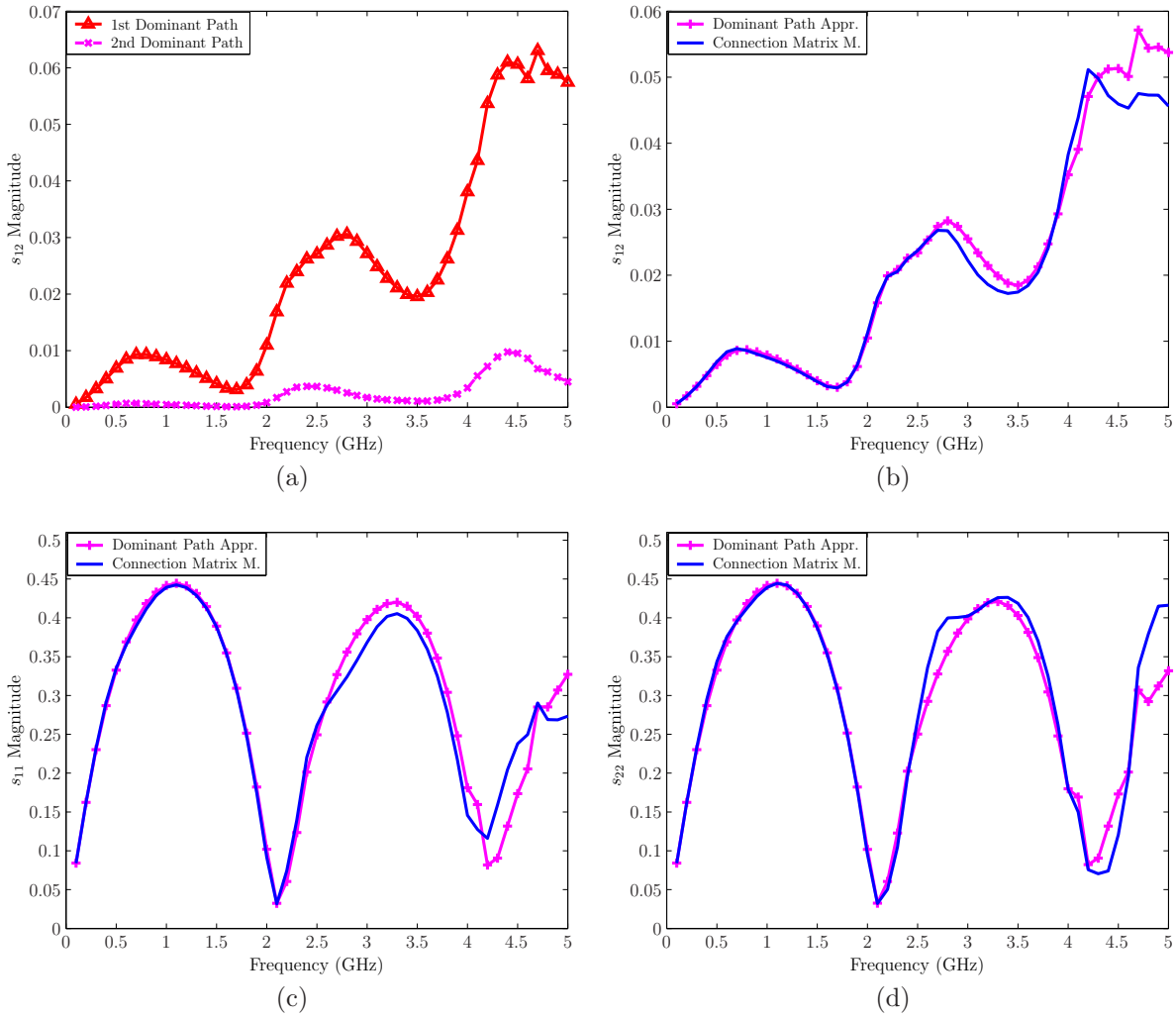


Figure 6.2.5: The magnitude of the scattering parameters relating the voltage source and the target load

connection method. The superposition of the transmission coefficients associated to these two paths shows a good agreement with the exact values of the magnitude of s_{12}. Since the circuit is passive and linear, the coefficient s_{21} is identical to s_{12} and is not determined here. The propagation paths corresponding to its computation have also the same order and travel over the same circuit nodes in an opposite direction.

The reflection coefficients s_{11} and s_{22} are computed considering the first dominant path identified by the algorithm. The corresponding paths are not drawn in Figure 6.2.4, since the focus is only on the signal transmission between the voltage source and the target load. In Figure 6.2.5(c) the magnitude of s_{11} is represented over a frequency range of 5 GHz. Again the results are validated by the multiport connection method. The approximated reflection coefficient $s_{11}(\mathcal{P}_1)$ associated to the most dominant path reflecting the waves at the source is compared with the validation method [37, 45]. In Figure 6.2.5(d) the reflection coefficient $s_{22}(\mathcal{P}_1)$ is compared to the exact curve computed using the multiport connection method. For both reflection coefficients good convergence betweeen the results of the dominant path approach and the validation method are obtained. Consequently

an equivalent two-port scattering matrix approximating the system relating the voltage source and the target load is obtained. It is given as

$$\boldsymbol{S} \simeq \begin{pmatrix} s_{11}\left(\mathcal{P}_1\right) & \sum_{r=1}^{2} s_{12}\left(\mathcal{P}_r\right) \\ \sum_{r=1}^{2} s_{21}\left(\mathcal{P}_r\right) & s_{22}\left(\mathcal{P}_1\right) \end{pmatrix}. \tag{6.2.9}$$

The solution of this matrix gives the incident and reflected power waves at the network ports. Thus, the corresponding voltage and current responses at the network terminals can be derived. In Figure 6.2.6 the voltage transfer function is represented.

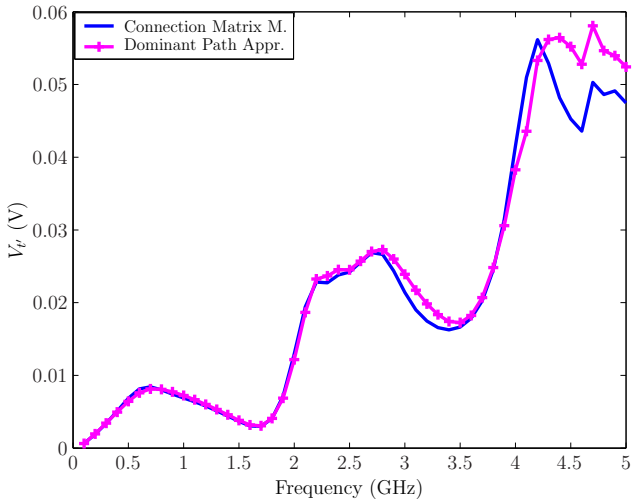


Figure 6.2.6: Voltage phasor of the transfer function

The transfer function obtained from the two-port scattering matrix determined by the dominant path approach is validated using the one derived by the multiport connection method. The results using the dominant signal path approach agree very well with the ones of the validation method. A small deviation is observed for the frequencies above 4.2 GHz.

Target Linear Termination

In the following the time domain analysis is performed by combining the frequency domain results of the dominant path approach with the Harmonic Balance technique. First a sine voltage excitation with an amplitude of 100 V, and a frequency of 10 MHz is applied to the circuit in Figure 6.2.4. The response to this excitation at the target resistance R_2 is depicted in Figure 6.2.7(a).

In the same figure a comparison with the multiport connection method combined with the HB technique is represented. The curves representing both approaches are very close to each others. The response to a trapezoidal voltage impulse with an amplitude of 100 V, a basic frequency of 10 MHz, and a transition time of 5 ns is depicted in Figure 6.2.7(b). That is, the transient coupling impulses at the target resistance R_2. To synthesize the

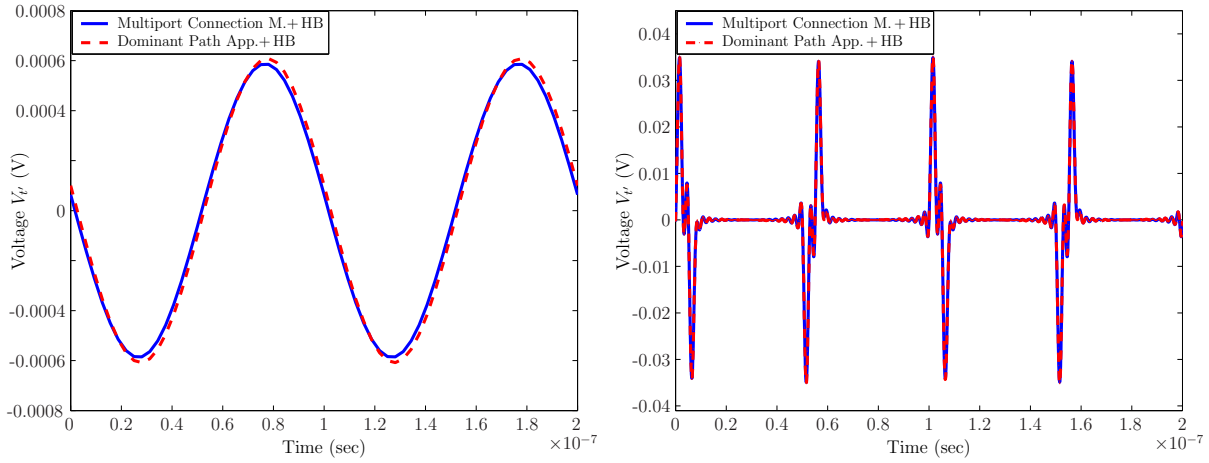


Figure 6.2.7: HB analysis of dominant signal paths for a: (a) sine, and (b) trapezoidal excitation

trapezoidal voltage 40 harmonics are used. Again, the curve representing the results is very close to that delivered by the validation method.

Target Nonlinear Termination

The target resistance R_2 in the schematic of Figure 6.2.4 is now replaced by a semiconductor diode of type d1n4148 with the parameters (C_{j0}=5 pF, ϕ=0.6, η=0.45, R_s=0.8 Ω, I_s=7 nA, τ_D=6 ns). A voltage source of trapezoidal impulses is applied at the input port of the system. The Harmonic Balance is used to compute the effect of the nonlinear diode on the behaviour of the propagating parasitic impulses. For this reason the periodic input voltage v is decomposed using Fourier series into a number N of harmonics approximating its shape. The truncated exponential Fourier series is expressed by

$$v(t) = \sum_{n=0}^{n=N} c_n \, e^{jn\,\omega_0 t},$$

where ω_0 is the fundamental radian frequency. The complex Fourier coefficients c_n are defined by

$$c_n = \frac{1}{T} \int_T v(t)\, e^{-jn\,\omega_0 t}\, dt,$$

where T is the period of the voltage v.

The impedance matrix $\boldsymbol{Z}$ of the linear interconnect part is computed from the two-port scattering matrix obtained by the dominant signal path approach using (3.1.12). The elements of its equivalent T-network are given by

$$\begin{cases} z_1 = z_{11} - z_{12} \\ z_2 = z_{12} \\ z_3 = z_{22} - z_{12} \end{cases}.$$

The simplified electrical equivalent circuit relating the noise source and the target diode is represented in Figure 6.2.8.

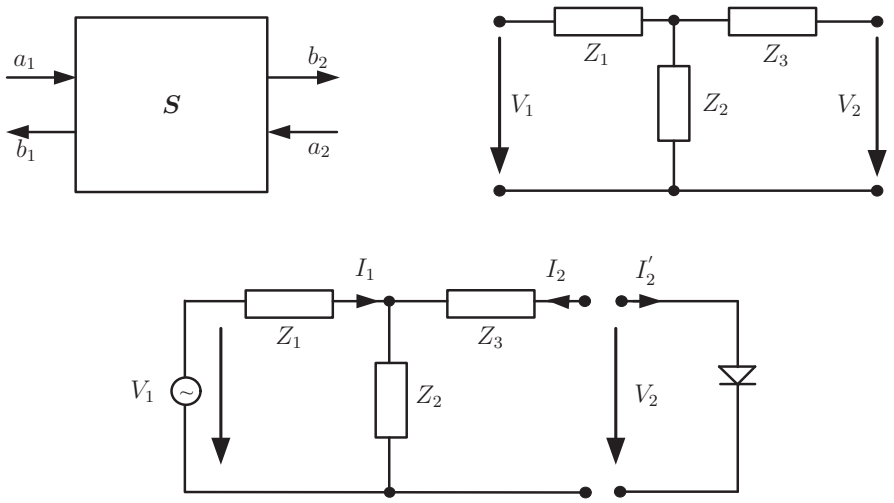
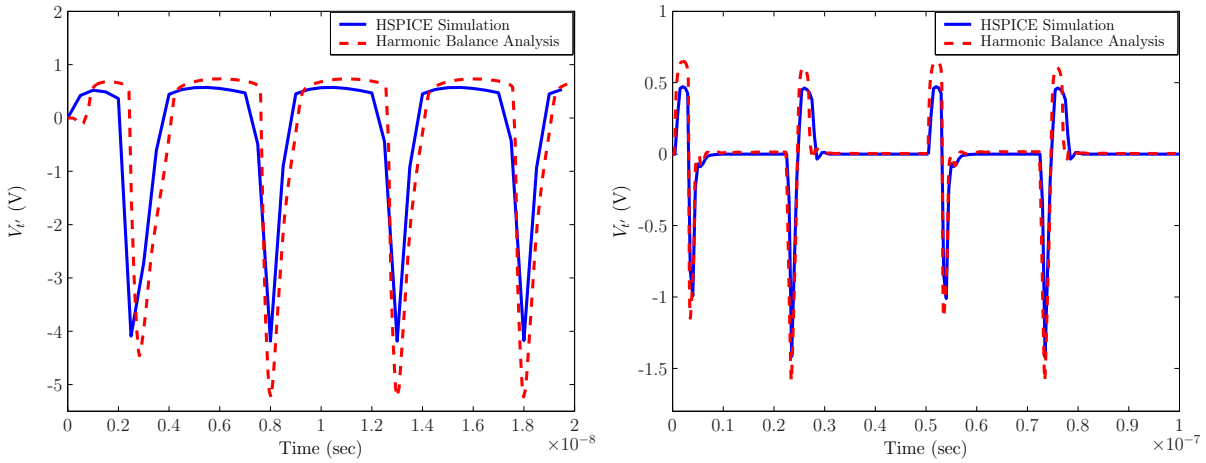


Figure 6.2.8: Linear/nonlinear interface with one port for the HB analysis of the circuit in Figure 6.2.4 with a diode [71]

The nonlinear analysis is performed as follows. After the phasor voltage V_2 is computed for all the harmonics composing the input signal V_1 a conversion using an IFFT algorithm is performed to get the time domain voltage at the interface port. The time value is used in the nonlinear analysis to compute the time domain current I_2' from the diode equation. The nonlinear time domain current value should be converted into the phasor current I_2. In the case where the currents at both circuit parts are matched, i.e. their difference is smaller than a specified threshold, a solution is found. Otherwise the *Newton* method is used in an iterative way until an approximate value of I_2 satisfying the matching procedure is found.

The simplified network in Figure 6.2.8 is simulated in time domain for a sine wave excitation with a frequency of 200 MHz, and an amplitude of 1 kV, and for a trapezoidal excitation with rise and fall times of 2 ns, a duration of 20 ns, a period of 50 ns, and a voltage amplitude of 1 kV. The linear part of the circuit is first characterized by the reflection and transmission coefficients computed over the frequency range of 1 GHz. For this simulation the most dominant signal path is only considered to compute each of these coefficients.

The response to the input sine wave voltage at the diode pin is depicted in Figure 6.2.9(a). In the same figure the curve of the HB technique is compared to the one of the standard HSPICE simulation. The response to the trapezoidal voltage wave is presented in Figure 6.2.9(b). The trapezoidal voltage is approximated using 30 harmonics of its fundamental frequency 20 MHz. The crosstalk voltage at the target diode is computed using the dominant path approach combined with the Harmonic Balance technique. The results for both excitations are validated by the HSPICE transient analysis. The deviation between the responses of the HB analysis and the validation method is related to the number of harmonics used, the optimization method, and the number of dominant paths considered by the approach.



(a) (b)

Figure 6.2.9: Harmonic Balance analysis of the circuit in Figure 6.2.4 loaded with a diode for a: (a) sine excitation, and (b) trapezoidal excitation

6.2.5 Example of an Active Nonlinear Device

The simulation of a complete dominant signal path consisting of linear interconnects and digital integrated circuit devices switched at some terminations is carried out in [66]. In this subsection the same circuit example, shown in Figure 6.2.10, is again analyzed. It consists of two and three parallel coupled microstrip transmission lines (of width 200 μm, height 35 μm) separated by a space of 200 μm above a FR4 ($\varepsilon_r = 4.2$) dielectric substrate of 365 μm height. The transmission lines which are not connected to the others are matched. The transmission line structures are characterized by their scattering parameter matrices. A voltage source representing a transient impulse and a nominal signal source are applied at the terminals 1 and 2 respectively.

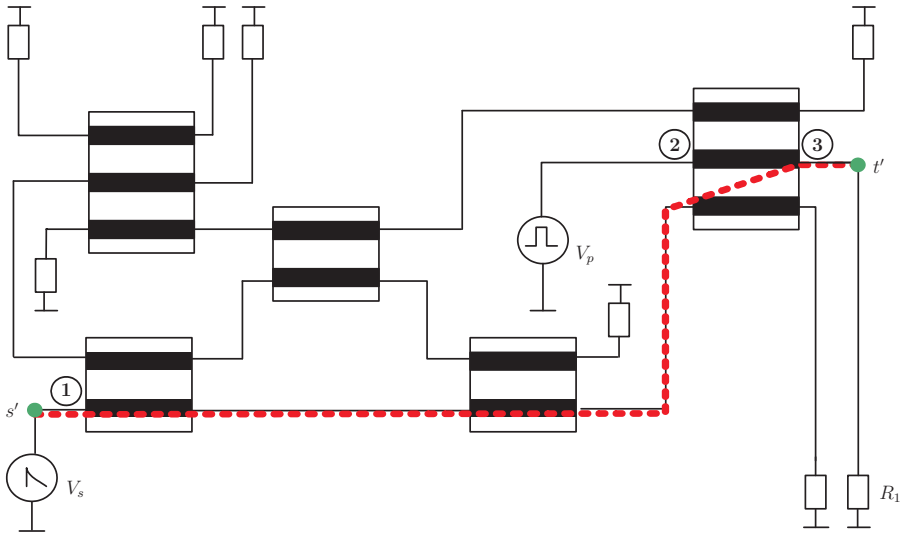


Figure 6.2.10: Interconnect schematic with a disturbance source and a nominal signal source [66]

The most dominant propagation path relating the disturbance source V_s and the target

resistance R_1 is extracted at the frequency of 2 GHz. For this interconnect it is sufficient to consider only the first weighted path, which transmits a significant amount of noise to the load R_1. This is, because this path remains the most dominant one over all the other frequency points considered. This path is drawn on the circuit schematic (dashed line).

The characterization of the most dominant noise path is performed in terms of the transmission coefficients, i.e. $s_{13}(\mathcal{P}_1)$. The results of all the scattering parameters are depicted in Figure 6.2.11. The comparison of the magnitude of the coefficient $s_{13}(\mathcal{P}_1)$ with the reference results, provided by the multiport connection method, is shown in Figure 6.2.11(a). The curves representing the dominant path approach and the validation method are identical over the whole range of the frequency analyzed. Thus, the remaining propagation paths may be neglected.

The dominant path approach can be applied to any linear circuit with more than two external ports connected to its noise, or signal sources. The complexity of computing the characterization matrix associated to the dominant signal paths can be reduced considering the passivity property. Since the propagation paths are extracted over the passive linear part of the network, the transmission coefficient s_{31} is identical to s_{13}. The dominant propagation path $\mathcal{P}_1$ associated to its computation is the same like that associated to s_{13}. That means that the most transmitted power from the target load R_1 to the source V_s flows through the same way, but in opposite direction. Moreover, there exist only one dominant path as was the case for s_{13}.

Using the same procedure the transmission coefficients s_{12} and s_{23}, representing the transfer of the power between the circuit ports 1, 2, and 3, are computed. The results in terms of the magnitudes are depicted in Figures 6.2.11(b) and 6.2.11(c). In addition the magnitude of the reflection coefficients s_{11}, s_{22} and s_{33} are also computed considering a number of reflection paths approximating their exact responses (Figures 6.2.11(d), 6.2.11(e), 6.2.11(f)). Also identical results are obtained here considering only the dominant signal paths reflecting the most power to each input port itself. The results in terms of phases, not presented here, agree also very well with that of the validation method. In general the number of the paths delivering a good approximation may be different for each of the reflection or transmission coefficients. For lucidity and because the focus of interest is only on the noise transmitted from the noise source V_s to the load R_1, these paths are not drawn in the circuit schematic.

The resulting three-port scattering matrix associated to the dominant signal paths is given as

$$\boldsymbol{S} \simeq \begin{pmatrix} \sum_{r=1}^{3} s_{11}(\mathcal{P}_r) & s_{12}(\mathcal{P}_1) & s_{13}(\mathcal{P}_1) \\ s_{12}(\mathcal{P}_1) & s_{22}(\mathcal{P}_1) & s_{23}(\mathcal{P}_1) \\ s_{13}(\mathcal{P}_1) & s_{23}(\mathcal{P}_1) & s_{33}(\mathcal{P}_1) \end{pmatrix}. \tag{6.2.10}$$

Consequently a three-port network described by the scattering matrix $\boldsymbol{S}$ from the dominant paths, relating the noise voltage source (port 1), signal generator (port 2), and the target load (port 3), is synthesized.

In order to consider the chip port behaviour by the simulation of the whole dominant noise propagation path the target resistance R_1 of the circuit in Figure 6.2.10 is replaced

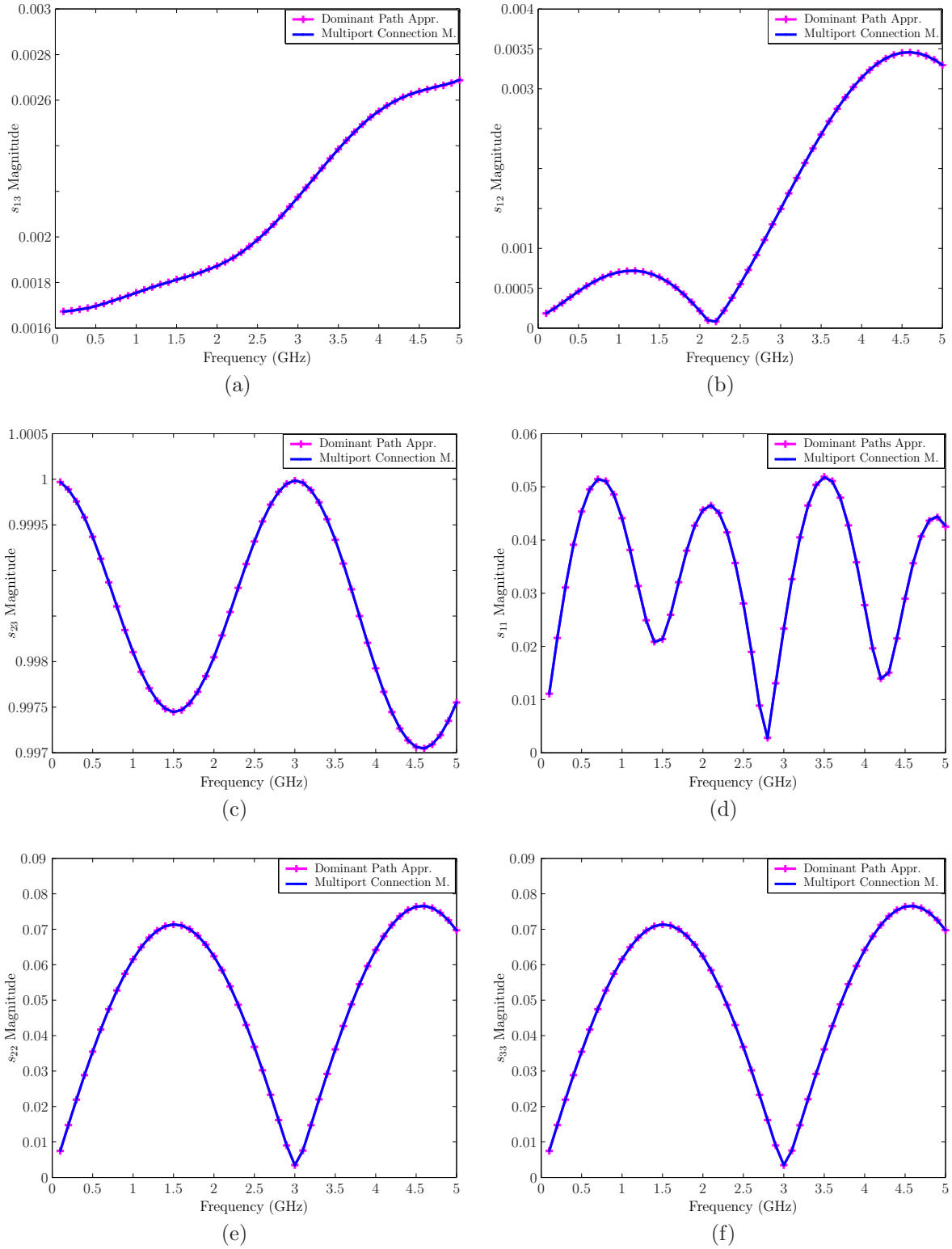


Figure 6.2.11: The magnitude of the scattering parameters: (a-c) transmission coefficients, (d-f) reflection coefficients

by a 5 V CMOS inverting buffer SN74LV04A of Texas Instruments, loaded by a shunt RC (R=100 Ω, C=2.5 pF). Another buffer of the same type which represents a chip output

port is switched to the second terminal of the resulting interconnect network. This buffer is driven by a digital data signal. The noise impulses are injected into the interconnect through the first port of the resulting network. The schematic of this reduced network with the inverters is depicted in Figure 6.2.12.

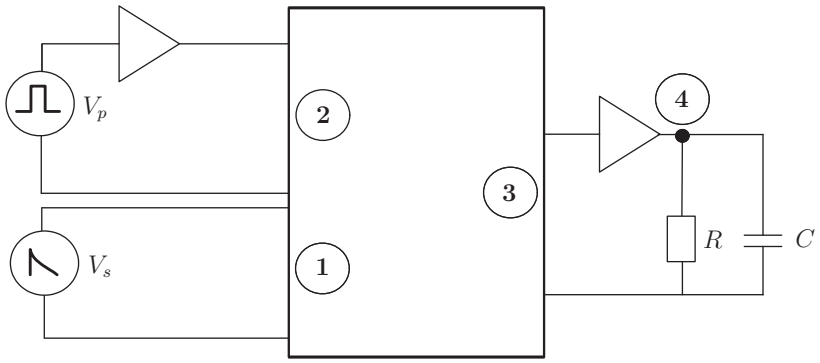


Figure 6.2.12: Simplified network structure for time domain analysis

The inverters are represented by their encrypted SPICE transistor level macromodels. The transient waveform analysis of the resulting netlist is performed using the HSPICE circuit simulator. The noise impulses and the data signal are represented in Figure 6.2.13. The noise voltage in Figure 6.2.13(a) is a repetitive trapezoidal signal V_s characterized by the rise and fall times of 5 ns, a duration of 45 ns, a period of 100 ns, and a maximum voltage value of 1 kV. To determine the influence of the noise impulses on a data signal the input bit sequence (01001000), represented in Figure 6.2.13(b), is applied at the input port of the inverter connected to the port 2 of the circuit.

The resulting waveform at the port 3 and at the pin RC are also shown in Figure 6.2.13. In Figure 6.2.13(c) the coupling impulses are superimposed to both signal states at the input pin of the second inverter. In Figure 6.2.13(d) the shape of the functional signal at the pin RC is represented. Obviously the noise impulses affect the low-states of the output data, causing static faults, i.e. logic perturbation. For voltage impulses with amplitudes exceeding the value of 1 kV the dominant transmission path between the source V_s and the load inverter becomes critical.

In general the failure is depending on the amplitude and rise/fall times of the noise impulses as well as on the dimension of the interconnection structures. The determination of the noise level that may affect the digital signal at a specified chip pin and the propagation paths of the noise provides important information on the susceptibility of electronic systems.

A comparison of the time domain response obtained from the HSPICE S-parameter simulation of the dominant signal paths with the conventional transient analysis of HSPICE is provided in Figure 6.2.13(d). The comparison between both approaches show small differences in the number of impulses coupled which are due to the time step control in the transient simulation.

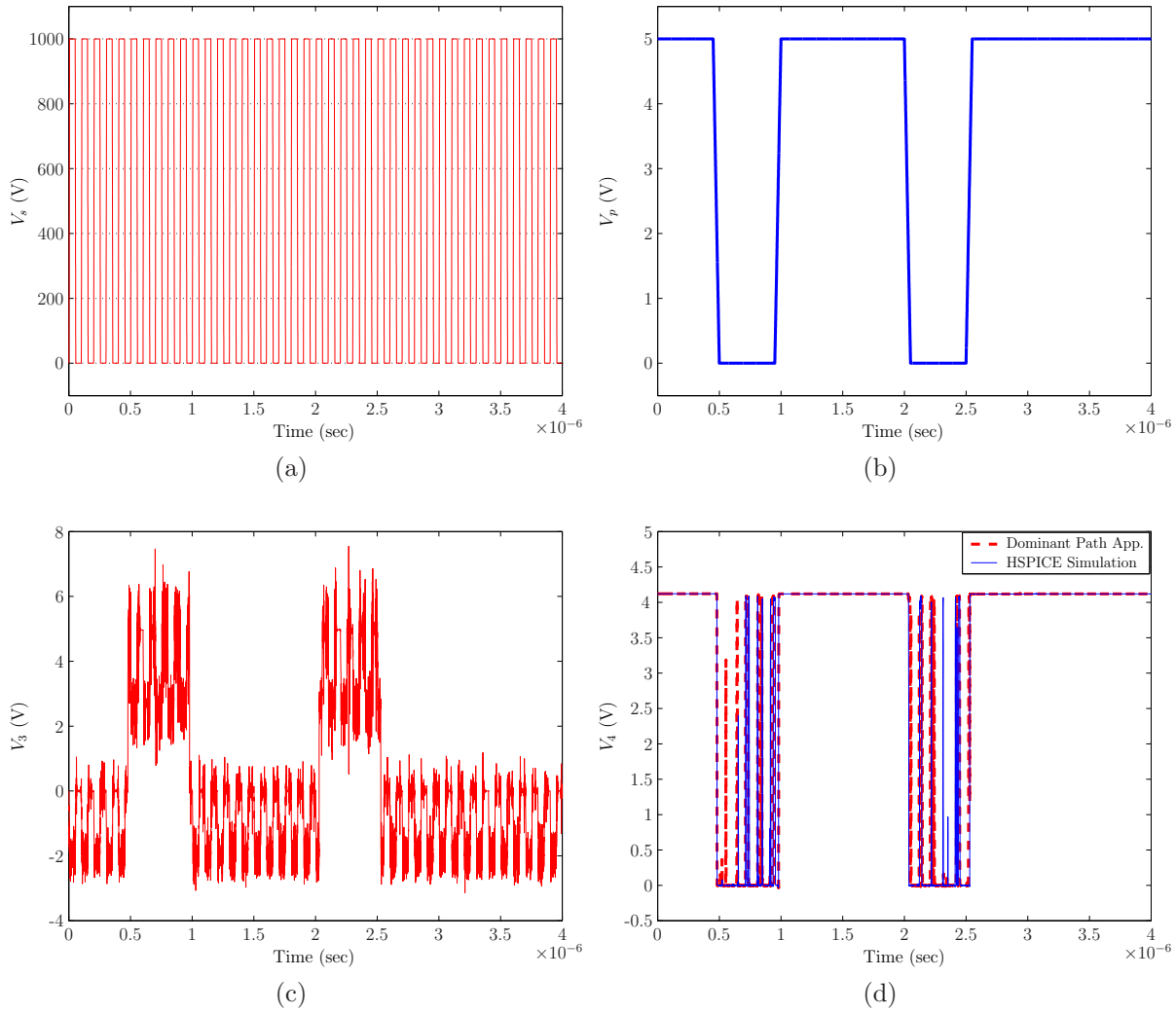


Figure 6.2.13: Signal at the ports of the network in Figure 6.2.12: (a) noise impulses, (b) nominal bit sequence, (c) signal at driver output pin, (d) signal at receiver output pin [66]

6.3 Investigation of Influence Parameters

This section will apply the dominant path approach considering many aspects of a circuit. First a circuit with discontinuities is analyzed. Second multiple sources of noise impulses are considered. Third the approach is used to analyze critical subcircuits. In the last part the effects of the termination loads on the propagation of transient impulses is investigated.

6.3.1 Signal Paths with Interconnects of Arbitrary Geometries

The dominant signal path approach presented so far can be applied to any PCB with transmission structures of arbitrary geometries. In this subsection the circuit in Figure 6.3.1 which consists of blocks of interconnect transmission structures and linear passive components is analyzed [72]. The first and the second blocks, indicated by (TSTR 1), are three deformed coupled microstrip transmission lines. The third block, denoted by (TSTR 2), is

a single trace with a two bends. The fourth block, i.e. (TSTR 3), consists of two parallel coupled microstrip lines and the last block, i.e. (TSTR 4), is a three-parallel coupled traces.

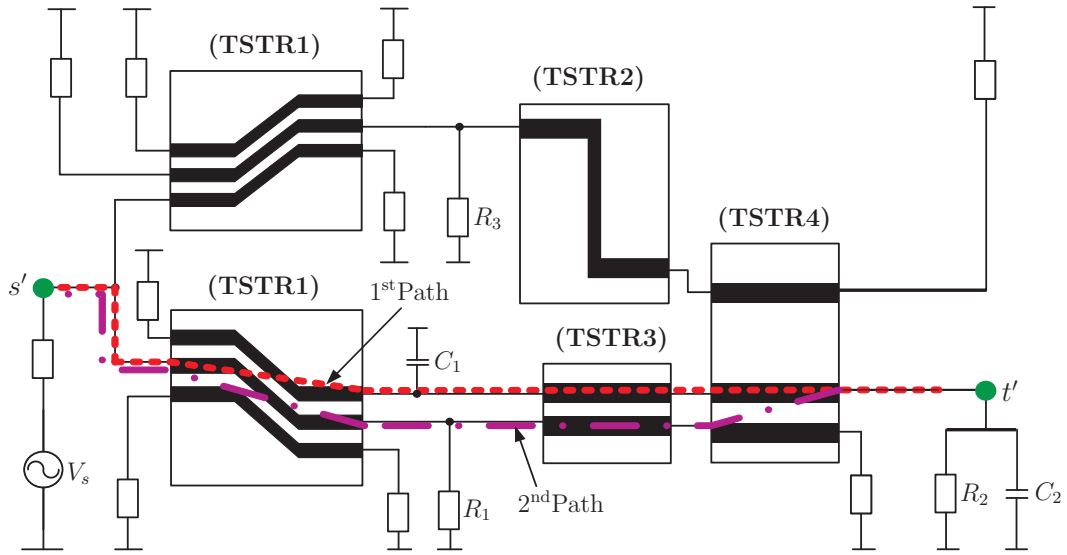


Figure 6.3.1: Interconnect circuit with arbitrary geometric structures [72]

A voltage source modeling a disturbance is applied to the circuit at the first and second strips of the first and second blocks (TSTR 1) respectively. Two resistances R_1 and R_3 of $100\,\Omega$ and a capacitance C_1 of $5\,\mathrm{pF}$ are connected between some traces belonging to different blocks. The target load consisting of a shunt R_2C_2 (R_2= $75\,\Omega$, C_2=$5\,\mathrm{pF}$) is located at the fifth port of the structure (TSTR 4).

All the microstrip structures are mounted on a FR4 substrate of thickness $365\,\mu m$ and with a relative permittivity 4.5. The ground plane and the microstrips of thickness $35\,\mu m$ are assumed to be perfect conductors. The geometrical dimensions of the individual structures are represented in Figure 6.3.2. Their characterization is performed in terms of the scattering parameters using the high frequency structure simulator HFSS.

The most dominant signal path from the noise source V_s to the target load R_2C_2 is extracted and evaluated. This path is indicated in the circuit schematic (dashed line). The extraction is performed at the frequency of $2\,\mathrm{GHz}$. The CPU time required for its extraction on a Pentium IV $2\,\mathrm{GHz}$ platform is about $10\,\mathrm{ms}$.

The dominant signal propagation path results from the crosstalk between the ports of the transmission structure (TSTR 4). This propagation way is trivial since the bends of the structure (TSTR 2) and the big space of the structure (TSTR 4) reflect and damp a large portion of the noise flowing over these structures. Propagation paths may generally also include reflection subpaths.

In Figure 6.3.3 the most dominant signal path $\mathcal{P}_1$, evaluated in terms of the magnitude of the voltage transfer function $V_{t'}/V_{s'}$, is represented. A good agreement is obtained comparing with the total transfer function provided by HSPICE frequency domain simulation. It is obvious that this propagation path does not change for frequencies up to

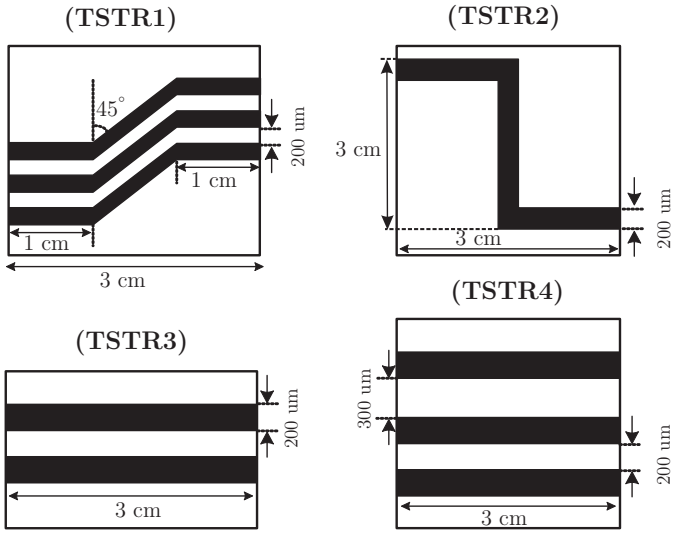


Figure 6.3.2: Physical characteristics of the microstrip structures of the PCB in the schematic 6.3.1 according to [72]

5 GHz, even for resonant ones. This represents only a special case since a dominant path may vary with the frequency, and therefore changes its order.

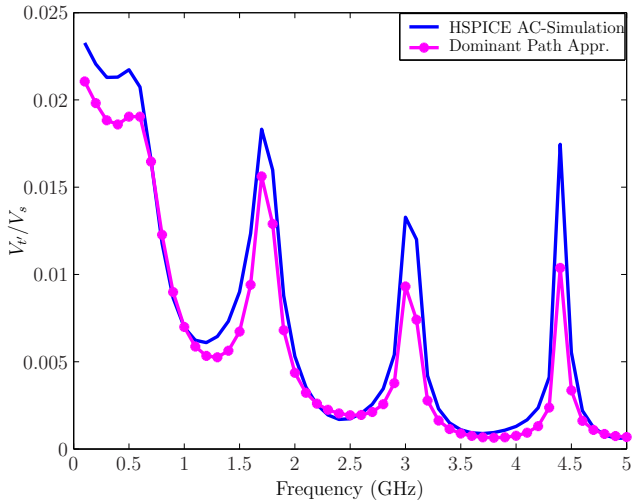


Figure 6.3.3: Voltage transfer function associated to the most dominant coupling path connecting the source $V_{s'}$ and the load RC

Clearly the transfer function associated to the most dominant signal path is very close to the total transfer function relating the noise source and the target load R_2C_2, and which corresponds to all existing propagation paths. Eventhough it is very important that the most dominant path will be extracted at many frequency points and then interpolated over the interval of the analysis. In that way the resonant frequencies leading to higher parasitic coupling, and which are responsible for the failure of sensitive digital devices may be captured.

In order to reduce the coupling impulses, protection procedures have to be made at some

circuit nodes belonging to the most dominant or critical path. The great advantage of such procedure leads in attenuating the noise at several target device pins by accessing only a single or a small number of nodes at the PCB-level.

The time domain analysis of the circuit in Figure 6.3.1 is performed using a single transient impulse generated according to the ESD model presented in [21]. The electrical network of this model is depicted in Figure 6.3.4.

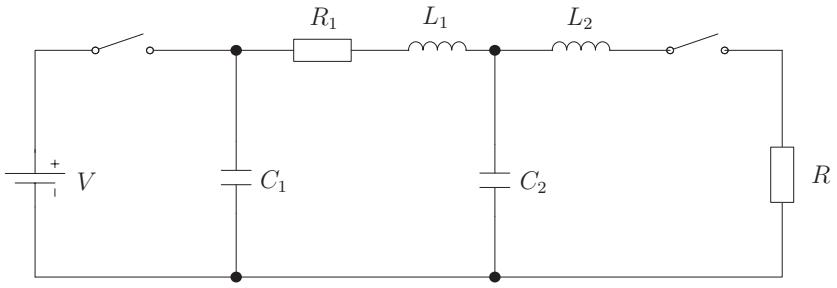


Figure 6.3.4: Example of a ESD generator network: R_1=330 Ω, C_1=150 pF, L_1=90 nH, C_2=2.5 pF, and L_2=60 pF

For this analysis a discharge voltage of 6 kV is considered. The characteristics of the ESD voltage waveform generated by this model, loaded by a resistance R =50 Ω, is represented in Figure 6.3.5(a). The corresponding frequency spectrum is presented in Figure 6.3.5(b). It is clear that the energy spectrum of this pulse is contained in the frequency range of 1 GHz, since no significant components exist above this frequency.

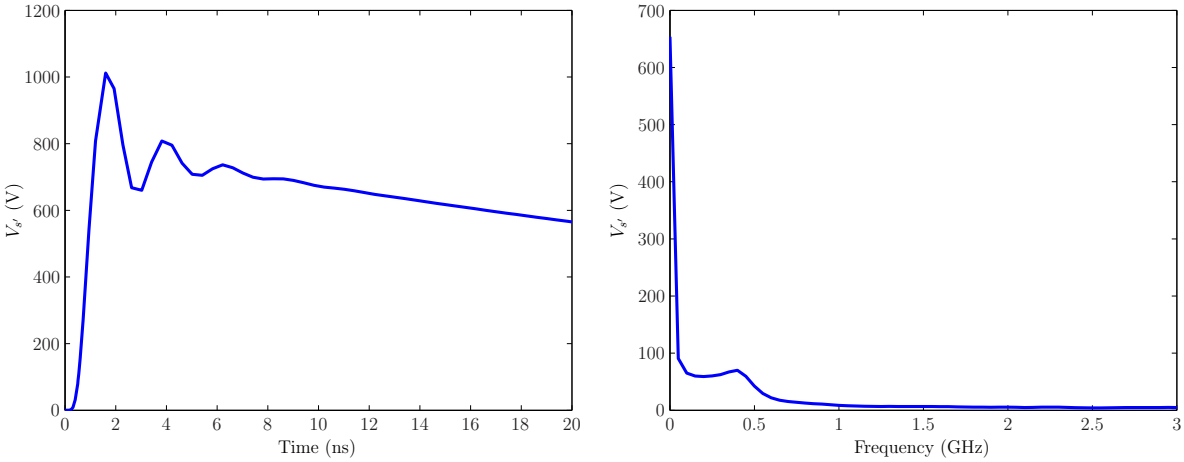


Figure 6.3.5: Example of an ESD impulse: (a) waveform, (b) spectrum

The time domain response to the ESD pulse, up to 200 ns, is given in Figure 6.3.6. The coupling impulses are computed using a combination of the ESD generator model and the scattering parameters determined considering the most dominant transmission path. Comparing with the total response obtained by the conventional time domain analysis, significant amplitudes of the path extracted are observed.

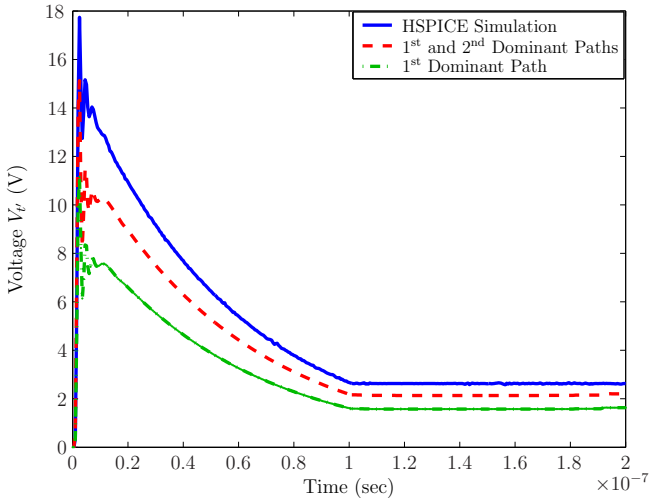


Figure 6.3.6: Time domain response to the ESD waveform in Figure 6.3.5

6.3.2 Propagation of Noise Impulses from Multiple Sources

In this subsection the dominant path approach is applied to more than one noise source. Dominant, or critical, signal traces transferring significant noise form multiple noise sources to digital device input ports are determined separately. Accordingly, a scattering matrix describing the linear interconnect system, which is terminated with the noise sources and IC I/O ports, is synthesized.

The dominant path approach has been applied to the PCB shown in Figure 6.3.7. It consists of eleven parallel coupled microstrip transmission lines, passive linear terminations, inverter gates and voltage sources. Microstrip lines which are not connected to each other are terminated by $50\,\Omega$ loads. The voltage sources V_1 and V_2 are assumed to be noise sources, whereas V_3 represents the nominal signal source. The transmission lines have the same physical properties like that of the schematic in Figure 6.2.10.

The linear part of the circuit containing the transmission lines and their passive linear terminations is analyzed using the dominant path approach in thefrequency range of 5 GHz. The scattering matrix relating the external ports, corresponding to the voltage noise sources and the chip pins, is determined by evaluating the dominant signal paths relating these ports. For each coefficient the number of signal paths required to give a good approximation to its exact value are extracted. The extraction of the paths is performed at the frequency of 2.5 GHz. This is here enough to speed up the algorithms instead of processing all the frequency points in the range of the analysis, since if the order of the first set of the paths remains unchanged. The extraction in DC or low frequencies must be avoided.

The dominant transmission paths relating the voltage noise sources V_1 and V_2 and the target inverter at the node t' are indicated in the schematic of Figure 6.3.7. For both noise sources a good approximation is already reached considering only the most dominant propagation path. In Figure 6.3.8(a) the magnitude of the transmission coefficient s_{14} is represented. The curve representing the value obtained by the dominant path approach overlaps with the exact analytical curve computed using the multiport connection

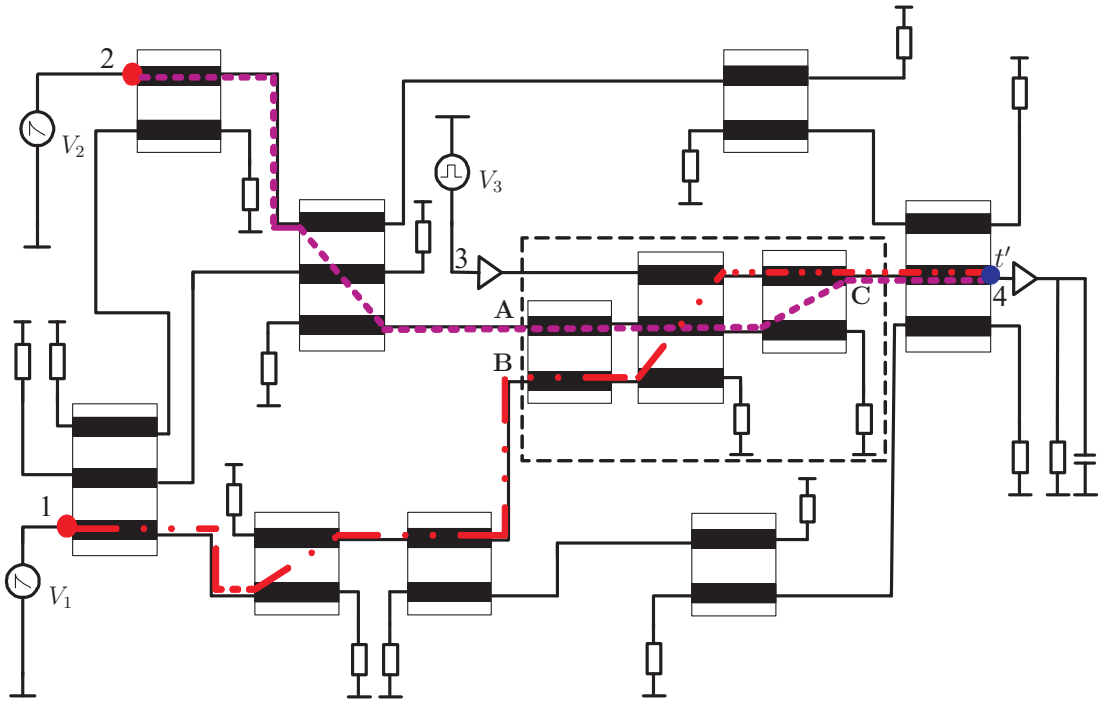


Figure 6.3.7: Interconnect system with two noise sources [73]

method. The remaining propagation paths for the determination of the coefficient s_{14} may be neglected. Similarly, the transmission coefficient s_{24} associated to the voltage source V_2 is computed. Its magnitude over the frequency range of 5 GHz is represented in Figure 6.3.8(b). Also here, the results are very close to the exact value of s_{24}. The phase of the transmission coefficients s_{14} and s_{24} are also computed. Their results are represented in the Figures 6.3.8(c) and 6.3.8(d), respectively. Except a small shift below the frequency of 1 GHz for s_{14}, a good agreement between the dominant path approach and the multiport connection method is obtained.

The remaining transmission and reflection coefficients describing the interactions between the ports connected to voltage sources and inverters are also computed. The magnitudes of transmission coefficients s_{12}, s_{13}, s_{23}, and s_{34} are depicted in Figure 6.3.9. For the computation of the coefficients s_{13} and s_{34} in the Figures 6.3.9(b) and 6.3.9(d), the first dominant path is required, whereas three dominant signal paths are extracted for the coefficients s_{12}, s_{23} in the Figures 6.3.9(a) and 6.3.9(c). The results show a good convergence with comparison to the validation method.

The magnitudes of the reflection coefficients s_{11}, s_{22}, s_{33}, and s_{44} are depicted in Figure 6.3.10. For the coefficients s_{11} and s_{33} two dominant signal paths are required to get the approximations shown in the Figures 6.3.10(a) and 6.3.10(c). However, the reflection coefficients s_{22}, and s_{44} represented in the Figures 6.3.10(b) and 6.3.10(d) are computed using a superposition of three dominant signal paths.

The scattering matrix computed in that way can be used to perform the frequency and time domain simulations. Of course, the superposition of the phases of the paths is also considered. Again, and due to the reciprocity of the paths, the transmission parameters s_{21}, s_{31}, s_{32}, s_{41}, s_{42}, and s_{43} do not have to be extracted and evaluated. Their propagation

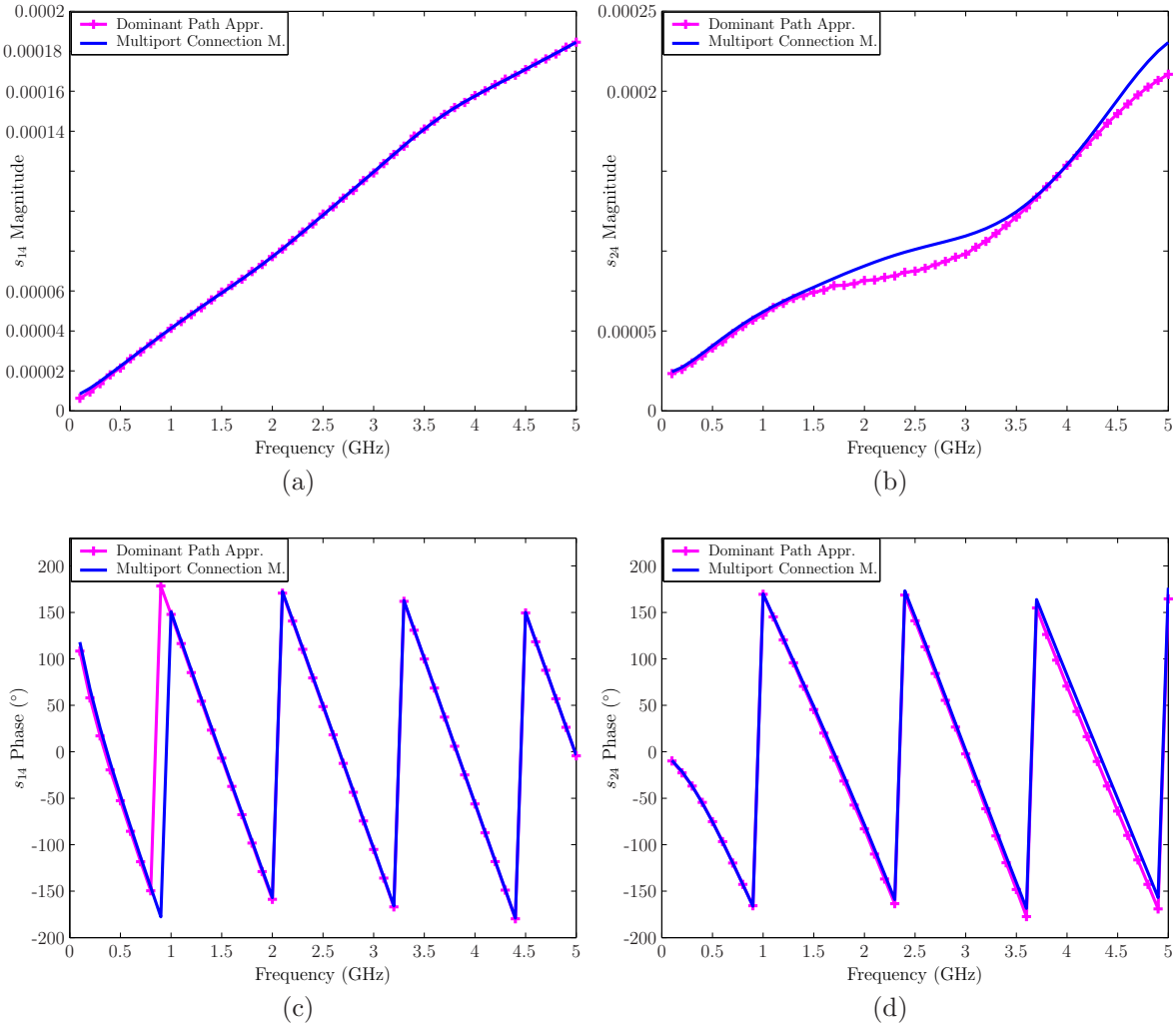


Figure 6.3.8: Transmission coefficients s_{14} and s_{24} of dominant paths: (a-b) magnitudes, (c-d) phases [73]

paths are similar to those of their symmetrical coefficients. In other words the transmitted power between two nodes takes the same way or path. The linear circuit part analyzed so far can be regarded as four-port network characterized in terms of the scattering matrix expressed by

$$\boldsymbol{S} = \begin{pmatrix} \sum_{r=1}^{2} s_{11}\left(\mathcal{P}_r\right) & \sum_{r=1}^{3} s_{12}\left(\mathcal{P}_r\right) & s_{13}(\mathcal{P}_1) & s_{14}(\mathcal{P}_1) \\ \sum_{r=1}^{3} s_{12}\left(\mathcal{P}_r\right) & \sum_{r=1}^{3} s_{22}\left(\mathcal{P}_r\right) & \sum_{r=1}^{3} s_{23}\left(\mathcal{P}_r\right) & s_{24}(\sum_{r=1}^{2} \mathcal{P}_r) \\ s_{13}(\mathcal{P}_1) & \sum_{r=1}^{3} s_{23}\left(\mathcal{P}_r\right) & \sum_{r=1}^{3} s_{33}\left(\mathcal{P}_r\right) & s_{34}(\mathcal{P}_1) \\ s_{14}(\mathcal{P}_1) & s_{24}(\sum_{r=1}^{2} \mathcal{P}_r) & s_{34}(\mathcal{P}_1) & \sum_{r=1}^{3} s_{44}\left(\mathcal{P}_r\right) \end{pmatrix}.$$

The structure of the resulting circuit is shown in Figure 6.3.11. This circuit is analyzed in time domain considering the voltage sources and two 1.8 V CMOS single inverter gates of the type SN74AUC1GU04 of Texas Instruments [57]. Two types of excitation voltages that are applied at the ports 1 and 2 of the network are studied. The first is a repetitive fast trapezoidal wave modeling an EFT burst, and characterized by the rise and fall times of 5 ns, a duration of 45 ns, a period of 100 ns, and a variable amplitude. The second is a ESD impulse generated by a standard RC model ($R = 330\,\Omega$, $C = 150\,\text{pF}$) under a discharge of 1 kV. At port 3 an input voltage source representing a data signal is applied. The inverter connected to port 3 represents an integrated circuit output port, i.e. driver. The one connected to port 4, represents the input port of another digital IC, i.e. receiver. Its input pin is connected to the target node, i.e. port 4, and its output port is terminated by a shunt RC (R=1 kΩ, C=30 pF).

The determination of the time domain response is performed using an S-parameter simulation. The scattering parameter model of the four-port network is used in a HSPICE circuit netlist which includes the voltage sources and the SPICE models of the CMOS

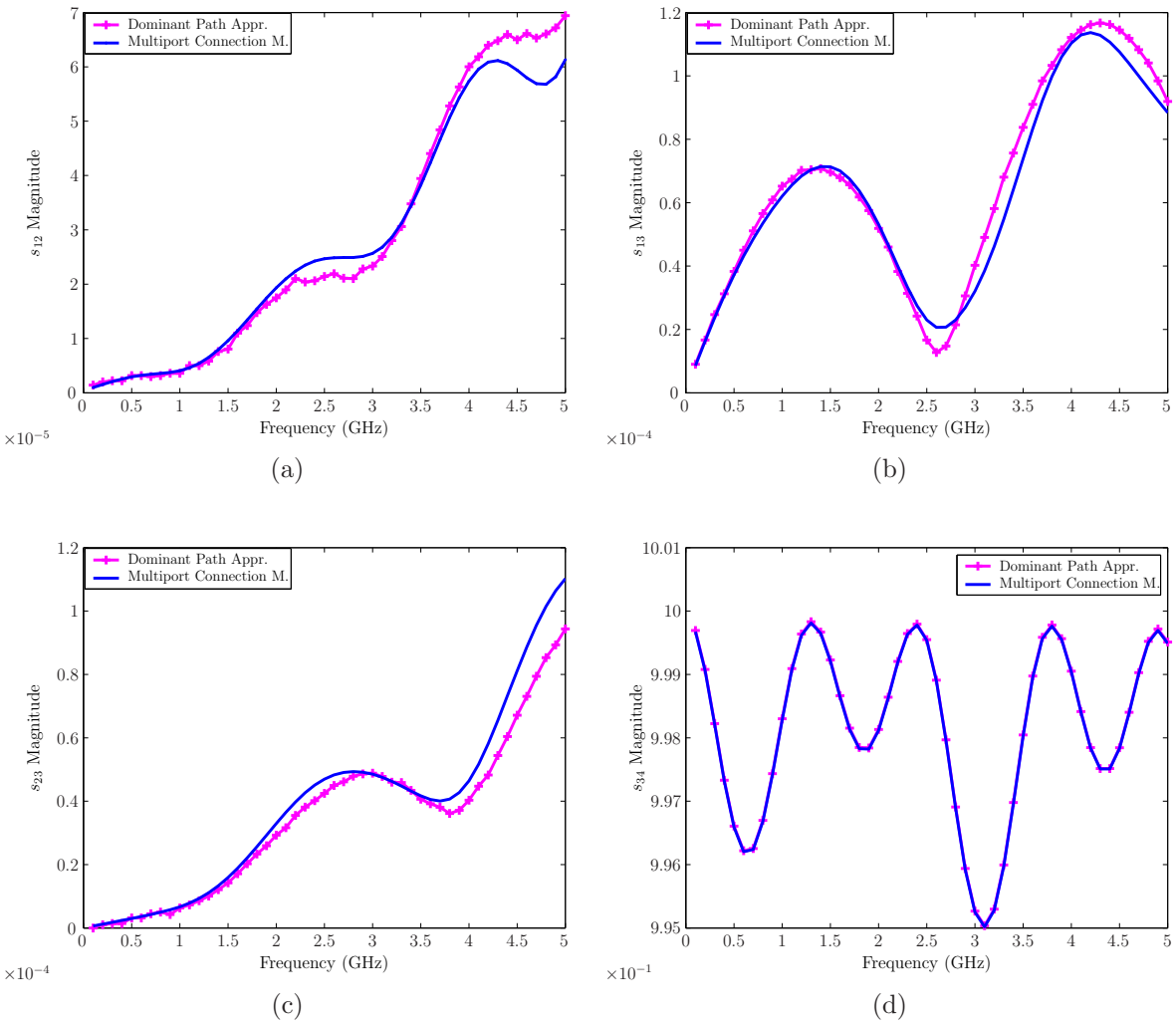


Figure 6.3.9: Magnitude of the remaining transmission coefficients: $s_{12}, s_{13}, s_{23}, s_{34}$

inverters including the package parasitics.

To analyze the failure of the CMOS receiver located at the port 4 due to glitches induced by the coupling propagation paths, time domain simulation is performed. The results are depicted in Figure 6.3.12. The noise impulses from both disturbances are superposed to the data signal at the input pin of the receiver. Figure 6.3.12(a) shows the voltage impulses obtained at the pin *RC* for the trapezoidal excitation. The shape of the impulses is obtained by the amplitudes of 10 V, and 30 V for V_1 and V_2 respectively. In Figure 6.3.12(b) the voltage waveform obtained at the pin *RC* for ESD excitations is represented [74]. Here, the ESD impulses from V_1 and V_2 are applied to the circuit at the time instants 0.3 μs and 0.9 μs respectively. For both impulse types perturbations of the logic states of the functional signal at the receiver output pin are observed.

For the periodic excitation the coupling impulses cause permanent signal failures, whereas single impulses affect the functional signal only for the duration of the impulses. In general the coupling disturbance from many noise sources depends also on the polarization of the individual pulses and the delay between them. The time domain response obtained by

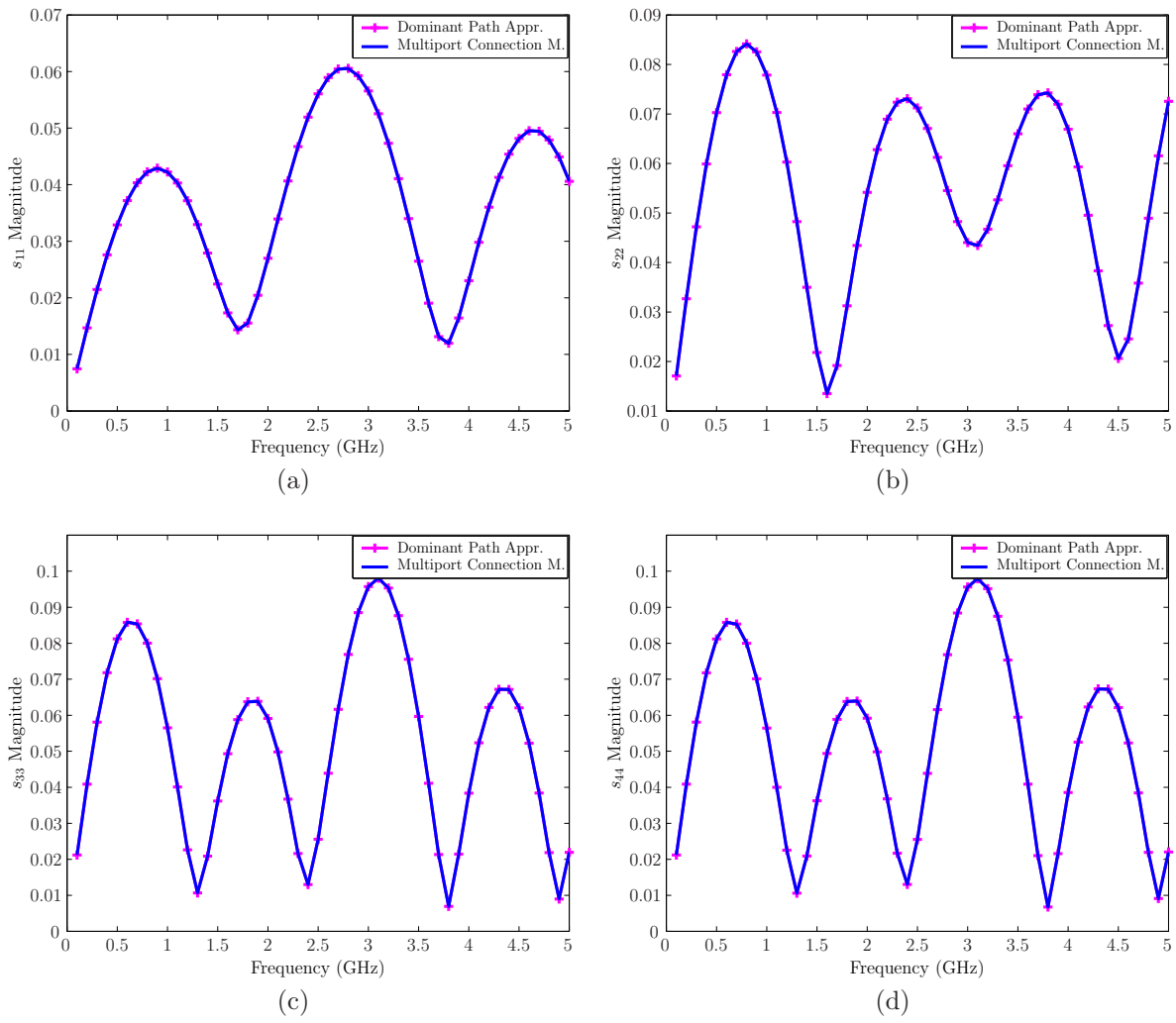


Figure 6.3.10: Magnitude response of the reflection coefficients

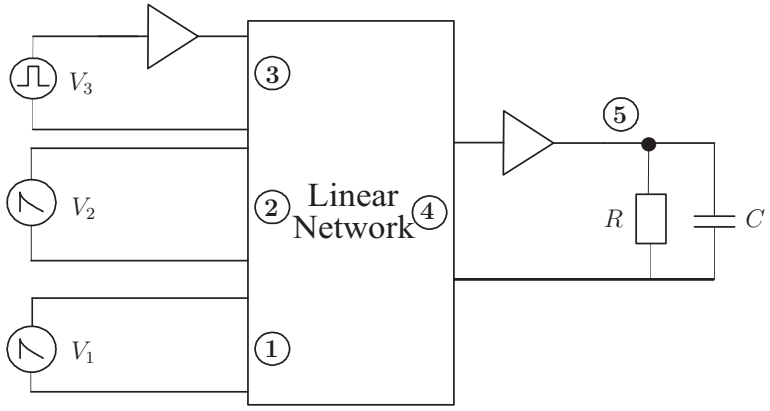
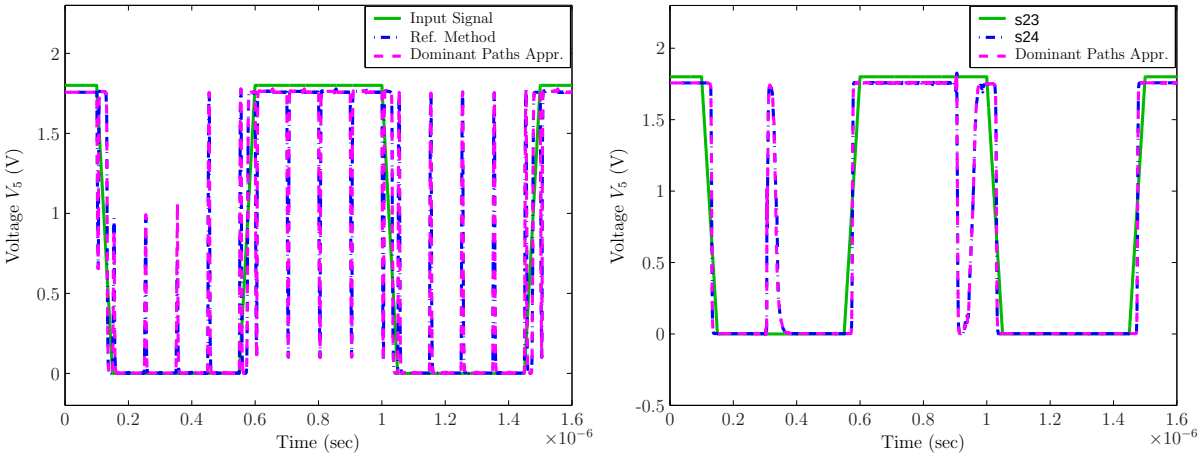


Figure 6.3.11: Simplified multiport structure for transient simulation



(a) (b)

Figure 6.3.12: Coupling noise impulses at the shunt RC for a: (a) trapezoidal excitation, and (b) ESD impulse [73]

the S-parameter simulation is compared to the conventional transient circuit simulation. For both types of excitations the system responses considering dominant paths show good agreement with the total system response.

The simulation time of the whole signal path is dominated by the transient analysis due to the nonlinear behaviour of the inverters. Nevertheless the S-parameter simulation proposed is more efficient than the conventional SPICE transient analysis.

6.3.3 Signal Propagation within Subcircuits

In order to study the influence of preprocessing some subcircuits on the dominant signal paths the transmission structures in the dashed frame of Figure 6.3.7 are grouped as a single subcircuit which is characterized separately. Figure 6.3.13 shows the structure of the resulting schematic after this modification.

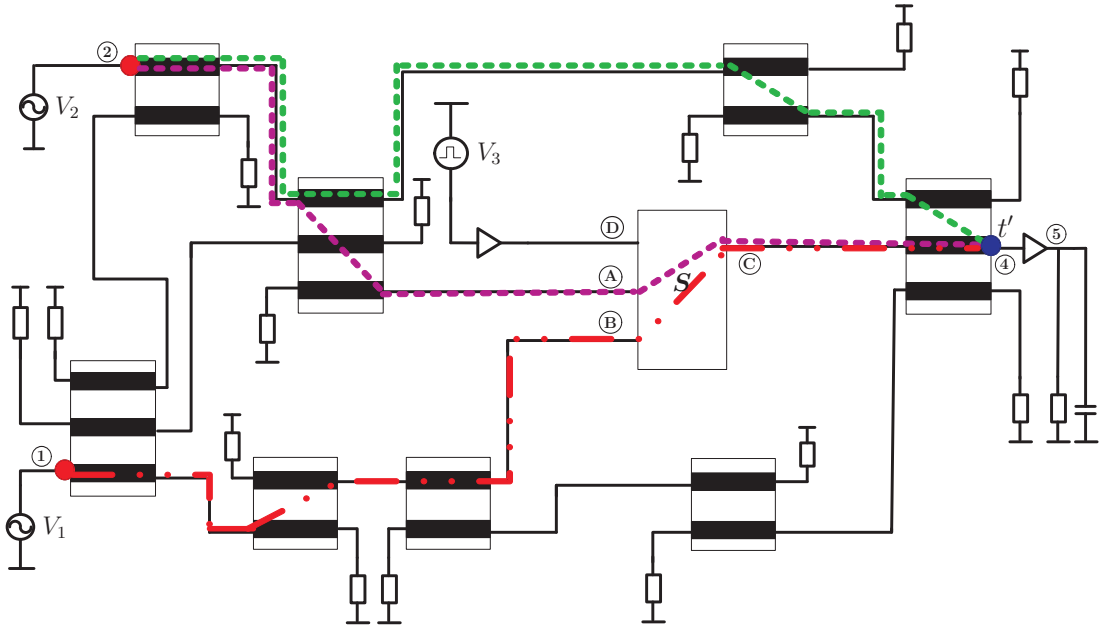


Figure 6.3.13: Signal paths belonging to different subcircuit parts

For this purpose the circuit netlist is modified and the dominant transmission paths relating the voltage sources V_1 and V_2, and the target component located at node t', are again determined and the associated coefficients are evaluated. The dominant transmission paths associated to the coefficients s_{14} and s_{24} are identical to the ones already computed without subcircuit reduction. As shown in Figure 6.3.13 the dominant transmission paths associated to the sources V_1 and V_2 travel over the pairs of external nodes (B, C) and (A, C) of the subcircuit, respectively.

The magnitude of the transmission coefficient s_{14} in the original case, where the global system is considered, is compared to the case where the subcircuit in the dashed area is represented by an equivalent multiport. The results of this comparison are in presented in Figure 6.3.14. Identical curves are computed for the coefficient s_{14}. The same will still valid for the remaining coefficients.

The advantage of preprocessing a set of interconnect structures as a subcircuit leads in the reduction of the circuit size. This procedure may be used when local information within a subcircuit are not important. This is the case when some structures could not be changed during the layout design. These can be considered and analyzed as a single subcircuit whose external ports only are connected to the rest of the system.

On the other hand the subcircuit in the dashed area is analyzed separately. The interactions between its external ports $\mathrm{A}, \mathrm{B}, \mathrm{C}$, and D are analyzed using the dominant path approach. Thus, allowing for the determination of weighted noise propagation paths in local structures and subcircuits. Figure 6.3.15 shows the analyzed subcircuit.

Considering this subcircuit the dominant signal paths between the ports A, B, and C are extracted. In the subcircuit schematic the most dominant signal paths relating the ports A, B to the port C are shown. As in the case of considering the global system, the subpaths extracted within the subcircuit travel the same circuit nodes. As a result the

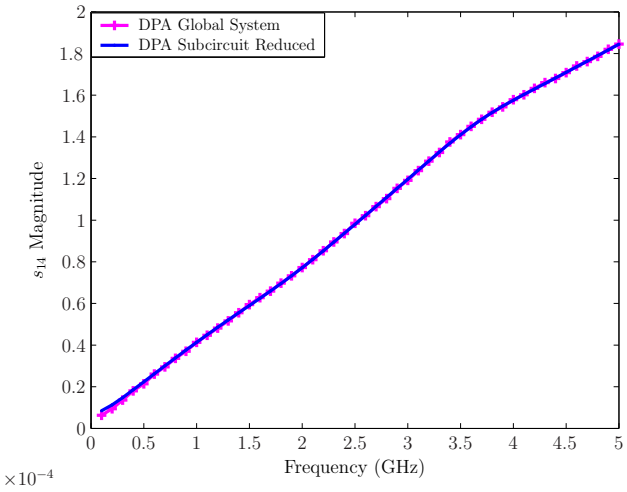


Figure 6.3.14: Magnitude of $s_{14}(\mathcal{P}_1)$ computed using the whole system, and the system after subcircuit reduction

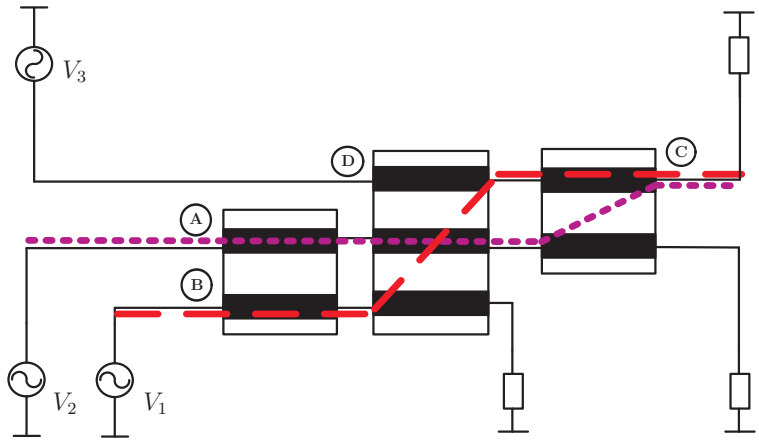


Figure 6.3.15: Subcircuit schematic analyzed

global dominant path contains the local subpath determined between the external ports of the subcircuit. The results of evaluating the transmission coefficients associated to the local dominant paths between the external ports of the subsircuit in Figure 6.3.15 are depicted in Figure 6.3.16.

It is in many situations very important to identify a dominant noise path which does not include some specific transmission substructures, especially when these substructures are already well designed. In other words the layout arrangement should be improved using any other substructures that have a secondary effect on the signal paths. To illustrate such procedure the circuit schematic in Figure 6.3.13 is considered. In order to extract a further signal path which does not share any nodes with the substructures in the dashed area, the approach to dominant signal path extraction is applied until a propagation path is determined which does not intersect the specified subcircuit.

This procedure is applied to the source V_2 in the schematic in Figure 6.3.13 for the identification of a dominant path which has no common nodes with the substructures in the dashed area. The extracted path is indicated in the same figure. It corresponds to

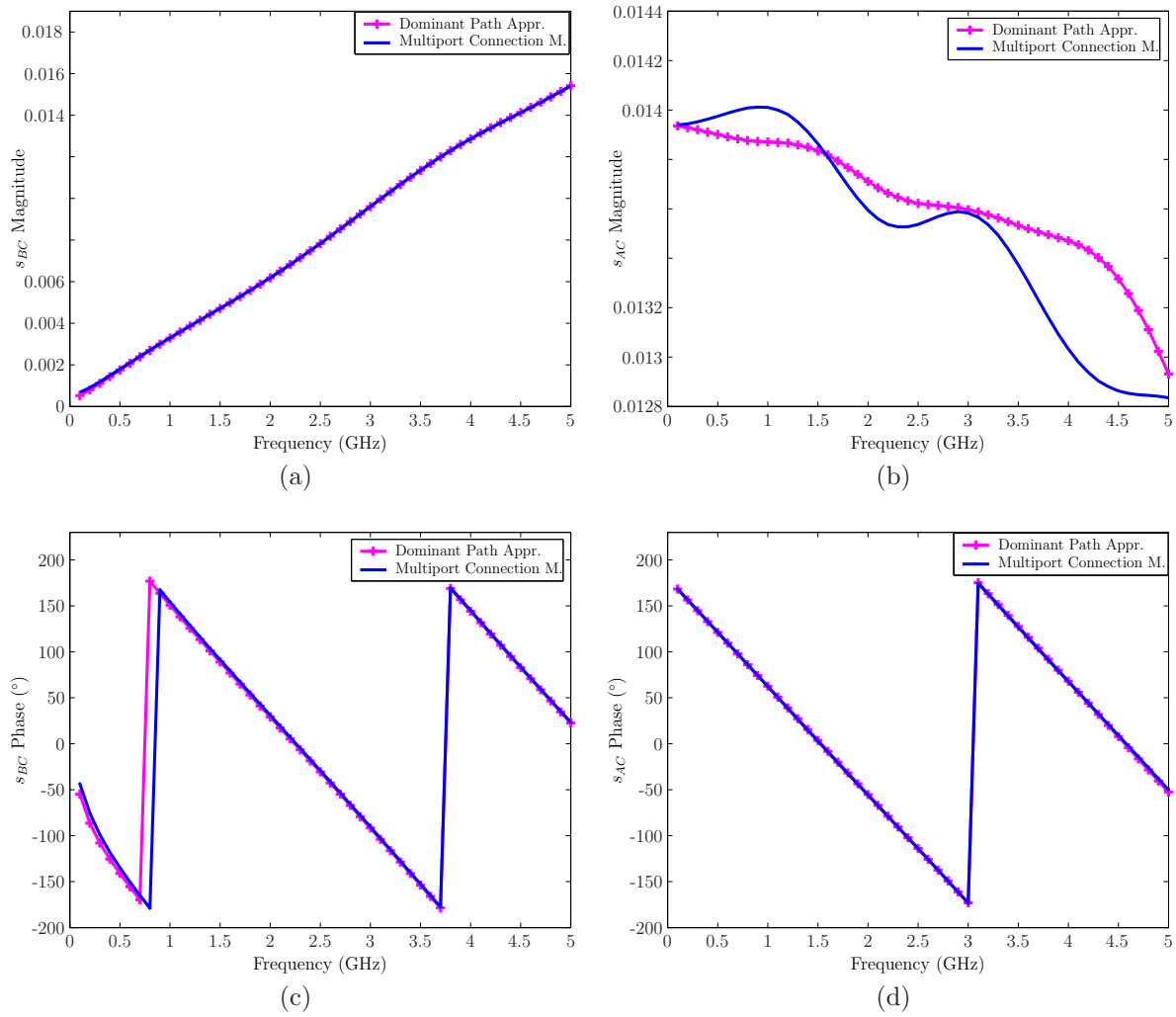


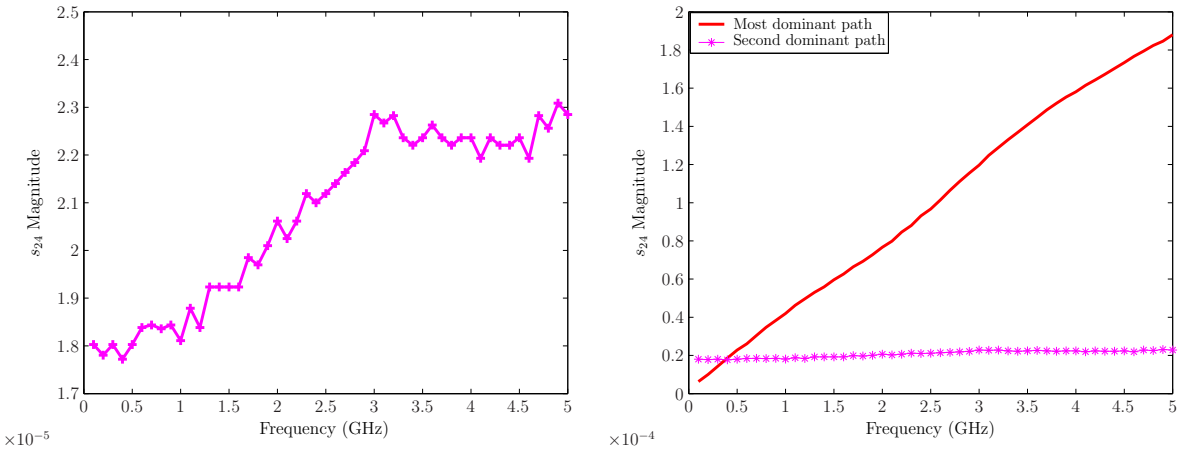
Figure 6.3.16: Evaluation of the transmission coefficients s_{BC} and s_{AC}: (a-b) magnitudes, (c-d) phases

the second dominant path if the whole system is considered. The evaluation of the new path extracted is shown in Figure 6.3.17. In Figure 6.3.17(a), the magnitude of $s_{24}(\mathcal{P}_2)$ is represented up to the frequency of 5 GHz. Its comparison to the first dominant path is shown in Figure 6.3.17(b). From this comparison, the second dominant path and its influence on the functional signal can be neglected above the frequency of 400 MHz.

6.3.4 Impact of Linear Interconnect Terminations

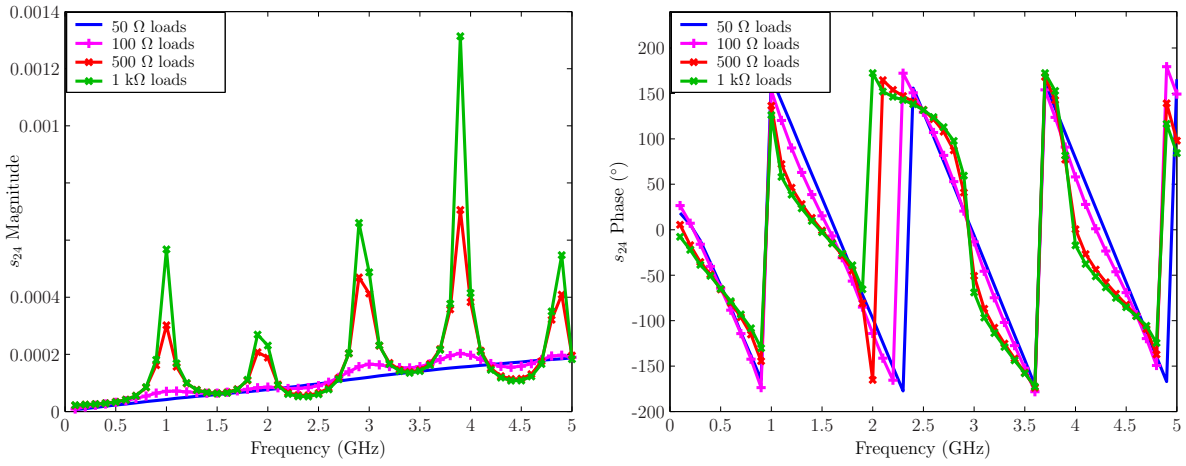
In order to investigate on the effects of the transmission structures terminations on the noise propagation paths the interaction between the ports 2 and 4 of the circuit in Figure 6.3.7 is studied [74]. For this purpose, the first dominant propagation path $s_{24}(\mathcal{P}_1)$ is determined for different ohmic loads: 50 Ω, 100 Ω, 500 Ω, and 1 kΩ. The results in terms of the magnitude and phase are presented in Figure 6.3.18.

In Figure 6.3.18(a) the magnitude of $s_{24}(\mathcal{P}_1)$ is shown. With increasing values of the



(a) (b)

Figure 6.3.17: Transmission coefficient s_{24} for: (a) $s_{24}(\mathcal{P}_1)$, and (b) $s_{24}(\mathcal{P}_1)$ and $s_{24}(\mathcal{P}_2)$



(a) (b)

Figure 6.3.18: Transmission coefficient s_{24} for various resistive terminations [74]

termination resistances resonances appear periodically. Moreover, the crosstalk noise at the resonance frequencies is increasing with the values of the terminations. The reason is that the reflected noise power from the termination loads of the transmission lines, which increases with the value of the termination resistance, is transmitted through the individual signal paths to the target load. The phase of the same path, i.e. $s_{24}(\mathcal{P}_1)$, is shown in Figure 6.3.18(b). The curves of the phases show almost similar results, except for the frequencies between 2 and 2.4 GHz. This result is not always the case, especially when the termination loads consist of capacitors or inductors.

Generally the order of a propagation path may change when applying different load conditions to the terminations of the interconnect structures. For instance the second dominant path $s_{24}(\mathcal{P}_2)$ for a 50 Ω and 1 kΩ loads are different. Figure 6.3.19 shows the magnitudes of the transmission coefficient of the second path $s_{24}(\mathcal{P}_2)$ for 50 Ω and 1 kΩ loads. The curve corresponding to 1 kΩ resistances is absolutely above the one corresponding to 50 Ω terminations over the frequency range of the analysis.

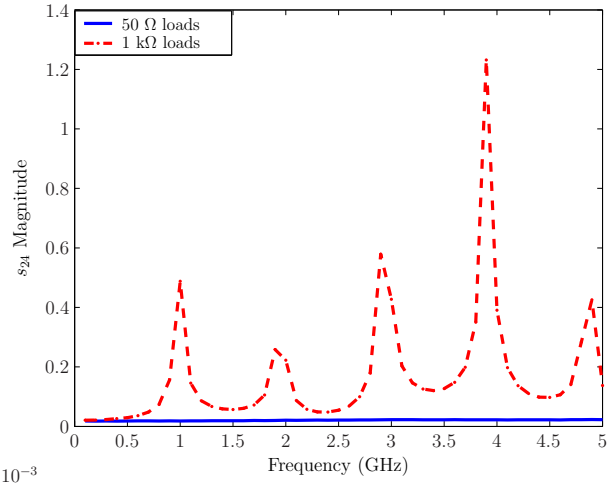


Figure 6.3.19: Magnitude of the transmission coefficient $s_{24}(\mathcal{P}_2)$ for different terminations

The effect of linear termination loads on the characterization of the propagation paths can be added to the parasitic behaviour of the layout to get a complete view on the noise propagation in the circuit. For this purpose appropriate linear models of digital devices ports can be used to model the pins terminating the transmission structures.

6.4 Implementation

This section describes the implementation process in this thesis. The algorithm efficiency and convergence are discussed. The modules of the algorithm and program input netlist and output parameters are described.

6.4.1 Efficiency and Convergence Issues

The simulation of circuits can be regarded as solving related systems of linear algebraic equations. The classical method used to solve a system of linear equations is the Gaussian elimination. This method is not efficient for large circuits. Alternatively, the system matrix can be decomposed into a lower triangular matrix $\mathbf{L}$ and an upper triangular matrix $\mathbf{U}$. For dense matrices, such decomposition requires a total number of arithmetic operations of

$$N_t = \frac{n^3}{3} + n^2 - \frac{n}{3}.$$

where n is the dimension of the circuit matrix. For sparse matrices, this number grows approximately linearly with the size of the matrix. The $\mathbf{LU}$ decomposition can be applied to compute the determinants of the matrices, given by (5.2.3), and thus called once for each dominant path. The structure and the size of the circuit matrix and SFG depend on the topology and the partitioning of the PCB. More partitions lead to sparse matrices and graphs, whereas less partitions give dense matrices and graphs.

The identification of the dominant signal paths relating two nodes in a graph leads to efficient analysis according to equation (5.2.3). Now the summation over all paths is reduced to a limited number of weighted ones. For a circuit with a number n of nodes and n_T termination loads, the circuit scattering matrix used for the evaluation of the signal paths has $n^{'} = 2\,(n - n_T)$ entries. The SFG generated from this matrix has also the same number of nodes $n^{'}$, and a number m of edges

$$m = \sum_{i=1}^{i=n_B} n_i^2,$$

where n_i is the number of internal ports in the block representing the i-th multiport in the circuit, and n_B is the total number of these blocks.

The problem of solving k-shortest paths algorithm using the algorithm proposed in Section 5.1.2 leads to $o(k\,(m + n' \log n'))$ operations in the optimistic case. This is the additional time to the conventional frequency domain solution of the circuit matrix. For dense circuit matrices, this time overhead can be neglected when compared to the polynomial time required by the classical methods that are based on the determinant, or inverse matrix computations. In the case of sparse matrices the total simulation time, including the time to determine the dominant paths, still vary roughly linearly with the size of the matrix. The dimension of the problem is then the number of the paths multiplied by the number of all simulation frequency points.

The transient analysis of the individual propagation paths characterized by their transmission coefficients may be carried out using the time domain convolution of the HSPICE simulator. The scattering parameters of each port are converted into voltages and currents. This requires the application of the IFFT to the frequqency domain scattering parameters to compute the impulse responses. The accurcy of this method depends on the number of data samples available. This method is very accurate results, but inefficient.

An important technique which is more efficient in comparison with the conventional time domain analysis is the HB technique. This technique is best suited for weakly nonlinear circuits with almost sinusoidal excitation. In strong nonlinear circuits containing waveforms with sharp transitions, the number of Fourier coefficients needed to describe the unknown waveform accurately is large. Accordingly, a rapid increase in memory and simulation time consumption are caused. Therefore, HB cannot be applied accurately and efficiently. Another disadvantage of this method is its limitation to periodic signals. In such cases the HSPICE S-parameter simulation can be performed.

6.4.2 Data Structures

The main algorithms for the identification of dominant signal paths are implemented in C++ language using Microsoft Visual Studio 6.0. The matrix routines have been implemented in a stand-alone applications using the package of MATLAB and then exported in form of dynamic link libraries to the signal tracing module.

The whole module to dominant path tracing uses also a *Complex* and a *Matrix* library containing the routines of complex numbers manipulation and memory allocation and

deallocation, respectively. For the generation of the SFG and the circuit matrix a *MultiPort* library, which manages the transmission structures data and the topology of the circuit, is implemented.

The algorithms to identify and evaluate the critical signal paths are coded within the module *KSShortestPaths*. The main application is implemented in the module *DominantPaths*. The modules constituting the whole program are represented in the diagram of Figure 6.4.1.

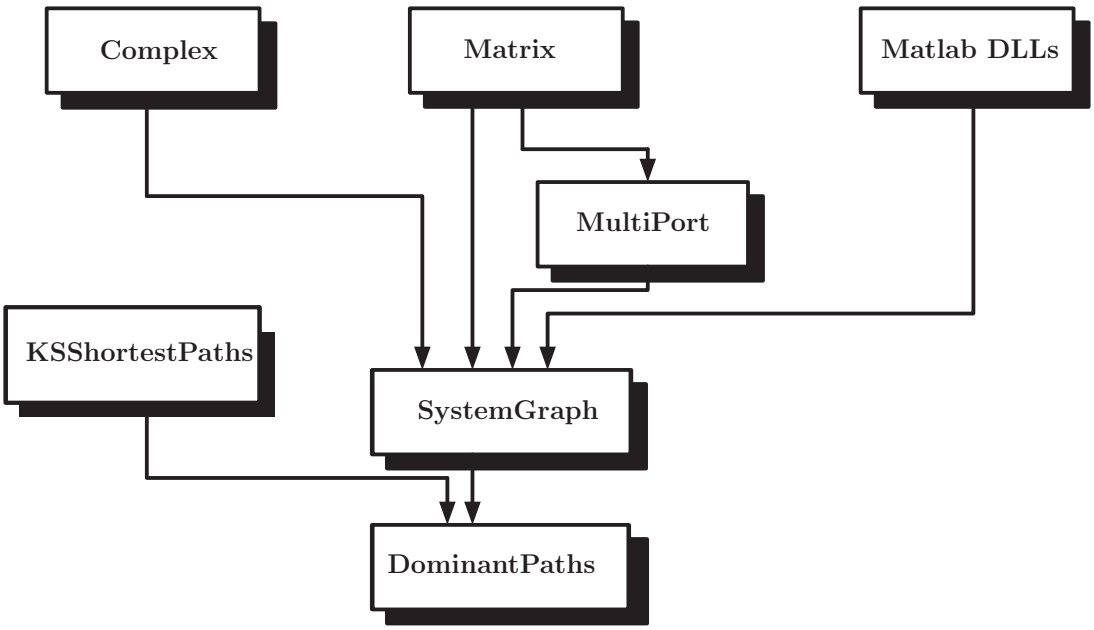


Figure 6.4.1: Modules of dominant path approach

For the implementation of the algorithms the C++ Standard Template Library (STL) is used [75, 76]. It provides a significant level of flexible functionality, generalized and efficient algorithms, and low run-time cost.

6.4.3 Input and output Parameters

The program uses input network files which are similar to the SPICE netlist. However there are some internal transformations which convert the circuit data into a multiport representation. The transmission structures can be expressed directly in terms of the scattering parameters, or in terms of the per unit length matrices $\boldsymbol{R}, \boldsymbol{L}, \boldsymbol{G}$, and $\boldsymbol{C}$. The interconnect scattering matrices are stored in touchstone files and the per unit length matrices are saved in ASCII files, respectively. An example showing the general format of a network file is given as

```
V 2 0 1
P 7
B1[6] 3 4 2 5 7 1 block_Area00.tch
B2[4] 7 8 19 9 rlgc_tchFile02.rlgc
R1 9 12 1.000000E+3
R2 5 0 1.000000E+3
```

```
C1 5 0 5.000000E-12
L1 9 12 5.000000E-9
...
```

In this netlist the start node is assumed to be located at the noise source V, and the target node is represented by the letter P. The symbol Bn[m] represents a transmission structure with the identifier n and a number of ports m. R, L, and C represent any lumped elements in the circuit.

The input parameters needed to run the program are:

- Name of the circuit file
- Start, stop, and step frequencies
- Extracting frequency

The output parameters of the programm are the circuit critical connections that belong to the dominant noise path nodes. At the circuit SFG-level these are given by the nodes in the SFG. Bellow an example of such output representation.

```
*************************************************************
Processing Path Number  0 ..........................
*************************************************************
    0 Path cost:9.24695 Number of nodes: 15 5-2-16-15-29-28-40-38-66-65-
    74-72-53-51-57
*************************************************************
Processing Path Number  1 ..........................
*************************************************************
    1 Path cost:13.1686 Number of nodes: 15 5-2-16-15-29-28-40-39-67-64-
    73-72-53-51-57
    ...
```

At the netlist level the paths are given by the multiports identifiers and the associating ports numbers. The following example shows the output connections for such representation.

```
MultiPortId: 1  PortId: 3
MultiPortId: 2  PortId: 1
MultiPortId: 3  PortId: 4
...
```

Chapter 7

Conclusion

This thesis presented a CAD-technique for the determination of noise distribution with respect to conducted transient impulses at the PCB level. The shown methodology merits the capability to extract the dominant or critical noise propagation paths that carry significant noise power from a specified peripheral connector pin to a sensitive device pin, while the entire system under consideration. The extraction of the dominant paths is performed for linear interconnects in the frequency domain and their contribution to the faults of the digital device pins is predicted. The noise propagation paths include capacitive, inductive, galvanic and multiple reflections paths.

This approach can be used to analyze PCB architectures including passive interconnection structures with different geometry configurations and lumped circuit elements. Instead of simulating the entire complex system consisting of complex interconnecting structures in an electromagnetic field simulator all at once, the whole system is partitioned into substructures. From these substructures only a fundamental set that may represent approximately all existing substructures in the system is characterized. Therefore a reduction of the complexity of the system is achieved by considering only a specific number of fundamental structures representing the existing physical paths in the circuit.

The extraction of the critical noise propagation paths is carried out using a combination of efficient graph searching algorithms and the scattering matrix representing the circuit equations. By means of the k-shortest paths algorithm, simple signal paths are identified in the signal flow graph that represents the electronic network. These paths are extracted in a rating order of their associated weights or transfer functions. Their evaluation is performed by employing the circuit scattering parameters matrix. The scattering parameters associated to the individual paths are computed by the means of the matrix form of *Mason*'s Formula.

The time domain analysis of the dominant signal paths terminated with passive linear models of the IC ports is carried out by the Inverse Fourier Transform algorithm for the frequency domain results. For a complete simulation of the dominant signal paths consisting of non-linear terminations, hybrid analysis methods are used. An example of such hybrid methods is the harmonic balance technique, which interfaces the frequency domain analysis of the linear part of a circuit with the conventional time domain analysis

of the non-linear part. This technique is more efficient than the conventional time domain analysis based on numerical integration techniques. Its disadvantages are the aliasing problem and its limitation to periodic signals. The errors introduced by aliasing can be avoided by over-sampling, but this is achieved at the cost of a higher run time.

The time domain simulation of the whole signal path consisting of the noise source, the interconnects and the chip's I/O ports, represented with their electrical or behavioural models, can be performed by combining the scattering parameter model of the signal paths and the buffer models of the chip. The resulting circuit netlist can be simulated using the HSPICE circuit simulator.

Examples of single and repetitive excitation impulses with fast signal transitions and high amplitudes are applied to some interconnecting systems with CMOS inverter gates. The propagating noise impulses considering dominant signal paths are computed at the input ports of these inverters. This methodology provides the ability to analyze and to detect the critical structure for a detailed analysis. Multiple sources of noise are simulated and their responses are superimposed.

It was shown that the consideration of a limited number of dominant paths with respect to a specified noise source and a target device pin may be enough to describe the interaction between the corresponding ports. Consequently, the results in terms of scattering parameters and coupling impulses show a close alignment with the validation methods corresponding to the global system response.

Since the methodology presented is a frequency domain technique, the signal propagation paths depend generally on the frequency. A dependency of the signal paths on interconnects characteristics and transient noise parameters is obvious. The signal waveform at digital device pins is dependent on the noise margin of the device. The consideration of such a dependency may be helpful for the designer to attenuate the noise transmitted by these paths.

Moreover, the method proposed takes into account that the critical paths provides not only an approximation to the total system response, but also allows the identification of a minimum set of weak subnets at an early stage before any physical implementation of circuits takes place. The information about signal paths carrying considerable amounts of the electromagnetic power may be helpful for the designer to develop reliable layouts. The parasitic behavior can be compensated by taking appropriate and efficient compensation procedures into account by accessing the critical positions on the PCB level.

Appendix A

Complex Fourier Series

An alternative way to determine the Fourier series is to use the complex form of its coefficients. In that way the Fourier coefficients can be easily computed than in the case of the trigonometric form. A periodic signal with a period T can be represented in the time domain by the complex Fourier series expansion defined as

$$f(t) = \sum_{-\infty}^{+\infty} c_n \exp(jn\omega_0 t), \tag{A.1}$$

where ω_0 is the fundamental angular frequency of the signal and which is given by

$$\omega_0 = \frac{2\pi}{T}.$$

The complex Fourier coefficient c_n are defined by

$$c_0 = \frac{1}{T}\int_{t=t_0}^{t_0+T} f(t)\,dt, \tag{A.2}$$

$$c_n = \frac{1}{T}\int_{t=t_0}^{t_0+T} f(t)\,\exp(-jn\omega_0 t)\,dt, \tag{A.3}$$

$$c_{-n} = \frac{1}{T}\int_{t=t_0}^{t_0+T} f(t)\,\exp(n\omega_0 t)\,dt, \tag{A.4}$$

where t_0 can be any value of time.

The complex form of the Fourier series contains positive and negative values of the harmonic frequencies. To obtain the one-sided spectrum (positive frequencies), the coefficients c_n for the double-sided spectrum are doubled, and the DC component c_0 remains unchanged. In contrast to the real-valued trigonometric coefficients a_n and b_n, the Fourier coefficients c_n may be complex-valued. The trigonometric Fourier coefficients a_n and b_n can be computed from c_n using the relations

$$a_n = 2\,Re\{c_n\}$$
$$b_n = -2\,Im\{c_n\}.$$

For each frequency point the amplitude spectrum is given by

$$A_n = \sqrt{a_n^2 + b_n^2}$$

The time domain analysis of the individual signal paths using the HB technique is carried out by considering a number of harmonics approximating the periodic transient signal. Both signal rise and fall times should be accurately approximated in order to represent the frequency spectrum. The highest sine wave frequency required, i.e bandwidth, depends on the rise time.

Figure A.1 shows an example of a periodic trapezoidal signal for which the Fourier coefficients and the frequency spectrum are evaluated. The switching time during each period is denoted by t_i. The rise and fall times are assumed to be identical and denoted by t_r.

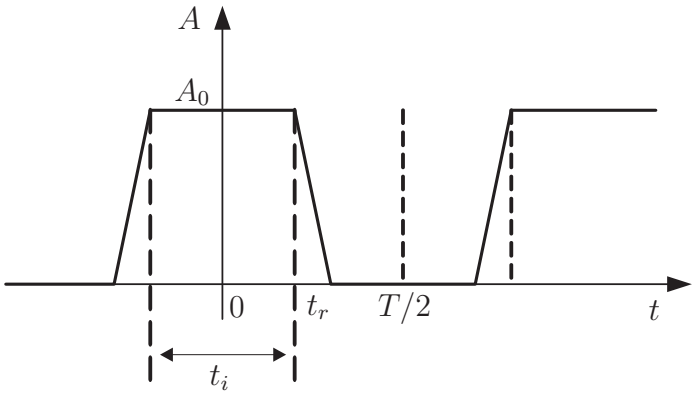


Figure A.1: Characteristics of a trapezoidal wave

The coefficient a_0 can be computed as

$$a_0 = \frac{2}{T}\left[\int_0^{t_i/2} A_0\, dt + \int_{t_i/2}^{t_i/2+t_s} A_0\,(\frac{-t}{t_s} + \frac{t_i}{2} + t_s)\, dt\right] \tag{A.5}$$

$$a_0 = \frac{A_0}{T}\,(t_i + t_s) \tag{A.6}$$

The coefficient a_n is computed as

$$\begin{aligned} a_n &= \frac{4}{T}\left[\int_0^{t_i/2} A_0\,\cos(n\omega_0 t)\, dt + \int_{t_i/2}^{t_i/2+t_s} A_0\,(\frac{-t+t_i/2}{t_s} + 1)\,\cos(n\omega_0 t)\, dt\right] \\ &= \frac{A_0\, T}{n^2\,\pi^2\, t_s}\left[-\cos(\frac{2\,n\,\pi}{T}(t_s + \frac{t_i}{2})) + \cos(\frac{n\,\pi\,t_i}{T})\right] \\ &= 2\frac{A_0\, T}{n^2\,\pi^2\, t_s}\left[\sin(\frac{n\,\pi}{T}(t_s + t_i))\,\sin(\frac{n\,\pi\,t_s}{T})\right] \end{aligned} \tag{A.7}$$

Using the symmetry of the function in Figure A.1, $b_n = 0$. Therefore, the total amplitude spectrum A_n is given by a_n.

$$A_n = 2\frac{A_0\, T}{n^2\,\pi^2\, t_s}\left[\sin(\frac{n\pi}{T}(t_s + t_i))\,\sin(\frac{n\,\pi\,t_s}{T})\right] \tag{A.8}$$

Figure A.2 shows the frequency spectrum of a trapezoidal signal with a period $T = 100\,\text{ns}$, a transition time $t_r = 5\,\text{ns}$, and a pulse width $t_i = 50\,\text{ns}$. The same figure shows also the frequency spectrum envelopes approximating this signal at three regions.

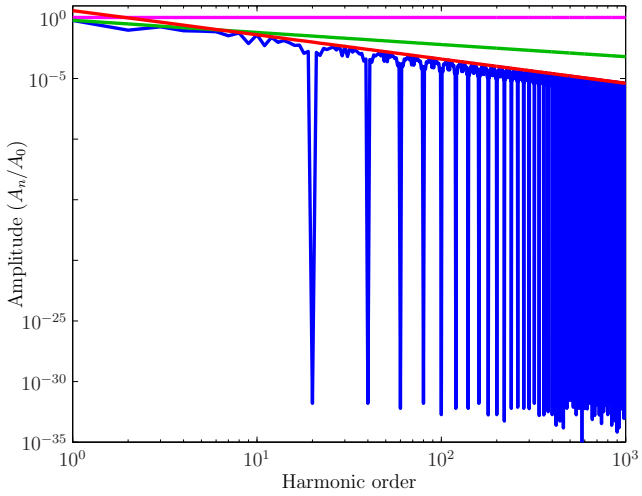


Figure A.2: Frequency spectrum envelope

The direct computation of the Fourier coefficients can become difficult for some waveforms. More complex periodic, but piecewise linear waveforms, can be decomposed into a linear combination of more simple functions. For each of these simple functions the Fourier coeffcients are easily computed. Using the properties of Fourier Transformation the resulting spectrum of the original waveform can be derived.

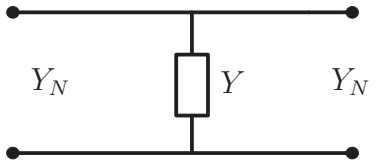
Appendix B

Some Fundamental Scattering Matrices

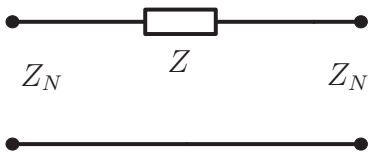
In order to generate the signal flow graphs of various components and junctions that occur in a microwave circuit the scattering matrices should be derived. The individual subgraphs can be be connected together to construct the entire network. Some basic microwave circuit elements commonly used in CAD programs and their scattering matrices are given bellow.

$$\boldsymbol{S}_{11} = \frac{Z - Z_N^*}{Z + Z_N}$$

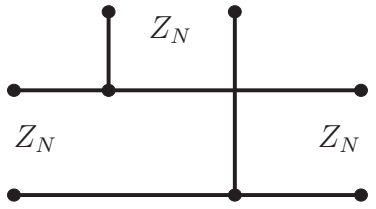
$$\boldsymbol{S} = \frac{1}{Y + 2Y_N} \begin{pmatrix} -Y & 2Y_N \\ 2Y_N & -Y \end{pmatrix}$$



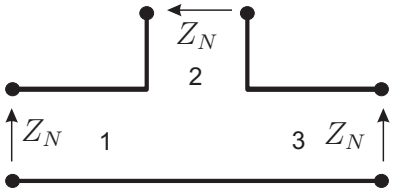
$$\boldsymbol{S} = \frac{1}{Z + 2Z_N} \begin{pmatrix} -Z & 2Z_N \\ 2Z_N & -Z \end{pmatrix}$$



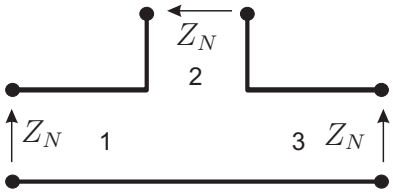
$$\boldsymbol{S} = \frac{1}{3} \begin{pmatrix} -1 & 2 & 2 \\ 2 & -1 & 2 \\ 2 & 2 & -1 \end{pmatrix}$$



$$\boldsymbol{S} = \frac{1}{3}\begin{pmatrix} 1 & 2 & 2 \\ 2 & 1 & -2 \\ 2 & -2 & 1 \end{pmatrix}$$



$$\boldsymbol{S} = \frac{1}{3}\begin{pmatrix} 1 & -2 & 2 \\ -2 & 1 & 2 \\ 2 & 2 & 1 \end{pmatrix}$$



References

[1] R. P. Clayton, *Introduction to Electromagnetic Compatibility*, 3rd ed. New York, USA: John Wiley and Sons Inc., 1992.

[2] M. Kamon, S. McCormick, and K. Shepard, "Interconnect parasitic extraction in the digital IC design methodology," in *Proc. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, San Jose, CA, USA, Nov. 1999, pp. 223–230.

[3] K. Banerjee, D. Y. Kim, A. Amerasekera, C. Hu, S. S. Wong, and K. E. Goodson, "Microanalysis of VLSI interconnect failure modes under short-pulse stress," in *Proc. 38th IEEE Annual International Reliability Physics Symposium (IRPS)*, San Jose, CA, USA, Apr. 2000, pp. 283–288.

[4] H. Qian, J. N. Kozhaya, S. R. Nassif, and S. S. Sapatnekar, "A chip-level electrostatic discharge simulation strategy," in *Proc. of the 2004 IEEE/ACM International Conference on Computer-aided Design*, San Jose, CA, Nov. 2004, pp. 315–318.

[5] B. Deutschmann, E. Sicard, and S. B. Dhia, "On the effects of transient electromagnetic interference on integrated circuits," *Electronic Device Failure Analysis*, vol. 8, no. 4, pp. 16–24, Nov. 2006.

[6] E. Lamoureux, "Étude de la susceptibilité des circuits intégrés numériques aux agressions hyper-fréquences," Ph.D. dissertation, L'Institut National des Sciences Appliquées de Toulouse (INSA), France, Jan. 2006.

[7] M. Evans and J. Dunnihoo, "Low-capacitance ESD protection on high-speed ports (USB 2.0 and DVI)," California Micro Devices, June 2003, Application Note 220.

[8] R. Carlton, G. Racino, and J. Suchyta, "Improving the transient immunity performance of microcontroller-based applications," Freescale Semiconductor, Inc., June 2005, Application Note 2746. [Online]. Available: http://www.freescale.com/files/microcontrollers/doc/app_note/AN2764.pdf

[9] F. Fiori and F. Musolino, "A new technique for the measurement of IC susceptibility to electrical fast transients," in *Proc. International Conference on Electromagnetic Compatibility, EMC Europe*, Eindhoven, The Netherlands, Sept. 2004, pp. 147–150.

[10] B. Deutschmann, G. Winkler, T. Ostermann, and K. Lamedschwandner, "Electromagnetic immunity: System-versus chip-level," in *Proc. International Symposium on Electromagnetic Compatibility, Eindhoven*, vol. 2, Eindhoven, The Netherlands, Sept. 2004, pp. 843–848.

[11] B. Deutschmann, G. Langer, and G. Auderer, "Characterizing the immunity of integrated circuits against electrical fast transient disturbances," in *Proc. 4th International Workshop on Electromagnetic Compatibility of Integrated Circuits*, Angers, France, Mar. 2004.

[12] F. Musolino and F. Fiori, "Investigation on the susceptibility of microcontrollers to EFT interference," in *Proc. IEEE International Symposium on Electromagnetic Compatibility*, Chicago IL, USA, Aug. 2005, pp. 410–413.

[13] F. Fiori and F. Musolino, "Investigation on the effectiveness of the IC susceptibility TEM cell method," *IEEE Transactions on Electromagnetic Compatibility*, vol. 46, no. 1, Feb. 2004.

[14] J. Kiwitt, "Effiziente Simulation elektrodynamischer Wechselwirkungen und Parameteroptimierung in beliebig geformten Leiterstrukturen," Ph.D. dissertation, Universität Fridericiana Karlsruhe, Germany, July 1999.

[15] A. Dietermann, J. Kiwitt, and K. Reiss, "Hybrid time/frequency-domain simulation of transient electromagnetic coupling of interconnect," in *Proc. 1st IEEE Workshop On Signal Propagation On Interconnects*, Travemünde, Germany, May 1997.

[16] I. Ndip, W. John, and H. Reichl, "A novel methodology for efficient modeling and optimization of complete signal paths in IC packages and PCBs," in *3rd European Design Automation Conference (ZEDAC)*, Köln, Germany, Nov. 2005.

[17] F. Fiori and F.Musolino, "Comparison of IC conducted emission measurement methods," in *IEEE International Conference on Electromagnetics in Advanced Applications*, Torino, Italy, Sept. 2001, pp. 319–322.

[18] F. Fiori and P. Crovetti, "Comparison of the susceptibility to EMI of MOS and BJT operational amplifiers," in *Proc. 15th International Zurich Symposium on Electromagnetic compatibility*, Zurich, Switzerland, Feb. 2003, pp. 369–372.

[19] Y.-S. Huang and T.-L. Wu, "Numerical and experimental investigation of coupling perturbed by ESD currents on printed circuit boards," in *Proc. IEEE International Symposium on Electromagnetic Compatibility*, vol. 1, Boston, MA, USA, Aug. 2003, pp. 479–486.

[20] S. E. Meiners, "An impulse generator simulation circuit," Master's thesis, University of Pittsburgh, Pittsburgh PA, USA, Nov. 2002.

[21] R. D. Leo, F. Moglie, and V. M. Primiani, "Analyzing ESD transient suppressors in printed circuits," *Compliance Engineering Journal*, Jan. 2001. [Online]. Available: http://www.ce-mag.com/archive/01/Spring/DeLeo.html

[22] *HSPICE Signal Integrity Guide*, Synopsys, Inc., Mountain View, CA, Mar. 2003. [Online]. Available: http://www.dzzl.cn/admin/Editor/UploadFile/200752422350165.pdf

[23] *CST Microwave Studio 2006*, Darmstadt, Germany, 2006. [Online]. Available: http://www.cst.com/Content/Products/MWS/Overview.aspx

[24] S.-H. Kim, J.-Y. Nam, K.-I. Ouh, S.-J. Hong, and C. Rim, "Analysis of coupling mechanism and solution for EFT noise on semiconductor device level," in *Proc. of the International Conference on Electromagnetic Interference and Compatibility*, New Delhi, India, Dec. 1999, pp. 120–125.

[25] W. H. Parker, "Electromagnetic Interference: A tutorial," in *Proc. IEEE Aerospace Applications Conference*, vol. 3, Aspen, CO, USA, Feb. 1996, pp. 177–186.

[26] P. Kralicek, W. John, and H. Garbe, "Modeling electromagnetic emission of integrated circuits for system analysis," in *Proc. of the conference on Design, Automation and Test in Europe (DATE)*, Munich, Germany, Mar. 2001, pp. 336–340.

[27] J. Hawwary and G. Mönich, "Eine Schnelle Charakterisierung des Abstrahlverhaltens kleiner Leiterplatten," in *Proc. Internationale Fachmesse und Kongress für Elektromagnetische Verträglichkeit*, Düsseldorf, Germany, Apr. 2002, pp. 207–214.

[28] J. Hawwary, "Kenngrößen zur Charakterisierung des Emissionsverhaltens kleiner Leiterplatten," Ph.D. dissertation, Technische Universität Berlin, Germany, Apr. 2003.

[29] M. Roca, E. Isern, and F. Moll, "Improved crosstalk modeling for noise constrained interconnect optimization," in *Proc. Asia South Pacific Design Automation*, Yokohama, Japan, Jan. 2001, pp. 373–378.

[30] L. Ding, D. Blaauw, and P. Mazumder, "Accurate crosstalk noise modeling for early signal integrity analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 5, pp. 627– 634, May 2003.

[31] D. M. Pozar, *Microwave Engineering*, 3rd ed. USA: John Wiley and Sons, Inc., 2005.

[32] S. Öing, W. John, and M. Künne, "Berechnung des Abstrahlungsverhaltens von Verdrahtungsstrukturen auf Leiterplatten," in *Proc. Internationale Fachmesse und Kongress für Elektromagnetische Verträglichkeit (EMV 94)*, Karlsruhe, Germany, Feb. 1994, pp. 521–532.

[33] S. Öing, M. Künne, U. Keller, F. Sabath, and M. Bücker, "Controlling EMI with the extended EMC-workbench," in *Proc. 11th International Zurich Symposium and Technical Exhibition on Electromagnetic Compatibility*, Zurich, Switzerland, Mar. 1995, pp. 557–578.

[34] F. Fiori, "Experimental evaluation of IC susceptibility to RFI," *Compliance Engineering Journal*, vol. 18, no. 2, pp. 62–65, Mar. 2001. [Online]. Available: http://www.ce-mag.com/ce-mag.com/archive/01/03/0103CE_062.html

[35] L. Davis, "Logic family noise margin." [Online]. Available: http://www.interfacebus.com/Logic_Family_Noise_Margin.html

[36] F. K. W. Lee, "Modeling of high-speed printed circuit board," Master's thesis, University of Malaya, Oct. 1997.

[37] K. Gupta, R. Garg, and R. Chadha, *Computer Aided Design of Microwave Circuits*, 1st ed. Washington, USA: Artech House, Inc., 1981.

[38] R. P. Clayton, *Analysis of Multiconductor Transmission Lines*, 1st ed. New York, USA: Wiley, 1994.

[39] G. Stewart, M. Kay, H. Riedell, and R. Pomerleau, "Microstrip discontinuity modeling," in *Proc. IEEE Energy and Information Technologies in the Southeast*, vol. 1, Columbia, SC, USA, Apr. 1989, pp. 107–111.

[40] L. C. Howard and J. M. Dunn, "An expression for the S-parameters of arbitrary oriented microstrip lines," in *Proc. International IEEE Symposium on Microwave Theory and Technique*, vol. 2, 1991, pp. 1085–1086.

[41] R. Araneo and F. Maradei, "Passive equivalent circuits of complex discontinuities: an improved extraction technique," in *Proc. IEEE International Symposium on Electromagnetic Compatibility*, vol. 3, Chicago IL, USA, Aug. 2005, pp. 700– 704.

[42] P. H. Harms and R. M. Fellow, "Equivalent circuits for multiconductor microstrip bend discontinuities," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 1, pp. 62–69, Jan. 1993.

[43] R. Poddar, E. Moon, M. Brooke, and N. Jokerst, "Accurate, rapid, high frequency empirically based predictive modeling of arbitrary geometry planar resistive passive devices," *IEEE Transactions on Components, Packaging and Manufacturing Technology—Part B: Advanced Packaging*, vol. 21, no. 2, pp. 177–183, May 1998.

[44] *Agilent High-Frequency Structure Simulator 5.6*, Agilent Technologies, Inc., Palo Alto, CA 94304 USA, 2000, Application Note 150-15. [Online]. Available: http://eesof.tm.agilent.com/docs/hfss/tutorial/hfss56_tut.pdf

[45] J. A. Dobrowolski, *Introduction to Computer Methods for Microwave Circuit Analysis and Design*, 3rd ed. Boston, USA: Artech House, 1991.

[46] J. P. Parmantier, "An efficient technique to calculate ideal junction scattering parameters in multiconductor transmission line networks," ONERA, Châtillon, FRANCE, pp. 1–14, 1963, AFRL Interaction Note 536.

[47] J. P. Parmantier, J. C. Alliot, G. Labaune, and P. Degauque, "Electromagnetic topology: junction characterization methods," *La Recherche Aerospatiale, ISSN 0379-380X*, no. 5, pp. 71–82, 1990.

[48] J. Vlach and K. Singhal, *Computer Methods for Circuit Analysis and Design*, 2nd ed. Waterloo, Canada: Van Nostrand Reinhold, 1994.

[49] J. O. Attia, *Electronics and Circuit Analysis Using MATLAB*, 2nd ed. Boca Raton, Florida, USA: CRC Press LLC, 2004.

[50] D. Duehren, W. Hobbs, A. Muranyi, and R. Rosenbaum, "I/O buffer modeling spec simplifies simulation for high speed systems," Mar. 1995. [Online]. Available: http://www.eigroup.org/ibis/

[51] T. Steinecke, W. John, H. Koehne, and M. Schmidt, "EMC modeling and simulation on chiplevel," in *Proc. International IEEE Symposium on Electromagnetic Compatibility*, vol. 2, Aug. 2001, pp. 1191–1196.

[52] *PCB Design Guidlines for Reduced EMI*, TEXAS INSTRUMENTS, Dallas, Texas, USA, 1999. [Online]. Available: http://focus.ti.com/lit/an/szza009/szza009.pdf

[53] C. E. Baum, T. K. Liu, and F. M. Tesche, "Numerical results for multiconductor transmission-line networks," Science Applications Inc. Berkeley Calif, Sept. 1977, Interaction Note 322.

[54] C. E. Baum, "On the use of electromagnetic topology for the decomposition of scattering matrices for complex physical structures," CA, USA, July 1985, Interaction Note 454.

[55] C. E. Baum, T. K. Liu, and F. M. Tesche, "On the analysis of general multiconductor transmission-line networks," CA, USA, Nov. 1978, Interaction Note 350.

[56] L. Brancík, "Techniques of time-domain simulation of transmission lines based on laplace transformation methods," BRNO University of Technology, Czech Republic, 1999, Habilitation Thesis, sv.38.

[57] *Logic Selection Guide*, TEXAS INSTRUMENTS, Dallas, Texas, USA, 2001. [Online]. Available: http://focus.ti.com/lit/ml/sdyu001z/sdyu001z.pdf

[58] N. Deo, *Graph Theory with Applications to Engineering and Computer Science*, 1st ed. Englewood Cliffs, N. J.: Prentice-Hall, Inc., 1974.

[59] D. Jungnickel, *Graphen, Netzwerke und Algorithmen*, 1st ed. Leipzig, Wien, Zürich: BI Wissenschaftsverlag Mannheim, 1994.

[60] D. Eppstein, "Finding the k shortest paths," *SIAM Journal on Computing*, vol. 28, no. 2, pp. 652–673, Apr. 1998.

[61] A. Marzal and V. M. Jimenez, "A comparative study of classical algorithms and new approaches for the search of the k-best paths in a graph," Universidad Politecnica de Valencia, Spain," Technical Report DSIC-II/28/92, 1992.

[62] E. Q. V. Martins and M. M. B. Pascoal, "A new implementation of Yen's ranking loopless paths algorithm," *4OR Quarterly Journal of the Belgian, French and Italian Operations Research Societies*, pp. 121–134, 2002.

[63] J. Hershberger, M. Maxel, and S. Suri, "Finding the k shortest simple paths: A new algorithm and its implementation," in *Proc. 5th Workshop on Algorithm Engineering and Experiments, ALENEX03*, Baltimore, Jan. 2003, pp. 26–36.

[64] J. Hershberger and S. Suri, "Vickrey prices and shortest paths: What is an edge worth?" in *Proc. of the 42nd Symposium on the Foundations of Computer Science, IEEE Computer Society Press, Los Alamitos*, 2001, pp. 252–259.

[65] M. Taki, P. Kralicek, U. Keller, and W. John, "Extraction of critical noise propagation paths in high-density interconnect environment," in *Proc. 17th International Wroclaw Symposium and Exhibition on EMC*, Wroclaw, Poland, June 2004, pp. 308–313.

[66] M. Taki and W. John, "Analysis of propagation paths with respect to induced transient noise for interconnect designs," in *Proc. International Symposium on Electromagnetic Compatibility, EMC Europe*, vol. 2, Barcelona, Spain, Sept. 2006, pp. 1106–1110.

[67] M. Taki, C. Hedayat, W. John, and U. Hilleringmann, "Noise propagation paths at PCB-level: A simulation tool," in *Proc. 19th International Wroclaw Symposium and Exhibition on EMC*, Wroclaw, Poland, June 2008, pp. 34–39.

[68] G. W. Rhyne, M. B. Steer, and B. D. Bates, "Frequency-domain nonlinear circuit analysis using generalized power series," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 2, pp. 379–387, Feb. 1988.

[69] C. R. Chang, P. L. Heron, and M. B. Steer, "Harmonic Balance and frequency-domain simulation of nonlinear microwave circuits using the block newton method," *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 4, pp. 431–434, Apr. 1990.

[70] *Guide to Harmonic Balance Simulation in ADS*, Agilent Technologies, Inc., Palo Alto, CA 94304 USA, 2004. [Online]. Available: http://eesof.tm.agilent.com/docs/adsdoc2004A/pdf/adshbapp.pdf

[71] M. Taki and W. John, "Path tracing for injected parasitic noise into printed circuit boards," in *Proc. IEEE International Symposium on Electromagnetic Compatibility*, vol. 3, Chicago IL, USA, Aug. 2005, pp. 937 – 942.

[72] M. Taki, U. Keller, and W. John, "An efficient approach for the extraction and evaluation of most critical transient noise paths on HDI," in *Proc. International Symposium on Electromagnetic Compatibility, EMC Europe*, vol. 1, Eindhoven, The Netherlands, Sept. 2004, pp. 480–484.

[73] M. Taki and W. John, "Determination of propagation of fast induced transient impulses on PCB-level," in *Proc. IEEE International Symposium on Electromagnetic Compatibility*, ser. ISBN: 1-4244-1350-8, Honolulu, Hawaii, USA, July 2007.

[74] M. Taki, W. John, C. Hedayat, and U. Hilleringmann, "Noise propagation for induced fast transient impulses on PCB-level," in *Proc. 18th International Zurich Symposium on Electromagnetic Compatibility*, Munich, Germany, Sept. 2007, pp. 57–60.

[75] M. H. Austern, *Generic programming and the STL*, 1st ed. Reading, MA: Addison-Wesley Professional, Oct. 1999.

[76] B. Eckel, *Thinking in C++: Introduction to Standard C++*, 2nd ed. Upper Saddle River, NJ: Prentice Hall, 2000.