In this thesis an efficient approach to identify and evaluate the critical transient noise paths on printed circuit board level is presented. This approach is based on the determination of the flow of the noise power induced into a system of interconnects and distributed to any sensitive integrated circuit device ports. The noise paths may result from all coupling mechanisms between the transmission structures. Moreover, the noise paths are extracted considering the entire printed circuit board. Dominant and critical signal traces transferring significant noise from a specified noise source to digital device I/O ports can be determined in the frequency domain using advanced and efficient k shortest path algorithms. These are then combine with the signal flow graph circuit matrix to compute the transfer function of the individual weighted signal paths. The noise paths are evaluated in terms of the transmission coefficients over the frequency range of interest. The superimposition of several dominant signal paths delivers a good approximation to the total system response. The associated coupling waveform can be computed by analyzing the whole dominant signal paths, including device drivers and receivers, in the time domain. This can be performed using a hybrid analysis like the harmonic balance technique or the S-parameter analysis. Depending on the component noise margin the path can be identified as critical or not. The approach proposed is able to predict the interconnects responsible for majority of signal degradations at the chip ports. Based on this information protection measure may be introduced to improve the printed circuit board design and develop more reliable circuits.