In this work, the new scalable GigaNetIC chip-multiprocessor architecture was designed and implemented. Due to its flexible and parameterizable hardware structure it is adaptable to various requirements of different application scenarios, thus resulting in a most resource-efficient solution. Especially designed for this architecture, the new hierarchical GigaNoC on-chip network forms the backbone of this chip-multiprocessor system.

A holistic tool chain was developed for the GigaNetIC architecture. It features detailed analysis and optimization of all hardware components, even back-annotated simulation and script-driven modification of the hardware description. In cooperation with the project partners of the University of Paderborn, a self-contained and interlocking tool chain has been developed that also consists of an automatic generated compiler and a C-based, cycle-accurate instruction-set simulator.

Due to the implementation of application-specific instruction set extensions of the N-Core processor core, performance speed-ups of up to 25% for networking applications could be observed. The additionally implemented hardware accelerators enabled a reduction of the processing time of up to three orders of magnitude accompanied by a moderate increase of the chip area. In addition to this, the power consumption of the system-on-chip could be considerably reduced.

Essential measures and formalisms for a cost-function-based analysis and rating of chip-multiprocessors and their components have been introduced, and are applied exemplarily.

Variants of the GigaNetIC architecture are demonstrated as FPGA-prototypes and realized using two current CMOS standard cell technologies.