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Abstract:

**High-Speed MOS ICs for a Signal Processor Input Interface of an Optical Synchronous QPSK Receiver and Related Clock Distribution Issues**

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The exponential growth of the internet traffic makes it necessary to increase the transmission capacity of the backbone optical transmission system. At present most of the internet backbone operates at data rates up to 10 Gbit/s (OC-192/STM-64). Upgrading the capacity of the existing transmission systems using novel modulation techniques is one solution. The Quadrature PSK (QPSK) with polarization multiplex quadruple channel capacity over the intensity modulation scheme. The synchronous QPSK transmission with return to zero (RZ) coding and polarization division multiplexing emerge as the most promising way of upgrading the existing fiber links. This modulation technique can upgrade existing 10 Gbit/s links to 40 Gbit/s. The European commission funded synQPSK project aimed at developing the commercially unavailable components of the synchronous QPSK transmission system. The phase noise tolerant clock and data recovery module is one such component that is being developed. This module includes A/D converters and a digital signal processing (DSP) unit. The nominal data rate of an A/D converter output channel is 10 Gbit/s. The A/D converted received signal is then processed in the DSP unit. The DSP unit is designed using CMOS technology in order to reduce the cost of fabrication and the power consumption. The standard cell module of the DSPU can not operate at 10 GHz clock frequency. Therefore it is necessary to develop a full custom input interface for the CMOS DSPU. The interface reduces the input data rate to a level the standard cell DSPU can process. This dissertation presents the design of the input interface of the synchronous QPSK receiver DSPU (with and without polarization multiplex). The interface was designed using 130 nm bulk CMOS technology. It includes a 1:8 DEMUX stage and a source coupled FET logic to CMOS logic converter stage. The dissertation discusses the design issues of various circuit blocks of the interface as well as the layout. The simulation and test results of both interface, stand alone static frequency divider chip, and 1:2 DEMUX chip are discussed. The results of the simulation of ultra high speed circuit modules are also presented. Furthermore this dissertation presents a method of estimating the expected value of the skew of a balanced H-tree clock distribution network in the presence of random process variations and nonuniform substrate temperature. The proposed algorithm can estimate the expected value of the clock skew when the substrate temperature is non uniform with higher degree of accuracy. The simulation and calculation results are compared to verify the claim.