

Field-programmable Gate Arrays (FPGAs) are widely used for the realization of many different digital circuits in electronic systems. One of the main advantages of FPGAs is that their function can be defined after the production of the chip (*in-field programmability*). Some FPGAs can be reconfigured partially and dynamically (i.e. during run-time). This feature opens completely new ways for the design of digital systems. A system component must no longer be a static element represented by a part of the systems circuitry. With dynamic reconfiguration, system components can be loaded into the system whenever needed. Furthermore, hardware resources can be saved when several system components share the same resources over time instead of occupying a dedicated set of resources each. This thesis explores different approaches of loading dynamic system components into FPGA-systems at run-time. It shows how a mapping of system components to available reconfigurable resources can be managed at run-time and deduces the requirements to the on-chip communication infrastructure. All presented approaches were realized on a prototyping platform. The resource efficiency of different system architectures is analyzed based on these implementations. Furthermore, the costs and benefits of partially and dynamically reconfigurable systems are shown and compared with state-of-the-art static FPGA-systems.