Abstract

The state-of-the-art inverter used in standard and servo AC drives has a control system with two processors. One of them is a microcontroller (MC), whose main job is to accomplish communication with the external world and the other is a DSP (digital signal processor) core, responsible to carry out faster current-control or torque loop. These two processors are memory-mapped for easy exchange of data. To accomplish control, current and rotor position of the motor are necessary to be acquired. To get these information for processing in the DSP, analog-to-digital converters (ADCs) and their associated interface for communication are essential. The interfaces are usually implemented using discrete ICs. The data converters (ADCs) are also external to the DSP; interfaced using serial communication. Design engineers in drives industry like to keep the system untouched for years, but unfortunately, modifications or upgrades in these discrete components or products push the engineers to modify their system. In order to accomplish these hardware modifications, the interfaces can be realized using re-programmable logic chips such as PLDs (programmable logic device). However, PLDs have a very limited range of flexibility and logic capabilities. The cost of the reprogrammable logic has reduced drastically in this decade and along with it the density of logic functions on chip has increased tremendously. These two factors helped the design engineers to think beyond these small interface logic circuits resulting in FPGA entering the field of drive controls. In the near future it is highly probable that FPGAs become the heart of inverter platform to run the control algorithms. The motivation for this thesis is based on utilizing the potential capabilities of FPGA optimally to address the open issues of drive control.

The control system running on a FPGA can easily be approximated as a continuous-time system, due to its very small execution time. Based on this approach in the thesis a special focus is given on analytical design procedure and performance enhancement of well-known AC motor-control schemes (FOC, ISC and DTC). Also the efficient realization of data acquisition systems based on $\Delta\Sigma$-ADC, dynamically reconfigurable control for improving the drive performance and fault-tolerance capabilities are addressed.