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Abstract

High-current variable-voltage (HCVV) rectifiers are used in the metal and chemical industries. Typical power ratings vary from tens of kW to hundreds of MW. Even with the advancement of the power factor correction rectifiers, accepted choices of high-current AC to DC converters remain 6, 12 or 24-pulse thyristor/diode rectifiers, because of high reliability, efficiency and availability of suitable semiconductor devices. The main issues with these rectifiers are poor input power factor, high current harmonic distortion, high-maintenance cost, high weight and large volume. Moreover, to achieve low output voltage ripple, large capacitive filters are required. To tackle these issues, a two-pronged approach is taken in this thesis. First, the power quality issues of thyristor rectifiers are addressed with the help of passive and hybrid filters. Second, completely different, medium-frequency transformer-based topologies are proposed for the HCVV applications.

After a due study of the state-of-the-art rectifiers, two core issues pertaining to the power quality of the HCVV rectifiers are identified, i.e. large reactive power rating of passive filters and inability of passive filters to provide varying reactive power compensation. A topology, with a thyristor assisted tap-changing transformer and a diode-bridge rectifier, is proposed that results into reactive power rating reduction of the passive filter. This scheme is optimized to determine an optimum turns-ratio of the transformer and optimum reactive power rating of the passive filter. Experimental results are presented to evaluate the performance of the system. To deal with the issue of fixed compensation of passive filters, a hybrid filter consisting of a parallel combination of a dominant-harmonic passive filter and a distribution static compensator (DSTATCOM) is proposed. The DSTATCOM is used to provide variable reactive power compensation. Along with it, the dominant-harmonic passive filter, with substantial amount of reactive power support, is provided to reduce required rating of the DSTATCOM. An experimental set-up is built to verify the effectiveness of the hybrid filter. A comparison of this hybrid-filter-based rectifier with a state of the art chopper-rectifier is also presented.

Diverting away from the bulky thyristor/diode rectifiers, for medium-voltage applications, power supplies with medium-frequency transformer are proposed. Two topologies with different levels of modularity are discussed. Systems utilise a modular multilevel rectifier at the input side for connection to the medium voltage grid. Rectified DC voltage is converted to the low-voltage DC using suitable isolated DC-DC converters. These configurations provide unique advantages like good efficiency, high input power factor, good input current quality and controlled output current (with low output voltage ripple) over the full operating range. Moreover, these topologies are modular and result into size reduction as compared to the conventional rectifiers. Circuit configurations, design, control, simulation results and performance (power factor, current THD, efficiency and volume) of the proposed system are discussed in detail. A comparison of these topologies with the state of the art chopper-rectifier is also carried out.

Zusammenfassung

Hochstrom-Gleichrichter mit variabler Ausgangsspannung (HCVV-Rectifiers) werden in der Metall- und der Chemischen-Industrie verwendet. Die typische Nennleistung beträgt zwischen mehreren zehn Kilowatt bis einigen hundert Megawatt. Selbst mit der Weiterentwicklung durch Leistungsfaktorkorrektur-Gleichrichter bleiben 6-, 12- oder 24-pulsige Thyristor-/Dioden-Gleichrichter der Stand der Technik bei AC/DC Wandlern. Die Hauptgründe sind ihre hohe Zuverlässigkeit, der hohe Wirkungsgrad und die Verfügbarkeit geeigneter Halbleiter-Bauelemente. Die größten Probleme sind ihr geringer Eingangs-Leistungsfaktor, die hohe Verzerrung des Stroms, ein hohes Gewicht und ihre Baugröße. Um diesen Herausforderungen zu begegnen, werden in dieser Arbeit zwei Ansätze verfolgt. Als erstes werden Probleme des Thyristor-Gleichrichters bezüglich der Leistungsqualität durch passive und hybride Filter angegangen. Im zweiten Teil der Arbeit, werden unterschiedliche Transformator-basierte Topologien, die mit mittlerer Frequenz arbeiten, für HCVV-Lasten vorgestellt.

Nach eingehender Analyse von Gleichrichtern auf dem Stand der Technik, können zwei Kernprobleme identifiziert werden, welche die Leistungsqualität dieser Gleichrichter beeinträchtigen. Dies sind die Reduktion der Filtergröße und die Tatsache, dass passive Filter nicht in der Lage sind für eine variable Blindleistungskompensation zu sorgen. Ein Transformator mit mehreren Thyristor gesteuerten Anzapfungen- und einem nachgeschalteten Dioden-Gleichrichter wird vorgeschlagen. Diese Konfiguration bietet eine reduzierte Blindleistung durch den passiven Filter. Sie ist darauf ausgelegt, ein optimales Windungsverhältnis des Transformators und eine optimale Blindleistungsreduktion des passiven Filters zu erreichen. Versuchsergebnisse werden präsentiert, um die Leistungsfähigkeit des Systems zu bewerten. Um dem Problem der festen Kompensation des passiven Filters zu begegnen, wird ein hybrider Filter vorgeschlagen, welcher aus einer parallelen Zusammenstellung eines passiven Filters zur Unterdrückung der dominanten Harmonischen und einem statistischen Blindleistungskompensator (DSTATCOM) besteht. Der statistische Blindleistungskompensator sorgt für eine variable Blindleistungskompensation. Dank dem passiven Filter zur Unterdrückung der Harmonischen kann ein hoher Anteil der Blindleistung kompensiert werden, was die Anforderungen an den statistischen Blindleistungskompensator verringert. Ein Versuchsaufbau wird genutzt, um die Wirksamkeit des Hybridfilters zu bestätigen. Zudem wird ein Vergleich zwischen einem Gleichrichter mit Hybridfilter und einem Gleichrichter nach dem aktuellen Stand der Technik durchgeführt.

Abweichend von voluminösen Thyristor-/Dioden-Gleichrichtern werden Netzteile mit Mittelfrequenz-Transformator vorgestellt. Zwei Topologien mit verschiedenen Modulationsgraden werden behandelt. Diese Systeme verwenden einen modularen mehrstufigen Gleichrichter, einen Umrichter, einen Mittelfrequenz-Transformator und einen Dioden-Gleichrichter um eine Mittel-Wechselspannung in eine Nieder-Gleichspannung über einen Mittelfrequenz-Wechselspannungs-Zwischenkreis zu wandeln. Die Konfigurationen bieten spezifische Vorteile wie z.B. eine hohe Effizienz, einen großen Leistungsfaktor am Eingang, eine gute Eingangsspannungsqualität und einen regelbaren Ausgangsstrom über den gesamten Betriebsbereich. Zusätzlich sind die Konfigurationen modular und führen zu einer Verkleinerung der Baugröße im Vergleich zu konventionellen Gleichrichtern. Die Konfigurationen der Schaltung, Auslegung, Reglung, Ergebnisse der Simulation und die Leistungsfähigkeit

(Leistungsfaktor, Verzerrung des Stroms, Wirkungsgrad und Baugröße) des vorgestellten Systems werden im Detail beschrieben.

Table of Contents

Nomenclature

Symbol	Description
α, α_1, α_2	Thyristor firing angles
β	Extinction angle
δ	Skin depth
ε	Voltage ripple across sub-module capacitor
ϕ	Phase-angle difference between input voltage and current
θ	Rotating-reference-frame transformation-angle
ρ	Resistivity of wire
ρ_i	Density of core material
ω	Angular grid frequency
A_1, A_2	Area of the conductors of primary and secondary windings
A_c	Cross section area of core
a_c	Width of the middle limb of core
A_L	Area product
A_w	Window area
a_w	Length of side of window
B_m	Maximum flux density
B_{sat}	Saturation flux density
C_c	Output capacitor of chopper-rectifier
C_{dc}	Output capacitor of thyristor- or diode-based rectifier
C_{dcst}	DC-bus capacitor of DSTATCOM

C_f	Capacitor of passive filter
C_o	Output filter capacitor of medium-frequency transformer-based topologies
C_i	Capacitor of MMI sub-module
C_r	Capacitor of MMR sub-module
E_{on}	Turn-on energy
E_{off}	Turn-off energy
f	Frequency
f_s	Switching-frequency of DSTATCOM
f_{si}	Switching-frequency of MMC inverter
f_{sr}	Switching-frequency of MMC rectifier
H	Harmonic order
h_w	Height of the winding
i_{dcl}	DC Load current
i_{dev}	Current through the semiconductor device
i_{dcmv}	DC current through medium-voltage DC-bus
i_{fa}, i_{fb}, i_{fc}	Passive filter currents of phase *a*, *b*, and *c*
i_L	Load current
i_{L1}, i_{L2}, i_{L3}	Currents through output inductors of the chopper-rectifier
i_{La}, i_{Lb}, i_{Lb}	Cumulative current of the rectifier and passive filter in the three phases
$i_{L\alpha}$, $i_{L\beta}$	Cumulative current of the rectifier and passive filter in α–β coordinates
i_{Ld}, i_{Lq}	Cumulative current of the rectifier and passive filter in rotating ref. frame
i_{na}, i_{nb}, i_{nc}	MMC-rectifier Upper-arm currents of phase *a*, *b*, and *c*
i_{pa}, i_{pb}, i_{pc}	MMC-rectifier Upper-arm currents of phase *a*, *b*, and *c*
i_{ra}, i_{rb}, i_{rc}	12-pulse thyristor-rectifier currents of phase *a*, *b*, and *c*

i_{rA}, i_{rB}, i_{rC}	6-pulse diode-rectifier currents of phase *a*, *b*, and *c* on the secondary side of transformer
i_{sa}, i_{sb}, i_{sc}	Source side currents of phase *a*, *b*, and *c*
$i_{s\alpha}$, $i_{s\beta}$	Source side currents in α–β frame
i_{sd}, i_{sq}	Source side currents in d-q frame
i_{sta}, i_{stb}, i_{stc}	DSTATCOM currents in the phase *a*, *b*, and *c*
i_{std}, i_{stq}	DSTATCOM currents in rotating ref. frame
i_{Ta}, i_{Tb}, i_{Tc}	Input currents in the phase *a, b, and c* of voltage sequence control-based rectifier
i_{Ta1}, i_{Ta2}	Currents through thyristor pair 1 and 2 of phase-*a*
i_{za}, i_{zb}, i_{zc}	Circulating currents of phase *a*, *b*, and *c*
J	Current density
K_{pA}, K_{iA}	PI-controller gains average capacitor voltage balancing control
K_{pB}	P-controller gains for capacitor voltage balancing control
K_{pdcmv}, K_{idcmv}	PI-controller gains for medium voltage DC-bus voltage control
K_{pid}, K_{iid}	PI-controller gains for *d*-axis current control
K_{piq}, K_{iiq}	PI-controller gains for *q*-axis current control
K_{pL}, K_{iL}	PI-controller gains for load current control
k_w	Winding fill factor
k_f	Form factor
l_1, l_2	Length of the conductors of primary and secondary windings
L_c	Chopper-rectifier filter inductor
L_{dc}	Rectifier output filter inductor
L_f	Passive filter inductor
L_{l1}, L_{l2}	Leakage inductances of primary and secondary windings

l_{mt}	Length of the mean turn
L_r	Input filter inductor at the rectifier stage of medium-frequency transformer-based topologies
L_s, X_s	Source side inductor and inductor impedance
L_{st}	DSTATCOM filter inductor
L_l, X_l	Transformer leakage inductor and impedance
m	number of sub-modules in one phase-leg
n_1, n_2, n_s	Transformer turns ration of primary winding 1, 2 and secondary winding
N_1, N_2	Transformer turns ration of primary and secondary winding
$\overline{p}_{cdev}$	Conduction loss of semiconductor device
$\overline{p}_{sdev}$	Switching loss of semiconductor device
Q	Quality factor of the passive filter
Q_f	Reactive power rating of passive filter
Q_{fPH}	Reactive power rating of passive-filter of parallel hybrid filter
Q_{max}	Maximum reactive power
Q_{min}	Minimum reactive power
Q_{st}	Reactive power rating of DSTATCOM
Q_{VSCPH}	Reactive power rating of VSC of parallel hybrid filter
r_1, r_2	Resistances of primary and secondary windings of Transformer
R_s	Resistance of source side inductor
R_l	Transformer winding resistance
r_L	Load resistor
r_{lT}	Load resistance at top load line
r_{lB}	Load resistance at bottom load line

S	Apparent power
T	Semiconductor device temperature
T_s	Time period
v_a, v_b, v_c	Three-phase line-neutral grid voltages
v_α, v_β	Grid voltages in α–β frame
v_{AN}, v_{BN}, v_{CN}	Three-phase line-neutral voltages on secondary side of transformer
v_{ac}, v_{ba}, v_{cb}	Three-phase line-to-line grid voltages
V_c	Root mean square converter side voltage
v_{ca}	Average of capacitor voltages of sub-modules of phase-*a*
v_{cxj}	Capacitor voltages of sub-module SM*xj* (*x*=*a*, *b*, *c* and *j*=1-8)
v_d, v_q	Grid voltages in d-q frame
v_{dcl}	Load voltage
v_{dcl0T}	load voltage at top load line with zero current
v_{dcl0B}	load voltage at bottom load line with zero current
v_{dcmv}	Medium-voltage DC-bus voltage
v_{dcst}	DC-bus voltage of DSTATCOM
v_{dev}	Voltage across the semiconductor device in on-state
v_L	Load voltage
V_{LLsec}	Root mean square line-to-line voltage at the secondary side of transformer
V_{LL}	Root mean square line-to-line voltage
V_m	Peak amplitude of the phase-neutral grid voltage
v_{pa}, v_{na}	MMC-rectifier upper- and lower-arm voltages of phase *a*
V_s	Root mean square grid voltage

v_{xj}^{*}	Reference voltage signal for switching-pattern generation of SMxj (x=a, b, c and j=1-8)
v_{Bxj}	Signal for switching-pattern generation, corresponds to balancing sub-module capacitor voltages (x=a, b, c and j=1-8)
v_{Ax}	Signal for switching-pattern generation corresponds to balancing the average voltage of sub-module capacitors (x=a, b, c)
V_i	Volume of the transformer core
V_w	Volume of the transformer windings

Acronyms

AC	Alternating current
BLL	Bottom load line
CRPF	Chopper-rectifier with passive filter
DC	Direct current
DF	Distortion factor
DPF	Displacement power factor
DSTATCOM	Distribution static compensator
IGBT	Insulated gate bipolar transistor
LV	Low voltage
MMC	Modular multi-level converter
MMI	Modular multi-level inverter
MMR	Modular multi-level rectifier
MV	Medium voltage
MF	Medium frequency
OLTC	On load tap changer

PF	Power factor
PI	Proportional and integral
PSB	Phase-shifted full-bridge
RMS	Root mean square
SM	Sub-module
SST	Solid-state transformer
STATCOM	Static compensator
TDD	Total demand distortion
THD	Total harmonic distortion
TLL	Top load line
TRHF	Thyristor rectifier with hybrid filter
UPS	Uninterruptible power supply
VSC	Voltage source converter
ZCS	Zero current switching
ZVS	Zero voltage switching

1. Introduction

Depending on the required DC voltage, rectifiers can be broadly divided into two categories: variable- and fixed-output-voltage types. Front-end rectifiers with fixed DC-bus voltage are required in the AC-AC conversion process for motor drives, uninterruptible power supplies, inverters, wind power converters, DC power supplies and high-voltage DC transmission system etc.. Because of the vast number of applications, sufficient research and development efforts were put into the advancement of these rectifiers. Thus, rectifiers for these applications (mostly boost type) stand at a fairly advanced stage with a good input power factor, low current THD, low DC-voltage ripple and good reliability. Conversely, variable DC-voltage rectifiers, falling into a niche category, are still dominated by multi-pulse rectifiers using diodes or thyristors.

High-current variable-voltage (HCVV) rectifiers are required for supplying power to DC-arc furnaces, electrolysers, water-purifiers and resistive heaters etc.. The power requirement spans from a few hundreds of kW (small size hydrogen electrolyser) to hundreds of MW (aluminum smelter). Based on the load power, these rectifiers can be connected to a distribution-voltage grid or a medium-voltage grid. Depending on the characteristics, HCVV loads can be segregated into arcing loads, electrolysers and resistive loads. Most commonly, diode and thyristor based rectifiers are used for high-power high-current applications because of their proven reliability, good efficiency, availability of suitable ratings of semiconductor switches, robustness, long life and simplicity of the solutions. A snapshot of the topologies, issues and proposed solutions is provided in Fig. 1.1. Depending on the power level, grid voltage and other application specific requirements, different types of configurations are used in industry, such as:

1. Multi-pulse diode rectifier with tap-changing (OLTC) transformer and saturable reactor
2. Multi-pulse thyristor rectifier with tap-changing transformer
3. Multi-pulse thyristor rectifier
4. Chopper-rectifier (multi-pulse diode rectifier followed by multi-phase chopper)

For high-power applications (more than a few MWs), rectifiers are connected to the medium-voltage (MV) grid and ‘multi-pulse diode rectifier with tap-changing (OLTC) transformer and

saturable reactor' and 'multi-pulse thyristor rectifier with tap-changing transformer' are used for rectification. Because of OLTC and multi-pulse rectifiers, input power factor and power quality remains fairly good. However, these rectifier-systems suffer from issues of mechanical wear and tear of OLTC. Moreover, dynamic response of the rectifiers remains poor due to the slow mechanical parts. Till 10-30 MW power-level, chopper-rectifiers are also used. Chopper-rectifiers with 12- or 24-pulse diode rectifier fair well in terms of current THD (8-10 %), power factor (0.9-0.96), output-voltage ripple and dynamic response, but not on the count of size and weight. Besides, because of the use of line-frequency transformer and filter components, all these topologies are very bulky.

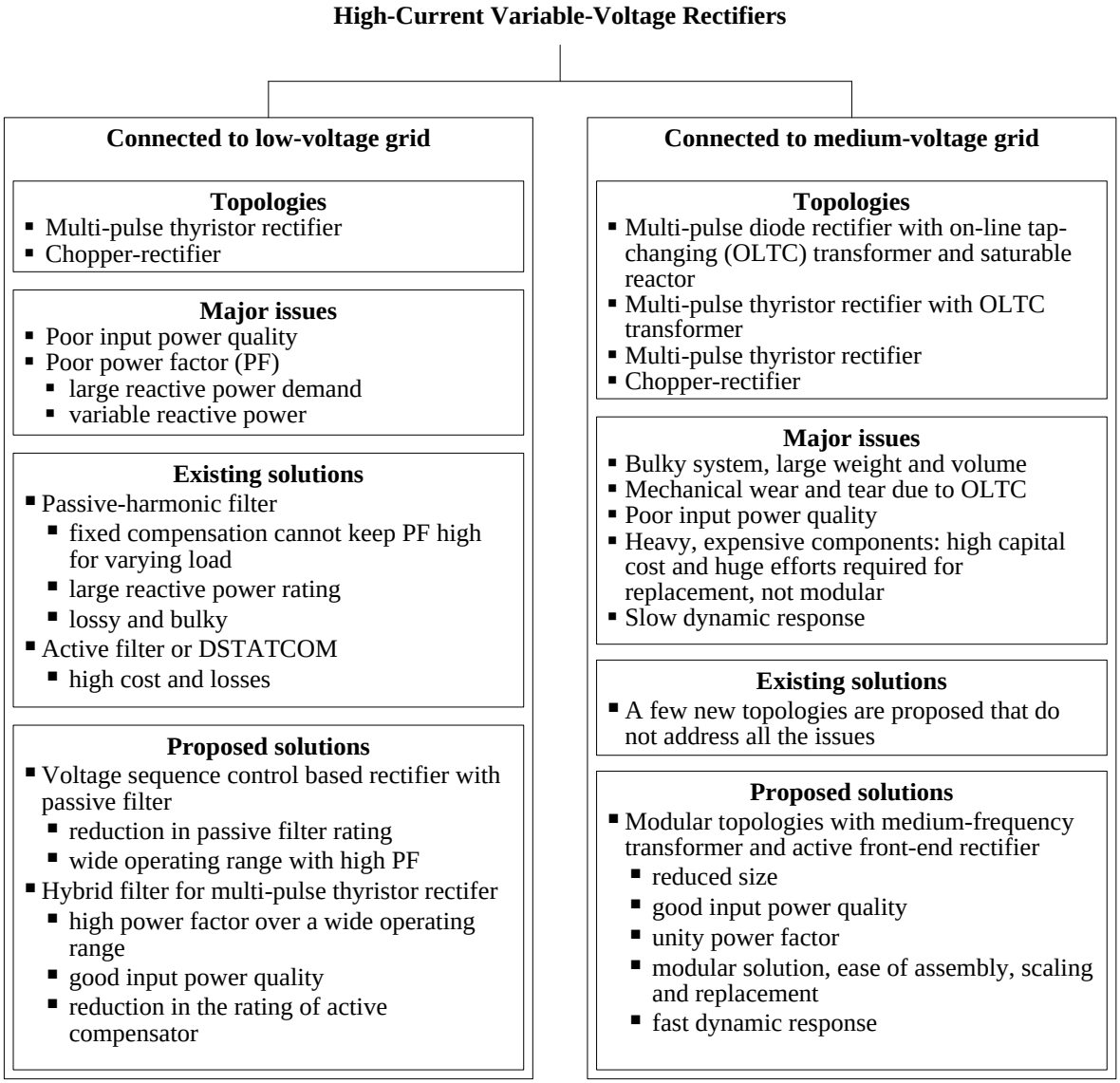


Fig. 1.1 Snapshot of the state of the art rectifier topologies, issues and proposed approach.

At the distribution-voltage level, multi-pulse thyristor rectifiers and chopper-rectifiers are more commonly used. The issues with thyristor-rectifiers, connected to the distribution-voltage level, differ from rectifiers connected to medium-voltage level. At distribution-voltage level, OLTC is not put to the use due to its commercial unavailability. Therefore, multi-pulse thyristor rectifiers suffer from issues of poor power factor and high current THD. Passive harmonic filters are most commonly used to deal with these issues. However, it fails to keep the power factor high, over a wide load range, due to the fixed nature of compensation. Additionally, passive filters add to the overall losses and size. None the less, the applicability of compensating devices cannot be ruled out especially for retrofit applications. Therefore, the need is to minimize the required rating of compensating devices and improve their operation so as to achieve high power factor and low current THD over a wide operating range.

In the present work, attempts have been made to deal with some of the above-stated problems catering with HCVV rectifiers. As shown in Fig. 1.1, a two-fold approach is used to deal with the issues:

- investigation of compensating devices for thyristor-converters to deal with the power quality issues and (mainly at the distribution-voltage level)
- development of new topologies involving medium-frequency (1-2 kHz) transformers (at medium voltage level)

Active and passive reactive power and harmonic compensation techniques, pertaining to 6- or 12-pulse rectifiers are looked into detail. The approach taken concentrates on the power factor improvement of the existing 6- or 12-pulse thyristor rectifiers. Attempts have been made to:

- reduce the rating of passive filter by voltage sequence control-based rectifier topology
- investigate hybrid filter (passive filter parallel with DSTATCOM) with a reduced DSTATCOM rating

A comparison of the performance of the hybrid-filter-based rectifier with state of the art chopper-rectifier is also carried out.

As discussed, for high-power applications most of the rectifiers are connected to the medium-voltage grid. In the next-step, new configurations involving medium-frequency transformers are proposed for medium-voltage applications.

The thesis is divided into 7 chapters including the Introduction and Conclusions. Chapter 2 covers the state of the art of rectifier topologies. In this chapter, applications and topologies along with their advantages and disadvantages are covered. Power quality issues are discussed and gaps and challenges are identified. This chapter essentially describes the motivation to carry out this work and defines the direction of the study.

With the motivation of reducing the reactive power rating of the passive filter, a voltage sequence control-based topology is discussed in Chapter 3. This topology includes a thyristor-based tap-changing transformer and a six-pulse diode rectifier along with a dominant-harmonic passive filter. The principle of operation is discussed and the system is optimized to reduce the passive filter rating and enhance the operating range with high power factor.

Compensating devices pertaining to multi-pulse rectifiers are discussed in Chapter 4. Analysis, design, control and implementation of hybrid filter for varying reactive power load is presented.

Being the most advanced rectifier solution, which is actively used in industry for HCVV applications, the chopper-rectifier is discussed in Chapter 5. A detailed comparison between chopper-rectifier and thyristor rectifier with hybrid filter is included in this chapter.

Chapter 6 proposes new rectifier configurations for HCVV applications. The concept of using medium-frequency transformer along with medium-voltage active rectifiers is dealt in detail. Two topologies with different level of modularity are investigated.

Chapter 7 concludes the work.

2. State of The Art: High-Current Variable-Voltage Rectifiers

High-current rectifiers are required in many industrial processes, especially in the metal and chemical industries [1]–[5], [A]. With the industrial revolution, the need for more and more metal has led to bigger metallurgical plants. Today smelters with power rating of few GW are used for aluminium extraction [47]. The required current ratings have gone up to 350 kA [2]. It all started with electro-mechanical rectifiers and from stages of mercury arc rectifiers and diode rectifiers presently thyristor rectifiers are the main work-horse for the industry. In relatively small power applications (up to 25 MW), solutions based on IGBT technology are also being employed [1].

In this chapter, a review of the existing rectifier technology is presented. Although the focus of the thesis is rectifiers with the power rating up to 10 MW, the review tries to covers the entire space of high-current variable-voltage rectifiers. This furnishes two purposes, 1. the existing techniques used for higher power applications may be utilised to improve the rectifiers in focus and 2. learning form this work may be extended to higher power levels. The organisation of this chapter is as follows: in the first Section, an introduction is given for the foremost applications requiring high-current variable-voltage DC power-supplies. After that, rectifier topologies, used in the industry are introduced and their applications, advantages/disadvantages and other salient features are described. Apart from this other circuit configurations proposed in literature (but not commonly used by industry) are also reviewed. Power quality issues with the thyristor rectifiers are highlighted and various compensation techniques proposed in the literature are discussed briefly. At the end, major gaps and challenges are outlined that provides the motivation to carry out this work.

2.1 High-Current Variable-Voltage DC Applications

Depending on the load characteristics, as shown in Fig. 2.1, the high-current loads can be segregated into two categories: arcing loads and electrolysers [1]–[5]. Arcing loads, such as DC arc furnaces and plasma torches, are used for melting (e.g. iron scrap melting, conducting feed material) [6]–[7]. Whereas chemical electrolysis is used in metal refining and winning [1],

[8]–[10]. Electro-refining is electro-deposition of a pure metal at the electrode from the impure metal and electro-winning is metal deposition from ore. The process is used for extraction of copper, aluminium, zinc and magnesium etc.. Hydrogen, chlorine, sodium hydroxide, sodium chlorate, oxygen and adiponitrile production also utilises the electrolysis process [11]–[13]. Table I provides a list of typical high-current applications [1], [2]. There are other applications of high current variable voltage rectifiers, which include heating power supplies and power supplies for ship applications. In traditional electrical-propulsion vessels, multiple DC connections are made to thrusters, propulsion drives and water purifiers. Power consumption via DC link can be as high as 80 % of the total electrical power consumption. These applications typically fall under less than 1 MW power category and are connected to a distribution-level grid.

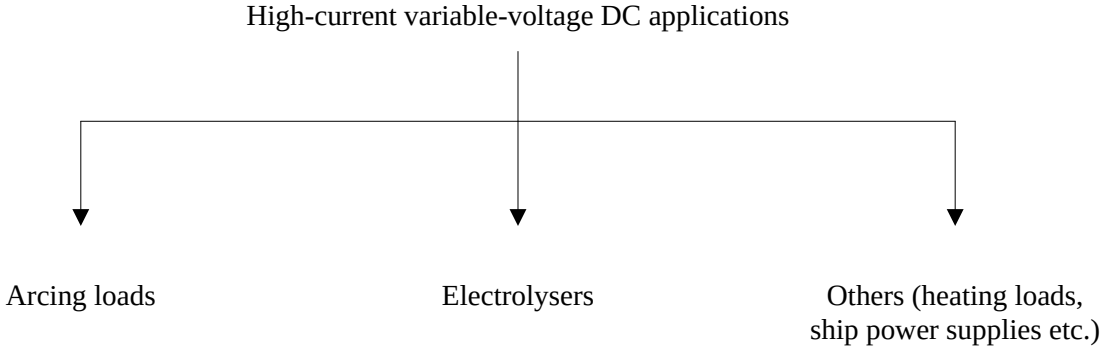


Fig. 2.1 Classification of high-current variable-voltage DC loads.

Table 2.1 Typical rating of high-current variable-voltage rectifiers used in different applications [1], [2]

Application	**Load Current in kA**	**Load Voltage in V**
Chemical electrolyzer	5-150	40-1000
Aluminum potline	10-300	<1300
DC arc furnace	50-130	600-1150
Graphitizing furnace	20-120	50-250
Hydrogen electrolysis	5-100	100-1000
Copper refining	10-50	40-350
Plasma torch	1-10	500-3000

The DC furnace technology provides some advantages over AC furnaces, such as simpler design, lower consumption of the electrode material, relatively stable arc production, better temperature distribution, lower noise and less voltage flicker and harmonic generation [6], [7]. Voltage and current requirements of DC arc furnaces vary over a large range (a relatively high-voltage is needed to establish the arc contracted to a low-voltage during normal operation). Fig.

2.2 shows the characteristics of a 10 MW DC arc furnace. Voltage and current vary from 1000 V, 10 kA to 385 V, 28 kA. Another arcing application, which requires a high-current rectifier is plasma arc generation. Such equipments are used for waste disposal. The power requirement of such plasma generation units depends on the size and vary from several hundreds of kW to tens of MWs. Fig. 2.3 shows the typical load curve of a 4 MW 2300–3000 V, 300–1700 A plasma arc generator.

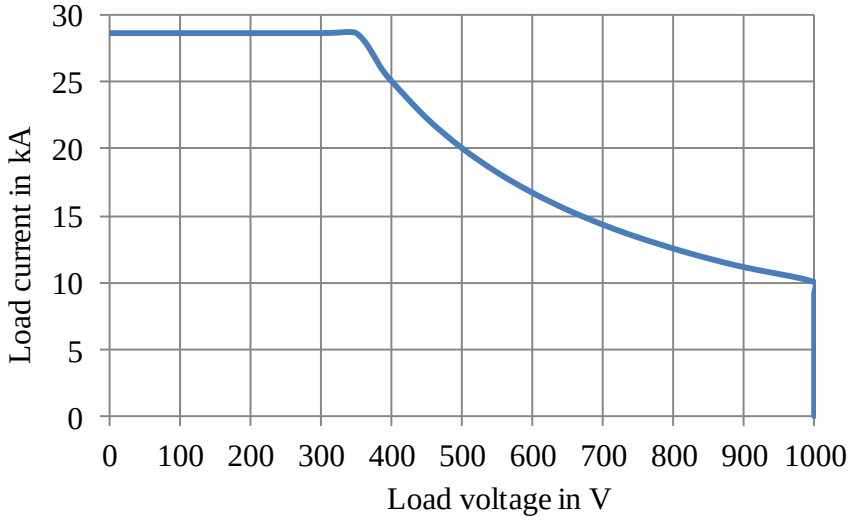


Fig. 2.2 Load curve of a 10 MW arc furnace.

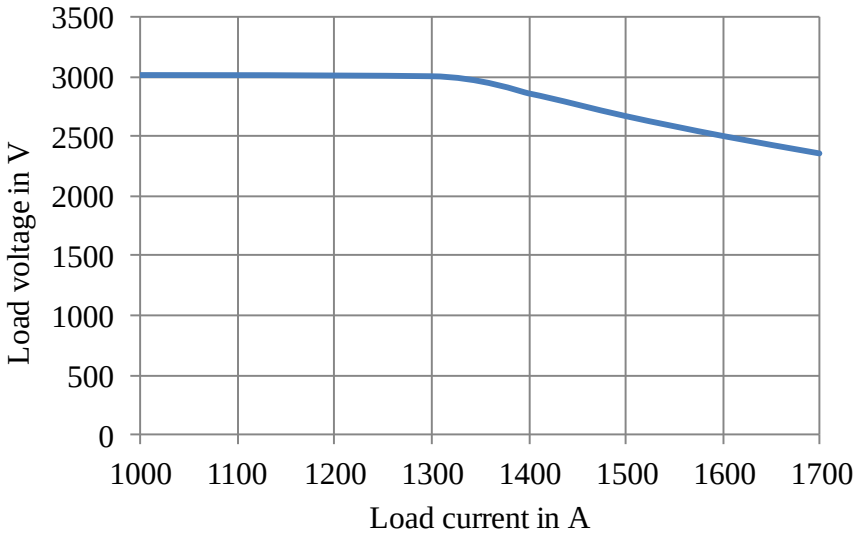


Fig. 2.3 Load curve of a 4 MW plasma generator.

Another type of load that requires high-current rectifiers is an industrial electrolyser [1], [2], [8]–[13]. Fig. 2.4 shows a typical load curve of a 1 MW electrolyser for hydrogen production. The production rate is proportional to the load current and the voltage depends on the cell open-

circuit voltage and internal resistance. The internal resistance varies with temperature and the age of the cell. Electrolysers for hydrogen production are available in different power levels. Electrolysers with the rating of few hundreds of kW are used at hydrogen filling stations. The typical output voltage is below 200 V and the input is connected to a distribution-level three-phase grid. Other types of multi-MW electrolysers are employed in conjunction with renewable (solar or wind) power plants to generate hydrogen at a large scale. These plants are typically connected to a medium-voltage grid.

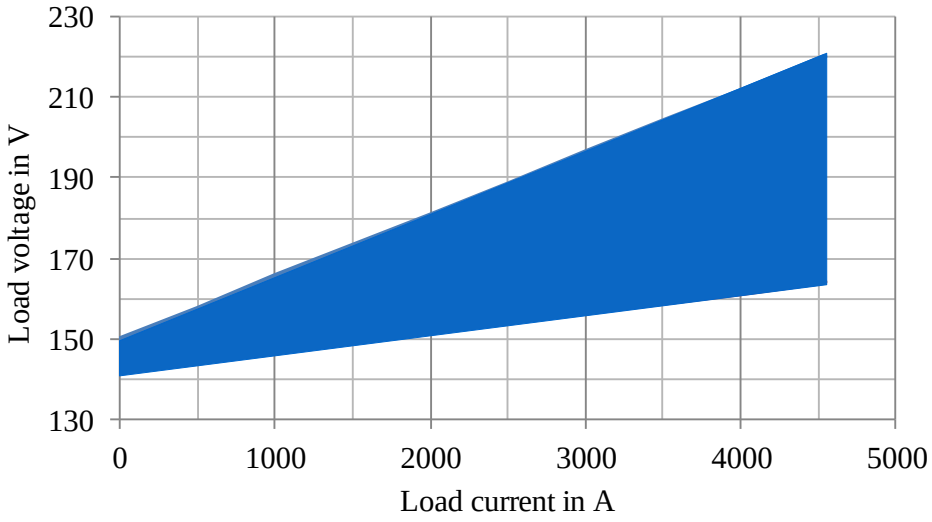


Fig. 2.4 Area of operation of a 1 MW electrolyser for hydrogen generation.

2.2 General Requirements of Rectifiers for High Current Applications

The requirements for a rectifier can be divided into different performance criteria, such as, output voltage and current quality, input power quality and power factor, reliability, efficiency and size etc.. Apart from requirements in terms of input/output voltage, current, power, frequency level and range, other requirements can be listed as [2]:

- Low ripple in voltage and current as required by load over the requisite load variation
- Fast dynamics of output voltage and current as required by the process
- Overload capability
- Power factor higher than the limit set by the utility, ideally unity power factor.
- Low current THD as specified by utility or power quality standards
- High reliability as specified by customer in terms of MTBF (mean time between failure)
- Installation and running costs

- Modularity, ease of assembling manufacturing and repair
- High efficiency achievable by economically viable means
- Lower weight, foot print and volume as specified by customer depending on the site constraints

Apart from these, there could be other constraints like grid short circuit level (weak grid may put extra limitation on harmonic pollution and voltage regulation), production schedule, start up currents etc.

2.3 State of The Art Rectifier Topologies for High-Current Variable-Voltage Applications

Diode and thyristor-based rectifiers are most commonly used for high-power high-current applications because of their proven reliability, availability of suitable ratings of semiconductor switches, robustness, long life and simplicity of the solutions [1]–[5]. Depending on the power levels and other application specific requirements, different types of configurations are used in the industry:

- Multi-pulse diode rectifier with tap-changing transformer and saturable reactor
- Multi-pulse thyristor rectifier with tap-changing transformer
- Multi-pulse thyristor rectifier with passive filters
- Chopper-rectifier (multi-pulse diode rectifier followed by multi-phase chopper)

Apart from these topologies, GTO or IGBT and diode (in series) based current source rectifier, other variants of thyristor rectifiers and modular topologies are also proposed for high current applications; however, presently these topologies are not commonly used in the industry [1], [2], [4], [5].

Before going deep into the merits of each of the above-mentioned topologies it is important to look into the two structures of six-pulse rectifiers shown in Fig. 2.5 and Fig. 2.6. Fig. 2.5 shows the bridge configuration, which is widely used in practice; however, for low-voltage applications, a six-phase or double-star configuration (Fig. 2.6) is more common as it results in better semiconductor efficiency. In this configuration, the neutrals of two star circuits are connected using an inter-phase-transformer, which facilitates the parallel operation of the two star windings and diode rectifiers. This six-pulse configuration can be paralleled with another

similar rectifier along with a star-primary to form a 12-pulse rectifier [24]. Rectifier configurations shown in Fig. 2.5 and Fig. 2.6 are also known as ANSI 25 and ANSI 45 circuits, respectively and are discussed in various text books [14]–[18].

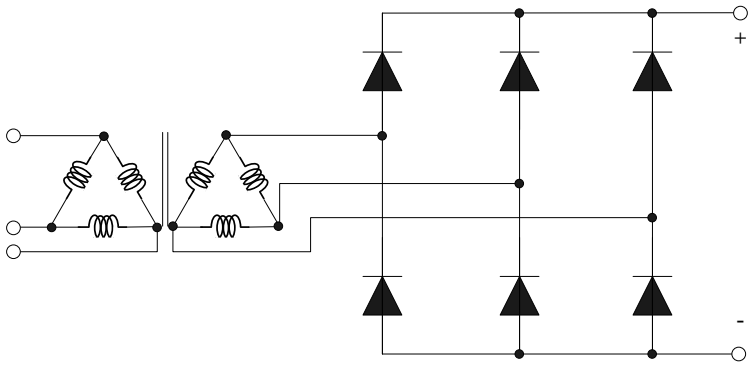


Fig. 2.5 ANSI 25 rectifier configuration.

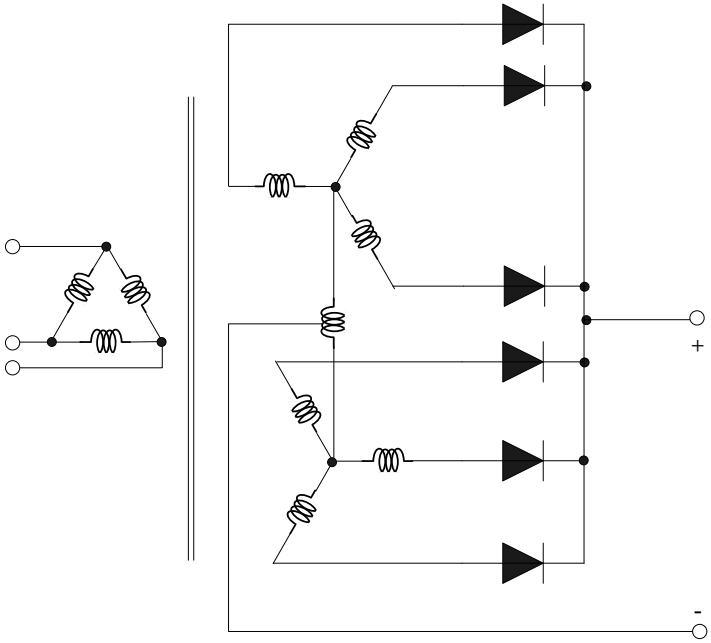


Fig. 2.6 ANSI 45 rectifier configuration

2.3.1 Multi-Pulse Diode Rectifiers with On-Load Tap-Changing Transformers and Saturable Reactors

Multi-pulse diode rectifiers along with mechanical on-load tap-changers (OLTC) and saturable reactors are used for step-less output DC voltage control [1], [2], [21]–[23]. Fig. 2.7 shows the block diagram of the rectifier system. The topology is generally used for very high-power applications. The tap-changer is mostly connected at the primary side of the transformer and used for coarse control of the output DC voltage. The saturable reactor has a control

winding, which is fed through a DC source. As the DC current in the control winding is increased, core saturates and inductance value reduces. Thus the output voltage is controlled using impedance variation of a satuarble reactor. Since the saturable reactor can provide only small change in the output voltage due to electrical constraints, several taps are introduced at the primary winding of the transformer. Moreover, the number of taps is kept high because of the limitation arising from the highest allowed tap to tap voltage of the tap changer to limit the short-circuit current flowing between the contacts. Both oil-filled and vacuum tap changers are commercially available for the use up to 300 kV system voltage with maximum of 5 kV voltage step. This configuration is used for very high-power applications such as aluminium potline, graphitizing furnaces and electrolysers [2]. Several diode rectifiers are used to feed the entire load as shown in Fig. 2.8. A separate transformer is used in some cases depending on the voltage of the medium-voltage grid. The input power factor and current THD of the system remains fairly good because of the multi-pulse operation and use of the tap-changing transformer. The biggest draw-back of this configuration is the mechanical wear and tear of the tap-changer and high maintenance cost [2]. The system also suffers from the poor dynamic behaviour of the tap changer with a response time of the order of a few seconds [22], [23]. This time delay can cause over-currents during potline switching operations. Apart from this, the system is quite bulky because of the use of line frequency transformer and reactors.

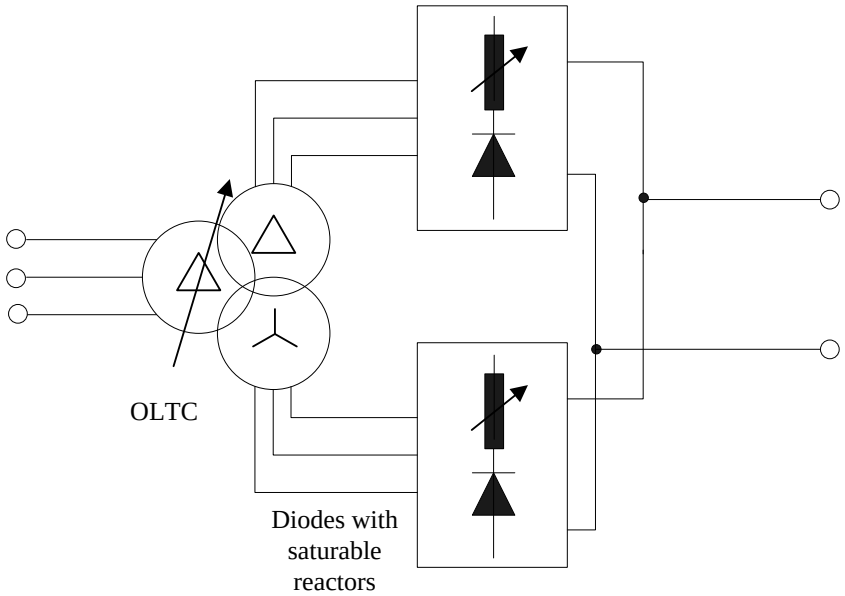


Fig. 2.7 Block diagram of 12-pulse diode rectifiers with tap-changing transformer and saturable reactors.

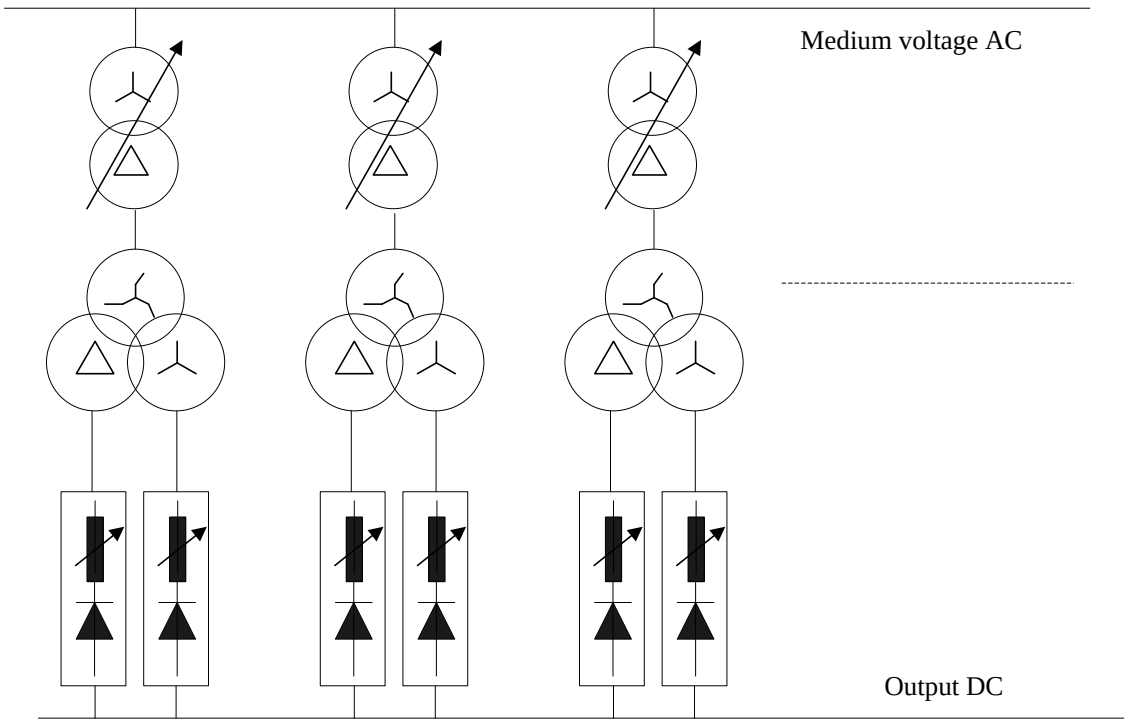


Fig. 2.8 Rectifier units connected in parallel to feed high-power load.

2.3.2 Multi-Pulse Thyristor Rectifiers with On-Load Tap-Changing Transformers

Instead of using bulky and loss making saturable reactor, thyristor based rectifiers can be used to achieve variable voltage by changing the firing angle of the rectifier [1]–[5], [24]–[27]. However, for applications with wide output-voltage variation such as DC arc furnaces, a tap-changing transformer is used in conjunction with the thyristor rectifier in order to limit the range of firing-angle control and to keep the power factor of the circuit above a certain limit (0.9 to 0.95). Apart from DC arc furnaces, thyristor rectifies are also used for copper refining and other chemical electrolysis applications. A circuit diagram of a typical thyristor rectifier system is shown in Fig. 2.9. To cater to the demand for high-power loads, many of these rectifier units are connected in parallel similar to the system shown in Fig. 2.8. The main issue remains mechanical wear and tear of the tap changer, as in the previous case. Apart from that, for applications where only one 12-pulse unit is connected into operation, poor current THD is also an issue. The size of the system reduces as compared to multi-pulse diode rectifier with saturable inductors because of the elimination of the saturable inductors. However, as in the case of previous topology, because of the line frequency transformer, the system still remains very bulky. The power losses in the

saturable reactors are eliminated. The semiconductor conduction losses increases due to higher voltage drop in thyristors as compared to diodes.

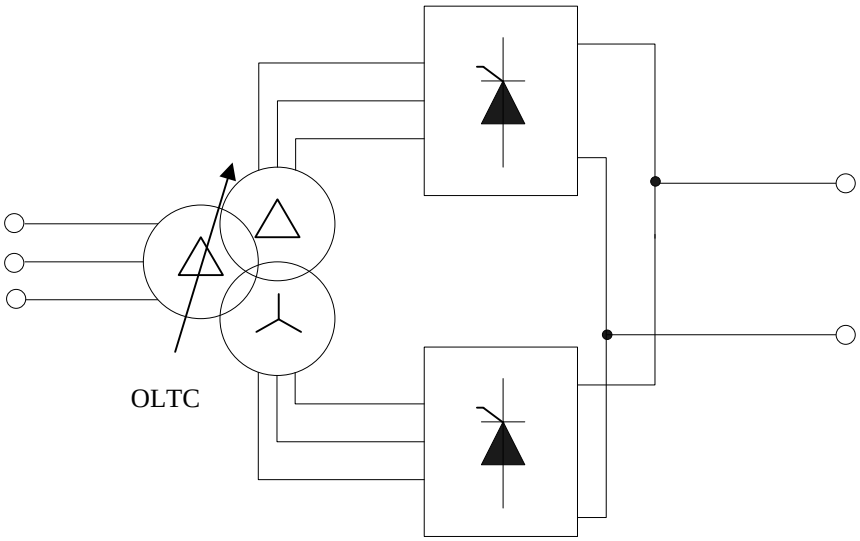


Fig. 2.9 Block diagram of 12-pulse thyristor rectifiers with tap-changing transformers

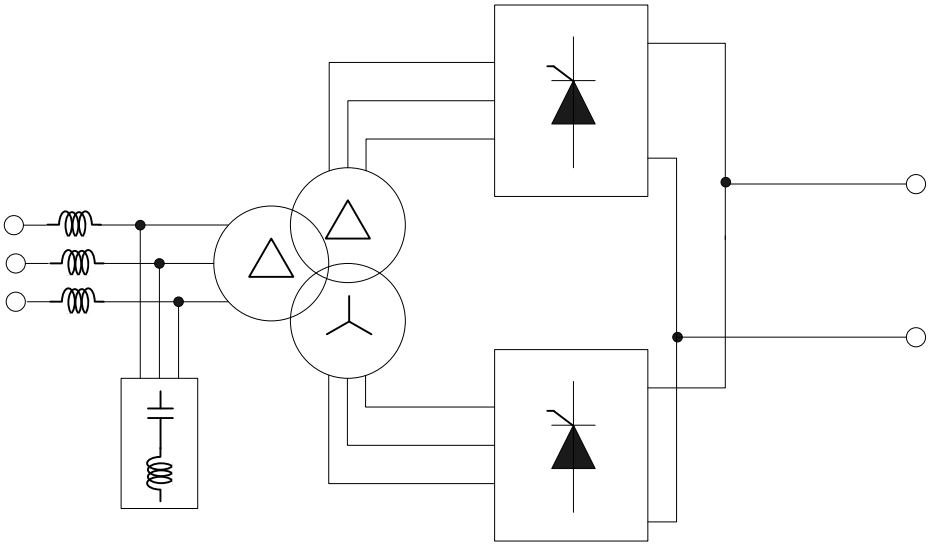


Fig. 2.10 Block diagram of multi-pulse thyristor rectifiers with passive filters

2.3.3 Multi-Pulse Thyristor Rectifiers with/without Passive Filters

For applications with a relatively narrow output-voltage range, the tap-changing transformer can be eliminated and a multi-pulse thyristor rectifier can be used [1]–[5], [24]–[27]. Additionally, because of the commercial non-availability of OLTC at the distribution voltage level, the multi-pulse thyristor rectifiers become the natural choice. Fig. 2.10 shows the basic block diagram of such a 12-pulse rectifier system. The system is widely used for applications

with power rating of a few hundreds of kW to tens of MW. The input voltage can be at distribution level (400V, 440 V, 580 V) for less than 1 MW power rating or medium level (6.6 kV, 10 kV, 33 kV etc.) for multi-MW power rating. However, depending upon the voltage range, change in the firing angle can lead to considerable reactive power burden, poor power factor and poor input current THD. To deal with the reactive power burden and high current THD, passive harmonic filters with considerable reactive power compensation capability are employed. Since passive filters provide only fixed compensation for variable load scenarios it is not possible to keep a very high power factor over the full load range. Therefore, the power factor drops sharply at light load conditions. Moreover, passive filters lead to loss making bulky system with inherent issues of resonance.

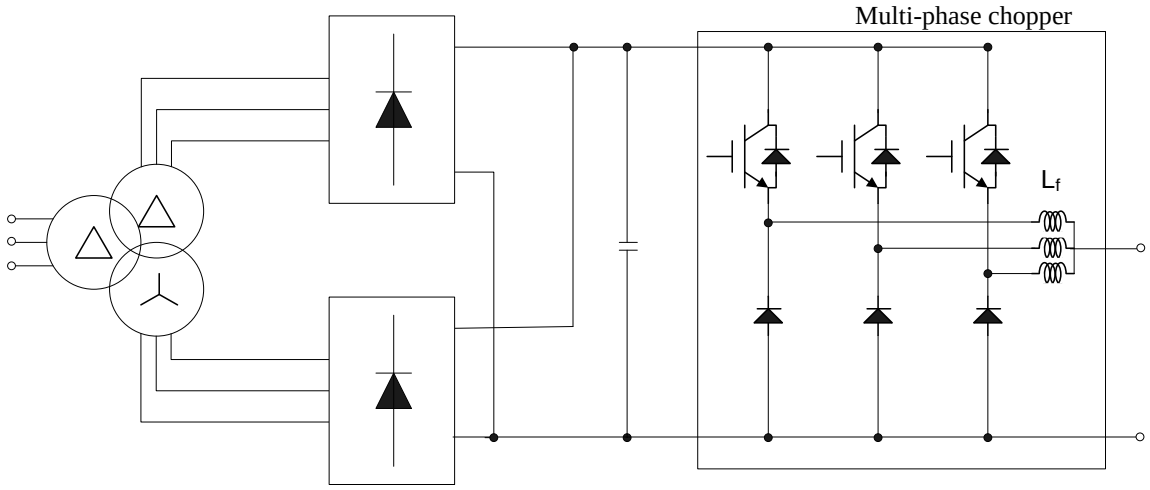


Fig. 2.11 Block diagram of chopper-rectifier with 12-pulse diode rectifier and 3-phase chopper

2.3.4 Chopper-Rectifier

Instead of thyristor rectifiers, multi-pulse diode rectifiers followed by DC-DC chopper are proposed in the literature [1], [2], [4], [5], [28]–[33]. Some companies are producing these units [1]. Fig. 2.11 shows the system configuration of a 12-pulse diode rectifier followed by a three-phase chopper. The chopper-based system provides distinct advantages over the thyristor-based system in terms of transformer size reduction (up to 15-25 %), elimination of the online tap changer, high power factor (0.9-0.96), low input-current harmonics (8-10 %), better control over load current and voltage, lower output-filter requirement and simpler control [1], [30]. In order to improve the THD and power factor further, a dominant-harmonic filter with appropriate reactive power compensation can be added at the input. Chopper-based solutions are used in industry for

electrolysers and plasma-arc generation. The system is put to industrial use up to power rating of tens of MW. However, systems remain bulky because of the line-frequency 12-pulse transformer at the input stage.

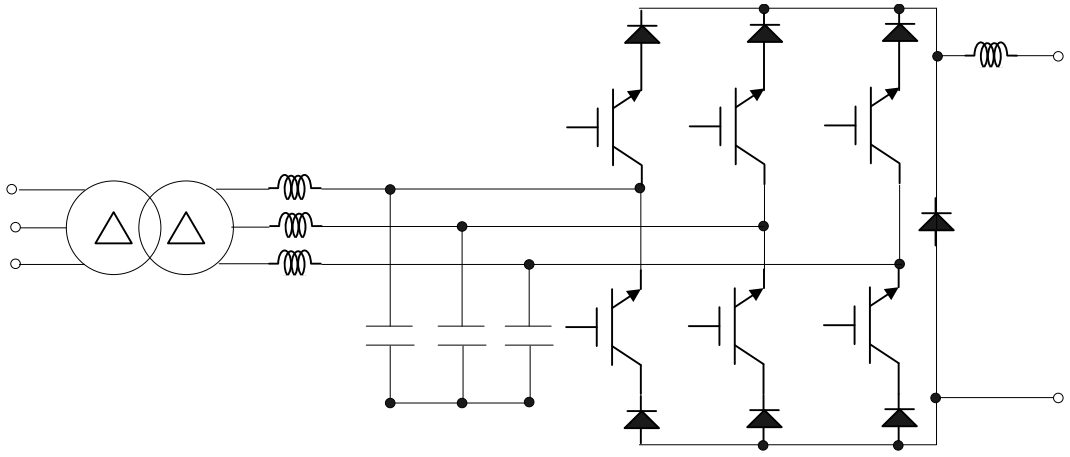


Fig. 2.12 Block diagram of current source rectifier

2.3.5 Current Source Rectifier (Three-Phase PWM Buck Rectifier)

Although not reported to be in the practical use for the aforementioned applications, current source converters are documented in the literature as one of the advanced options that can provide unity power factor operation over a wide load-voltage range with a very good input current THD [1], [2], [34], [35], [43]. Fig. 2.12 shows the circuit diagram of the rectifier. IGBTs in series with diodes or GTO thyristors (Gate turn off) are used as the switching devices. Because of the unavailability of these devices with large current ratings, several devices need to be paralleled. A transformer is still required to step-down the voltage in order to achieve practically suitable duty ratios of the switching devices. A DC inductor is required to reduce the output current ripple and AC-side capacitors are required to filter the input current ripple. The size of the input filter is substantial because of the high magnitude of the input current ripple. As a result of the series connection of the IGBT and diode, conduction losses are expected to be high for high-current applications. Because of these aforementioned reasons, current source rectifiers are not being put to use in high current applications; although, the topology is suitably used for uninterruptible power supply (UPS) applications [35]. For high current applications till ~500 kW, with high output-voltage requirement (e.g. 400 V output DC with 400 V input AC), these rectifiers can prove to be a good option as the input transformer can be eliminated.

However for lower/higher output voltages a line frequency transformer is required, which adds to losses, weight and volume of the rectifier.

2.3.6 Other Reported Circuit Topologies

There are several other circuit configurations proposed in the literature for high-current applications. Reference [36] proposes a series connection of thyristor rectifiers with a by-pass switch on the DC side. Depending on the output-voltage requirement, modules can be inserted or removed using the by-pass switch. However, for high-current applications the rating of the by-pass switch will be impractically high. An optimized sequential-control technique-based high-current rectifier for copper electrowinning is proposed in [37]. The converter comprises two series-connected six-pulse double-star rectifiers, a step-down transformer, and a tuned input filter. Although, a power factor greater than 0.95 can be achieved, the system is too complicated and bulky. Instead of using a standard current-source rectifier configuration, reference [38] proposes a three-phase thyristor rectifier followed by an IGBT switch (or buck converter). The IGBT and thyristors are operated such as to achieve input current wave-shaping. The circuit have limitations because of the active commutation strategy. Hence, appropriate snubber circuits or soft-switching networks are required for application of the converter at a high power level. A completely different approach involving AC-DC-AC-DC conversion stages is proposed by Wiechmann et al. [39]. The system comprises a multi-pulse transformer, a multi-pulse diode rectifier, a multi-level inverter, another multi-pulse transformer and a multi-pulse rectifier. This topology provides good input power quality; however, because of two transformers and multiple power-conversions stages, the bulky system leads to unacceptably high power losses. Reference [40] proposes a multi-cell approach. IGCT-based current-source rectifiers are paralleled at the output DC side, whereas on the input side a multi-pulse approach is used to achieve a sufficient power quality. It is claimed to be able to achieve similar efficiency as a thyristor rectifier with a passive filter. Good reliability and availability are claimed due to the parallel operation of several units. However, the system uses bulky line-frequency transformers. Further, IGCTs are used for the rectification at the low-voltage side; these devices are generally used for high-voltage applications. This leads to a poor utilisation of the semiconductor devices. A high-frequency transformer based approach is discussed recently by Guzman et al. [41], [42]. System consists of a voltage- or current-source rectifier connected to a voltage- or current-source inverter followed

by a transformer and diode rectifier. Three of these units are connected in parallel to achieve higher-power ratings. This configuration exhibits a good input and output power quality. However, as two-level configurations are used at the front-end, the system is only suitable to be connected to the distribution-level grid. This limits the applicability of the circuit to higher input voltage levels. Moreover, no study/comment has been made about the efficiency of the system. Apart from these specific topologies for high current rectification, a number of other (not specifically for high-current applications) multi-level and PWM topologies exist in the literature [43], [44]. Multi-pulse topologies with increased number of pulses provide better harmonic performance, but with no effect on the displacement power factor arising from firing-angle variation. Also, with the increase in the number of pulses, the complexity of the system increases.

2.4 Gaps and Challenges

So far in this chapter, topologies used for HCVV applications are presented. Along with each topology, its advantages and disadvantages have also been highlighted. In this section, major issues with present topologies are consolidated and highlighted. This section indeed forms the motivation to investigate further in the subject.

2.4.1 Power Quality Issues with High-Current Thyristor Rectifies

Many electricity utilities put limits to allowed load power factor. Depending on the utility it can be 0.9, 0.95 or 0.98. There also exist requirements for current harmonics introduced by the equipments. Thyristor rectifiers, connected to distribution-level grid, working without tap-changing transformer, lead to significant amount of the reactive-power demand. This reactive-power is generally compensated with help of passive filters with significant reactive-power compensation capability [45]–[48]. Even with OLTC, at medium-voltage level, passive filters are used to improve the THD of the input current [50]. With the help of the OLTC, the power factor of thyristor rectifiers can be kept high by limiting the variation of the firing-angle; however, OLTC introduces mechanical wear and tear issues. Moreover, for rectifiers connected to the distribution-level grid, it is not feasible to use OLTC. In these kinds of systems, a single 12-pulse thyristor rectifier with passive filters is employed. Aspects of the passive filter design are dealt in IEEE standard 1531 [51] and other publications [52]. As already discussed, a passive filter fails to keep the power factor high enough for the entire operating range because of the

fixed nature of compensation. Moreover, passive filters increase losses, weight and volume. For six-pulse thyristor rectifiers (that are widely used in low-power applications), even multiple passive filters (5^{th}, 7^{th} and 11^{th} etc.), cannot provide good current THD over the entire range of operation. To deal with a variable reactive-power demand, the use of thyristor-based static VAR compensators is proposed; however, these systems lead to current harmonics [18], [53]. Although not specifically for high-current applications, active filters or STATCOMs (static compensators) or DSTATCOMs (distribution static compensators) are proposed for variable reactive-power compensation [54], [56]. Additionally, these units can provide compensation to harmonics and unbalance currents. A STATCOM consists of a voltage source converter (VSC) with a capacitor connected at the DC link. The VSC is connected to the point of common coupling through three-phase filter inductors. The VSC is controlled such that compensating fundamental-frequency reactive and harmonic-frequency currents are generated as desired. However, a STATCOM is an expensive option and introduces extra losses to the system too. In order to reduce the capital cost, several hybrid combinations of STATCOM and passive filters are proposed [57]–[63]. However, most of these combinations mainly target diode rectifiers with a DC side capacitive filter (low reactive-power and high amount current harmonics) as a load to be compensated [57]–[61]. Conversely, a parallel combination of a passive and an active filter is suitably proposed for thyristor converter that can be taken for further study [62], [63].

2.4.2 Weight, Volume and Capital Cost

Line-frequency magnetics, DC inductors and AC/DC capacitors are the major contributors to the weight and volume of the discussed topologies. Multi-pulse rectifiers invariably need a bulky line-frequency transformer. Passive filters with considerable high reactive-power rating need huge AC capacitors. Additionally, according to the current- and voltage-ripple specifications, the DC-side, too, needs bulky capacitors and inductors. The size of the equipment affect the capital cost in two ways: 1. large foot print of the equipment means bigger space requirement on the premises and thus higher real-state cost, 2. if we study the break-up of the cost of different components in this type of rectifiers, cost of magnetics and capacitors comes out to be largest contributor. Apart from these, transportation and installation cost also increases with size of the equipment. Size of these components can be reduced by decreasing the rating of components

and/or increasing the frequency of operation. Both of these approaches are utilised in the course of present investigation.

2.4.3 Modularity

Most of the topologies used in industry have proven reliability. Therefore, any new proposed solution should also have the matching reliability. Accuracy of estimation of the reliability is severely limited at the development stage of the topology. To establish the reliability, most accurate methods involve the continuous load cycling of the product in harsh conditions. This requires a considerable amount of time and effort and is not in the scope of the present work. However, obvious failure modes can be avoided at the conceptual and design stage. Moreover, learning from other high-power applications (with proven reliability) can be used to develop the robust solutions.

Inferior reliability affects the running cost of the system. Not only cost of repair but also loss of revenue due to down time need to be considered. But even with high reliability, failures do happen. Cost, time and efforts required to replace the huge components are significant. Therefore, modularity is a desired feature in high power systems. Modularity leads to easy and cost effective replacement of damaged components. Besides, it also reduces capital cost of manufacturing due to ease of assembling and transportation. This is one of the features missing in existing topologies, which needs to be considered for advanced solutions.

2.5 Summary

In this chapter, main topologies used for high-current applications have been discussed. The advantages and disadvantages of each topology have been highlighted. Gaps in the technologies are discussed that form the points for further action. Major areas of improvement are power quality, size and modularity.

3. Voltage Sequence-Control-Based Rectifier with Passive Filter

Although thyristor- or diode-based rectifiers have issues with power quality, these rectifiers cannot be written-off completely due to their high reliability, efficiency and widespread use. As discussed in the previous chapter, because of poor power factor of these types of rectifiers, passive filters are used [1], [2], [49]–[52]. There are two major issues with these types of systems, (a) with varying load, fixed reactive power compensation fails to keep a high power factor over a large operating range (b) the required reactive power rating of passive filter is fairly high. Because of using a large passive filter, the losses in passive filter also are at high level. In order to deal with this issue for very large power, medium-voltage applications, rectifier transformer with several taps along with a mechanical tap-changer is used [1], [2]. The main issues with this system are mechanical wear and tear and large footprint. Moreover, customized for medium-voltage applications, commercial availability of mechanical tap-changers for distribution-voltage-level application is severely limited. Instead, for distribution voltage-level applications both discrete and sequence-controlled thyristor based tap-changing transformers are discussed in the literature [15], [18], [65], [66].

In this chapter, a combination of voltage sequence-controlled thyristor-based tap-changing transformer followed by a diode rectifier is discussed to enhance the range of operation with high power factor and minimize the rating of reactive power compensation [G]. The circuit, as shown in Fig. 3.1 consists of back to back connected thyristors operating in voltage sequence-control mode to achieve a variable AC voltage at the secondary side of the transformer. A three-phase diode rectifier is connected at the secondary to achieve AC to DC conversion. The circuit provides specific advantages for high-current applications in terms of reducing the rating of passive filter and increasing the range of high power factor operation. Moreover, for high-current low-voltage applications (high primary to secondary transformer turns ratio) the circuit leads to an efficiency improvement as conduction losses of a diode rectifier is lower than a thyristor rectifier. The range of operation and required rating of the passive filter are closely linked to the tapping provided at the primary of the transformer. A study is carried out to find an optimum value of n_1/n_2 ratio so as:

(1) to achieve a specified power factor with minimum reactive power compensation and
(2) to maintain the specified power factor for a broadest possible load voltage range.

The optimization is carried out for different values of power factors i.e. 0.9, 0.95 and 0.97. Based on the findings design guidelines are formed. Finally the system is implemented at 62.5 kW (load voltage 25 V and load current 2500 A) level to verify the system performance.

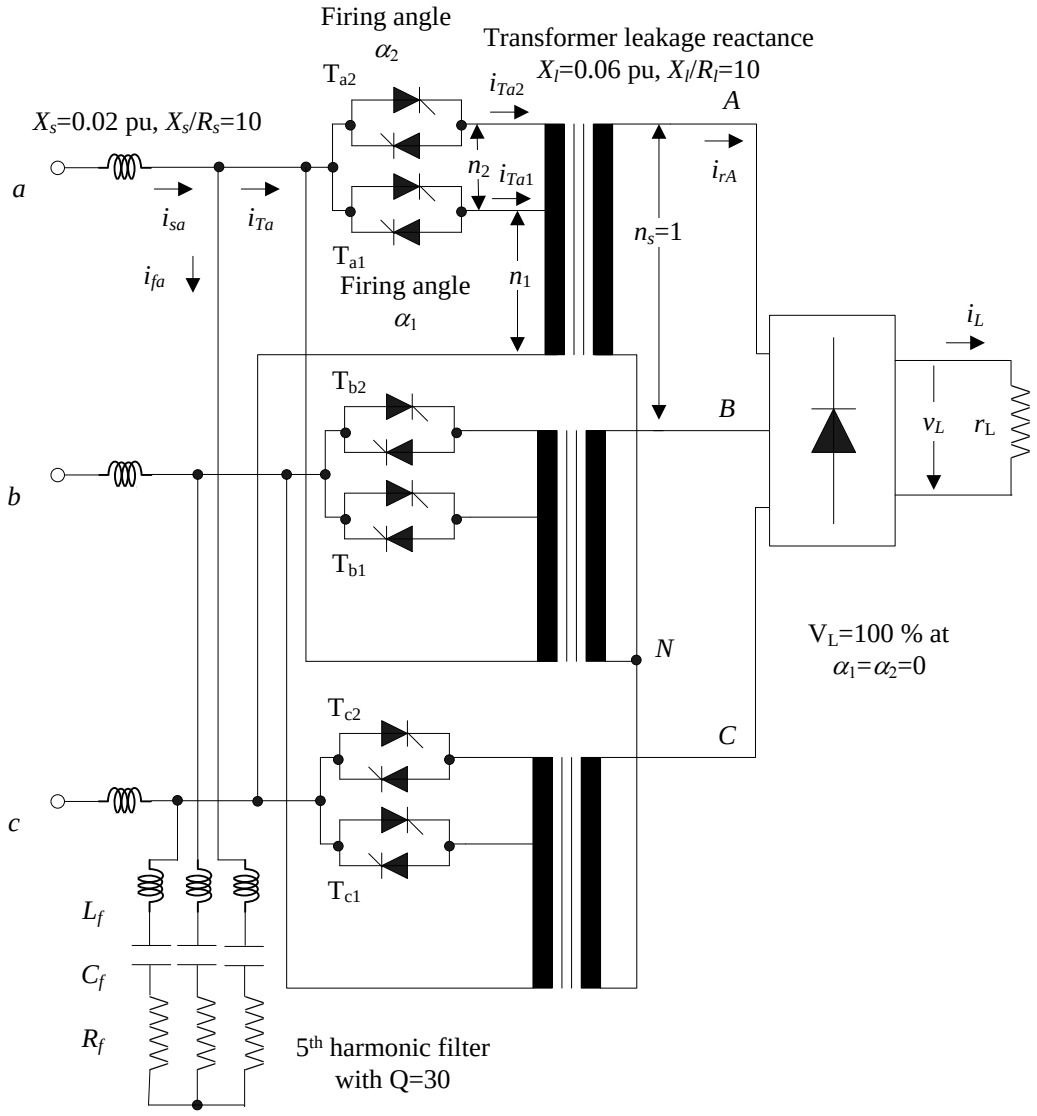


Fig. 3.1 Circuit diagram of rectifier system with dominant-harmonic passive filter.

3.1 System Description and Working Principle

The rectifier system as shown in Fig. 3.1 consists of a thyristor-based sequential tap changer followed by a three-phase diode rectifier. The transformer primary windings are connected in

delta and secondary in star arrangement. A star connection on the primary side will require neutral to be connected, which is not always available. Without neutral connection to the star point of the transformer, its voltage potential will oscillate severely due to thyristors switching, therefore this connection is avoided. A delta connection on the secondary side leads to a much higher reactive power demand. Therefore a delta-star configuration is selected. A filter is employed at the input side to compensate for the reactive power and dominant-harmonic current.

There are two modes of operation of this circuit. During mode 1, the firing angle α_2 is kept at zero and only firing angle α_1 is varied (see Fig. 3.1 for the definition of α_1 and α_2). During mode 2 firing angle α_1 is kept at 180° (or thyristors not gated) and firing angle α_2 is varied. Fig. 3.2 shows the variation of secondary side phase voltage during modes 1 and 2 for a single-phase system for simplifying the understanding. The output DC voltage varies according to the variation of the diode rectifier input AC voltage variation. At the starting points of modes 1 and 2 the applied voltage to the rectifier remains purely sinusoidal and therefore leads to a high displacement power factor.

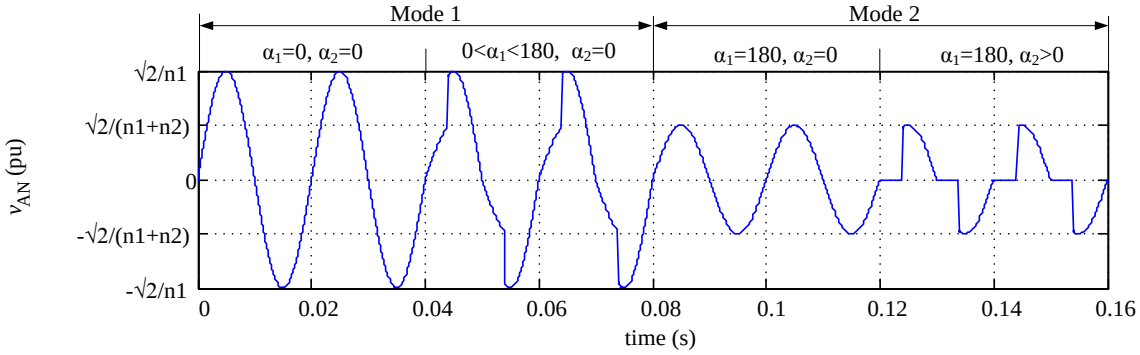
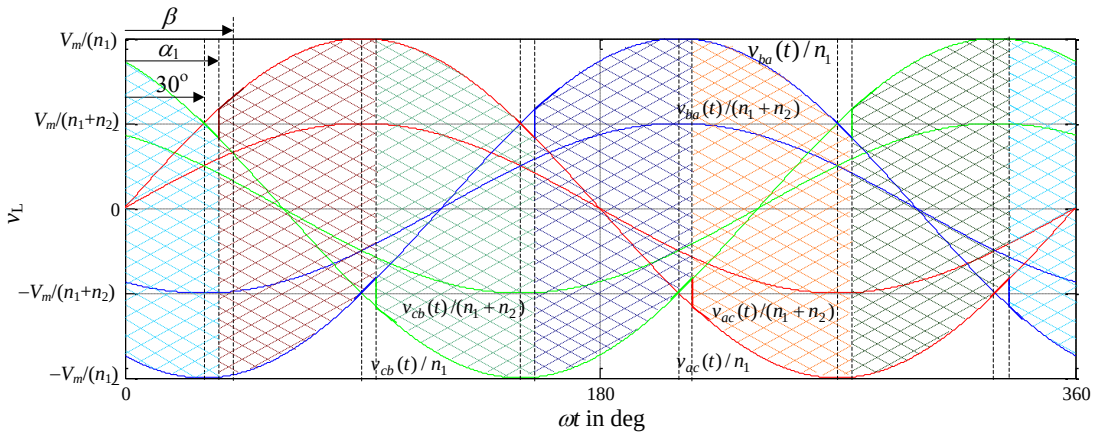
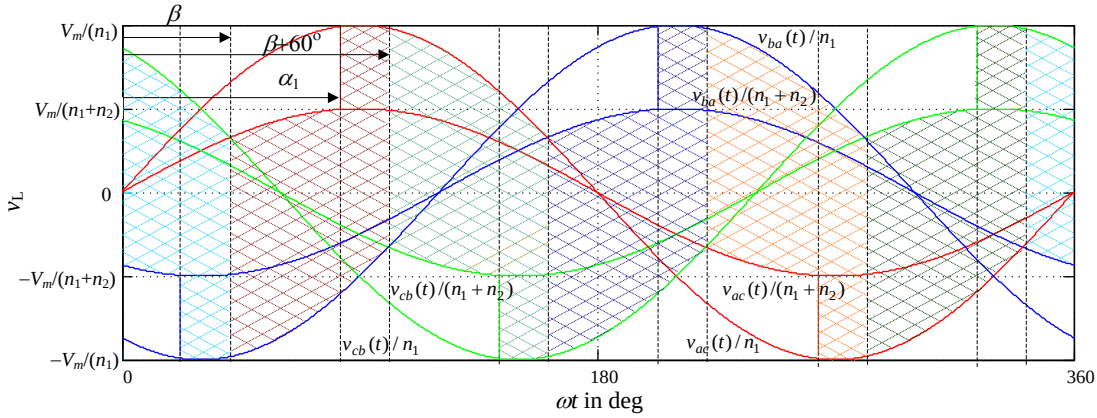


Fig. 3.2 Waveform of the secondary side phase voltage under different modes of operations.

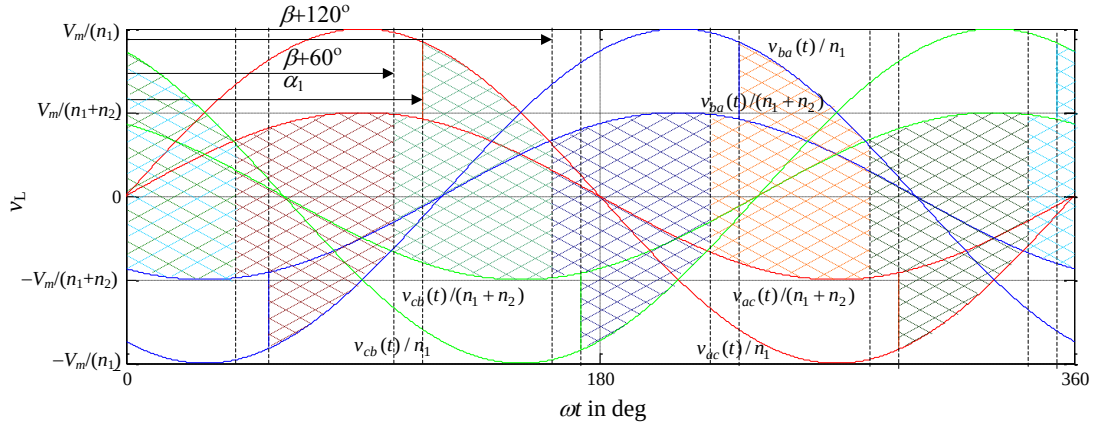
The operation of the three-phase system with diode rectifier as a load is shown in Fig. 3.3 (a)-(d). The DC voltage is constructed with the help of three-phase AC voltages for different ranges of firing angles under mode 1. As it can be seen from the circuit diagram the input line-to-line voltage appears as phase voltage on the secondary side (with appropriate voltage scaling due to transformer turns ratio). The voltage appearing across the load is shown as checkered lines. As the different AC voltages appear on the DC load side, color of the checkered lines changes.


β
α1
30°
Vm/(n1)
Vm/(n1+n2)
0
−Vm/(n1+n2)
−Vm/(n1)
vL
vba(t)/n1
vba(t)/(n1+n2)
vcb(t)/(n1+n2)
vac(t)/(n1+n2)
vcb(t)/n1
vac(t)/n1
0
180
360
ωt in deg

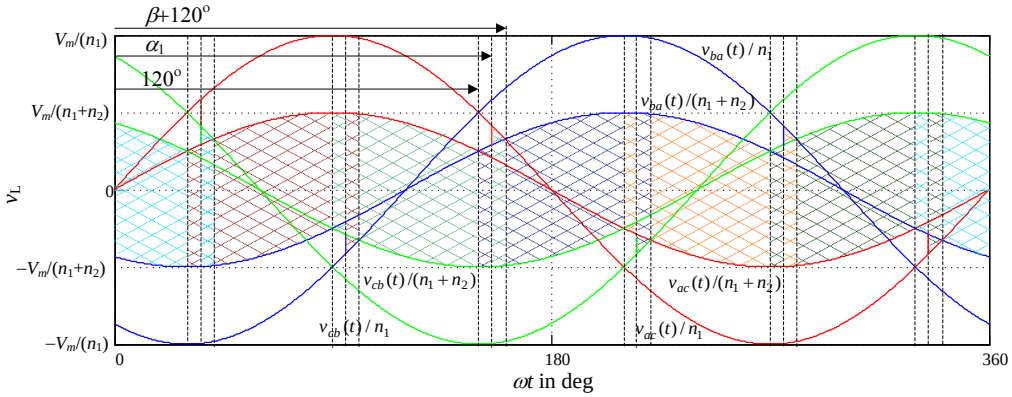
(a)


β
β+60°
α1
Vm/(n1)
Vm/(n1+n2)
0
−Vm/(n1+n2)
−Vm/(n1)
vL
vba(t)/n1
vba(t)/(n1+n2)
vcb(t)/(n1+n2)
vac(t)/(n1+n2)
vcb(t)/n1
vac(t)/n1
0
180
360
ωt in deg

(b)


β+120°
β+60°
α1
Vm/(n1)
Vm/(n1+n2)
0
−Vm/(n1+n2)
−Vm/(n1)
vL
vba(t)/n1
vba(t)/(n1+n2)
vcb(t)/(n1+n2)
vac(t)/(n1+n2)
vcb(t)/n1
vac(t)/n1
0
180
360
ωt in deg

(c)



(d)

Fig. 3.3 Output DC voltage for different values of firing angles under mode 1 (a) 30°≤ α_1≤ β (b) β≤ α_1≤ β+60° (c) β+60°≤ α_1≤ 120° and (d) 120°≤ α_1≤ β+120°.

The input AC line-to-line voltages are defined as:

$$v_{ac}(t) = V_m \sin(\omega t) \tag{3.1}$$

$$v_{ba}(t) = V_m \sin(\omega t - 120°) \tag{3.2}$$

$$v_{cb}(t) = V_m \sin(\omega t - 240°) \tag{3.3}$$

where V_m is the peak line-to-line voltage and ω is the angular frequency. Depending on the value of firing angle α_1 the operation can be divided into four zones i.e. (a) 30° ≤ α_1 ≤ β, (b) β ≤ α_1 ≤ β+60°, (c) β+60° ≤ α_1 ≤ 120° and (d) 120° ≤ α_1 ≤ β+120°. Where β is the extinction angle, defined as the instance when higher tapping voltage of incoming phase is equal to the lower tapping voltage of outgoing phase and given as:

$$\beta = \tan^{-1}\left\{\frac{\sqrt{3}(n_1 + n_2)}{(3n_1 + n_2)}\right\} \tag{3.4}$$

In usual three-phase B6C thyristor converter this angle is 30°. The first zone of operation is defined as when firing the angle is between 30° and β. This is a relatively short zone of operation when the secondary voltage of the transformer is nearly sinusoidal and the displacement power factor remains very high. Fig. 3.3 (a) depicts this zone of operation (for 30°≤ α_1≤ β). The DC load voltage in this zone results as:

$$v_L(t)=\begin{cases}\dfrac{v_{cb}(t)}{n_1}-\dfrac{v_{ba}(t)}{n_1} \text{ for } 30^\circ \le \omega t < \alpha_1 \\ \dfrac{v_{ac}(t)}{n_1}-\dfrac{v_{ba}(t)}{n_1} \text{ for } \alpha_1 \le \omega t < \alpha_1 + 60^\circ \\ \dfrac{v_{ac}(t)}{n_1}-\dfrac{v_{cb}(t)}{n_1} \text{ for } \alpha_1 + 60^\circ \le \omega t < 120^\circ \end{cases} \tag{3.5}$$

The next two zones cover relatively broad ranges of firing angles. The load voltage waveforms are depicted in Fig. 3.3 (b) and (c). For the zone b, the output voltage results as:

$$v_L(t)=\begin{cases}\dfrac{v_{ac}(t)}{n_1+n_2}-\dfrac{v_{ba}(t)}{n_1} \text{ for } \beta \le \omega t < \alpha_1 \\ \dfrac{v_{ac}(t)}{n_1}-\dfrac{v_{ba}(t)}{n_1} \text{ for } \alpha_1 \le \omega t < \beta + 60^\circ \\ \dfrac{v_{ac}(t)}{n_1}-\dfrac{v_{cb}(t)}{n_1+n_2} \text{ for } \beta + 60^\circ \le \omega t < \alpha_1 + 60^\circ \\ \dfrac{v_{ac}(t)}{n_1}-\dfrac{v_{cb}(t)}{n_1} \text{ for } \alpha_1 + 60^\circ \le \omega t < \beta + 120^\circ \end{cases} \tag{3.6}$$

and for the zone c as:

$$v_L(t)=\begin{cases}\dfrac{v_{ac}(t)}{n_1+n_2}-\dfrac{v_{ba}(t)}{n_1+n_2} \text{ for } \beta \le \omega t < \alpha_1 - 60^\circ \\ \dfrac{v_{ac}(t)}{n_1+n_2}-\dfrac{v_{ba}(t)}{n_1} \text{ for } \alpha_1 - 60^\circ \le \omega t < \beta + 60^\circ \\ \dfrac{v_{ac}(t)}{n_1+n_2}-\dfrac{v_{cb}(t)}{n_1+n_2} \text{ for } \beta + 60^\circ \le \omega t < \alpha_1 \\ \dfrac{v_{ac}(t)}{n_1}-\dfrac{v_{cb}(t)}{n_1+n_2} \text{ for } \alpha_1 \le \omega t < \beta + 120^\circ \end{cases} \tag{3.7}$$

Similar to zone a, zone d is relatively short as compared to zones b and c. The displacement power factor is relatively high due to nearly sinusoidal voltage waveforms at the secondary side of the transformer. The waveform is shown in Fig. 3.3 (d) and the load voltage is given as:

$$v_L(t)=\begin{cases}\dfrac{v_{ac}(t)}{n_1+n_2}-\dfrac{v_{ba}(t)}{n_1+n_2} & \text{for } \beta \le \omega t < 60^\circ \\ \dfrac{v_{ac}(t)}{n_1+n_2}-\dfrac{v_{cb}(t)}{n_1+n_2} & \text{for } 60^\circ \le \omega t < \alpha_1 - 60^\circ \\ \dfrac{v_{ac}(t)}{n_1+n_2}-\dfrac{v_{ba}(t)}{n_1} & \text{for } \alpha_1 - 60^\circ \le \omega t < \beta + 60^\circ \\ \dfrac{v_{ac}(t)}{n_1+n_2}-\dfrac{v_{cb}(t)}{n_1+n_2} & \text{for } \beta + 60^\circ \le \omega t < 120^\circ \\ \dfrac{v_{ba}(t)}{n_1+n_2}-\dfrac{v_{cb}(t)}{n_1+n_2} & \text{for } 120^\circ \le \omega t < \alpha_1 \\ \dfrac{v_{ac}(t)}{n_1}-\dfrac{v_{cb}(t)}{n_1+n_2} & \text{for } \alpha_1 \le \omega t < \beta + 120^\circ \end{cases} \tag{3.8}$$

In mode 2 firing angle α_1 is kept at 180° (or thyristors not gated) and firing angle α_2 is varied. This mode of operation is very similar to standard three-phase thyristor rectifier and therefore not elaborated further.

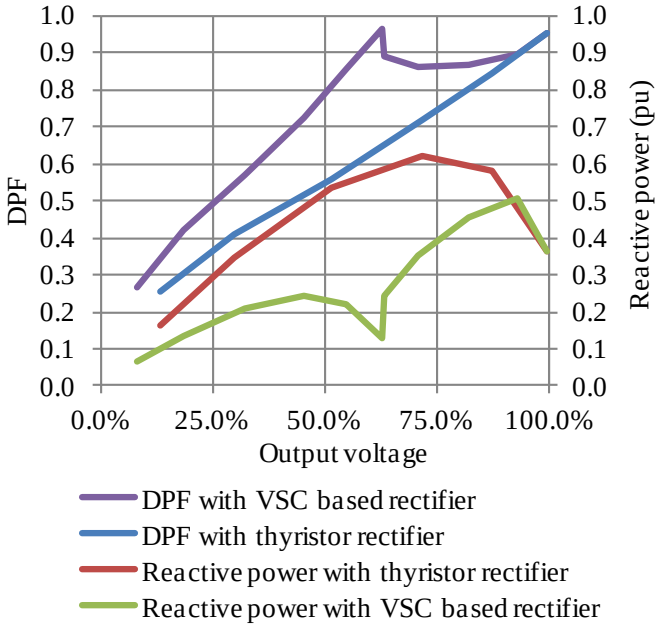


Fig. 3.4 Variation of power factor and reactive power for thyristor converter and voltage-sequence-control-based rectifier.

With the resistive load and voltage waveforms discussed under mode 1, it can be inferred that input displacement power factor (DPF) first decreases and then increases during mode 1 with the increase in firing angle α_1. Moreover, the distortion in transformer secondary voltage also increases with increase in firing angle initially and then reduces as the firing angle approaches to

zone d. Under mode 2 DPF decreases monotonically as α_2 is increased. To analyze the circuit behavior further a generalized system is considered and specifications (in per unit) are provided in Table 3.1. The input line-to-line voltage (root mean square value) is taken as base voltage and rated output power (at maximum output DC voltage with α_1=0 and α_2=0) is taken as base power. Since per unit values of the input/output voltage are used, analysis can easily be generalized for any other system rating.

Variation of displacement power factor (DPF) and reactive power is shown in Fig. 3.4 with respect to the output voltage with n_2/n_1=0.6. This Fig. also shows variation of these quantities for a standard 3-phase 6-pulse B6C thyristor rectifier feeding the same load. Clearly, the reactive power demand comes out to be much smaller for a voltage sequence-control-based rectifier than a B6C thyristor rectifier. Also the DPF remains fairly high for a large voltage range for a voltage sequence-control-based rectifier as compared to B6C thyristor rectifier.

Table 3.1 System specifications

Input voltage	1.0 pu
Maximum output power	1.0 pu
Output voltage	0-100 %
Load type	Resistive
Input inductance	0.02 pu X_s/R_s=10
Transformer	turns ratios n_1:1 and n_1+n_2:1, leakage: 0.06 pu X_l/R_l=10

3.2 Transformer Turns Ratio Optimization

For a voltage sequence-control-based rectifier, the reactive power demand and its variation depends on the ratio of the transformer tap settings (n_2/n_1). Fig. 3.5 shows the variation of reactive power over the voltage range for different values of n_2/n_1 ratios. It can be observed, as the n_2/n_1 ratio is increased from zero (B6C thyristor rectifier) the peak reactive power demand reduces considerably. Moreover, the difference of maximum to minimum reactive power also reduces considerably. This is a favorable aspect in designing a fixed reactive power compensation device like passive filter. Designing a passive filter has two aspects, (1) specified power factor and (2) load range for which the specified power factor has to be maintained. There is generally a tradeoff between these two requirements. The objective here is to find out a value of ratio n_2/n_1 so as:

1. the specified PF can be achieved with minimum passive filter reactive power rating.

2. the combination of turns ratio and passive filer rating should also maintain the specified power factor for the widest load range. In this case the load range means output voltage range.

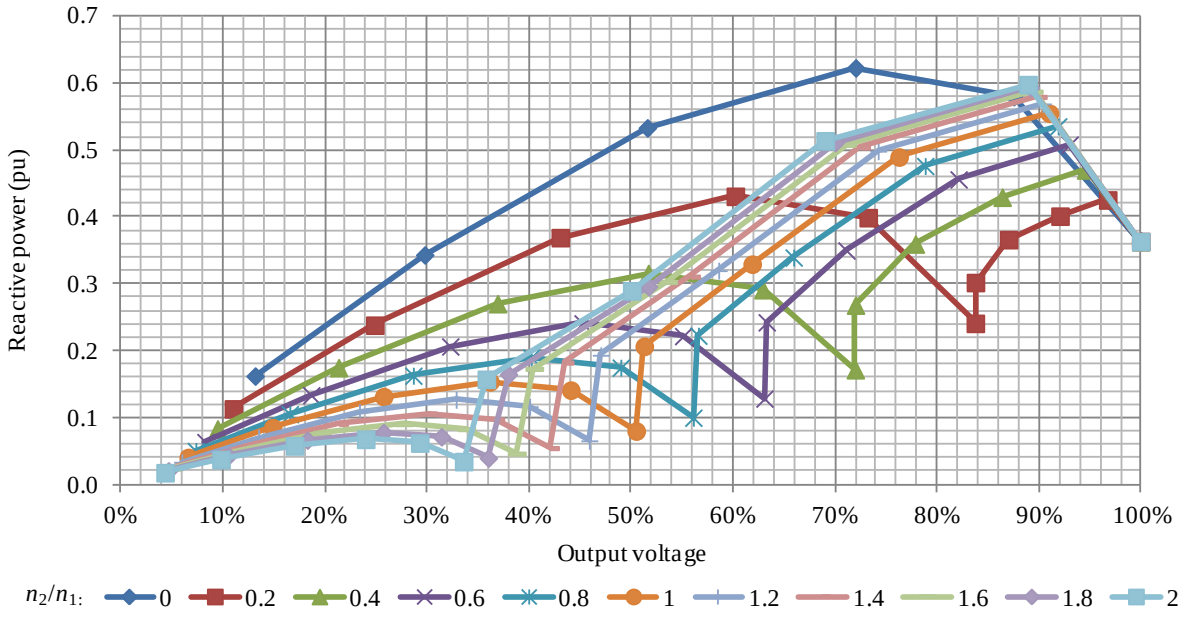


Fig. 3.5 Variation of reactive power of voltage sequence-control-based rectifier for different n_2/n_1 ratios.

To find out the optimum n_2/n_1 ratio, a generalised three-phase six-pulse voltage sequence-control-based rectifier feeding a resistive load with a dominant-harmonic filter is taken into consideration. The following steps are pursued to optimize the system:

1. Through simulation of a voltage sequence-control-based rectifier (without passive filter), variation of reactive power is estimated against the output voltage for different values of n_2/n_1

2. Minimum reactive power compensation, required to achieve DPF greater than 0.9, is established for each n_2/n_1 ratio (a sufficient margin is kept in DPF to achieve PF greater than 0.9 as DF is always less than unity)

3. Simulation of voltage sequence-control-based rectifier with dominant-harmonic passive filter (rating identified in the previous step) is carried out for crosschecking actual PF variation for each n_2/n_1 ratio. Load voltage range is plotted for which the power factor is greater than 0.9.

Fig. 3.5 shows the variation of reactive power for various values of the n_2/n_1 ratio. Fig. 3.6 shows the required rating of passive filters to keep the DPF greater than 0.9 for each case. Fig. 3.7 shows the minimum possible output voltage, till which PF is greater than 0.9, for various

values of transformer turns ratio. It is observed that PF greater than 0.9 can be achieved for n_2/n_1=0.6 with minimum passive filter rating for maximum possible output voltage range. A considerable reduction from 0.42 pu to 0.17 pu in required reactive power compensation is observed for n_2=0 to n_2/n_1=0.6. It can also be observed that the required reactive power rating is comparable for n_2/n_1=0.6 to 1.0; however, n_2/n_1=0.6 provides the widest output voltage range with PF greater than 0.9. It can be noted from Fig. 3.6 and Fig. 3.7 that unlike the required reactive power compensation, the voltage range does not follow a regular pattern with respect to n_2/n_1 ratio. This is because required reactive power compensation depends on the peak reactive power demand and difference of maximum to minimum reactive power. Whereas, the voltage range (with PF greater than a certain value) depends on the variation of reactive power demand over the load voltage under different modes, which is non-linear as depicted in Fig. 3.5.

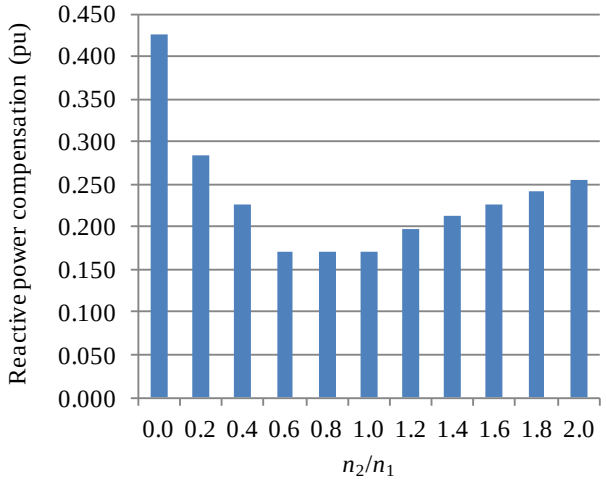


Fig. 3.6 The required rating of passive filters for different n_2/n_1 ratios.

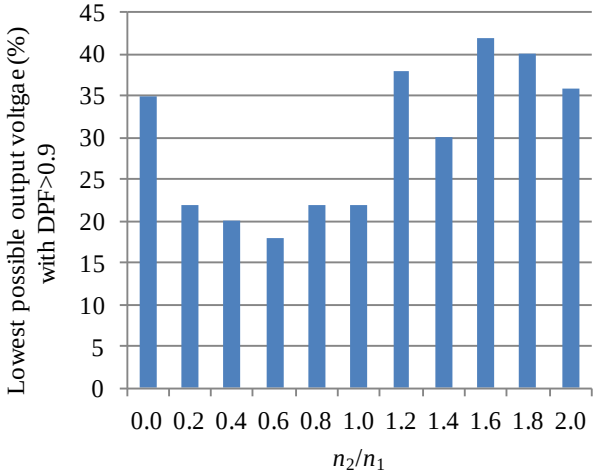


Fig. 3.7 Minimum output voltage with DPF greater than 0.9 for different n_2/n_1 ratios.

Similarly, this investigation can be repeated for different values of required power factor such as 0.95 and 0.97. The optimum n_2/n_1 ratio can be determined with minimum reactive power rating of the passive filter. Table 3.2 illustrates the optimised n_2/n_1 ratio, passive filter rating and voltage range with PF higher than a certain value, which forms the design guidelines.

Table 3.2 Optimised turn ratios and passive filter ratings for different power factor values

	PF> 0.97	PF> 0.95	PF> 0.9
Optimised turn ratio	n_2/n_1=0.4	n_2/n_1=0.6	n_2/n_1=0.6
Passive filter rating	0.27 pu	0.23 pu	0.17 pu
Voltage range	100-57 %	100-40 %	100-35 %

3.3 Experimental Results

To verify the design procedure an industrial power supply is build for 62.5 kW (25 V and 2500 A) load. Input mains voltage and frequency are 400 V ± 5 %, 50 Hz. The minimum specified power factor over the widest possible load range is 0.95. As per the design, transformer turns ratios are n_1/n_s=17 and n_2/n_s=10 (rated primary voltage: 400 V, on-load secondary voltages: 14.81 V and 23.53 V). The actual transformer short circuit impedance is 7.05 %. The total transformer losses at full load are 2100 W (with sinusoidal currents). A fifth harmonic filter (tuned at 4.7×50 Hz) is used to improve the displacement power factor and current THD. Resulting from the requirement, the reactive power rating of passive filter should be 0.23 pu (please refer to Table 3.2). However, a slightly higher rating 0.28 pu (C_f=332 µF and L_f=1380 µH) of the filter is selected because of commercial/stock availability of the capacitors. The buffer inductor value is 325.95 µH. Infineon thyristors TT-Module 180N16KOF and diodes D5810N04T are used to assemble the circuit.

Under mode 1 and 2 of operations, Fig. 3.8-3.12 and Fig. 3.13-3.16, respectively show recorded waveforms of the circuit with a grid voltage of 384 V, 50 Hz and a resistive load of 25/2200 Ω (circuit is designed for 400 V rated voltage and 25/2500 Ω; however, abovementioned conditions prevailed at the time of recording of waveforms). Mains voltage has THD of 1.8 % due to the presence of 5th and 7th harmonics. Fig. 3.8 shows the recorded waveforms of input line-to-line voltage v_{ab}, phase-*a* input current i_{sa}, passive filter current i_{fa} and system current i_{Ta} at 25 V output load voltage and 2200 A current. An improvement in the wave-shape of the source side current as compared to the system current is clearly evident. The secondary side voltage v_{AB}, and load voltage v_L is shown in Fig. 3.9 along with input voltage and

current. It is important to observe the secondary side AC voltage wave-shape due to the diode switching (therefore the thyristor turns off due to the current falls below the holding current). Currents flowing through thyristors along with input voltage and rectifier current are shown in Fig. 3.10. Recorded power measurements shown in Fig. 3.11 (a) and (b) show the improvement in the power factor (0.84 to 0.95) due to the use of passive filter. Improvement in the input current THD is shown in Fig. 3.12 (a) and (b) from 19.2 % to 9.1 %.

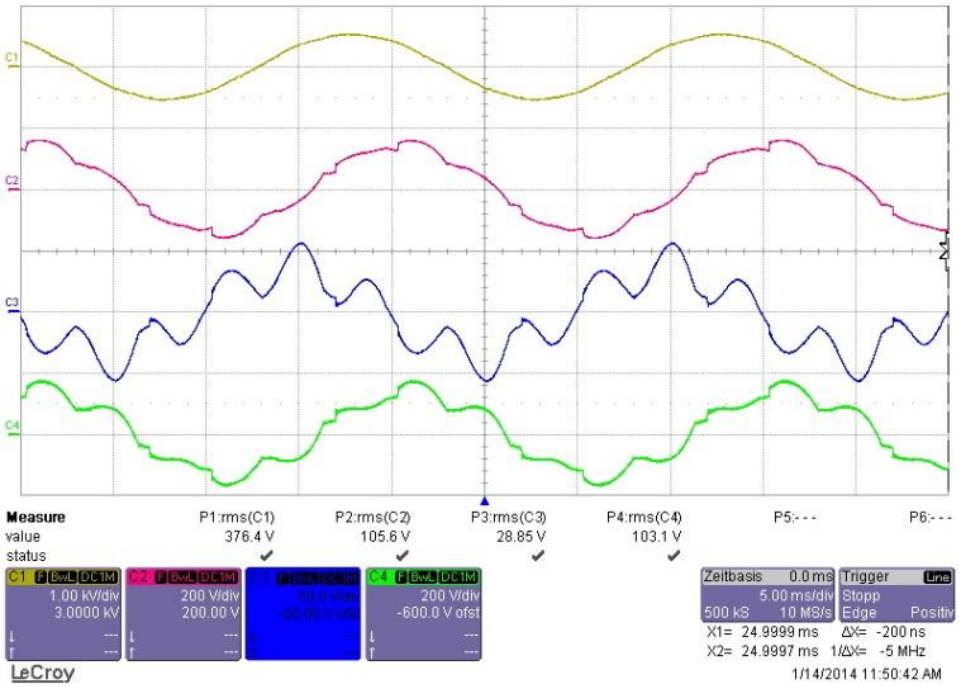


Fig. 3.8 Waveform at mode 1, showing, Ch 1 (yellow): input line-to-line voltage v_{ab} (1 kV/div), Ch 2 (red): input current i_{sa} (200 A/div), Ch 3 (blue): passive filter current i_{fa} (50 A/div) and Ch 4 (green): system current i_{Ta} (200 A/div). Time scale: 5 ms/div.

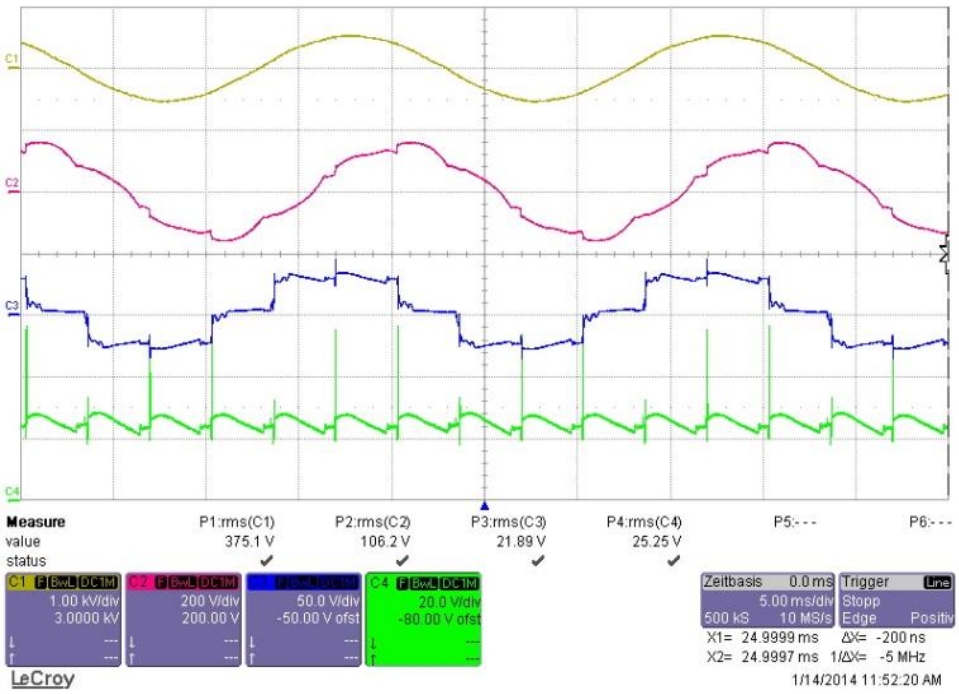


Fig. 3.9 Waveform at mode 1, showing, Ch 1 (yellow): input line-to-line voltage v_{ab} (1 kV/div), Ch 2 (red): input current i_{sa} (200 A/div), Ch 3 (blue): transformer secondary line-to-line voltage v_{AC} (50 V/div) and Ch 4 (green): load voltage v_L (20 V/div). Time scale: 5 ms/div.

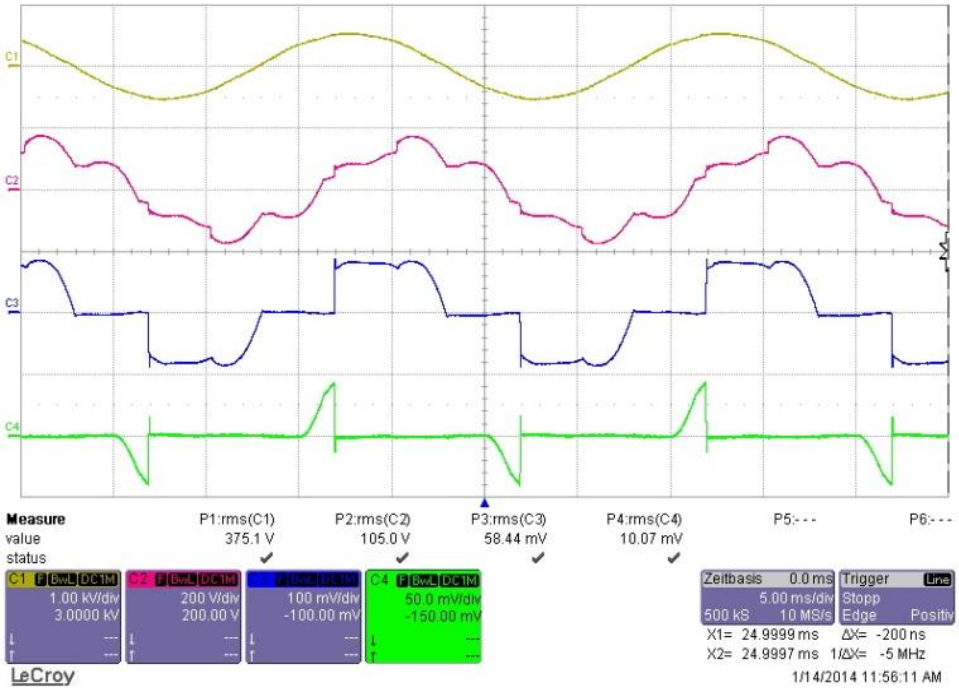
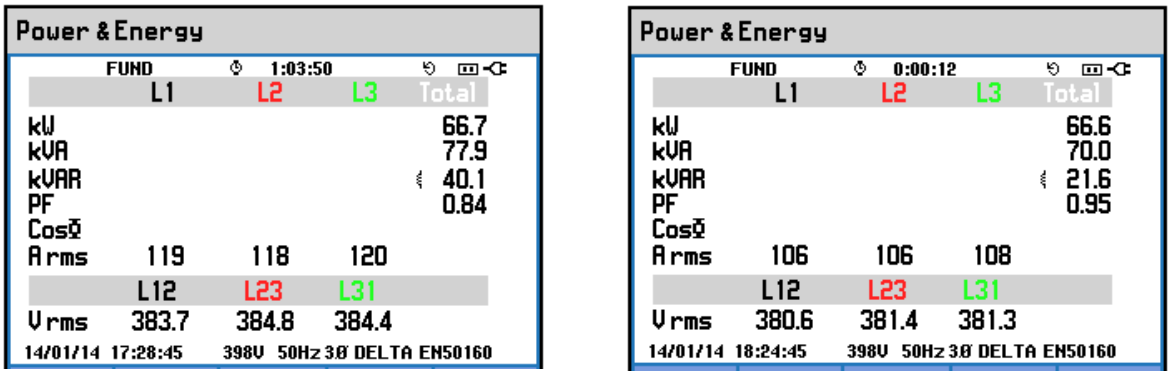
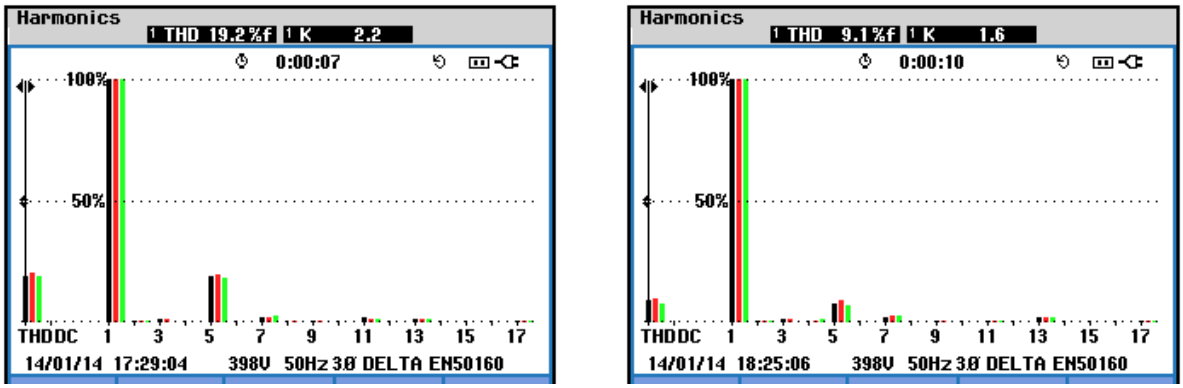


Fig. 3.10 Waveform at mode 1, showing, Ch 1 (yellow): input line-to-line voltage v_{ab} (1 kV/div), Ch 2 (red): system current i_{Ta} (200 A/div), Ch 3 (blue): thyristor T_{a1} current i_{Ta1} (100 A/div) and Ch 4 (green): thyristor T_{a2} current i_{Ta2} (50 A/div). Time scale: 5 ms/div.



(a) (b)

Fig. 3.11 Input voltage, current, active, apparent and reactive power and power factor measurements under mode 1 (a) without passive filter and (b) with passive filter.



(a) (b)

Fig. 3.12 Input current THD (a) without passive filter and (b) with passive filter.

Operation of the circuit under mode 2 is depicted in Fig. 3.13, which shows the source side, passive filter and circuit side currents at 15.7 V output load voltage and 1400 A current. Fig. 3.14 shows the thyristor currents (channel 3 and 4), as expected: the current is flowing only through thyristors T_{a2}. The transformer secondary voltage and current are shown in Fig. 3.15. Input current THD and power factor are depicted in Fig. 3.16 (a) and (b). It can be seen that at power level of 29 kW, the power factor is at 0.99 with a current THD of 12.7 %.

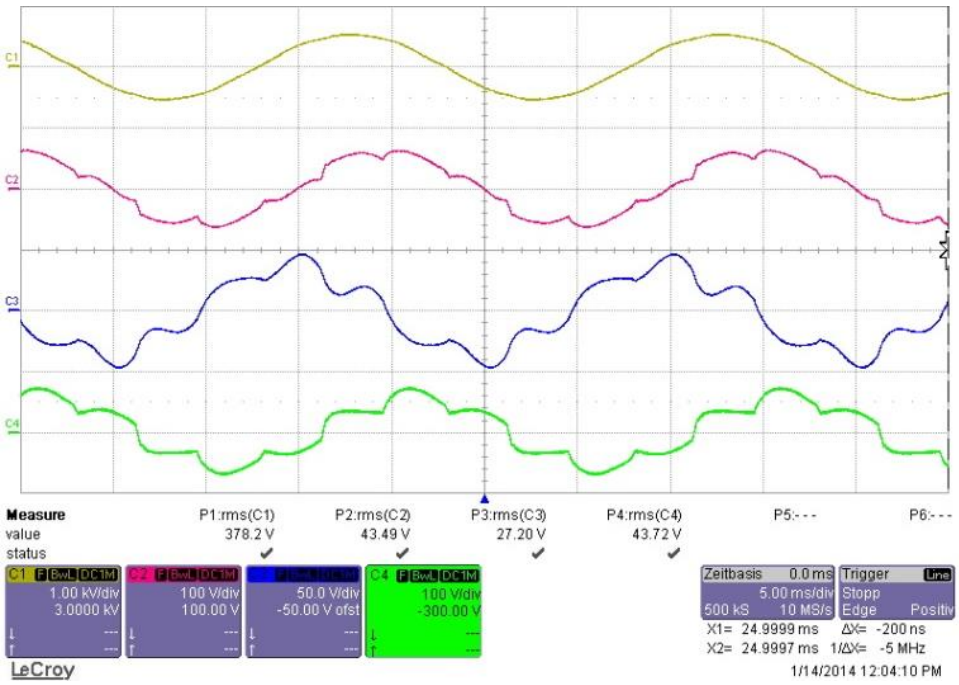


Fig. 3.13 Waveform at mode 2, showing, Ch 1 (yellow): input line-to-line voltage v_{ab} (1 kV/div), Ch 2 (red): input current i_{sa} (100 A/div), Ch 3 (blue): passive filter current i_{fa} (50 A/div) and Ch 4 (green): system current i_{Ta} (100 A/div). Time scale: 5 ms/div.

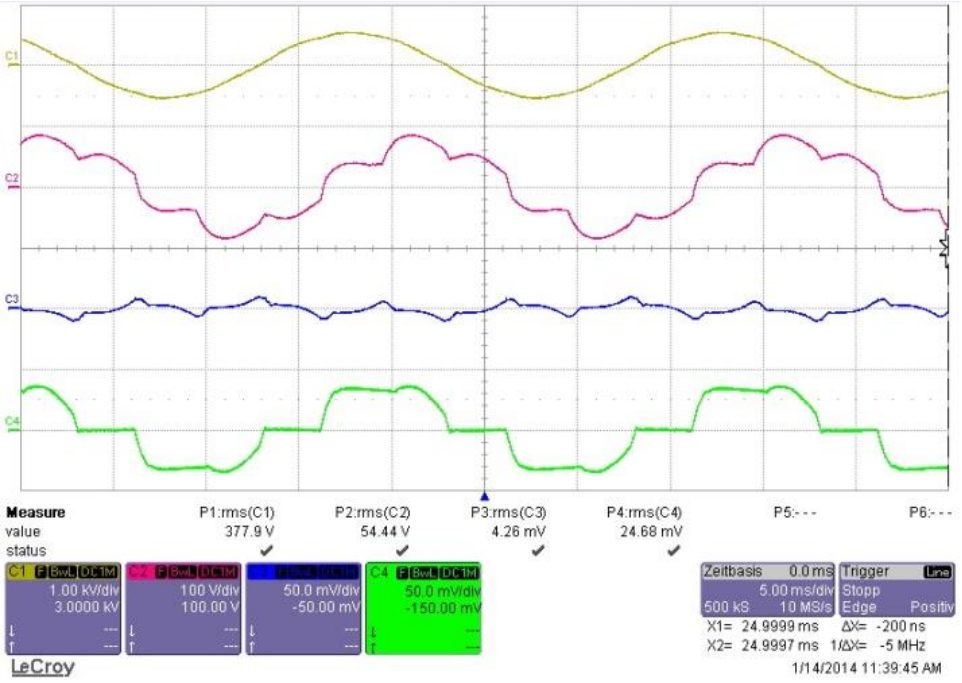


Fig. 3.14 Waveform at mode 2, showing, Ch 1: input line-to-line voltage v_{ab} (1 kV/div), Ch 2 (red): system current i_{Ta} (100 A/div), Ch 3 (blue): thyristor T_{a1} current i_{Ta1} (50 A/div) and Ch 4 (green): thyristor T_{a2} current (50 A/div) i_{Ta2}. Time scale: 5 ms/div.

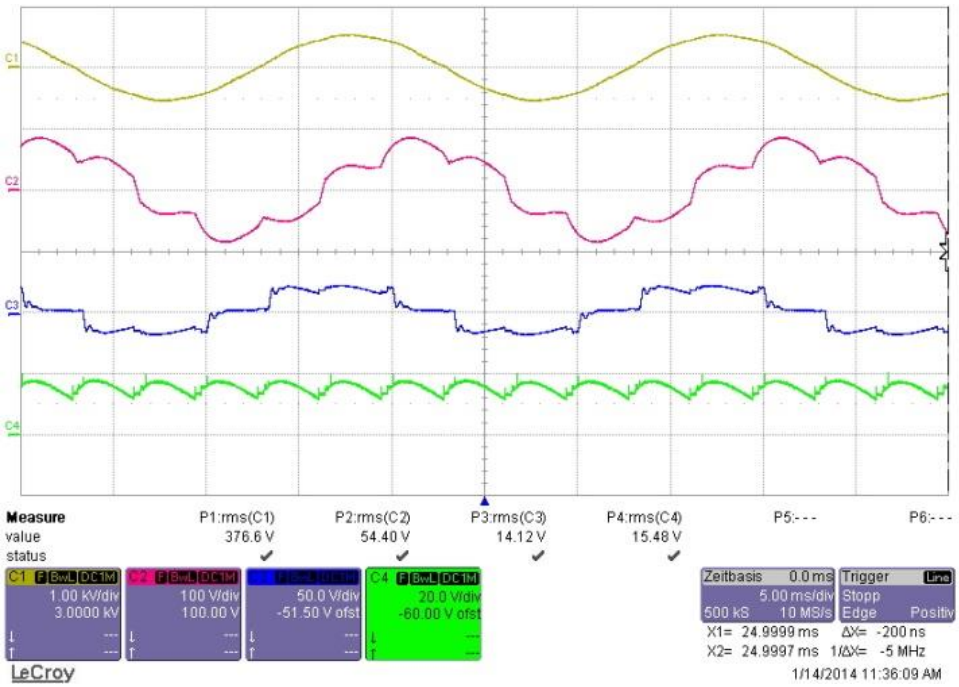
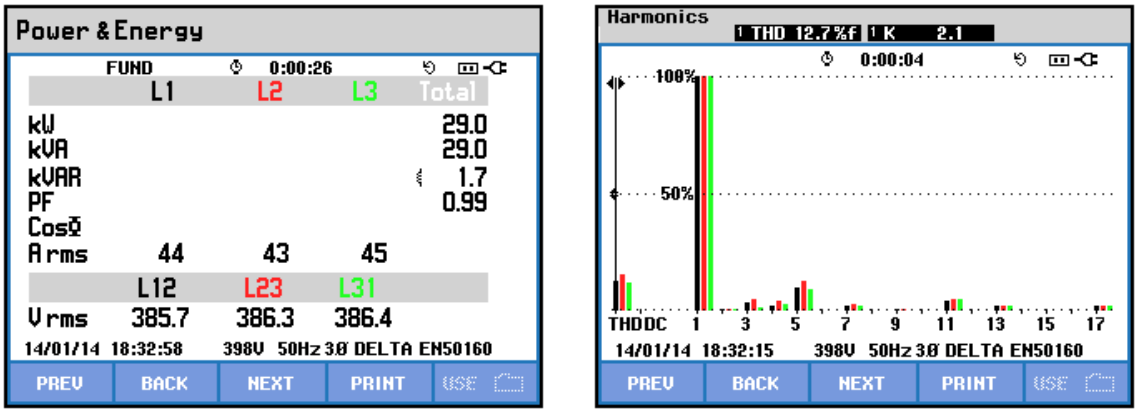


Fig. 3.15 Waveform at mode 2, showing, Ch 1 (yellow): input line-to-line voltage v_{ab} (1 kV/div), Ch 2 (red): system current i_{Ta} (100 A/div), Ch 3 (blue): transformer secondary line-to-line voltage v_{AB} (50 V/div) and Ch 4 (green): load voltage v_L (20 V/div). Time scale: 5 ms/div.



(a) (b)

Fig. 3.16 With passive filter under mode 2 (a) input voltage, current, active, apparent and reactive power and power factor measurements (b) input current THD.

Fig. 3.17 shows the simulated and experimental variation of power factor over the output DC voltage (with AC mains voltage of 400 V and 25 V/2500 A load resistor). It can be seen that the power factor remains higher than 0.95 for the required range of the output voltage i.e. 100 % to 36 %. Moreover, the simulated and experimental values of power factor are within close conformity. The small difference between experimental and simulated results emerges from the non-ideal conditions such as input voltage distortion not considered during simulation. Variation of

input current THD is shown in Fig. 3.18. Since only a 5th harmonic filter is used the current THD stays above 10 % for most of the load range

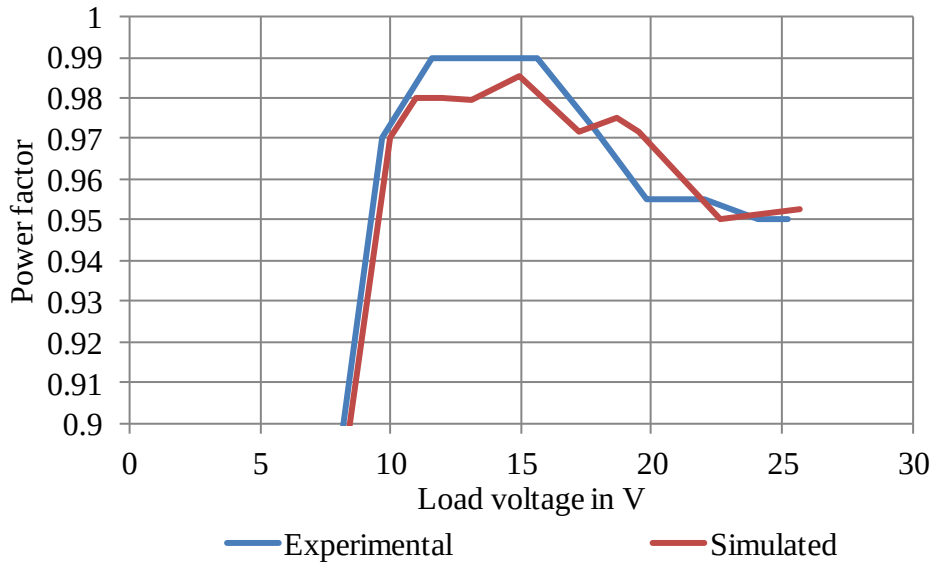


Fig. 3.17 Variation of power factor with output voltage

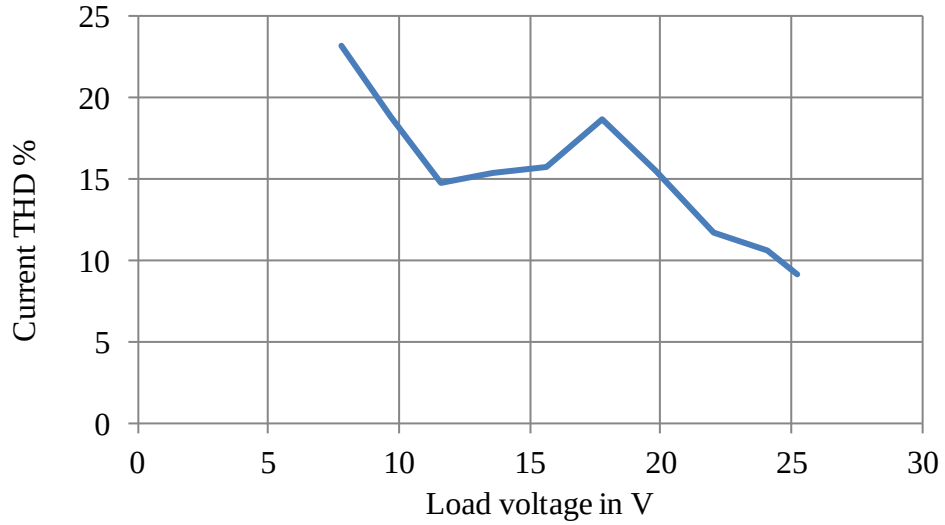


Fig. 3.18 Variation of input current THD with output voltage

3.4 Summary

In this chapter, a thyristor and diode-based rectifier topology is discussed for high-current variable-voltage applications. Apart from working principle, turns-ratio optimization and experimental results are presented.

It is demonstrated that the topology with optimized turns-ratio results in reduction of passive filter rating as compared to the conventional B6C thyristor rectifier. The topology also results into enhancement of the voltage range, over which, the high power factor is maintained. Experimental results, at industrial scale, verify the theoretical findings. Design rules has been formulated for different values of power factor that provide optimized turns ratio, minimum required rating of passive filter and voltage range.

The major limitations of the system are listed below.

1. Due to use of a fixed compensation provided by the passive filter, the desired power factor cannot be achieved over the full operating range. Moreover as the specified power factor increases the load voltage range (with specified power factor) shrinks.
2. As only a dominant-harmonic filter is used the current THD reduction is limited; however, the current THD can be further reduced by adding passive filters tuned at other frequencies (7^{th} harmonic, 11^{th} harmonic and high pass).
3. The number of parts increases as compared to the standard B6C thyristor rectifier. Because of this reason a 12-pulse variant of the present system becomes very complex. Moreover, full cancellation of 5^{th} and 7^{th} harmonics is not possible, as star and delta winding configurations lead to different magnitude of these harmonic currents. Nevertheless, a 12-pulse configuration results in improved harmonic performance as compared to the six-pulse configuration; however, with significant amount of 5^{th} and 7^{th} harmonic current components.

4. High Current Rectifier Systems with Compensating Devices

In order to overcome the shortfalls of the fixed compensation provided by passive filters, active power filters (APFs) or DSTATCOMs (distribution static compensators) are proposed in the literature [46]–[63]. An APF or a DSTACOM can provide a varying amount of harmonic current, reactive power and unbalanced current compensation to achieve the desired power factor. An APF or a DSTATCOM is principally the same technology but named differently by different researchers. A DSTATCOM consists of a voltage source converter (VSC), connected to the AC mains through inductive filters. With the increasing reactive power need (with high-power high rectifier firing angles), required rating of DSTATCOM also increases. This in turns leads to higher cost and lower efficiency of the overall system. To cater the issue of higher cost of a DSTATCOM, a number of hybrid filters are proposed. These filters use a combination of a passive and an active filter [57]–[63]. There are several possible combinations in which a passive filter and an active filter can be connected, most popular of these are: (a) the combination of a series active filter with a shunt passive filter [57] and (b) shunt operation of series connected active and passive filters (also known as parallel hybrid filter) [58]. Series active and shunt passive filter combination uses extra transformers in series with the load that increases volume of the system significantly. A parallel hybrid filter tries to reduce the voltage rating of the active filter. However, current flowing through the active filter remains same. This type of hybrid filter is more suitable for a diode bridge type of load connected to a medium-voltage grid. In this type of system, the reactive power demand is not significantly high and reduction in the voltage rating of the active filter can be achieved because of series connection of active and passive filter. However, in case of a high reactive power demand at the low-voltage grid (400 V), the semiconductor switches (of VSC) shall be rated at very high current and low voltage. This type of switches are not readily available, therefore, it results in higher capital cost. Another type of hybrid combination proposed in literature is parallel operation of passive and active filters [62], [63]. However, detailed investigations of this kind of solution have not been published for a practical industrial load with experimental results.

This chapter discusses a parallel combination of a passive filter and a DSTATCOM employed with a 12-pulse rectifier for feeding a variable-voltage high-current DC load [B], [C]. The combination of passive filter and DSTATCOM provides both harmonic current and reactive power compensation. The DSTATCOM provides only reactive power compensation and the harmonics are compensated by a dominant-harmonic (11^{th} harmonic) passive filter. Rating of the DSTATCOM is reduced as the reactive power compensation is predominantly provided by the passive filter. The DSTATCOM is mainly used to provide the variable reactive power compensation so that the power factor can be maintained above a certain limit. Design and performance of such a rectifier system is discussed in the next few sections and simulation and experimental results are presented to demonstrate the performance of the system.

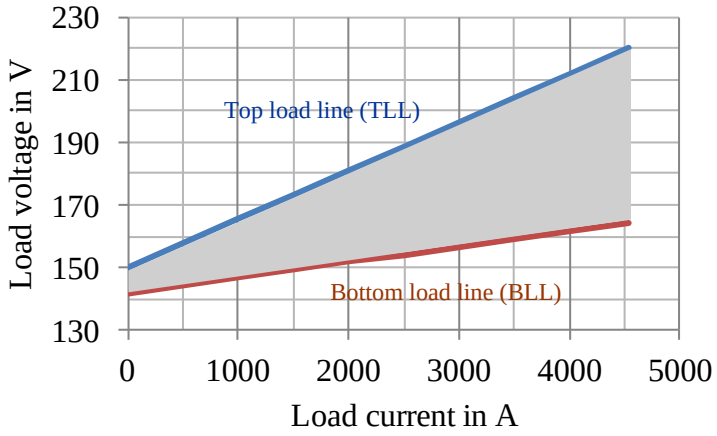


Fig. 4.1 Operating area of the 1 MW electrolyser with top and bottom load lines showing the extreme operating conditions.

4.1 Load Profile and Specifications

The load profile of a considered electrolyser is shown in Fig. 4.1. It can take any state in the shaded area of operation, depending on physical parameters of the load. Approximate linearization of load profile at top and bottom boundary lines is carried out and load voltages for top and bottom curves can be represented in terms of load current, respectively as:

$$v_{dcl} = v_{dcl0T} + r_{lT} i_{dcl} \tag{4.1}$$

$$v_{dcl} = v_{dcl0B} + r_{lB} i_{dcl} \tag{4.2}$$

where v_{dcl0T} and v_{dcl0B} are load voltage at zero current at top load line (TLL) and bottom load line (BLL) respectively. Internal resistances at TLL and BLL are represented by r_{lT} and r_{lB}

respectively. Values of v_{dcl0T} and v_{dcl0B} are 150 V and 142 V respectively and r_{lT} and r_{lB} are 15.4 mΩ and 4.84 mΩ respectively. The process requires controlling the DC current and the load voltage varies according the load profile. One can observe that several load voltage values/points are possible for one particular value of current. This is because the internal resistance of the electrolyser varies with ageing and other physical parameters. The requirements/specifications from the equipment are given in Table 4.1 and design of the rectifier is carried out according to these customer requirements.

Table 4.1 Equipment specifications and requirements

Input voltage	400 V ± 5 %
Input frequency	50 Hz
Maximum output voltage	220 V
Maximum output current	4545 A
Output voltage ripple	5 %
Input power factor	> 0.98 (at 30–100 % current)
Input current THD	< 5% (at full load)

4.2 System Description and Design

The circuit diagram of a 12-pulse thyristor rectifier along with an 11th harmonic passive filter and DSTATCOM is shown in Fig. 4.2. Design of different components is discussed in the following sections.

4.2.1 Design of 12-Pulse Rectifier

In order to achieve relatively better current THD (as compared to six-pulse rectifier), a 12-pulse thyristor rectifier is proposed for present application. The transformer turns-ratio (2.316) is decided according to minimum input voltage and maximum DC load voltage. The leakage inductance L_l of the transformer is designed to be 6 %. Minimum average current rating of the thyristor should be one sixth of the total DC load current; however, a safety factor of 2 is a common practice in industry. The repetitive voltage ratings V_{rrm} and V_{drm} should be 2.5 times of the line-to-line voltage at transformer secondary. A DC inductor L_{dc} is connected at the output-side of the thyristor rectifiers as shown in Fig. 4.2. This inductor serves two purposes: first is to limit the circulating current flowing between the two bridge-rectifiers and second, if chosen properly, it can reduce input current harmonics significantly. T. Tanka et al. [64] defines the criteria for the selection of DC inductor. The value of the DC inductor is estimated according to below mentioned expression:

$$L_{\mathrm{dc}} \cong \frac{1.608 V_{LL\mathrm{sec}}}{4.44 \times 6 f I_{dcl}} \sin\alpha - 4L_{\mathrm{l}} \tag{4.3}$$

where V_{LLsec} is the root mean square (RMS) value of the line-to-line voltage at transformer secondary, f is the line-frequency, I_{dcl} is the rated output DC load current, α is the firing-angle and L_{l} is the leakage inductance of the transformer. The DC side capacitor is fixed at 80 mF (chosen through simulations) to keep the voltage ripple within limits defined in Table 4.1.

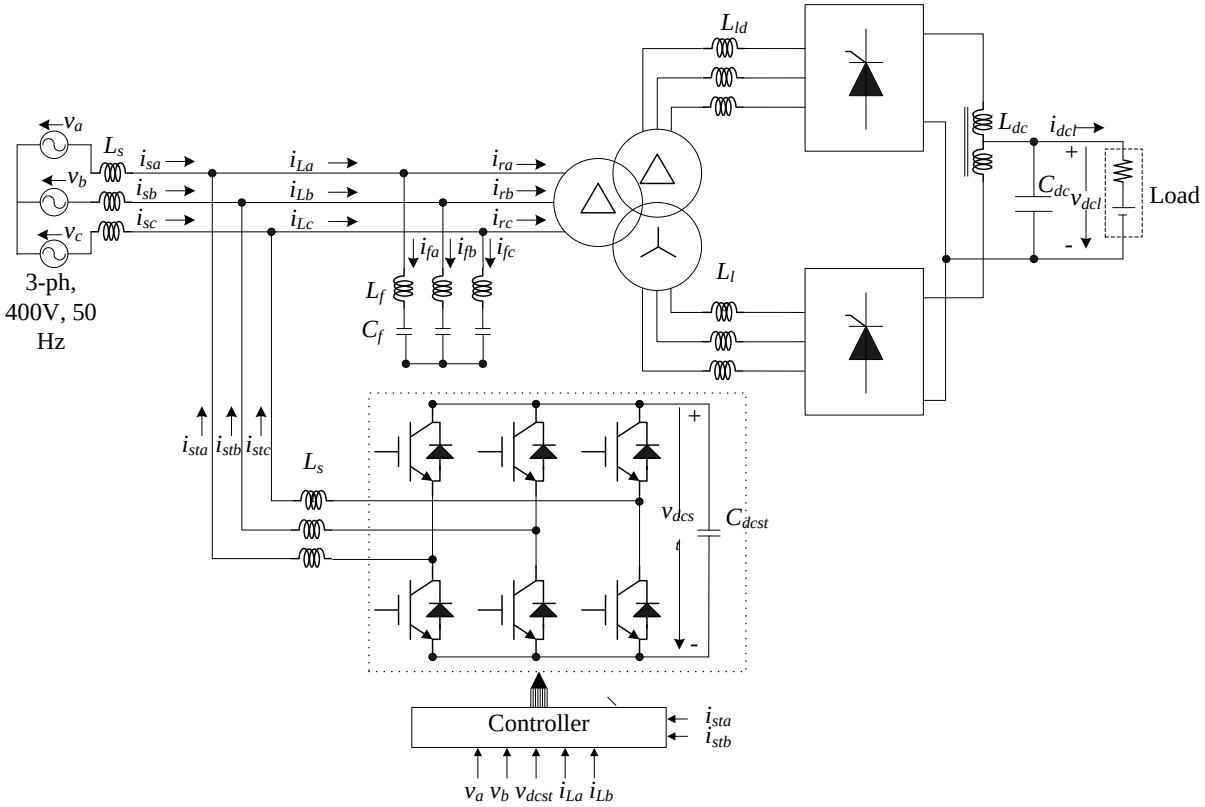


Fig. 4.2 Block diagram of the system with 12-pulse rectifier, passive filter and DSTATCOM.

Simulation of such a 12-pulse rectifier is carried out at the top and bottom load lines, defined by (4.1) and (4.2), respectively. The input grid voltage is kept at its nominal value. The load current is varied from 30 % to 100 % of its rated value. The variation of reactive power with the load current is shown in Fig. 4.3. Looking at the spread of reactive power demand, it can be concluded that a fixed compensation by a passive filter cannot maintain the power factor above 0.98 over the full operation range. In order to tackle this problem, a DSTATCOM is added in parallel with an 11$^{\mathrm{th}}$ harmonic filter (dominant-harmonic). The observed current THD remains below 10 % throughout the operating range without any filter. Therefore it can be said that a

dominant-harmonic passive filter should be able to bring the current THD below 5 % at full load (later verified through simulation and experimentation). Therefore, the DSTACOM is not used to provide harmonic compensation. This helps in reducing rating of the DSTATCOM. Additionally as no harmonic current compensation is provided by the DSTATCOM, it can work with relatively lower switching-frequency, thus results in lower switching losses in the VSC working as the DSTATCOM.

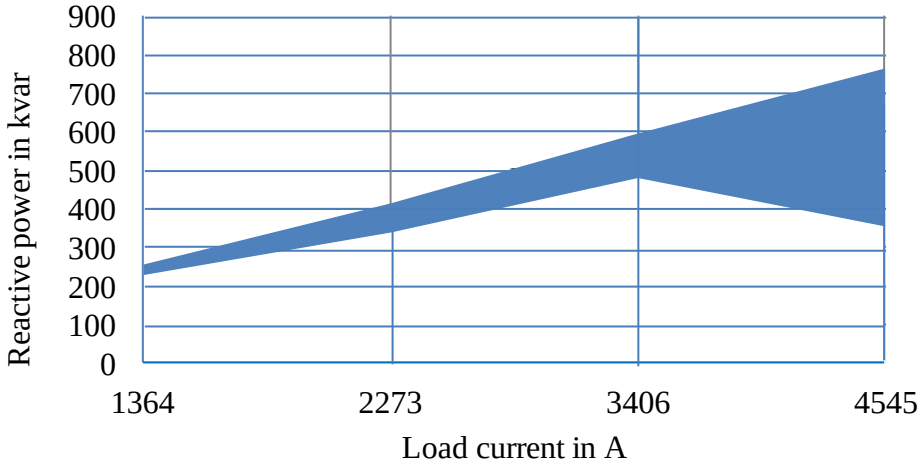


Fig. 4.3 Reactive power variation of rectifier over the load operation area.

4.2.2 Application and Design of Dominant-Harmonic Passive Filter

At this point, it is important to discuss in more detail about application of the dominant-harmonic filter for 12-pulse rectifiers. It has been widely reported that the use of only dominant-harmonic passive filter for a 12-pulse rectifiers can lead to resonances at the 5^{th} and 7^{th} harmonic frequencies or leads to an increase of harmonic currents due to harmonic amplification [55]. Therefore, recommended practice is to use 5^{th} and 7^{th} harmonic filters along with an 11^{th} harmonic filter. A 12-pulse rectifier usually results in approximately 8-10 % THD at full load (with DC side inductive filter). An appropriate 11^{th} harmonic filter alone is sufficient to reduce the THD below 5 %; however, this may lead to resonances at 5^{th} and 7^{th} harmonic frequencies. The sources of 5^{th} and 7^{th} harmonics are the grid (which can have voltage THD of 1-2 %) and the non-ideal rectifier itself. The most common rectifier non-ideality comes from multi-pulse transformer that may have different voltage ratios and different leakage inductances between delta and star windings. A controller, which provides equal firing angles to star and delta rectifiers will lead to unequal current sharing and hence 5^{th} and 7^{th} harmonics. Conversely, a

controller trying to maintain equal average DC currents from star and delta rectifiers will result into different firing angles for two rectifiers; hence, it will result into non-perfect cancelling of 5^{th} and 7^{th} harmonics. However, with a careful transformer design these issues can be reduced drastically if not eliminated completely. Moreover, an inclusion of a 2-3 % inductor on the source side can reduce the flow of harmonic currents into the filter from source side. Filter can also be over designed to accommodate for some amount of 5^{th} and 7^{th} harmonic currents. A careful design can lead to the use of only a dominant-harmonic filter with 12-pulse rectifier, with some overrating of filter components. The issue will be further discussed in section 4.5.1, while discussing the experimental performance of harmonic filter.

Fig. 4.2 shows the full circuit diagram of the rectifier system. Reactive power ratings of filter and DSTATCOM are decided by minimum and maximum demand of reactive power to keep PF≥ 0.98. If the reactive power rating of the passive filter and the DSTATCOM are defined by Q_f and Q_{st} respectively:

$$Q_f = (Q_{\max} + Q_{\min})/2 \tag{4.4}$$

$$Q_{st} = (Q_{\max} - Q_{\min})/2 \tag{4.5}$$

where $Q_{\min}$ and $Q_{\max}$ are minimum and maximum reactive power demands respectively to keep PF≥ 0.98. In this case $Q_{\min}$ and $Q_{\max}$ are 275 kVA and 615 kVA respectively and estimated values of Q_f and Q_{st} are 445 kVA and 170 kVA respectively. The capacitance value C_f of the capacitor used in the 11^{th} harmonic passive filter can be estimated as:

$$C_f = \frac{Q_f}{2\pi f V_{LL}^2}\left(1 - \frac{1}{H^2}\right) \tag{4.6}$$

where V_{LL} is the RMS value of the nominal input line-to-line voltage and H is the order of the harmonic. The inductor value used in the passive filter is given as:

$$L_f = \frac{1}{4H^2\pi^2 f^2 C_f} \tag{4.7}$$

The quality factor, defined as the ratio of reactance to resistance of the filter inductor, is selected as 20 to keep the filter losses low.

4.2.3 Design of DSTATCOM

Rating of the VSC working as DSTATCOM is decided as per (4.5). The average value of the DC-bus voltage V_{dcst} of the VSC should be higher than √2 times AC line-to-line voltage [59]. As the semiconductor losses incurred in VSC swells with increase in the DC-bus voltage, one wants to keep the DC-bus voltage as low as possible. However, considering voltage drops in switches and AC inductors, the reference DC-bus voltage is fixed at 750 V. With a DC link voltage fixed at 750 V and reactive power rating of 170 kVA, semiconductor devices with current and voltage rating of 60 A and 1200 V, respectively, can be used to realize the VSC. These are commonly available switch ratings, therefore, capital cost of DSTATCOM remains low. Switching frequency f_s of the VSC is kept at 5 kHz to keep the losses in DSTATCOM minimal. Value of filter inductor L_{st} can be found from basic boost operation of VSC (short-circuiting the grid line-to-line voltage through inductors and switches and then opening of switches to charge DC link capacitor). The value of the filter inductors L_{st} can be calculated as:

$$L_{st} = \frac{\sqrt{2}V_{LL}}{2 f_s \Delta i_{st}} \left(1 - \frac{\sqrt{2}V_{LL}}{V_{dcst}}\right) \tag{4.8}$$

where Δi_{st} is the permissible ripple in the DSTATCOM input current that is set at 10 %. However, there is another criterion for designing the input inductor that is based on the voltage drop across the inductors. Once the DC link voltage is decided, the maximum voltage generated by the VSC is fixed. The voltage drop across the inductor should not be more than the difference between VSC-side voltage and grid-side voltage. Therefore, one should crosscheck the rated voltage drop across the inductors at rated DSTATCOM current.

The value of the DC link capacitor, in terms of DC-bus voltage ripple Δv_{dcst} and RMS value of the AC current I_{st} can be estimated by:

$$C_{st} = \frac{\sqrt{2}I_{st}}{f_s \Delta v_{dcst}} \left(1 - \frac{\sqrt{3}V_{LL}}{\sqrt{2}V_{dcst}}\right) \tag{4.9}$$

Table 4.2 summarizes the ratings of different components used in the realization of the rectifier system.

Table 4.2 System parameters

Source	3-ph, 400 V, 50 Hz, L_s=10 µH
Transformer	3-ph, 1075 kVA, Dd0y1, V_{pri}=400 V, V_{sec}=172 V, L_l=4.7 µH
Rectifier	L_{dc}=45.63 µH, C_{dc}=8000 µF, Thyristor average current=757 A
DSTATCOM	170 kVA, f_s=5 kHz, L_{st}=0.55 mH, C_{dcst}=1600 µF, IGBT voltage and current: 750 V and 60 A
Passive filter	445 kVA, C_f=8780 µF, L_f=9.54 µH, Q=20

4.3 Control of DSTATCOM

The synchronous reference frame (SRF) theory is used to realize the control of DSTATCOM. SRF theory is based on the transformation of the currents in synchronously rotating d-q frame [60]. Fig. 4.4 explains the basic building blocks of the control algorithm. If the grid (or input) phase-neutral voltages are given as:

$$v_a(t) = V_m \sin(\omega t) \tag{4.10}$$

$$v_b(t) = V_m \sin(\omega t - 2\pi/3) \tag{4.11}$$

$$v_c(t) = V_m \sin(\omega t - 4\pi/3) \tag{4.12}$$

where ω is the angular frequency and V_m is the peak of the input phase voltage.

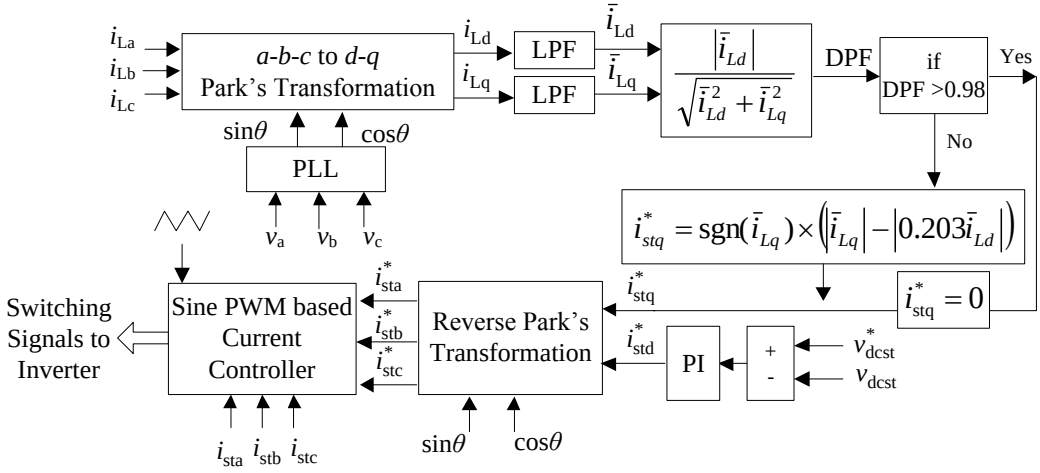


Fig. 4.4 Control block diagram of DSTATCOM.

Respective sensed currents (i_{La}, i_{Lb} and i_{Lc}) that are the sum of rectifier currents (i_{ra}, i_{rb} and i_{rc}) and passive filter currents (i_{fa}, i_{fb} and i_{fc}) are given as:

$$i_{La}(t) = \sum I_{Lan} \sin(n\omega t - \phi_{an}) \tag{4.13}$$

$$i_{Lb}(t) = \sum I_{Lbn} \sin\{n(\omega t - 2\pi/3) - \phi_{bn}\} \tag{4.14}$$

$$i_{Lc}(t) = \sum I_{Lcn} \sin\{n(\omega t - 4\pi/3) - \phi_{cn}\} \tag{4.15}$$

where I_{Lan}, I_{Lbn} and I_{Lcn} are the peak values of the n[th] harmonic component of the three-phase currents. Angles ϕ_{an}, ϕ_{bn} and ϕ_{cn} are the phase-angles of the n[th] harmonic component of the three-phase currents.

In *a-b-c* coordinates, *a-b-c* axes are fixed on the same plane, apart from each other by 120°. If θ is the transformation angle, the currents transformation (Park's transformation) from *a-b-c* to *d-q* frame (rotating reference frame) is defined as:

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ -\sin\theta & -\sin(\theta - 2\pi/3) & -\sin(\theta + 2\pi/3) \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{4.16}$$

These *d* and *q* axis currents are filtered with the help of a low pass filters (LPF) for removal of harmonic components present in the current (rectifier+passive filter current). The extracted average components $\bar{i}_{Ld}$ and $\bar{i}_{Lq}$ represents fundamental frequency components present in the rectifier plus filter current. The displacement power factor (DPF) can be calculated as,

$$DPF = \frac{\left|\bar{i}_{Ld}\right|}{\sqrt{\bar{i}_{Ld}^2 + \bar{i}_{Lq}^2}} \tag{4.17}$$

If DPF≥ 0.98, the DSTATCOM does not supply or consume any reactive power. This is ensured by setting the reference *q*-axis DSTATCOM current equal to zero. For DPF less than 0.98 reactive power is supplied by the DSTATCOM to achieve a displacement power factor equal to 0.98. In this case, the *q*-axis DSTATCOM reference current is set to;

$$i_{stq}^{*} = \mathrm{sgn}(\bar{i}_{Lq}) \times \left(\left|\bar{i}_{Lq}\right| - \left|0.203\bar{i}_{Ld}\right|\right) \tag{4.18}$$

The DSTATCOM is operated in self-supporting DC-bus voltage mode. This means no separate DC source is used to maintain the DC-bus voltage. Therefore, it is required that the losses occurring in the DSTATCOM system (switching and conduction losses of devices, losses in reactor and dielectric losses of DC capacitor) should be supplied by the AC mains. Hence, the reference current of the DSTATCOM has two components; first, the reactive power component

computed by (4.19) and second, the current component to compensate for the losses in the DSTATCOM. To compute the second component of reference active current, a reference DC-bus voltage v_{dcst}^{*} is compared with the sensed DC-bus voltage v_{dcst} of the DSTATCOM. This results in a voltage error, which is processed in a PI controller. Output of this PI controller provides a *d*-axis DSTATCOM reference current i_{std}^{*}. These DSTATCOM references currents are transformed back to the *a-b-c* frame and are fed to a current controller to generate the switching signals for the DSTATCOM.

4.4 Simulation Results and Discussion

Modeling and simulation of the 12-pulse rectifier with passive filter and DSTATCOM is carried out in MATLAB Simulink and PLECS. The model is analyzed using ode15s (stiff/NDF) solver with a maximum step size of 1×10^{-6} s and relative tolerance of 1×10^{-4}. Fig. 4.5 shows the behavior of the system at a DC load current of 4545 A and load voltage of 220 V. Quantities shown in figure are phase-*a* voltage v_a, phase-*a* source current i_{sa}, phase-*a* rectifier current i_{ra}, phase-*a* passive filter current i_{fa}, phase-*a* DSTACOM current i_{sta}, DC-bus voltage of DSTATCOM v_{dcst}, DC-load voltage v_{dcl} and load current i_{dcl} respectively from top to bottom. In this condition, the active and reactive powers are 1 MW and 355.4 kVA. The total capacitive reactive power supplied by the passive filter is 445 kVA. This leads to an overall power factor of 0.997. Since the DPF is higher than 0.98, no reactive power is supplied by the DSTACOM. However, some real power is consumed by the DSTATCOM to maintain its DC-bus voltage constant at 750 V. Fig. 4.6 shows the harmonic spectrum of the source current. The current THD of the supply current is reduced to 2.4 % from 9.5 % because of the passive filter. Fig. 4.7 shows the performance of the rectifier system at the bottom load line with a rated DC load current of 4545 A. This operation point corresponds to the condition that requires maximum reactive power. In this case, the DSTATCOM supplies reactive power to its maximum rating and increases the power factor from 0.699 to 0.98. The active power is 754.4 kW. Fig. 4.8 shows the harmonic spectrum of the source current with THD of 2.72 %. Table 4.3 summaries the performance of the rectifier system along top and bottom load lines.

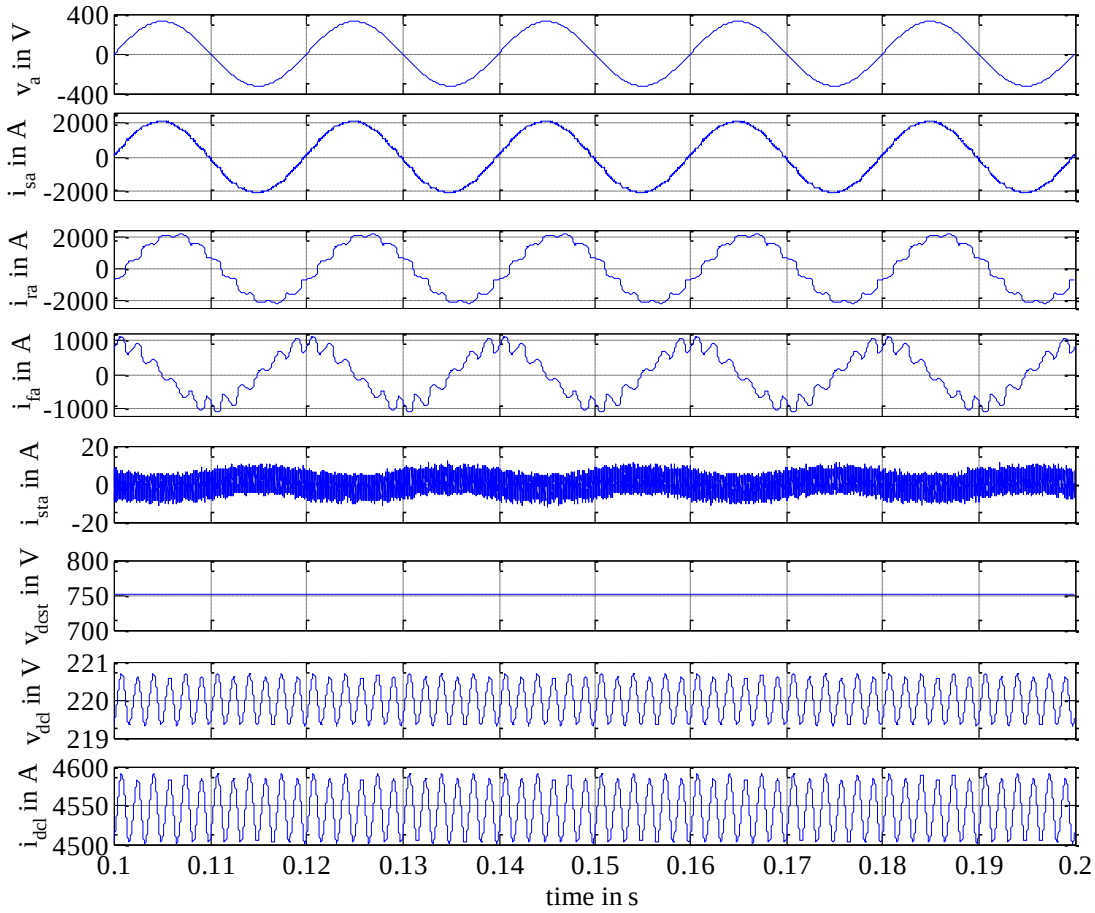


Fig. 4.5 Response of rectifier system with operation point at load profile given by (4.1) with maximum (4545 A) load current.

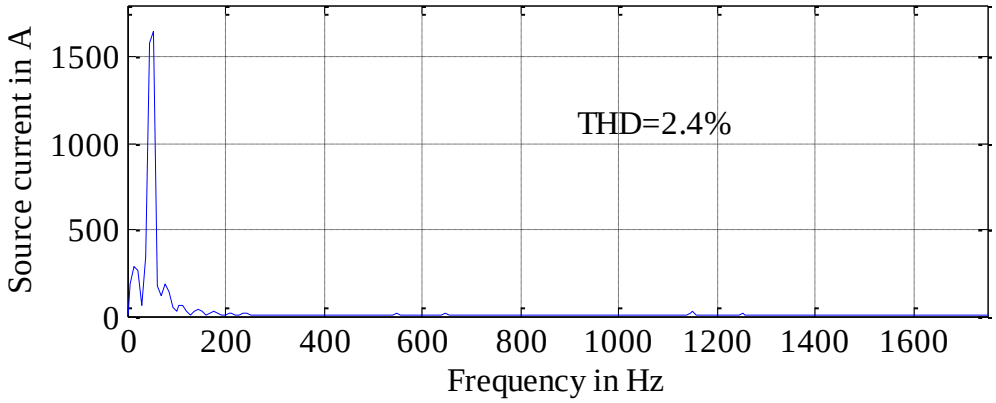


Fig. 4.6 Harmonic spectrum of source current at with operation point given by (4.1) with maximum (4545 A) load current.

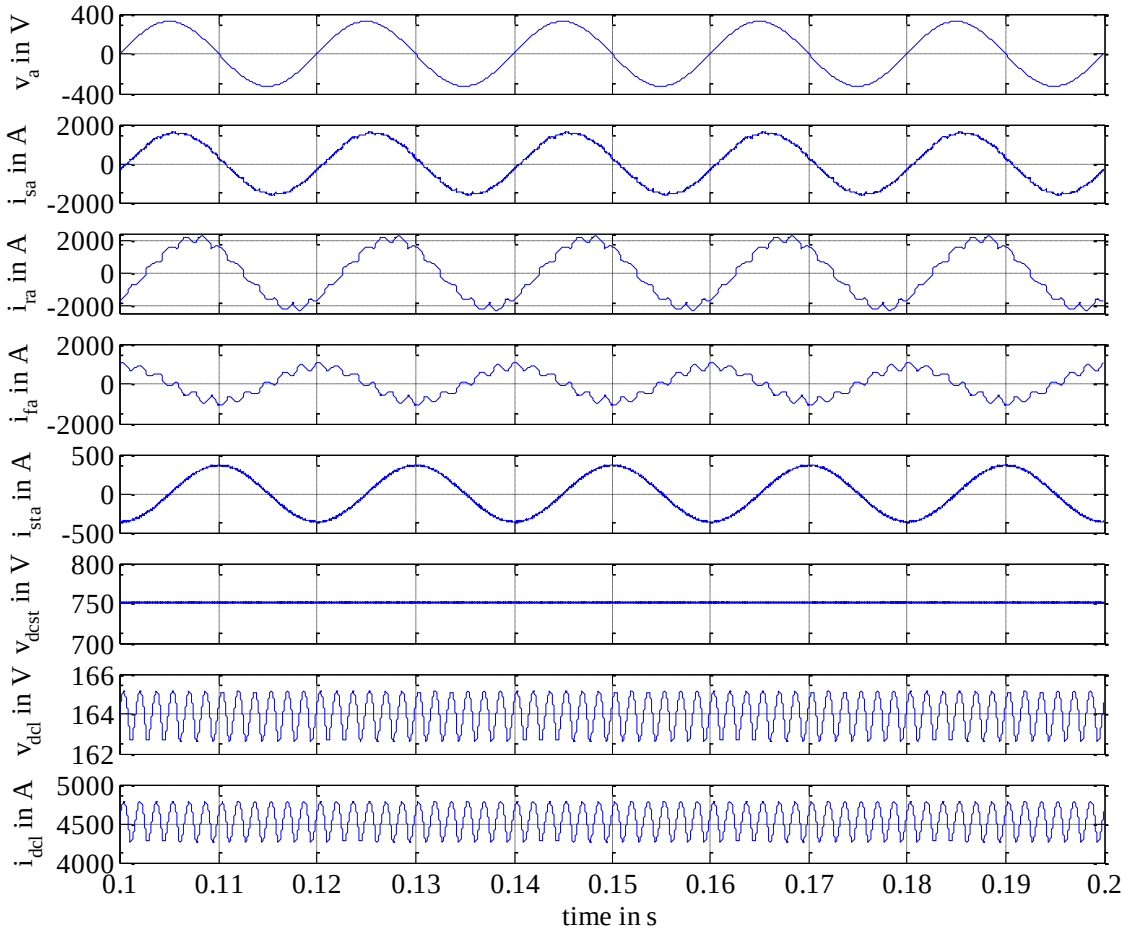


Fig. 4.7 Response of rectifier system with operation point at load profile given by (4.2) with maximum (4545 A) load current.

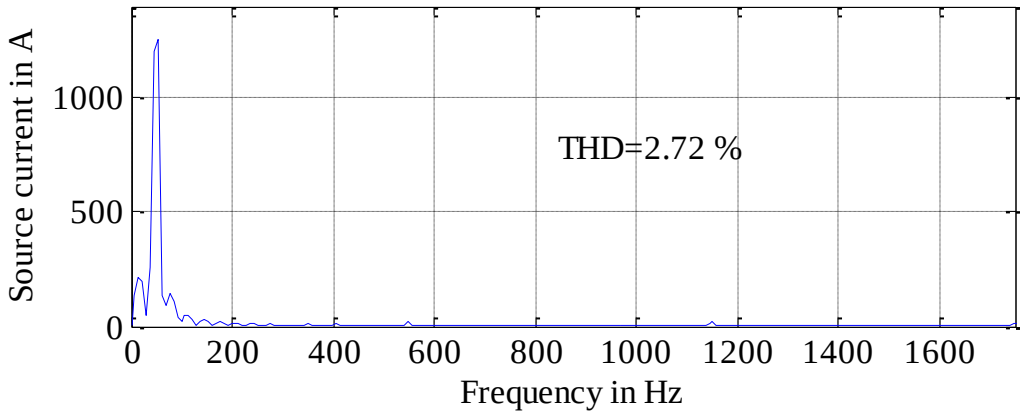


Fig. 4.8 Harmonic spectrum of source current at with operation point given by (4.2) with maximum (4545 A) load current.

Table 4.3 Load current, load voltage, real power, reactive power, power factor and current THD variation with load current variation for 12-pulse rectifier compensated by passive filter and DSTATCOM

Load current in A	Load voltage in V	ΔVpp in %	Real power in kW	Reactive power in kVA	Power factor	Current THD in %
At top load line						
4545.0	220.0	2.5	1008.7	77.1	0.997	2.4
3408.5	202.5	2.0	697.2	33.8	0.998	2.6
2275.0	185.0	2.5	427.0	87.3	0.980	2.6
1359.5	171.0	2.0	237.7	48.9	0.980	3.5
At bottom load line						
4544.5	164.0	2.5	754.4	154.5	0.980	2.7
3406.5	158.5	2.5	546.5	111.5	0.980	3.0
2275.0	153.0	2.0	353.0	29.0	0.996	3.7
1363.5	148.6	0.5	207.0	44.0	0.980	3.9

4.5 Experimental Verification

A scaled-down 20 kW 12-pulse rectifier was built to examine the performance of proposed hybrid filter. The system is connected to the 400 V, 50 Hz grid. Since the design of the passive filter depends on the variation of load, a load curve similar to the 1 MW electrolyser (Fig. 4.1) is assumed. This load curve has a similar voltage variation; however, the current rating is adapted to achieve full load power of 20 kW (rated voltage 220 V and current 90 A). The experimental load curve is shown in Fig. 4.9. Since the considered load is a scaled down representation of the actual load, findings from the experimental set-up provide a clear understanding of the actual system.

A Dd0y1, 400 V/165 V transformer and Infineon TT61N14KOF thyristors are used to form a 12-pulse rectifier. The leakage inductances (referred to the secondary side) of star and delta windings are 0.385 mH and 0.353 mH respectively. At the output side of the rectifier, an inductive capacitive filter of 2173 µH and 2000 µF (BHC A2S31A1160KF) is used as shown in Fig. 4.2. Experimental variation of the reactive power along the top and bottom load lines is shown in Fig. 4.10. The maximum and minimum values of reactive power for a load current variation from 30 % to 100 % result as 13.4 kVA and 4.8 kVA, respectively. The maximum and minimum values of the reactive power, to be compensated, to achieve 0.98 power factor, are 10.2 kVA and 0.6 kVA respectively. This leads to the required reactive power rating of the passive filter as 5.4 kVA (capacitance 107 µF) and DSTATCOM as 4.8 kVA. The nearest

possible commercially available capacitor (MKK440-I-6.9-01 by EPCOS AG) rating of 116 μF (5.8 kVA) is used to form the 11th harmonic passive filter along with a 721 μH inductor. A three-phase buffer inductor L_s of 509 μH is used to reduce the flow of harmonics from the grid and provide sufficient harmonic voltage drop for effective functioning of the passive filter.

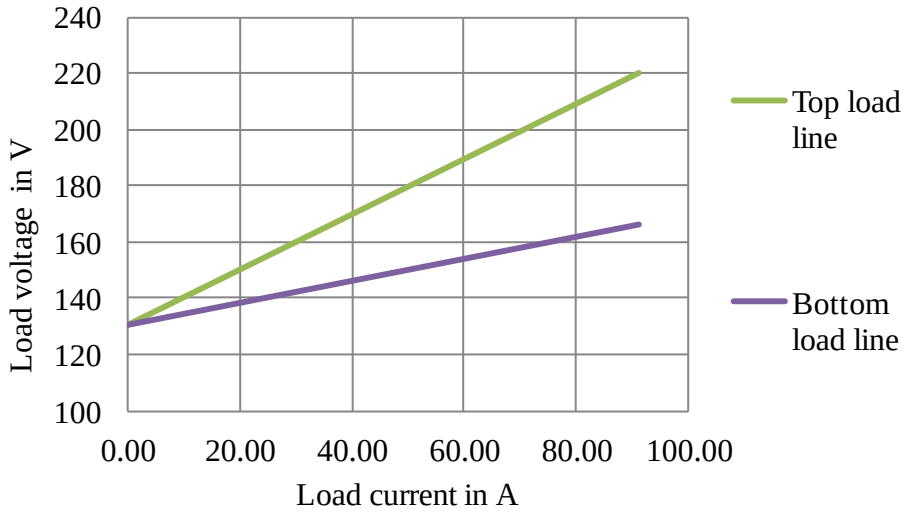


Fig. 4.9 Load lines used for experimental set-up.

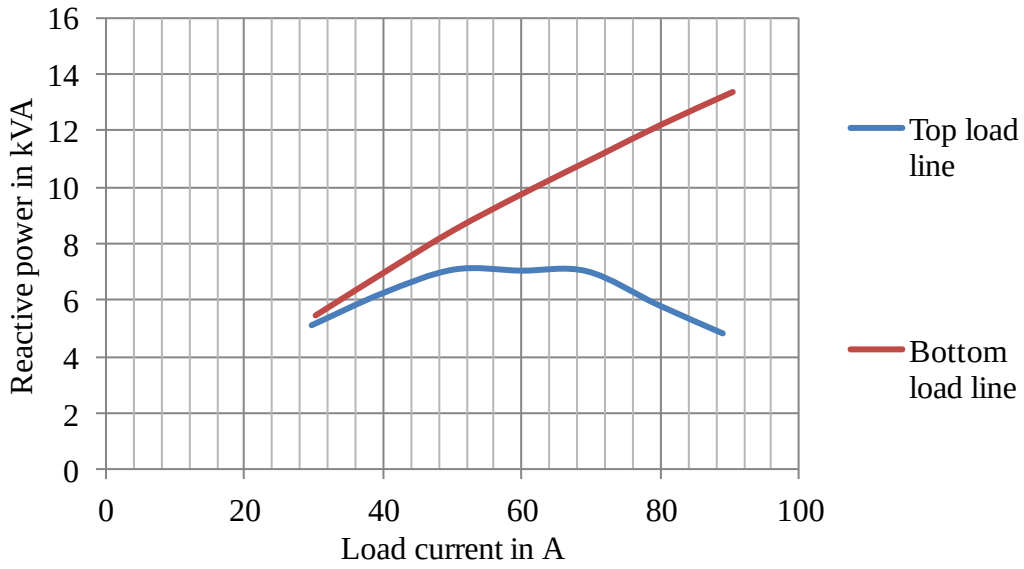


Fig. 4.10 Variation of reactive power for a 12-pulse rectifier along the top and bottom load lines.

As stated earlier, the reactive power rating of the VSC working as a DSTATCOM comes out to be 4.6 kVA. A SEMITEACH module by SEMIKRON is used as voltage source converter. The module uses 1200 V, 50 A IGBTs (SKM50GB123D) along with 1100 μF, 800 V DC link capacitor bank and SKHI22A as gate driver units. Apart from these, it has a three-phase diode rectifier and a brake chopper that are not used. A three-phase filter inductor of 10.8 μH is used to

reduce the switching frequency noise. Since the rating of the DSTATCOM is considerably less than the full scale system, a higher switching frequency of 10 kHz is selected. A DS1103 dSPACE board is used for controlling the DSTATCOM.

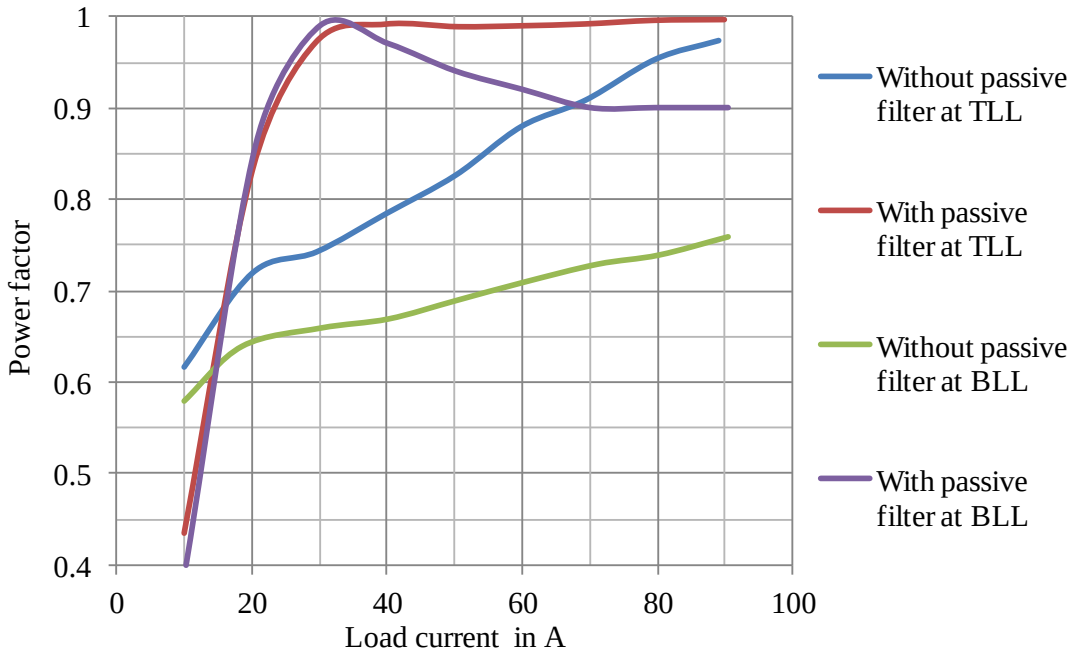


Fig. 4.11 Variation of power factor with load current along top and bottom load lines, with and without passive filter

4.5.1 Performance of 12-Pulse Thyristor Rectifier with Dominant-Harmonic Passive Filter

Before looking at the hybrid filter performance, it is important to assess the performance of the rectifier system with passive filter alone. Fig. 4.11 shows the variation of power factor with and without passive filter. It can be seen, as expected, the passive filter improves the power factor considerably over the top load line (TLL). At TLL, the power factor remains higher than 0.98 till almost 30 % of the rated load current. However, over the bottom load line (BLL), since reactive power demand is significantly higher, the improvement in the power factor is limited to 0.9 at full load. Fig. 4.12 shows the variation of the total harmonic distortion (THD) over the load range. The application of dominant-harmonic filter alone leads to a significant reduction in harmonics at top and bottom load lines. A THD of less than 5 % is achieved at full load and it remains less than 10 % till 30 % of the rated-load current for both TLL and BLL.

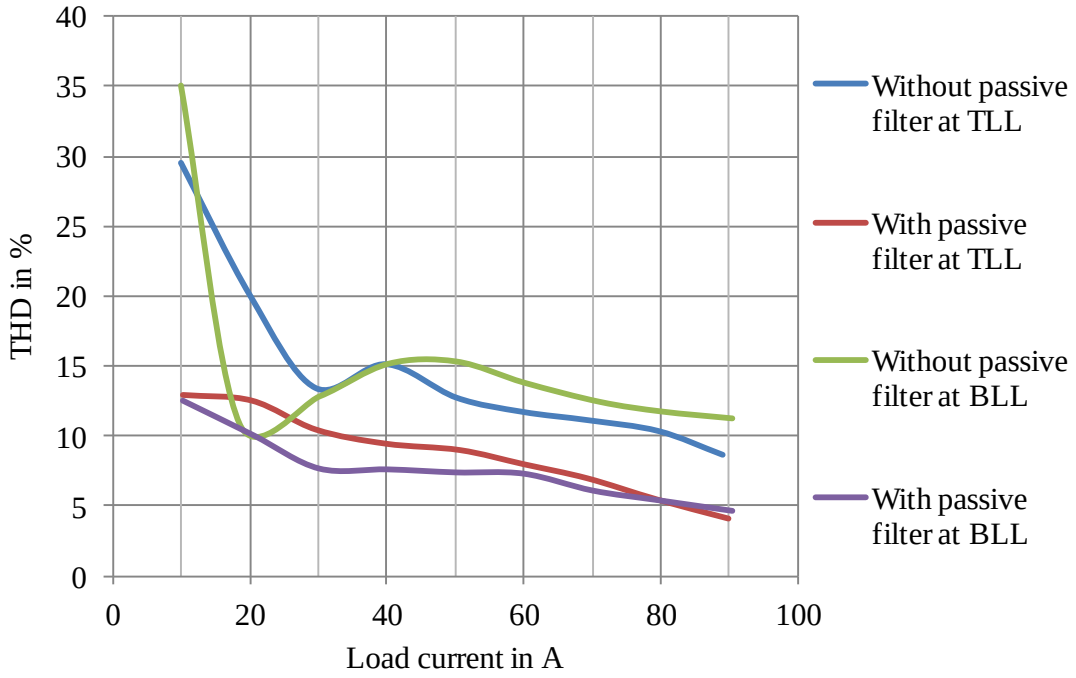
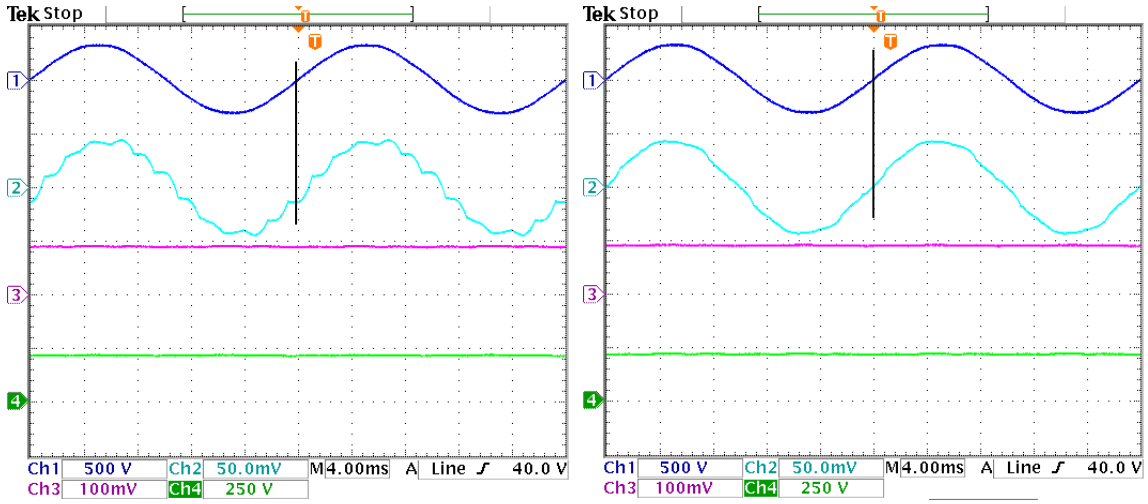


Fig. 4.12 Variation of input current THD with load current along top and bottom load lines, with and without passive filter.



(a) (b)

Fig. 4.13 Waveform showing at TLL with full load current, Ch.1 (blue): input phase voltage v_{sa} (500 V/div), Ch.2 (cyan): source current i_{sa} (50 A/div), Ch.3 (red): load current i_{dcl} (100 A/div), Ch.4 (green): load voltage v_{dcl} (250 V/div) (a) without passive filter (b) with passive filter. Time scale: 4 ms/div.

Waveforms of input phase-*a* voltage v_a, source/input current i_{sa}, load voltage v_{dcl} and load current i_{dcl}, without and with passive filter operation, are shown in Fig. 4.13 (a) and (b), respectively. Because of the passive filter application, an improvement in the source current wave-shape is clearly evident. Also, the phase-shift reduction between voltage and current is

observable due to the application of the passive filter. Source current i_{sa}, passive filter current i_{fa} and rectifier side current i_{ra} are shown in Fig. 4.14. Here again, it can be observed due to injection of current in the quadrature-phase with respect to voltage by the passive filter leads to an improvement in displacement power factor. Moreover, compensated harmonic currents improve the distortion factor.

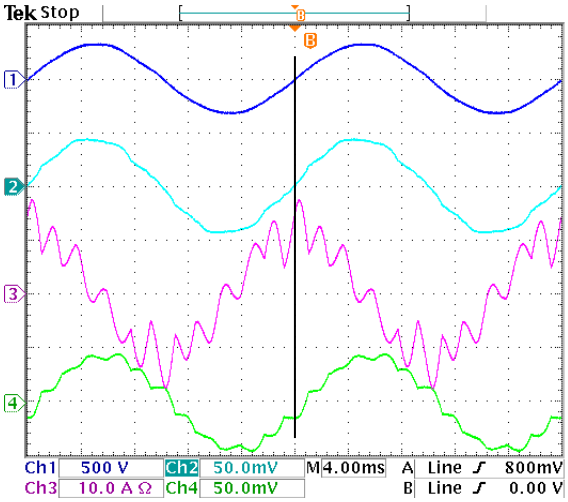
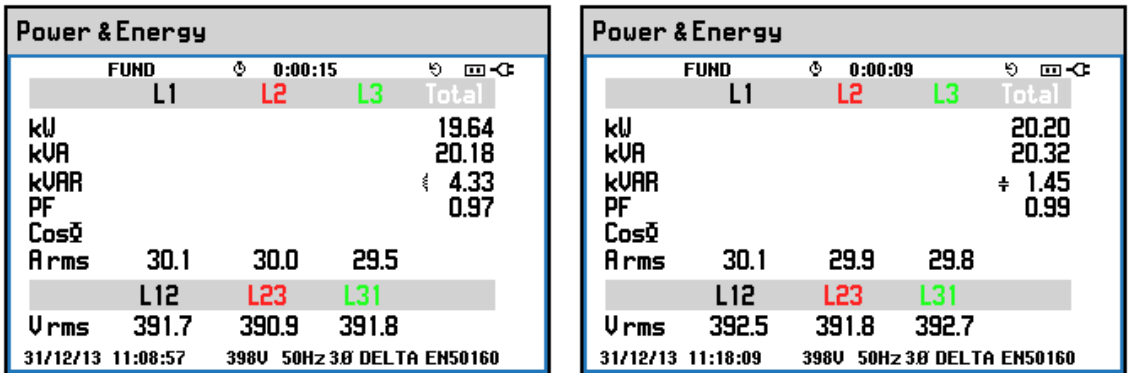


Fig. 4.14 Waveform showing at TLL with full load current, Ch.1 (blue): input phase voltage (500 V/div), Ch.2 (cyan): source current (50 A/div), Ch.3 (red): passive filter current (10 A/div), Ch.4 (green): rectifier current (50 A/div). Time scale: 4 ms/div.



(a) (b)

Fig. 4.15 Input voltage, current, active power, reactive power, apparent power and power factor data at TLL with full load current (a) without passive filter (b) with passive filter.

The quantitative improvement in the power factor is measured with the help of a three-phase power quality analyzer (Fluke 435). Fig. 4.15 (a) and (b) provide important test data. The line-to-line grid voltage is at approximately 391 V with a small amount of unbalance between different phases. The grid voltage has some amount of 5^{th} and 7^{th} harmonics with THD of 1.3 % (as shown in Fig. 4.16). The input currents also show 1.22 % unbalance without application of the passive

filter and 0.5 % after the application of the passive filter, which is a result of unbalance currents in the passive filter. Due to the application of the passive filter, the power factor changes from 0.97 to 0.99. Reactive power is changing from 4.33 kVA lagging to 1.55 kVA leading. A small change in active power seen in the two recordings is due to the losses in the passive filter and change in the grid voltage.

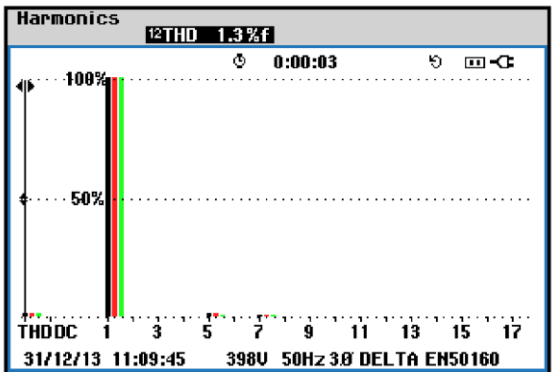
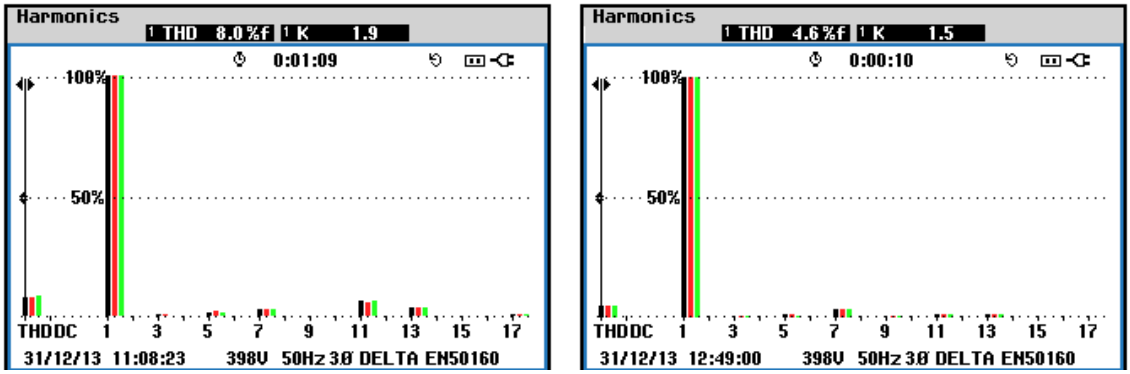


Fig. 4.16 Three-phase grid voltage harmonic spectra.

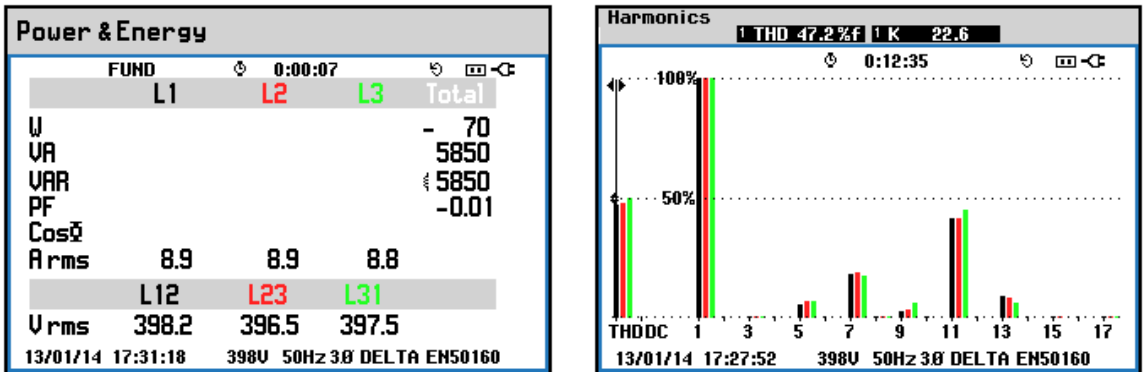


(a) (b)

Fig. 4.17 Harmonic spectra of three-phase source current at TLL with full load current (a) without passive filter (b) with passive filter.

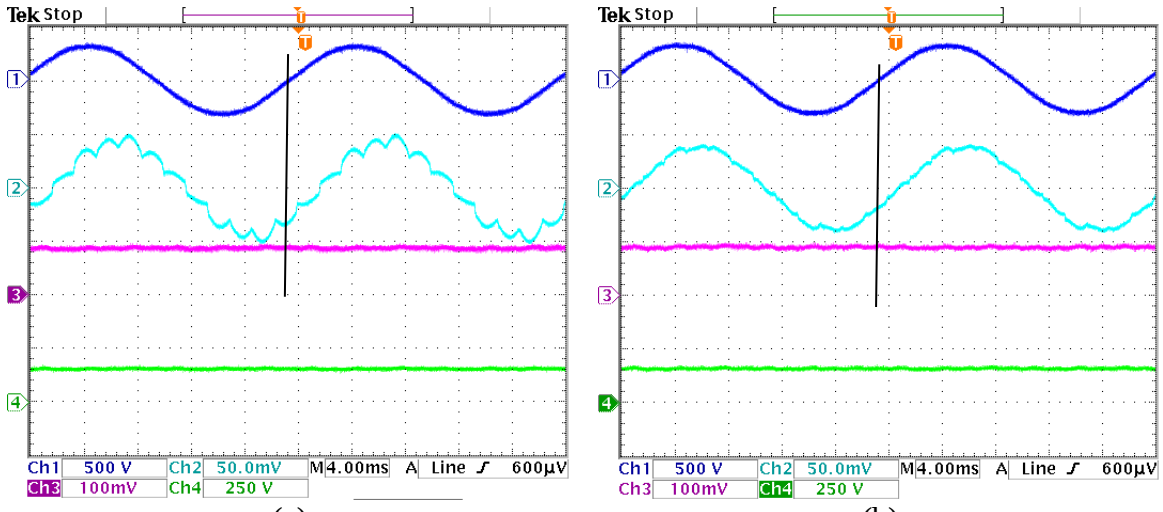
Because of the application of the passive filter, change in the input current harmonic spectrum can be seen in Fig. 4.17 (a) and (b). The current THD reduces from 8.0 % to 4.6 % due to the application of the 11^{th} harmonic passive filter. Reduction in the amplitudes of 11^{th} and 13^{th} harmonic currents can easily be observed from these two harmonic spectra. Due to the imperfect rectifier transformer (unequal leakage inductances) and grid voltage distortion, 5^{th} and 7^{th} harmonics can also be observed in the spectrum. Some amount of these 5^{th} and 7^{th} harmonic currents also flows through the passive filter as seen in the next figure. Fig. 4.18 (a) shows power data and Fig. 4.18 (b) shows the harmonic spectra of passive filter current. Data show a reactive power of 5.85 kVA with losses of 70 W (loss appears negative due to the direction of current

probe). The harmonic spectrum of the passive filter current shows that the highest amplitude occurs at the 11th harmonic. Significant amount of 5th and 7th harmonic current also flow because of reasons explained previously. However, once designed (rated as per the IEEE standard for passive filter design [51]) for these non-idealities, dominant-harmonic passive filter leads to a significant reduction in source current THD without any observed resonance. It is an important finding with respect to the application of a dominant-harmonic passive filter for a 12-pulse rectifier. As mentioned in the section 4.2, with proper design of 12-pulse transformer, buffer inductor and dominant-harmonic passive filter, the power quality performance of 12-pulse rectifier can be improved significantly.



(a) (b)

Fig. 4.18 Passive filter (a) current, active power, reactive power and apparent power date (b) current harmonic spectra.



(a) (b)

Fig. 4.19 Waveform showing at BLL with full load current, Ch.1 (blue): input phase voltage (500 V/div), Ch.2 (cyan): source current (50 A/div), Ch.3 (red): load current (100 A/div), Ch.4 (green): load voltage (250 V/div) (a) without passive filter (b) with passive filter. Time scale: 4 ms/div.

Fig. 4.19 (a) and (b) show the input and load voltages and currents without and with the passive filter at bottom load line (full load current). Similar to top load line, application of the passive filter leads to an improvement in the power factor and current THD at bottom load line. The variations of power factor and current THD at the BLL have already been discussed with the help of Fig. 4.11 and Fig. 4.12. For the operation at BLL, further waveforms are not presented to avoid repetition.

4.5.2 Performance of 12-Pulse Thyristor Rectifier with Dominant-harmonic Passive Filter and DSTATCOM

It is evident from experimental data shown in Fig. 4.11 that the passive filter alone cannot keep the power factor higher than 0.98 over the required range of operation. Therefore, a DSTACOM is employed to provide the variable reactive power compensation in addition to the passive filter. Since, along the top load line, the power factor with passive filter already reaches its required value of 0.98, the DSTATCOM does not supply any reactive power for most of the operating range. Therefore operation of DSTATCOM can best be observed over the bottom load line.

Fig. 4.20 shows the operation of the DSATCOM at the BLL with full load current. The figure shows input phase-*a* voltage v_{sa}, source current i_{sa}, DSTATCOM current i_{sta} and DSTATCOM DC-bus voltage v_{dcst}. Fig. 4.21 depicts similar waveforms except showing the rectifier plus passive filter current (shown as i_{La} in Fig. 4.2). From these two figures, one can observe that the injection of current in the quadrature-phase of the voltage leads to the power factor improvement at the source side. It can be clearly observed that the DSTATCOM operation reduces the phase-angle difference between source current and grid voltage. Fig. 4.22 shows the passive filter current along with DSTATCOM and source current. It can be observed that the DSTATCOM current remains sinusoidal and passive filter current compensates the harmonics in the rectifier current. The DSTATCOM is operated with self-supporting DC-bus voltage control. It can be seen from Fig. 4.20 that the DC-bus voltage is maintained at 750 V. Improvement in the power factor from 0.9 to 0.98 is observed because of DSTATCOM operation from the data presented in Fig. 4.23 (a) and (b). At the time of experiment, the grid voltage stands at approximately 394 V with small unbalance. The load voltage is 164.4 V at load current of 90 A. The input active power is 16.4 kW and with the DSTATCOM operation reactive power changes from 7.7 kVA to 3.0 kVA. Figure 4.24 shows the DSTATCOM power data. The total losses in the DSTATCOM

including AC inductive filter, switches and DC capacitor are 120 W. The DSTATCOM is supplying 4.9 kVA of reactive power that comes out to be the difference shown in reactive power data in previous figures, Fig. 4.23 (a) and (b). Three-phase currents supplied by the DSTATCOM are 7.2 A, 7.4 A, and 7.2 A. Because of hybrid filter operation, the input current THD changes from 11.1 % to 4.5 %. Again, at the full load, current THD comes out to be less than 5 % that is the system specification.

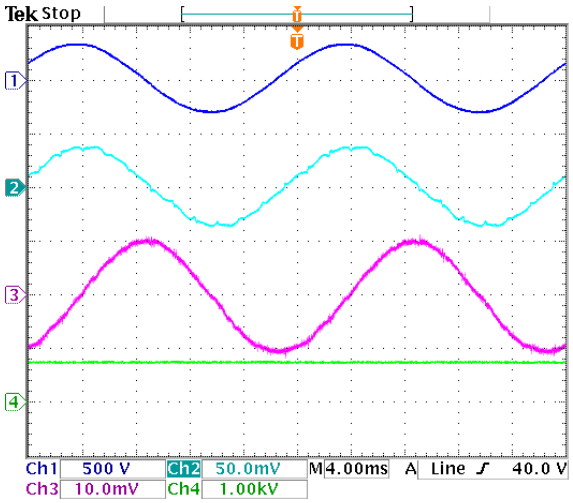


Fig. 4.20 Response of passive filter and DSTATCOM operating at BLL with full load current showing Ch.1 (blue): input phase voltage (500 V/div), Ch.2 (cyan): source current (50 A/div), Ch.3 (red): DSTATCOM current (10 A/div) and Ch.4 (green): DSTATCOM DC-bus voltage (1 kV/div). Time scale: 4 ms/div.

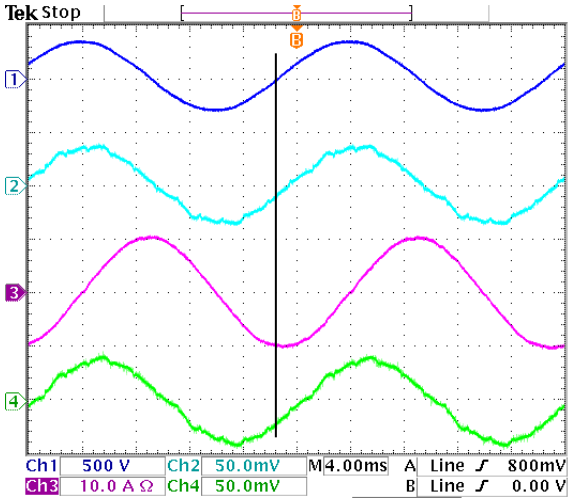


Fig. 4.21 Response of passive filter and DSTATCOM operating at BLL with full load current showing Ch.1 (blue): input phase voltage (500 V/div), Ch.2 (cyan): source current (50 A/div), Ch.3 (red): DSTATCOM current (10 A/div) and Ch.4 (green): rectifier plus passive filter current (50 A/div). Time scale: 4 ms/div. Time scale: 4 ms/div.

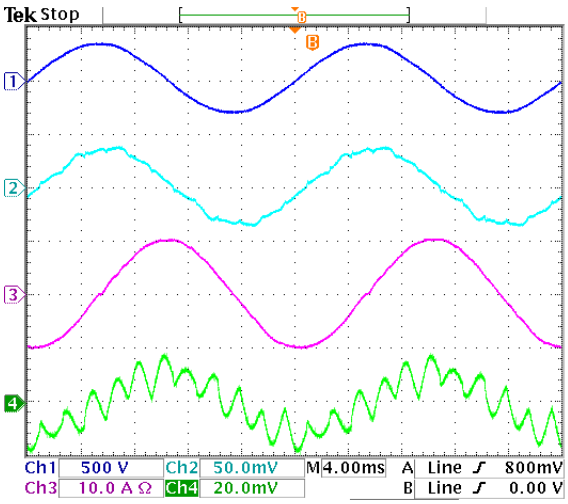
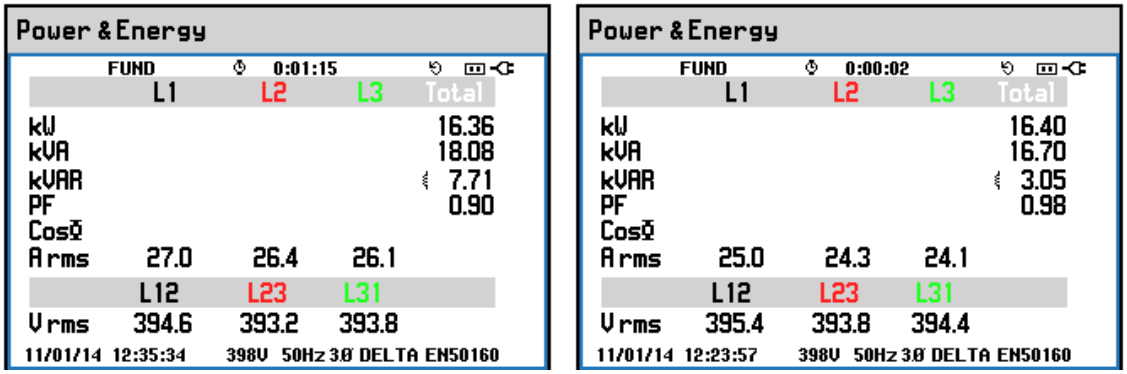


Fig. 4.22 Response of passive filter and DSTATCOM operating at BLL with full load current showing Ch.1 (blue): input phase voltage (500 V/div), Ch.2 (cyan): source current (50 A/div), Ch.3 (red): DSTATCOM current (10 A/div) and Ch.4 (green): passive filter current (20 A/div). Time scale: 4 ms/div.



(a) (b)

Fig. 4.23 Voltage, current, active power, reactive power, apparent power and power factor data (a) without DSTATCOM (with passive filter) (b) with DTSTACOM.

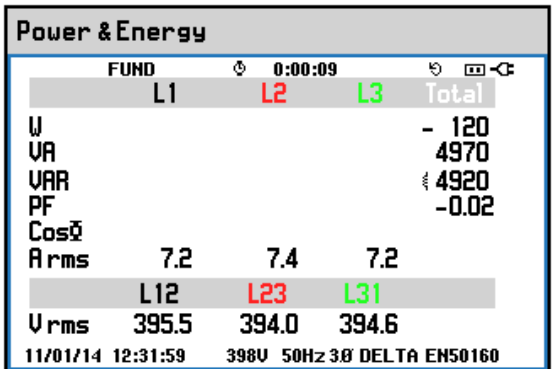
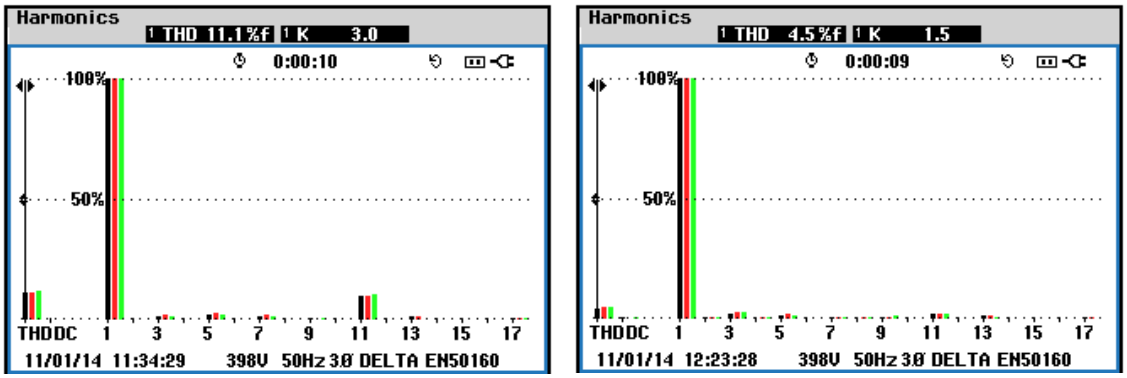


Fig. 4.24 Active power, reactive power, apparent power and power factor supplied by DSTATCOM.



(a) (b)

Fig. 4.25 Harmonic spectra of input current (a) without DSATCOM and passive filter (b) with DSATCOM and passive filter.

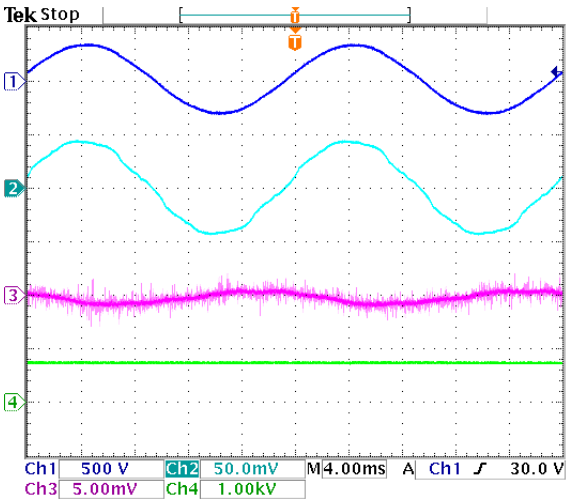


Fig. 4.26 Response of passive filter and DSTATCOM operating at TLL with full load current showing Ch.1 (blue): input phase voltage (500 V/div), Ch.2 (cyan): source current (50 A/div), Ch.3 (red): DSTATCOM current (5 A/div) and Ch.4 (green): DSTATCOM DC-bus voltage (1 kV/div). Time scale: 4 ms/div.

As explained in the control section, the DSTATCOM supplies reactive power only if the power factor is less than 0.98. This can be seen from Fig. 4.26, since at top load line with full load current, the power factor reaches 0.99 with passive filter, therefore DSTATCOM does not supply any reactive power. The small current flowing in the DSTATCOM takes care of the losses taking place in VSC to maintain the DC-bus voltage.

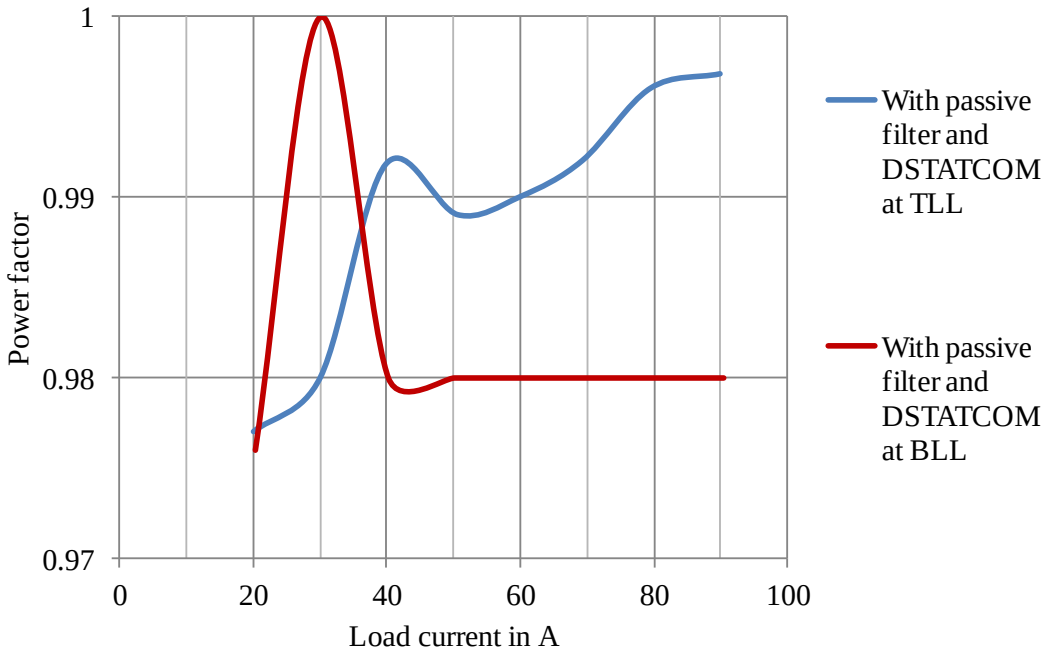


Fig. 4.27 Variation of power factor over top and bottom load lines with DSTATCOM and passive filter.

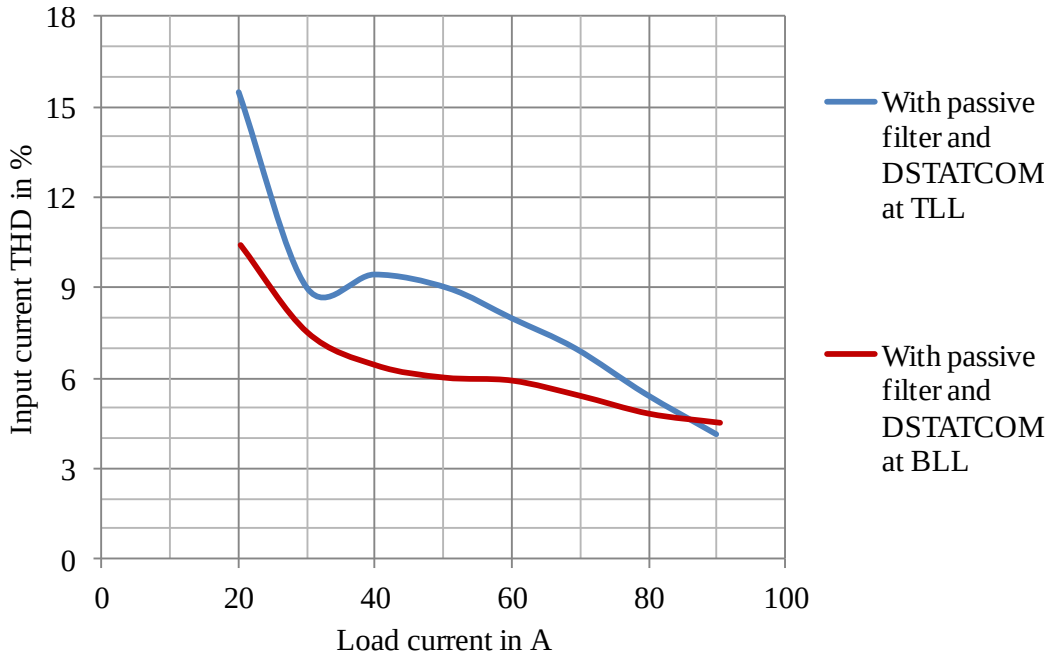


Fig. 4.28 Variation of input current THD over top and bottom load line with DSTATCOM and passive filter.

Variations of the power factor and the source current THD over the top and bottom load lines are shown in Fig. 4.27 and Fig. 4.28 respectively. It can be seen that DSTATCOM is able to keep the power factor greater than 0.98 (as specified) over the load current range of 30-100 %.

The source current THD remains less than 5 % at full load and less than 10 % till 30 % of rated load current.

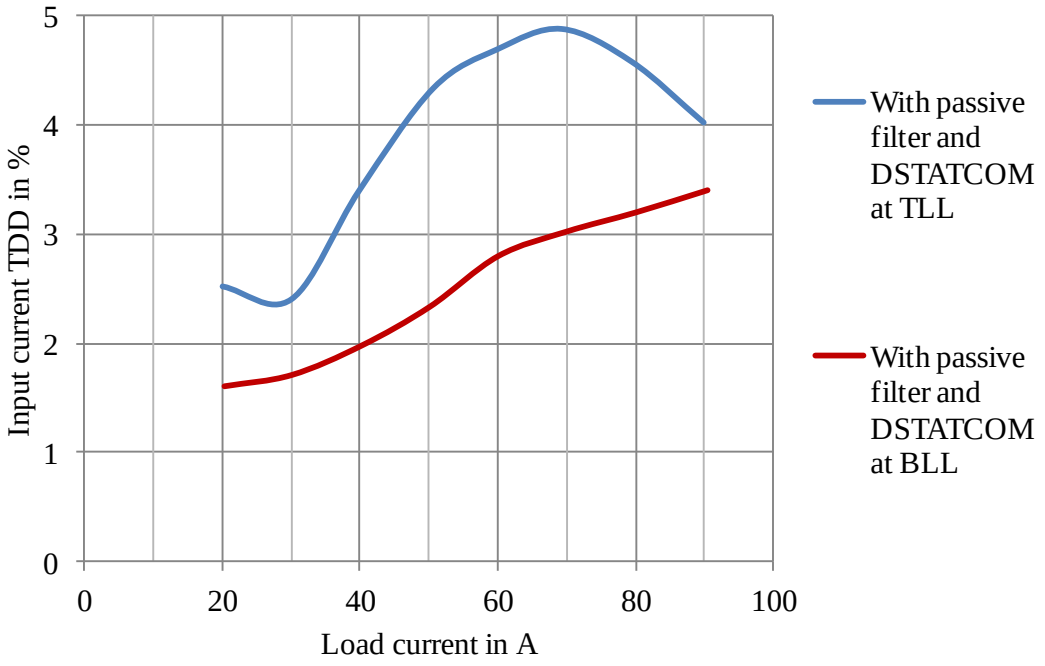


Fig. 4.29 Variation of input current TDD over top and bottom load line with DSTATCOM and passive filter.

4.5.2.1 Compliance with Power Quality Standard

So far in this chapter, the THD is considered as a measuring index of harmonic distortion. However, most of the power quality standards define distortion limits in terms of TDD (total demand distortion), which measures the harmonic distortion with respect to the rated current [45]. The limit prescribed by IEEE standard 519 is 5 % for a system having the ratio of short circuit current to the rated system current I_{SC}/I_L less than 20 (worst case scenario). It can be seen from Fig. 4.29 that the operation of the hybrid compensator meets the TDD limits set by IEEE 519. The standard also prescribes the limits to individual harmonics. Limits stand at 4 % of the rated current value for 5^{th} and 7^{th} harmonics and 2 % for 11^{th} and 13^{th} harmonics. Figures 4.30 (a)-(d) show the variations of source current harmonics over the load range. The measurement of these currents are carried out for phase-*a* with help of a single-phase power quality analyzer ZES Zimmer LMG95. During the time of the measurement, grid voltage THD remains at 1.2 %. It can be seen from shown figures that individual harmonics (5^{th} to 13^{th}) are within the prescribed limits. Only the 7^{th} harmonic component during the operation at top load line violates the limit

for a short load range. At this point, it is important to mention that different countries follow different standards thus different limits for harmonics. Moreover, individual current harmonics are highly dependent on the particular voltage harmonic component present in the grid supply. Depending on the individual cases other harmonic filters must be added to meet the standards. The value of the buffer inductor can also be increased to reduce the current harmonics.

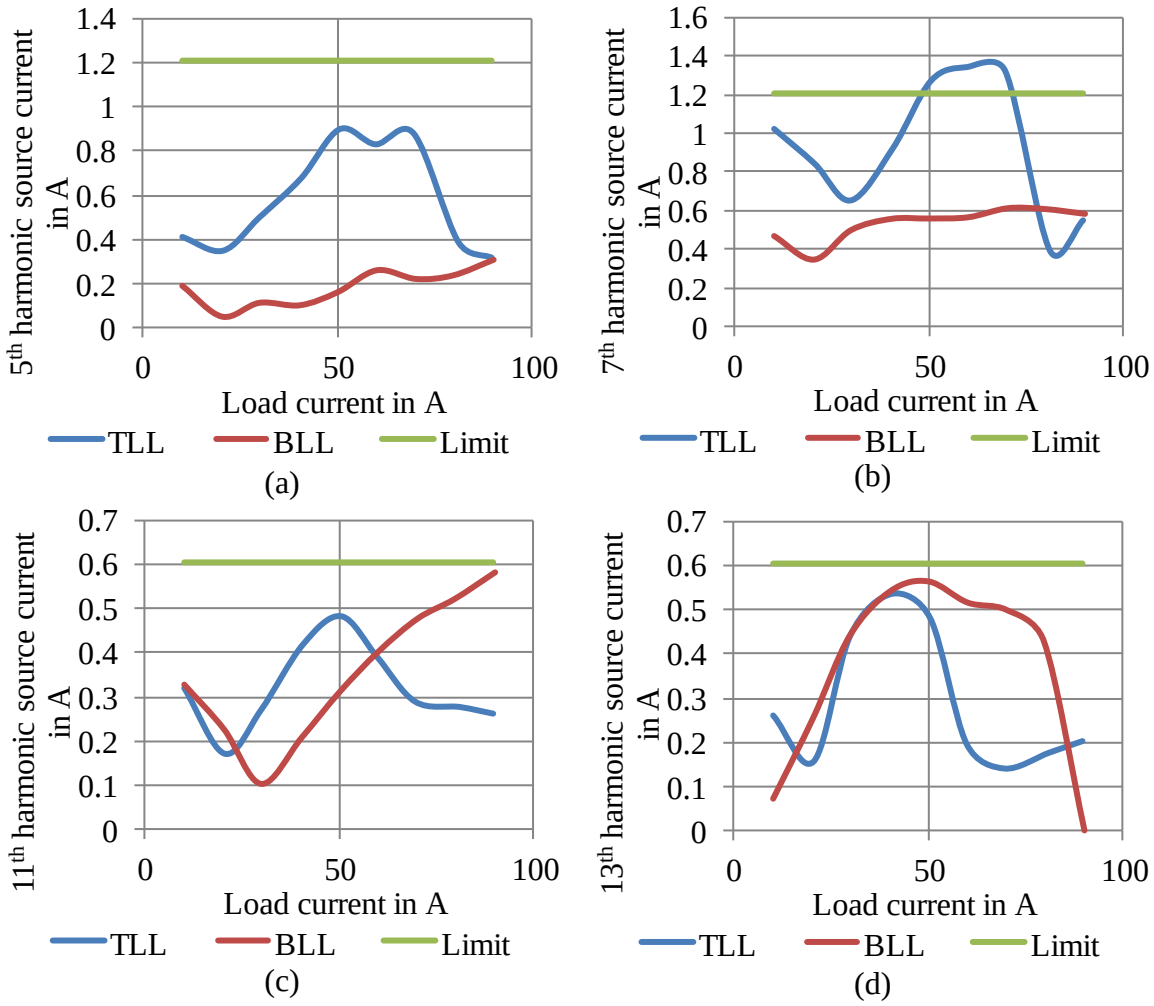


Fig. 4.30 Variation of individual harmonic components of the source current with respect to the load current

4.5.2.2 Dynamic Performance of the DSTATCOM

Till now, the dynamic performance of the system has not been discussed. The reason is that for an electrolyser type of load, the power does not change rapidly. However, this hybrid compensator can be also applied for other type of loads. Hence, the capability of the DSTATCOM to respond to load change is shown in Fig. 4.31. The step change in DC load is not

reflected on the rectifier input side as a step change due to the rectifier controller dynamics. Therefore, to observe the dynamic behavior of the DSTATCOM, the passive filter is turned off suddenly. For this purpose an operating point is chosen such that the DSTATCOM alone can improve the power factor using its full capacity. Load current of 80 A at top load line is selected as operating point because approximately 5 kVA of reactive power compensation is required at this operating point to achieve a power factor of 0.98. Moreover, at this operating point, the passive filter alone can maintain power factor greater than 0.98. Therefore, turning off the passive filter leads to a 100 % step change in current supplied by the DSATCOM. As shown in Fig. 4.31, at time t_0 the passive filter is turned off (Ch. 1: passive filter current), this leads to a power factor reduction, triggering the DSTATCOM to start (Ch. 3: DSTATCOM current). As shown in this figure, the time taken for the whole process (from time t_0 to t_1) is 10 ms, which is the delay caused by the low pass filter, filtering *d-q* axis load currents as shown in Fig. 4.4. The effect of the passive filter turn off can be seen on source current waveform (Ch. 2: source current) indicating more distortion. This step load change does not have an observable effect on the DC-bus voltage (Ch. 4: DC-bus voltage of VSC) of the DSTATCOM because of relatively a bigger capacitor used at the DC link.

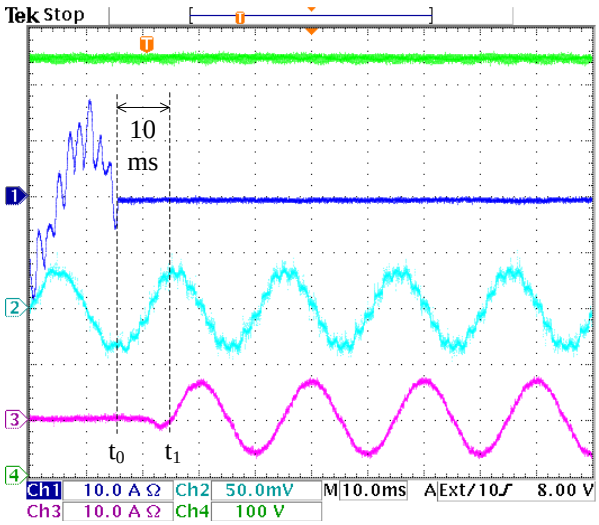


Fig. 4.31 Dynamic performance of the DSTATCOM Ch.1 (blue): passive filter current (10 A/div), Ch.2 (cyan): source current (50 A/div), Ch.3 (red): DSTATCOM current (10 A/div) and Ch.4 (green): DSTATCOM DC-bus voltage (100 V/div). Time scale: 10 ms/div.

4.6 Medium-Voltage Hybrid Compensator

In this section, the concept of the hybrid combination of a passive filter and a DSTATCOM is extended to the medium-voltage (MV) grid applications. Since design of the system is discussed previously, in this section, more emphasis is given on the suitability of the solution for loads with variable reactive power demand and connected to the medium-voltage grid.

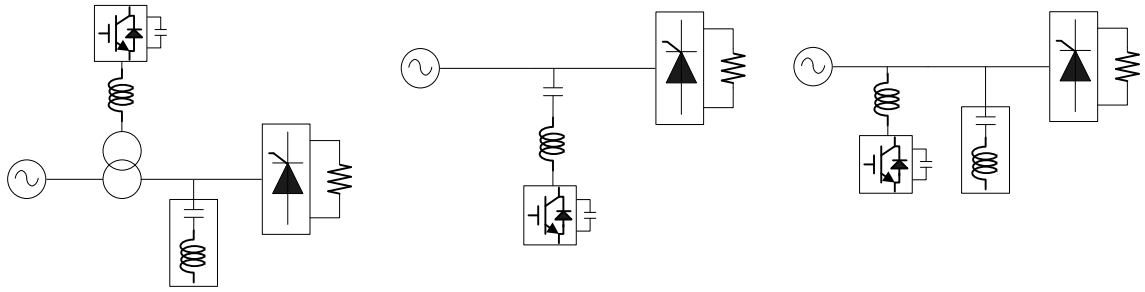


Fig. 4.32 (a) Shunt passive and series active filter (b) Parallel hybrid filter which is a series connection of a shunt passive and a shunt active filter, (c) parallel connection of a shunt passive and a shunt active filter.

There are many hybrid combinations of active and passive filters [57], the most common arrangements are (a) combination of shunt passive and series active filter (shown in Fig. 4.32 (a)), (b) parallel hybrid (series connection of shunt passive and shunt active filter, as shown in Fig. 4.32 (b)) and (c) parallel connection of shunt passive and shunt active filter (as shown in Fig. 4.32 (c)). Shunt passive and series active filters are more suitable for voltage fed type of loads [54], [57] and require transformers for connecting the active filter in series with the line. A Parallel hybrid filter leads to an advantage of reducing the voltage rating of the voltage source converter (VSC) working as a DSTATCOM. This advantage minimizes when the system is connected at distribution voltage level as discussed at the beginning of this chapter (since voltage is already less, current rating of VSC increases considerably, which makes this configuration non suitable at low voltage levels for high reactive power compensation requirements). However, at medium-voltage level, parallel hybrid filter can reduce voltage rating of the VSC. Let us assume that a 12-pulse rectifier supplying a 1 MW electrolyser load, as explained in the previous section. However, at the input side, the rectifier is connected to the 10 kV grid. With the same load, the minimum and maximum reactive power, required to keep the power factor greater than 0.98, remain the same, i.e. 275 kVA and 615 kVA, respectively.

A parallel hybrid filter controls the reactive power by changing the voltage applied by VSC thus controlling the voltage across the passive filter. The VSC voltage can be in-phase with the grid voltage or in-phase opposition of the grid. The minimum reactive power Q_{min} and maximum reactive power in terms of the passive filter reactance $X = \omega L - 1/(\omega C)$ are given as:

$$Q_{\min} = (V_s - V_c)V_s / X \tag{4.19}$$

$$Q_{\max} = (V_s + V_c)V_s / X \tag{4.20}$$

where V_c is line-to-line RMS AC voltage rating of the VSC and V_s is the grid voltage. For a parallel hybrid filter, the reactive power ratings of the passive filter Q_{fPH} and the VSC Q_{VSCPH} are given as;

$$Q_{fPH} = \frac{(V_s+V_c)^2}{X} = 2\frac{Q_{\max}^2}{Q_{\max} + Q_{\min}} \tag{4.21}$$

$$Q_{VSCPH} = \frac{(V_s+V_c)V_c}{X} = \frac{Q_{\max}(Q_{\max} - Q_{\min})}{Q_{\max} + Q_{\min}} \tag{4.22}$$

The values of reactive power ratings of the passive filter and the VSC come out to be 850 kVA and 235 kVA, respectively. The AC line-to-line RMS voltage rating of the VSC V_c in terms of grid voltage V_s is given as;

$$V_c = V_s \frac{Q_{\max} - Q_{\min}}{Q_{\max} + Q_{\min}} \tag{4.23}$$

With given parameters, it comes out to be 3.82 kV that means a two-level topology cannot be used for VSC; however, a multi-level topology can be employed.

The combination of a shunt passive and a shunt active filter proves to be advantageous for large and variable reactive power demand at the distribution-level voltage because the passive filter supplies a major portion of the reactive current (therefore VSC rating reduces considerably). At medium-voltage level, the VSC has to be rated for the full system voltage. 2-level or 3-level topologies with a transformer can be used. However, recently there has been a lot of research interest in modular multilevel converter topology (MMC) for medium-voltage applications. The MMC is suitable for medium-voltage power conversion due to easy construction, assembling and modularity. It provides advantages such as transformer-less grid connection, distributed capacitive energy storage, redundancy, and simple voltage scaling by

series connection of the modules. A MMC can be used as a VSC supplying reactive power in parallel combination of active and passive filters. The ratings of passive filter and VSC are given as;

$$Q_{fSH} = \frac{Q_{\max} + Q_{\min}}{2} \tag{4.24}$$

$$Q_{VSCSH} = \frac{Q_{\max} - Q_{\min}}{2} \tag{4.25}$$

The ratings of passive filter and VSC come out to be 445 kVA and 170 kVA respectively. VSC should be rated to the full system voltage i.e. 10 kV.

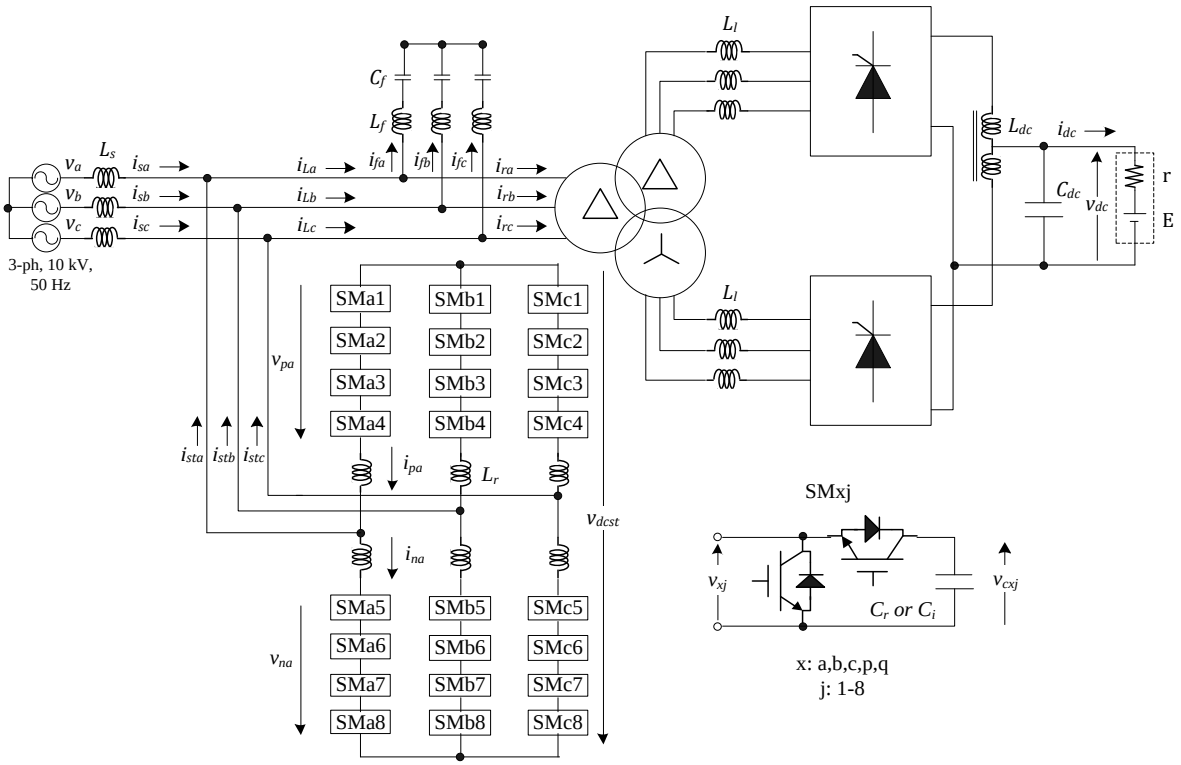


Fig. 4.33 12-pulse rectifier connected to medium-voltage grid with medium-voltage hybrid filter.

When comparing the two hybrid-filter configurations, it can be seen from (4.21), (4.22) and (4.24), (4.25) that the ratings of both passive filter and VSC are smaller for later combination (i.e. the combination of shunt passive and shunt active filter). Rating of the passive filter and the VSC for the parallel combination of the passive filter and the DSTATCOM come out to be 48% and 28% less than that of the configuration shown in Fig. 4.32 (b), respectively. Moreover, the advantage of voltage rating reduction in a parallel hybrid filter does not allow using 2-level topology with readily available 1200 V semiconductor devices. Therefore, the parallel

combination of a shunt passive filter and a shunt active filter clearly comes out to be the favorable combination for this type of applications, with variable reactive power demand.

Fig. 4.33 shows the system diagram of a hybrid-filter topology suitable for medium-voltage applications. The system consists of a dominant-harmonic passive filter along with a VSC working as a DSTATCOM. A Modular multilevel converter (MMC) topology with a suitable number of modules can be used to form the VSC. The DC-bus voltage can be selected based on the criterion described before. Apart from the internal modulation strategy of the converter, the control of the DSTATCOM remains similar as depicted in Fig. 4.4. The modulation strategy of the MMC and its design is discussed in detail in 6. Since other details of the hybrid filter system and its performance have already been discussed, further details are not presented, to avoid repetition.

4.7 Summary

In this chapter, passive and hybrid compensating techniques are discussed. It is shown, with the help of experimental system, that a dominant harmonic passive filter alone can improve the input current THD of 12-pulse rectifier without leading to resonance. The hybrid filter consists of a passive filter and a DSTATCOM. The main motive behind using a hybrid set-up was to reduce the DSTATCOM rating while maintaining the required power factor over a load range. Choices, such as DSTATCOM is used to supply only reactive power, have been instrumental in reducing losses by reduction in switching-frequency. System and control design has been discussed in detail and simulation and experimental results showing the effectiveness of the system. The power factor is maintained greater than 0.98, as required. As specified, at full load current THD of less than 5 % is achieved. Although, the power factor is maintained greater than 0.98, if required, the system can be designed to achieve unity power factor; however, with higher rating of compensators.

5. Chopper-Rectifier

Chopper-rectifier is the most advanced topology that is put in industrial use for high-current variables-voltage applications. Therefore, it is necessary to discuss this topology in detail and make a comparison with the proposed hybrid filter-based solution. Thus in this chapter, first the performance of a chopper-rectifier is discussed along with experimental results. Afterwards, a comparison of chopper-rectifier and thyristor rectifier with hybrid filter is carried out in terms of power quality, size, efficiency and cost.

5.1 12-Pulse Three-Phase Chopper-Rectifier

Chopper-rectifiers have been put to the use for electrolysers and DC arc furnaces up to 10-30 MW power level. Fig. 5.1 shows a typical circuit configuration of a chopper-rectifier consisting of a 12-pulse diode-rectifier and a three-phase chopper unit. The choice of a 12 or 24-pulse rectifier unit depends on the power level and required THD of the input current. To control the output current, a 3-phase chopper is utilized. A multi-phase chopper utilizes interleaving principle leading towards reduction of output filter requirement. The choice of the number of interleaved (multi-phase) chopper units also depends on the power level and availability of required rating of switches. However, higher number of interleaved units result in increased control complexities, therefore, many switches are paralleled together to keep the number of interleaved units low. For higher power applications, multiple units of a chopper-rectifier can also be used in parallel. The selection of switching frequency affects the size of filter inductors, losses and current ripple. The minimum value of intermediate DC link voltage (rectifier output voltage) is selected based on minimum grid voltage, line voltage drop, maximum output voltage and maximum duty ratio of chopper-section. However, this minimum value of intermediate DC link voltage may not be the optimum value of the voltage in terms of the overall losses. For high-current applications, as the intermediate DC link voltage is increased, current in the front end rectifier reduces, therefore, reducing the conduction losses in the rectifier stage. In chopper-stage, higher input voltage results in higher switching losses, higher magnetic losses (due to current ripple in output inductors). Therefore, an optimum intermediate DC link voltage can be

reached, which provides minimum losses. Based on these considerations and design equations provided in text books and key references [14]-[17], [28]-[32], the design of a chopper rectifier is carried out for 1 MW load (as specified in the previous chapter). The key circuit parameters are furnished in Table 5.1.

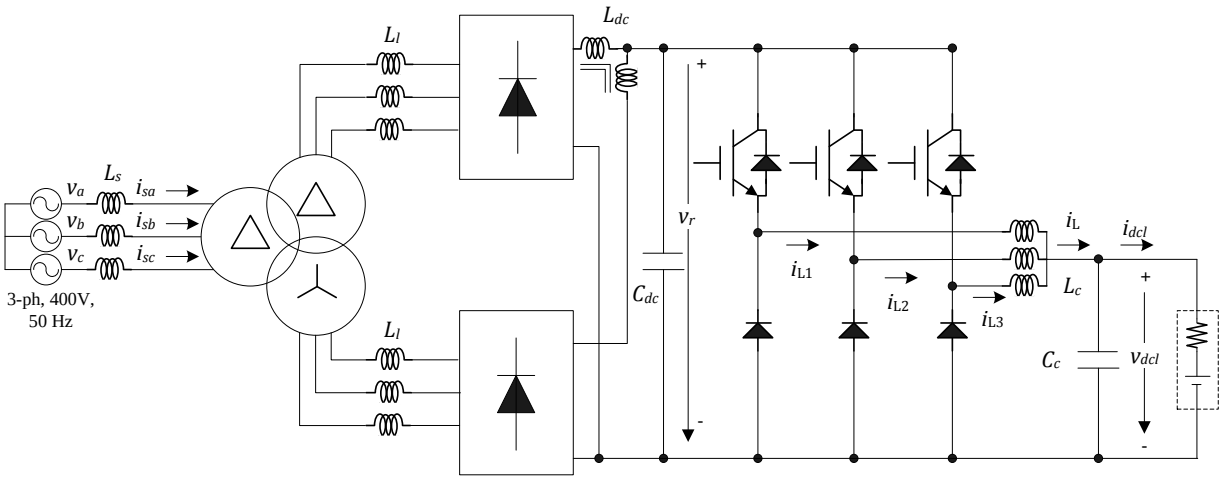


Fig. 5.1 Basic block diagram of 12-pulse three-phase chopper-rectifier.

Table 5.1 System parameters

Source	3-ph, 400 V, 50 Hz, L_s=20 µH
Transformer	1000 kVA, Dd0y1, 400 V/235.5 V, X_l=6 %
Rectifier	C_{dc}=8000 µF, L_{dc}=45.63 µH
Chopper	3-phase, f_s=1 kHz, L_c=96 µH, C_c=2100 µF

5.1.1 Simulation Results

The chopper-rectifier circuit, with above mentioned parameters, is simulated using MATLAB Simulink and PLECS block-set. Simulation is carried out using ode15s (stiff/NDF) solver with a maximum step size of 1×10^{-6} s and relative tolerance of 1×10^{-4}. Fig. 5.2 (a) and (b) show the waveforms of the key quantities at top load line (refer to Fig. 4.1) with full load current. The input current, shown in Fig. 5.2 (a), represents typical 12-pulse diode rectifier current. The output voltage and current shown have ripples of 4 V (1.8 %) and 200 A (4.4 %), respectively. The inductor currents are well balanced as shown in Fig. 4.2 (b) and because of interleaving operation, the ripple in the cumulative current i_L is significantly reduced as compared to the individual inductor currents. The variation of the power factor with load current, over top and bottom load lines, is shown in Fig. 5.3. Due to the front-end diode rectifier, the power factor remains above 0.97 for a considerable range of load current variation. This is one of the

important advantages of using a chopper-rectifier. Moreover, if an even higher power factor is desired, a passive filter can be added on the AC side. The variation of input current THD is shown in Fig. 5.4, indicating the 12-pulse diode rectifier performance again. A passive filter can also help in reducing the current harmonics thus reducing the THD.

In the later section of this chapter, a comparison is carried out between chopper-rectifier and thyristor rectifier to fulfill a given set of specifications. To meet the THD and power factor specification, a dominant-harmonic passive filter is added with the chopper-rectifier. Further details like efficiency, size and cost of the chopper-rectifier with passive filter are discussed in later sections.

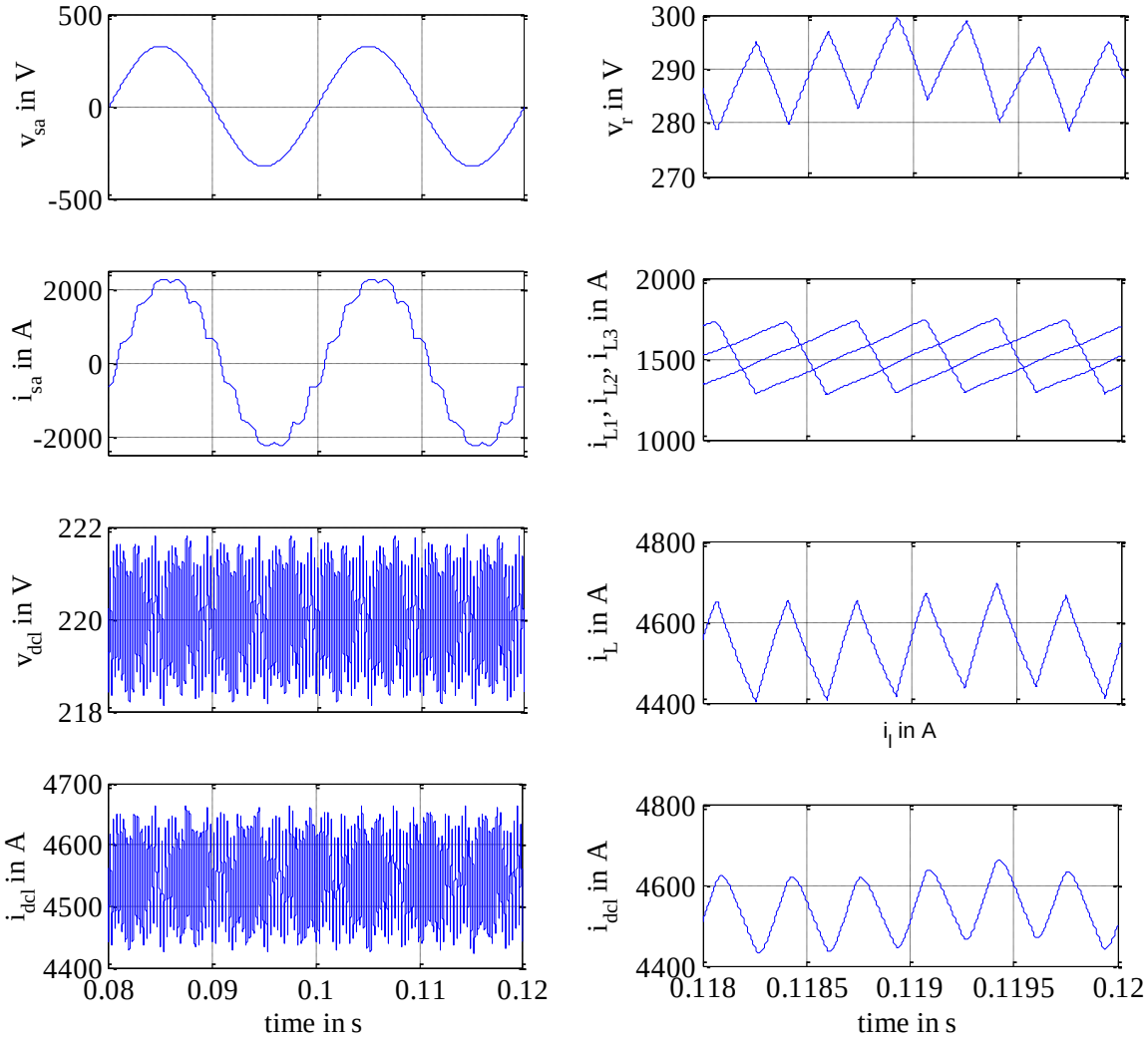


Fig. 5.2 Simulated performance of chopper-rectifier.

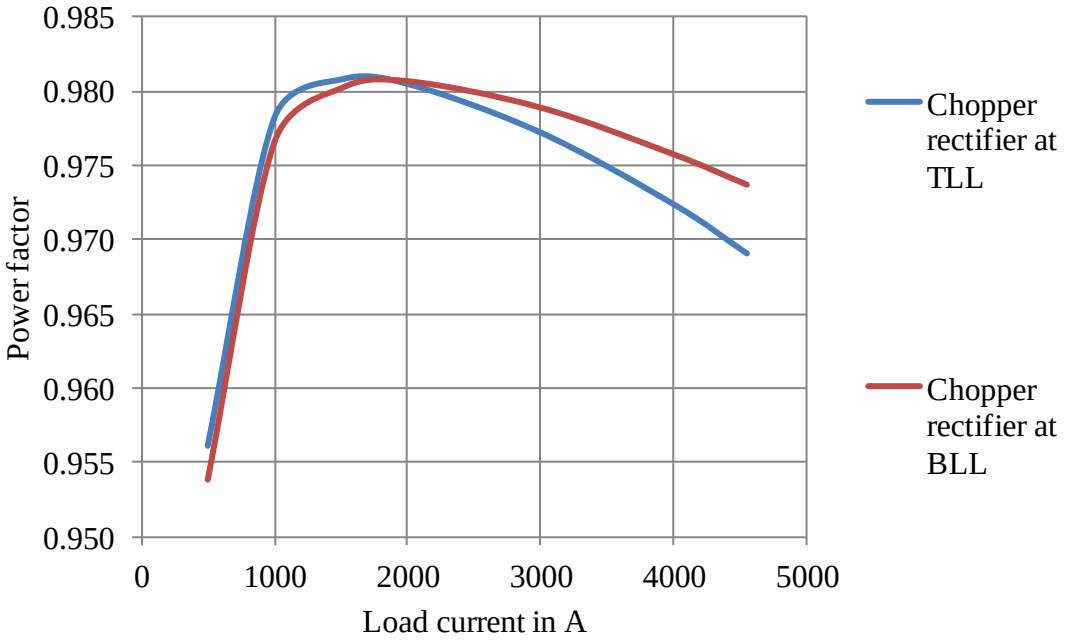


Fig. 5.3 Simulated variation of input power factor over the top and bottom load lines with 1 MW chopper-rectifier.

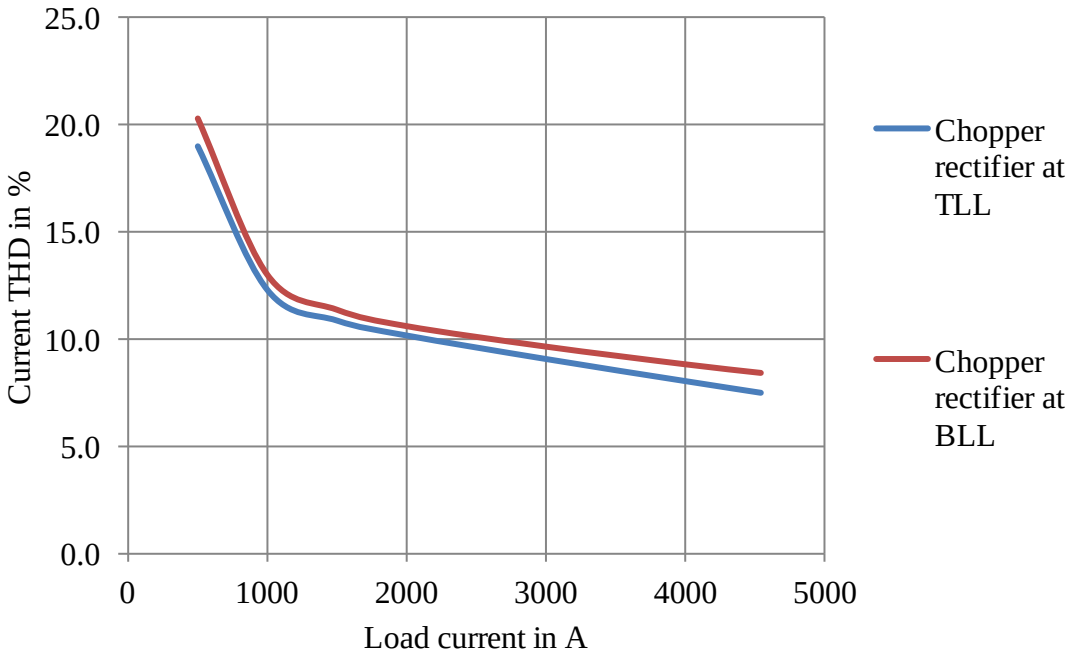


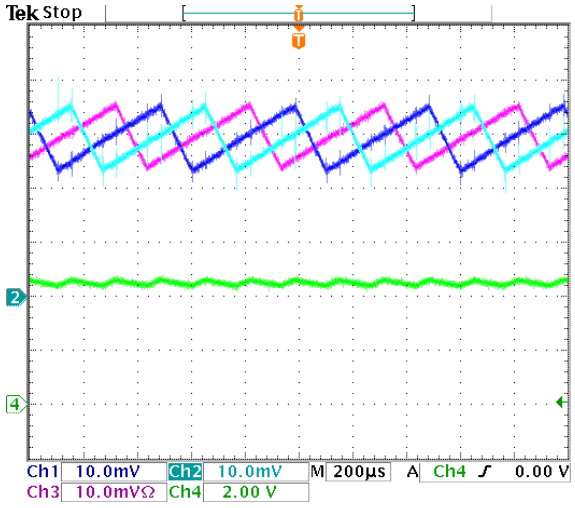
Fig. 5.4 Simulated variation of input current THD over the top and bottom load lines with 1 MW chopper-rectifier.

5.1.2 Experimental Results

The experimental set-up used to implement the hybrid filter (as explained in the previous chapter) is modified to evaluate the behavior of a chopper-rectifier. Utilizing previous set-up to

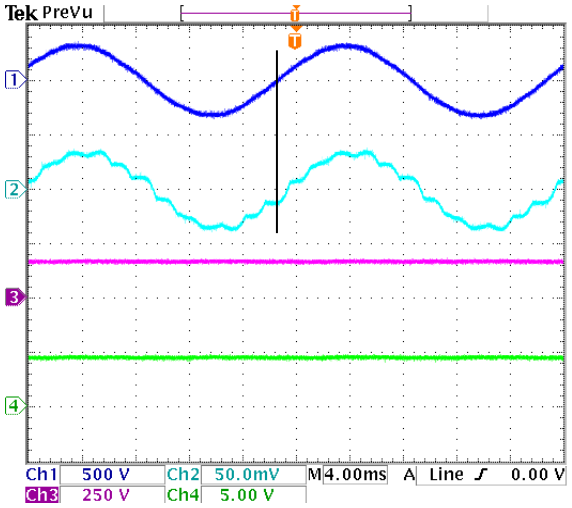
implement chopper-rectifier leads to some compromises; however, this was the only option available because of some non-technical issues. Since the rated output voltage of the 12-pulse rectifier system is 220 V, this becomes the input voltage for the chopper-section. At the top load line (TLL), the rated load voltage stands at 220 V that cannot be achieved with the present hardware system due to finite voltage drop in the chopper-section. Therefore, on the top load line, this experimental chopper-rectifier set-up cannot operate for a load current higher than 60 A. Nevertheless, operation of the chopper-rectifier can be studied over the complete bottom load line (BLL). The converter unit from SEMIKRON (used previously as a DSTATCOM) is used to form the three-phase chopper-section. Three dual IGBT blocks having anti-parallel diodes, constitute the chopper switches with gate drives of top IGBTs disabled. Since it is a scaled-down version as compared to 1 MW unit, the switching frequency of the chopper unit is selected to be 2 kHz. With 1.77 mH chopper inductors (as available in the stock) the current ripple in the individual units is estimated to be 17 %. A DC link capacitor of 60 μF (Siemens B43441-A4606-T) is used at the load side to reduce the load voltage ripple. At the output of the diode-rectifier, 2.1 mH inductor and 3.1 mF capacitor are used as a filter (inductor and capacitor as existing from previous setup).

Fig. 5.5 (a) shows the current waveforms in the chopper-section at the BLL with rated load. The figure demonstrates the sharing of currents in the three interleaved units along with the total current. The cumulative current has considerably reduced ripple due to the interleaving. The input and load voltages and currents are shown in Fig. 5.5 (b). At this point of operation (BLL with rated load current), the power factor turns out to be 0.977 with an input current THD of 9.3 %. The grid voltage stands at 395 V and the rectifier output voltage remains 219 V. The values of the input and output power turns out to be 16.29 kW and 14.8 kW, respectively. Variation of the power factor over the load range is shown in Fig. 5.6. As stated before, tracing the TLL above 60 A of the load current has not been possible. However, the power factor curve for TLL is expected to be similar to that of BLL due to the front-end diode rectifier. The power factor remains higher than 0.97 for 30-100 % load current approximately. Variation of the input current THD is shown in Fig. 5.7. As expected the current THD remains to be less than 10 % at the rated load and increases upto 20 % at light load conditions.



(a)

Ch.1 (blue), 2 (cyan) and 3 (red): inductor currents (i_{L1}, i_{L2}, i_{L3}) in the chopper-section (10 A/div) and Ch. 4 (green): total output current of chopper-section before filter capacitor i_L (40 A/div). Time scale: 200 µs/div.



(b)

Ch.1 (blue): input grid voltage v_a (500 V/div), Ch.2 (cyan): source current i_{sa} (50 A/div), Ch.3 (red): load voltage v_{dcl} (250 V/div) and Ch.4 (green): load current i_{dcl} (100 A/div). Time scale: 4 ms/div.

Fig. 5.5 Performance of chopper rectifier at BLL with rated current.

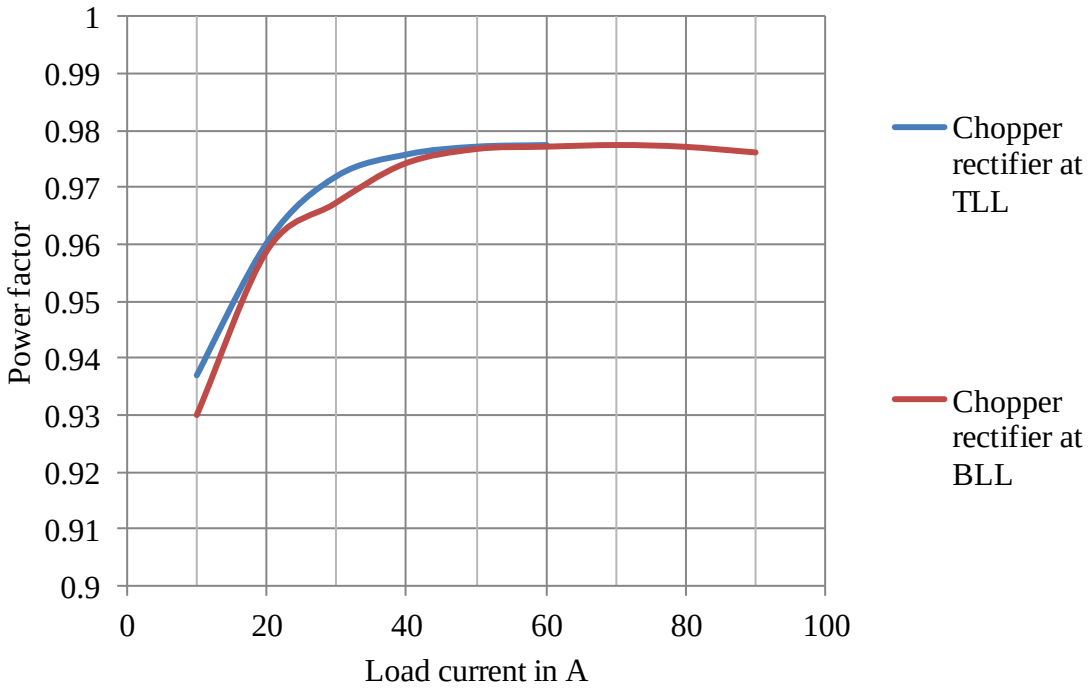


Fig. 5.6 Variation of PF for chopper rectifier over the top and bottom load lines.

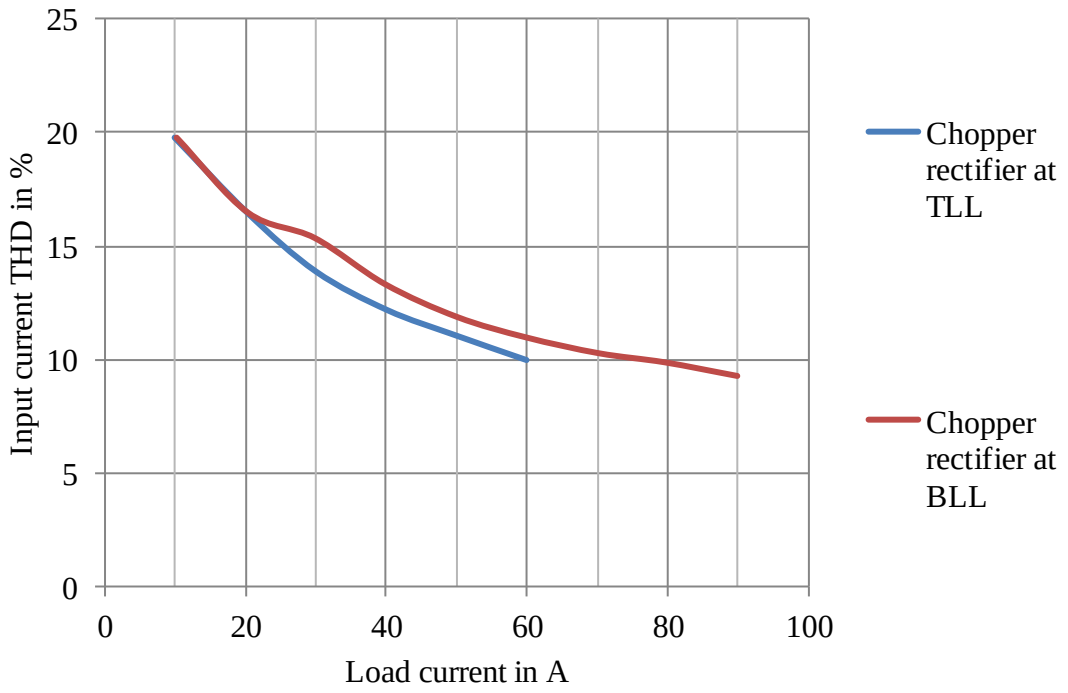


Fig. 5.7 Variation of input current THD for chopper rectifier over the top and bottom load lines.

5.2 Comparison of Thyristor-Rectifier with Hybrid Filter and Chopper-Rectifier for High-Current Variable-Voltage Application

The qualitative comparison of thyristor rectifier and chopper-rectifier has been discussed in literature [1], [2]. However, a comprehensive and quantitative comparison for an industrial load with a precise set of specifications has not been discussed.

This section compares the 12-pulse thyristor rectifier with hybrid filter (TRHF) and 12-pulse diode rectifier with passive filter followed by multi-phase chopper (CRPF) [D]. The performance of two rectifier systems is evaluated for supplying power to a 1 MW high-power high-current industrial load with certain input and output power quality specifications. Both systems are designed to meet a set of performance criteria and then compared in terms of efficiency, size and cost.

5.2.1 System Specifications

Comparison of the two rectifier systems is carried out to feed the load as specified in section 4.2 and Fig. 2.2. The requirements/specifications of the equipment are given in Table 4.1 and design of the rectifiers is carried out according to these system requirements.

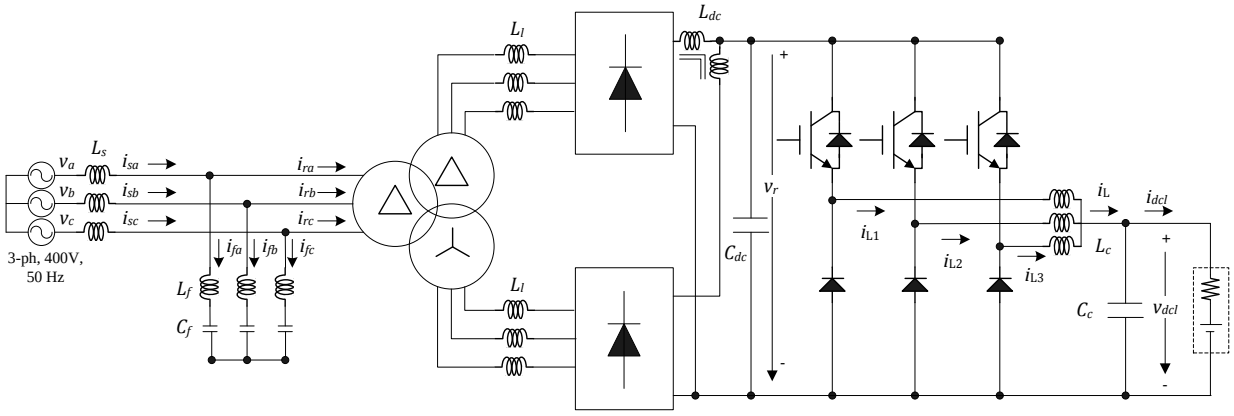


Fig. 5.8 Basic block diagram of 12-pulse diode rectifier with three-phase chopper and 11th harmonic input passive filter (CRPF).

Table 5.2 System Parameters

TRHF	**CRPF**
Source: 3-ph, 400 V, 50 Hz, L_s=10 µH	Source: 3-ph, 400 V, 50 Hz, L_s=20 µH
Transformer: 1000 kVA, Dd0y1, 400 V/172 V, X_l=6 %	Transformer: 1000 kVA, Dd0y1, 400 V/235.5 V, X_l=6 %
Rectifier: L_{dc}=45.63 µH, C_{dc} =8000 µF (FFLI6B1007K by AVX 8 in parallel), Thyristor current: 757 A, TZ800N12KOF by Infineon (2 in parallel)	Rectifier: L_{dc}=45.63 µH, C_{dc} =8000 µF (FFVE6K0107K by AVX, 10 in parallel), diode current: 560 A, DD600N12KOF by Infineon (2 in parallel)
DSTATCOM: 170 kVA, f_s=5 kHz, L_{st}=0.55 mH, C_{dcst}=1600 µF (FFLC6L1607K by AVX), V_{dcst}=750 V, switch voltage and current: 750 V and 60 A, IGBT: FF100R12YT3 by Infineon	Chopper: 3-phase, f_s=1 kHz, L_c=96 µH, C_c=2100 µF (FFLI6B2407K by AVX), switch voltage and current: 300 V and 1120 A, FD600R06ME3 by Infineon (4 in parallel)
Passive filter: 445 kVA, C_f=8780 µF (2GCA280774A0030 and 2GCA280780A0030 by ABB), L_f=9.54 µH, Q=30	Passive filter: 70 kVA, C_f=1392 µF (MKK400-D-20-01 B25667C3397A375 and B25669A3996J375 by Epcos), L_f=60 µH, Q=30

5.2.2 12-Pulse Thyristor Rectifier with Hybrid Filter (TRHF)

Design, control and performance of the 12-pulse thyristor rectifier with hybrid filter (TRHF) were already discussed in Chapter 4. Fig. 4.2 shows the system configuration. The design of the system is carried out to fulfill the requirements provided in Table 4.1. Table 5.2 provides various system parameters of the TRHF system. Selection of semiconductors is carried out depending on the next safe voltage rating commercially available and a ~100 % current margin is maintained for average current rating. Commercially available capacitors are used with closest safe voltage

and RMS current ratings. Magnetic components are designed using the standard design procedures as explained in Appendix B and reference [19], [20].

5.2.3 12-Pulse Diode Rectifier followed by Chopper (CRPF)

Fig. 5.8 shows the system configuration. The design of the system is carried out to fulfill the requirements provided in Table 4.1. Because of the front end 12-pulse rectifier configuration the displacement power factor (DPF) of the system ideally remains to be unity. However, due to the leakage inductance and transformer magnetizing current, the DPF is below unity (approximately 0.96-0.97 as shown in Fig. 5.3). Moreover, due to the distortion factor, the power factor of the system reduces further at light load conditions. To deal with this problem an 11^{th} harmonic filter is added to reduce the current THD and improve the power factor by supplying a small amount of reactive power. Table 5.2 provides various system parameters of the rectifier system. Selection of semiconductors and other components is carried out employing the same criteria as explained in the previous section.

5.2.4 Comparison

The comparison of the two systems is carried out for supplying power to the load specified by eq. (4.1) and (4.2) and meeting the specification provided in Table 4.1. The comparison is carried out in term of performance, efficiency, size and cost.

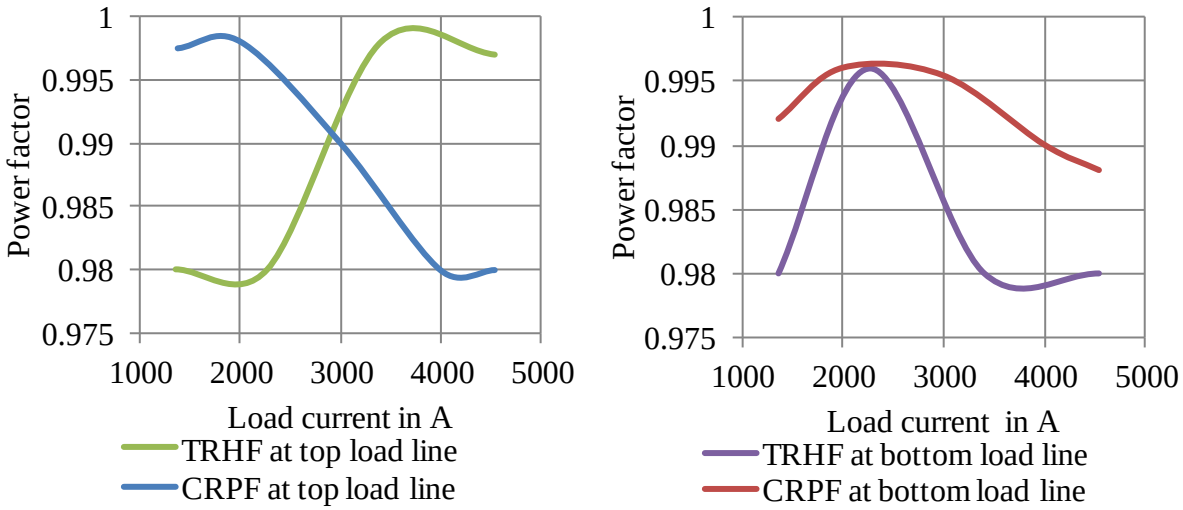


Fig. 5.9 Variation of input power factor of TRHF and CRPF at top and bottom load lines.

5.2.4.1 Power Quality

Fig. 5.9 (a) and (b) show the variation of the power factor (PF) of the two topologies along the top and bottom load lines. It can be observed that with the help of appropriate reactive power compensation, the two systems are able to meet the requirement i.e. PF≥ 0.98. Variation of the input current THD is depicted in Fig. 5.10 (a) and (b). It can be seen that due to the bigger (higher reactive power rating) passive filter, the TRHF provides better harmonic cancellation characteristics. Also, with CRPF at light load, the current THD becomes marginally higher than 5 % limit.

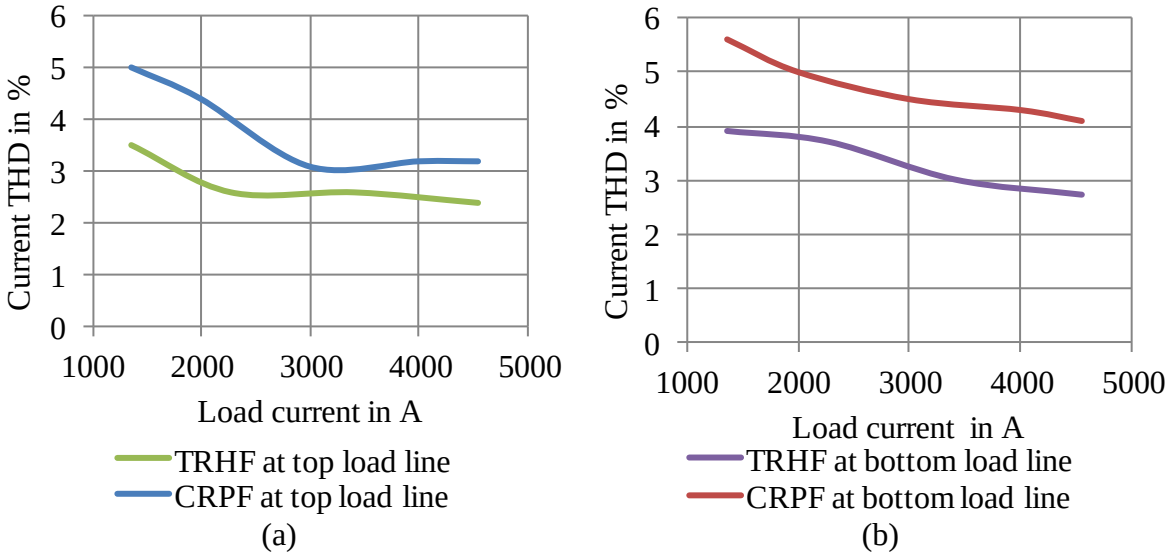


Fig. 5.10 Variation of current THD of TRHF and CRPF at top and bottom load lines.

5.2.4.2 Efficiency

The comparison of estimated system level efficiencies is shown in Fig. 5.11 (a) and (b). The semiconductor losses are estimated using parameters from the datasheets and MATLAB and PLECS simulation models. PLECS utilizes forward characteristics to compute the instantaneous conduction losses that are averaged over the cycle to compute the average conduction loss. For switching loss computation, the energies involved at turn on and off processes with respect to device current and voltage (as provided in the data sheet) are added over a period of unit time. The data is inputted corresponding to the maximum junction temperature; therefore, the estimated semiconductor losses are pessimistic. For more details please refer to Appendix A. The magnetic losses are determined using standard design equations [19], [20].

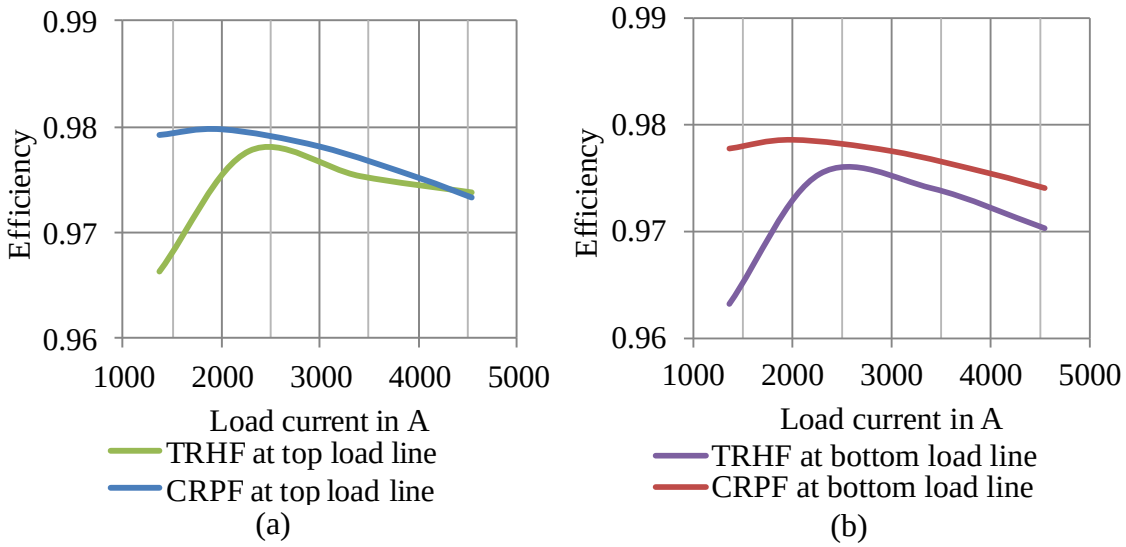


Fig. 5.11 Variation of estimated efficiencies of TRHF and CRPF at top and bottom load lines.

For low-voltage high-current applications the CRPF appears to be the clear winner. However, at top load line under full load condition, the efficiencies of two systems are fairly close. To investigate the reasons behind poor efficiency of the TRHF, one needs to look at the contribution of different system components to the power losses. Fig. 5.12 shows the distribution of losses. The largest contributors to the losses of TRHF are thyristor conduction and transformer losses. For high-current low-voltage applications, the choice of thyristor versus diode makes a significant difference. For low-operating currents and at higher-operating voltages, the losses of the chopper-section tend to offset this difference. However, at higher currents, thyristor conduction losses become dominant enough leading to lower efficiencies. As far as the transformer losses are concerned, it can be optimized for particular topology and application. However, to make a fair comparison, here the transformer material (CRGO M6, 0.3 mm lamination thickness), the flux density (1.5 T) and the current density (4 A/mm^2) are kept constant. Keeping these parameters constant, the full load efficiency (neglecting losses due to harmonics) of the transformer used for CRPF is slightly better than that of TRHF for the same transformer size (98.55 % for TRHF and 98.75 % for CRPF). If one wants to make transformer efficiencies equal for the two rectifier systems, the overall difference between efficiencies of the CRPF and TRHF can be reduced. Moreover, around rated current at top load line, the efficiency of TRHF becomes marginally higher than CRPF. Large-current-rectifier transformers have higher copper losses and merely 10-15 % iron losses. This explains the behavior of efficiency curves shown in Fig. 5.11 with peak system efficiency occurring at relatively lighter loads. Other

dominant contributors to the losses of TRHF are the passive filter and the DSTATCOM. Due to the DSTATCOM action there is a significant dip in the system efficiency of TRHF at light load condition.

In case of the CRPF, the semiconductor losses occurring in the chopper-section leads to a significant amount of losses apart from the transformer and the diode rectifier losses. To maintain low semiconductor losses, the switching frequency of the chopper section is kept low (1 kHz). Losses in the output inductor are also significant at 6.2 % and 8.5 % at the rated load current operations at the top and bottom load lines respectively. Losses in various capacitors are found to be negligible hence not included.

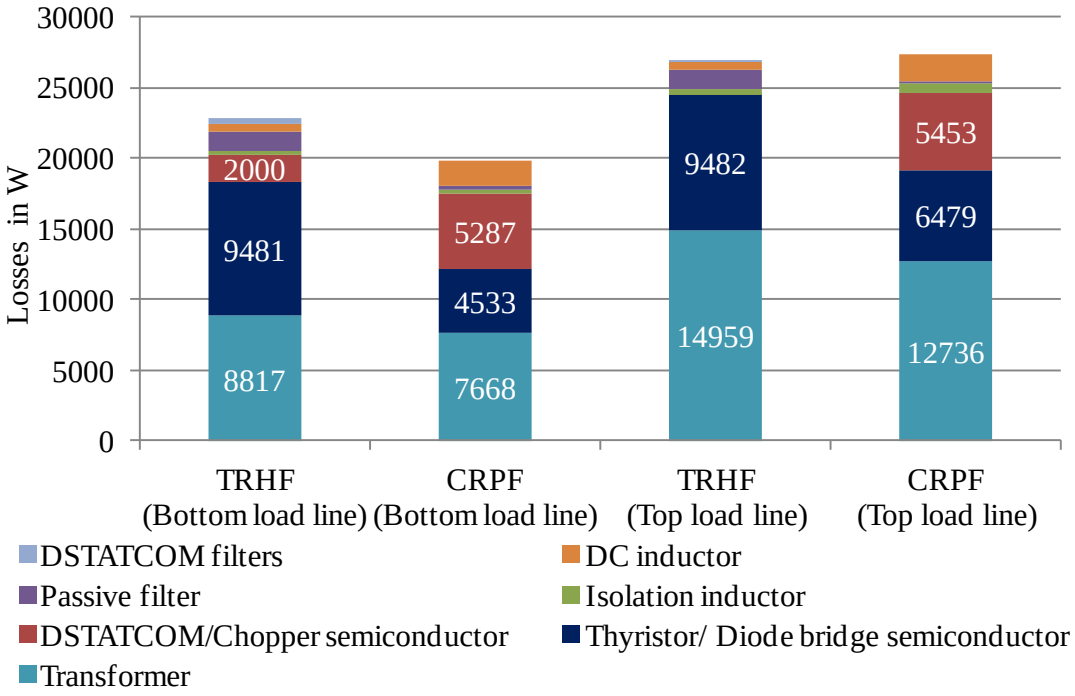


Fig. 5.12 Distribution of estimated losses of different components used for TRHF and CRPF.

5.2.4.3 Size

A comparison of the estimated volumes of the two considered rectifier systems is shown in Fig. 5.13. The volumes of the selected components are calculated with the help of dimensions provided in the datasheets. The biggest contributors to the size of a circuit are magnetic components (especially for low frequency operations). Here too, transformer and filter inductors are the main contributors to the size of the system. As discussed in the previous section, size of the transformer is almost same for the two topologies. However, sizes of the AC and DC

inductors are bigger for CRPF. But this difference in the inductor sizes is offset by the AC capacitor used for passive filter of TRHF. This leads to the overall bigger size of TRHF as compared to CRPF. Size of the cooling system is not considered.

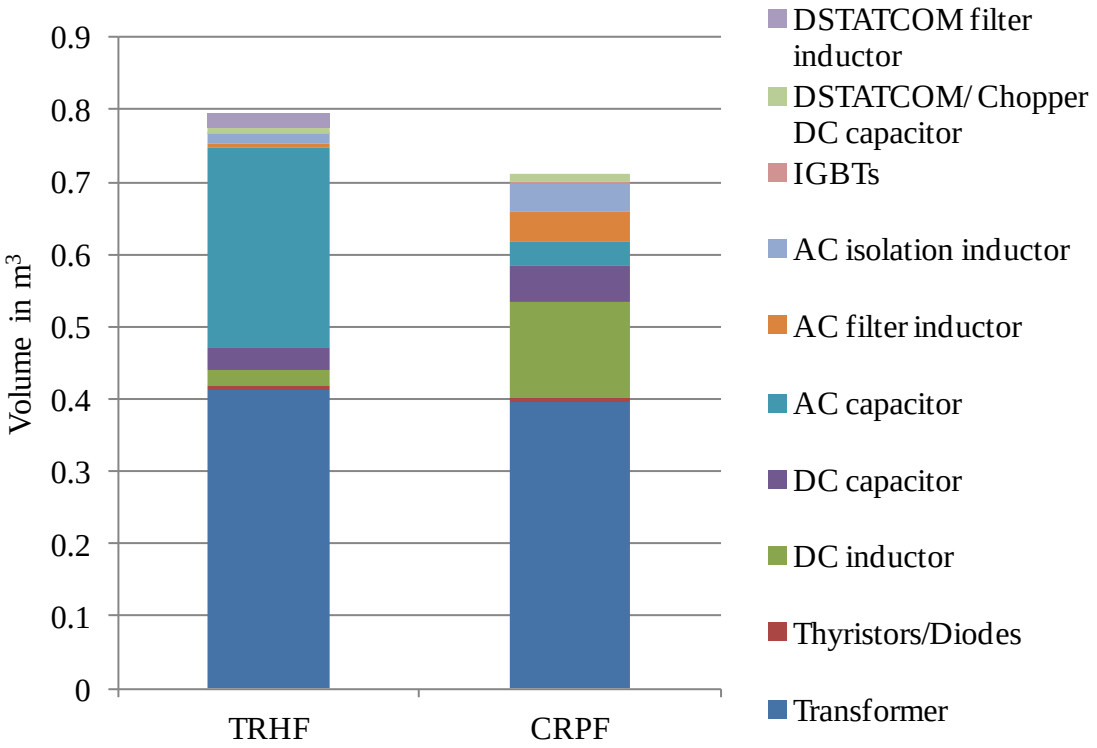


Fig. 5.13 Estimated size of different components used for TRHF and CRPF.

5.2.4.4 Cost

The dominant part of the cost of the system comes from magnetic components. In this case the largest component comes from transformer. Since the transformer used for TRHF is slightly bigger than that of CRPF, cost of the former will be marginally higher. To compare the cost of the filter inductors, peak energy ratings can be compared (at the same operating frequency). The cumulative peak energy ratings of the line-frequency inductors are 173.6 J and 126.8 J for TRHF and CRPF, respectively. Whereas, DC side inductors ratings for the TRHF and the CRPF are 140.5 J and 475.45 J, respectively. Another more accurate way to estimate the cost is to compare the iron and copper weight. Estimated iron and copper weight of various inductors used for the TRHF are 205 kg and 122 kg, respectively. Cumulative iron and copper weights of the inductors used for the CRPF stand at 491.7 kg and 242.5 kg, respectively. Therefore, the material cost of the inductors will be more than double in case of CRPF as compared to TRHF. For comparison of the semiconductor cost, one needs to estimate the VA ratings of the semiconductor switches.

Table 5.3 provides an overview of installed VA ratings of the semiconductor switches. However, actual market price of the semiconductor switches depends on many other factors apart from VA rating, such as, production volume, demand and availability etc. Because of these reasons, normally a dual IGBT leg is priced less as compared to a chopper leg of the same rating. Thyristor modules are priced higher than diode modules of similar rating. Apart from these, cost of DC and AC capacitors is the remaining major part. Since both AC and DC capacitor ratings are higher in case of TRHF, cost of the same will also be higher.

Table 5.3 Total ratings of semiconductor components

Semiconductor components	Rating in MVA	
	TRHF	CRPF
Thyristors or Diodes	23.04	17.28
IGBTs and Diodes	1.44	8.64

5.3 Summary

Two topologies of rectifier system, thyristor rectifier with hybrid filter and chopper-rectifier with passive filter are compared for feeding to a high-power (1 MW) high-current (4.5 kA) load with a set of specifications. The two systems are designed to meet certain power factor, input current THD and output voltage and current ripple requirements. The analysis shows that the CRPF provides better efficiency compared to the TRHF. This is because of the dominant thyristor conduction losses for low-voltage and high-current applications as compared to losses in diode-rectifier and chopper-section. Hybrid filter losses also contribute to lower efficiency of the TRHF, especially when the DSTATCOM starts operating to improve the power factor. However, this depends on the type of load. For load with relatively lower-current at higher operating voltages and lighter filter requirements, TRHF can provide better efficiency. The size of the TRHF is higher than the CRPF due to the bigger input passive filter. Costs of the two systems have also been compared. Two circuits found to have almost same transformer cost; however, TRHF have higher cost of AC and DC capacitors. Magnetic cost component is expected to be higher for CRPF at the selected frequency. However, as the switching frequency of the chopper section is increased, magnetic cost comes down at the expense of higher losses. Therefore, efficiency, cost and volume are interlinked parameters. There is always a possibility to improve on one parameter by negatively affecting the other.

6. Medium-Frequency Transformer-Based High-Power High-Current Power-Supplies

In the previous chapters, rectifier systems connected to the low-voltage (LV) distribution-grid were studied. As the power rating of the load increases more than a few MWs, the rectifier is connected to a medium-voltage (MV) grid. Both, thyristor rectifiers and chopper-rectifiers use either a separate MV to LV transformer or an appropriately rated rectifier transformer, for connection to the MV grid. Passive-harmonic filters can be directly connected to the medium-voltage grid. As discussed in section 4.6, active devices like the DSTATCOM can be connected to the MV grid via a transformer or an appropriate topology can be chosen for direct connection. However, the techniques, discussed in the previous chapters, continue to use bulky magnetic components that add to losses and weight.

The challenges remain in coming-up with a compact converter topology with good power-quality and reasonable efficiency. Topologies used for generating low-power DC cannot be directly employed for high-power high-current applications because of the high-input voltage and high-output current. However, appropriate converter topologies can be used to form a power-supply with a medium-voltage rectifier followed by a medium-voltage medium-frequency inverter, an isolating transformer and a rectifier. A 2-level converter with series-connected semiconductor devices, a neutral point-clamped multi-level converter, and a flying capacitor converter are discussed in the literature for medium-voltage applications [67]. A 2-level converter with series connected devices leads to unequal voltage sharing between the semiconductor devices and reliability issues. Neutral-clamped multi-level converters, with more than 3-levels, become increasingly complex due to the required number of diodes [67]. Similarly, for medium-voltage level applications, a high number of capacitors are required to realize a flying-capacitor multilevel converter [67]. Recently, there has been a lot of research interest in modular multilevel converter (MMC) for high-voltage high-power applications [68]-[71]. The MMC is suitable for operation at medium/high voltage levels due to simple construction, easy assembling and modularity. It provides advantages, such as, transformer-less grid connection, distributed capacitive energy storage, redundancy and simple voltage scaling by series connection of

modules. There exist different configurations of MMC, namely, double star configuration using chopper cells (concept was first introduced by Marquardt [68]) and star connected configuration using full bridges (also known as cascaded converter). So far, the inverter and rectifier mode of operation and control (PWM control, fundamental frequency switching) have been discussed in the literature [68]–[74].

In the present chapter, two circuit configurations are studied for providing AC to DC conversion. These configurations are suitable for direct connection to the MV AC grid. Both configurations utilize the MMC concept for the rectification from MV AC to MV DC. This DC voltage is again inverted but at medium-frequency (MF) AC. With the help of medium-frequency transformer/transformers followed by diode rectifier/rectifiers, the required low-voltage DC is produced. The two circuit configurations utilize different levels of modularity and can be applied in different scenarios. Because of the input-stage active-rectification, the configurations achieve a very good input power factor and low current THD. Similarly, the inverter stage leads to very good control over output voltage and current, with low output voltage and current ripples. These topologies incorporate MF transformers that lead to reduced weight and volume of the overall system. In this chapter, the circuit configuration, design, control and performance of these topologies are discussed. Although the power supplies are connected to the medium-voltage (10 kV) grid, the load profile is assumed to be the same as discussed in the previous chapter (Fig. 4.1), in order to draw easy inferences between the approaches discussed in this chapter and the previous configurations.

6.1 MMC-Based Power-Supply utilising Central MF Transformer and Output Rectifier

This section proposes a power-supply based on the modular multi-level topology, as shown in Fig. 6.1 [F]. The power-supply is connected to the medium-voltage (MV) grid. A modular-multilevel rectifier is used to convert MV AC to MV DC. Medium voltage DC is inverted back to a medium-voltage, medium-frequency AC voltage. With the help of a medium-frequency transformer, the voltage is stepped-down. Finally, a diode-rectifier is used to feed the low-voltage high-current DC load. This architecture provides unique advantages in terms of an excellent input power quality (low current THD and unity power factor), removal of bulky line-frequency transformer and improved control over output voltage and current. Moreover, the power-supply uses modular components. The complete design and control of the power-supply

are discussed in section 6.1.1 and 6.1.2. Simulation of the system is carried out in the MATLAB/PLECS environment and results are presented to demonstrate the effectiveness of the system (section 6.1.3). Efficiency and volume estimation are presented in section 6.1.4, 6.1.5, respectively.

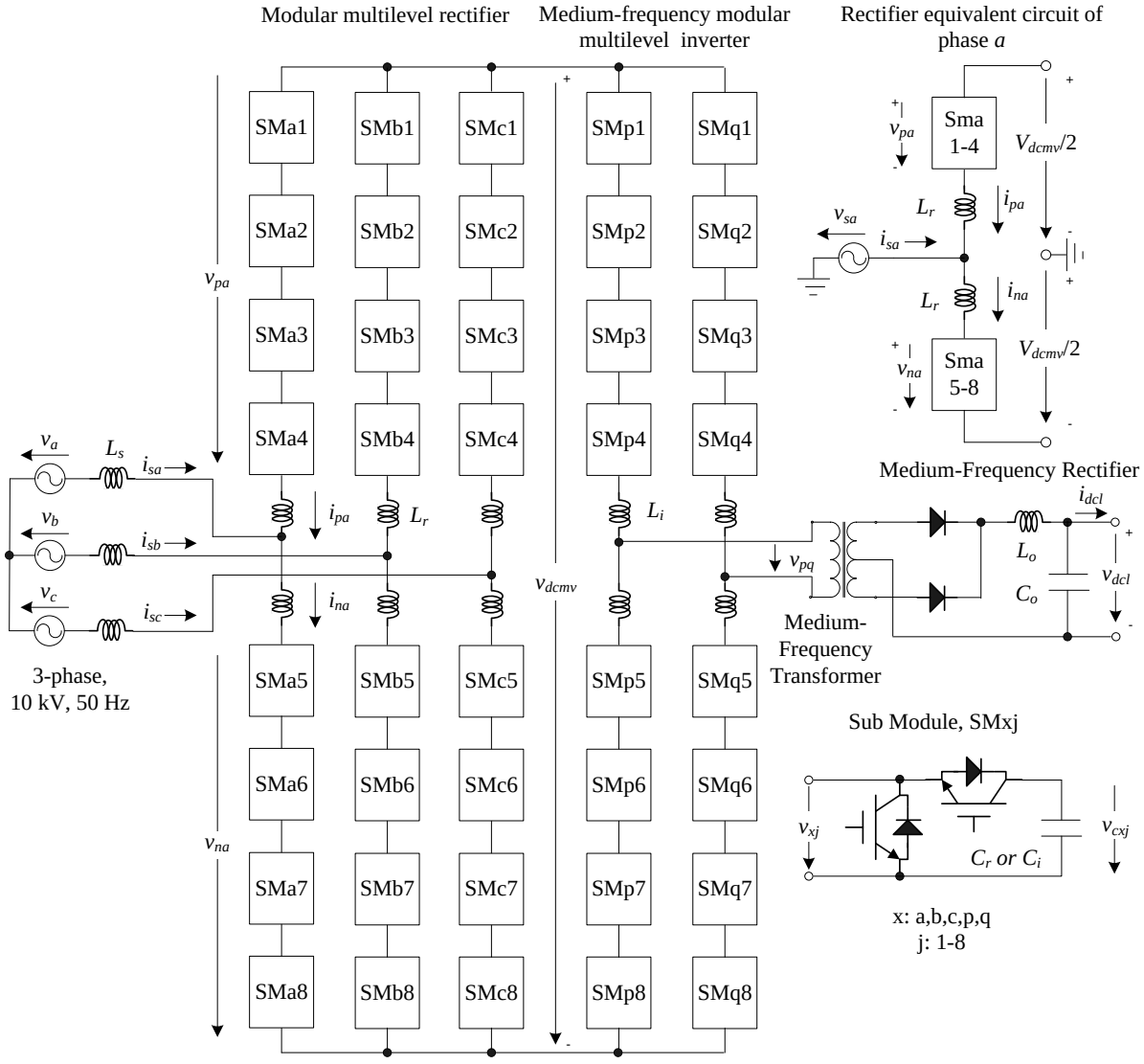


Fig. 6.1 Block diagram of the MMC-based power-supply with central transformer and rectifier.

6.1.1 System Design

The circuit diagram of the proposed power-supply is shown in Fig. 6.1. Characteristic of a considered 1 MW industrial load is shown in Fig. 4.1. As explained in section 4.1, variation of the load current is from 0 to 4545 A and the load voltage varies from 150 V to 220 V.

Input line-to-line voltage is 10 kV and the medium-voltage DC-link (MVDC) voltage v_{dcmv} is kept at 18 kV. As shown in Fig. 6.1, there are four sub-modules per arm of the modular-multilevel rectifier and inverter. Therefore, the capacitor voltage v_{cxj} (where *x*=*a*, *b*, *c*, *p* and *q* and *j*=1 to 8) of each sub-module (SM) is regulated at 4.5 kV. The switching-frequencies of rectifier and inverter, f_{sr} and f_{si} respectively, are selected as 1 kHz to achieve moderate switching losses. At the output stage, a center-tapped medium-frequency transformer followed by a rectifier is used. Various system parameters are provided in Table 6.1.

Input phase voltages in terms of angular frequency $\omega = 2\pi f$ and peak voltage V_m are given as:

$$v_a = V_m \sin(\omega t); v_b = V_m \sin(\omega t - \frac{2\pi}{3}); v_c = V_m \sin(\omega t - \frac{4\pi}{3}) \tag{6.1}$$

and respectively the three-phase input currents of the modular multilevel rectifier (MMR) are given as:

$$i_{sa} = I_s \sin(\omega t - \varphi) \tag{6.2}$$

$$i_{sb} = I_s \sin(\omega t - \frac{2\pi}{3} - \varphi) \tag{6.3}$$

$$i_{sc} = I_s \sin(\omega t - \frac{4\pi}{3} - \varphi) \tag{6.4}$$

where φ is the phase angle between voltage and current waveforms and I_s is the peak amplitude of the current. The required value of the capacitor, connected to each SM is given as [70]:

$$C_r = \frac{\bar{v}_{dcmv}^2 \bar{i}_{dcmv}}{4\varepsilon m \omega V_m \bar{v}_{cxj}^2 \cos\varphi} \left\{ 1 - \left(\frac{V_m \cos\varphi}{\bar{v}_{dcmv}} \right)^2 \right\} \tag{6.5}$$

where $\bar{v}_{dcmv}$ and $\bar{i}_{dcmv}$ are the average values of input stage rectified MVDC-bus voltage and current, ε is the voltage ripple across a capacitor ($0 < \varepsilon < 1$), *m* is the number of sub-modules per arm and $\bar{v}_{cxj}$ is the average value of capacitor voltage. With unity power factor and ε=0.05 and other parameters as given in Table 6.1, the required values of capacitors for the rectifier stage and the inverter stage are 344 µF and 17.2 µF respectively.

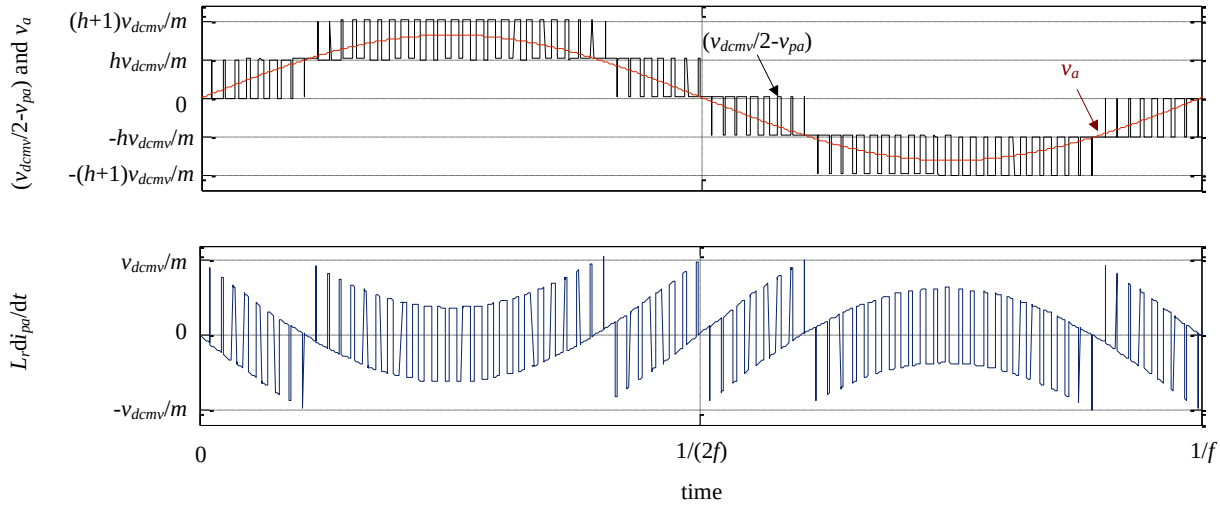


Fig. 6.2 Waveforms of inductor voltage and its components in the input rectifier stage.

The equations of phase-*a* inductor currents (i_{pa} and i_{na} as shown in Fig. 6.1), assuming fictitious midpoint voltage of the DC bus is at zero potential as compared to AC neutral, are given as:

$$L_r \frac{\mathrm{d}i_{pa}}{\mathrm{d}t} = \frac{v_{dcmv}}{2} - v_{pa} - v_a \tag{6.6}$$

$$L_r \frac{\mathrm{d}i_{na}}{\mathrm{d}t} = \frac{v_{dcmv}}{2} - v_{na} + v_a \tag{6.7}$$

where v_{pa} and v_{na} are the cumulative voltages across series connected sub-modules of upper and lower arms. Fig. 6.2 shows the different voltages involved in (6.6) and (6.7). Voltages v_{pa} and v_{na} are of switching nature and follow a reference sinusoidal voltage, with a DC offset of $+v_{dcmv}/2$ and $-v_{dcmv}/2$ respectively. The inductor voltage, as shown in this figure, has a peak to peak value of v_{dcmv}/m and a frequency of *m* times switching-frequency f_{sr}. The maximum current ripple is observed during the phase voltage peak (also current peak at unity power factor). The input current i_{sa} is given by the difference between lower arm current i_{na} and upper arm current i_{pa}. The frequency of the input current ripple is twice the frequency of ripple in the arm current. Therefore, the required inductance value L_r for a particular value of maximum input current ripple is given as:

$$L_r = \frac{\{(h+1)\bar{v}_{dcmv}/m - V_m\}(V_m - h\bar{v}_{dcmv}/m)}{2\bar{v}_{dcmv} f_{sr} \Delta i_{sa}} \tag{6.8}$$

where h is an integer defined as $(h+1)\bar{v}_{dcmv}/m > V_m > h\bar{v}_{dcmv}/m$. For a current ripple of 5 %, the inductor value is calculated as 20.1 mH.

In the modular multilevel inverter (MMI) section, a fundamental-frequency modulation is used, inductors for ripple reduction are not required. However, small inductors can be used to avoid shoot through condition. At the load side, to filter ripple content, an inductive-capacitive filter is used. The values of inductance and capacitance can be estimated as [17]:

$$L_o = \frac{\bar{v}_{dcl}(1 - n\bar{v}_{dcl}/\bar{v}_{dcmv})}{2 f_{si} \Delta i_{Lo}} \tag{6.9}$$

$$C_o = \frac{\bar{v}_{dcl}(1 - n\bar{v}_{dcl}/\bar{v}_{dcmv})}{32 f_{si}^2 L_o \Delta v_{Co}} \tag{6.10}$$

where $\bar{v}_{dcl}, n, f_{si}, \Delta i_{Lo}$ and Δv_{Co} are output rated average voltage, turns-ratio of medium-frequency transformer, switching-frequency of MMI, inductor current ripple and capacitor voltage ripple, respectively. With a transformer turns-ratio n=76 and current and voltage ripple of 5 % each, values of filter inductor and capacitor are 31 µH and 3.2 mF respectively.

6.1.2 Control

The rectifier stage control utilizes the capacitor balancing technique discussed in [69] and adapts it for rectifier mode of operation. A vector control of input currents is added in the scheme, therefore, there are two parts of control scheme of MMR:

(1) input–output power balance by vector control of input currents for maintaining DC-bus voltage and unity input power factor

(2) capacitor voltage balancing of individual sub-modules that involves average capacitor voltage control and balancing control.

6.1.2.1 Vector Control

Fig. 6.3 (a) shows the vector control of input currents. In *a-b-c* coordinates *a-b-c* axes are fixed on the same plane, apart from each other by 120°. The sensed currents, as given by (6.2)-(6.4) can be transformed (Park's transformation) into *d-q* frame as follows:

$$\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ -\sin\theta & -\sin(\theta - 2\pi/3) & -\sin(\theta + 2\pi/3) \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \tag{6.11}$$

where, θ is the transformation angle.

Sensed rectifier DC-bus voltage v_{dcmv} is compared with the reference voltage and the error is fed to a PI controller (gains K_{pdcmv} and K_{idcmv}). Output of the PI controller provides the *d*-axis reference current i_{sd}^*, which is compared with the sensed *d*-axis input current, given by (6.12). The error is fed to another PI controller (gains K_{pid} and K_{iid}), which provides the *d*-axis reference voltage v_d^*. The *q*-axis current is forced to zero using a *q*-axis PI controller (gains K_{piq} and K_{iiq}). These reference voltages v_d^* and v_q^* are transformed back to *a-b-c* frame and utilized further for the rectifier control as:

$$\begin{bmatrix} v_a^* \\ v_b^* \\ v_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & -\sin\theta \\ \cos(\theta - 2\pi/3) & -\sin(\theta - 2\pi/3) \\ \cos(\theta + 2\pi/3) & -\sin(\theta + 2\pi/3) \end{bmatrix} \begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} \tag{6.12}$$

6.1.2.2 Capacitor Voltage Balancing Control

Balancing of the capacitor voltages for the MMR is achieved by controlling the average value of all capacitor voltages of a particular phase and individual capacitor voltages [69]. Fig. 6.3 (b) and (c) show these control loops. The average of the capacitor voltages of phase-*a* is given as:

$$v_{ca} = \frac{1}{2m} \sum_{j=1}^{2m} v_{caj} \tag{6.13}$$

This average capacitor voltage is compared with the reference capacitor voltage ($v_c^* = v_{dcmv}^*/m$) and the error is processed by a PI controller (gains K_{pA} and K_{iA}). The output of the PI controller provides the reference value of the loop current (or circulating current). The loop current for phase-*a* is given as:

$$i_{za} = \frac{i_{pa} + i_{na}}{2} \tag{6.14}$$

The error between reference and actual values of the DC loop current is processed by another PI controller (gains K_{piz} and K_{iiz}) to achieve the averaging voltage command v_{Aa}^{*}.

For controlling the individual capacitor voltages, the actual capacitor voltage is compared with the reference voltage and the error is processed with a proportional controller (gain K_{pB}). Depending on the sign of arm current (i_{pa} and i_{na}), the sign of the processed voltage command is decided. The voltage command for sub-modules j = 1 to m is given as:

$$v_{Baj}^{*} = \begin{cases} K_{pB}(v_c^{*} - v_{caj}) & \text{if } i_{pa} > 0 \\ -K_{pB}(v_c^{*} - v_{caj}) & \text{if } i_{pa} < 0 \end{cases} \tag{6.15}$$

and for sub-modules $j = m$+1 to 2m:

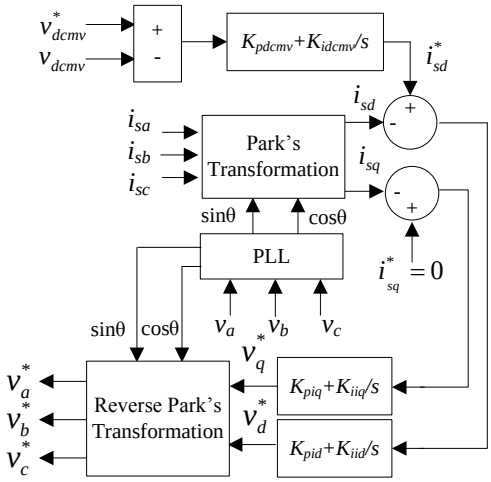
$$v_{Baj}^{*} = \begin{cases} K_{pB}(v_c^{*} - v_{caj}) & \text{if } i_{na} > 0 \\ -K_{pB}(v_c^{*} - v_{caj}) & \text{if } i_{na} < 0 \end{cases} \tag{6.16}$$

The voltage commands for PWM signal generation for sub-modules are given as below:

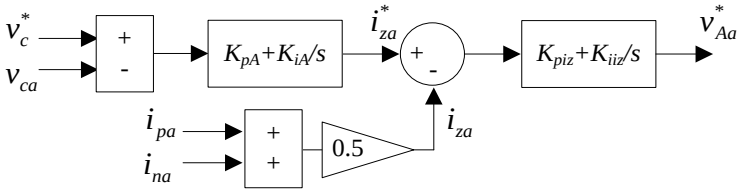
$$v_{aj}^{*} = v_{Aa}^{*} + v_{Baj}^{*} - v_a^{*}/m - v_{dcmv}^{*}/2m \quad \text{for } j = 1 \text{ to } m \tag{6.17}$$

$$v_{aj}^{*} = v_{Aa}^{*} + v_{Baj}^{*} + v_a^{*}/m - v_{dcmv}^{*}/2m \quad \text{for } j = m+1 \text{ to } 2m \tag{6.18}$$

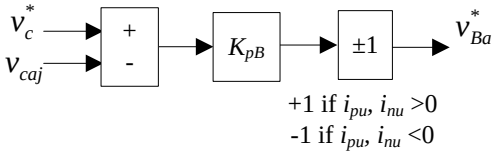
These voltage commands are normalized with respect to the reference capacitor voltage and compared with triangular carrier signals for PWM generation. The triangular signals have a maximum value of unity and minimum value of zero with a frequency of f_{sr} (1 kHz). The carrier signals for different sub-modules of each phase are phase-shifted by 360°/2m and the phase-shift between signals for the same arm is 360°/m.



(a)



(b)



(c)

Fig. 6.3 (a)-(c) Modular multilevel rectifier control block-diagrams.

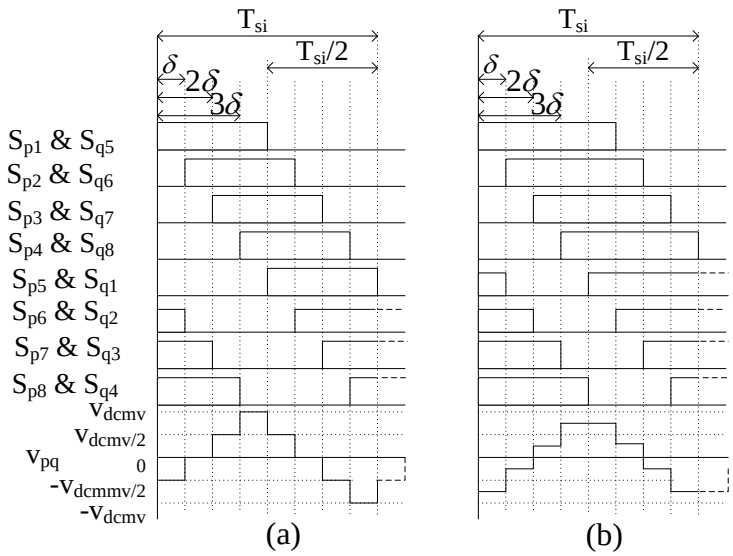


Fig. 6.4 Modular multilevel inverter mode switching signals with (a) 50 % duty ratio and (b) duty ratio higher than 50 %.

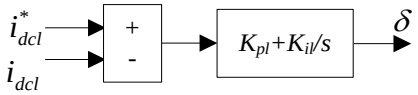


Fig. 6.5 Output current control block diagram.

6.1.2.3 Control of DC-DC Converter

The DC-DC converter consists of a modular multilevel inverter (MMI) operating in square wave mode, a medium-frequency step-down transformer and a rectifier. The operation of MMI in square-wave mode is shown in Fig. 6.4 (a) and (b). As shown in Fig. 6.4 (a), each sub-module is turned on for the duration of $T_{si}/2$ (50 % duty cycle). The phase shift between the gating signals of the sub-modules within one arm is used to control the output voltage. The upper and lower arm sub-module commands of the same leg are phase-shifted by 180°. Zero phase shift between modules yields the maximum RMS (root mean square) voltage, equal to the value of $\bar{v}_{dcmv}$. As the phase shift increases to 60°, the RMS voltage reduces to $\sqrt{1/6}\bar{v}_{dcmv}$. An expression of RMS voltage in terms of delay angle δ for $0^o \leq \delta \leq 60^o$ is given as:

$$V_{pqrms} = \bar{v}_{dcmv}\sqrt{1-5\delta/360°} \tag{6.19}$$

Further reduction in voltage can be achieved by increasing the duty cycle of switches beyond $T_{si}/2$, as shown in Fig. 6.4 (b). In order to balance the capacitor voltages, the sequence of gating signals is changed in a circular manner, after each time period. The phase delay between the sub-

modules is estimated by a PI controller over the output inductor current as shown in Fig. 6.5. The sensed output current i_{dcl} is compared with the reference current value and the error is processed with the help of a PI controller (gains K_{pl} and K_{il}). The output signal of the PI controller constitutes the required phase delay δ for the inverter section.

Table 6.1 System parameters

Input	3-ph, 10 kV, 50 Hz
Load	1 MW, 150-220 V, 0-4545 A, voltage ripple=5 %
Modular multilevel rectifier	L_r=20.1 mH, C_r=344 µF, m=4, h=1, f_{sr}=1 kHz, K_{pdcmv}=0.1 A/V, K_{idcmv}=10 A/Vs, K_{pid}=100 V/A, K_{iid}=3000 V/As, K_{piq}=100 V/A, K_{iiq}=3000 V/As, K_{pA}=0.1 A/V, K_{iA}=10 A/Vs, K_{piz}=10 V/A, K_{iiz}=600 V/As and K_{pB}=0.4
Modular multilevel inverter	L_r=1 µH, C_i=17.2 µF, m=4, f_{si}=1 kHz, K_{pl}=9×10^{-4} deg/A and K_{il}=1.8 deg/As
Transformer	n=76, L_1=1.6 mH, L_2=2.87 µH, r_1=0.36 Ω, r_2=71 µΩ
Output filter	L_o=31 µH, C_o=3.2 mF

6.1.3 Results and Discussion

Modeling and simulation of the power-supply is carried out in MATLAB Simulink and PLECS. The model is analyzed using ode15s (stiff/NDF) solver with a maximum step size of 1×10^{-6} s and relative tolerance of 1×10^{-3}. Fig. 6.6 shows the dynamic behavior of the system with a DC load current of 4545 A and load voltage of 220 V. Quantities shown in this figure are the three-phase voltages (v_a, v_b, v_c), the three-phase source currents i_s, the MVDC link voltage v_{dcmv}, the sub-module capacitor voltages for phase-a, v_{caj}, j=1 to 8, the output load voltage v_{dcl}, and the load current i_{dcl} respectively from top to bottom. At time t=0.4 s the load current command is changed from 4545 A (rated current) to 2000 A. Load voltage and current settle down to the command value within 5 ms. The MVDC link voltage and the input currents settle down fully within two cycles of the input line frequency. The capacitor voltage variation of different sub-modules of a phase is well within the limits (±100 V i.e. 4 %, during steady state at full load).

Fig. 6.7 (a) and (b) show the output voltage v_{pq} and the currents i_{pq} of the medium-frequency inverter section apart from the sub-module capacitor voltages v_{cpj}, j=1 to 8 during full and light load conditions. The shape of inverter section voltage changes as per the required output voltage. Individual capacitor voltages are fairly balanced. Fig. 6.8 shows the harmonic spectra of input current at 4545 A and 2000 A load current. The input current THDs are 0.56 % and 1.03 % at

load current of 4545 A and 2000 A respectively. From Fig. 6.6 it can be observed that input currents are in phase with input voltage, which means the input power factor is unity over the whole range of operation.

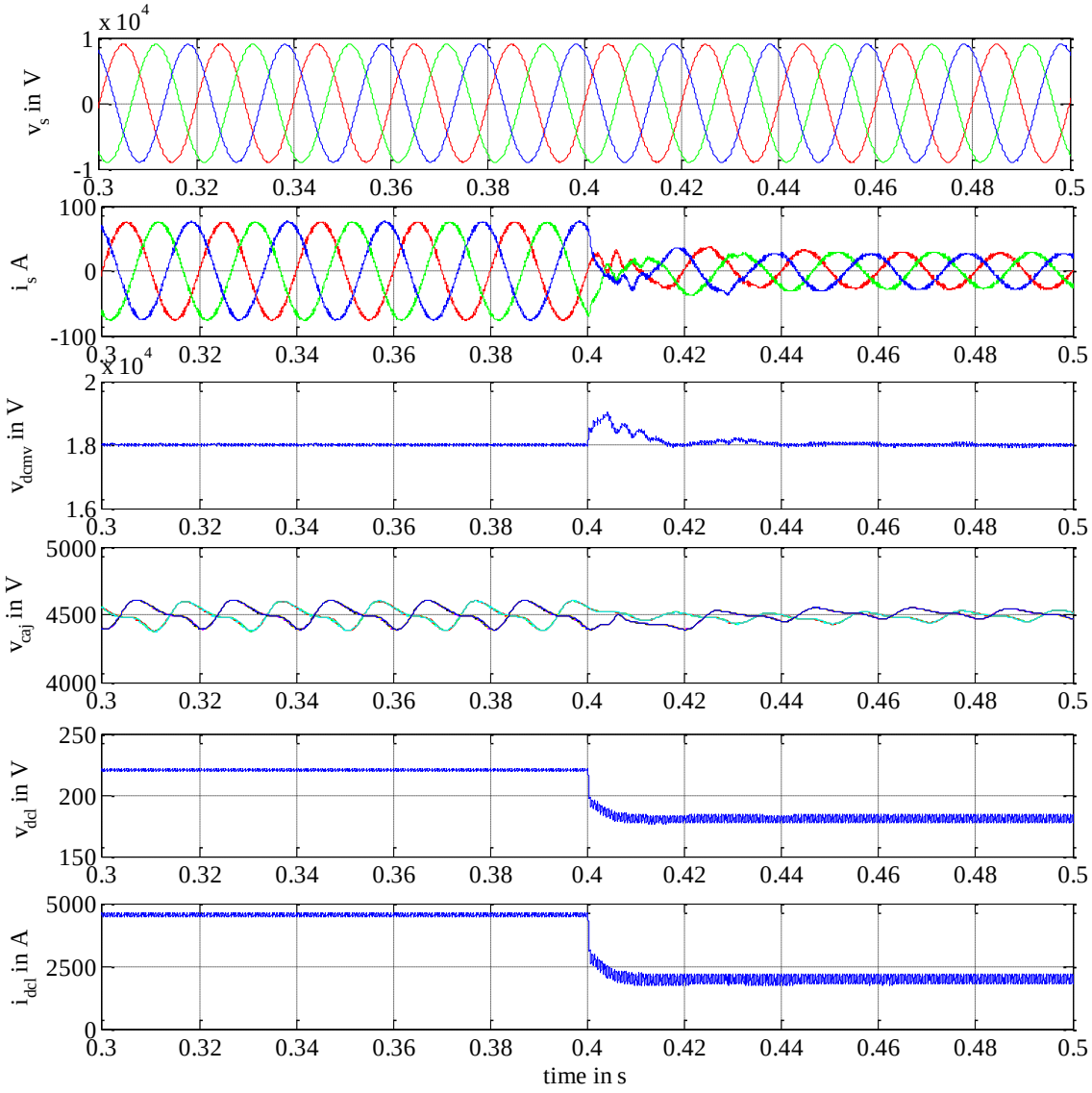
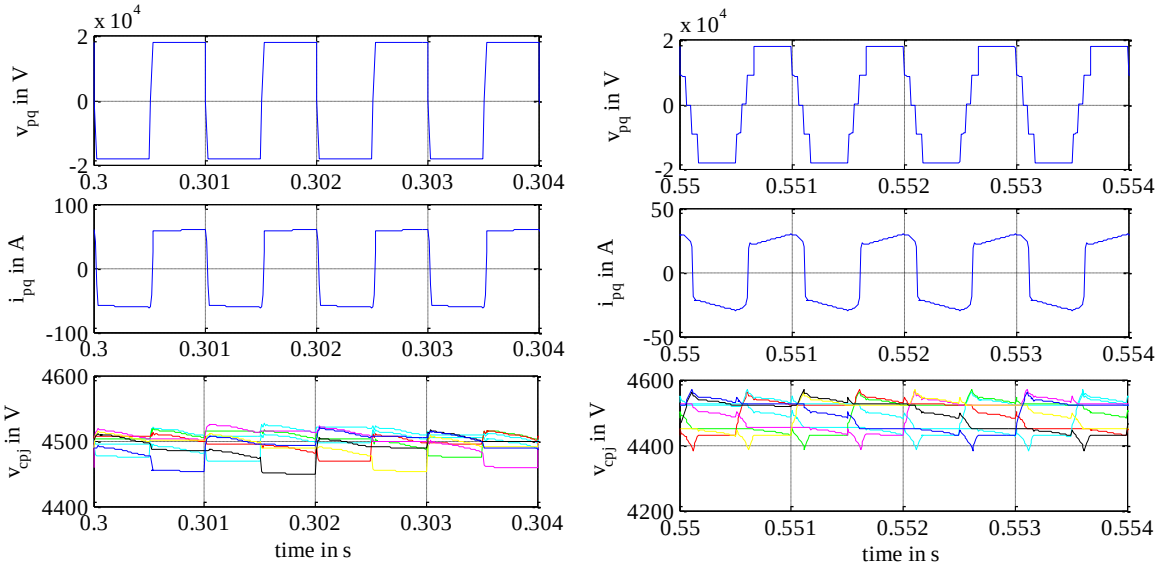
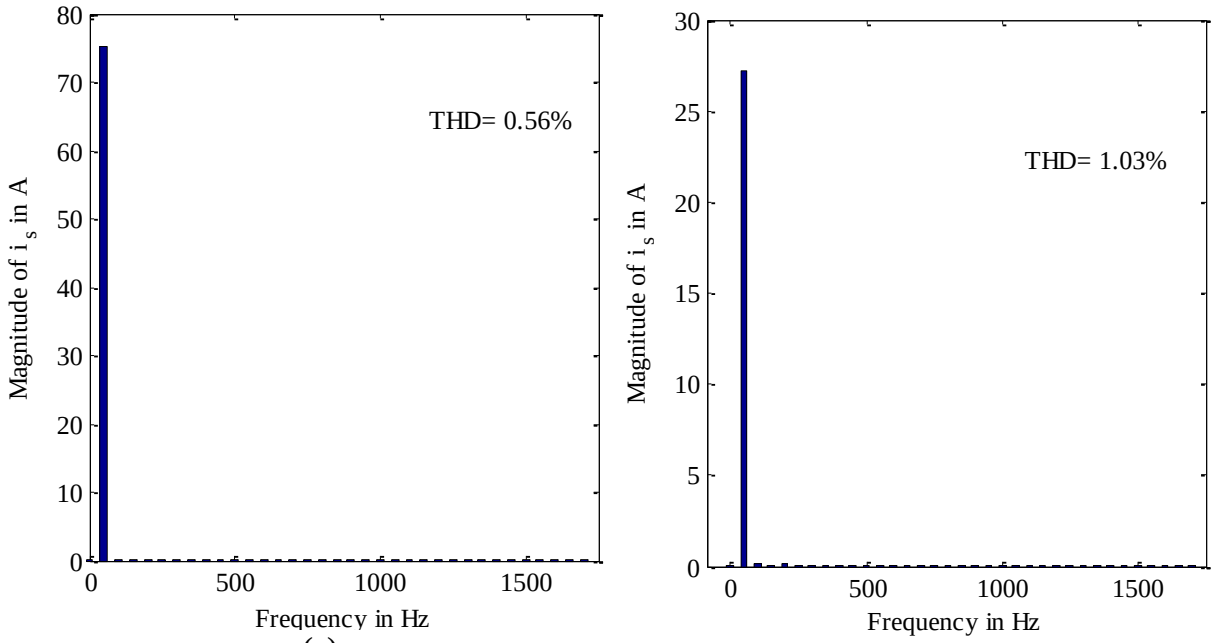


Fig. 6.6 Dynamic response of the system with a step change in the output current from 100 % to 30 % at t=0.8 s.



(a) (b)

Fig. 6.7 (a) and (b) MM-inverter performance at 100 % and 30 % load current respectively.



(a) (b)

Fig. 6.8 Harmonic spectra of input current (a) at rated load current (4545 A) (b) at 2000 A of load current.

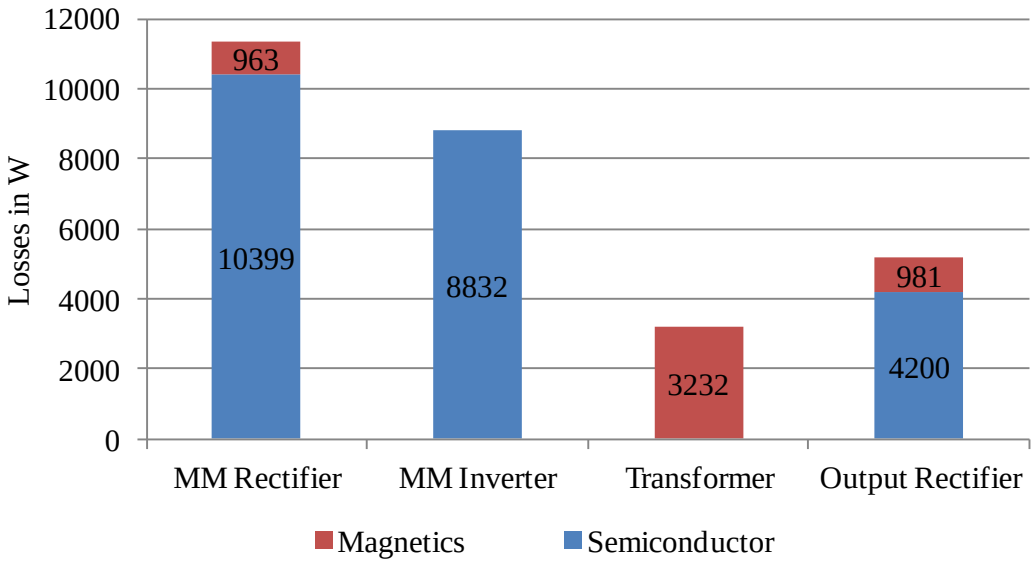


Fig. 6.9 Losses in different sections of the power-supply at full load on top load line.

6.1.4 Efficiency Estimation

At the input rectifier stage, maximum current flows through the anti-parallel diodes with IGBTs used in the sub-modules. The average diode and IGBT currents at full load are 17 A and 7 A, respectively, at a voltage rating of 4.5 kV. IGBTs of 6.5 kV, 25 A rating (5SMX 12M6501) and 50 A diodes (5SLX 12M6520) by ABB can be used for the application with sufficient margins for current and voltage. For the inverter section, most of the current (25 A) flows through the IGBT, therefore, two chips of the same IGBT can be used in parallel to achieve a sufficient safety margin for current. Welding diodes of 400 V, 5.1 kA by ABB (5SDF63B0400) can be used at the output stage. Data of these devices (on-state characteristics, switching-energy variations with voltage and current) is utilized to estimate the semiconductor losses, taking place in the power-supply at various current levels along the top and bottom load lines with the help of a PLECS model (please refer to Appendix A for more details). The magnetic components like AC inductors, transformer and output filter inductor are also designed and losses are estimated (please refer to Appendix B for more details). The losses in the capacitors are estimated but found to be negligible, therefore ignored. Fig. 6.9 provides an overview about the distribution of losses in different components. The overall estimated losses at full load are 28588 W that results in an efficiency of 97.2 %. Variation of the estimated efficiency with the changing current values at top and bottom load lines is depicted in Fig. 6.10.

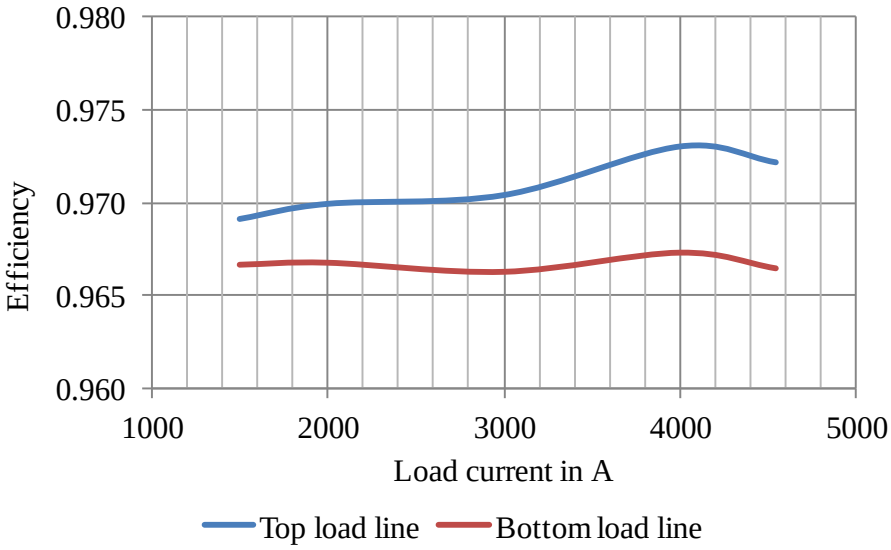


Fig. 6.10 Variation of efficiency over the load current.

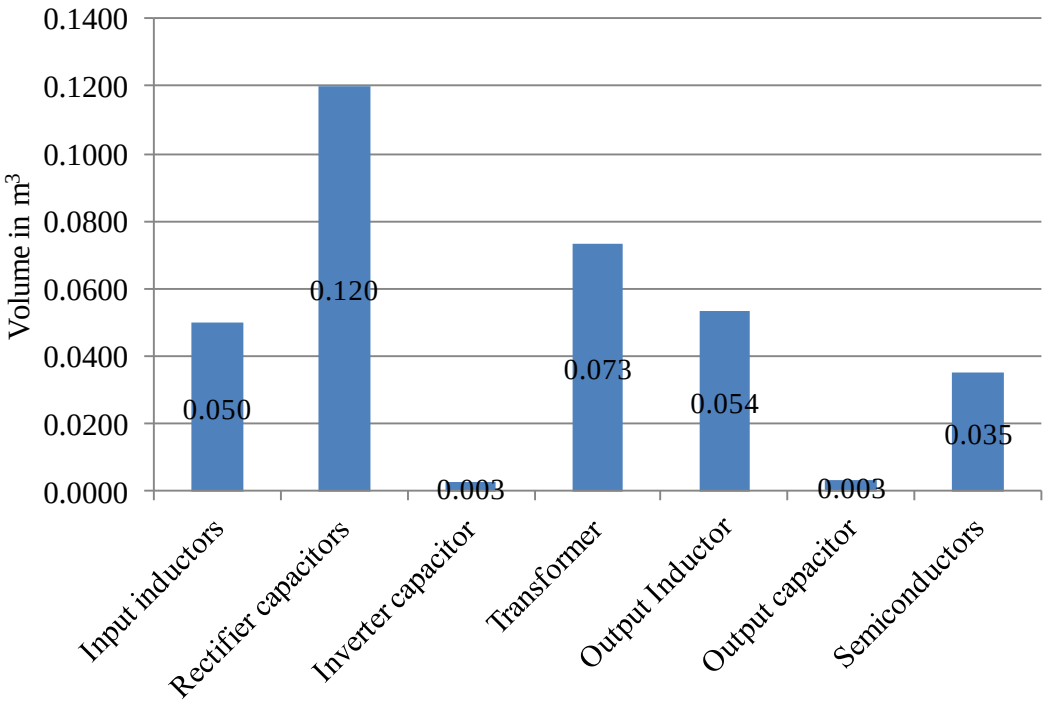


Fig. 6.11Volume of different components of the power-supply.

6.1.5 Volume Estimation

Fig. 6.11 shows the estimated volumes of various components used in the power-supply. Volumes of the selected components are calculated with the help of dimensions provided in datasheets. Size of the magnetic components is estimated with the standard design procedure as explained in Appendix B. For medium frequency transformer, high Silicon 10JNEX900 core is

used. The biggest contributors to the size of this circuit are the DC capacitors. Afterwards, transformer and filter inductors are the main contributors to the size of the system. The total volume of the power-supply comes out to be 0.337 m^3, which is less than half of the volume of the topologies discussed previously (chopper-rectifier and thyristor rectifier with hybrid filter).

6.2 A Completely Modular Power Converter for High-Power High-Current DC Applications

Reliability and availability are the important requirements for the power converter apart from power quality. In case of thyristor rectifiers, n-1 redundancy is provided by parallel connection of the semiconductor devices. However, several centralized components (such as filters, transformer etc.) are used that lead to multiple failure modes. Replacement of these large components is both time consuming and costly. Therefore, modularity of the system is a highly desired feature for high-power applications as it eases assembling, scaling, duplication, maintenance, and replacement in case of a failure. In the previous section, a MMC based power-supply is discussed. This topology is able to connect to a medium-voltage input (10 kV or higher) and able to provide a high output current with an excellent input and output power quality and leads to a reduction of volume, too. The front-end rectifier and medium-frequency inverter are made of modular units. However, the system still consists of centralized components like a medium-frequency transformer and a diode rectifier. In this section, the level of modularity is extended and a completely-modular solution is discussed [E]. The envisaged topology is shown in Fig. 6.12 (a) and (b). Each module consists of a front-end chopper cell followed by an isolated DC-DC converter as shown in Fig. 6.12 (b). The input of the power converter is connected to a medium-voltage AC grid. The medium-voltage DC-bus capacitor of each module is used to tap the power. An isolated DC-DC converter is connected to step-down the capacitor voltage suitably. The outputs of these DC-DC converters are paralleled to feed a low-voltage high-current load. This architecture provides unique advantages in terms of excellent input power quality (low current THD and unity power factor), removal of bulky line frequency transformer and improved control over output voltage and current. Further, it suits the needs of blocking high-voltage at the input side and providing high-current at the output side by series and parallel operations at input and output sides, respectively. Moreover, the design is completely modular. The chopper cell configuration (half-bridge as compared to fill-bridge)

leads to a higher number of sub-modules, which is an added advantage for high-current applications. Architecture, design, control and performance of such a power converter are discussed in this section. Loss estimation is presented for different components of the power converter to highlight the efficiency benefits. Simulations of the system are carried out in the MATLAB, Power System Blockset and PLECS environments and results are presented to demonstrate the effectiveness of the system.

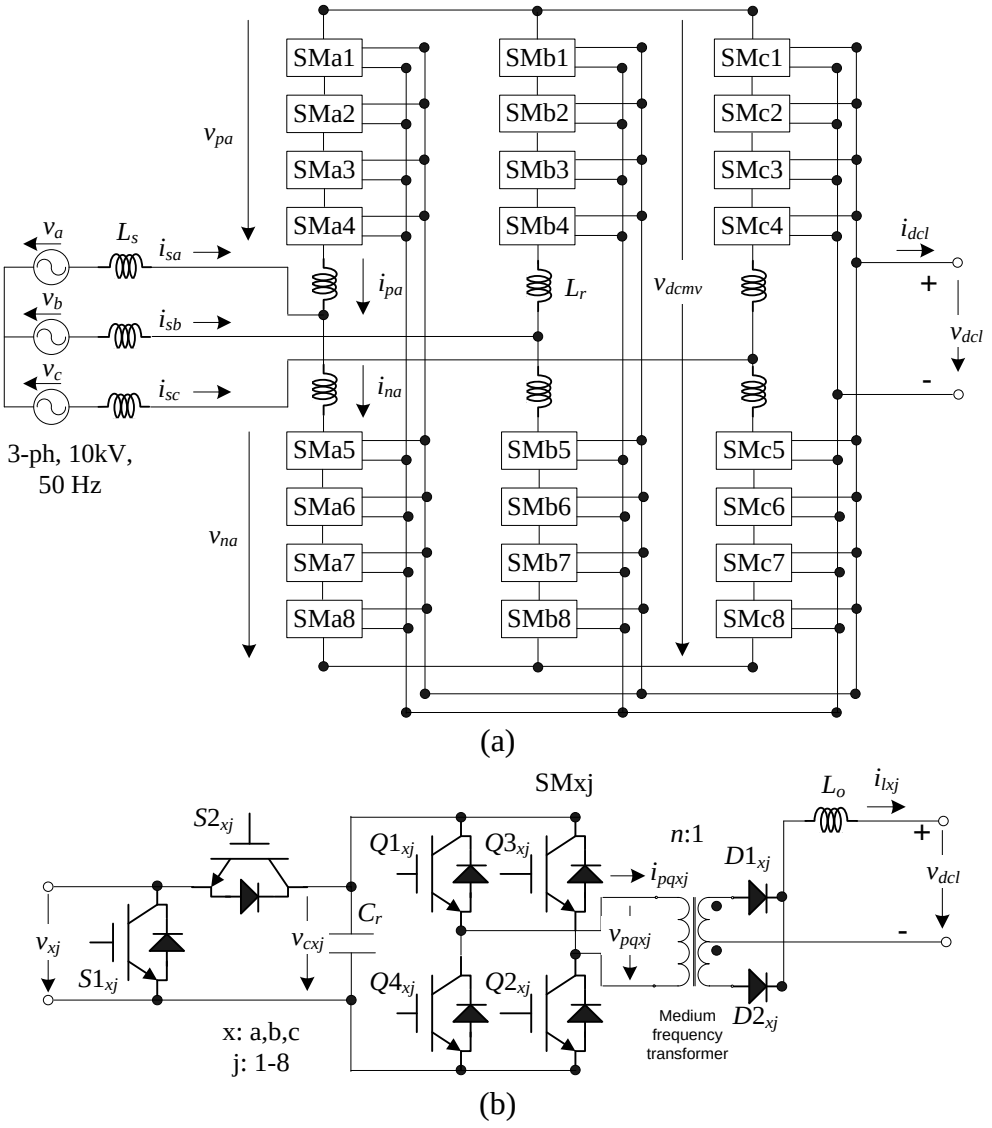


Fig. 6.12 (a) and (b). Circuit diagram of the completely-modular power-converter.

6.2.1 Design and System Specifications

The circuit diagram of the proposed power converter is shown in Fig. 6.12. The system consists of 24 sub-modules (SMs), 8 sub-modules per phase. All SMs (4×2×3) are connected in

parallel at the output-stage, to supply the required amount of load current. Each sub-module comprises of a chopper cell (*S*1 and *S*2) a DC capacitor (C_r), a medium-frequency H-bridge inverter (*Q*1-*Q*4), a medium-frequency transformer, a diode rectifier (*D*1 and *D*2) and a filter inductor (L_o). The medium-level DC-link voltage v_{dcmv}, (as shown in Fig. 6.12 (a)) is kept at 18000 V that results in capacitor voltages v_{cxj} (x = *a*, *b* and *c* and j=1-8) equal to 4500 V. The switching-frequency is selected as 1 kHz to achieve moderate switching losses. At the output stage, an interleaving concept is used to minimize the output inductor requirement. This also leads to discontinuous inductor currents, which is expected to reduce switching losses in the DC-DC conversion stage.

The number of modules used per arm is a design choice; here 4 modules are used per arm. This leads to a voltage of 4.5 kV per SM. Which means 6.5 kV IGBTs can be used as semiconductor switches. One can increase the number of modules to reduce the voltage per module and use IGBTs with lower voltage rating. The number of modules can be optimized for losses, life and cost; however, this topic lies out of the scope of this work.

The characteristic of the considered industrial load of 1 MW power rating is shown in Fig. 4.1. Design criteria for input inductor, chopper cell capacitor and remains the same as explained in previous section. Design values of the various components are provided in Table 6.2. Symbols, used in this section, also remain same as the previous section.

For the DC-DC stage, the required value of output inductor (with interleaving) is given as [17]:

$$L_o = \frac{\bar{v}_{dcl}(1 - n\bar{v}_{dcl} / \bar{v}_{dcmv})}{12 m f_{si} \Delta i_{Lo}} \tag{6.20}$$

where $\bar{v}_{dcl}$, n, f_{si} and Δi_{Lo} are output rated average voltage, transformer turns-ratio, switching-frequency of DC-DC converter and inductor current ripple respectively. With a transformer turns-ratio, n=18 and load current ripple of 5 %, value of filter inductor is 19 µH, respectively.

Various design parameters are provided in Table 6.2.

6.2.2 Control

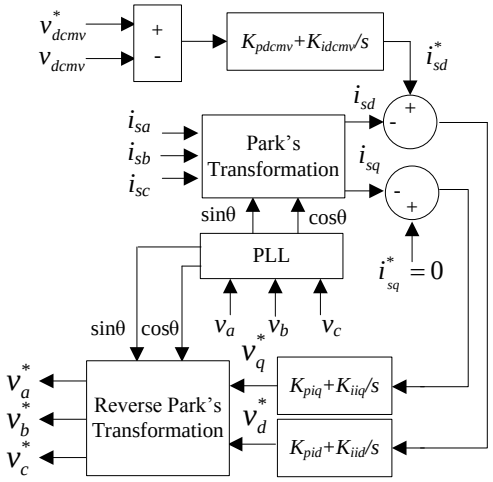
Control methodology for the input rectifier stage remains the same as that of previous topology. Therefore, repetition of the control equations is avoided. However, the control block diagrams are provided in Fig. 6.13 (a)-(e) for ready reference. These figures show various control block diagrams. There are three objectives of the employed control system:

1. to maintain power balance between input and output, and, at the same time, to maintain unity power factor at the input stage with good current quality (Fig. 6.13 (a)),

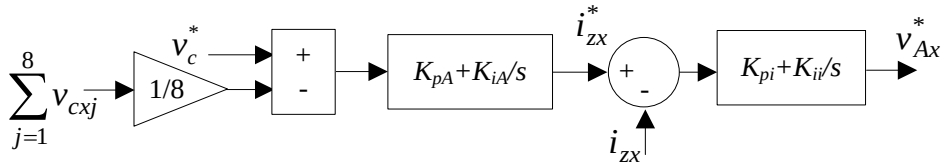
2. to achieve voltage balance between capacitors of different SMs (Fig. 6.13 (b)-(d)),

3. to provide required amount of current to the load (Fig. 6.13 (e)).

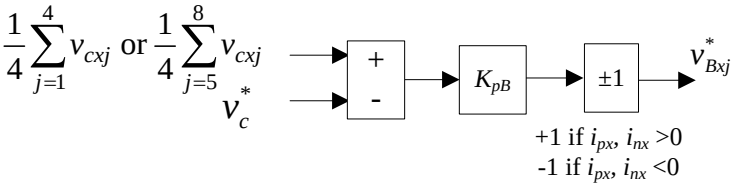
Different control loops are employed to achieve these objectives as shown in Fig. 6.13. Various control parameters are provided in Table 6.2.



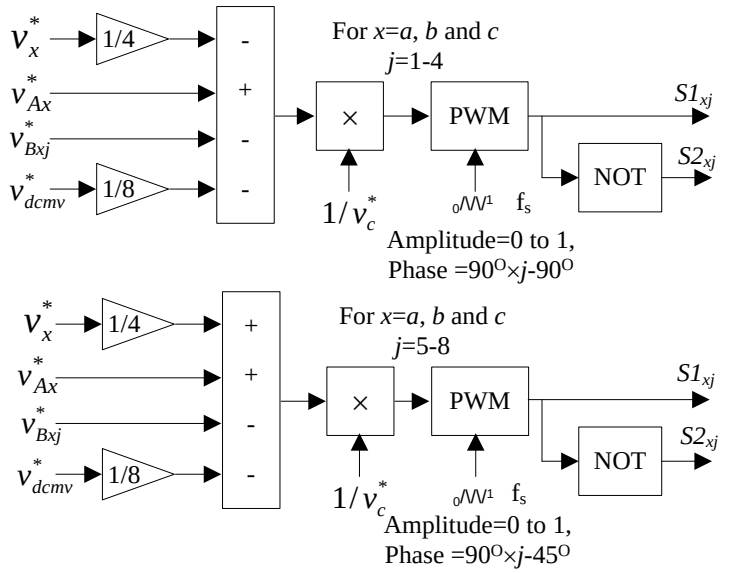
(a)



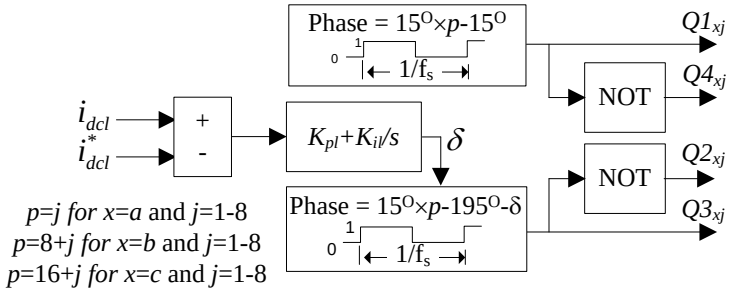
(b)



(c)



(d)



(e)

Fig. 6.13 (a) Power balance vector control (b) Average capacitor voltage control (c) Individual capacitor voltage control (d) Switching signal generation for chopper cell (e) Output current control

As compared to the previous topology, here the DC-DC converter consists of a standard H-bridge operating in square-wave mode, a medium-frequency step-down transformer and a center tapped rectifier. Control of this section differs from the previous topology and to control the output current the phase-shifted PWM technique is used. The phase delay between the switching signals is estimated by a PI controller (gains K_{pl} and K_{il}) over the output current i_{dcl} as shown in Fig. 6.13 (e). The output signal of the PI controller constitutes the required phase delay δ for the

H-bridge. To achieve interleaving, the switching signals of different modules are phase shifted by $360^o/6m$.

Table 6.2 System Parameters

Input	3-ph, 10 kV, 50 Hz
Load	1 MW, 150-220 V, 0-4545 A, voltage ripple=5 %
Sub module	L_r=20.1 mH, C_r=344 µF, f_s=1 kHz, L_o=19 µH, m=4
Transformer	n=18, L_{l1}=1.97 mH, L_{l2}=5.3 µH, r_1=0.75 Ω, r_2=2.8 mΩ
Control parameters	K_{pdcmv}=0.18 A/V, K_{idcmv}=5 A/Vs, K_{pid}=20 V/A, K_{iid}=3000 V/As, K_{piq}=20 V/A, K_{iiq}=3000 V/As, K_{pA}=0.1 A/V, K_{iA}=8 A/Vs, K_{pi}=15 V/A, K_{ii}=500 V/As, K_{pB}=1, K_{pl}=2.1×10^{-8} A^{-1} and K_{il}=4.2×10^{-5} $A^{-1}s^{-1}$

6.2.3 Results and Discussion

Modeling and simulation of the converter is carried out in MATLAB Simulink and Power System Blockset. The model is analyzed using ode15s (stiff/NDF) solver with a maximum step size of 1×10^{-6} s and relative tolerance of 1×10^{-3}. Fig. 6.14 shows the dynamic behavior of the system with DC load current of 4.5 kA and load voltage of 220 V. The quantities shown in this figure are the three phase voltages v_s, the three phase source currents i_s, the medium level DC link voltage v_{dcmv}, the SM capacitor voltages v_{caj} of phase-*a*, where j=1 to 8, the output DC load voltage v_{dcl} and the load current i_{dcl} respectively from top to bottom. At time t=0.5 s the load current command is reduced from 4.5 kA to 2.0 kA. The variations of the capacitor voltages, in the different sub-modules of phase-*a*, are well within the limits. The input current THD is 1.2 % and 2.5 % during 4.5 kA and 2.0 kA output current respectively. From Fig. 6.14, it can be observed that the input currents are in phase with the input voltages, which means input power factor is unity.

Various control signals (as defined by Fig. 6.13 (d) and (e)) are shown in Fig. 6.15. It can be seen that change in the current command at t=0.5 s results into a change of phase-shift δ. The phase-shift controls the output voltage of DC-DC stage. Performance of the DC-DC stage is shown in Fig. 6.16. Quantities shown are capacitor voltage v_{ca1}, H-bridge output voltage v_{pqa1}, H-bridge output current i_{pqa1} and output inductor current i_{la1} of first SM of phase-*a*. It can be seen that variation of capacitor voltage leads to variation of peak value of the output inductor current. Although the ripple in the current of each inductor of SMs is very high, due to interleaving operation current ripple in the output current is fairly low.

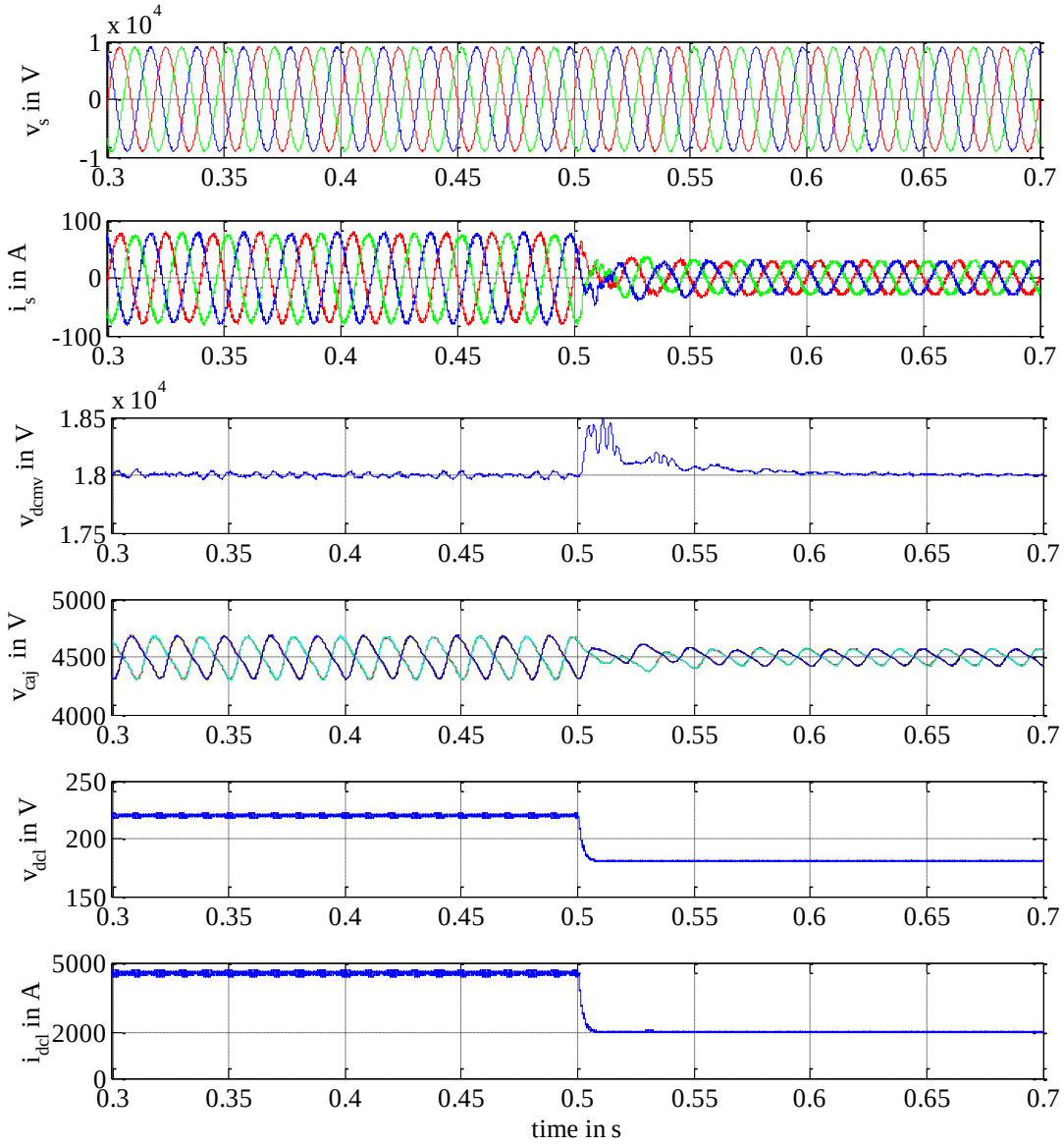


Fig. 6.14 Dynamic response of the system with change in output current from 4545 A to 2000 A.

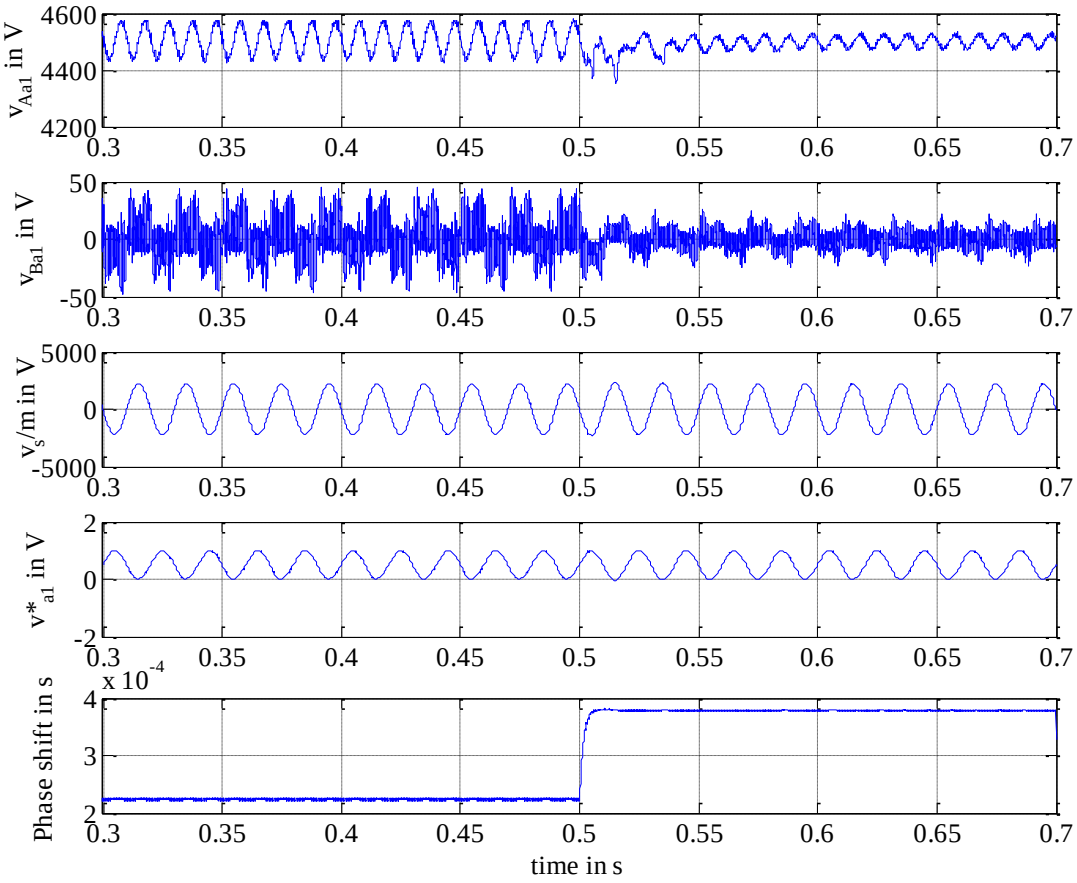


Fig. 6.15 Variation of control signals with step change in output current from 4545 A to 2000 A at t=0.5 s.

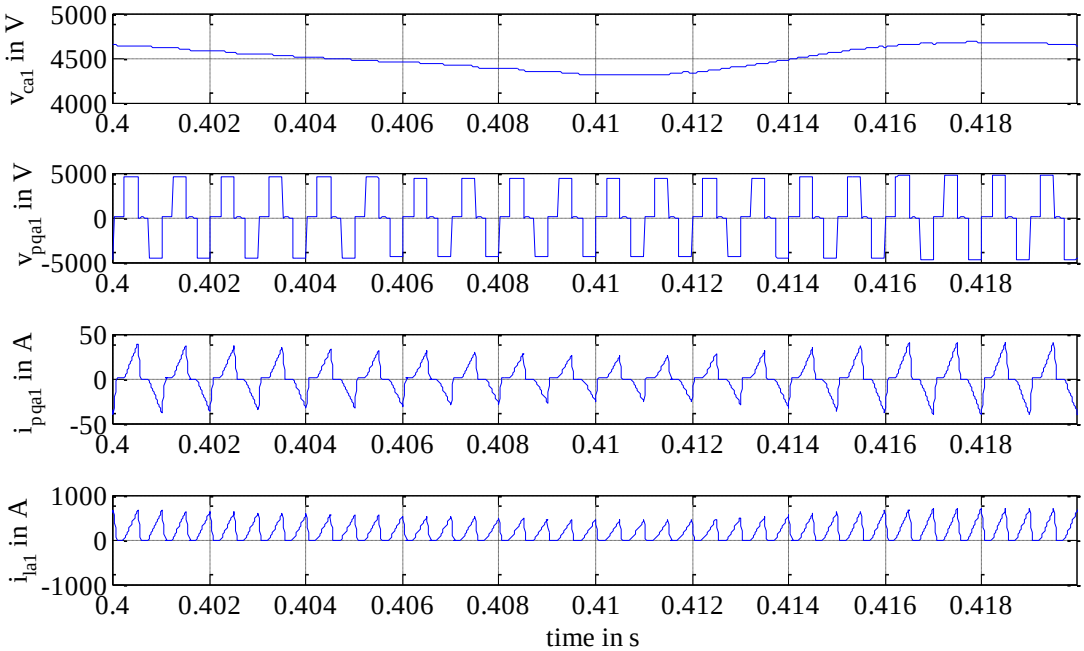


Fig. 6.16 Waveforms of the DC-DC stage at 4.5 kA output current.

6.2.4 Efficiency Estimation

Diodes in parallel with IGBTs ($S1_{xj}$ and $S2_{xj}$) take maximum amount of current at input rectifier stage. The average diode and IGBT currents at full load are 11 A and 1.5 A respectively, at a voltage rating of 4.5 kV. However, the repetitive peak current value goes as high as 46.0 A. IGBTs of 6.5 kV, 25 A rating (5SMX 12M6501) and 50 A, 6.5 kV diodes (5SLX 12M6520) by ABB can be used in parallel for the application with sufficient margins for current and voltage. For the inverter, most of the current (I_{ave}=5 A, I_{peak}=28 A) flows through the IGBT, therefore a 25 A, 6.5 kV IGBT (5SNA 0400J650100) from ABB can be used to achieve a sufficient safety margin for the current. A fast recovery diode (D241S) with a rating of 240 A by Infineon can be used at the output stage rectifier with sufficient current margin. As stated in the section 6.1.4, data of these devices are utilized to estimate the semiconductor losses with the help of a PLECS model. The magnetic components like AC inductors, transformer and output DC filter inductor are also designed and losses in each component are estimated. The losses in the capacitors are estimated but found to be negligible, therefore ignored. The overall estimated losses are 42.6 kW and 50.9 kW at full power with a load current of 4545 A at TLL and BLL. This results in an overall efficiency of 95.9 % and 93.5 % respectively. Losses occurring in different components at full load are shown in Fig. 6.17. Variation of the efficiency at top and bottom load lines is shown in Fig. 6.18. It can be observed that efficiency of this topology is lower as compared to the topology shown in Fig. 6.1. From Fig. 6.17, it can seen that the major amount of losses take place in the H-bridge inverter. Moreover, when compared to the previous topology (Fig. 6.9), overall losses in the transformer-section have also increased. The losses in the front-end rectifier remain the same, whereas it reduces marginally in the output rectifier section. As the RMS value of current flowing through transformer increases (due to the higher peak value in discontinuous current mode of operation), size and losses of the transformer also increase. However, the raise in transformer losses has affected the efficiency only by 0.6 %. The major reason of the drop in the efficiency is the losses in the H-bridge section. Losses in the inverter section have doubled as compared to the previous topology. As discussed before, the H-bridge inverter works in discontinuous-conduction mode. This leads to zero current turn-on (ZCS) of IGBTs and zero current turn-off of rectifier diodes. However, as the peak current increases, turn off of IGBTs takes place at relatively high current. This is the major contributor of the losses in the H-bridge section. Methods to reduce this component shall be discussed in the section 6.2.6.

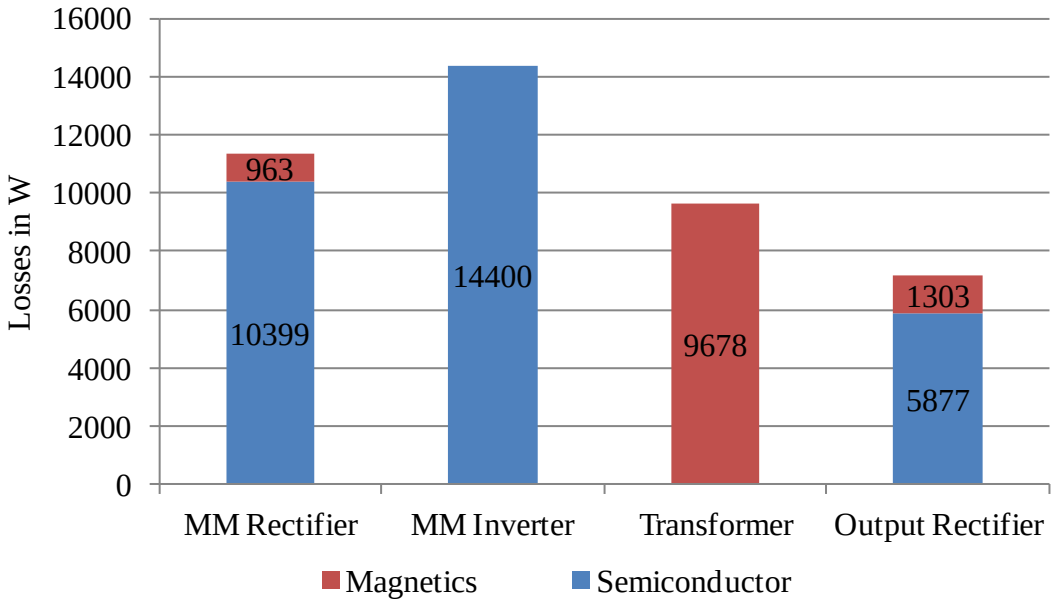


Fig. 6.17 Distribution of power loss in different components

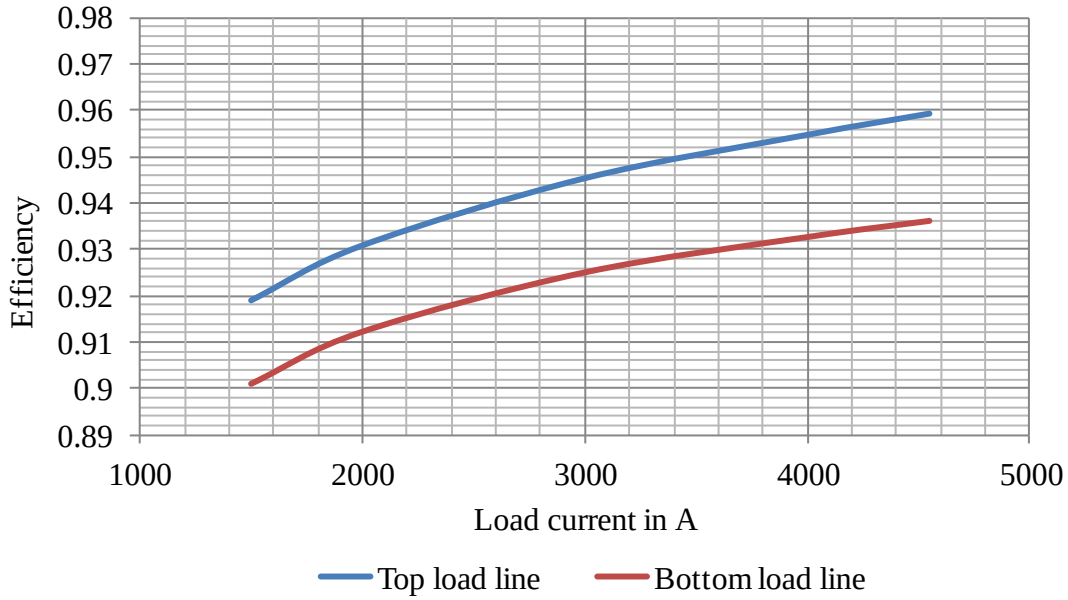


Fig. 6.18 Variation of efficiency with load current

6.2.5 Volume Estimation

Similar to section 6.1.5, volume estimation is carried out for the completely-modular topology. Fig. 6.19 shows the estimated volume of different circuit components. The same rules are followed for designing magnetic components and dimensions as per the datasheets are utilized to compute the volumes of other components. The total volume comes out to be 0.423 m^3, which is ~25 % higher than the previous topology (as shown in Fig. 6.1). The main

contributor to this rise is the cumulative volume of transformers, which is almost double as compared to the volume of a single transformer used in the previous topology discussed in section 6.1. Higher peak current and RMS current rating is the main cause of the bigger size of the transformers. Sizes of the rectifier stage components remain the same in both topologies. Due to the interleaving, size of the output filter components reduces drastically. As the number of semiconductor increases, the semiconductor volume has also increased. Overall, increase in transformer volume becomes the dominating factor and leads to the increase in system volume.

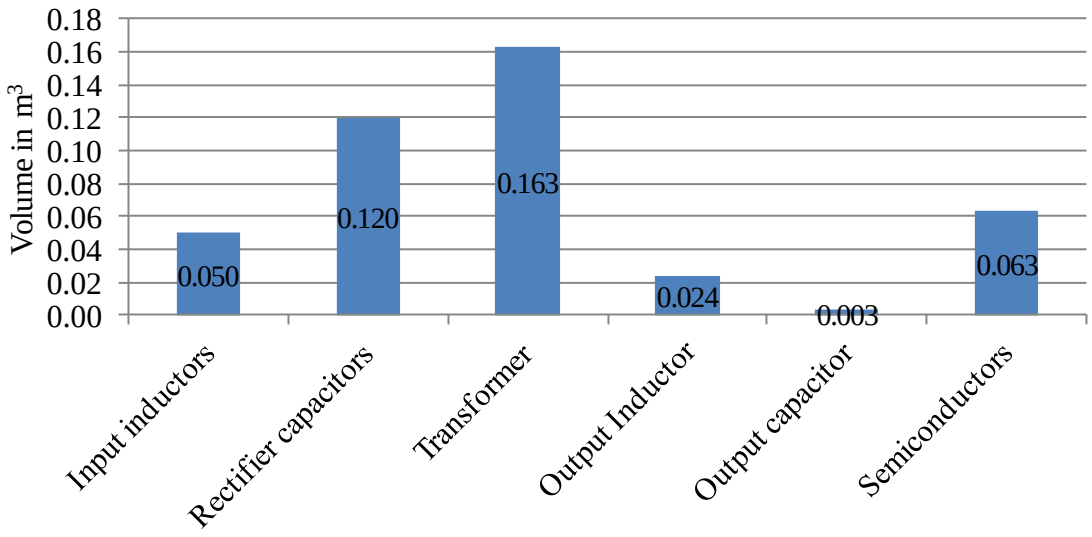


Fig. 6.19 Volume of different components of the power-supply

6.2.6 Efficiency Improvement of H-bridge Section

Recent activities in the field of solid state transformer (SST) have boosted the research interest in high-power high-voltage DC-DC converters [75], [76]. Furthermore, high-power high-voltage DC-DC converters are perceived as a building block of the future high-power converters for applications such as solid-state transformers, medium-voltage drives, battery-storage systems and bulk renewable-energy generation systems etc. [77]. However, there are two significant differences between the high-current variable-voltage (HCVV) applications and SST, i.e. (1) SST requires (mostly) bidirectional power flow and (2) SST output voltage does not vary over a wide range. Due to these reasons, the soft-switched (series resonant) bidirectional isolated dual-active-bridge DC-DC converter is suitable for SST but is less qualified for HCVV applications. A comparison carried out for high power DC-DC soft switched topologies point out that for unidirectional applications the zero-voltage switching (ZVS) phase-shifted full-bridge (PSB)

provides a better efficiency [78]. A Qualitative comparison of ZVS-PSB with discontinuous-current operation of the full-bridge (DCB) is given below (Table 6.3).

Table 6.3 ZVS-PSB vs DCB

	ZVS-PSB	DCB
IGBT turn-on	ZVS	ZCS
IGBT turn-off	ZVS	Hard switching (at peak current)
Rectifier diode turn-off	Hard switching	ZCS
Operation/ comments	Continuous current, higher output filter inductance and additional primary side inductor	Discontinuous current, lower output inductance with high peak current

Therefore, with respect to the semiconductor losses, the main tradeoff lies between the IGBT turn-off losses in DCB and rectifier diode reverse recovery losses in ZVS-PSB. Additionally, as the peak current reduces, the RMS current also reduces in the semiconductor and magnetic component of ZVS-PSB. Therefore, the overall conduction losses reduce. ZVS-PSB will provide zero voltage switching only if the current is continuous, therefore, the output inductance value will have to be increased from its present value to achieve continuous current. This will lead to an increase in core size of the inductor (even though increase in the inductance results into reduction in the peak current, overall effect is the increase in energy stored in the inductor). However, the size of the transformer reduces as the effective current reduces. An estimated variation of the efficiency of the rectifier topology with soft-switched DC-DC converter is given in Fig. 6.20. The distribution of the losses, in various components, is shown in Fig. 6.21. It can be seen that the efficiency improves significantly over the entire load range and especially at the bottom load line and light load conditions. The distribution of losses depicts the shifting of the losses from the H-bridge section to the output diode rectifier and filter inductor.

Although, the output inductor volume increases due to the increased energy rating, the overall volume remains the same due to the reduction in the transformer volume. The new overall system volume is 0.433 m^3.

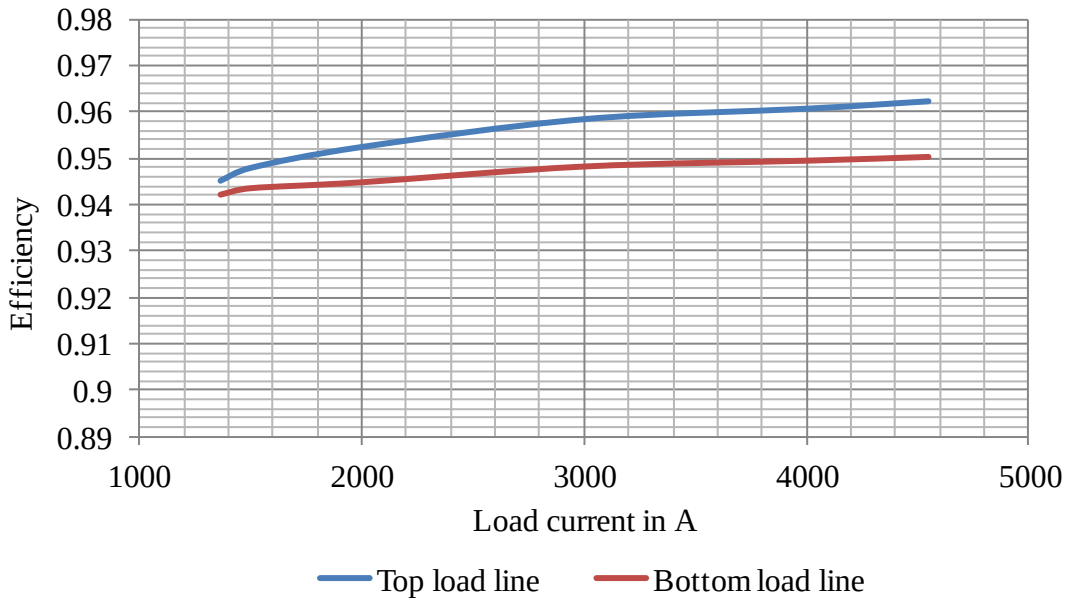


Fig. 6.20 Variation of efficiency with load current with soft-switched DC-DC converter section

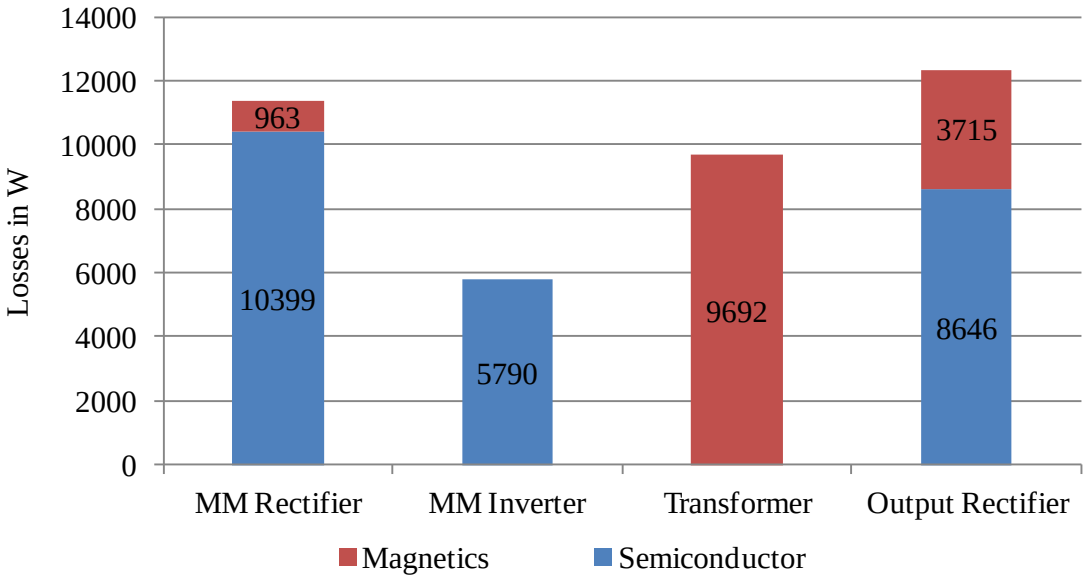


Fig. 6.21 Distribution of power loss in different components with soft-switched DC-DC converter section

6.3 Comparison of Medium-Frequency Transformer Based Topologies with Chopper-Rectifier

A chopper-rectifier with and without input passive filters (as shown in Fig. 5.1 and Fig. 5.8, respectively) can be easily connected to the medium-voltage grid due to the presence of the input transformer. When comparing with the medium-frequency transformer (MFT) based topologies, the chopper-rectifier is at the clear disadvantage in terms of power factor, input power quality

and modularity. However, as a system, the chopper-rectifier has a much simple structure and control. In this section, a comparison of the chopper-rectifier with passive filter (CRPF) and the two MMC-based topologies is discussed with respect to efficiency and size. The topology involving a modular-multilevel rectifier, a modular-multilevel inverter, a medium-frequency transformer and a diode rectifier (as shown in Fig. 6.1) is abbreviated as MMC-1 and the completely modular topology with a soft-switched H-bridge is denoted as MMC-2.

Fig. 6.22 (a) and (b) show the variation of efficiency of the three topologies over the top and bottom load lines, respectively. Clearly with one stage of power conversion less, CRPF provides a better efficiency, even if the MF transformer in the MMC-1 and MMC-2 are designed for higher efficiency as compared to the line-frequency transformer used in the CRPF. Between the MMC based topologies, MMC-1 results in the better efficiency profile because of lower transformer and output rectifier losses. At TLL with full load current, MMC-1 provides a comparable efficiency as CRPF.

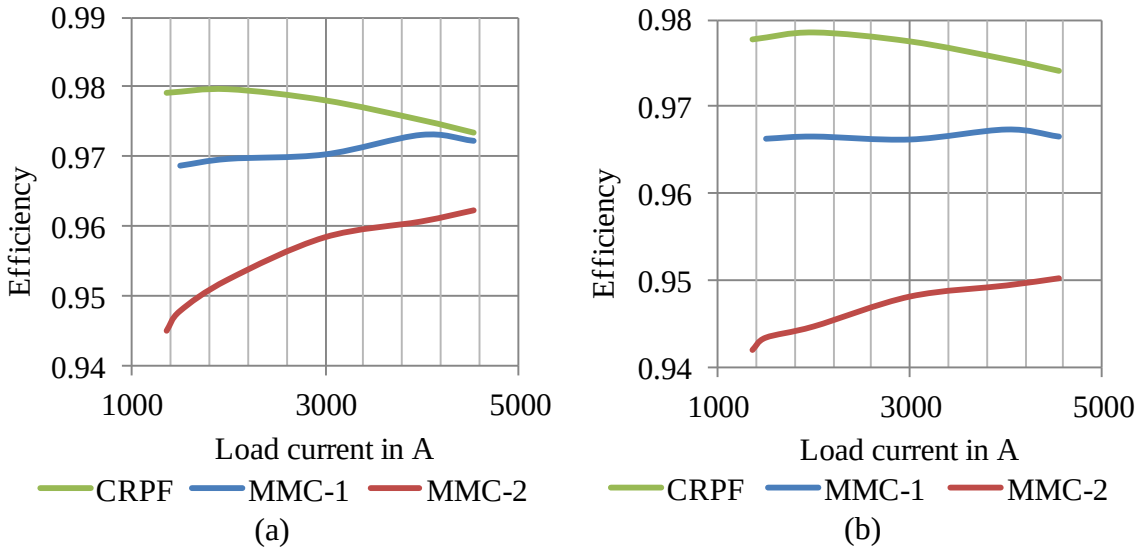


Fig. 6.22 Variation of efficiency for chopper-rectifier and MFT based topologies with the load current over (a) top load line and (b) bottom load line.

As shown in Fig. 6.23, the overall volume of the CRPF is higher than the two MMC based topologies. The biggest difference comes from the size reduction of the transformer. The capacitors used in the chopper cells of the MF transformer-based topologies occupy significant space. This reduces the advantage gained by the transformer size reduction. As discussed previously, due to the transformer, the volume of the MMC-2 comes out to be higher.

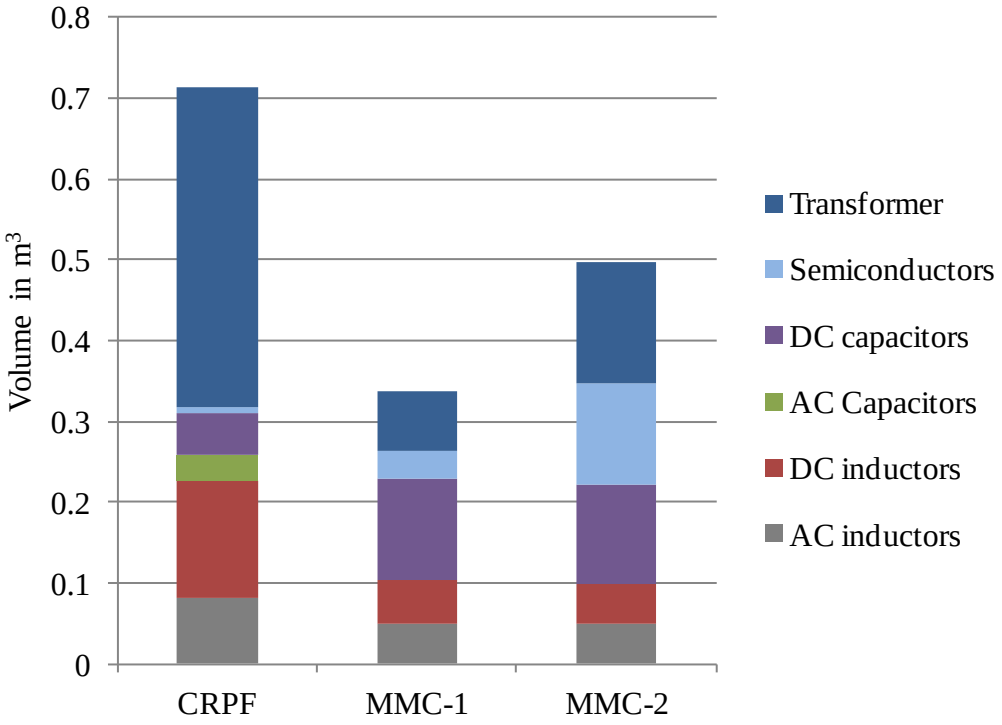


Fig. 6.23 Comparison of sizes of different components of chopper-rectifier and medium-frequency transformer based topologies

As both topologies have been designed to operate at medium voltage level, transformers and other circuit components should be suitably rated for the break-down voltage levels (basic impulse insulation level, BIL). For chopper-rectifier, only input transformer and passive filter need to have appropriate BIL rating (apart from the switch-gear and protection). For MMC based topologies, situation is different. Especially for completely modular topology, each transformer (its connection etc.) have to be rated for required BIL. In this respect, MMC-1 topology is relatively better because of single medium-voltage transformer.

6.4 Summary

Two modular multilevel converter based power supplies for high-current loads are discussed in detail. With active-frontend rectifier, unity power factor is achieved with current THD less than 5 %. Modularity is an added advantage that leads to ease of assembling, expansion and replacement in case of failure. As modular multilevel converters have already achieved inroads in HVDC and high-power drives applications with proven reliability, the same can be expected for the reliability in HCVV applications. A comparison of these MF transformer-based topologies with chopper-rectifier shows that, these topologies perform better in terms of the

power-quality and power factor. Due to the use of MF transformer, the overall size of the system also reduced. However, because of multiple power conversion stages, the efficiency of these topologies comes out to be lower as compared to the chopper-rectifier.

With respect to these findings, it can be said that the size of the system can be further reduced by increasing the frequency of operation; however, this leads to the higher losses. Therefore, a scope exists for further work to reduce switching losses by means of suitable soft switching techniques. Moreover, losses can be reduced with the help of wide band gap devices. This work, investigated two advanced topologies (with medium-frequency transformer) that provides the stepping stone for further investigation in terms of new topologies, utilizing different multi-level converters and other configurations.

7. Conclusions

In the present work on ‘High Power Factor High-Current Variable-Voltage Rectifiers,’ contributions are made in the fields of compensating devices and advanced medium-frequency transformer based topologies. Each chapter includes a summary section, in which, main findings are highlighted. Therefore, this chapter is kept brief. The main conclusions from the study are the following:

Voltage sequence control-based rectifier topology, with optimised transformer turns-ratio and passive filter, results in reduction of the reactive power rating of the passive filter. Moreover, the system provides high power factor over the wider load range as compared to the standard six-pulse thyristor rectifier. Design rules are formed after the optimisation exercise and the same are verified with a 62.5 kW experimental system. However, there are some limitations such as fixed reactive power compensation, poor input current THD and higher number of components. Due to these reasons, the topology is suitable for low-power (less than 500 kW) applications connected to the distribution-level voltage grid.

For HCVV applications, suitability of the multi-pulse thyristor rectifier with the hybrid filter (dominant-harmonic passive filter and DSTATCOM) is demonstrated with simulation and experimentation. A Power factor greater and 0.98 and TDD less than 5 % are achieved for an electrolyser load for the required range of operation. The comparison of the 12-pulse thyristor rectifier with hybrid filter based (TRHF) and the chopper-rectifier with passive filter (CRPF) has concluded that the CRPF results in better efficiency and lower volume. However, as the thyristor rectifiers are the main work horse of the industry, proposed hybrid filter approach can be suitably applied to retrofit applications to achieve power quality improvements.

Proposed advanced topologies, incorporating medium-frequency (MF) transformer/transformers and an active front-end rectifier, have demonstrated improvement in the input power quality and power factor. Additionally, the volume of the system reduces due to the replacement of line-frequency transformer with medium-frequency transformer. Moreover, these topologies are modular. A comparison of these MF transformer-based topologies with

chopper-rectifier clearly establishes their superiority in terms of size and power quality; however, these topologies lead to lower efficiency as compared to the chopper-rectifier. There is a lot of scope for research in the field of modular topologies in terms of new configurations, use of wide-band-gap devices and soft-switching techniques.

Appendix A: Semiconductor Loss Estimation

In this work, semiconductor losses are estimated using MATLAB and PLECS models. For calculation of the conduction losses of a semiconductor device, the on-state characteristic of the device from the datasheet is inputted in a form of look-up table to the PLECS model. These characteristics can be inputted for different values of the device junction temperature. Depending on the instantaneous temperature T and current flowing through the device, instantaneous voltage drop is interpolated with the help of look-up table. The instantaneous power loss (multiplication of instantaneous voltage and current) is then averaged over a time period T_s to compute the conduction loss of the semiconductor device $\bar{p}_{cdev}$, which is given as:

$$\bar{p}_{cdev} = \frac{1}{T_s}\int_0^{T_s} v_{dev}(i_{dev}, T, t) i_{dev}(t)\mathrm{d}t \tag{A.1}$$

where $v_{dev}(i_{dev}, T, t)$ and $i_{dev}(t)$ are the instantaneous values of voltage drop across semiconductor device. In the present study, the on-state characteristics of the devices are inputted for a maximum junction temperature i.e. 125°C.

The turn-on and turn-off losses are also computed in a similar manner. The energies involved in the switching process (E_{on} and E_{off}) are inputted as three-dimensional look-up tables with respect to the device off-state voltage v_{offdev} and on state-current i_{ondev}. The data is inputted corresponding to a maximum junction temperature i.e. 125°C. Cumulative energy over a period of time divided by the time period gives the total switching losses. The same can be represented as:

$$\bar{p}_{sdev} = \frac{1}{T_s}\sum E_{on}(v_{offdev}, i_{ondev}) + \frac{1}{T_s}\sum E_{off}(v_{offdev}, i_{ondev}) \tag{A.2}$$

For diodes, turn-on losses are negligible and therefore ignored and only the reverse recovery losses are considered.

Appendix B: Design of Magnetic Components

The design and development of high-power medium-frequency transformer is currently a matter of interest for many researchers [79], [81]. There exist many challenges in terms finding the suitable core material (and its handling), predicting and controlling parasitics and estimation of losses. To deal with each of these aspects, a detailed study is required, which is not in the scope of this work. However, to evaluate and compare various topologies, the performance of the magnetic components has to be taken into account. A uniformity has to be maintained with respect to assumptions, materials and design procedure. Without going deep into the challenges of medium- and low-frequency transformer design, a standard approach including the area product calculation is taken here to design the transformers. In this appendix, basic design approach and assumptions are discussed for a single-phase medium frequency transformer [19], [20], [79]. Three-phase transformer can also be designed similarly. Following are the steps:

1. For line-frequency transformers, cold rolled grain oriented steel M6 (Saturation flux density B_{sat}=2.0 T) is used and high silicon steel 10JNEX900 (B_{sat}=1.8 T) is used for medium-frequency transformers [80], [81]. Maximum flux density B_m is selected as 1.0 T and 0.55 T for line-frequency and medium-frequency transformers, respectively.
2. Current density J is 4×10^6 A/m^2 and winding fill factor k_w of 0.5 is selected.
3. Area product A_p is defined as the product of cross section area of core A_c and area of window A_w. It is computed using cumulative apparent power rating S, form factor of voltage k_f, maximum flux density B_m, winding-factor k_w, rated current density J and frequency f. The expression of area product is given as:

$$A_p = A_c A_w = \frac{S}{4k_f k_w J B_m f} \tag{B.1}$$

4. In general, the next step of transformer design procedure is to select the core matching the area-product requirement. However, most of these transformers are custom/specially designed, finding an off-the-shelf core is difficult. Therefore, a different approach is taken, in which, primary number of turns is selected iteratively (using computer program) to achieve minimum overall (core and copper) losses.

5. With primary number of turns N_1 and primary voltage V_{pri} the cross-section area of core is computed as:

$$A_c = \frac{V_{pri}}{4k_f N_1 f B_m} \tag{B.2}$$

6. Window area is computed using area product and cross section area of the core as:

$$A_w = \frac{A_p}{A_c} \tag{B.3}$$

7. E-core is selected for designing the transformers and middle limb and window geometry is assumed to be square in shape, initially. Using these assumptions, the core dimensions are computed as:

$$\begin{aligned} a_c &= \sqrt{A_c} \\ a_w &= \sqrt{A_w} \end{aligned} \tag{B.4}$$

where a_c and a_w are the width of the middle limb and width of the window, respectively.

8. From core geometry, the mean length of the turn l_{mt} in computed. Moreover, using current density and primary and secondary rated currents (I_1, I_2), required areas of the copper conductor cross sections (A_1 and A_2) is computed. With mean length of turn and number of turns, lengths of the primary and secondary wires (l_1 and l_2) are computed as:

$$l_{mt} = 4(a_c + a_w) \tag{B.5}$$

$$\begin{aligned} l_1 &= N_1 l_{mt} \\ l_2 &= N_2 l_{mt} \end{aligned} \tag{B.6}$$

$$\begin{aligned} A_1 &= I_1 / J \\ A_2 &= I_2 / J \end{aligned} \tag{B.7}$$

9. Using wire lengths, conductor cross section areas, copper resistivity ρ and skin-depth δ, resistances of primary and secondary windings can be computed as:

$$\begin{aligned} r_1 &= \rho \frac{l_1}{\sqrt{4\pi A_1}\delta} \\ r_2 &= \rho \frac{l_2}{\sqrt{4\pi A_2}\delta} \end{aligned} \tag{B.8}$$

10. Copper loss is computed depending on the values of winding resistances and RMS currents as:

$$p_c = I_1^2 r_1 + I_2^2 r_2 \tag{B.9}$$

11. With core geometry the core volume V_i is computed. Using datasheet of the core material (material constants: ρ_i, K_i, α, β), core/iron loss p_i is computed as (according to Steinmetz's equation):

$$p_i = V_i \rho_i K_i f^{\alpha} B_m^{\beta} \tag{B.10}$$

12. Number of turns and core geometry is adjusted to achieve good balance in core and copper losses and minimization of overall losses. Based on final geometry and number of turns, the previously computed parameters and losses are finalized.
13. Leakage inductances (L_{l1} and L_{l2}) can be computed in terms of winding volume V_w and winding height h_w as [79]:

$$L_{l1} = \mu_0 \frac{N_1^2 V_w}{3h_w^2}$$
$$L_{l2} = \mu_0 \frac{N_2^2 V_w}{3h_w^2} \tag{B.11}$$

14. With dimensioned defined in Fig. B.1, overall volume (Length×Height×Width) of the transformer is computed.

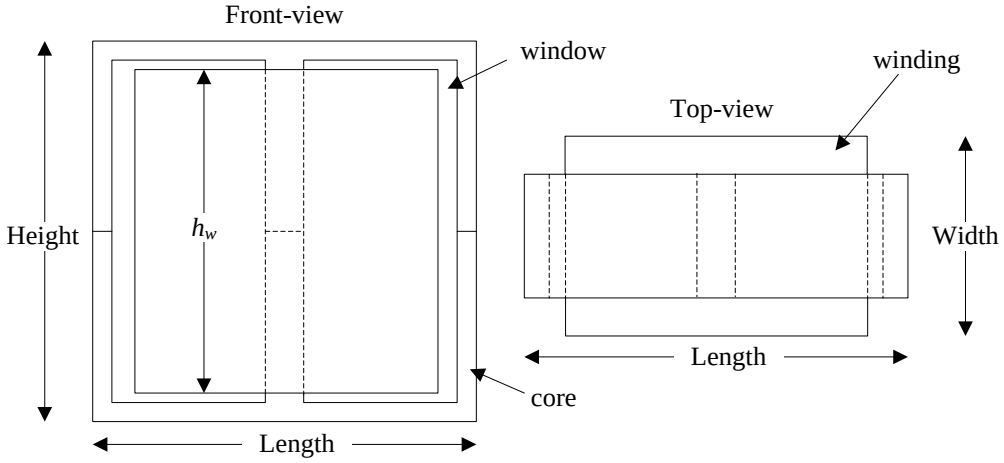


Fig. B.1. Transformer front and top view.

Appendix C: Performance of 188 kW Chopper-Rectifier

In this appendix, performance of a 188 kW industrial chopper-rectifier is discussed in brief. The unit is developed in corporation with the industrial partner for commercial purposes. Results and waveforms from this unit are included to provide a perspective about the performance of large power chopper-rectifier. Fig. C.1 shows the circuit diagram of the unit. System parameters are provided in Table C.1. At the input side a 12-pulse rectifier provides AC to DC conversion. Two semi-controlled rectifiers are used to limit the inrush current in a DC capacitor bank connected at the rectifier output side. The rectifier DC bus voltage is selected to be 273 V, to minimize the overall losses. A single-phase chopper is used to feed the electrolyser load. The rated load voltage and current are 209 V, 900 A, respectively. To provide the required load current, 8 IGBTs (1200 V, 300 A, Semikron SKM300GB12) are paralleled (dual IGBT leg is used due to the availability in the stock, however lower IGBT is not gated). Switching frequency is kept at 5 kHz. At the output side, 87.5 µH inductor and 8.4 mF capacitor are used to achieve load voltage ripple of less than 5 %. A diode is used at the output side to avoid back flow of the current from the electrolyser.

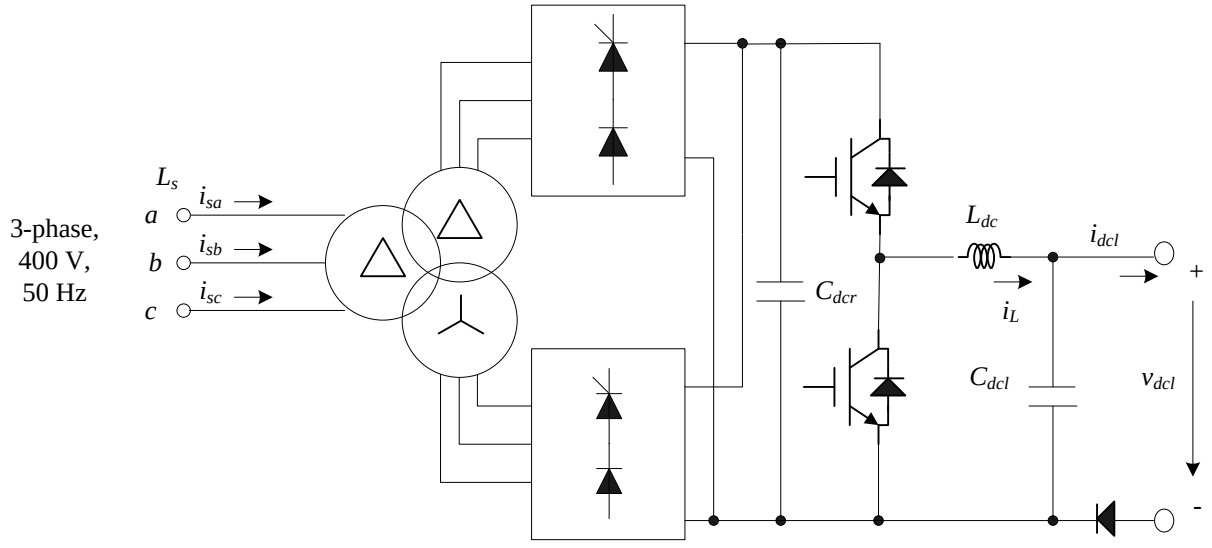


Fig. C.1. Circuit diagram of the chopper-rectifier.

Table C.1. System parameters

Supply	400 V ± 5 %, 50 Hz
Transformer	225 kVA, 400 V/195 V, leakage reactance=6 %
Rectifier	Switch: TD180N, C_{dcr}: 5.04 mF (12×420 µF)
Chopper	Switch: SKM300GB12 (8 in parallel), L_{dc}: 87.5 µH, 1200 A, C_{dcl}: 8.4 mF (20×420 µF), switching frequency: 5 kHz
Output Diode	DZ1070N (2 in parallel)

Fig. C.2 shows the waveforms of input line-to-line voltage, input current, output voltage and inductor current at the full load (output voltage: 209 V, current: 900 A). A typical 12-pulse behavior can be observed from the input current waveform. The output current has ripples corresponding to the switching frequency and six times the line frequency. This is because the controller is purposefully kept slow and bandwidth is also limited as load does not require high dynamics.

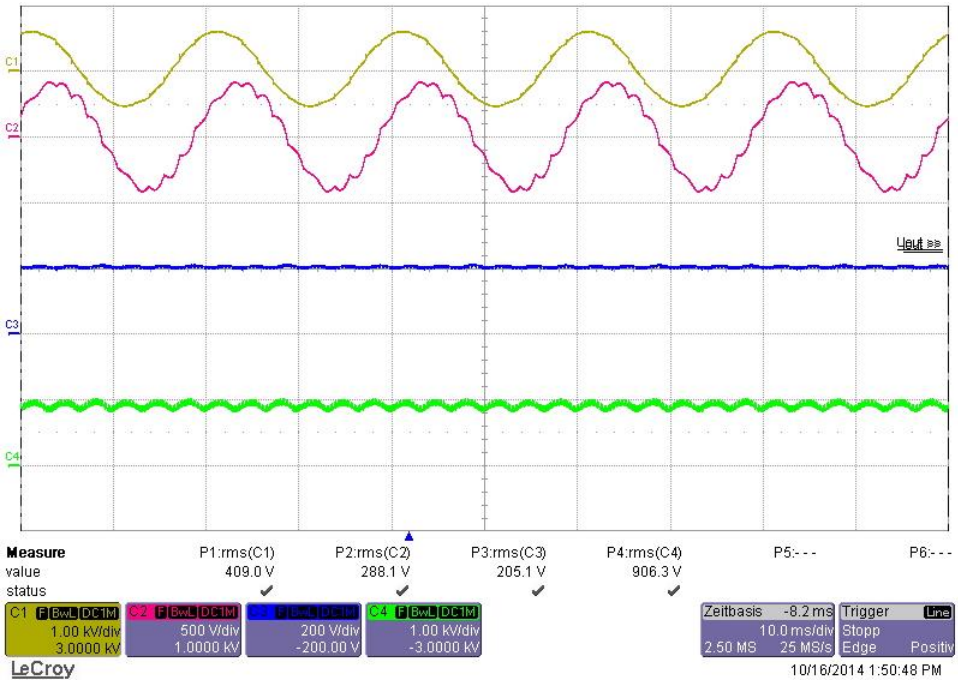


Fig. C.2. Waveforms showing Ch.1 (yellow): input line-to-line voltage v_{ab} (1 kV/div.), Ch.2 (red): input phase-*a* current i_{sa} (500 A/div.), Ch.3 (blue): output voltage v_{dcl} (200 V/div) and Ch.4 (green): inductor current, i_L (1 kA/div). Time scale: 10 ms/div.

Variation of the power factor and input current THD is shown in Fig. C.3 (a) and (b). As the exact characteristic of the electrolyser was not available, experiment was carried out with fixed resistive load (209 V/900 A). The power factor and current THD comes out to be poor as compared to the results obtained with 20 kW experimental system (as shown in Fig. 5.6 and Fig.

5.7). This is because the input 12-pulse rectifier is controlled differently in the present case as compared to the experimental system. In the present 12-pulse rectifier, the DC currents from star and delta rectifiers are not controlled to be equal. There are two different controllers (master and slave), used to generate the firing angles for input semi controlled rectifiers. The master controller senses the rectified voltage and set the equal firing angles for master and slave controller. Therefore, AC currents in star and delta windings differ, hence the higher current THD and poor power factor. Never the less the input power factor remains above 0.95 till 50 % load current (25 % load power), which meets the customer requirements.

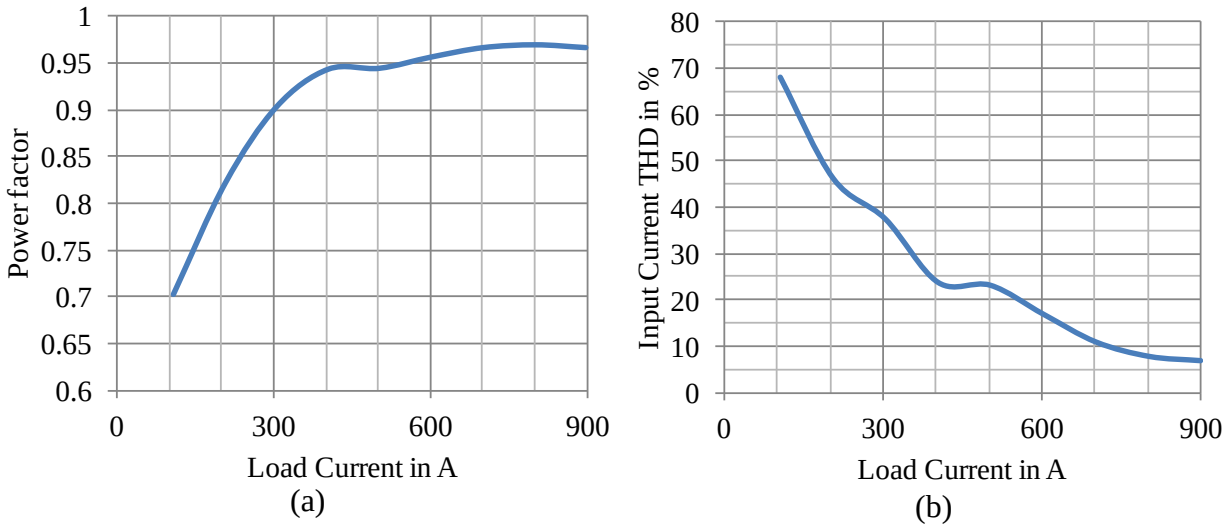


Fig. C.3 With respect to load current, variation of (a) power factor and (b) input current THD.

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