UNIVERSITÄT PADERBORN
Die Universität der Informationsgesellschaft

FAKULTÄT FÜR
ELEKTROTECHNIK,
INFORMATIK UND
MATHEMATIK

Compact Storage-Based Resistance Spot Welding Power Supplies

Von der Fakultät für Elektrotechnik, Informatik und Mathematik
der Universität Paderborn

zur Erlangung des akademischen Grades

Doktor der Ingenieurwissenschaften (Dr.-Ing.)

genehmigte Dissertation

von

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Tag der mündlichen Prüfung: 21.10.2016

Paderborn, 2016

Diss. EIM-E/326

Abstract

Compact Storage-Based Resistance Spot Welding Power Supplies

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Storage-Based Resistance Spot Welding Power Supplies (SBRSWPS) are useful in eliminating certain drawbacks of their counterparts without an energy storage element. Till date, the state of the art in SBRSWPS is limited to Capacitor Discharge Welding (CDW). Uncontrolled mode of discharge makes it mandatory to use foil capacitors and a heavy transformer (due to high volt-sec and peak current requirement), which make the CDW systems bulky and heavy.

The extremely small welding time (less than 10 ms) supported by CDW is indeed beneficial in welding high thermal conductivity materials (like aluminium). However, the welding duration can be increased, and the welding current can be reduced in most of the cases which involve materials like iron (sheets). This, additional degree of freedom gives an opportunity to explore the possibility of a new category of SBRSWPS. This new category of welding machines can be characterised by a more compact storage system, coupled with a high-frequency power supply.

The first step in this direction involves the analysis and selection of a suitable power supply topology. The next step involves the selection of the type of energy storage and its dimensioning where one can think of replacing foil capacitor storage with more compact options such as Electrolytic Capacitor Storage (ECS), Double Layer Capacitor Storage (DLCS) or a Flywheel Storage System (FSS).

The thesis starts with the specifications of the desired SBRSWPS, followed by an evaluation of a set of suitable power supply topologies. After a careful pre-selection of suitable storage systems, a detailed analysis and comparison between ECS, DLCS and FSS with respect to the application under consideration is presented. Practical results from a DLC based SBRSWPS prototype (developed as a proof of concept) are also presented. Finally, the important conclusions drawn, along with some suggestions for future work are put forward.

Zusammenfassung

Compact Storage-Based Resistance Spot Welding Power Supplies

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Das speicherbasierte Widerstands-Punkt-Schweißen eliminiert eine Reihe von Nachteilen der speicherlosen Schweißsysteme. Heutzutage ist das Kondensator-Entladungs-Schweißen Stand der Technik bei speicherbasierten Schweißsystemen. Die hohen ungeregelten Impulsströme und Spannungszeitflächen erfordern jedoch Folienkondensatoren und schwere Transformatoren, die das Gesamtsystem sperrig und schwer machen. Diese Schwächen lassen sich durch geregelte Leistungssteller beheben.

Für Metalle mit hoher thermischer Leitfähigkeit (z.B. Aluminium) ist in der Tat ein Impuls-Schweißvorgang (<10 ms) vorteilhaft, wofür die Versorgung durch einem Impulskondensator prädestiniert ist. Für Metalle wie Stahl hingegen kann der Schweißvorgang verlängert werden und mit reduziertem Strom erfolgen. Dieser Freiheitsgrad ermöglicht es, auf eine alternative Schweißstromquelle zu setzen, die sich durch einen kompakten Energiespeicher und eine hohe Schaltfrequenz auszeichnet.

Die Annäherung an eine solche Lösung führt zunächst zur Auswahl einer geeigneten Schaltungstopologie sowie deren Analyse und Auslegung. Der nächste Schritt adressiert die Gegenüberstellung kompakter Speichertechnologien wie z.B. Schwungradspeicher, Elektrolyt- oder Doppelschicht-Kondensatoren. Die vorliegende Dissertation beginnt mit der Spezifikation der Schweißstromquelle sowie der Bewertung geeigneter Schaltungstopologien. Nach einer Vorauswahl des Speicherprinzips erfolgen eine genaue Analyse und ein Vergleich zwischen Elektrolyt- und Doppelschicht-Kondensatoren sowie Schwungradspeichern hinsichtlich der Anforderungen für eine Schweißstromquelle. Eine praktische Verifikation erfolgt durch einen Prototyp der Schweißstromquelle mit Doppelschichtkondensatoren. Abschließend werden die Ergebnisse zusammengefasst und Empfehlungen für Weiterentwicklungen gegeben.

Acknowledgements

This work will certainly not be complete unless acknowledgements are paid to all those who have helped me in presenting this thesis in its present form. It is a great pleasure to express my gratitude to Prof. Dr.-Ing. Joachim Böcker, whose esteemed guidance played a key role during the process of this research work.

It is a great pleasure to thank my immediate supervisor Dr.-Ing. Norbert Fröhleke for his valuable and inspiring guidance, comments, suggestions and encouragement towards the completion of this thesis. Special thanks to Prof. Dr.-Ing. Jürgen Petzoldt who has spent a lot of time and efforts in reviewing my manuscript. I would also like to pay my sincere acknowledgements to all the committee members for their kind support towards the realization of this dissertation.

I would also like to extend my gratitude to all my colleagues of the department of LEA at the University of Paderborn, for their valuable suggestions and constructive criticism. Finally, I would like to dedicate this work to my family and especially my wife for supporting me at a personal and emotional level, without which, this thesis could have not been possible.

Contents

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List of Acronyms

Symbol	Description
BCR	Buck Controlled Resonant
BLDC	Brushless DC motor
CDW	Capacitor Discharge Welding
CPS	Charging Power Supply
DF	Dissipation factor
DLC	Double Layer Capacitor
DLCS	Double Layer Capacitor Storage
ECS	Electrolytic Capacitor Storage
EMI	Electromagnetic Interference
EOL	End of Life
ESR	Equivalent Series Resistance
FSS	Flywheel Storage System
IBC	Interleaved Buck Converter
IBCRC	Interleaved Buck Controlled Resonant Converter
ICT	Inter-Cell Transformer
ICTBC	Inter-Cell Transformer based Buck Converter
IM	Induction Motor
IPMSM	Integrated Permanent Magnet Synchronous Motor
IPSFBC	Interleaved Phase-Shifted Full-Bridge Converter
ITIBC	Interleaved Tapped-Inductor Buck Converter
L.H.S	Left Hand Side
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
NL	Nominal-Load (Welding power of 50 kW)
PL	Peak-Load (Welding power 100 kW)
PLC	Programmable Logic Controller

PSFB	Phase-Shifted Full-Bridge
PWM	Pulse Width Modulation
R.H.S	Right Hand Side
RMS	Root Mean Square
RSW	Resistance spot welding
SBRSW	Storage-Based Resistance Spot Welding
SBRSWPS	Storage-Based Resistance Spot Welding Power Supply
SMD	Surface Mount Device
SOL	Start of Life (Beginning of life)
SPMSM	Surface Mount Permanent Magnet Synchronous Motor
SRM	Switch Reluctance Motor
SyRM	Synchronous Reluctance Motor
TIBC	Tapped-Inductor Buck Converter
VRM	Voltage Regulator Module
WPS	Welding Power Supply

List of Symbols

a_{ratio}	Aspect ratio
A	Circumferential ampere loading
B_{avg}	Spacial average of the absolute value of air-gap flux density
B_{m}	Peak flux density
$B_{\text{m,ag}}$	Peak flux density in the air-gap of the motor
d	Small Variation in duty-cycle
D	Duty-cycle
D_{TI}	Duty-cycle of tapped-inductor buck converter
DF_{lf}	Low-frequency dissipation factor
E_{fw}	Total energy that needs to be stored in the flywheel
E_{Smax}	Usable component of stored energy in a storage system
Ed_{ec}	Energy density of an electrolytic capacitor
Ed_{fw}	Volumetric energy density of flywheel
f_{e}	Electrical frequency
f_{s}	Switching frequency
i_{L}	Small variation in the buck converter inductor current (averaged over one switching cycle) resulting from a small variation in duty-cycle
I_{c}	RMS value of capacitor current
I_{d}	d axis terminal current
I_{DLCn}	Output current of the DLCS at nominal-load
I_{DLCp}	Output current of the DLCS at peak-load
I_{dm}	d axis magnetising current
I_{q}	q axis terminal current
I_{qm}	q axis magnetising current
I_{k}	RMS value of k^{th} harmonic frequency component of the ripple current
I_{load}	Load current

ΔI_{load}	Load current ripple
I_{L}	Output current of a single buck converter
I_{L}^{*}	Current reference of a single buck converter
J	Moment of inertia of flywheel
K_{v}	voltage de-rating factor (rated voltage/applied voltage)
K_{w}	Motor winding factor
l_{fw}	Length of flywheel
l_{m}	Motor length
l_{r}	Rotor length
L	Stator magnetising inductance for a SPMSM
L_{b}	Buck converter inductance
L_{exp}	Expected life of electrolytic capacitor
L_{ESL}	Equivalent series inductance of an electrolytic capacitor
L_{lk}	Sum of leakage inductance of all the transformers in an inter-cell transformer based buck converter
L_{load}	Load inductance
L_{o}	Specified life time at maximum core temperature limit
m_{fw}	Mass of flywheel
m_{stator}	Mass of the stator yoke
p	Number of poles
P_{capL}	Capacitor power losses
P_{cdh}	Core losses during discharge phase
P_{crtd}	Rated core losses
P_{cudh}	Copper losses during discharge phase
P_{curtd}	Rated copper losses
P_{in}	Motor terminal power input
$P_{\text{in,dch}}$	Motor terminal power during discharge (during welding)
P_{omax}	Maximum output power from a voltage source
P_{sL}	Losses in the storage system corresponding to P_{weld}
P_{Smax}	Maximum output power capacity of the storage system
P_{m}	Motor power rating
$P_{\text{mech,ch}}$	Mechanical power that needs to be generated during charging

P_{mloff}	Motor losses during the interval between consecutive weldings (charging phase)
P_{mlw}	Motor losses during welding
P_{mlrated}	Motor losses under rated load conditions
$P_{\text{mlw,PL}}$	Motor losses during peak welding load
P_{weld}	Welding power
P_{WPSL}	Welding power supply losses corresponding to P_{weld}
$P_{\text{WPSip,PL}}$	Input power of the welding power supply at peak-load
r_{b}	Equivalent resistance of a synchronous buck converter
r_{fw}	Radius of flywheel
$r_{\text{fw,max}}(\omega)$	Maximum flywheel radius allowed at an angular speed ω
r_{im}	Rotor radius ($\approx$ motor bore radius)
r_{m}	Motor radius
R_{cu}	Winding resistance per phase
R_{DLC}	Low-frequency series resistance of DLCS
R_{ESR}	Equivalent series resistance of an electrolytic capacitor
R_{ESRhf}	High-frequency equivalent series resistance of an electrolytic capacitor
R_{i}	Virtual resistance to mimic the motor core losses
R_{P}	Equivalent parallel resistance of an electrolytic capacitor
R_{s}	Internal source resistance
$R_{\text{thc-case}}$	capacitor core to case thermal resistance
t_{w}	Weld duration
t_{woff}	Time gap between two consecutive weldings
T_0	Maximum rated ambient temperature
T_{x}	Ambient temperature
ΔT_0	Capacitor core to ambient temperature difference at rated current
$T_{\text{p}}(s)$	Plant transfer function for a buck converter (output current to duty-cycle)
$[T_{\text{p}}(s)]_{R_{\text{s}}}$	Plant transfer function for a buck converter with a source resistance (output current to duty-cycle)
ΔT	Capacitor core to ambient temperature difference
ΔT_{m}	Difference between the ambient and peak hot-spot temperature in the motor, for the given charge - discharge loading

ΔT_{mv}	Difference between the ambient and valley of the hot-spot temperature corresponding to intermittent loading
$\Delta T_{\mathrm{rated}}$	Difference between the ambient and peak hot-spot temperature when running under rated conditions
V_{d}	d axis terminal voltage
V_{DLC}	Charged state open circuit voltage of the DLCS
V_{m}	Rated phase voltage of the motor (peak)
V_{max}	Terminal voltage limit (peak)
V_{o}	Average output voltage across load resistance
V_{q}	q axis terminal voltage
V_{r}	Rated capacitor voltage
V_{s}	Source voltage
W	Warburg impedance
η	Rated efficiency of the motor
η_{DLCp}	Efficiency of the DLCS at peak-load
η_{DLCn}	Efficiency of the DLCS storage at nominal-load
ψ_{d}	d axis flux linkages
ψ_{p}	Permanent magnet flux linkages
ψ_{q}	q axis flux linkages
υ_{ec}	Capacitor volume
υ_{eff}	Effective volume of the flywheel storage system
σ_{m}	Tensile strength of the material
τ_{m}	Thermal time constant of the motor
γ	Poissons ratio
ω_{e}	Electrical rotational velocity
ω_{m}	Rated speed of the motor

Chapter 1

Introduction and Thesis Overview

1.1 Background

Resistance spot welding (RSW) is one of the most important processes in automotive industry, especially during the car body manufacturing phase. In this process, work pieces (metal sheets) are held together with localized high pressure at a particular point and an electric current is passed for a short time duration. The heat developed by the resistance to the electric current forms a molten region between the work pieces, at the point where the high pressure is applied. When the molten region cools, the work pieces are welded together.

RSW falls into the category of pulsed power applications. The power demand during welding can be as high as 100 kW and the duration of welding is usually less than 500 ms. The minimum time gap between two consecutive weldings is usually greater than five seconds.

As shown in Fig 1.1, a conventional RSW power supply consists of an AC to DC converter which converts the three phase AC grid voltage to a DC voltage (DC link) and a DC to DC converter, which is responsible for generating a low voltage (less than 5 V) and high current (approximately 20 kA) as required by the welding load.

Such an arrangement suffers from two major disadvantages

1. High ratio of peak to average power loading on the AC mains and
2. The voltage transients (swells, sags, brownouts etc) on the grid have an influence on the welding quality. Sometimes, this can also result in unwanted delays in production lines of automotive parts.

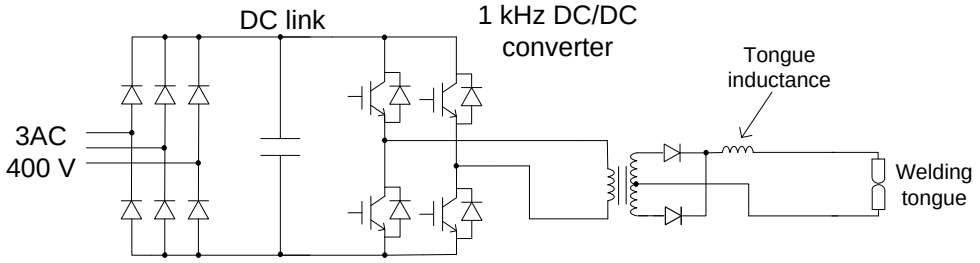


Fig. 1.1: A conventional resistive spot welding power supply.

In order to overcome these disadvantages, it is useful to add an energy storage element in between (as shown in Fig 1.2), where energy is extracted from the grid at a slow rate and stored. The stored energy in turn is used up at a high power, during the RSW process. Such a system is termed as a Storage-Based Resistive Spot Welding Power Supply (SBRSWPS).

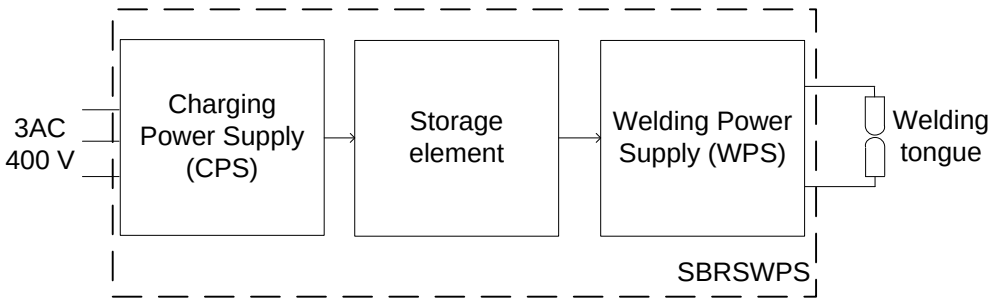


Fig. 1.2: A storage-based resistive spot welding power supply.

As shown in Fig 1.2, a storage-based resistance spot welding system consists of a Charging Power Supply (CPS), a storage element and a Welding Power Supply (WPS). The WPS is rated for the load power while the CPS can be designed for a fractional value of the WPS rating.

1.2 Storage-based welding power supply - state of the art

As shown in Fig 1.3, the state of the art of SBRSWPS is the Capacitor Discharge Welding (CDW) method. CDW is characterized by very short welding times. The capacitor bank (usually composed of foil capacitors) is charged at a slow rate, using a charging circuit, so that the input mains does not experience the extreme peak power loading as in case of a conventional system. The charging circuit consists of a three phase diode bridge, which is connected to the 3AC 400 V mains. The resulting DC voltage (approximately 580 V) is boosted using an additional full bridge based high-frequency DC to DC converter to charge the foil capacitor bank.

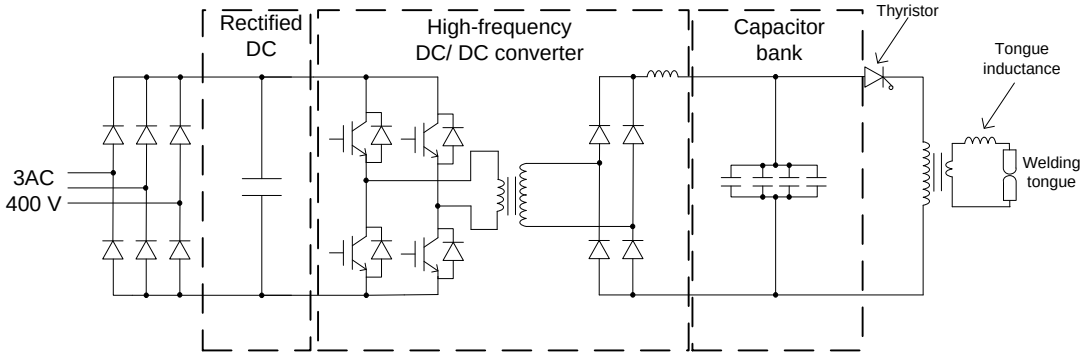


Fig. 1.3: State of the art of storage-based resistive spot welding power supply. This is also called capacitor discharge welding.

When the capacitor bank is fully charged (to a maximum of approximately 3 kV), it is switched to a welding transformer, using a thyristor switch. This transformer steps down the capacitor voltage to a voltage of approximately 20 V (maximum open circuit voltage) and simultaneously produces a welding current greater than 100 kA. The welding duration is also extremely small (smaller than 10 ms). Though this configuration results in extremely high weld quality due to localised heating (because of short welding times and high currents), it suffers from the following disadvantages.

1. High cost and weight of the transformer
2. Capacitors need to be rated to handle repetitive high peak discharge currents, which make the solution bulky and expensive.

The extremely small welding times supported by CDW are indeed beneficial in welding high thermal conductivity materials (like aluminium). However, the welding duration can be increased, and the welding current can be reduced in most of the cases which involve lower thermal conductivity materials such as iron etc. The reduction in peak welding currents results in a greater design flexibility, in terms of power converter topology and storage system selection. This thesis explores the possibility exploiting the additional flexibility in order to build a new category of SBRSWPS with the following desired characteristics.

1. High-frequency WPS (for reduced size) with fully controllable welding current
2. A storage system which is less bulkier than that used in CDW
3. Capability of producing controlled load current pulses for durations in the order of 5-500 ms.

The objective of the first desired characteristic is to reduce the size and weight of the WPS, so that it can be easily placed on a robot that needs to perform a number of manoeuvres in an automotive production line. The objective of the second desired characteristic is to save valuable space in an industrial production set-up. While, the objective of the third desired characteristic is to provide the user with a flexibility to tightly control the quality of welding, depending on the welded material, thickness of the sheets etc. With reference to Fig 1.2, this thesis concentrates itself, only on the design and analysis of WPS and the storage element, which are the most critical parts of the SBRSWPS. The design of the CPS lies out of the scope of this thesis.

1.3 Research objectives

The objectives of this research are

1. To analyse and select a suitable power electronic topology and control strategy for the WPS with the previously mentioned characteristics.
2. Evaluate electrolytic capacitors, Double Layer Capacitors (DLCs) and Flywheels as storage elements and propose the best energy storage option for SBRSWPS.

1.4 Dissertation Outline

In order to exemplify the path towards achieving the stated research objectives, this dissertation is outlined as follows. Chapter 2 presents the specifications and characteristics of the desired SBRSWPS. The analysis which follows in the remaining chapters will be based on these specifications. The state of the art in low voltage and high current power supplies is presented in Chapter 3. Each of the topologies is studied with respect to the requirements specified in Chapter 2 and conclusions drawn are also presented. Chapter 4 presents the analysis of Electrolytic Capacitor based Storage (ECS), Double Layer Capacitor based Storage (DLCS) and Flywheel Storage System (FSS) for the SBRSWPS under consideration. Conclusions from the resulting analysis are finally summarised in this chapter. Implementation of a WPS prototype based on DLCS is discussed and the corresponding results are presented in Chapter 5. Chapter 6 concludes the thesis, summarising the findings of this research work. Appendix A provides some information which was used for performing magnetic volume calculations for different power electronic topologies that were considered. Additional information in relation to FSS basics are provided in Appendix B.

Chapter 2

Specifications of the desired power supply

2.1 Introduction

This chapter specifies the characteristics of the desired high-frequency SBRSWPS. The presented performance characteristics of the new category of SBRSWPS have been developed in coordination with NIMAK GmbH, as part of the research project funded by the Federal Ministry of Economic Affairs and Energy within the ZIM program. These specifications are in general desirable by an SBRSWPS unit used in serial production of cars and automotive parts. The basis of the output current and voltage specifications come from the state of the art, non-storage-based 1 kHz power supplies, which are mounted on welding robots. Topology selection and storage system analysis during the course of the remaining part of this thesis are performed with respect to these specifications. Thus, this chapter serves as a baseline for the analysis throughout this document.

2.2 Output characteristics

The load voltage and the current requirement curves for the desired SBRSWPS are shown in Fig 2.1 (Source: NIMAK GmbH).

The objective is to maintain a high current (approximately 20 000 A) at low voltage (less than 5 V) for a specified duration. The initial period of relatively higher voltage (approximately 20 V) and lower current (approximately 5000 A) is due to the oxide layers on welding elements. This oxide layer presents an additional resistance during the

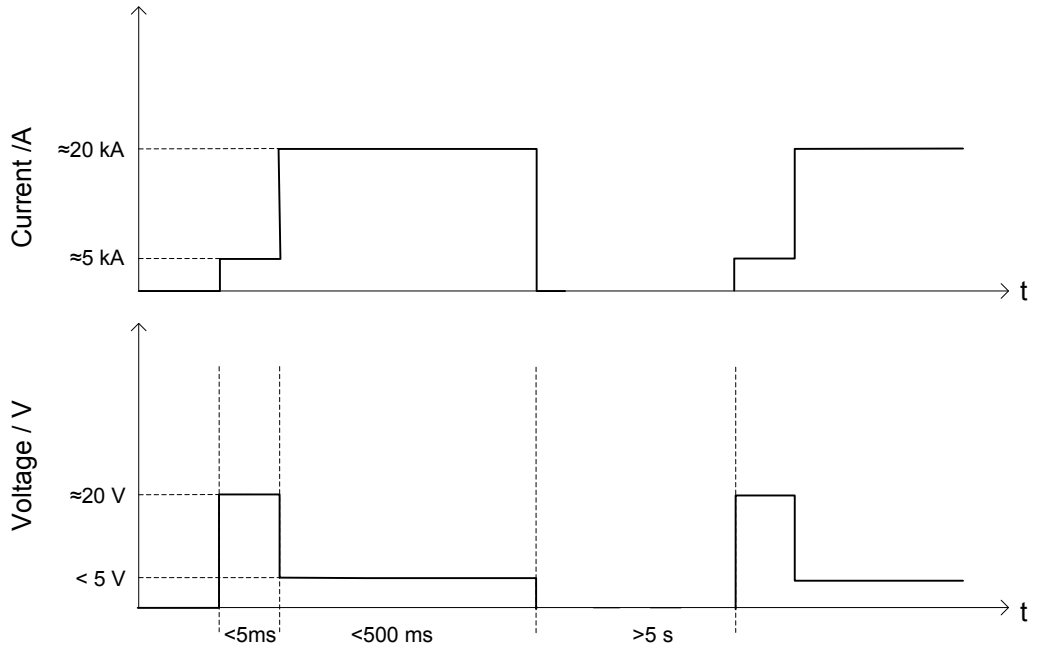


Fig. 2.1: The load voltage and the current requirement curves for the desired SBRSWPS (Source: NIMAK GmbH).

initial transient and is burnt in about 5-10 ms of the initial phase. This initial transient requirement of relatively higher voltage can be generated using an additional auxiliary power supply. However, if the concept of the WPS enables a single power supply to meet both the steady state and transient requirements (without added weight or volume), it has to be considered as more qualified.

To summarize, the output requirement of the desired WPS is basically low voltage and high current. The input voltage is, however, a design variable. As an example, an input voltage of 400-500 V might be suitable when using an ECS or an FSS while, an input of less than 40 V might be suitable when using a DLC based storage. Thus, the specifications for the WPS input voltage cannot be decided upon, at an initial stage of the analysis.

2.2.1 Nominal and peak output power

As described earlier, the welding load can demand a current of 20 000 A at a voltage of 5 V, for a specified duration of the welding. However, the 5 V and 20 000 A output is the worst case (maximum power case) that can exist. The most probable (nominal) output corresponding to about 90 % of load cases is different (Example: 15 000-20 000 A and 1.5-2.5 V). Determining the most probable (nominal) output conditions can be based on statistical information or on application specific engineering experience. This is an important aspect in sizing the storage, which will be described in Chapter 4. The

WPS under consideration, needs to support a peak welding power of 100 kW (5 V and 20 000 A) and a nominal welding power of 50 kW (2.5 V and 20 000 A).

2.3 Other desirable characteristics

2.3.1 Audible noise

Since RSW is an industrial process, no stringent noise requirements exist. But nonetheless, it is desirable to deliver a noise-free solution to the customer. Thus the switching frequency of the desired SBRSWPS needs to be greater than 20 kHz which lies out of the audible frequency range.

2.3.2 Galvanic isolation between storage element and output

As per norms, no galvanic isolation between the storage element and the welding element is necessary, if the voltage across the storage element is less than 100 V. But it is always necessary that the output of a SBRSWPS is galvanically isolated from the input mains.

When the storage system voltage is higher than 100 V, galvanic isolation between the storage element and the welding element is obligatory. This is independent of weather galvanic isolation exists between the input mains and the storage system or not.

2.3.3 Load duty ratio

Maximum welding duration is less than 500 ms and the minimum time gap between successive weldings is 5 s. Discussion on the reason behind these specifications lies out of the scope of this thesis, since they originate from the properties of materials used in automotive industry and the process timings involved in the automotive manufacturing process.

2.3.4 Weight and volume

The WPS part of the SBRSWPS is usually mounted on a welding robot which needs to move to various locations in space, depending on the parts to be welded. Minimum energy consumption and easy manoeuvrability are desired features of the robots. Hence, the volume and weight of the WPS needs to be as small as possible. One needs to be clear that the storage system can be mounted away from the moving part of the robot

and therefore can be heavier if necessary. But as far as its volume is considered, it is desirable that it occupies minimum space. This is because the floor place is always a critical issue in most manufacturing lines.

2.4 Specification sheet

Specifications which are desired by the new category of SBRSWPS are summarized in Table 2.1

Table 2.1: Specification sheet of the desired SBRSWPS

S.No.	Parameter	Data
1	Input	3AC 400 V, 50 Hz mains
2	Output current maximum (oxide layer burning phase / welding phase)	5000 A / 20 000 A
3	Output voltage maximum (oxide layer burning phase / welding phase)	20 V / 5 V
4	Welding duration	<500 ms
5	Current rise time	<10 ms
6	Storage type	Needs to be selected
7	Time gap between consecutive welding instances	>5 s
8	Current control range	5000-20 000 A
9	Output isolation	Required only if energy storage voltage >100 V
10	Switching frequency	>20 kHz to eliminate audible noise.
11	Nominal welding power (NL)	50 kW
12	Peak welding power (PL)	100 kW

Chapter 3

Power Supply Topology

3.1 Modularity

Extreme high current semiconductors, which are available on the market, are optimised for conduction losses and their switching performance is not fast enough to support switching frequencies higher than 20 kHz. Thus, the use of devices with smaller current ratings and higher switching speeds becomes mandatory. Therefore, it is apparent that the WPS under consideration should be based on a modular structure, where converters with smaller current ratings are operated in parallel, in order to keep the switching currents within manageable limits. Further, modularity brings with it obvious benefits in manufacturing and has an effect of reducing the down-time of any system.

Further, the number of parallel modules in the WPS should not be too high, in order that that the system remains simple to install and maintain. A basic survey was performed on the availability of high current, high switching frequency MOSFETs and diodes. From the analysis, it was concluded that it is possible to build high-frequency (greater than 20 kHz) power electronic blocks with 2000 A output capacity. Hence by choice, it would be desirable that the WPS is made up of 10 identical modules connected in parallel, each with an output current capability of 2000 A (Fig 3.1). Considering such a modular solution, the specifications for each module of the desired WPS are listed down in Table 3.1. The remaining part of this chapter will be in connection with the topology analysis with respect to these requirements.

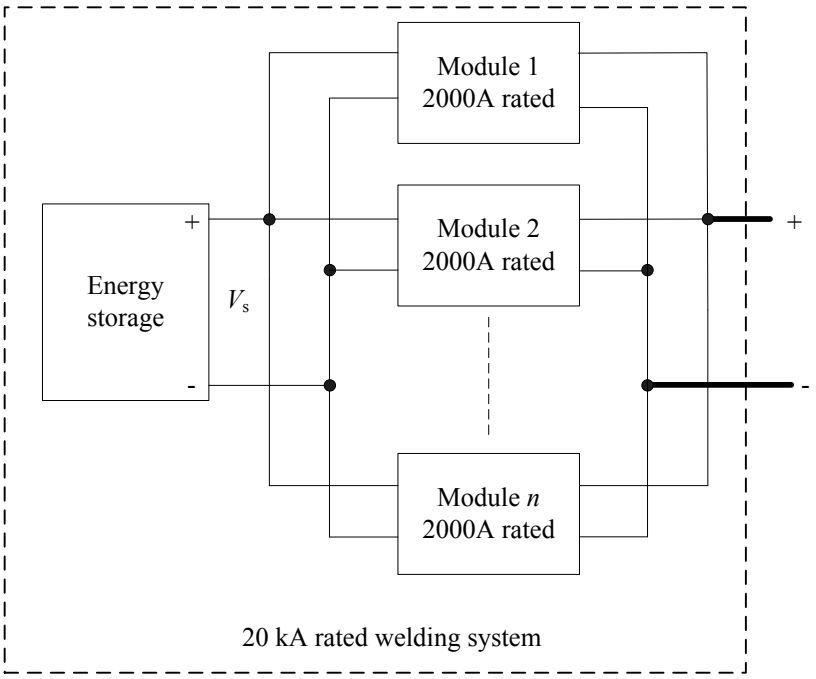


Fig. 3.1: Picture depicting a modular solution for the SBRSWPS.

Table 3.1: Specifications for each module of the desired SBRSWPS

S.No.	Parameter	Data
1	Output current maximum (oxide layer burning phase / welding phase)	500 A / 2000 A
2	Output voltage maximum (oxide layer burning phase / welding phase)	20 V / 5 V
3	Welding duration	<500 ms
4	Current rise time	<10 ms
5	Time gap between consecutive welding instances	>5 s
6	Current control range	500-2000 A
7	Output isolation	Required only if energy storage voltage >100 V
8	Switching frequency	>20 kHz to eliminate audible noise.
9	Nominal welding power	5 kW
10	Peak welding power	10 kW

3.2 Potentially suitable converter topologies

The desired module current of 2000 A is still high enough to bother a designer, especially when a high switching frequency (greater than 20 kHz) is desired. To achieve the required module current, it is expected that a specific number of converters need to be operated in parallel or in an interleaved fashion.

Thus one needs to select a topology that is suitable for parallel or interleaved operation. Cases may exist, where a certain topology can be paralleled when coupled with a certain control structure. As an example [1][2][3] and [4] describe some methods of paralleling buck converters. While,[5][6] describe the paralleling of fly-back converters. Higher output current requirement is of course not specific to some converter topologies and research on the topic of paralleling is also being extended to resonant converters [7] and inverters [8][9][10].

Based on initial studies on topologies used for high current and low voltage applications, the following topologies were found to have a potential to be used for the development of the power modules.

1. Interleaved Buck Converter (IBC)
2. Interleaved Buck Controlled Resonant Converter (IBCRC)
3. Interleaved Phase-Shifted Full-Bridge Converter (IPSFBC)
4. Inter-Cell Transformer based Buck Converter (ICTBC)
5. Interleaved Tapped-Inductor Buck Converter (ITIBC)

Sections 3.3 to 3.7 present a qualitative analysis of the above potentially suitable topologies. The analysis covers specific technical issues, state of the art and a summary of qualitative advantages and disadvantages. A quantitative comparison of the qualified topologies with respect to volume, efficiency and installed semiconductor power rating, is presented in Section 3.8.

3.3 Interleaved buck converter

Multiphase interleaved buck converter has been traditionally employed in Voltage Regulated Modules (VRMs) and telecom power supplies [11]. Where high output current and fast transient response are necessary and crucial. IBC topology is a well proven technology, simple in control and robust in nature. The circuit diagram of an interleaved buck topology with n number of phases is shown in Fig 3.2.

3.3.1 Advantages

Interleaved buck topology naturally reduces the output current ripple [12], as individual converters are operated with a certain phase shift. Interleaving not only reduces the

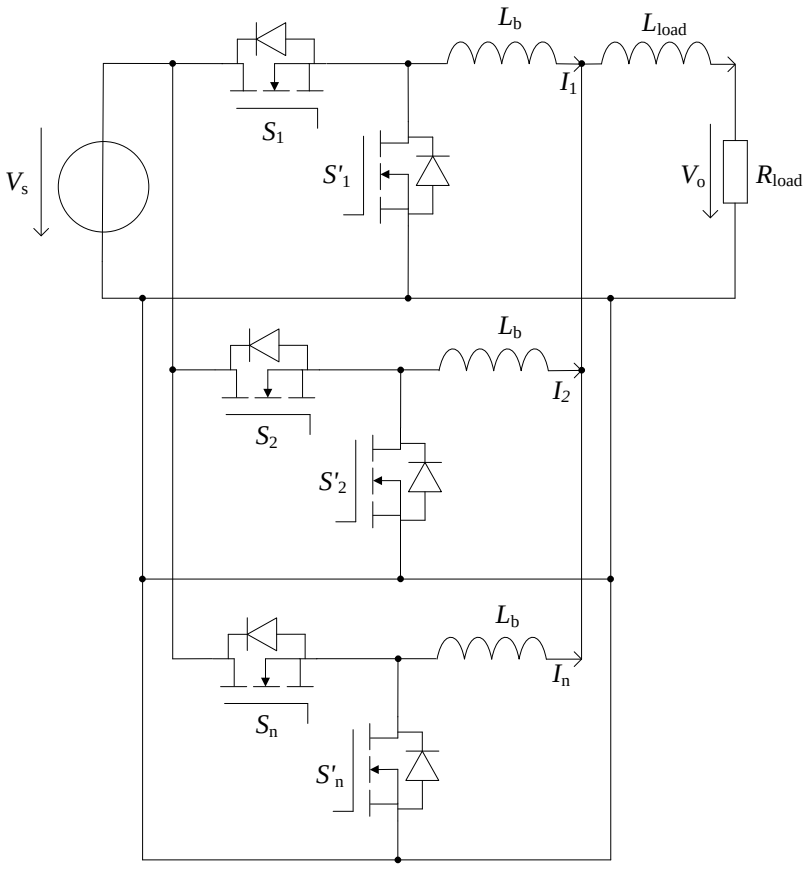


Fig. 3.2: Interleaved buck converter with n phases.

output ripple but also reduces the AC RMS component in the input current. Due to this effect, the needed capacitance (input) is reduced and a higher power density can be achieved [13] [14] [15]. On the other hand, individual buck converters handle only small power, which improves the design flexibility.

A quantitative analysis of the ripple reduction with respect to the number of interleaved phases with an output capacitor, is presented in [16]. The analysis presented in this publication can also be extended to the present case (without an output capacitor), by assuming that the average value of the load current is much higher as compared to its ripple component. If the inductance in each phase is given by L_b, L_load is the load inductance (welding tong inductance), V_o is the average output voltage, D is the duty-cycle and if f_s is the switching frequency, then the peak to peak-load current ripple is given by,

$$\Delta I_\mathrm{load} = \frac{V_\mathrm{o}}{\left(\frac{L_\mathrm{b}}{n} + L_\mathrm{load}\right) f_\mathrm{s}} \left(1 - \frac{m}{nD}\right) \frac{(1 + m - nD)}{n} \tag{3.1}$$

where m is given by the function $floor(nD)$. The function "$floor$" returns the greatest

integer value less than the argument nD. As an example, if D less than $1/n$, then m becomes equal to zero. For which case, the Equation 3.1 turns out to be

$$\Delta I_{\text{load}} = \frac{V_{\text{o}}}{\left(\frac{L_{\text{b}}}{n} + L_{\text{load}}\right) f_{\text{s}}} \frac{(1 - nD)}{n} \tag{3.2}$$

3.3.2 Drawbacks

The IBC topology however, suffers from the following drawbacks.

- Due to practical limitations on the minimum pulse width that can be generated, there exists a limitation on the highest switching frequency that can be used in case of higher input to output voltage ratios
- Switches need to be rated for the input voltage (switching voltage spikes should also be considered) and the output current per phase. Thus, making it an expensive solution, especially in case of higher input to output voltage ratios
- In order to achieve perfect current sharing between the interleaved converters, individual current sensors are mandatory. This makes the system bulky and expensive[12][17]
- The main disadvantage of the interleaved buck is increased ripple in individual phases, especially when operating close to 50 % duty-cycle. This limits the degree to which the inductor size can be reduced

3.3.3 Suitability for resistive spot welding applications

It has been reported that this topology has been used in Voltage Regulator Modules (VRMs) for output voltages of 3.3 and 5 V and for input voltages of up to 24 V [12][14][18]. The efficiency of the converter for such applications is reported to be in the range of 70-75 %, when using synchronous gating, which uses the reverse conduction charecteristic of MOSFETs. Till date, use of such topology has been mostly limited to about 200-300 A of load current [11] and to an input voltage upto 24 V. Higher current designs are feasible today, especially because of the availability of higher current, fast switching MOSFETs. Further, over-current protection can be incorporated into the gate circuit, which may obviate the need of individual current sensing for balancing.

3.4 Interleaved buck controlled resonant converter

One of the topologies which is of interest for high-frequency welding supplies is the buck controlled series LC resonant topology[19][20]. The basic circuit diagram of this topology is shown in Fig 3.3.

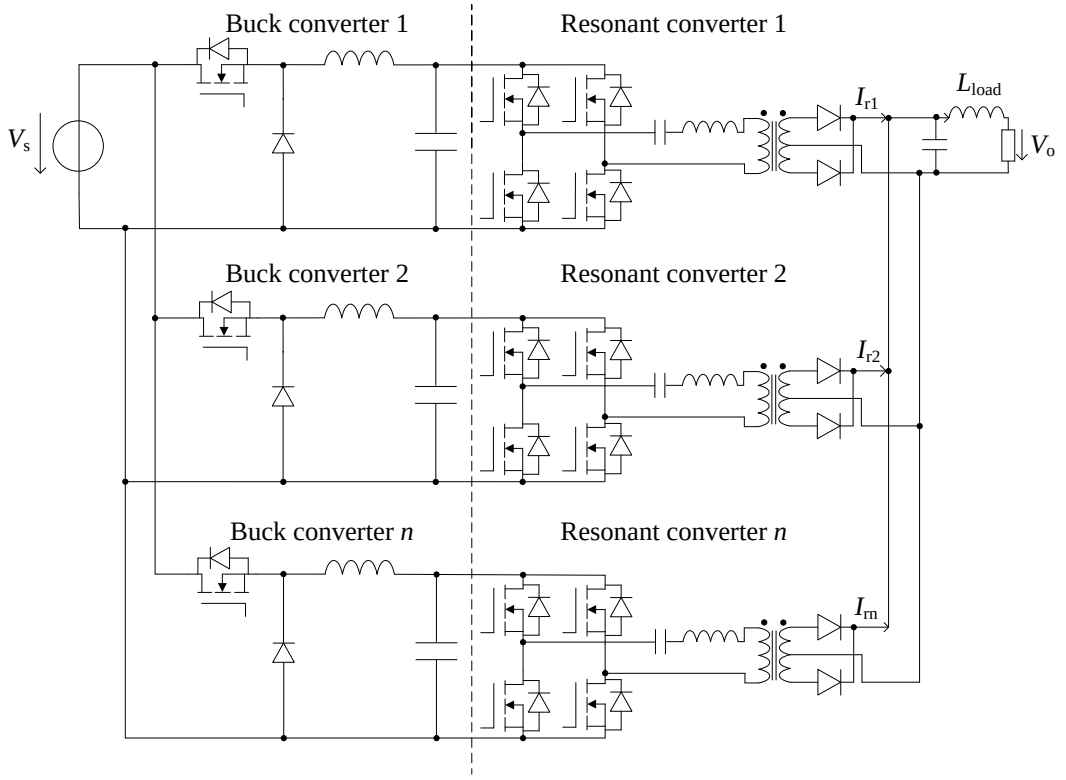


Fig. 3.3: Interleaved buck controlled series resonant converter.

Such a topology has been widely discussed in literature for applications in bi-directional converters [21] in electric vehicles. In addition, research on similar topologies has been reported for applications in the field of server power supplies [22]. Where an LLC converter follows a power factor correction stage. Even though the topology shown in Fig 3.3 looks to be similar to that used in the above mentioned applications, the mode of operation and control has to be totally different in case of RSW application.

In case of RSW applications, the buck converters in Fig 3.3 have to be operated in current control mode and are responsible for controlling the load current. The resonant converters operate at constant frequency (just above resonance) [23]. Their role is to amplify the current by stepping down the voltage. Multiple such converters can be interleaved to supply the same output capacitor for ripple reduction [22][24].

First question which arises in case of BCR topology is that, why does one require an additional buck converter, when a resonant converter can be designed to control the output current directly? The reasons are as follows.

- Interleaving of the output becomes possible, only when resonant converter operates at constant frequency
- Constant frequency operation and sinusoidal currents enables a good optimization of transformer size

3.4.1 Advantages

The IBCRC topology presents some very good advantages. the most important of these are listed down below.

- Extremely small transformer size
- Operation at high switching frequency can easily be realised because of soft switching and 50 % duty-cycle operation.
- Small current sensors can be utilised for the buck converters. In fact, resistive current sensors can be used without compromising on efficiency or cost
- Over-voltage spikes across the output rectifier diodes are practically inexistent. Thus, smaller voltage diodes can be utilised for the output rectifiers. This reduces the installed semiconductor power rating and increases efficiency

3.4.2 Drawbacks

The IBCRC topology suffers with an important drawback. The practical size of the resonant components increase with decrease in input voltage, mainly because of increase in primary current. Hence, such resonant converters are reported to be widely utilised only for input voltages above 300 V.

3.4.3 Possibility of application to resistive welding

Due to the availability of high speed and high current Schottky diodes and MOSFETs, major problems are not foreseen in the application of IBCRC for resistance spot welding. Further, the buck converters can be placed on a stationary base while the welding robot carries only the resonant converters. Thus, the weight on the welding robot can be drastically reduced.

3.5 Interleaved phase-shifted full-bridge converter

Phase-Shifted Full-Bridge (PSFB) with Zero Voltage Transition (ZVT) is been extensively used for a wide variety of applications. The applications range from automotive battery chargers to VRMs. Conventional control can be coupled with the advantages of zero voltage transition in case of such a topology. This is exactly what makes the topology widely accepted. It is reported [25] that such a topology is also utilised for arc welding applications where high dynamics are required. Fig 3.4 shows a circuit diagram of an IPSFBC.

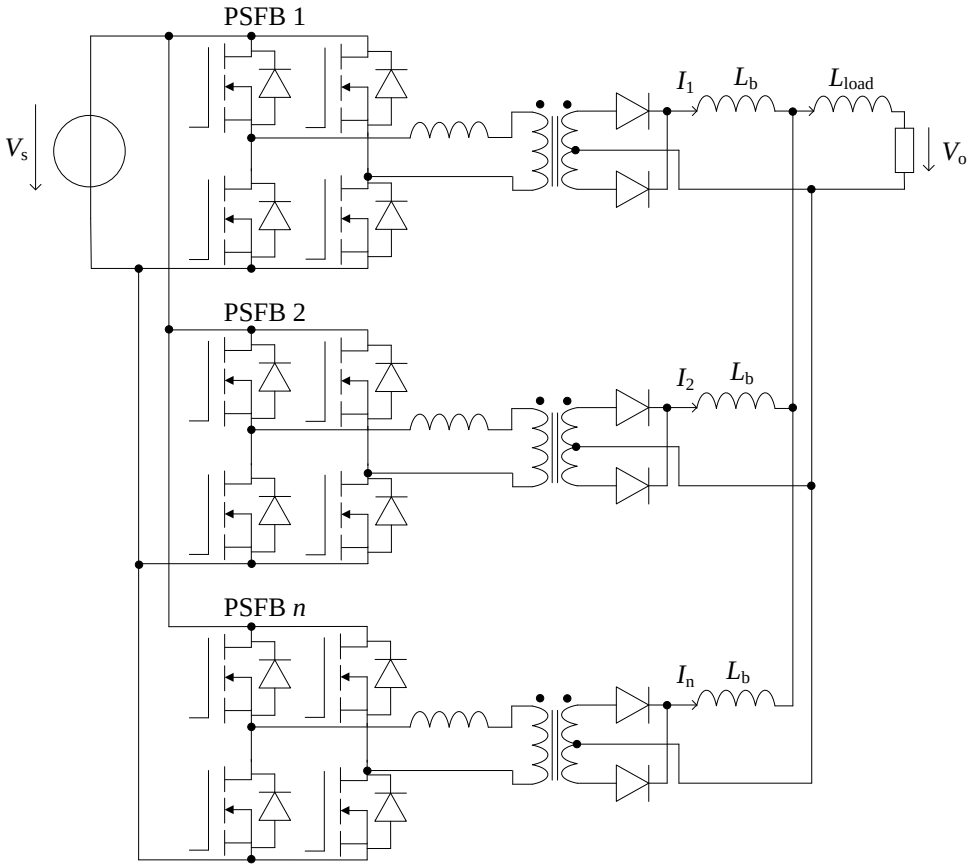


Fig. 3.4: Interleaved phase-shifted full-bridge converter.

The operating principle of the interleaved PSFB shown in Fig 3.4 is described in detail in [25][26][27] . The ripple reduction due to interleaved operation is very similar to that of an IBC topology.

3.5.1 Advantages

The main advantages presented by the IPSFB topology are as follows.

- High-frequency operation is possible because of the ZVT characteristic. Thus, the transformer can be small (but larger than that for series resonant converters)
- Low switching losses and EMI, because of soft switching behaviour
- Current sensors are small. In fact, resistive current sensors can be used without compromising on efficiency or cost
- Conventional method of control, similar to PWM control
- Low output current ripple as compared to resonant topology

3.5.2 Drawbacks

In-spite of having many advantages, the IPSFB topology also has got some drawbacks and limitations. Most important of these are listed down as,

- the converter becomes hard switched at low loads currents [28][29]. Nonetheless, this drawback, in general, is not applicable to welding power supplies, as the question of small load currents does not arise
- reliability of MOSFETs is a concern, in case of extremely small pulse duration [25]
- non-sinusoidal transformer currents

3.5.3 Suitability for resistive spot welding applications

PSFB has been reported to be applied in the field of VRMs with current rating in the range of a few hundred amperes [19]. A modular scheme using such converters has been reported, which was applied to generate extremely large currents in the range of 20 kA [30]. Therefore, it can be said that this topology can be used to develop the modular SBRSWPS under consideration.

3.6 Inter-cell transformer based buck converter

As mentioned earlier, the main disadvantage of the IBC is an increased ripple in individual phases. This drawback can be overcome by magnetically coupling the interleaved converters. Such a multiphase buck converter with a magnetically coupled inductor is termed as an Inter-Cell Transformer based Buck Converter (ICTBC), whose circuit diagram is shown in Fig 3.5. The PWM signal applied to each phase of an ICT is exactly

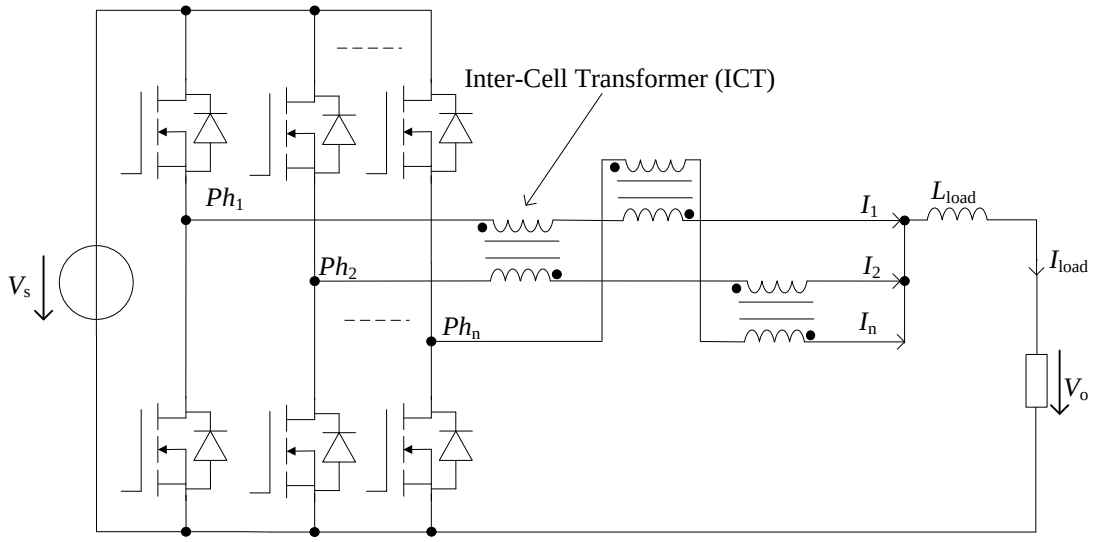


Fig. 3.5: Inter-cell transformer based buck converter.

similar to that of an IBC topology. However, since each phase is magnetically coupled, the current in each phase has to be equal (under the assumption of ideal coupling and negligible magnetizing current as compared to the total phase current). The theory behind the operation of ICTBC is explained in detail in [31].

If the sum of the leakage inductance of all the transformers is given by L_{lk}, if L_{load} is load inductance (welding tong inductance), if V_{o} is the output voltage, D is the duty-cycle and if f_{s} is the switching frequency, assuming the average load current to be much higher than its peak to peak ripple, the load current ripple turns out to be

$$\Delta I_{\mathrm{load}} = \frac{V_{\mathrm{o}}}{(L_{\mathrm{lk}} + L_{\mathrm{load}})\, f_{\mathrm{s}}} \left(1 - \frac{m}{nD}\right) \frac{(1 + m - nD)}{n} \tag{3.3}$$

Though this equation looks pretty similar to that of 3.1, the only difference is that the ripple current in individual phases is equal to n^{th} part of the load current ripple ΔI_{load}.

As described in [31], the ICTBC can be based on an individual magnetic element structure using standard cores or based on a monolithic coupled inductor structure (also termed as ICT). Each of these two configurations can be in turn implemented using different mechanical designs. An exhaustive list of monolithic ICT structures is presented in [31]. The report also presents a detailed methodology for the design of ICTs, along with core material selection and loss optimization. Even though the magnetic design is different, the principle of operation still remains the same across different ICTBC configurations.

3.6.1 State of the art

ICT based converters are reported to be used in voltage regulator modules (VRMs) for load currents up to 100 A and for output voltages smaller than 5 V [32]. Surface mount monolithic coupled inductors, suitable for up to five phase converters are available in market [33]. Main applications of such surface mount ICTs are limited to small power supplies for computers and microcontroller boards. ICTs are also been researched, to be applied in the field of motor drives and UPS systems. In [34] it is reported that circulating currents between parallel inverters can be limited by using ICTs between the parallel inverters and the load. It is also reported that the use of ICTs can reduce the output current harmonics in a three phase inverter systems [35]. A comparison between inductors and ICTs for filtering in PWM inverters is presented in [36]. ICTs have also been reported to be used in high voltage and high current applications. A 10 kV, 6 kA DC/DC converter is reported to be developed for supplying the magnetic coils of the particle accelerator at the European Organization for Nuclear Research [37].

3.6.2 Drawbacks

It is clear that the use of ICTs helps in reducing the current ripple in individual phases of an interleaved converter. Further, the use of ICTs particularly yields better results, with a large number of phases, due to the additive effect of the leakage inductances. However, one of its drawbacks is the complicated design of magnetic components, which usually needs a lot of research efforts to be put in, especially for converters with more than two phases [31]. Another technical challenge is to deal with the core saturation problem of the ICT. In practice, a magnetic flux imbalance exists across the windings of an ICT, which can result in core saturation [38]. This flux imbalance can be completely unintentional and can happen as a result of tolerances in gate drive propagation delays or differences in switching characteristics of various devices. However, such imbalances can be avoided by utilising individual phase current control.

3.6.3 Suitability for resistive spot welding applications

The main advantage presented by ICTBC over IBC is ripple reduction in individual phases. Further in [31] it has also been proved that, the core losses as well as the magnetic volume are reduced, as compared to the IBC topology. Considering these aspects, the ICTBC seems to be a perfect candidate for WPS under consideration. But on the other hand, it has to be kept in mind that the required research efforts for the ICT development are quite high. Also, once an ICT is designed to suit a particular mechanical

layout, it will be difficult to make changes to the design later on, thus reducing design flexibility.

3.7 Interleaved tapped-inductor buck converter

An important issue regarding the small duty-cycle operation of a synchronously gated buck converter is low efficiency [39]. For buck converter designs with small output to input voltage ratio, the semiconductor switches need to be rated to block the input voltage, which is far higher than the output voltage. Higher voltage rating implies larger conduction as well as switching losses, coupled with a bad body-diode performance. Thus, both the switching and conduction losses are together increased. The TIBC is an attractive solution, exactly suitable under the condition of low output to input voltage ratios [40–49].

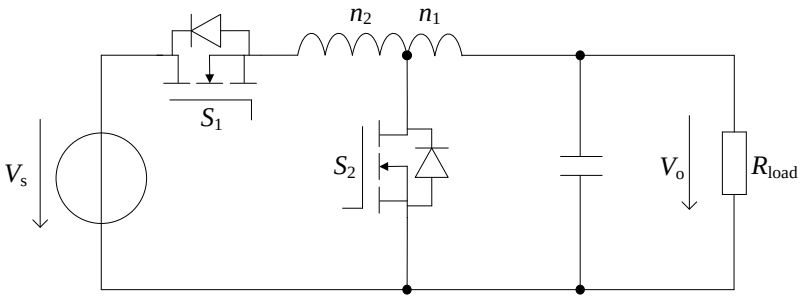


Fig. 3.6: Tapped-inductor buck converter.

A Tapped-Inductor Buck Converter (TIBC) can be termed as a modified buck converter where the two terminal inductor is replaced with a three terminal inductor. The three terminals of the tapped-inductor are connected as shown in Fig 3.6. Operating principle of such a converter is explained in detail in the literature [39–50]. The most noticeable point is the output current wave shape (to the left of the capacitor), which is discontinuous in shape.

3.7.1 Advantages

Most important advantage of the TIBC is its higher duty-cycle operation against that of a conventional buck converter, for a given output to input voltage ratio of M. This advantage makes the control design much easier when using high switching frequencies (larger than 100 kHz). Its duty-cycle D_{TI} of the TIBC is given by

$$D_{\mathrm{TI}} = \frac{n_{\mathrm{TI}} M}{1 + (n_{\mathrm{TI}} - 1)M} \tag{3.4}$$

where $n_{\mathrm{TI}} = (n_1 + n_2)/(n_1)$, n_1 denotes the number of turns between switch S_2 and the output capacitor and n_2 denotes the number of turns between switch S_1 and S_2.

Apart from the benefit in terms of increased pulse width, the voltage rating of switch S_2 and current rating of switch S_1 can be considerably reduced (depending on the turns ratio of the tapped-inductor) as compared to that of the conventional buck solution.

3.7.2 Drawbacks

It is important to note that the TIBC also presents certain drawbacks. One of its drawbacks is the higher current rating requirement of the switch S_2. Further, the use of output capacitor becomes mandatory due of the discontinuous nature of the current through the turns n_1. This output capacitor can indeed turn out to be very bulky in case of welding applications due to the extremely high current requirement. The most important drawback is however the need of a snubber circuit in order to limit the turn off voltage spike across the switch S_2. This is because of the presence of a large leakage inductance in the commutation mesh due to non-ideal coupling between the two windings of the tapped-inductor. Many solutions have been presented by researchers, to efficiently utilise the energy stored in the leakage inductance by means of regenerative (loss-less) snubbers. The most simple and cost effective solution till date, was presented by Kaiwei Yao in 2005 [41]. The circuit diagram of the topology proposed in the publication is shown in Fig 3.7. Detailed description of its operation and design can be found in [42], where the solution is compared with a conventional buck and a classical TIBC.

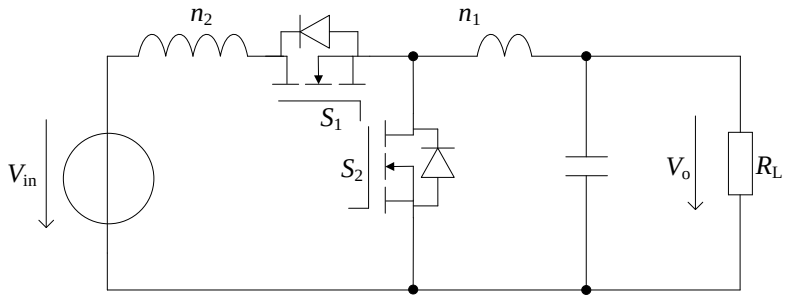


Fig. 3.7: A tapped-inductor buck topology proposed by Kaiwei Yao.

3.7.3 Suitability for resistive spot welding applications

As previously said, an output capacitor and a snubber circuit is mandatory when using a TIBC. The size of both these components could become comparable to the size of the rest of the power circuit, when dealing with high welding currents. Hence, it can be said

that the TIBC may not be the right choice for realising a welding power supply, even when interleaved.

3.8 Quantitative comparison of the qualified topologies

Theoretically, all the five topologies, namely, the IBC, the IBCRC, the IPSFBC, ICTBC and the ITIBC topologies, can be potentially used for developing the modular SBRSWPS under consideration. However, practical considerations make ITIBC solution not suitable for the SBRSWPS under consideration. From the remaining four topologies, selection can be made, based on the voltage at which the energy is stored (converter input voltage).

As shown in Fig 3.8, the IBC and the ICTBC can be beneficially used for input voltages below 100 V. IPSFB can be used for a wider range of input voltages (40-300 V) while, the IBCRC can be beneficially used between input voltages of 300 V and 600 V. The ranges of the input voltages given here are only approximate and there exists a band of voltages (near boundaries), in which, either of the corresponding topologies can be a suitable choice.

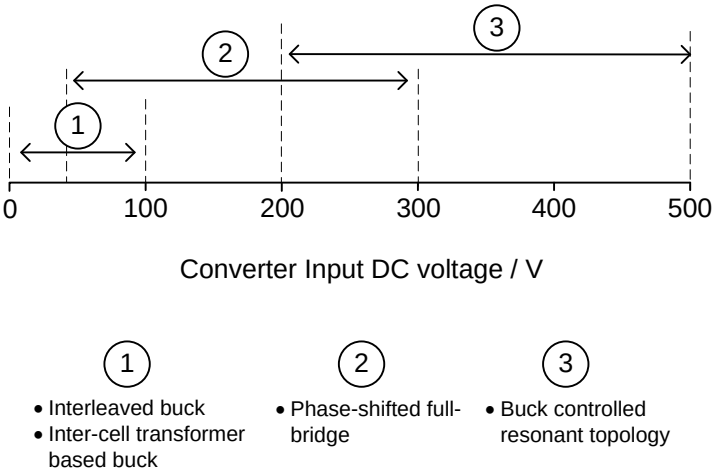


Fig. 3.8: Conclusions drawn from converter topology study.

In the next subsections, a comparative analysis of the IBC, IBCRC, IPSFBC and the ICTBC is presented. An evaluation is made, with respect to magnetic component volume, installed semiconductor power and efficiency. For the purpose of uniformity, six interleaved phases per module are considered (for all the four topologies).

3.8.1 Comparison with respect to magnetic volume

Fig 3.9 shows a normalised comparison of the required magnetic volume for the four topologies. From the figure, it is very clear that the best option with respect to magnetic volume is the ICT based buck topology. However, one needs to take a decision between the complexity of magnetic design and the gain with respect to the magnetic volume.

A fairly detailed analysis was performed, in order to obtain the results shown in Fig 3.9. The assumptions made for the analysis and the process are discussed in Appendix A. Fundamentals on magnetics design presented in [51] was extensively utilised for this purpose.

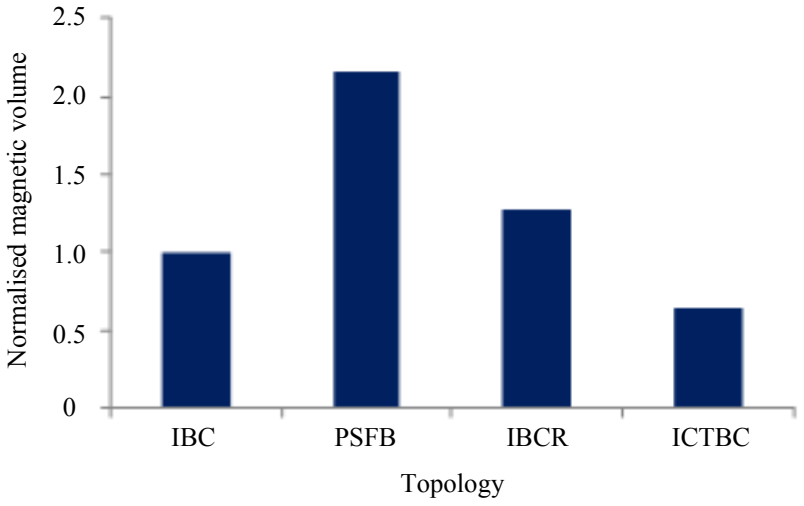


Fig. 3.9: A normalised comparison of the required magnetic volume for the four topologies.

3.8.2 Comparison with respect to power losses

Even-though, converter efficiency is not the most important objective in a resistive spot welding application, a rough estimate of the converter losses is however practically necessary. It will be seen later that such estimations are indeed useful when determining the size of the storage system.

A basic efficiency calculation was performed for each of the four topologies under consideration. Semiconductor switching losses, semiconductor conduction losses and losses in the magnetic components are included in the efficiency calculations, while, other loss components are neglected. Switching losses and conduction losses are calculated according to [52]. The magnetic losses corresponding to a surface loss density of $0.16\,\mathrm{W/cm^2}$ were utilised (refer Table A.3 in Appendix A). For calculation purpose, a semiconductor junction temperature of $25\,^{\circ}\mathrm{C}$ was considered.

For the purpose of semiconductor device selection, an output voltage of 3 V and an output current of 20 kA was assumed (distributed among 10 modules, each containing six interleaved phases). Input voltage was taken as 30 V for non-isolated topologies while, it was 400 V for topologies with galvanic isolation. Table 3.2 gives a list of devices selected (for purpose of loss calculation) in each phase of the module, along with the calculated RMS and average current through the devices. It can be seen that the device current rating is approximately twice the calculated RMS current for MOSFETs and twice of the calculated average current for diodes.

Table 3.2: List of RMS or average currents flowing through devices under nominal-load condition and selected devices for the purpose of loss calculation

Module Topology (six phases per module of 2000 A)	Semiconductor component corresponding to each phase of the module	Number of devices per phase	RMS current at nominal output (A)	Average current (A)	Device voltage rating (V)/current rating (A)	Device × No. in parallel
Interleaved buck with input voltage = 30 V	Buck switch	1	104		100/180	IPB025N10N3 G × 1
Interleaved buck with input voltage = 30 V	Freewheeling diode (Synchronously gated MOSFET)	1	313	297	100/600 (100/540)	DSA300I100NA × 2 (IPB025N10N3 G × 3)
Interleaved phase-shifted full-bridge with input voltage = 400 V	MOSFET of the full bridge on the transformer primary	4	11.66		600/26	IXTT26N60P × 1
Interleaved phase-shifted full-bridge with input voltage = 400 V	Secondary side diode (Secondary side synchronously gated MOSFET)	2	233	165	100/330 (100/540)	DSA300I100NA × 1 (IPB025N10N3 G × 3)
Interleaved Buck controlled resonant with input voltage = 400 V	Buck switch	1	6.39		600/14	IXTA14N60P × 1
Interleaved Buck controlled resonant with input voltage = 400 V	Freewheeling diode of the buck converter	1		14	600/30	DSEP 30-06A × 1

Table 3.2: List of RMS or average currents flowing through devices under nominal-load condition and selected devices for the purpose of loss calculation

Module Topology (six phases per module of 2000 A)	Semiconductor component corresponding to each phase of the module	Number of devices per phase	RMS current at nominal output (A)	Average current (A)	Device voltage rating (V)/current rating (A)	Device × No. in parallel
Interleaved Buck controlled resonant with input voltage = 400 V	MOSFET of the full bridge on the transformer primary	4	12.95		600/26	IXTT26N60P × 1
Interleaved Buck controlled resonant with input voltage = 400 V	Secondary side diode (Secondary side synchronously gated MOSFET)	2	259	165	100/330 (100/540)	DSA300I100NA × 1 (IPB025N10N3 G × 3)
ICT based buck converter with input voltage = 30 V	Buck switch	1	104		100/180	IPB025N10N3 G × 1
ICT based buck converter with input voltage = 30 V	Freewheeling diode (Synchronously gated MOSFET)	1	313	297	100/600 (100/540)	DSA300I100NA × 2 (IPB025N10N3 G × 3)

Fig 3.10a shows the expected welding power supply losses for each topology at Nominal-Load (NL) with Schottky diodes on the low voltage output side. Fig 3.10b shows the expected welding power supply losses for each topology at Peak-Load (PL), with Schottky diodes on the low voltage output side. Fig 3.11a shows the expected welding power supply losses for each topology at NL, with synchronously gated MOSFETs for freewheeling on the low voltage output side while, Fig 3.11b shows the expected welding power supply losses for each topology at PL, with synchronously gated MOSFETs for freewheeling on the low voltage output side.

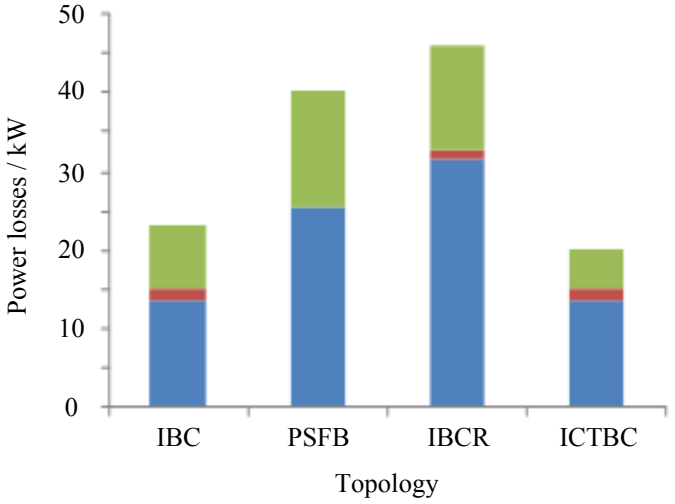
From the Figures 3.10b to 3.11b it is clear that the ICTBC is the most efficient, mainly because of its smaller magnetic losses. The next most efficient is the IBC topology. The PSFB and the IBCR topologies perform the worst in terms of efficiency, mainly because of the transformer and additional semiconductor switches in the current path. It can also be noted that there is a significant improvement in the efficiency performance by opting for synchronous gating. Further, irrespective of the topology, semiconductor conduction losses contribute to a the major part of the total losses. It can also be clearly noticed that there exists no significant change in loss performance, between nominal-load and peak-load operations.

3.8.3 Comparison with respect to installed semiconductor power rating

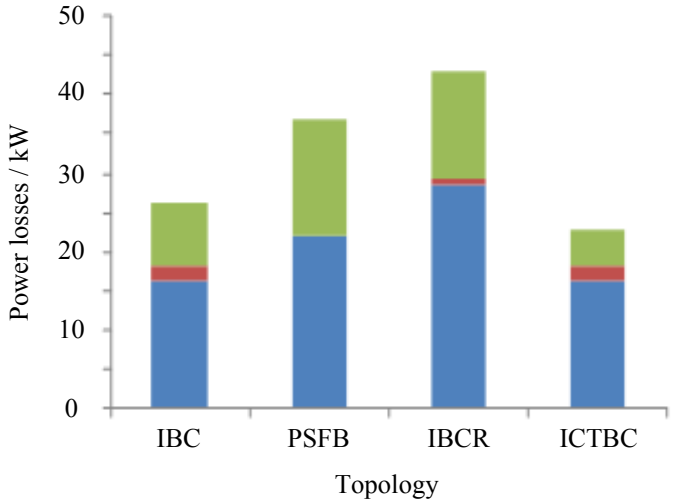
Based on the semiconductors listed in Table 3.2, a normalised comparison of installed semiconductor power for each of the four topologies is presented in Fig 3.12. It can be seen that the semiconductor power rating is minimal in case of non-isolated topologies. It is approximately half as compared to that of isolated topologies. It must be noted that an absolute comparison of semiconductor power rating is impractical because there always exists an option of reducing the conduction losses by installing more devices in parallel (especially when using synchronous gating)

3.8.4 Conclusion

From the qualitative analysis presented in the previous section and the quantitative comparison presented in this section, it can be concluded that an ICTBC or an IBC are the obvious choices when the DC link voltage is below 100 V while, the IPSFB is suitable when the DC link voltage is higher.

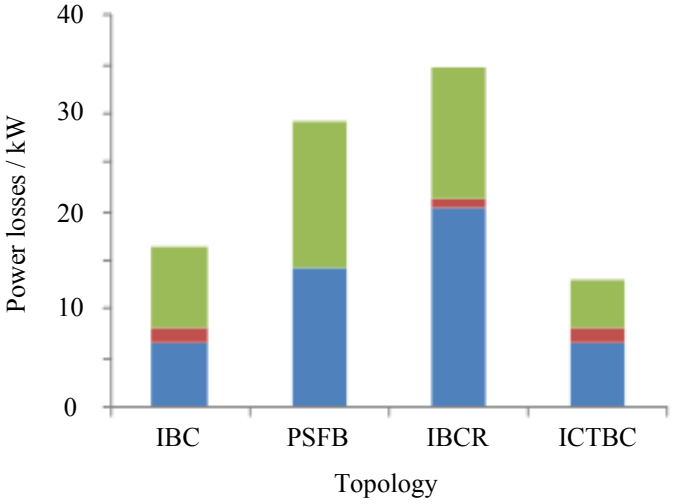


(a)

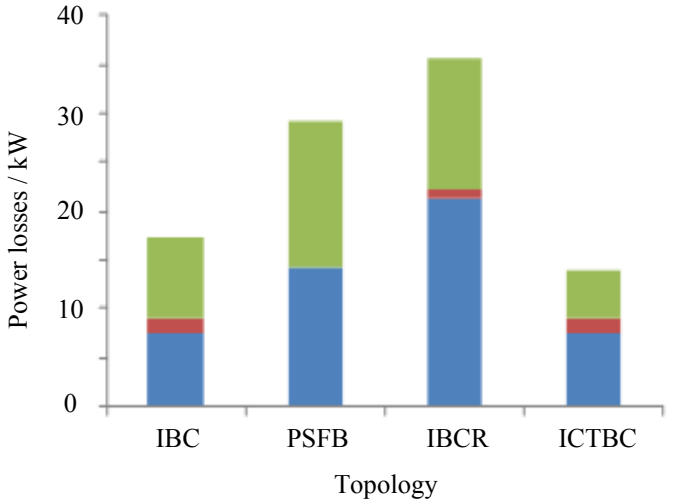


(b)

Fig. 3.10: Expected welding power supply losses for each topology with schottky diodes on the low voltage output side (a) at Nominal-Load (NL) and (b) at Peak-Load (PL). Legend; Blue: Conduction losses, Brown: Switching losses, Green: Losses in magnetic components



(a)



(b)

Fig. 3.11: Expected welding power supply losses for each topology with synchronously gated MOSFETs on the low voltage output side (a) at Nominal-Load (NL) and (b) at Peak-Load (PL). Legend; Blue: Conduction losses, Brown: Switching losses, Green: Losses in magnetic components

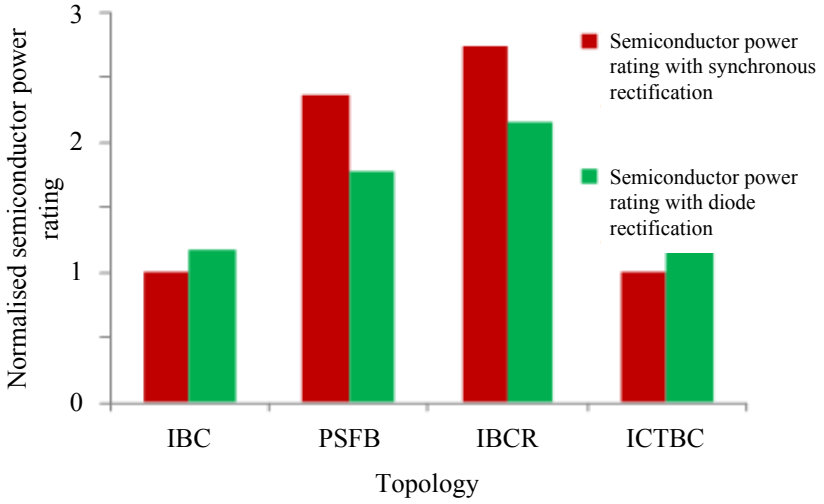


Fig. 3.12: A normalised comparison of installed semiconductor power for the topologies considered, based on semiconductors selected in Table 3.2.

Chapter 4

Energy Storage

4.1 Introduction

A great deal of research in the recent past has been dedicated towards the characterization of various energy storage technologies. A major portion of the research in this direction has been centred on the design of hybrid energy storage systems for electric vehicles [53–55] or smart grids [56–58]. Some publications also deal with energy storage systems for portable electric equipments, which mostly use batteries. Further, the advantages and disadvantages of various types of energy storage technologies have been presented by many researchers. Unfortunately, nothing significant has been reported in the field of storage systems for pulsed power supplies (power supplies with intermittent loading).

Energy storage is the most important component of modern pulsed power applications like resistive spot welding. The biggest advantage presented by a SBRSWPS as compared to a non-storage-based system, is the reduction of peak power demand on the mains. Further, the presence of the storage element improves the repeatability of weld quality, by isolating the load from the disturbances in the mains. This chapter presents a comparative evaluation of Electrolytic Capacitor Storage (ECS), Double Layer Capacitor Storage (DLCS) and Flywheel Storage System (FSS) for the SBRSWPS under consideration. A detailed analysis considering energy storage, efficiency, lifetime considerations, volume and cooling requirements is presented. The analysis throughout the chapter is performed based on the specifications of SBRSWPS presented in Chapter 2. However, the conclusions drawn and the procedure used can be applicable to other pulsed power systems with similar requirements.

4.1.1 Criteria for selection of a storage technology

According to [56], for any given application, the major factors influencing the selection of energy storage technology are,

- energy and power density (both weight and volumetric density)
- efficiency
- reliability
- response time
- charge rate
- energy retention or "self discharge" time

An additional factor which has not been considered by most of the researchers is the limit on the operating temperature of the storage system. Further, the volume, weight and efficiency of the charging and discharging power converter can also play an important role in the selection of a storage system for a given application.

4.1.2 Storage technology pre-selection

In applications like automotive and space, small weight is the primary objective to be achieved while, smaller volume is given a second preference. But in case of RSW applications, the storage system is usually stationary and hence achieving smaller volume becomes more important than achieving smaller weight. Thus, primary objective will be to select a storage system which presents the highest compactness and at the same time gives a good performance with respect to all above listed criteria. A detailed analysis of various energy storage technologies along with some interesting research findings can be found in [56–58]. Where various battery technologies, DLCS, pressurised gas storage, super conducting coils, ECS, FSS, etc have been studied in detail. But as mentioned earlier, almost all of the existing research takes into consideration either the requirements of smart grid or that of electric and hybrid propulsion systems. However, from a basic study of the publications [55–58], it can be concluded that ECS, DLCS and FSS can be competitive options for delivering short duration (shorter than 500 ms) power pulses. Hence, these technologies are considered as suitable energy storage options for the SBRSWPS under consideration and thus were taken up for further analysis. Though super conducting coil based storage also seems to be an option, it has not been considered for this work. This is because this technology is still confined to research [59] and more technological maturity is needed in order to consider its use in industrial products.

4.1.3 Main factors influencing the storage system sizing

Two factors, which have the greatest influence on storage system dimensioning for SBRSWPS are the stored energy and peak output power requirements. The inequalities that needs to be met are,

$$E_{\mathrm{Smax}} > \int_0^{t_{\mathrm{w}}} (P_{\mathrm{weld}} + P_{\mathrm{WPSL}} + P_{\mathrm{sL}})\, dt \tag{4.1}$$

and

$$P_{\mathrm{Smax}} > \max(P_{\mathrm{weld}} + P_{\mathrm{WPSL}}) \tag{4.2}$$

where E_{Smax} is the stored energy, t_{w} is the weld duration, P_{weld} denotes the value of welding power, P_{WPSL} denotes the welding power supply losses corresponding to P_{weld}. P_{sL} denotes the losses in the storage system corresponding to the welding power P_{weld} and P_{Smax} denotes the maximum output power capacity of the storage system.

4.2 Evaluation of electrolytic capacitor based storage

Aluminium electrolytic capacitors are widely used in power electronic systems for industrial, telecommunications, automotive, military, medical and consumer electronics applications. Owing to the high energy and power density supported by the ECS, it is considered to be one of the strong competitor for application in SBRSWPS [55]. The construction of aluminium electrolytic capacitors is explained in detailed in [60]. Discussion on the physics of electrolytic capacitor construction lies out of the scope of this work and hence it is omitted in this report. Further analysis presented in this thesis focuses on the application specific criteria of electrolytic capacitors in SBRSWPS.

4.2.1 Energy density

It is interesting to see that the volumetric energy density of electrolytic capacitors is a function of their voltage rating. The energy density increases as the voltage rating increases. Such a characteristic can be attributed to practical technological limitations and production standardisations. The ideal voltage rating of electrolytic capacitors corresponding to maximum energy density is about 300 to 400 V. Rated voltage versus energy density curves generated for the particular manufacturer (Vishay) can be seen in Fig 4.1. It can be seen that the practically storable energy densities are about 20 % less as compared to the rated storable energy densities. This comes from fact that 10 % voltage de-rating is prescribed by almost all manufacturers. Further, the energy

densities which are really usable in case of pulse power applications are much lower, since only about 30 % voltage cycling is allowed for electrolytic capacitors [61].

In general, energy density of an electrolytic capacitor Ed_{ec} can be written as

$$Ed_{\mathrm{ec}} = \frac{\frac{1}{2}C(K_{\mathrm{c1}}V_{\mathrm{r}})^2 - \frac{1}{2}C(K_{\mathrm{c2}}V_{\mathrm{r}})^2}{\upsilon_{\mathrm{ec}}} \tag{4.3}$$

where C is the rated capacitance, V_{r} is the rated capacitor voltage , and υ_{ec} denotes the volume of the capacitor. The rated storable energy density is obtained using K_{c1} and K_{c2} equal to one and zero respectively. The practically storable energy density is obtained using K_{c1} and K_{c2} equal to 0.9 and zero respectively while, the usable energy storage density is obtained by substituting K_{c1} and K_{c2} with 0.9 and 0.63 respectively.

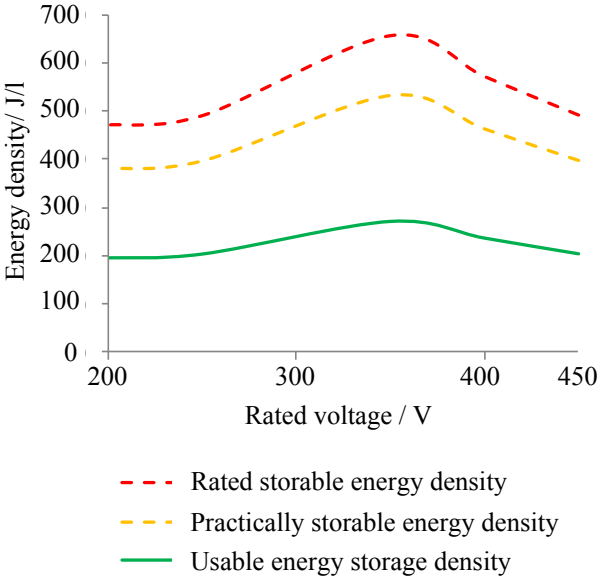


Fig. 4.1: Rated voltage versus volumetric energy density for aluminium electrolytic capacitors (based on long life aluminium capacitors from Vishay).

4.2.2 Equivalent circuit representation

Quite a few electrical-circuit models of electrolytic capacitors have been proposed by researchers, in order to emulate their electrical behaviour [62–65]. A suitable model has to be selected based on the requirements of the application and accuracy targets. The model presented in Fig 4.2 has been selected for this particular analysis [62, 63] as the main target is to analyse the low-frequency (less than 10 Hz) performance, which will be described in the following subsections.

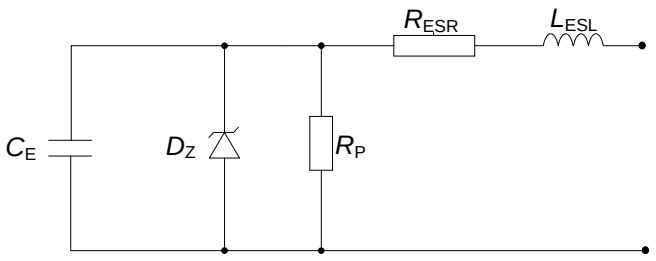


Fig. 4.2: Equivalent circuit representation of electrolytic capacitors.

In the figure, C_{E} is the equivalent capacitance, which decreases with increase in frequency. The capacitance decrease can be tenfold between 10 Hz to 10 kHz. This frequency dependence is not very important for the present analysis since high-frequency current components are usually supported by the foil capacitors, which are part of input EMI filter of the WPS. L_{ESL} is the equivalent series inductance, which depends on the geometry and the size of the capacitor. Its value usually range from 10 nH to 30 nH for radial leaded type capacitors, 20 to 50 nH for screw-terminal type, and up to 200 nH for axial leaded types [62, 63]. The resistance R_{P} is the equivalent parallel resistance and accounts for the leakage current. This depends on temperature and the rated capacitance. It usually has a value close to hundreds of MΩ in parallel for each µF of capacitance value. This component is also not very important in case of WPS application, since the question of long term storage does not arise. The Zener diode D_{Z} closely models the overvoltage and the reverse voltage behaviour of an electrolytic capacitor [63]. The Resistance R_{ESR} is the Equivalent Series Resistance (ESR). With respect to the WPS under consideration, it is the most important factor that needs to be considered, as it has a direct influence on the power losses. Further, it is also very important and interesting to know the characteristics of this ESR.

4.2.3 Characteristics of equivalent series resistance

The ESR of an electrolytic capacitor increases with decrease in frequency. In order to understand this behaviour one needs to look into the physical structure and the chemical characteristics of the electrolyte used [66]. According to [63, 66], for electrolytic capacitors, the mathematical relation between ESR and frequency (for approximately less than 10 Hz) is represented by the below equation.

$$R_{\mathrm{ESR}} = \frac{DF_{\mathrm{lf}}}{2\pi f C} + R_{\mathrm{ESRhf}} \tag{4.4}$$

where R_{ESR} is the effective ESR at frequency f, DF_{lf} is the low-frequency dissipation factor (refer [63, 66] for the definition of dissipation factor), R_{ESRhf} is the high-frequency ESR and C is the rated capacitance. The low-frequency dissipation factor DF_{lf} results

from the power lost by the applied electric field in orienting the molecules of the dielectric. R_{ESRhf} results from the resistive losses in the foils, connections and the resistance offered by the electrolyte used [63]. DF_{lf} usually ranges from 0.015 to 0.03. Further, the temperature dependence of low-frequency ESR is almost negligible, as compared to that of high-frequency ESR, which decreases with temperature [63]. Furthermore, the term low-frequency is used to signify the range of frequencies for which DF_{lf} comes into effect, which is usually below 10 Hz. Fig 4.3, shows the expected frequency versus R_{ESR} characteristic of a 350 V, 15 mF capacitor from a particular manufacturer (Vishay). The curve corresponds to an R_{ESRhf} of 12 mΩ and DF_{lf} of 0.025. This frequency characteristic of the R_{ESR} is not expected to change significantly across different manufacturers, particularly the part of the curve for frequencies below 10 Hz.

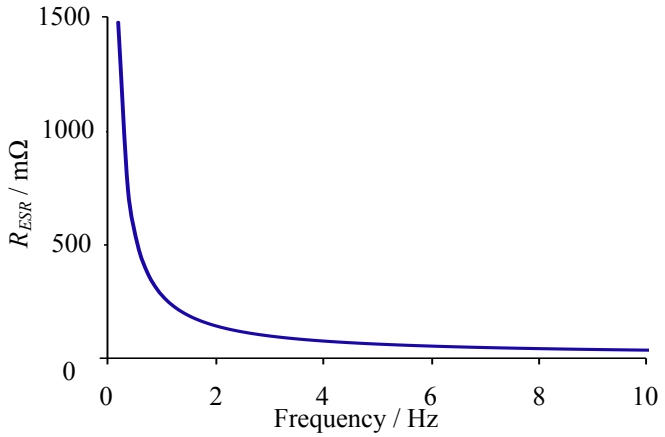


Fig. 4.3: R_{ESR} versus frequency characteristic for a 350 V, 15 mF capacitor from Vishay.

4.2.4 Power loss calculation

Due to the frequency dependence of the R_{ESR}, the power losses have to be separately calculated for each frequency component of current flowing through the capacitor. The sum of these losses correspond to the total power loss, as represented by the following equation.

$$P_{\mathrm{capL}} = \sum_{\mathrm{k}=1}^{n} I_{\mathrm{k}}^2 \, (R_{\mathrm{ESR}})_{\mathrm{k}} \tag{4.5}$$

where I_{k} is the RMS value of k^{th} harmonic frequency component of the ripple current, and $(R_{\mathrm{ESR}})_{\mathrm{k}}$ is the R_{ESR} corresponding to the k^{th} harmonic. [67, 68] present the detailed procedure of calculating the losses in electrolytic capacitors, following 4.5. The practical limit of n is, where the square of the RMS value of capacitor current (I_{c}) becomes almost equal to the sum of squares of RMS values of all the components up to the n^{th} harmonic, as shown below.

$$I_{\mathrm{c}}^2 \approx \sum_{\mathrm{k}=1}^{n} I_{\mathrm{k}}^2 \tag{4.6}$$

4.2.5 Designing for life time

The life time of electrolytic capacitors is dependent on its internal temperature, ambient temperature and to a little extent on the voltage de-rating [60]. The expected life of an electrolytic capacitor can be calculated using the following equation.

$$L_{\text{exp}} = K_{\text{v}}\, L_{\text{o}}\, 2^{\frac{T_{\text{o}}-T_{\text{x}}}{T_1}}\, 2^{\frac{\Delta T_0-\Delta T}{T_2}} \tag{4.7}$$

where L_{exp}= expected life,
L_{o} = specified life time at maximum core temperature limit,
T_0 = maximum rated ambient temperature,
T_{x} = actual ambient temperature. It is assumed that the actual ambient temperature is completely controlled by the cooling system and is a constant during operation. Further, the upper limit of the cooling liquid temperature in an industrial set-up is usually 40 °C,
ΔT_0 = raise in temperature at rated current (core temperature minus ambient temperature),
ΔT = actual raise on temperature = $P_{\text{capL}}\, R_{\text{thc-case}}$. Where $R_{\text{thc-case}}$ is the thermal resistance of the capacitor from core to case, which is provided by the capacitor manufacturer,
K_{v} = voltage de-rating factor (rated voltage/applied voltage) and
T_1 and T_2 are constants equal to 10 K and 5 K respectively.

The design process of an ECS can be explained in short as follows. As an initial guess, a capacitor bank is chosen as per energy requirements (this will be dealt in the next sections). Then, the capacitor power losses are calculated as per Equation 4.5. Once the capacitor power losses are known, Equation 4.7 can be used to calculate the maximum ambient temperature which needs to be maintained, in order to achieve the target life time (usually 10 years). If the calculated value of this temperature is below 40 °C, it means that, the given capacitor bank is not enough to achieve the target life. Therefore, one needs to increase the storage size by connecting more number of capacitors in parallel, which in turn reduces the ESR and the losses.

4.2.6 Step-wise process for storage sizing

The process for sizing the electrolytic capacitor storage for a SBRSWPS is shown in Fig 4.4.

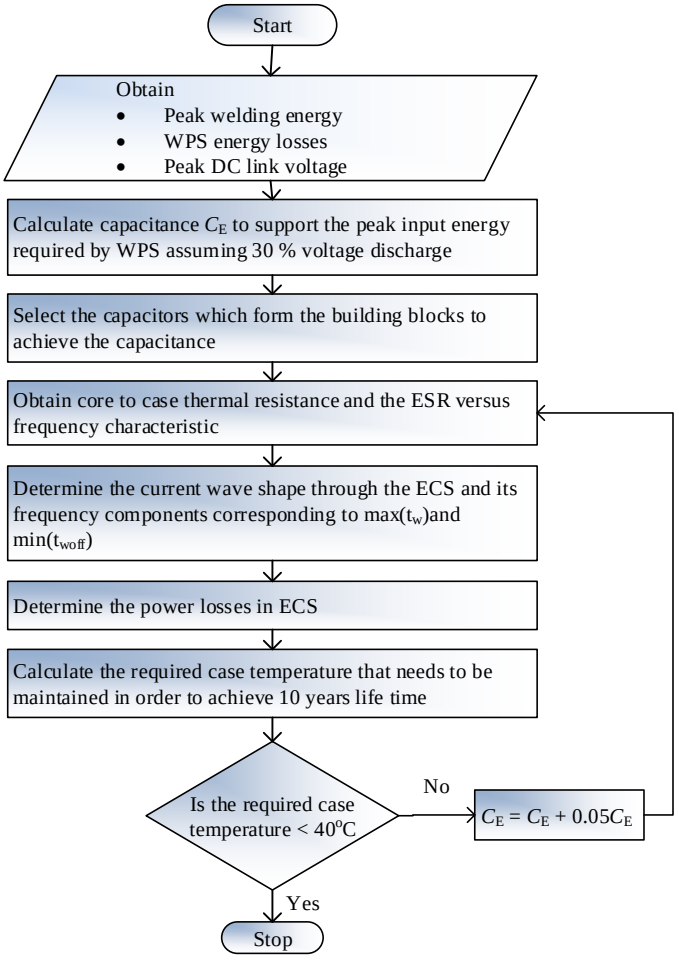


Fig. 4.4: Flow chart showing the process to be followed for sizing the electrolytic capacitor storage for a SBRSWPS.

As shown in Fig 4.4 the first step is to determine the peak welding energy and the corresponding energy losses in the WPS. From Fig 4.1, the voltage rating corresponding to maximum energy density is 350 V (can vary slightly for different manufacturers). Thus, the appropriate peak DC link voltage turns out to be 315 V (90 % of rated voltage). The second step is to determine the capacitance required, based on the usable energy density. The basic capacitor component that will be used to achieve the required capacitance (by connecting a number of them in parallel) is selected in the next step. Further, the corresponding core to case thermal resistance and the R_{ESR} versus frequency characteristic (like the one shown in Fig 4.3) is obtained. In the following step, the current profile through the capacitor bank needs to be determined. Additionally, the harmonic components in the current needs to be determined. As an example, with a capacitance of 2.57 F, with a peak storage voltage of 315 V and for approximately 30 % voltage discharge at the end of the welding process, the approximate waveform of

capacitor current through the storage system and its frequency components are shown in Fig 4.5. The load corresponds to 100 kW of power supplied to the weld pieces plus 30 kW of power losses in the WPS. Charging at constant power (13 kW) was considered during the no-load period.

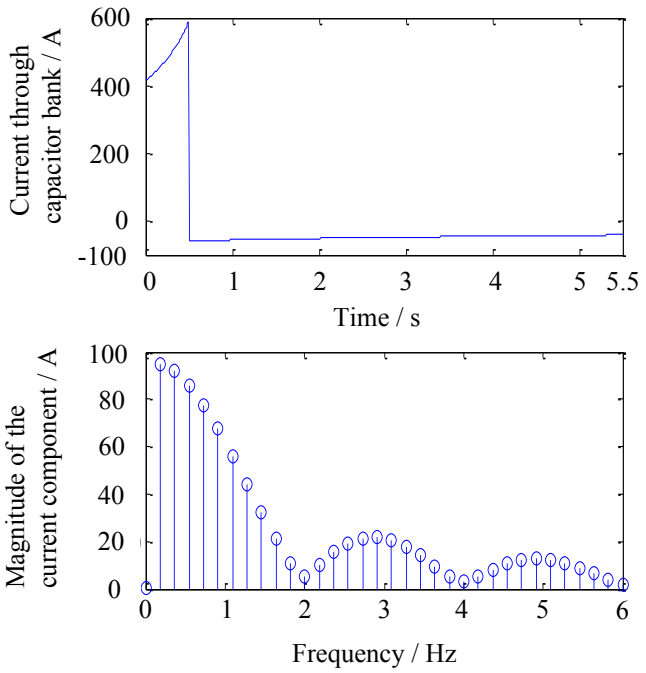


Fig. 4.5: Waveform of current through the storage system and its frequency components.

Further, the current components in each of the parallel capacitor elements can be easily determined, as the number of capacitor elements in parallel is known. The next step is to calculate the power losses in each capacitor using the Equation 4.5. The maximum case temperature (cooling liquid temperature) that needs to be maintained to achieve a life of 10 years is calculated in the next step. If this temperature turns out to be less than 40 °C, then the capacitance has to be increased till a point where the required case temperature is above 40 °C. Table 4.1 shows the characteristics of the required electrolytic storage system, which can support the specifications of the SBRSWPS presented in Chapter 2. WPS topology is assumed to be a PSFB and the corresponding losses are taken from Fig 3.11 in Chapter 3.

One needs to notice that the volume of 240 l corresponds to the use of long life capacitors from Vishay. By utilising commercial capacitor types which have a higher energy density, it is possible to reduce the volume to about 80 % of this value.

Table 4.1: Parameters of the electrolytic capacitor storage suitable for the SBRSWPS specified in Chapter 2

Parameter	Data
Volume of electrolytic capacitor bank	$\approx 240\,\mathrm{l}$
Storage efficiency at peak-load	99.87 %
Storage efficiency at nominal-load	99.96 %
Total capacitance	2.57 F
Capacitance element	15 mF
Manufacturer	Vishay
Part number	MAL210445153E3
Voltage rating	350 V
Storage voltage	315 V
Discharged voltage	220.5 V
Thermal resistance (Core to bottom of case)	0.31 °C/W
Thermal resistance (Case to ambient)	1.67 °C/W
Temperature of cooling liquid required	$\leq 105\,^{\circ}\mathrm{C}$

4.3 Evaluation of double layer capacitors based storage

The volumetric energy density of DLCs is quite higher than that of electrolytic capacitors. Further, the energy density of DLC modules is almost independent of its voltage rating. This is due to the fact that higher voltage DLC modules are always made up of series connection of 2.7 V modules with an additional voltage balancing circuit [69]. The rated value of energy density is approximately about $9\,\mathrm{kJ\,l^{-1}}$. In practice this is never achievable due to the voltage de-rating, which is necessary to achieve a reasonable life time. The typical dependency of lifetime on applied voltage and operating temperature of a DLC is pictorially shown in Fig 4.6. Life degradation has a larger influence on the series DC resistance, rather than that on the capacitance value. As per industrial standards, the End of Life (EOL) corresponds to a 20 % decrease in capacitance or a 100 % increase in the series DC resistance or both [69].

As mentioned earlier, for industrial setups, the maximum temperature limit of the cooling liquid circulated is 40 °C. Hence, each cell needs to be operated at approximately 2.38 V (instead of 2.7 V) in order to achieve a life of 10 years. This corresponds to a voltage de-rating of 11.8 %, which in turn reduces the usable volumetric energy density of DLCs to $6.96\,\mathrm{kJ\,l^{-1}}$. This is about 22 % less than the corresponding rated volumetric energy density of $9\,\mathrm{kJ\,l^{-1}}$.

4.3.1 Power density

The term “power density” can be defined as the maximum power that can be delivered by unit volume of storage. According to the maximum power transfer theorem, the peak

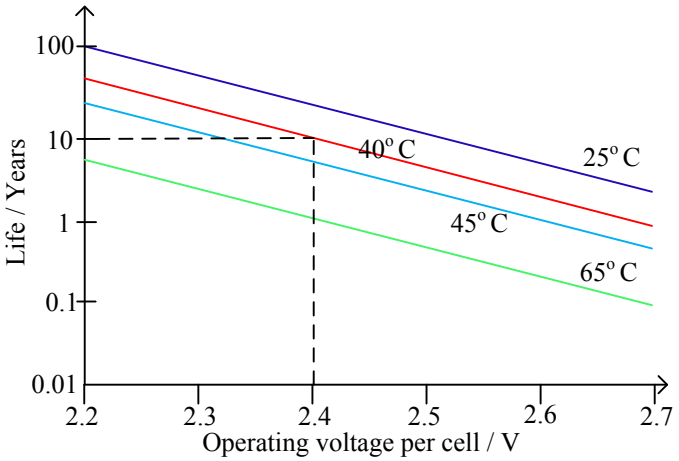


Fig. 4.6: Typical DLC life time dependency on applied voltage and its operating temperature [70]

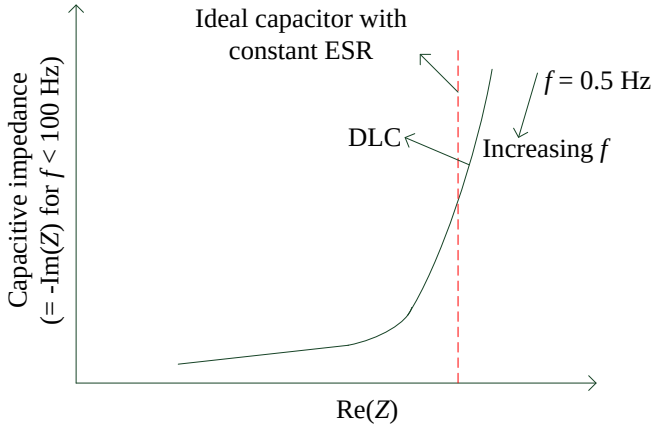
deliverable power output from any DC power source is practically limited to

$$P_{\text{omax}} = \frac{1}{2}\frac{V_{\text{s}}^2}{R_{\text{s}}} \tag{4.8}$$

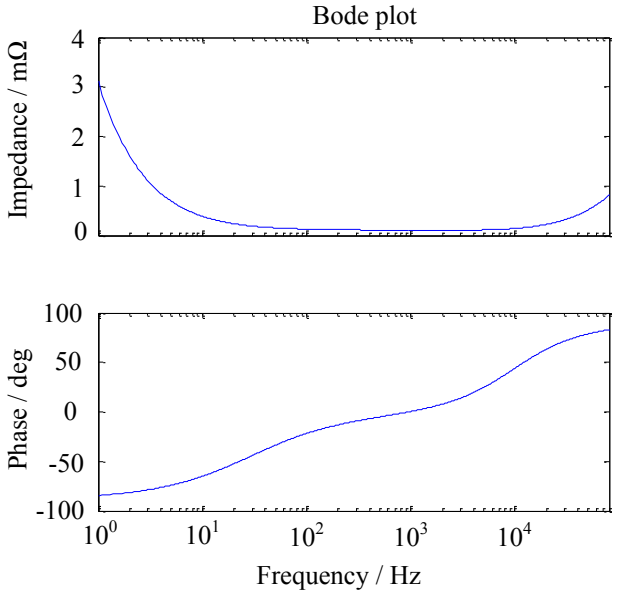
where V_{s} is the source voltage and R_{s} is the internal resistance of the source. In the present context, the source has to be replaced with a charged DLC module. DLCs have a considerably large low-frequency internal resistance, R_{DLC} (refer DLC model in the next subsections). For a DLC module with rated capacitance of C_{DLC}, the $R_{\text{DLC}}\,C_{\text{DLC}}$ time constant is about 1 second (this is based on the present state of the DLC technology) which is quite high as compared to that of electrolytic capacitors. This results in a usable peak power density of about $1.8\,\text{kW}\,\text{l}^{-1}$. Further, this usable power density corresponds to the beginning of discharge and goes down as the DLC discharges. Furthermore, it is important to note that the storage efficiency is just 50 % when utilising the maximum power density (from maximum power point theorem), which cannot be considered as reasonable.

4.3.2 Frequency characteristics

Fig 4.7a and Fig 4.7b show a typical frequency characteristic of a DLC module. Fig 4.7a shows the typical variation of resistance and reactance with frequency f, not considering the ESL [71]. While Fig 4.7b shows a typical Bode plot of the terminal impedance of a DLC. The Bode plot at lower frequencies (less than 100 Hz) is dominated by the capacitance and resistance characteristic. The increase in impedance at high-frequency (greater than 10 kHz) is due to the ESL.



(a) Typical resistance versus capacitive impedance characteristic of a DLC with varying frequency (f),without considering the ESL.



(b) Bode plot showing a typical impedance characteristic of a DLC.

Fig. 4.7: General frequency characteristic of DLCs.

4.3.3 Equivalent circuit model

There exist a variety of electrical models for DLCs, which are proposed by various researchers. Some models are based on lumped parameters, which use circuits with multiple branches, comprising of capacitive and resistive elements [72–74]. While, some of them are fractional models, arising from the chemical structure of the porous electrolyte [71]. The model shown in Fig 4.8 gives good accuracy with minimal efforts for parameter extraction [71].

In the equivalent circuit model shown, The capacitance C_1 is the DC capacitance of the DLC module, R_1 is the DC resistance (resistance at frequencies below 0.5 Hz). R_2 is the

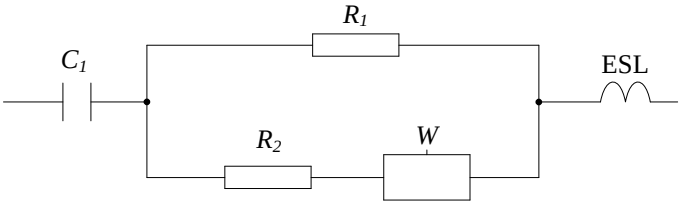


Fig. 4.8: Equivalent circuit model of a DLC

non-varying component of the AC resistance arising from the connectors, ω_0 is a constant with dimensions of rad/s which is introduced to maintain dimensional correctness of the model. While, W is the Warburg impedance which varies with frequency. The Warburg impedance is given by.

$$W = \frac{Z_o}{\left(j\frac{\omega}{\omega_0}\right)^{\frac{1}{2}}} = Z_o\sqrt{\frac{\omega_0}{\omega}}\left(\frac{1}{\sqrt{2}} - j\frac{1}{\sqrt{2}}\right) \tag{4.9}$$

The value of $Z_o\sqrt{\omega_0}$ is a constant proportional to the DC capacitance. The Warburg impedance brings in the frequency dependence of series resistance. When frequency is increased, the number of pores which are accessible are reduced. Further, the ion movement is restricted to the outer surface of the accessible pores. Hence, the resistance reduces with increase in frequency. This fractional behaviour is modelled by the Warburg impedance. It has been proved that the accuracy of such a model is reasonably good [71].

The ESL value is highly dependent on the DLC package style and size. Its value is specified in the datasheet. The values of C_1 and R_1 are also provided in the datasheet. R_2, which corresponds to the high-frequency resistance, can be obtained from the spectral analysis (usually at greater than 1 kHz). Thus, the only unknown constant is $Z_o\sqrt{\omega_0}$. Various values of $Z_o\sqrt{\omega_0}$ needs to be evaluated, and the value which gives the best fit has to be selected.

The conclusion from the discussion so far is that, at frequencies above 1 kHz, the inductive impedance of the DLC increases. At frequencies above 10 kHz, the DLC practically stops responding like a capacitor.

As far as SBRSWPS is considered, the high-frequency current components demanded by the input of the WPS are usually supported by its local input filter capacitors. Hence, the high-frequency response of DLCs is of less importance as far as the present RSW application is considered.

4.3.4 Step-wise process for storage sizing

Unlike electrolytic capacitor storage, the losses associated with DLC storage can be considerably higher and are highly dependent on the size of the DLC used. A larger DLC module (with same voltage rating) presents a smaller DC resistance and hence exhibits a better efficiency performance. The objective of this particular section will be to obtain the storage efficiency versus volume curve for a DLC storage, in reference to the SBRSWPS application under consideration. In order to simplify the process of DLC based storage system for a SBRSWPS, it is assumed that the change of the DLC voltage between its fully charged state to that at the end of the welding duration is negligible. This is a reasonable assumption, since, even when continuously delivering its maximum power output, the DLC voltage at the end of 500 ms duration will be about 70 % of initial voltage. The error introduced due to such an assumption decreases with the ratio of the load power to the peak power capability of the DLC storage. Fig 4.9 shows a flowchart depicting the process of obtaining the efficiency versus DLC volume curve for a SBRSWPS.

The first step in the process is to determine the nominal and peak welding powers from the specification sheet of the SBRSWPS under consideration. Also, the volumetric capacitance density ($\mathrm{F\,l^{-1}}$) and the RC time constant of the DLC modules have to be obtained from the DLC datasheet (product of R_1 and C_1 when considering the equivalent circuit model in Fig 4.8). The volumetric capacitance density value depends on the voltage rating of the DLC module (e.g. $6\,\mathrm{F\,l^{-1}}$ for 56 V DLC modules). The *RC* time constant depends only on the DLC technology and modern DLCs usually have a value between 0.8 to 1 s. In the second step, the losses of the WPS, corresponding to both nominal and peak welding power outputs are calculated and the corresponding input powers demanded by the WPS are obtained. One needs to note that the welding power supply losses are not negligible and hence need to be considered (refer Chapter 3 for WPS losses).

To begin with, a target storage efficiency of 50 % is assumed, when WPS is delivering peak welding output power (peak-load). The DLC output current and the required DC resistance of the DLC module that gives the target storage efficiency can be obtained by solving the following equations.

$$I_{\mathrm{DLCp}} = \frac{P_{\mathrm{WPSip,PL}}}{V_{\mathrm{DLC}}\,\eta_{\mathrm{DLCp}}} \tag{4.10}$$

$$R_{\mathrm{DLC}} = \frac{V_{\mathrm{DLC}}\,I_{\mathrm{DLCp}} - P_{\mathrm{WPSip,PL}}}{I_{\mathrm{DLCp}}^2} \tag{4.11}$$

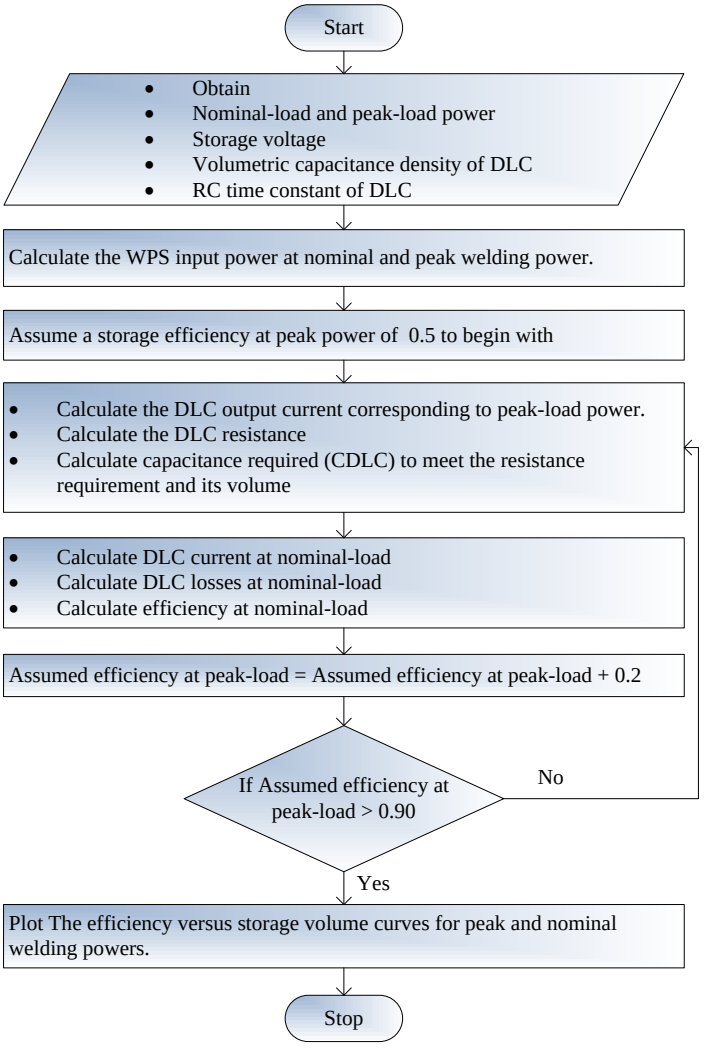


Fig. 4.9: Flow chart showing the process of obtaining the efficiency versus DLC storage volume curve for a SBRSWPS.

where I_{DLCp} is the output current of the DLC module at peak-load, η_{DLCp} is the target efficiency of the DLC storage at peak-load, R_{DLC} is its DC resistance, $P_{\mathrm{WPSip,PL}}$ is the WPS input power at peak-load and V_{DLC} is the charged state open circuit voltage of the DLC module.

Once the DC resistance is obtained, the required DLC module capacitance C_{DLC} can be calculated easily using the following relation.

$$C_{\mathrm{DLC}} = \frac{\tau_{\mathrm{DLC}}}{R_{\mathrm{DLC}}} \tag{4.12}$$

where τ_{DLC} is the RC time constant of the DLC technology.

Once the required DLC module capacitance is obtained, approximate volume of the DLC can be obtained using the volumetric capacitance density which is obtained in the first step.

In the next step, the DLC output current corresponding to nominal welding power is calculated by solving the following equation, where everything except I_{DLCn} is known.

$$P_{\mathrm{WPSip,NL}} = V_{\mathrm{DLC}}\, I_{\mathrm{DLCn}} - I_{\mathrm{DLCn}}^2\, R_{\mathrm{DLC}} \tag{4.13}$$

where $P_{\mathrm{WPSip,NL}}$ denotes the welding power supply input power when delivering nominal welding load and the subscript n denotes the corresponding parameters at nominal-load condition.

Once I_{DLCn} is known, the DLC storage efficiency at nominal power can be calculated using Equation 4.10, with subscript p changed to n.

Thus, the result of the process is a volume of the DLC and the corresponding storage efficiencies at nominal and peak power outputs of the WPS. In order to obtain the storage efficiency versus DLC volume curve, the same process can be iterated by incrementing the target peak-load efficiency.

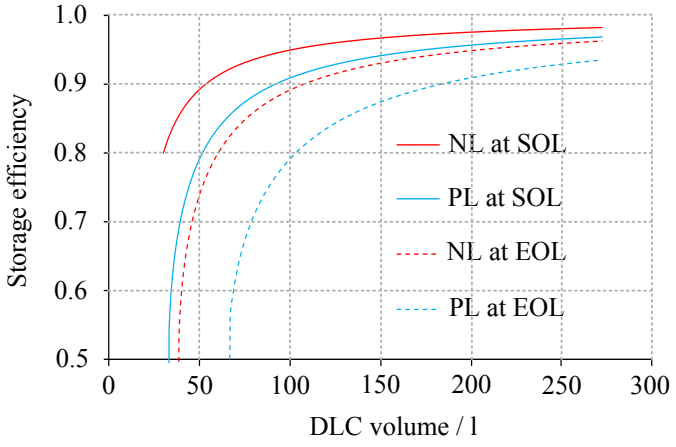


Fig. 4.10: Storage volume versus storage efficiency for nominal and peak power output at SOL and EOL. PL implies peak-load and NL implies nominal-load.

The above process was performed for a SBRSWPS with desired specifications given in Chapter 1. Data corresponding to 56 V Maxwell DLC modules with τ_{DLC} of 0.8 s was considered for analysis. Further, a storage voltage(V_{DLC}) of 44 V was considered. WPS power loss data corresponding to interleaved buck topology was utilised. The corresponding DLC storage efficiency versus volume curves obtained are shown in Fig 4.10. The figure shows the nominal and peak-load storage efficiency versus volume curves, both at Start Of Life (SOL) and End of Life (EOL) of the DLC capacitors. EOL

corresponds to a point in time, when the value of R_{DLC} has doubled to that at SOL. With ageing, one can expect a performance somewhere in between that of the corresponding SOL and EOL curves. From a system level perspective, it can be concluded that, when compared to electrolytic capacitor storage, the use of DLC storage reduces the storage system volume from about 250 l to 100 l at an expense of 5-10% drop in efficiency.

4.4 Evaluation of flywheel storage system

Fig 4.11 shows a possible configuration of a flywheel energy storage-based RSW power supply. As shown in the figure, the system consists of two back to back connected AC/DC converters which constitute the charger which is rated to a fractional value of the peak-load power. This charger is responsible to accelerate the flywheel to its rated angular velocity (ω_1). An additional fully rated AC/DC converter is employed to convert the AC voltage generated by the motor (working as a generator) to a DC voltage, which can be used by the welding power supply. A separate DC/DC converter constitutes the WPS, whose objective is to generate high currents at low voltages as required by the load. As an example, if the duty ratio of the load (welding duration (t_{w}) : idle duration (t_{woff})) is 1:10, the power rating of charger can be approximately 10 times smaller than that of the welding power supply. One can think of multiple other configurations resulting from various combinations of power electronic converters that can be used to achieve similar results. However, further analysis in this thesis will be based on the configuration shown in Fig 4.11.

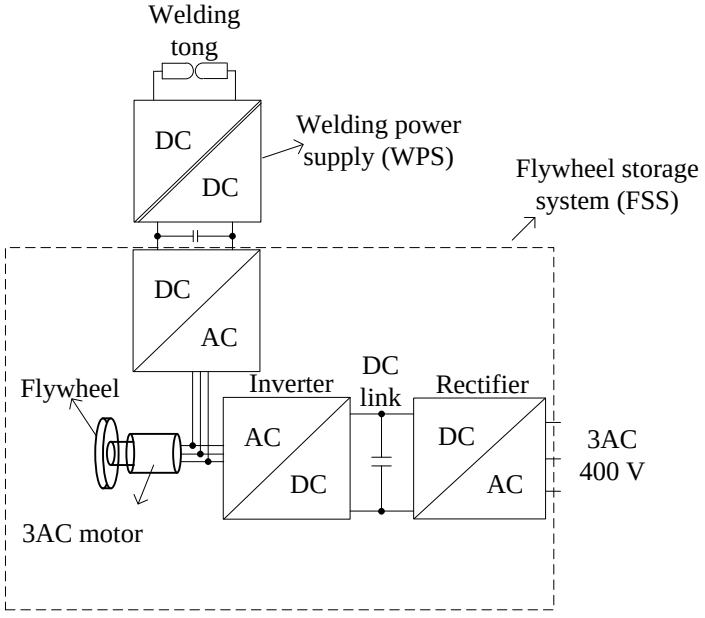


Fig. 4.11: Block diagram of a flywheel storage-based resistive spot welding system.

Theoretical design of a FSS involves a large number of variables. The variables of interest for the present analysis are presented in Table 4.2. The table also provides the assumed values for each of the variables and the reason behind those assumptions, wherever necessary.

Table 4.2: List of variables used for the analysis of FSS along with assumptions

Variable / Parameter	Assumption	Reason / Description
Motor type	Surface Mounted Permanent Magnet Synchronous Motor (SPMSM)	Please refer Section B.2 in Appendix B.
Motor efficiency η	0.95	In general, SPMSM motors are designed with efficiencies between 0.94 and 0.96 hence a figure of 0.95 is chosen.
Ampere loading A	$20\,\mathrm{kA\,m^{-1}}$ for air cooled and $80\,\mathrm{kA\,m^{-1}}$ for liquid cooled motors	These values correspond to values on the lower side of those achievable, as per literature [75, 76].
Peak air-gap flux density $B_{\mathrm{m,ag}}$	0.99 T	This can be obtained using rare earth magnets [75, 76].
Number of poles p	4	For rated speeds in the range of 5000-40 000 $\mathrm{min^{-1}}$, 4-8 poles seems to be a normal choice by manufacturers. Higher number of poles will result in manufacturing difficulties, while lower number of poles will result in larger size [77].
Aspect ratio (rotor length : pole pitch)	Between 2:1 and 4:1	This is an usual value for motors with rated speeds in the range of 5000-40 000 $\mathrm{min^{-1}}$[76, 77].
Winding factor	0.966	Two slots per pole per phase is assumed [78].
Motor Core material	ARNON 5	This is the core material of commercial choice for reduced core losses in high speed motors [79].
Motor inductance	0.2 Per Unit (P.U)	This is purely an assumption, as SPMSMs can be manufactured with different values of phase inductances, by varying the gap length. The normalisation quantity used for calculating the Per Unit (P.U) value is the rated voltage of the motor. As an example, 0.2 P.U of inductance implies an inductive voltage drop equal to 20 % of the rated motor voltage when operating under rated conditions.

Table 4.2: List of variables used for the analysis of FSS along with assumptions

Variable / Parameter	Assumption	Reason / Description
Rated speed of flywheel	5000-40 000 min^{-1}	For SBRSWPS applications, the energy storage requirement is not very high (as will be seen) and hence no real gain in volume is achievable by going for higher speeds. Further, magnetic bearings would be necessary at higher speeds, which increases cost.
Depth of discharge	<10 %	This results in a maximum energy discharge of 19 %. It is assumed that larger discharge depths in a discharge duration of <500 ms puts high stress on the mechanical parts. Refer Section B.3 in Appendix B for more description.
Flywheel shape and FSS design	Disk shaped solid flywheel coupled to a conventional inner rotor and outer stator motor	Solid disk shaped flywheel gives highest volumetric energy density and commercial availability of special motor types (outer rotor and axial flux machines etc) is limited [76].
Flywheel material	T-1000 Graphite, T-700 Graphite, Spectra 1000, Technora T220, Kevlar 49, S2 Glass, E Glass, 4340 steel	These materials are a usual choice for flywheels [76, 80]. For clarity purpose, it is worth mentioning that T-1000 implies that the maximum tensile strength of the corresponding material is 1000 ksi. Similarly the maximum tensile strength of T-700 graphite is 700 ksi, where "ksi" implies "kilo pascals per square inch".
Motor thermal time constant	Much larger then the time gap between consecutive weldings (5 s)	This is a reasonable assumption, which greatly reduces the complexity of thermal equations [81].
Windage and frictional losses	Neglected	In order to simplify the analysis.
Cooling jacket thickness	Negligible as compared to motor outer radius	In order to simplify the analysis.

Table 4.2: List of variables used for the analysis of FSS along with assumptions

Variable / Parameter	Assumption	Reason / Description
End winding effect on motor length	Considered by introducing a factor 1.3 between actual motor length to the rotor length	In order to simplify the analysis.
Flux density in the stator yoke	Same as that in air gap	–
Safety factor for mechanical stress in flywheel	2	Maximum stress in flywheel is limited to half of the material limit.

4.4.1 Geometrical structure used for the analysis

Motor structure: Motors with an outer rotor and inner stator structure can be significantly beneficial in reducing the overall volume of a FSS [82]. But the question is, are such motors commercially available? If not, is it commercially viable to develop such motors for low volume products like SBRSWPS. The answer is a clear no! (for both these questions). The same reasoning also holds good for axial flux machines. Indeed, due to practical cost considerations, the conventional radial flux inner rotor machines are the choice and hence used for the analysis.

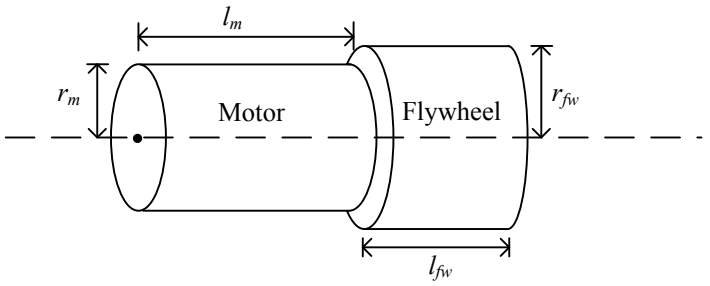


Fig. 4.12: Diagram showing the assumed motor and a flywheel structure for the analysis.

FSS structure: This thesis uses a simple FSS design concept. Where a flat disk shaped flywheel is connected to the rotor of an electrical motor. Fig 4.12 shows a diagram of such an arrangement. Other complex structures like, flywheel rotating on the outer hub of the electric motor etc. are not been considered in this work. It is unarguably agreed that such complex designs have a potential to reduce the volume of FSS. However, as it will be seen during the later part of this chapter, the energy that needs to be stored for SBRSWPS is relatively small and hence does not require a large flywheel. Thus, obviating the need for complex flywheel structures.

4.4.2 Step-wise process for storage sizing

Till date, no study has been reported in the direction of FSS volume estimation for pulsed power applications. Hence, out of necessity, an attempt has been made in this direction. The process consists of four major steps. In the first step, SPMSM dimensions are calculated for a given power rating, rotational speed, efficiency and aspect ratio. The distribution between copper and iron losses is also obtained. In the second step, the power losses in the motor, during the charging and discharging phase are calculated. Constraints due to thermal limits and demagnetization current limit are also considered. In the third step, the dimensions of the flywheel are calculated so that overall volume is minimised. In the fourth and final step, the efficiency of the obtained FSS at nominal power is calculated. The same process is repeated for different motor power ratings,

rotational speeds and aspect ratios. The results are appropriately plotted and analysed. Each of these steps is explained below.

4.4.3 Step 1: Determining the motor dimensions and loss distribution

The rotor dimensions of an electric motor are related to its power rating and rated rotational speed, by the following relation. [75, 76].

$$r_{\mathrm{im}}^2 l_{\mathrm{r}} = \frac{1}{\pi\sqrt{2}} \frac{P_{\mathrm{m}}}{A\, B_{\mathrm{m,ag}}\, K_{\mathrm{w}}\, \cos\Phi\, \eta\, \omega_{\mathrm{m}}} \tag{4.14}$$

where r_{im} is the rotor radius (approximately equal to the motor bore radius), l_{r} is the length of the rotor, P_{m} is the motor power rating, A is the circumferential ampere loading, $B_{\mathrm{m,ag}}$ is the peak flux density in the air-gap. Further, K_{w} is the motor winding factor, $\cos\phi$ is the displacement power factor, η is the efficiency of the motor and ω_{m} is the rated speed of the motor. For design purposes, a unity power factor is assumed. Further, to accommodate the stator end winding, a factor of 1.3 is assumed between the actual motor length l_{m} and calculated rotor length l_{r} from the above equation. Thus,

$$l_{\mathrm{m}} = 1.3\, l_{\mathrm{r}} \tag{4.15}$$

According to [76] and data provided in [77], the following inequality holds good.

$$1 < a_{\mathrm{ratio}} = \frac{p\, l_{\mathrm{r}}}{2\pi\, r_{\mathrm{im}}} < 4 \tag{4.16}$$

where p denotes the number of poles (p equal to four is assumed for this analysis as described in Table 4.2), a_{ratio} denotes the aspect ratio and r_{im} denotes the rotor radius (approximately equal to the motor bore radius). Further, an aspect ratio of close to 1 is suitable for low speed machines while, an aspect ratio of 4 is suitable for high speed machine designs [76]. From the datasheets of motor manufacturers [77], for speed ratings between $10\,000\,\mathrm{min}^{-1}$ and $40\,000\,\mathrm{min}^{-1}$, motors are available with aspect ratios between 2 and 4 (approximately). Hence, this analysis was carried out with aspect ratios of both 2 and 4. Further, one needs to understand that, as compared to Equation 4.14, which is true under all conditions, Equation 4.16 is just a design practice, based upon some practical manufacturing and application considerations.

Assuming the radial thickness of the stator yoke to be equal to half the pole pitch and not considering the depth of stator teeth, the outer radius r_{m} of the motor can be calculated

as

$$r_{\mathrm{m}} = r_{\mathrm{im}} \left(1 + \frac{\pi}{p}\right) \tag{4.17}$$

Neglecting the non-homogeneities in the stator flux and assuming sinusoidal flux distribution in the stator, the motor core losses can be approximately calculated using the Steinmetz equation.

$$P_{\mathrm{crtd}} = m_{\mathrm{stator}}\, K\, B_{\mathrm{m}}^{\alpha}\, f_{\mathrm{e}}^{\beta} \tag{4.18}$$

where m_{stator} is the mass of the stator yoke (can be calculated, once the volume of the yoke and its material density are known) K, α and β are the stator material constants, B_{m} is the peak flux density and f_{e} denotes the electrical frequency. It is very important to note that the core losses in the stator teeth are not considered in this work. In general, core losses in the stator teeth are considerable and cannot be neglected. Hence, it is proposed that the inclusion of the "core losses in stator teeth" will be taken up as part of the future work.

Using the "nlinfit" function in MATLAB for B_{m} in the range of 0.8-1.4 T and f_{e} in the range of 0.4 and 1.5 kHz, α equal to 1.7357, β equal to 1.2797 and K equal to $4.8\,\mathrm{mWkg^{-1}T^{-1.7357}s^{1.2797}}$ were obtained. These parameters result in an maximum relative error of less than 9% in the calculated power-loss density (within the given range of B_{m} and f_{e}). Power-loss density chart of ARNON-5 material in [83] was utilised as the data source for the purpose of curve fitting.

By utilising the above four equations and assuming that core and copper losses are the only loss contributors, one can make a fairly good estimate of the motor dimensions, its core and copper losses under rated conditions (provided that its power rating, rated speed, expected efficiency and other necessary parameters are known).

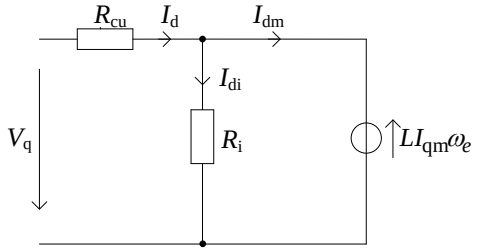
4.4.4 Step 2: Determining charging and discharging losses

Once the dimensions of the motor along with its rated core and copper losses are known, an estimate of the power losses during actual load conditions needs to be obtained. This is necessary, in order to determine the efficiency of the FSS, which in turn determines the efficiency of the welding process.

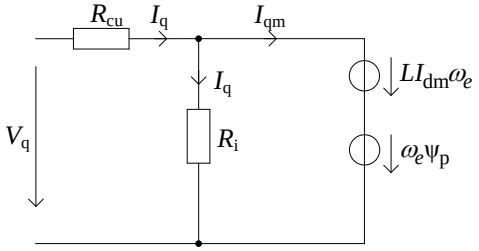
As stated earlier, this work utilises a 3-phase SPMSM for the purpose of the analysis. The classical two-dimensional voltage and current invariable representation [78] in the rotor reference frame is utilised for the analysis. The mathematical transformations behind the conversion of three phase quantities into two phase quantities are fairly

standard and hence no further explanation is provided here in connection to this subject. The conventions followed in [78] are utilised throughout this chapter.

Fig 4.13a and Fig 4.13b shows the steady state equivalent circuit model of a SPMSM in d-q reference frame, utilised in this work [84]. In the figures, I_{d} represents the d axis terminal current and I_{q} represents the q axis terminal current, I_{dm} represents the d axis magnetising current, I_{qm} represents the q axis magnetising current, ψ_{p} denotes the permanent magnet flux linkages, ω_{e} represents the electrical rotational velocity, L denotes the stator magnetising inductance (in both d and q axis), V_{d} represents the d axis terminal voltage and V_{q} represents the q axis terminal voltage. The effect of the stator leakage inductance has been neglected in the model.



(a) d axis equivalent circuit.



(b) q axis equivalent circuit.

Fig. 4.13: Steady state d and q axis equivalent circuits.

R_{cu} denotes the winding resistance per phase, which can be calculated once rated copper losses $P_{\mathrm{cu_rtd}}$, rated power P_{m} and rated peak phase voltage V_{m} of the motor are known. V_{m} is assumed to be 325 V for this work. The term R_{i} denotes a virtual per phase resistance to mimic the core loss power component, details of which are presented in [84]. The present analysis is performed, assuming constant speed operation (refer Section B.3 of Appendix B for details) hence, R_{i} is considered to be constant and equal to

$$R_{\mathrm{i}} = \frac{3}{2}\frac{V_{\mathrm{m}}^2}{P_{\mathrm{crtd}}} \tag{4.19}$$

where P_{crtd} are the rated core losses of the motor.

Considering the equivalent circuits in Fig 4.13a and Fig 4.13b, the steady state terminal power can calculated as

$$P_{\text{in}} = \frac{3}{2}R_{\text{cu}}(I_{\text{d}}^2 + I_{\text{q}}^2) + \frac{3}{2}\frac{\omega_{\text{e}}^2(\psi_{\text{d}}^2 + \psi_{\text{q}}^2)}{R_{\text{i}}} + \frac{3}{2}\omega_{\text{e}}\psi_{\text{p}}I_{\text{qm}} \tag{4.20}$$

where $\psi_{\text{d}} = I_{\text{qm}}L\omega_{\text{e}}$ denotes the d axis flux linkages and $\psi_{\text{q}} = \psi_{\text{p}}\omega_{\text{e}} + I_{\text{dm}}L\omega_{\text{e}}$ denotes the q axis flux linkages.

In the RHS of the above equation, the first term in the sum represents the copper losses, the second term represents the core losses and the third term equals the mechanical power generated.

During the welding process, the FSS discharges its stored energy and hence, the terminal power of the machine during the discharge phase (assuming constant welding power) is given by

$$P_{\text{in,dch}} = -P_{\text{WPSip}} = -(P_{\text{weld}} + P_{\text{WPSL}}) \tag{4.21}$$

where P_{WPSip} denotes input power of the welding power supply during welding, P_{weld} denotes the welding power and P_{WPSL} denote the welding power supply losses corresponding to welding power P_{weld}.

When the flywheel is being charged, the mechanical power that needs to be generated is given by

$$P_{\text{mech,ch}} = (P_{\text{cudh}} + P_{\text{WPSip}} + P_{\text{cdh}})\frac{t_{\text{w}}}{t_{\text{woff}}} \tag{4.22}$$

where P_{cudh} denotes the copper losses during discharge phase and P_{cdh} represents the core losses during discharge.

Voltage constraint: It is important to note that the terminal voltage of the motor needs to be limited to the voltage rating V_{max} of the inverter connected to the motor terminals. This limitation can be represented as

$$V_{\text{max}}^2 \geq (\psi_{\text{p}}\omega_{\text{e}} + I_{\text{dm}}L\omega_{\text{e}} + I_{\text{q}}R_{\text{cu}})^2 + (I_{\text{qm}}L\omega_{\text{e}} + I_{\text{d}}R_{\text{cu}})^2 \tag{4.23}$$

For the purpose of easier understanding, it could be beneficial to know that I_{q} is greater than or equal to zero during charging, I_{q} is less than or equal to zero during discharging and I_{d} is less than or equal to zero under both the operating modes. For this work, V_{max} is considered to be 2 % higher than the rated voltage V_{m}. Further, the maximum magnitude of I_{d} is limited by the demagnetization of the permanent magnets, which is a function of temperature and L. The higher the value of L and the temperature of the magnets, the lower the limit on the magnitude of I_{d}.

Thermal constraint: A simplified thermal model which can be used to determine the motor hotspot temperature under intermittent loading is presented in [81]. Under the assumption of forced cooling and considering the fact that the core losses does not vary much between the charging and the discharging phase, the model can be extended to the present case as follows.

$$\Delta T_{\mathrm{m}} = \Delta T_{\mathrm{rated}} \left(\frac{P_{\mathrm{mloff}}}{P_{\mathrm{mlrated}}} \right) + \Delta T_{\mathrm{rated}} \left(\frac{1 - e^{\frac{-t_{\mathrm{w}}}{\tau_{\mathrm{m}}}}}{1 - e^{\frac{-t_{\mathrm{w}} - t_{\mathrm{woff}}}{\tau_{\mathrm{m}}}}} \right) \left(\frac{P_{\mathrm{mlw}} - P_{\mathrm{mloff}}}{P_{\mathrm{mlrated}}} \right) \tag{4.24}$$

where
ΔT_{m} is the actual difference between the ambient and peak hot-spot temperature in the motor, for the given charge - discharge loading,
$\Delta T_{\mathrm{rated}}$ is the actual difference between the ambient and peak hot-spot temperature when running under rated conditions,
t_{w} = welding time,
t_{woff} = time gap between consecutive weldings,
τ_{m} = thermal time constant of the machine with respect to the hot-spot,
P_{mloff} = are the average motor losses during the interval between consecutive weldings (It consists of copper losses and core losses during charging),
P_{mlrated} = motor losses when operating under rated conditions and
P_{mlw} = average motor losses during welding.
A short background for the above equation is provided in Section B.5 of Appendix B

Given the assumption that τ_{m} is much larger than the sum of t_{w} and t_{woff}, the constraint introduced by thermal limit simplifies to

$$\frac{t_{\mathrm{w}} P_{\mathrm{mlw}} + t_{\mathrm{woff}} P_{\mathrm{mloff}}}{(t_{\mathrm{w}} + t_{\mathrm{woff}}) P_{\mathrm{mlrated}}} \leq 1 \tag{4.25}$$

The maximum value of the L.H.S in the Equation 4.25 is expected to occur under the conditions of worst case welding load cycle ($\max(t_{\mathrm{w}}) : \min(t_{\mathrm{woff}})$) coupled with peak-load conditions.

One can obtain the power losses during the charging and discharging phase by using the Equations 4.20, 4.21 and 4.22 under the constraint 4.23. Further, the constraint in Equation 4.25 can be used to check weather a particular underrated motor can be used without exceeding the specified thermal limit.

4.4.5 Step 3: Determining the optimal FSS volume

In steps 1 and 2 it has been explained how the motor outer radius r_{m} and its length l_{m}, along with its power losses under the operating conditions are obtained. Now, assuming motor losses to be constant during discharge phase and considering a maximum of 10% speed reduction during welding (under peak-load), the energy that needs to be stored in the flywheel E_{fw} is given by

$$E_{\mathrm{fw}} = \frac{1}{K_{10\%}} \left(P_{\mathrm{mlw,PL}} + P_{\mathrm{WPSip,PL}}\right) t_{\mathrm{w}} \tag{4.26}$$

where $K_{10\%}$ is a constant equal to 0.19 which corresponds to a maximum speed discharge of 10 %, $P_{\mathrm{WPSip,PL}}$ denotes the input power of the welding power supply under peak welding load, $P_{\mathrm{mlw,PL}}$ denotes the motor losses during welding under peak welding load (with motor working as a generator and delivering a terminal power equal to $P_{\mathrm{WPSip,PL}}$) and t_{w} denotes the welding duration.

Now, if r_{fw}, l_{fw} and ρ_{m} are the radius, length and mass density respectively of the required flywheel and if ω denotes the rated speed of the flywheel storage system. Then, assuming that the dimensions of the bearing enclosures are negligible to the length of the motor, the effective volume υ_{eff} used up by the combination of the motor and the flywheel system is given by.

$$\upsilon_{\mathrm{eff}} = \pi r_{\mathrm{fw}}^2 \left(l_{\mathrm{m}} + \frac{4E_{\mathrm{fw}}}{\pi r_{\mathrm{fw}}^4 \rho_{\mathrm{m}} \omega^2} \right) \text{ ; for } r_{\mathrm{m}} \leq r_{\mathrm{fw}} \leq r_{\mathrm{fw,max}}(\omega) \tag{4.27}$$

where $r_{\mathrm{fw,max}}(\omega)$ is the maximum flywheel radius allowed for the given material at an angular speed ω (refer Appendix B). υ_{eff} has a minimum value when,

$$r_{\mathrm{fw}} = \sqrt[4]{\frac{4E_{\mathrm{fw}}}{\pi \rho_{\mathrm{m}} \omega^2 l_{\mathrm{m}}}} \text{ ; limited by } r_{\mathrm{m}} \leq r_{\mathrm{fw}} \leq r_{\mathrm{fw,max}}(\omega) \tag{4.28}$$

The corresponding length of flywheel l_{fw} turns out to be

$$l_{\mathrm{fw}} = l_{\mathrm{m}}; \text{ limited by } l_{\mathrm{fw}} \leq \frac{4E_{\mathrm{fw}}}{\pi r_{\mathrm{m}}^4 \rho_{\mathrm{m}} \omega^2} \tag{4.29}$$

This is how the dimensions of the required flywheel can be determined. Further, it is important to note that the case of r_{m} greater than r_{fw} is out of question, for all practical purposes.

4.4.6 Step 4: Obtaining the volume versus efficiency curves

Storage efficiency of the FSS can be calculated as follows

$$\eta_{\mathrm{FSS}} = \frac{t_{\mathrm{w}}\, P_{\mathrm{WPSip}}}{t_{\mathrm{w}}\, P_{\mathrm{mlw}} + t_{\mathrm{woff}}\, P_{\mathrm{mloff}} + t_{\mathrm{w}}\, P_{\mathrm{WPSip}}} \tag{4.30}$$

Steps 1 to 3 can be repeated for various motor power ratings (P_{m} less than or equal to $\max(P_{\mathrm{weld}})$) at a given speed. The obtained efficiency versus FSS volume (motor and flywheel volume together) for peak-load and worst case welding load cycle can be plotted for that given speed.

As a next step, for the set FSS obtained earlier, the corresponding efficiencies when delivering nominal welding power and worst case welding load cycle can be calculated and plotted on the same graph.

The process can be repeated for several rated speeds and the corresponding volume versus efficiency curves be generated.

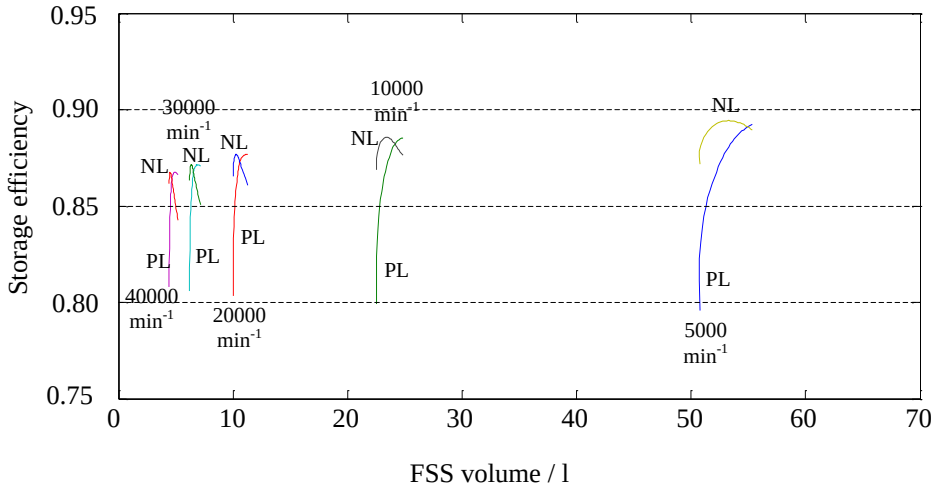


Fig. 4.14: Expected efficiency versus storage volume for FSS (motor volume plus flywheel volume) for the SBRSWPS under consideration. Aspect ratio = 2 and air cooling. Legend: PL - Peak-load, NL - Nominal-load.

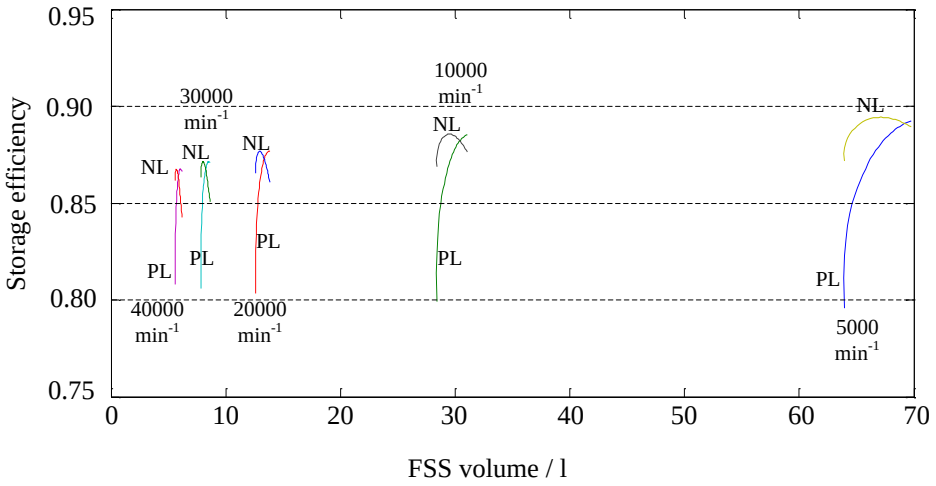


Fig. 4.15: Expected efficiency versus storage volume for FSS (motor volume plus flywheel volume) for the SBRSWPS under consideration. Aspect ratio = 4 and air cooling. Legend: PL - Peak-load, NL - Nominal-load.

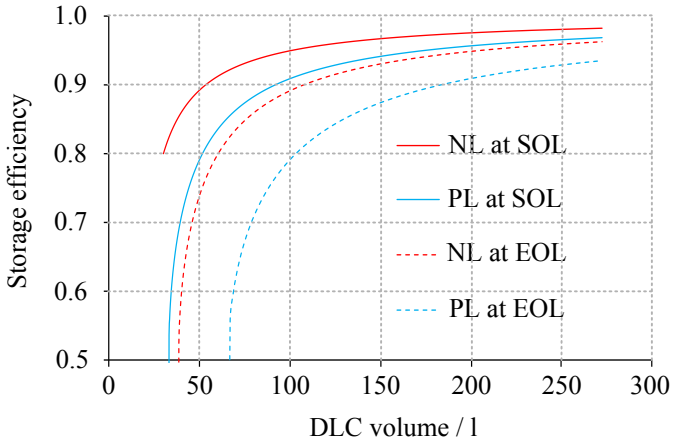


Fig. 4.16: Expected storage efficiency versus volume curves for a DLCS at nominal and peak power welding power (NL and PL respectively) at start of life (SOL) and end of life (EOL).

Fig 4.14 shows the expected volume versus efficiency curves for Peak-Load (PL) and Nominal-Load (NL) (at each speed), where the FSS is designed for peak-load case. The curves are plotted for an aspect ratio of 2 and with an assumption of air cooling. Fig 4.15 show the corresponding curves for an aspect ratio of 4. By comparing Fig 4.14 and Fig 4.15, it can be concluded that smaller aspect ratios of the motor result in smaller size of the FSS. Further, it is interesting to note that the peak efficiency of the FSS does not significantly depend on the aspect ratio. However, an obvious result that can be observed is the decrease of FSS volume, with increase in the speed. For the given application, the minimum possible motor rating without exceeding the thermal limit turns out to be approximately 40 % of the peak welding power (PL). This corresponds

to the lowest efficiency point on the curves for each speed. The maximum volume limit for each speed corresponds to a motor rating P_{m} equal to $\max(P_{\mathrm{weld}})$.

Fig 4.16 shows the volume versus efficiency curves for a DLCS at PL and NL, both at the Start of Life (SOL) and End of Life (EOL). If one designs a DLC storage for an minimum possible EOL efficiency of 0.5, the resulting storage volume is about 70 l. This is far more than that of FSS designed for speeds equal to or above $10\,000\,\mathrm{min}^{-1}$.

More interesting observation is that the peak nominal-load efficiency does not correspond to the peak volume of the FSS. This is due to the fact that a motor with larger power rating (at same rated speed) implies higher core losses, which are to a great extent independent of load (with the assumption of constant terminal voltage and speed [84]). While the rated core losses decrease with decrease in the motor power rating, the copper losses increase with the decrease in the motor power rating for a given load. Thus, there lies a motor rating (and corresponding volume of FSS) where the efficiency of the FSS is maximum.

The analysis uses ARNON-5 as the stator core material, with a lamination thickness of 0.127 mm. Though this material is a reasonable selection for high speed motors, there exist better materials [79] which can result in smaller core losses and higher peak efficiencies of the FSS. Further, it has to be noted that the motor efficiency assumed for the analysis is 0.95. When cost is not the deciding factor, this figure can be close to 0.97 in case of high speed machines.

The most important observation is that, when a DLC based storage system is designed for PL, its efficiency at NL is much higher than that corresponding to PL. However, this is not true for FSS with air cooled motors. When the motor utilises air cooling, the flywheel storage system can be best optimised for efficiency when the difference between PL and NL is small. However, the situation changes when a liquid cooled motor is used.

Fig 4.17 shows the expected volume versus efficiency curves for PL and NL for an aspect ratio of 2 and with liquid cooling.

From Fig 4.17 and Fig 4.14 it is very clear that the use of a liquid cooled motor results in better efficiencies of the FSS, together with a small decrease in the volume (motor and flywheel volume together) when compared to the respective air cooled counterparts. The main reason for such a shift in FSS efficiency can be attributed to the different loss distributions (core and copper loss distribution) for air and liquid cooled motors. In case of liquid cooled motors, the volume of the stator yoke is smaller as compared to that in case of air cooled motors. This is because the rotor radius and also flux in the air-gap decreases with increase in ampere loading. Hence, resulting in smaller core losses for liquid cooled motors as compared to that in air cooled motors (for a given

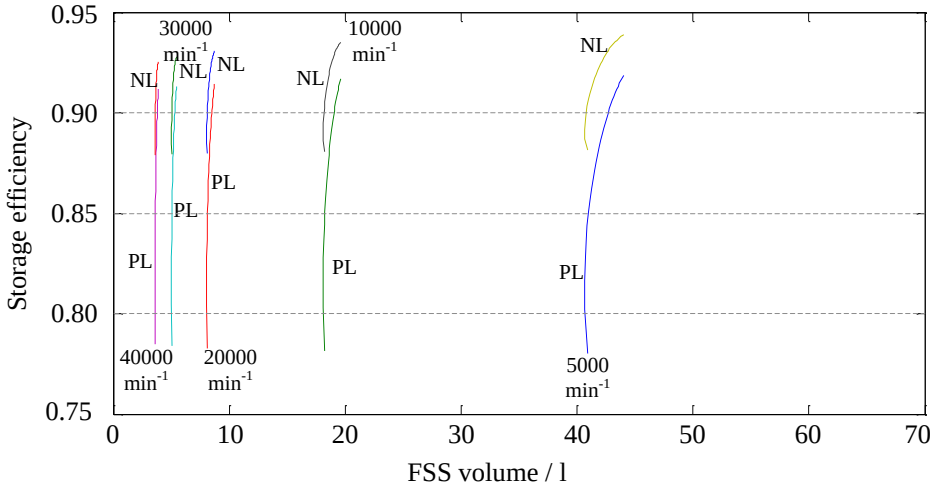


Fig. 4.17: Expected Efficiency versus storage volume for FSS (motor volume plus flywheel volume) for the SBRSWPS under consideration. Aspect ratio = 2 and liquid cooling. Legend: PL - Peak-load, NL - Nominal-load.

rated speed and power rating). The core losses are a major contributor to FSS charging losses (motoring operation), as a result FSS efficiency becomes better with liquid cooled motors.

It can be seen from Fig 4.16 that the DLC storage gives four different volume versus efficiency curves which correspond to Nominal-Load (NL) and Peak-Load (PL) at both Start of Life (SOL) and End of Life (EOL). But for flywheel storage, things are different as there is no effect of aging on efficiency. Hence, one can expect only two curves corresponding to NL and PL operation. It can be seen from Fig 4.17 that there are exactly two curves corresponding to each speed. One curve for NL operation and one curve for PL operation.

Let us analyse the curves corresponding to rated speed of $5000\,\mathrm{min}^{-1}$. The top right tip of the curves correspond to the NL and PL efficiencies for a $5000\,\mathrm{min}^{-1}$ flywheel storage system with its motor power rating equal to the peak welding power. Further, since welding application is an application with intermittent loading, one has the freedom to reduce the motor rating, without exceeding its thermal limits. If one concentrates on the peak-load (PL) curve corresponding to the rated speed of $5000\,\mathrm{min}^{-1}$ in Fig 4.17, two main observations can be made. The first observation is that the peak-load efficiency of the storage system drops as the motor power rating decreases, which is indeed expected. The second observation is that the curve reaches a minimum volume after which, any further reduction in motor rating results in a small increase in volume. This behavior can be explained as below.

Under the assumption that the flywheel radius is larger than the motor radius (which is true for the discussed cases), by definition the effective volume of the flywheel storage system is

$$\upsilon_{\text{eff}} = \pi r_{\text{fw}}^2 \left(l_{\text{m}} + l_{\text{fw}}\right) \tag{4.31}$$

Applying the Equations 4.28 and 4.29 in the above equation, we get

$$\upsilon_{\text{eff}} \propto \sqrt{\frac{E_{\text{fw}}}{l_{\text{m}}}} \left(l_{\text{m}} + l_{\text{m}}\right) \tag{4.32}$$

$$\propto E_{\text{fw}}^{\frac{1}{2}} \, l_{\text{m}}^{\frac{1}{2}} \tag{4.33}$$

From (4.26) it can be concluded that E_{fw} is a function of motor power rating P_{m}. This is because E_{fw} depends on the motor losses under peak welding load, which are in turn dependent on the motor power rating. Further, from 4.14 it is clear that l_{m} is also a function of P_{m}. Hence, by differentiating both sides of the above equation with respect to the motor power rating, we get

$$\frac{d\upsilon_{\text{eff}}}{dP_{\text{m}}} \propto E_{\text{fw}}^{\frac{1}{2}} \left(\frac{1}{2} l_{\text{m}}^{-\frac{1}{2}} \frac{dl_{\text{m}}}{dP_{\text{m}}}\right) + l_{\text{m}}^{\frac{1}{2}} \left(\frac{1}{2} E_{\text{fw}}^{-\frac{1}{2}} \frac{dE_{\text{fw}}}{dP_{\text{m}}}\right) \tag{4.34}$$

The above equation can be rearranged to get

$$\frac{d\upsilon_{\text{eff}}}{dP_{\text{m}}} \propto \frac{dl_{\text{m}}}{dP_{\text{m}}} \sqrt{\frac{E_{\text{fw}}}{l_{\text{m}}}} + \frac{dE_{\text{fw}}}{dP_{\text{m}}} \sqrt{\frac{l_{\text{m}}}{E_{\text{fw}}}} \tag{4.35}$$

In the above equation, the value of $\frac{E_{\text{fw}}}{l_{\text{m}}}$ increases with reduction in motor power rating. One can also note that $\frac{dE_{\text{fw}}}{dP_{\text{m}}}$ is negative and $\frac{dl_{\text{m}}}{dP_{\text{m}}}$ is positive. Hence, there exists a chance that $\frac{d\upsilon_{\text{eff}}}{dP_{\text{m}}}$ can have a zero value at some particular value of P_{m} that corresponds to minimum volume of the storage system. Further, at this point of time, it is worth recalling that the flywheel storage system is designed for peak-load requirements and the nominal-load (NL) curve corresponds to the same physical system (same volume) but reduced load operation.

It is very important to note that the results obtained from the analysis are with the assumptions under consideration. Two of the major effects which have not been considered in the analysis are the losses in the stator teeth and the effects of the switching converter (AC/DC). The loss estimates will certainly increase if one considers these effects. However, one need not be too pessimistic about the results obtained. It has to be noted that in practice the ampere-loading values can be much higher than that used for this work [75]. An increase in ampere-loading will result in smaller core losses, which can lead to an improvement in the expected FSS efficiency results. Further, it should be noted that AC/DC converter also contributes to the volume of the system. Especially,

when operating at high speeds, the motor and flywheel volume becomes smaller and hence, the volume of this additional converter can no more be neglected.

Finally, it is worth stating that the volume versus efficiency characteristic gives a better understanding of the benefits and drawbacks of the flywheel and DLC based storage systems. A successful attempt was made in developing a logical framework, under which such volume versus efficiency curves for flywheel storage can be generated and then compared to that of a DLCS. However, it is un-objectionably agreed that there is certainly a scope for further improvement to the analysis presented.

Chapter 5

Implementation Using Double Layer Capacitors and Interleaved Buck Converter

5.1 System overview

It is very clear from the previous analysis that, for the application under consideration, a FSS can be a smaller option as compared to a DLCS. However, based on the issues of implementation, maintenance, safety (controversial) and today's customer acceptance levels, it was decided to go ahead with a DLC based storage system.

The first choice of the converter topology turns out to be the ICTBC (with respect to efficiency and volume), followed by the IBC and the transformer based topologies. Further, the transformer based topologies need to be applied only if the storage system voltage is above 100 V. The IBC topology was selected for implementation, due to its simple structure, ease of implementation and no single point of failure.

The peak output voltage specification of the converter is 20 V. Hence, the storage voltage needs to be larger than 20 V. Based on availability, 56 V DLC modules were chosen, which limits the maximum storage voltage to about 44 V (due to life time issues).

Fig 5.1 shows a system level block diagram of the welding power supply. The system is divided into three blocks. The master card, the slave card and the power card. The function of the master card is to work as an interface between the external Programmable Logic Controller (PLC) system and the slave card. It receives the reference current value, processes it into a current signal (using an op-amp based voltage to current converter) which is transmitted as a current reference signal for all the slave cards. It

also communicates the welding duration to the slave cards, based on inputs from PLC system, safety limits and fault status of the slave cards. The master card is also the source of the synchronising signal for the PWMs on all slave cards.

The slave cards are responsible for phase shifting, control, signal conditioning, protection and communication of fault status to the master card. Each slave cards also incorporates in it, the necessary MOSFET drivers for the corresponding power cards. Each power cards contains six synchronously gated buck converters, the necessary magnetics, current sensors and the input EMI filters (SMD capacitors). Special care was taken during design, to reduce the loop inductances in the switching circuits. Each power card was designed to deliver a current of 1500 A, which corresponds to a current of 250 A per phase (with n equal to six).

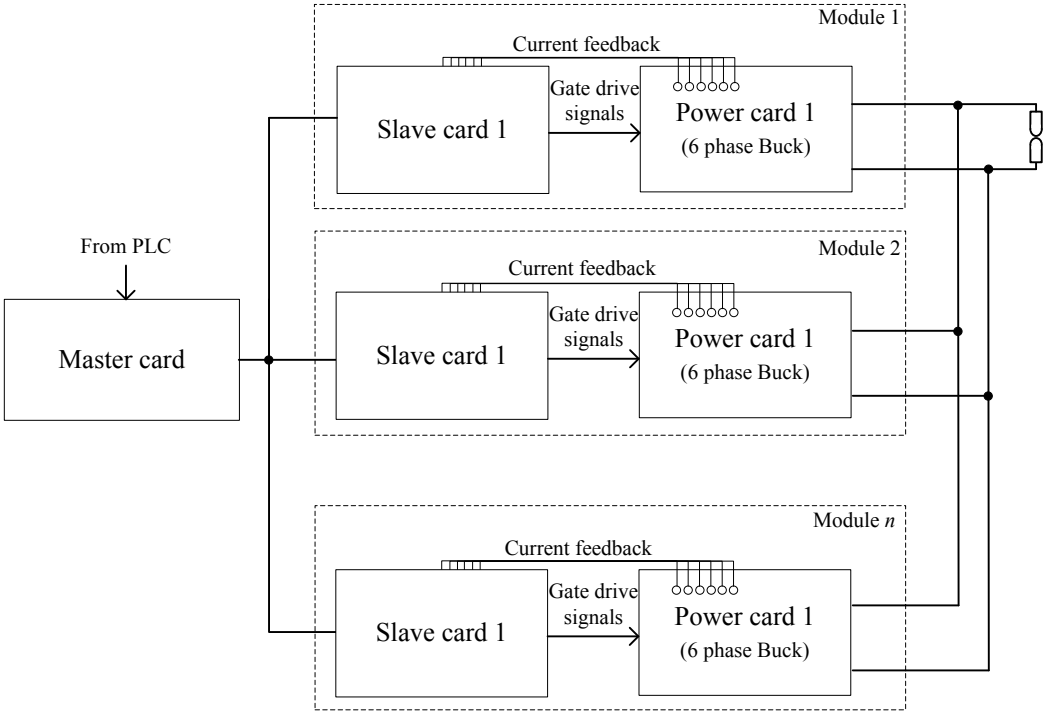


Fig. 5.1: System block diagram.

Fig 5.2, Fig 5.3 and Fig 5.4 show the pictures of the master, slave and power cards respectively.

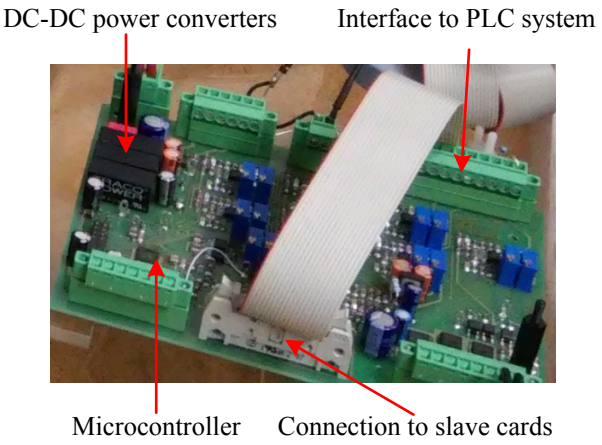
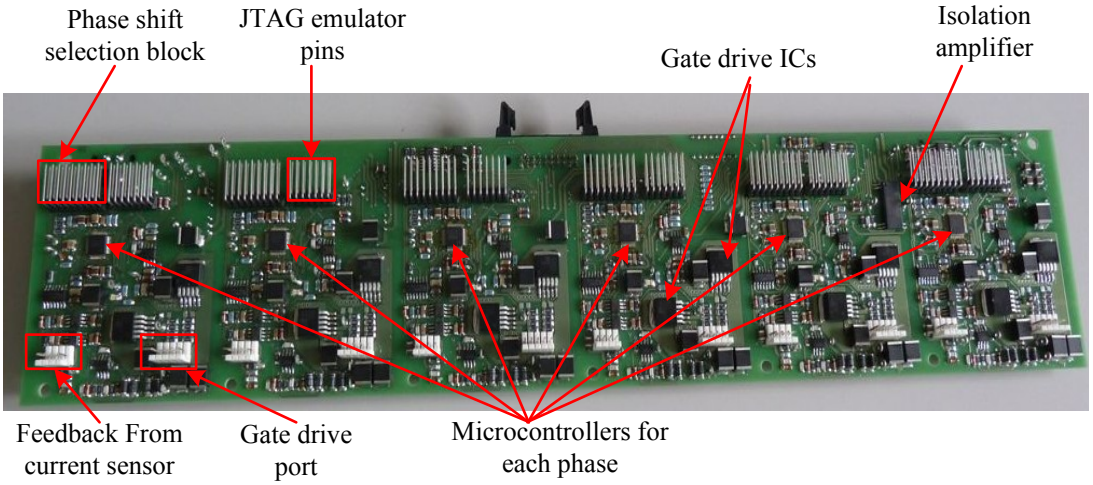
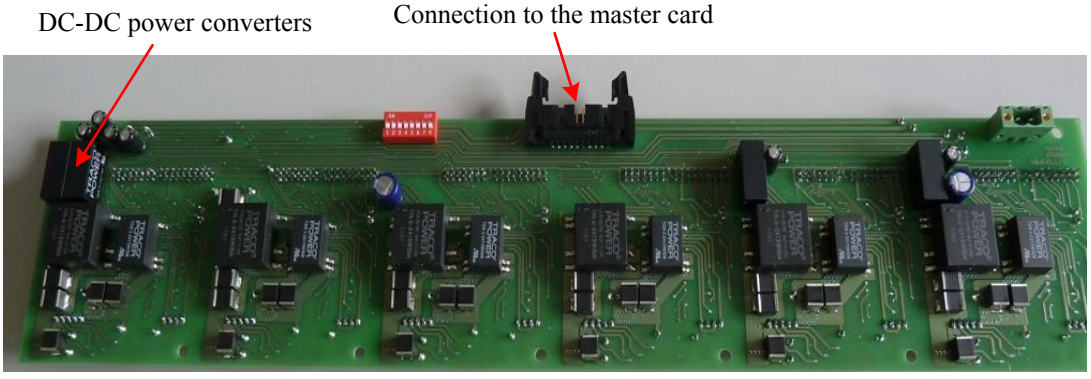


Fig. 5.2: Picture of the master card.

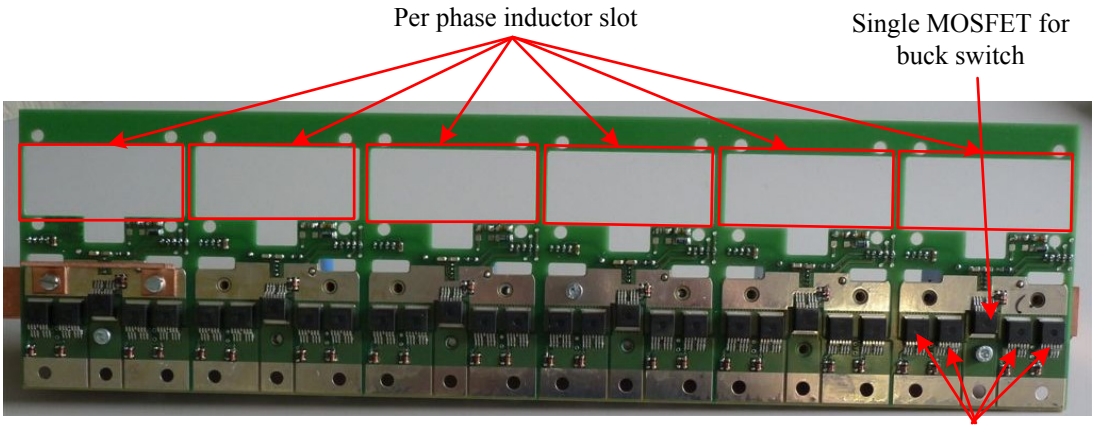


(a)

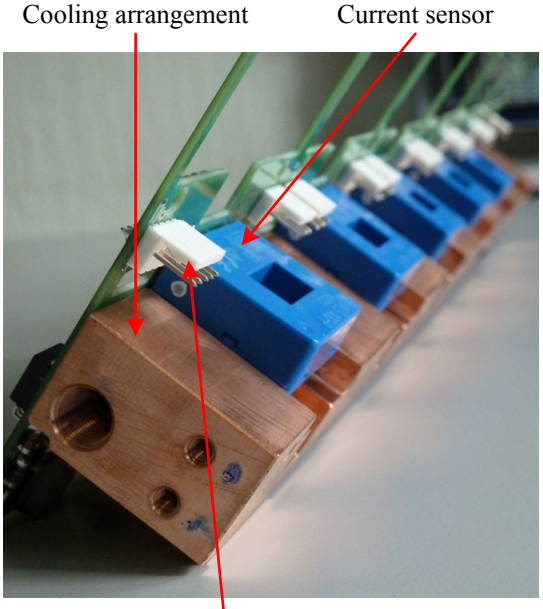


(b)

Fig. 5.3: Picture of the slave card (a) front view and (b) rear view.



(a)



(b)

Fig. 5.4: Picture of the power card (a) front view and (b) rear view.

The synchronously gated buck converter was made up of one IXFN360N10T MOSFET for the buck switch and four such MOSFETs in parallel for the synchronously gated freewheeling switch (refer Fig 5.4a). A DSA300I100NA Schottky diode was used in parallel to the synchronously gated freewheeling switches to avoid the conduction of the inverse diodes of these switches (MOSFETs) during the dead time. This improves the switching performance since the reverse recovery characteristics of a Schottky diode are far superior to that of the inverse diode of the synchronously gated MOSFETs.

It has to be noted that no snubber circuit was used across the semiconductor devices. This was mainly due to the fact that the size of the snubber circuitry becomes comparable to that of the actual power circuitry due to the magnitude of the currents switched. Instead, extreme care was taken in designing the layout, so that the stray inductances in the commutation mesh are minimised, in order to limit the over-voltage spikes across the MOSFETs during the switching transients. Further, the gate resistance was adjusted in order to make the switching transients as smooth as possible, without affecting the switching losses considerably.

5.2 Obtaining the worst case plant transfer function

Fig 5.5 shows a simple synchronous gating based buck converter without an output capacitor where V_{in} is the input voltage to the synchronously gated buck converter, S_{11} and S_{12} are respectively the main and synchronously gated MOSFET switches of the buck converter, L_{b} is the buck converter filter inductance, L_{load} denotes the inductance of the load and R_{load} denotes the load resistance.

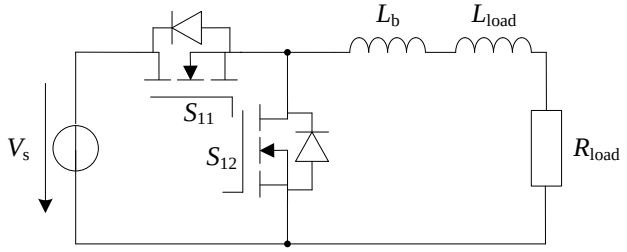


Fig. 5.5: Synchronously gated buck converter with load resistance and load inductance.

The dynamic model of the same buck converter is presented in Fig 5.6. This model is based on the assumption that the on-state voltage drop of the switch S_{11} is much smaller than the source voltage V_{s}. In the model, d denotes the variation in duty-cycle, r_{b} denotes the equivalent resistance of the buck converter and i_{L} is the dynamic average of the variation in the inductor current, as a result of variation in the duty-cycle.

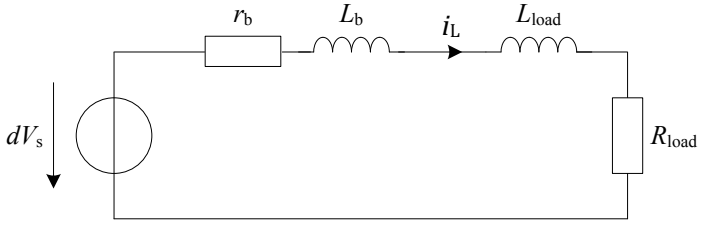


Fig. 5.6: Dynamic model of the synchronously gated buck converter with load resistance and load inductance.

The equivalent resistance r_b of the buck converter can be calculated as

$$r_\mathrm{b} = DR_{\mathrm{DS(on)},\mathrm{S}_{11}} + (1-D)R_{\mathrm{DS(on)},\mathrm{S}_{12}} + R_\mathrm{L} \tag{5.1}$$

where D is operating duty-cycle, $R_{\mathrm{DS(on)},\mathrm{S}_{11}}$ and $R_{\mathrm{DS(on)},\mathrm{S}_{12}}$ are the on-state resistance of the MOSFETs S_{11} and S_{12} respectively and R_L is the parasitic resistance of the inductor L_b. It is worth recalling that the switch S_{11} comprises of one MOSFET with $R_{\mathrm{DS(on)}}$ of 2.5 mΩ while the switch S_{12} comprises of four such MOSFETs in parallel, resulting in different effective resistances of the two branches. This is done because the RMS currents in switch S_{12} is bound to be much more than that through S_{11} due to low duty-cycle operation.

By utilising the model in Fig 5.6, the plant transfer function $T_\mathrm{p}(s)$ can be written as follows.

$$T_\mathrm{p}(s) = \frac{i_\mathrm{L}(s)}{d(s)} = \frac{V_\mathrm{s}}{r_\mathrm{b} + R_\mathrm{load} + s(L_\mathrm{b} + L_\mathrm{load})} \tag{5.2}$$

From the above two equations, it can be stated that the main parameters effecting the gain, bandwidth and the phase of the plant transfer function are the operating duty-cycle D, the load resistance R_load and series load inductance L_load. All other parameters being relatively constant.

The transfer function $T_\mathrm{p}(s)$ has the dimensions of A. Hence, for the purpose of generating Bode plots, one can introduce a transfer function $T'_\mathrm{p}(s)$ such that

$$T'_\mathrm{p}(s) = \frac{T_\mathrm{p}}{1\,\mathrm{A}} \tag{5.3}$$

The only difference between $T_\mathrm{p}(s)$ and $T'_\mathrm{p}(s)$ is that the former has the dimensions of A where as the later is dimensionless.

5.2.1 Effect of operating duty-cycle

In the transfer function $T_\mathrm{p}(s)$ the influence of D is not seen directly but it influences the the transfer function indirectly by effecting the equivalent resistance of the synchronously gated buck converter r_b (as shown in the Equation 5.1). Neglecting the parasitic resistance R_L of the inductor L_b, the effect of D on the plant transfer function $T_\mathrm{p}(s)$ is shown in Fig 5.7, in the form of Bode plots of $T'_\mathrm{p}(s)$. Table 5.1 shows the parameter values used to generate this Bode plot.

Table 5.1: Parameter values used to study the effect of duty-cycle D on the plant transfer function.

Parameter	Value
V_s	35 V
$R_{DS(on)}$	2.5 mΩ
R_{load}	2.0 mΩ
L_b	2.0 µH
L_{load}	0.125 mH

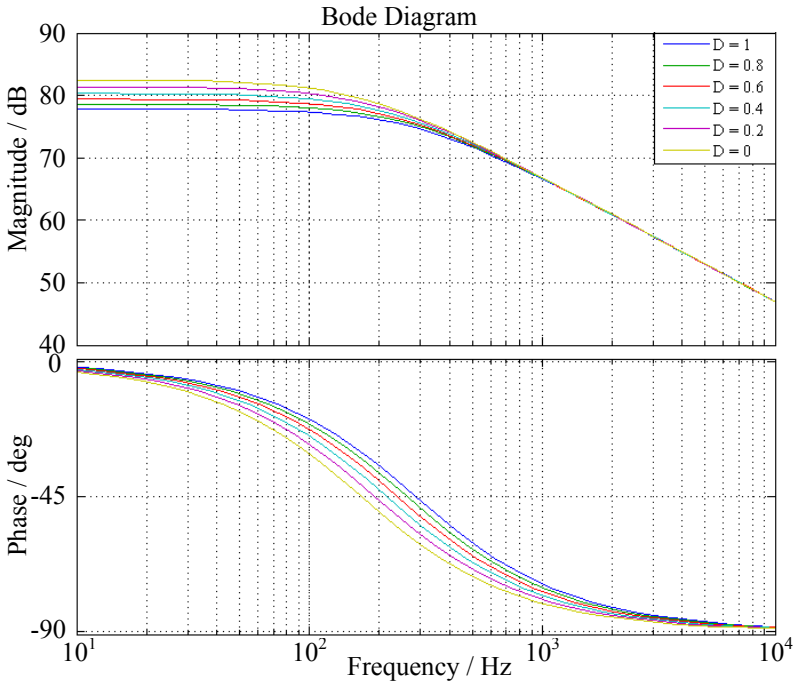


Fig. 5.7: Bode plots of $T_p'(s)$ for different values of D.

From Fig 5.7, it is clear that, as the duty-cycle D increases from 0 to 1 the gain of the plant transfer function $T_p(s)$ reduces. This is because of the increase in r_b. Maximum gain of the transfer function $T_p(s)$ is obtained when duty-cycle D is zero, which corresponds to a value of r_b equal to 0.625mΩ (for the hardware under consideration). Further, one has to note that the pole of the transfer function shifts to the lowest frequency when D is zero.

5.2.2 Effect of load resistance

The load resistance R_{load} should also be considered as a variable, in order to realise a robust design. Fig 5.8 shows the Bode plot of $T_p'(s)$ for different values of R_{load}. The values of the variables used for generating the plot are shown in Table 5.2.

An increase in the load resistance R_{load} results in a decrease in the gain of the transfer function $T_{\text{p}}(s)$ and a shift in the pole location towards a higher frequency. Thus, the worst case corresponds to a load resistance equal to zero, which corresponds to the outermost gain plot and innermost phase plot in Fig 5.8.

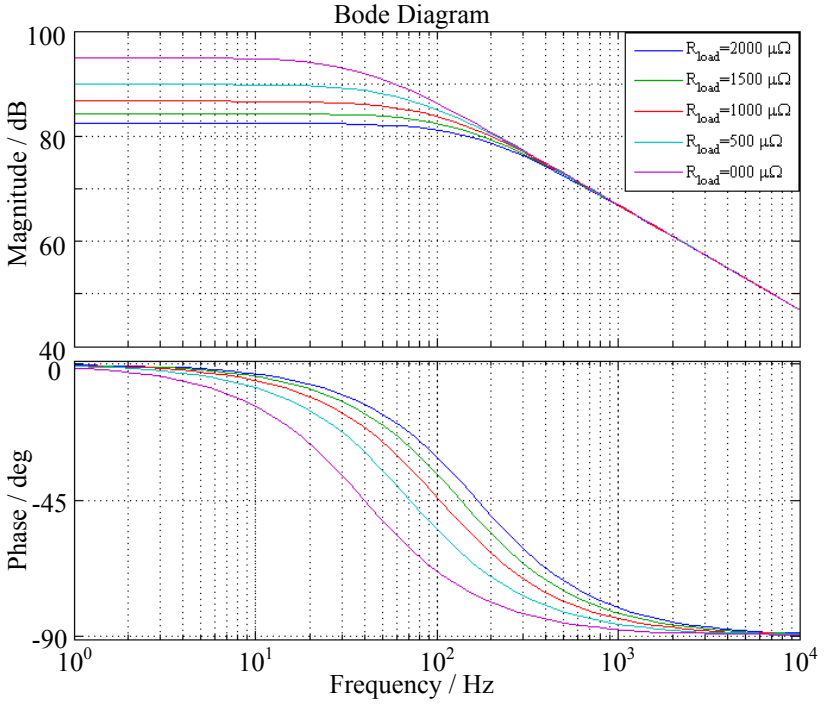


Fig. 5.8: Bode plots of $T'_{\text{p}}(s)$ by varying load resistance R_{load}.

Table 5.2: Parameter values used for studying the effect of load resistance R_{load} on plant transfer function.

Parameter	Value
V_{s}	35 V
$R_{\text{DS(on)}}$	2.5 mΩ
L_{b}	2.0 µH
D	0
L_{load}	0.125 mH

5.2.3 Effect of load inductance

The load inductance is dependent on the layout and the length of the cable between the power supply and the welding contacts (welding tong). This in turn influences the gain, bandwidth and the phase of the plant transfer function $T_{\text{p}}(s)$. Fig 5.9 shows the Bode plots of $T'_{\text{p}}(s)$ for various values of the load inductance L_{load}. The parameter values used for generating the plot are shown in Table 5.3. It has to be noted that the expected

variation of L_{load} used for the analysis is between 0 and 0.5 µH, which is much smaller than the inductance value of L_{b}. Therefore, a large variation is not observed between different plots. However, the bandwidth of transfer function is maximum when L_{load} is minimum. Further, there is no significant shift in the pole frequency with a change in the value of L_{load} (within the expected variation range of L_{load}). Thus, worst case transfer function corresponds to the case of L_{load} equal zero.

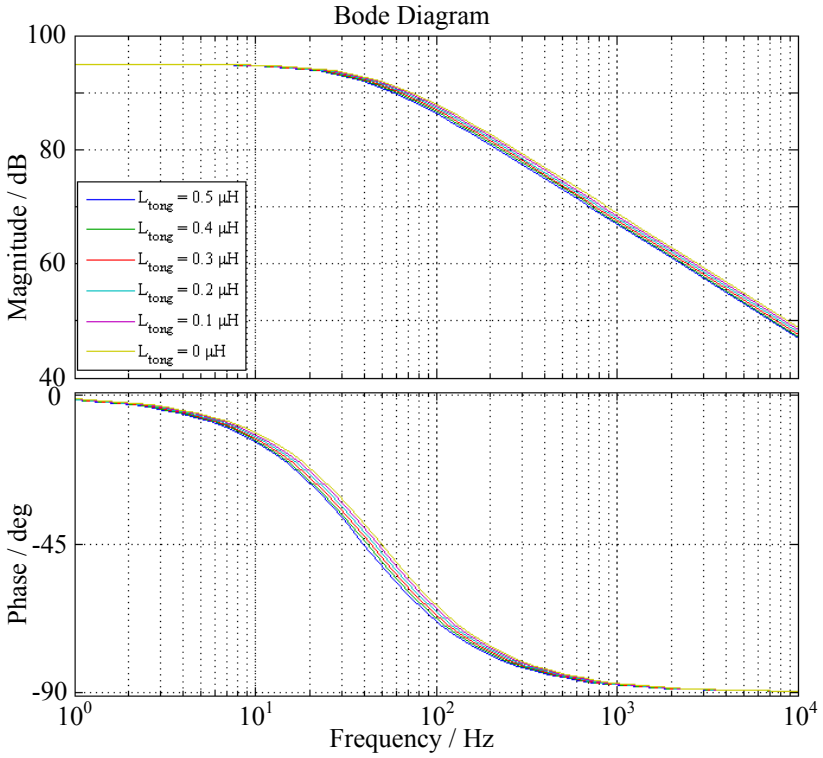


Fig. 5.9: Bode plots of $T'_{\text{p}}(s)$ by varying load inductance L_{load}.

Table 5.3: Parameter values used to analyse the effect of load inductance L_{load} on the plant transfer function.

Parameter	Value
V_{s}	35 V
$R_{\text{DS(on)}}$	2.5 mΩ
L_{b}	2.0 µH
D	0
R_{load}	0 mΩ

5.2.4 Worst case plant transfer function

Table 5.4 shows the parameter values which result in a worst case plant transfer function. The resulting worst case transfer function is represented by the Equation 5.4.

$$T_{\mathrm{p,worst\,case}}(s) = \frac{V_{\mathrm{s}}}{r_{\mathrm{b}} + sL_{\mathrm{b}}} \tag{5.4}$$

For the purpose of generating the Bode plot, the following normalised form of the worst case transfer function is introduced.

$$T'_{\mathrm{p,worst\,case}}(s) = \frac{T_{\mathrm{p,worst\,case}}(s)}{1\,\mathrm{A}} \tag{5.5}$$

Bode plot of the normalised transfer function $T'_{\mathrm{p,worst\,case}}(s)$ is shown in the Fig 5.10.

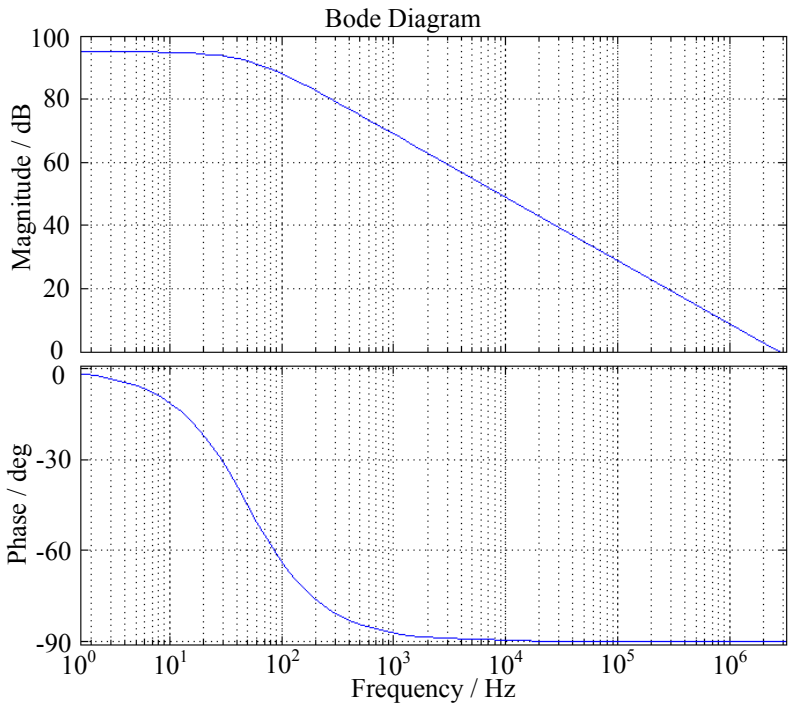


Fig. 5.10: Bode plot of transfer function $T'_{\mathrm{p,worst\,case}}(s)$ of synchronously gated buck converter.

Table 5.4: Parameter values corresponding to the worst case plant transfer function of synchronously gated buck converter.

Parameter	Value
V_{s}	35 V
$R_{\mathrm{DS(on)}}$	2.5 mΩ
L_{b}	2.0 µH
D	0
R_{load}	0 mΩ
L_{load}	0 µH

5.3 Influence of source resistance

The analysis upto this point was done under the assumption of ideal voltage source. However, DLC bank cannot be considered to be an ideal voltage source, especially when delivering currents close to and above its rating. Under these circumstances, the influence DLCs internal resistance cannot be neglected. This indeed can have a big influence on the system stability. The high-frequency characteristics of the DLC are not very important in this context since the high-frequency currents are usually supported by the input capacitors of the WPS.

Fig 5.11 represents the small signal dynamic equivalent model of a buck converter, when the voltage drop across the source resistance R_{s} is significant as compared to the source voltage. Equation 5.6 represents the corresponding linearised plant transfer function. This is obtained at an operating point corresponding to a combination of $D$and I_{L} and by neglecting the effect of the second and higher order differential terms. D and I_{L} denote the operating duty-cycle and the load current respectively, when a small perturbation in duty-cycle d is applied, which in turn produces a small variation in load current equal to i_{L} at steady state.

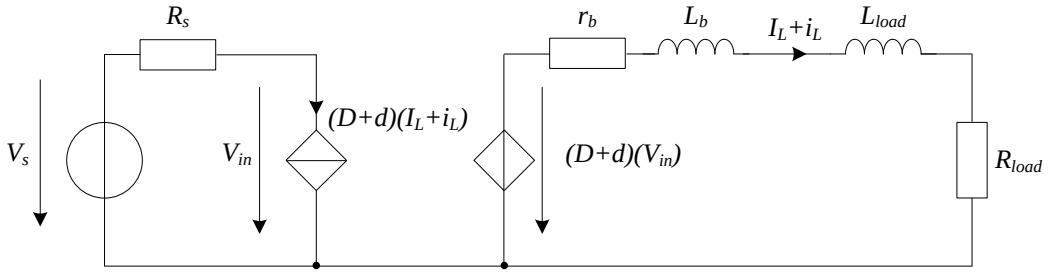


Fig. 5.11: Small signal dynamic model including the effect of source resistance.

$$[T_{\mathrm{p}}(s)]_{\mathrm{R_s}} = \frac{i_{\mathrm{L}}(s)}{d(s)} = \frac{V_{\mathrm{s}} - 2DR_{\mathrm{s}}I_{\mathrm{L}}}{R_{\mathrm{load}} + r_{\mathrm{b}} + s(L_{\mathrm{b}} + L_{\mathrm{load})} + D^2R_{\mathrm{s}}} \tag{5.6}$$

The worst case of the plant transfer function in Equation 5.6 when considering maximum gain and bandwidth, turns out to be

$$[T_{\mathrm{p,worst\,case}}(s)]_{\mathrm{R_s}} = \frac{V_{\mathrm{s}}}{r_{\mathrm{b}} + sL_{\mathrm{b}}} \tag{5.7}$$

which is the same as that in Equation 5.4, which is for the case without source resistance.

However, from the numerator of the right hand side of Equation 5.6, it is clear that, when the product $2DR_{\mathrm{s}}I_{\mathrm{L}}$ exceeds V_{s}, a negative phase shift of 180° is produced. This can have a significant influence on the system behaviour, when a closed-loop current control is employed. The physical meaning of this effect can be understood easily by using the steady state equivalent model of the synchronously gated buck converter with source resistance, as shown in Fig 5.12

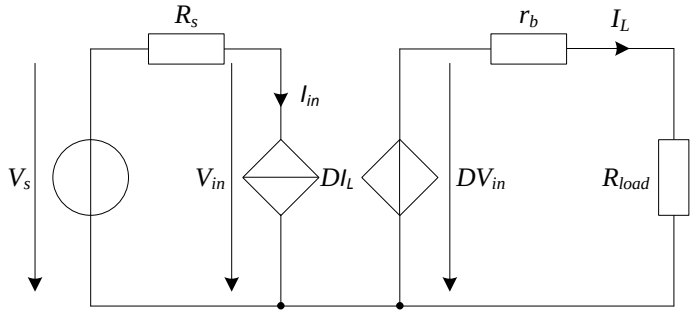


Fig. 5.12: DC model including the effect of source resistance.

by using the model shown in Fig 5.12, the equation for the steady state load current I_{L} can be written as,

$$I_{\mathrm{L}} = \frac{DV_{\mathrm{s}}}{R_{\mathrm{load}} + r_{\mathrm{b}} + D^2R_{\mathrm{s}}} \tag{5.8}$$

In case of buck converter with ideal source, the relation simplifies to

$$I_{\mathrm{L}} = \frac{DV_{\mathrm{s}}}{R_{\mathrm{load}} + r_{\mathrm{b}}} \tag{5.9}$$

Graphical representation of Equations 5.8 & 5.9 is shown in Fig 5.13. The figure corresponds to a source voltage of 35 V, load resistance of 4 mΩ and r_{b} of 0 Ω. Unlike the ideal voltage source case, the curve corresponding to a source resistance of 25 mΩ is non-linear.

The response shown in Fig 5.13 for buck converter with a finite source resistance can also be understood by applying the maximum power transfer theorem (refer to Equation

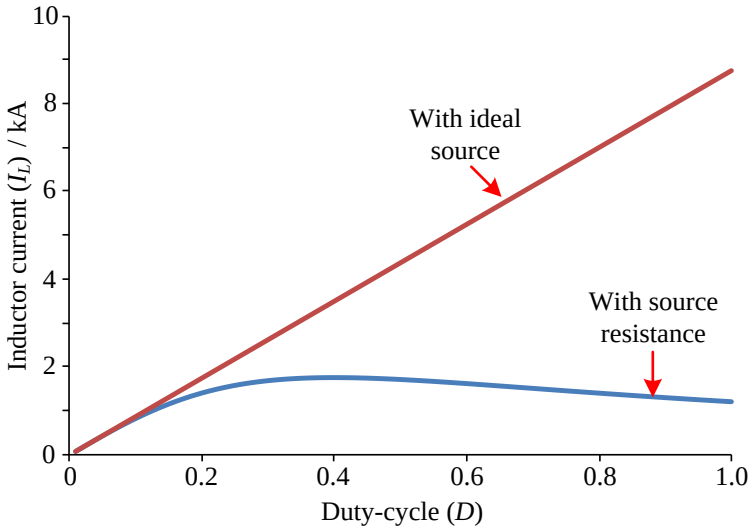


Fig. 5.13: Current response I_{L} with respect to duty-cycle D.

4.8). This non-linearity introduced due to source resistance can drastically influence the control performance, if the issue is not addressed appropriately in the control design.

5.3.1 Control issues due to source resistance

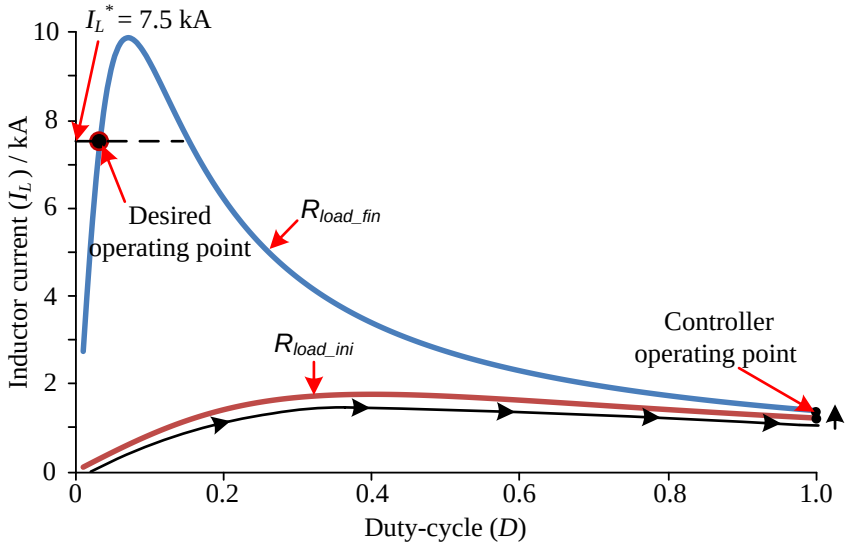


Fig. 5.14: Control problem when considering source resistance.

Consider a case where the load resistance dynamically changes from an initial value of $R_{\mathrm{load\_ini}}$ to a final value of $R_{\mathrm{load\_fin}}$ Fig 5.14 shows the steady state inductor current responses with respect to duty-cycle for $R_{\mathrm{load\_ini}}$ and $R_{\mathrm{load\_fin}}$ of 4 mΩ and 100 µΩ respectively, when the source resistance is 25 mΩ.

Let us assume a reference current I_{L}^{*} of 7.5 kA. In the beginning, due to high initial load resistance $R_{\mathrm{load\_ini}}$, the controller traces the curve in brown (Fig 5.14). In the aim of reaching the desired operating point, the controller operates at maximum duty-cycle of one. Now when the load resistance slowly changes to $R_{\mathrm{load\_fin}}$, the operating point shifts to the curve in blue. However, the system cannot reach the desired operating point because the controller tries to increase the duty-cycle whereas, it requires a reduction in duty-cycle to achieve the desired 7.5 kA. Such a problem can be surely expected in resistance spot welding applications, where the load resistance can dynamically vary during the welding.

It is not just the dynamic nature of the load that can take the operating point into the unstable region (negative slope region in Fig 5.14). There is also a possibility that high controller gains can push the operating point into this region during transients.

In order to restrict the operating point to the stable region under all circumstances, different solutions can be thought of, three of which (easily implementable) are listed below.

1. Limiting the duty-cycle based on the measured load current I_{L}
2. Limiting the duty-cycle based on measured input voltage V_{in}
3. Limiting the duty-cycle based on current reference I_{L}^{*}

In the first solution, the duty-cycle is limited so that the product $DR_{\mathrm{s}}I_{\mathrm{L}}$ is not allowed to go above one half of the internal source voltage V_{s}. This technique is very hard to implement if the solution is modular, where the current sensors are distributed. Further, it also requires the information of the source resistance, which can vary with ageing.

In the second solution, the terminal voltage of source is not allowed to go below one half of the internal source voltage(approximately), by adjusting the current reference. This solution does not require the information of the source resistance. But it requires an additional controller to be implemented.

The third solution is similar to the first solution. Here the duty-cycle is limited, so that the product $DR_{\mathrm{s}}I_{\mathrm{L}}^{*}$ is not allowed to go above one half of the internal source voltage V_{s}. Though, such a control is less complex to implement, it might suffer from the disadvantage of not meeting the higher voltage (approximately 20 V) needs of the welding load, during the initial phase of the welding. However, this solution was adapted for prototype testing since, testing was performed on fresh metal sheets (without any significant thickness of oxide layer). It is advisable to implement a different solution in the future, in order to address the initial higher output voltage requirement.

One has to consider the point that, when n number of converters are operating in parallel, then the limit on the duty-cycle can be written as

$$D \leq \frac{V_\mathrm{s}}{2nI_\mathrm{L}^* R_\mathrm{s}} \tag{5.10}$$

Further, when using a DLC based storage, the value of V_s in the above equation should correspond to the expected internal voltage of the DLC bank, at the end of the welding duration.

5.4 Controller design

The objective of the controller is to track the reference current and to give a decent dynamic performance. Thus, the open-loop transfer function needs to have a very high DC gain and a high enough bandwidth. Most important issue is that the controller has to be designed, for the system to be stable with the worst case plant transfer function. Thus, stability is guaranteed under all other operating conditions (robust control). A PI controller was deemed to be suitable and hence selected, in order to meet the above mentioned control objectives. A proportional gain K_p of $0.0004\,\mathrm{A}^{-1}$ and an integral gain K_i of $1.2\,\mathrm{A}^{-1}\,\mathrm{s}^{-1}$ was selected, so that the desired objective is achieved. The question of optimal controller design using the concepts of magnitude optimum etc does not arise since the load resistance is variable. Bode plot of the open-loop transfer function including the current controller and the worst case transfer function, is shown in Fig 5.15. The parameter values utilised for generating the plot are presented in Table 5.5. The corresponding Bode plot of the closed-loop transfer function and the step-response plot are shown in Fig 5.16 and Fig 5.17 respectively. One can see that, for the worst case plant transfer function under consideration, the control bandwidth is about 1 kHz and the phase margin is about 60°. The controller was digitised and implemented in the micro-controllers on the slave cards.

Table 5.5: Values of parameters used for obtaining the frequency response of the system, including the controller.

Parameter	**Value**
V_s	35 V
$R_\mathrm{DS(on)}$	2.5 mΩ
L_b	2.0 µH
D	0
R_load	0 mΩ
L_load	0 µH
K_p	$0.0004\ \mathrm{A}^{-1}$
K_i	$1.2\ \mathrm{A}^{-1}\,\mathrm{s}^{-1}$

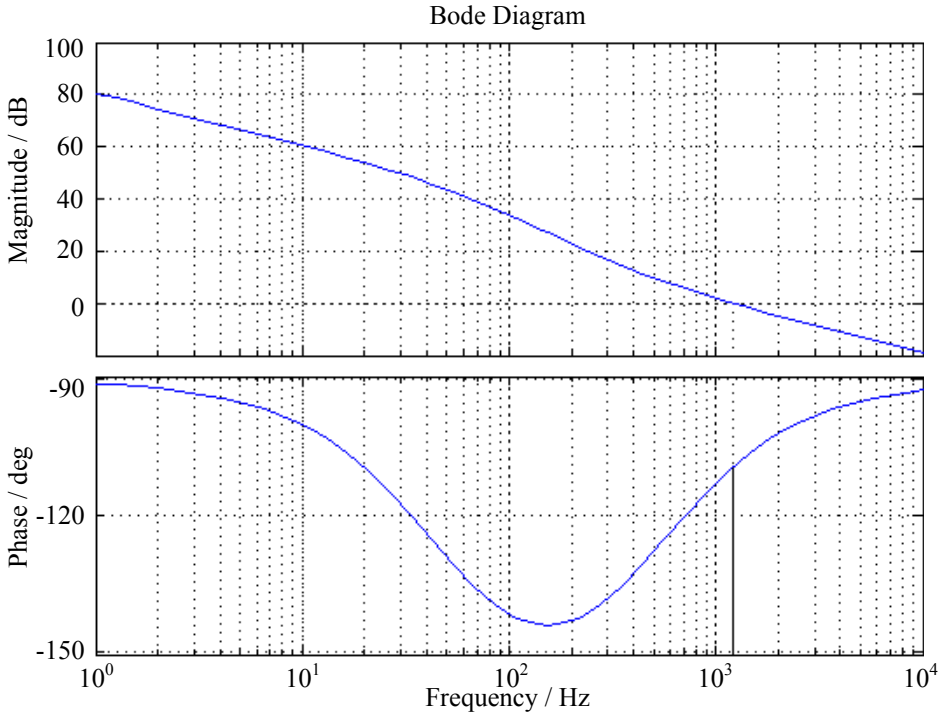


Fig. 5.15: Open-loop response of the system including the controller and the normalised worst case plant transfer function.

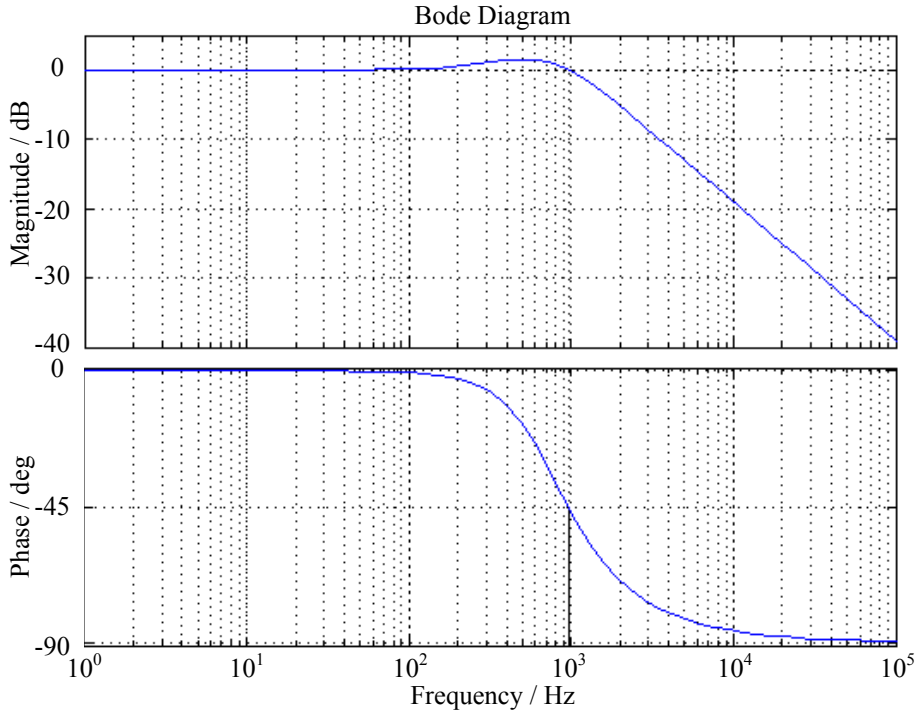


Fig. 5.16: Closed-loop system response including the controller and the normalised worst case plant transfer function.

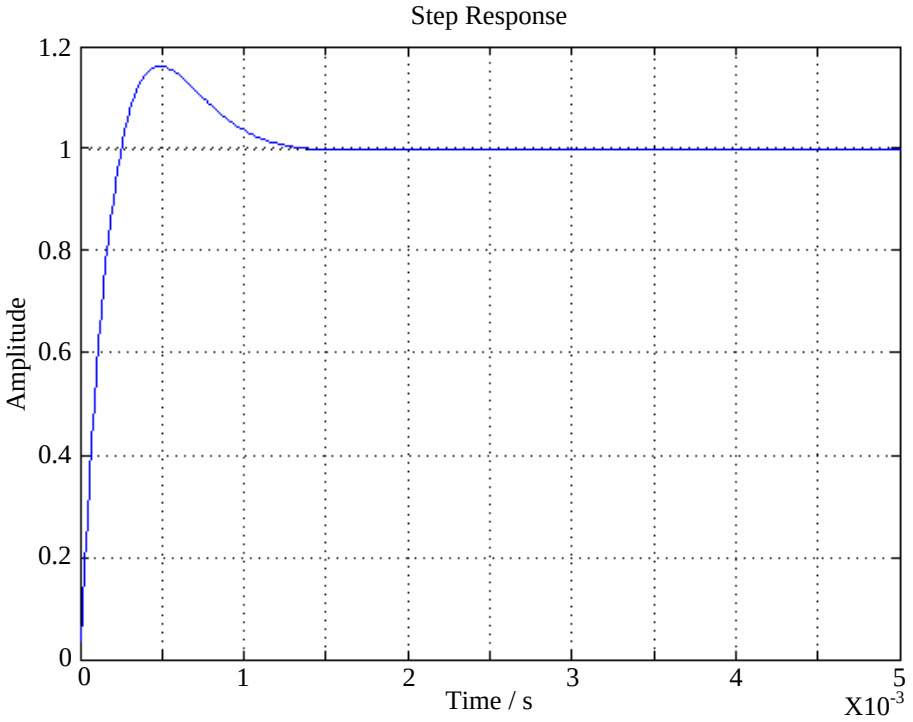


Fig. 5.17: Step-response for closed-loop system including the controller and the normalised worst case plant transfer function.

5.5 Experimental Setup

Fig 5.18 shows a picture of the experimental setup which includes a Programmable Logic Controller (PLC) system, a 100 F-50 V DLC bank (energy storage capacity equal to 125 kJ), the welding power supply prototype, metal sheets that need to be welded and a magnetic drive for generating the required force at the welding points on the metal sheets.

The PLC system interacts with the master card, which in turn appropriately communicates with the slave cards. Further, the PLC system also controls a charger circuit which is responsible for charging the DLC bank.

The welding power supply prototype consists of five power cards in parallel, each of which is capable of producing a current of 1.5 kA. Each power card comprises of six interleaved phases, each of which can produce 250 A.

Each slave card has six micro-controllers (TMS320F28027), each of which is dedicated to an individual phase of the IBC (refer Fig 5.4a). Embedded software for these controllers was developed, which incorporates the control algorithm, feedback sensing and conditioning, over current protection, phase shifting and other necessary components. The slave card also includes the signal isolator, gate driver and fault sensing circuits.

Experiments were performed on 0.7 mm iron sheets and the quality of the welds was tested by means of peel off tests. Peel off test is a process in which the welded metal sheets are forcefully pealed off and if it results in a hole on one of the metal sheets (at the weld site), the weld is considered to be of good quality. It requires approximately 5 kA for 100 ms to weld 2 iron sheets of thickness 0.7 mm (information source: NIMAK GmbH).

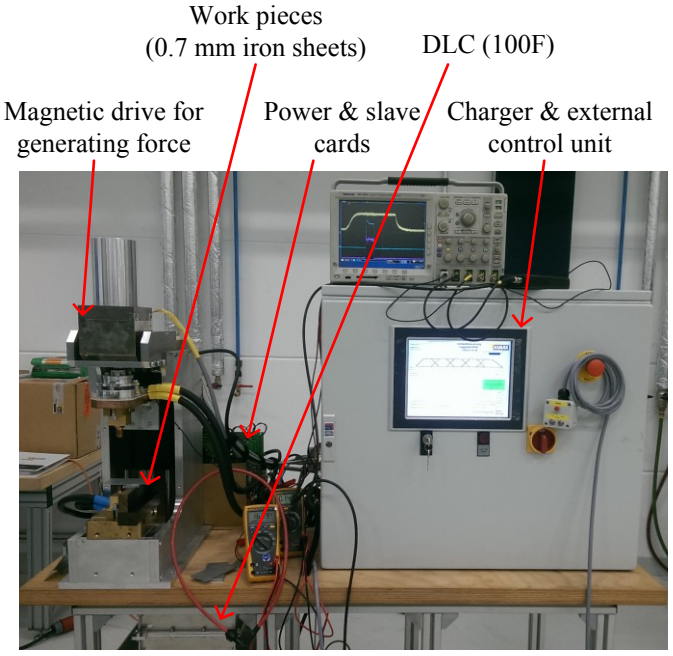


Fig. 5.18: Experimental setup of the DLC based RSW power supply prototype.

5.6 Results

In order to observe the system performance and test the correctness of the designed hardware and software, the input and output current of the welding power supply, together with the output voltage response of the system were measured. The power supply input current (DLC output current) was measured using a DC current sensor while, the output load current was measured using a Rogowski coil (Rogowski coil can be used because of the short duration of the current pulse). The load voltage was measured across the tips of the electrodes by using a RC filter as shown in Fig 5.19. A snapshot of measured DLC current, load current and load voltage is shown in Fig 5.20. Table 5.6 presents the parameter values corresponding to the results shown in Fig 5.20.

In Fig 5.20, one can clearly observe a small spike in the output voltage at the beginning of the welding duration, which can be attributed to a thin oxide layer on the metal

sheets. Further, the output current of 5 kA and an input current of approximately 350 A corresponds to an operational duty-cycle of approximately 0.07.

It can be noted that the step-response obtained in Fig 5.20 is different to that in Fig 5.17. The response in Fig 5.17 is a small signal response of a single buck converter under absolute short circuit conditions while the response in Fig 5.20 is a large signal response of 30 converters with individual current control, operating in parallel and driving a single load. One also needs to consider the effect of dynamically varying load resistance during the current build-up phase. Further, since it is an experimental setup which is not fully optimized with respect to mechanical design, there exists a significant load inductance due to long cables between the converter and the work pieces. Hence, one has to also account for this cable inductance and resistance. Some of the other factors which influence the response are the current sensor bandwidth ($\approx$ 50 kHz), the bandwidth of the RC filter($\approx$ 1 MHz) in the sensing loop, additional delay associated with digital implementation, the source resistance (DLC internal resistance), the impedance between the DLC module and the welding power supply etc.

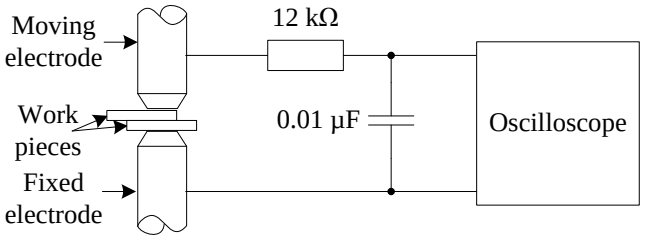


Fig. 5.19: Load voltage measuring circuit.

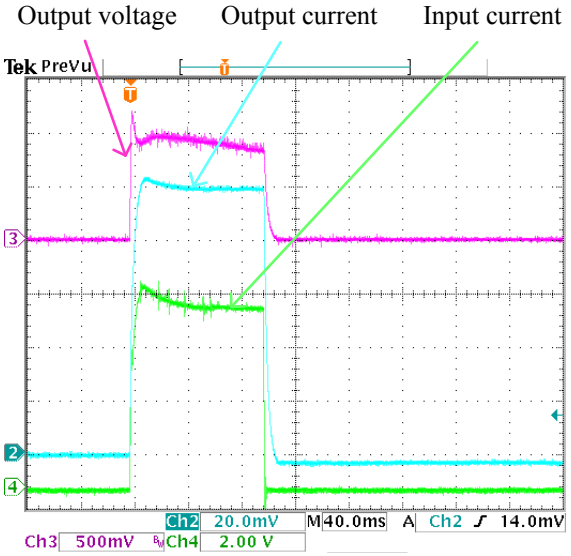


Fig. 5.20: Snapshot of power supply input current, load current and load voltage. Iutput current: 1 V represents 50 A, load current: 20 mV represents 1 kA.

Table 5.6: Parameter values used, corresponding to the results shown in Fig 5.20.

Parameter	**Value**
DLC voltage V_s (fully charged)	35 V
Internal source resistance R_s	7 mΩ
Operating Frequqency	50 kHz
Per phase inductance L_b	2 µH
Integral gain K_i (analog)	1.2 A^{-1} s^{-1}
Proportional gain K_p(analog)	0.0004 A^{-1}
Per phase current reference i_{ref}	≈ 170 A
Total current reference	5 kA
limit on D	0.4

A snapshot of the turn off voltage spike across drain-source of the buck MOSFET (switch S_{11} in Fig 5.5), when switching approximately 270 A is shown in Fig 5.21. The measurement was performed at an input voltage of 20 V and with a gate resistance of 10 Ω. The results show that the voltage spike is well within limits, thus will not cause any reliability issues.

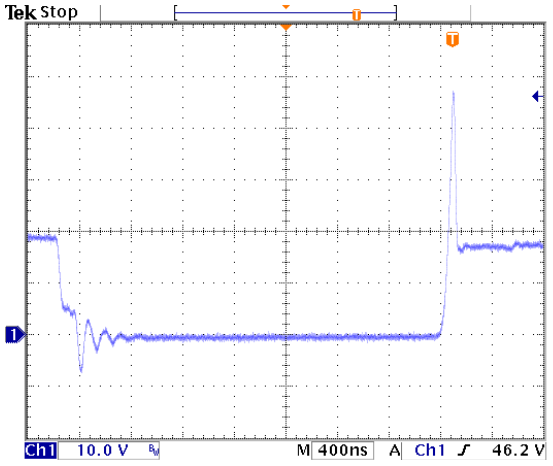


Fig. 5.21: Snapshot of the turn-off voltage spike across drain-source of the buck MOSFET. Switching current: 270 A, input voltage: 20 V

Fig 5.22a shows a photograph of the welded samples. The result of the peel-off test is shown in Fig 5.22b.

(a) (b)

Fig. 5.22: (a) Welded iron metal sheets (0.7 mm each) with 5 kA for 100 ms. (b) Hole made when the welded sample is peeled off.

Chapter 6

Conclusions and Future Work

6.1 Energy storage

As it was stated at the beginning of the thesis, Capacitor Discharge Welding (CDW) is characterised by extremely high welding currents coupled with extremely low welding times (higher than 100 kA and smaller than 10 ms respectively). Though such a characteristic is beneficial in resistance spot welding, in most of the cases, a current of less than 20 kA and welding times in the order of hundreds of ms (but smaller than 500 ms) is sufficient. Opting for a reduced welding current (as compared to CDW) can be highly beneficial in terms of the storage system volume and its cost. This is because the idea of controlled discharge of energy makes it possible to utilise ECS, DLCS and FSS as an option. Indeed, the use of any one of these three storage options, results in a many-fold decrease in the volume of a SBRSWPS as compared to CDW based systems.

Further, when a comparision is made between ECS, DLCS and FSS for a SBRSWPS application, in terms of the right compromise between volume and efficiency,

- the DLC solution performs better than the ECS, while the FSS solution fares better than the DLC solution.
- for a given efficiency, the FSS based solution is approximately 5-10 times more compact than the DLC solution (depending on the rated speed).
- liquid cooled motor based solutions outperform the air cooled solutions in terms of both efficiency and size.
- steel seems to be the best material to realise the flywheel for SBRSWPS under consideration.

. Additional benefits offered by FSS are,

- flywheel is a greener solution, since almost all the components in motor and flywheel are fully recyclable.
- the depreciation of investment can be negative when considering the price rise of permanent magnets and metals.
- higher efficiency as compared to DLC storage.
- proven reliability.
- easier cooling, due to higher temperature difference between coolant and the motor internal temperature.

However, every coin has two faces and similarly the FSS solution also has its own drawbacks. The main drawbacks being the concerns of safety and the dependence of efficiency on the time gap between welding instances. However, safety issues can be considered to be more of a mental blockage of the designers and customers, since containment enclosures can easily be developed, as the energy stored is not too high (smaller than 350 kJ). An additional drawback of FSS is the need for an extra power converter to convert the stored energy into an usable form (AC to DC voltage converter). Further, the benefits offered by the flywheel storage clearly overshadow its drawbacks and hence, it can be expected that, a proper change management process can put the FSS as a viable option for future SBRSW applications.

6.2 Power supply topology

The concept of controlled discharge also influences the choice of the power electronic topology. Though the conventional 1 kHz converter topology (State of the art for non-storage-based solution shown in Fig 1.1) can be applied, it suffers in terms of audible noise, high current raise times and low bandwidth. An evaluation of high-frequency-modular solutions shows that "Inter-Cell Transformer Based Buck" and the "Interleaved Buck" topologies perform the best in terms of efficiency, cost and volume. However, it requires that the storage system output is at low voltage (approximately smaller than 50 V). When considering isolated solutions, the "Buck Controlled Resonant" topology can be beneficial in reducing the weight on the welding robot (please refer Chapter 3).

A scaled down version of the required SBRSWPS was developed as a proof of the concept. This seems to be the smallest of its kind ever reported in literature. The developed prototype was tested on 0.7 mm thick iron sheets and good quality welds were obtained.

6.3 Future work

It was mentioned in Chapter 4 that the analysis performed for obtaining efficiency figures for a flywheel storage system, did not consider the core losses in the stator teeth. This has been identified as a major gray area which needs to be addressed as part of the future work. Nevertheless, flywheel storage seems to be a promising option for future resistive spot welding applications. Implementation of such a system indeed involves a lot of multidisciplinary engineering expertise and hence can be taken up as future work.

Use of "Inter-cell transformer" based buck solution can result in a more compact system and hence research needs to be focused in this direction. Use of transient voltage suppressor diodes across the MOSFETS to decrease the switching voltage spike can help in reducing the voltage rating of the MOSFETS used. This in-turn has an effect of reducing the conduction losses and thereby increasing the converter efficiency. Research can be carried out to check the viability and the quantitative benefits of such a solution for the application under consideration. Further, the system performance when welding metal sheets with considerable thickness of oxide layer has to be tested. Hence, such tests have to be performed and if required, the control needs to be appropriately modified. Development of a model based control scheme, taking important system parameters into consideration can also be a potential topic of further research.

Appendix A

Appendix A

A.1 Estimation of magnetics size

This appendix presents the assumptions made and to an extent, also the procedure utilised to make an estimate of the magnetic (inductors and transformers) volumes for the power electronic topologies under consideration. Basic equations on magnetics design from [51] were utilised for the purpose, which can be referred, in order to get a more detailed understanding of magnetic design. It has to be noted that only a normalised comparison of magnetic volume for various topologies is possible. It is almost impossible to give an absolute estimate of magnetic volume for any given topology, due to the fact that power loss density is a design variable.

A.1.1 Assumptions used in estimating the volume of the magnetics

The following assumptions were made in order to facilitate the theoretical calculation of inductor and transformer sizes.

1. Window utilization factor K_{win} of 0.5 for inductor with DC offset and equal to 0.2 for resonant inductors and transformers. This is because, for transformers and resonant inductors, it is assumed that litz wire is used, to accommodate for the larger amplitude of the high-frequency current components.
2. It is assumed that switching frequency is 50 kHz.
3. Ferrite core with a saturation flux density equal to 0.5 T is assumed as core materiel. The maximum peak to peak variation in flux density at the switching frequency of 50 kHz is assumed as 0.25 T.

4. Inductance of parasitic welding tong is assumed to be 500 nH.

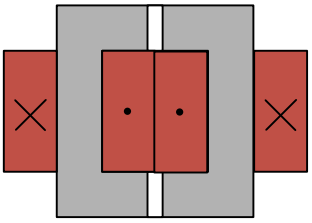
5. At test conditions, an output voltage equal to 3 V and an input voltage of 30 V, a peak to peak ripple current of 50 A per phase is taken as a baseline for determining the required per phase inductance values for IBC and the magnetizing inductance per phase, in case of ICTBC. Also, maximum output voltage required is fixed to 20 V (This which will be used as an input for selecting transformer secondary voltage in PSFB and buck controlled resonant topology)

6. Copper is assumed to be the conductor material and losses are calculated at a temperature of 20 °C.

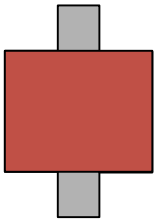
7. For ICT based buck, it is assumed that a current unbalance of 150 A may exist due to control transients and sensing inaccuracies.

8. Fig A.1a and Fig A.1b shows the assumed geometrical shape of the inductor which is used for the analysis while Fig A.2a and Fig A.2b shows the assumed shape of the transformer. The assumed shape of ICT is shown in Fig A.3a and Fig A.3b.

9. It is assumed that magnetic cores are available with any specified dimensions.



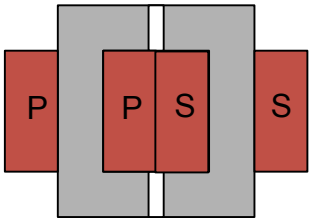
(a)



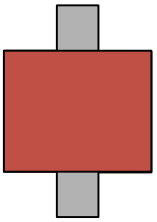
(b)

Fig. A.1: The assumed geometry of the inductor which is used for the analysis (a) front view and (b) side view.

The inductance values required per phase, in order to meet the ripple criteria mentioned previously are tabulated in Table A.1.The specifications of the transformers used in a PSFB or the buck controlled resonant topology are given in Table A.2.

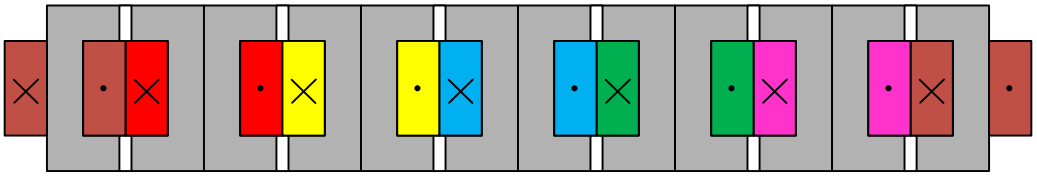


(a)

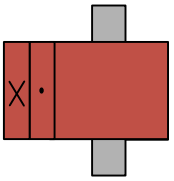


(b)

Fig. A.2: The assumed geometry of the transformer which is used for the analysis (a) front view and (b) side view.



(a)



(b)

Fig. A.3: The assumed geometrical shape of ICT, used for the analysis (a) front view and (b) side view.

A.1.2 Magnetics size estimation

Fig A.4a and Fig A.4b show the theoretical design graphs of the inductor for an interleaved buck converter (1 µH/400 A). One can see that the smallest volume can be achieved for the highest number of turns and highest current density. While the primary objective is smallest volume, one needs to also look at the power losses that are produced. A suitable choice has to be made, so that

1. The cooling is manageable (i.e. power loss density is manageable) and
2. The efficiency of the converter is not greatly affected.

Table A.1: Inductance values per each phase with different topologies

Topology	Inductance necessary and peak current rating
Interleaved buck	1.08 µH/400 A
PSFB	1.02 µH/400 A
ICT buck:Magnetizing inductance per ICT phase	0.6 µH(with 150 A unbalance currents)
External inductance per phase(similar to leakage inductance) in case of ICTBC	0.1 µH/400 A

Table A.2: Specifications of the transformers used in a PSFB or the buck controlled resonant topology

Parameter	Specification
Maximum input voltage	400 V
Maximum output voltage	20 V
Primary configuration	Single winding
Secondary configuration	Centre - tapped
Air gap length	No air gap
Average current per secondary winding	165 A
Switching frequency	50 kHz

A choice has to be made on the above two items, in order to get an exact estimate of the magnetic size. This choice is purely design specific issue (to an extent, choice also depends on cooling technology used). This makes an absolute magnetic volume estimation an almost impossible task. However, a normalised comparison of magnetic volume across different topologies is possible, by appropriately selecting the above two parameters.

In Fig A.4 the volume and corresponding losses for different designs which gives approximately the same volumetric loss densities have been highlighted (for 1 µH and 400 A inductor). The best choice among them is the design which gives the smallest volume (and smallest losses, since loss density is approximately constant). From Fig A.4, the best choice among the highlighted design options would be the one with power losses of approximately 135 W (during welding), volume of 0.05 l, with number of turns N equal to 3 and current density equal to 2.5 A/mm^2. From Fig A.4 it can be seen that if one goes for a solution with more number of turns and higher current density, the losses increase, the volume reduces and the loss density increases. The opposite happens when one tries to implement the magnetic element with less number of turns and lower current density. Hence, it is not very difficult to find the zone with a constant loss density.

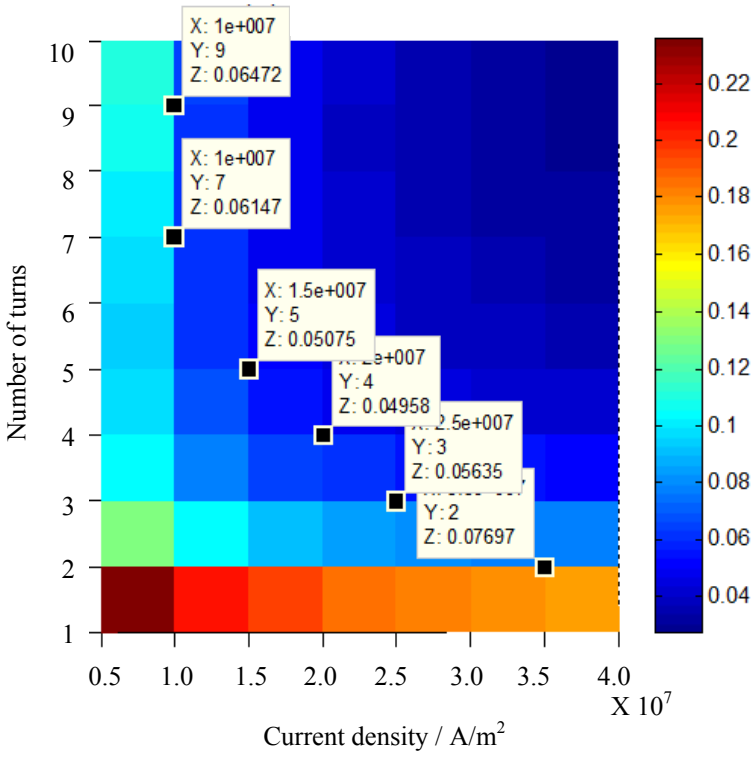
For the purpose of a normalised volume comparison, a selection of loss density has to be

made (since copper and core loss distribution is not very important in the application under consideration). It is however worth noting that, in a practical scenario, core sizes and wire cross-sections are discrete variables, instead of continuous variables.

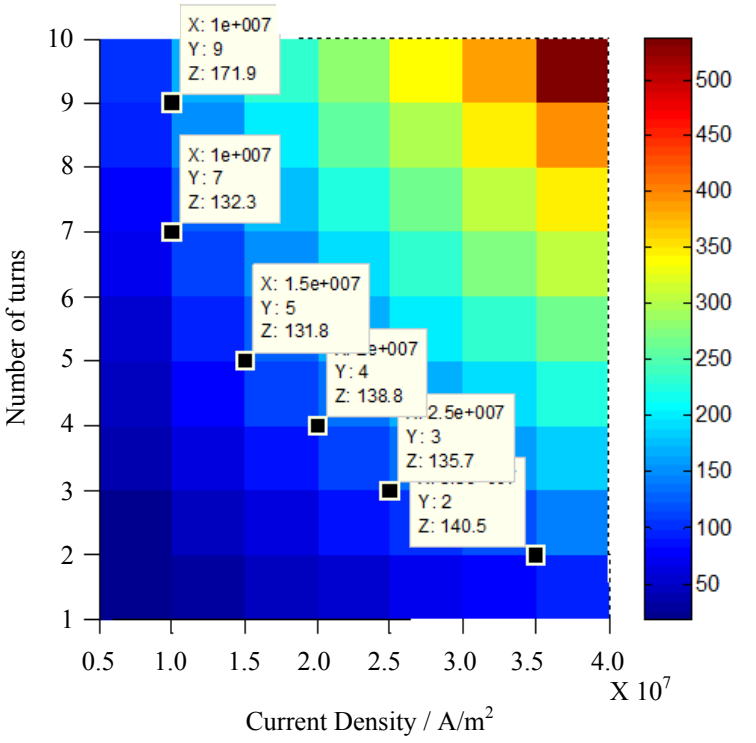
Similar analysis was performed on all magnetic components and the calculated volume of the magnetic components per 2 kA module (each module comprising of six interleaved phases), along with their theoretical power losses were obtained (for all four topologies considered). The results are tabulated in Table A.3. It is important to recollect that the absolute values presented in Table A.3 are not of much importance for the present analysis and our objective is to make a comparative analysis of magnetic volume between the topologies under consideration. Please note that, for the buck controlled resonant converter, the loss density selected of buck inductor is about half that of other inductors. This is because the buck part of the circuit can be placed away from the welding robot and hence can be designed for efficiency, rather than for size.

Table A.3: Calculated volume of the magnetic components for different topologies

Topology	Component	Volume in l/2 kA module	Details	Loss/surface-area (W/cm^2)
IBC	Inductor	0.05×6	Turns = 4 Current density = 20 A/mm^2	≈ 0.16
PSFB	Inductor	0.05×6	Turns = 4 Current density = 20 A/mm^2	≈ 0.15
PSFB	Transformer	0.056×6	Secondary turns = 3 Current density = 1.5 A/mm^2	≈ 0.16
BCR	Resonant inductor	0.004×6	Turns = 10 Current density = 40 A/mm^2	≈ 0.15
BCR	Transformer	0.056×6	Secondary turns = 3 Current density = 1.5 A/mm^2	≈ 0.16
BCR	Buck inductor (designed for efficiency)	0.075×6	Turns = 25 Current density = 30 A/mm^2	≈ 0.07
ICTBC	Inductor	0.006×6	Secondary turns =2 Current density = 20 A/mm^2	≈ 0.16
ICTBC	ICT	0.134	Secondary turns =3 Current density = 10 A/mm^2	≈ 0.17



(a)



(b)

Fig. A.4: (a) Calculated volume (in l) of the inductor for various current densities and number of turns and (b) corresponding power losses (in W) of the inductor of the interleaved buck converter.

Appendix B

Appendix B

B.1 Flywheel basics

Flywheels can be realised in different shapes like ring, flat disk, conical disk, etc. [76][85]. The most widely used being the flat disk or ring-shaped flywheels. It has been proved that, with respect to volumetric energy storage density, the flat disk shaped flywheels perform better than the ring-shaped flywheels [76]. Hence the flat disk shaped flywheel is chosen for the present analysis. All references to flywheel in this thesis refers to a flat disk shaped flywheel, unless otherwise specified.

Energy stored in a flywheel E_{fw} is given by the following equation.

$$E_{\mathrm{fw}} = \frac{1}{2} J \omega^2 \tag{B.1}$$

where J is the moment of inertia which depends on the geometry and mass of the flywheel and ω is the angular velocity of the flywheel. For a disk shaped flywheel made out of a homogeneous material,

$$J = \frac{1}{2} m_{\mathrm{fw}} r_{\mathrm{fw}}^2 \tag{B.2}$$

where m_{fw} is the mass of the flywheel and r_{fw} is the radius of the flywheel. From B.1 it is clear that, for a given flywheel, the energy stored can be increased by just increasing its angular velocity. The first question which arises is, to what extent can the angular velocity be increased?

Flywheel design has been dealt in detail in [76][85]. Utilising [76], it can be easily proved that, for a flat disk flywheel, if Ed_{fw} is the volumetric energy density, its maximum value $\max(Ed_{\mathrm{fw}})$ is a function of the tensile strength of the material σ_{m} and its Poissons ratio

γ (usually close to 0.33 for solids). It is important to note that Ed_{fw} is independent of the density of the material ρ_{m}. This is shown by the below equation where S_{f} is the safety factor (safety factor to accommodate the design, manufacturing and material imperfections).

$$\max(Ed_{\mathrm{fw}}) = \frac{2\sigma_{\mathrm{m}}}{S_{\mathrm{f}}(3+\gamma)} \tag{B.3}$$

$$\max(Ed_{\mathrm{fw}}) \approx 0.3\sigma_{\mathrm{m}}; \text{with } S_{\mathrm{f}} = 2 \tag{B.4}$$

Using the above equations, the achievable volumetric energy densities for flywheels, corresponding to some important materials is tabulated in Table B.1.

Table B.1: Theoretical volumetric energy density achievable with different flywheel materials using disk shaped geometry

Material	σ_{m} in N/m^2	ρ_{m} in kg/m^3	$\max(Ed_{\mathrm{fw}})$ in J/m^3
T-1000 Graphite	6.89×10^9	1799.194	2.07×10^9
T-700 Graphite	4.83×10^9	1799.194	1.45×10^9
Spectra 1000	3×10^9	968.7967	9.00×10^8
Technora T220	4.12×10^9	1383.995	1.24×10^9
Kevlar 49	3.62×10^9	1439.355	1.09×10^9
S2 Glass	4.14×10^9	2546.551	1.24×10^9
E Glass	3.1×10^9	2546.551	9.31×10^8
4340 steel	1.79×10^9	7833.413	5.38×10^8

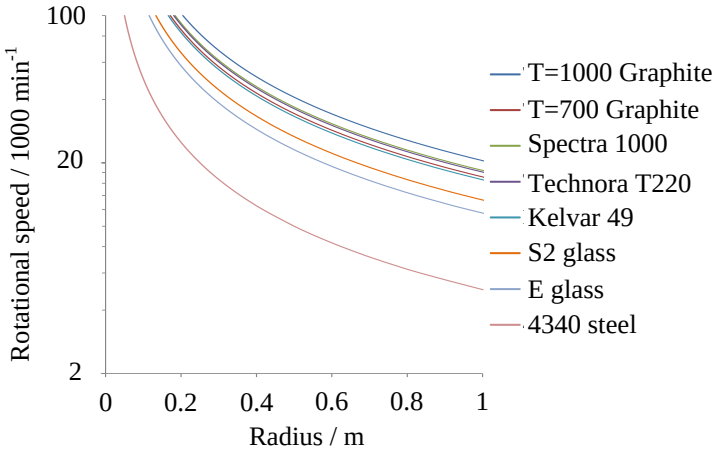


Fig. B.1: Flywheel radius versus maximum possible rotational speed for various materials.

The values of $\max(Ed_{\mathrm{fw}})$ shown in Table B.1 denote the theoretical maximum (with safety factor of 2) for a given material, when using disk shaped flywheels. For a given

material, a maximum rotational speed exists for each flywheel diameter, which corresponds to the value of $\max(Ed_{\text{fw}})$ mentioned in Table B.1. Fig B.1 shows the flywheel radius versus maximum possible rotational speed curves for various materials.

B.2 Motor type selection

Table B.2 summarises some of the the characteristics of different types of three phase AC motors, which are of interest when considering flywheel energy storage applications. A comparitive analysis between each motor type, with respect to each of the characteristic mentioned in Table B.2 is presented below. DC motors are not considered to be contenders for the application under consideration due to reliability reasons arising from brushes, their lower efficiency and due to their lower power density as compared to three phase AC motors.

Table B.2: Summary of characteristics of different types of motors. SPMSM: Surface Mount Permanent Magnet Synchronous Motor, IPMSM: Integrated Permanent Magnet Synchronous Motor, IM: Induction Motor (wound rotor or squirrel cage), SRM: Switch Reluctance Motor, SyRM: Synchronous Reluctance Motor, BLDC: Brushless DC motor, SBRSW: Storage-based resistive spot welding application.

Motor type	Volumetric power density (at a given efficiency)	Cooling complexity	Efficiency	Cost	Control complexity	Overall suitability for SBRSWPS
SPMSM	High	Medium	High	High	Low	Suitable
IPMSM	High	Medium	High	High	Medium	Suitable
IM	Low	High	High	Medium	High	Not suitable
SRM	Medium	Low	Low	Low	High	Suitable
SyRM	Medium	Low	Medium	Low	Medium	Suitable
BLDC	High	Medium	High	High	Low	Suitable

Volumetric power density: Because of the use of high strength permanent magnets from alloys of rare earth metals, the volumetric power density of the SPMSM, IPMSM and BLDC motors is the highest. The SRMs and SyRMs come next, followed by the IMs which are the bulkiest options. A good comparative analysis between different motor types has been presented in [78] and [86]. [87] presents the same with respect to Hybrid Electric Vehicle (HEV) application.

Cooling complexity: Liquid cooling is almost always employed when designing motors with high volumetric power density. Such a cooling becomes complicated when copper losses are distributed in both the stator and the rotor. Cooling of the rotor is particularly difficult in case of induction motors where rotor carries the armature winding. Though the rotor of the permanent magnet motors does not have any windings, sufficient amount of care has to be still taken for cooling the rotor. This is because the permanent magnets are sensitive to heat and therefore high rotor temperatures need to be avoided. Hence, it can be said that the cooling requirement for PMSM and BLDC motors is medium. It can also be said that cooling becomes much simpler for SRM and SyRM because the rotor is less sensitive to heat.

Efficiency: PMSMs and BLDC motors with full-load efficiencies close to 97 % are available. IMs can be designed to give efficiencies up to 95 % while efficiencies of about 90 % can be achieved with reluctance motors. Though these values are in general true, it has to be kept in mind that efficiency is a factor which depends greatly on power density.

Cost: The price of the motors with permanent magnets (PMSMs and BLDCs) is quite high, mainly due to permanent magnet prices. Induction motors being a cheaper option while the cheapest of all the motors are the reluctance motors, mainly due to the simple design of the rotor. However, one needs to understand that a standard inverter cannot be used for an SRM and hence, the overall cost of the drive system can go higher when using a SRM.

Control complexity: The BLDC motors are the easiest to control [88]. The control of a SPMSM is also simple because of its zero reluctance torque [78]. The control of IPMSM and SyRM is a bit more complex to that of a SPMSM [88][78]. IM control is much more complicated, mainly because of the requirement of rotor flux estimator[78] [81]. Control of SRM is also complicated because standard three phase control techniques cannot be used.

From the Table B.2 it is very clear that SPMSM and BLDC are the best options available with respect to volume and efficiency. For power ratings in excess of 10 kW, BLDCs are not preferred mainly because of its torque ripple. When cost becomes the driving factor,

the option of SyRM comes into the picture. However, it is very important to mention that, for applications demanding a wide speed range (discharged speed ω_2 much smaller than the fully charged speed ω_1), IPMSM or IM becomes an option which cannot be discarded. When long term storage is necessary, IM and the reluctance motors can be beneficial, since they present zero no-load core losses.

As far as the present WPS application is considered, PMSM is considered to be the best option available and hence, selected for further analysis. However, BLDC can be considered as an option mainly because of its simple control and converter structure, especially when discharging the flywheel.

B.3 Depth of discharge

All the energy stored in the flywheel may not be available for usage during the welding instance. This is because, as the motor speed decreases, its current output needs to be raised, in order to support the constant power output required during the welding process (maximum of 500 ms). Thus, it is clear that there must exist a higher and a lower cut off speed (ω_1 and ω_2 respectively). Thus, the reusable component of the stored energy in the flywheel "ΔE_{fw}" is given by the following equation.

$$\Delta E_{\text{fw}} = \frac{1}{2} J(\omega_1^2 - \omega_2^2) \tag{B.5}$$

Actual values ω_1 and ω_2 depend on the type of motor selected. Further, one needs to remember the rule of thumb that a 30 % reduction in speed results in approximately 50 % reduction in stored energy. It can be said that, for RSW applications where energy is used up at constant power, it is not advisable to reduce the speed approximately below 80 % of full speed. Such a trade off is particularly useful in reducing the required motor power rating which is the main cost factor in a flywheel storage system. For all the analysis in this thesis, it is assumed that ω_2 is equal to $0.9\,\omega_1$. Further, it is assumed that the generator (electric motor working as a generator) output current is constant throughout the welding duration, which is more or less true for the assumed 10 % speed variation.

B.4 Steel flywheel can be the best choice for SBRSWPS

During the analysis of FSS in Chapter 4, it turned out that 4340 steel is volumetrically the best option for the application under consideration. This is best explained from

the figures B.2 to B.5, which have been calculated by applying Equations 4.14 to 4.17, followed by Equations 4.27 and 4.28.

By comparing Fig B.3 and Fig B.5 on can clearly get an idea of how steel performs better to other materials when the stored energy is small (for speeds below $40\,000\,\mathrm{min}^{-1}$). But at higher values of stored energy, steel may not be the right choice (depends on the designed speed). The corresponding motor and the flywheel dimensions are shown in Fig B.2 and B.4 respectively.

B.5 Motor temperature under intermittent loading

Consider a continuous sequence of fixed time welding instances with a fixed time gap between each welding. The corresponding steady state motor temperature behaviour will have a peak temperature ΔT_{m} and a valley temperature ΔT_{mv} [81]. The peak temperature corresponds to the end of the welding, while the valley temperature corresponds to the start of the welding duration. The equations governing the temperatures ΔT_{m} and ΔT_{mv} are

$$\Delta T_{\mathrm{m}} = \Delta T_{\mathrm{rated}} \frac{P_{\mathrm{mlw}}}{P_{\mathrm{mlrated}}} + \left(\Delta T_{\mathrm{mv}} - \Delta T_{\mathrm{rated}} \frac{P_{\mathrm{mlw}}}{P_{\mathrm{mlrated}}} \right) e^{\frac{-t_{\mathrm{w}}}{\tau_{\mathrm{m}}}} \tag{B.6}$$

$$\Delta T_{\mathrm{mv}} = \Delta T_{\mathrm{rated}} \frac{P_{\mathrm{mloff}}}{P_{\mathrm{mlrated}}} + \left(\Delta T_{\mathrm{m}} - \Delta T_{\mathrm{rated}} \frac{P_{\mathrm{mlw}}}{P_{\mathrm{mlrated}}} \right) e^{\frac{-t_{\mathrm{woff}}}{\tau_{\mathrm{m}}}} \tag{B.7}$$

One can write B.6 and B.7 as B.8 and B.9 respectively.

$$\Delta T_{\mathrm{m}} = K_1 + (\Delta T_{\mathrm{mv}} - K_1)\, e^{p_1} \tag{B.8}$$

$$\Delta T_{\mathrm{mv}} = K_2 + (\Delta T_{\mathrm{m}} - K_2)\, e^{p_2} \tag{B.9}$$

where

$K_1 = \Delta T_{\mathrm{rated}} \frac{P_{\mathrm{mlw}}}{P_{\mathrm{mlrated}}}$

$K_2 = \Delta T_{\mathrm{rated}} \frac{P_{\mathrm{mloff}}}{P_{\mathrm{mlrated}}}$

$p_1 = \frac{-t_{\mathrm{w}}}{\tau_{\mathrm{m}}}$ and

$p_2 = \frac{-t_{\mathrm{woff}}}{\tau_{\mathrm{m}}}$

Substituting B.9 in B.8, we get

$$\Delta T_{\mathrm{m}} = K_1 + (K_2 + (\Delta T_{\mathrm{m}} - K_2)\, e^{p_2} - K_1)\, e^{p_1} \tag{B.10}$$

Simplification of B.10 gives

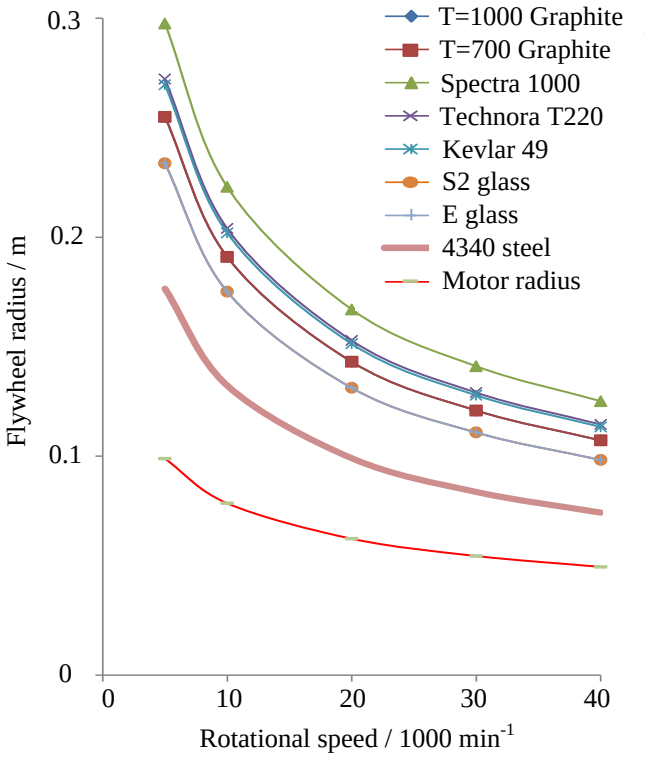
$$\Delta T_{\mathrm{m}} = K_1(1 - e^{p_1}) + K_2(e^{p_1} - e^{p_1+p_2}) + \Delta T_{\mathrm{m}}(e^{p_1+p_2}) \tag{B.11}$$

Adding and subtracting K2 to the R.H.S of B.11 and rearranging, we get

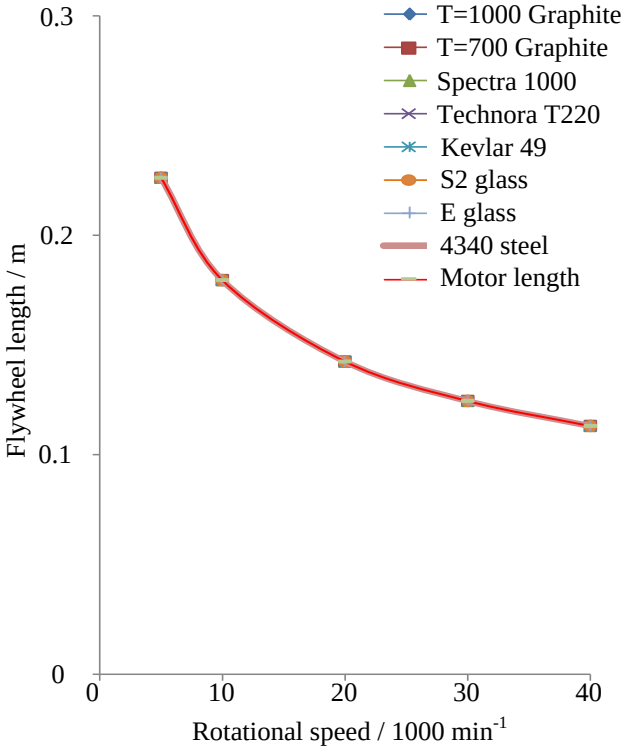
$$\Delta T_{\mathrm{m}}(1 - e^{p_1+p_2}) = K_1(1 - e^{p_1}) + K_2(-1 + e^{p_1}) + K_2(1 - e^{p_1+p_2}) \tag{B.12}$$

$$\Delta T_{\mathrm{m}}(1 - e^{p_1+p_2}) = K_2(1 - e^{p_1+p_2}) + (K_1 - K_2)(1 - e^{p_1}) \tag{B.13}$$

Rearranging the above equation will result in 4.24

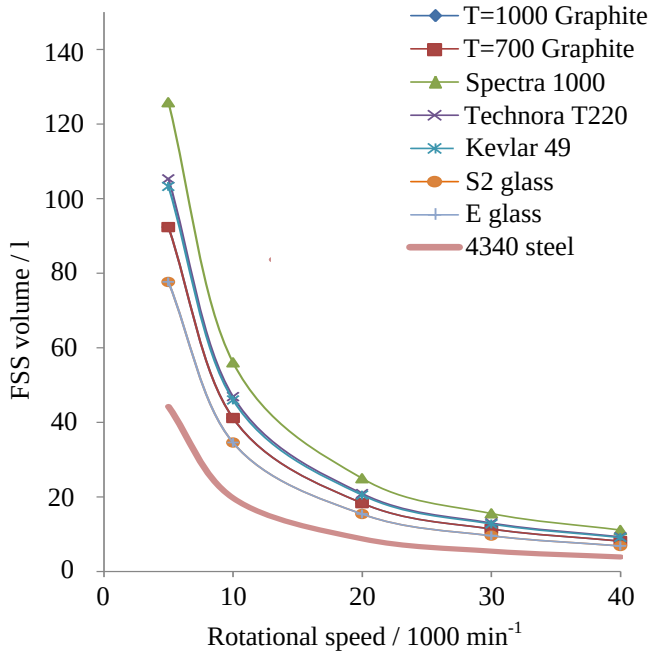


(a)



(b)

Fig. B.2: (a) Flywheel radius versus speed and (b)Flywheel length versus speed for various flywheel materials (Energy stored = 370 kJ, with liquid cooled motor of 100 kW, aspect ratio of 2 and number of poles equal to 4).



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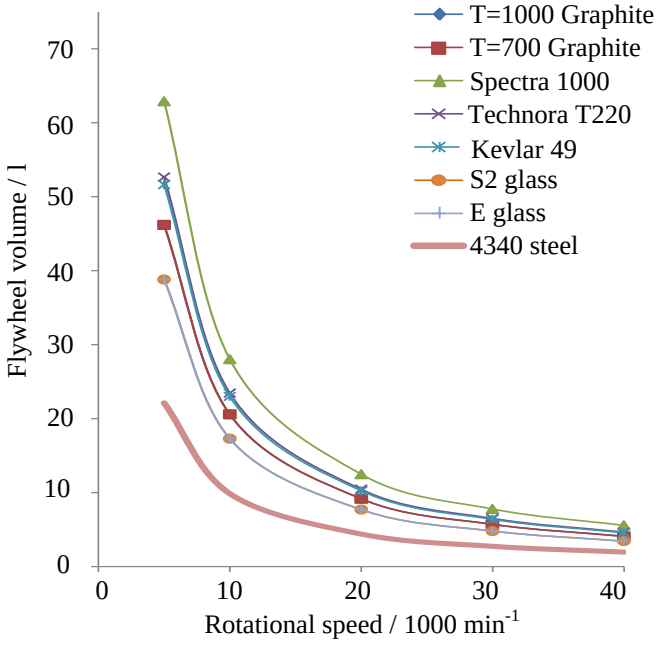
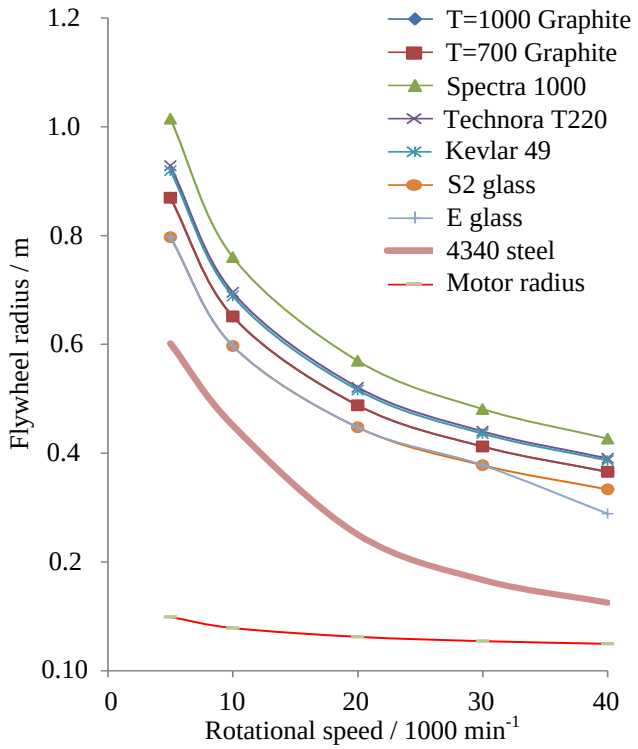
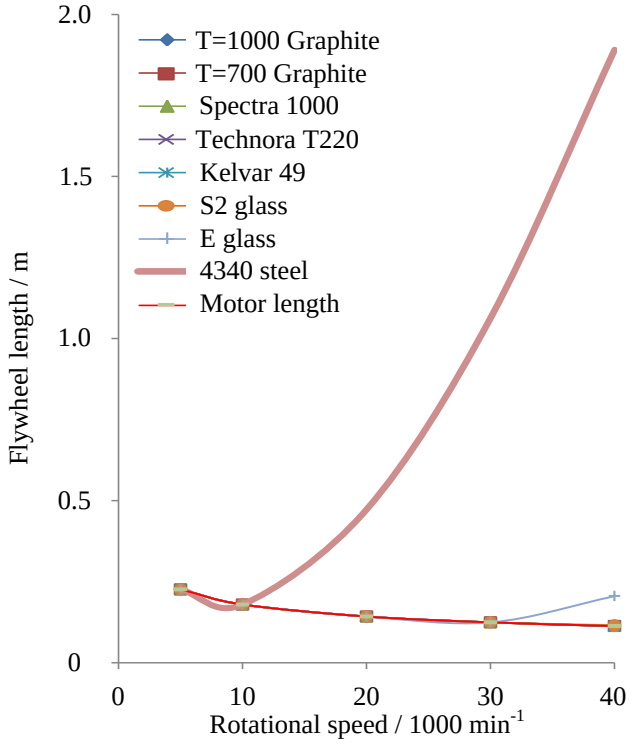


(b)

Fig. B.3: (a) FSS volume versus speed curves and (b) Flywheel volume versus speed for various flywheel materials (Energy stored = 370 kJ, with liquid cooled motor of 100 kW, aspect ratio of 2 and number of poles equal to 4).

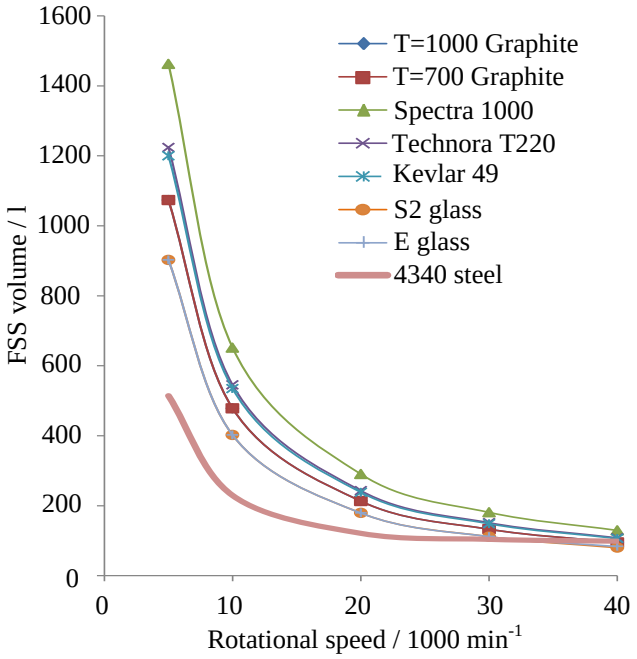


(a)

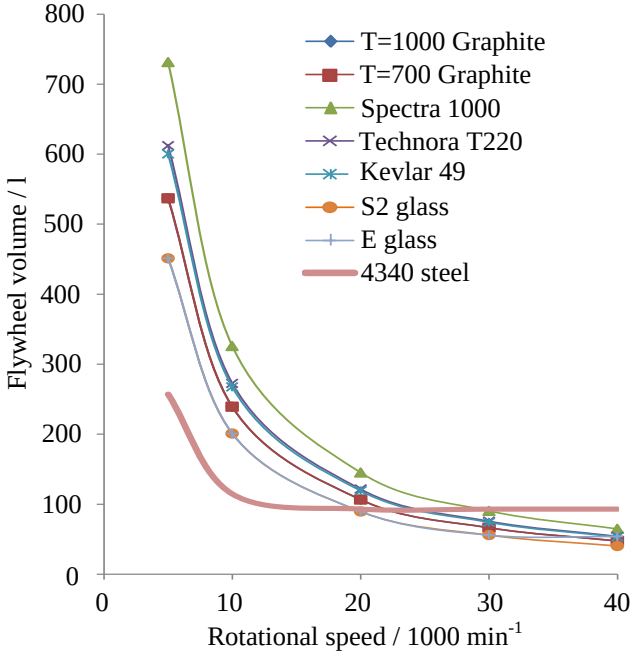


(b)

Fig. B.4: (a) Flywheel radius versus speed and (b)Flywheel length versus speed for various flywheel materials (Energy stored = 50 000 kJ, with liquid cooled motor of 100 kW, aspect ratio of 2 and number of poles equal to 4).



(a)



(b)

Fig. B.5: ((a) FSS volume versus speed curves and (b) Flywheel volume versus speed for various flywheel materials (Energy stored = 50 000 kJ, with liquid cooled motor of 100 kW, aspect ratio of 2 and number of poles equal to 4).

Publications

[AK09] V. Agarwal and D.V.M.M. Krishna. Statistical approach to robust design of control schemes for series or parallel connected power devices. *European Power Electronics and Drives (EPE) Journal*, 19(3):15–21, Sept 2009.

[DCN+12] Patent: Krishna Murali Dora, Silvio Colombi, Prabhakar Krishna Nerella, Narender Reddy Katukuri, and Yashomani Y. Kolhatkar. Control of four-leg transformerless uninterruptible power supply, 2012.

[KA05] D.V.M.M. Krishna and V. Agarwal. Active gate control of series connected igbts using positive current feedback technique. *IEEE Transactions on Circuits and Systems II*, 52(5):261–265, May 2005.

[KFBP13] D.V.M.M. Krishna, N. Frohleke, J. Bocker, and H. Preckwinkel. A simplified mathematical model for dc-balancing and capacitor ripple reduction in 3-level inverters. In *IEEE International Conference on Industrial Technology (ICIT)*, pages 457–462, Feb 2013.

[KPFB13] DVMM Krishna, H. Preckwinkel, N. Fröhleke, and J. Böcker. A novel lc resonant based partial booster scheme for improved efficiency and reduced cost of transformerless photovoltaic inverters. In *PCIM Europe*, pages 1554–1560, May 2013.

[PBB+13] H. Preckwinkel, A. Bünte, J. Böcker, N. Fröhleke, and K. Dora. A novel low cost solar central inverters topology with 99.2 % efficiency. In *15th European Conference on Power Electronics and Applications (EPE)*, pages 1–10, Sept 2013.

[PKFB11a] H. Preckwinkel, DVMM Krishna, N. Fröhleke, and J. Böcker. Entwicklung eines hocheffizienten photovoltaikwechselrichters für den leistungsbereich von 100 bis 500 kw. In *ETG Kongress*, 2011.

[PKFB11b] H. Preckwinkel, D.V.M.M Krishna, N. Frohleke, and J. Bocker. Photovoltaic inverter with high efficiency over a wide operation area - a practical

approach. In *37th Annual Conference on IEEE Industrial Electronics Society IECON*, pages 912–917, Nov 2011.

[PSK+12] Patent: Lakshmi Prasad, Lauro Strozzi, Narender Katukuri, Ivan Saporiti, and Krishna Murali Dora. Method and system for managing uninterruptable power supply for harmonic reduction, 2012.

Bibliography

[1] J. Li, C. R. Sullivan, and A. Schultz. Coupled-inductor design optimization for fast-response low-voltage dc-dc converters. In *Applied Power Electronics Conference and Exposition*, volume 2, pages 817–823, 2002.

[2] P.-L. Wong, P. Xu, B. Yang, and F. C. Lee. Performance improvements of interleaving vrms with coupling inductors. *IEEE Transactions in Power Electronics*, 16(4):499–507, July 2001.

[3] P. Zumel, O. Garcia, J. A. Cobos, and J. Uceda. Tight magnetic coupling in multiphase interleaved converters based on simple transformers. In *Applied Power Electronics Conference and Exposition*, volume 1, pages 385–391, March 2005.

[4] T. Meynard, F. Forest, E. Laboure, V. Costan, A. Cuniere, and E. Sarraute. Monolithic magnetic couplers for interleaved converters with a high number of cells. In *International Conference on Integrated Power Systems (CIPS)*, pages 1–6, June 2006.

[5] F. Forest, B. Gelis, J. Huselstein, B. Cougo, E. Laboure, and T. Meynard. Design of a 28 v-to-300 v/12 kw multicell interleaved flyback converter using intercell transformers. *IEEE Transactions on Power Electronics*, 25(8):1966–1974, August 2010.

[6] J.Y. Lin, C.Y. Lin, and Y.K. Lo. Active-clamping zvs flyback converter employing two transformers. *IEEE Transactions on Power Electronics*, 22(6):2416–2423, November 2007.

[7] B. C. Hyeon and B. H. Cho. Multiple output of dual half bridge llc resonant converter using pfm-pd control. In *IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1133–1140, September 2009.

[8] C. Liangliang, X. Lan, H. Wenbin, and Y. Yangguang. Application of coupled inductors in parallel inverter system. In *Sixth International Conference on Electrical Machines and Systems (ICEMS)*, volume 1, pages 398–401, November 2003.

[9] D. M. Vilathgamuwa, C. J. Gajanayake, and P. C. Loh. Modulation and control of three-phase paralleled z-source inverters for distributed generation applications. *IEEE Transactions on Energy Conversion*, 24(1):173–183, March 2009.

[10] J. Salmon, A. Knight, and J. Ewanchuk. Single phase multi-level pwm inverter topologies using coupled inductors. In *IEEE Power Electronics Specialists Conference (PESC)*, pages 802–808, June 2008.

[11] Y. Panov and M. M. Jovanovic. Design and performance evaluation of low-voltage/high-current dc/dc on-board modules. *IEEE Transactions on Power Electronics*, 16(1):26–33, January 2001.

[12] X. Zhou, X. Peng, and F. C. Lee. A high power density, high efficiency and fast transient voltage regulator module with a novel current sensing and current sharing technique. In *Fourteenth Annual Applied Power Electronics Conference and Exposition (APEC)*, volume 1, pages 289–294, March 1999.

[13] A. F. Roman and K. J. Fellhoelter. Circuit considerations for fast, sensitive, low-voltage loads in a distributed power system. In *Tenth Annual Applied Power Electronics Conference and Exposition (APEC)*, volume 1, pages 34–42, March 1995.

[14] X. Zhou, P.L. Wong, X. Peng, F. C. Lee, and A. Q. Huang. Investigation of candidate vrm topologies for future microprocessors. *IEEE Transactions on Power Electronics*, 15(6):1172–1182, November 2000.

[15] M. T. Zhang, M. M. Jovanovic, and F. C. Lee. Design considerations for low-voltage on-board dc/dc modules for next generations of data processing circuits. *IEEE Transactions on Power Electronics*, 11(2):328–337, March 1996.

[16] S. Tjukovs and D. Pikulins. Investigation of emi reduction and output voltage ripple minimization using interleaved buck converters. *Scientific Journal of RTU*, 8:27–30, 2008.

[17] M. L. Bolloch, M. Cousineau, and T. Meynard. Current-sharing control technique for interleaving vrms using intercell transformers. In *Tenth Annual Applied Power Electronics Conference and Exposition (APEC)*, pages 1–10, September 2009.

[18] P. L. Wong, F. C. Lee, X. Zhou, and J. Chen. Vrm transient study and output filter design for future processors. In *IEEE Proceedings of the 24th Annual Conference of Industrial Electronics Society (IECON)*, volume 1, pages 410–415, August 1998.

[19] T. F. Wu, H. P. Yang, and C. M. Pan. Analysis and design of variable frequency and phase-shift controlled series resonant converter applied for electric arc welding machines. In *IEEE Proceedings of the 21st International Conference on Industrial*

Electronics, Control, and Instrumentation Society (IECON), volume 1, pages 656–661, November 1995.

[20] V. Sivachidambaranathan and S. Dash. Simulation of half bridge series resonant pfc dc to dc converter. In *Recent Advances in Space Technology Services and Climate Change (RSTSCC)*, pages 146–148, November 2010.

[21] D. Y. Jung, S. H. Hwang, Y. H. Ji, J. H. Lee, Y. C. Jung, and C. Y. Won. Soft-switching bidirectional dc/dc converter with a lc series resonant circuit. *IEEE Transactions on Power Electronics*, 28(4):1680–1690, April 2013.

[22] T. Jin and K. Smedley. Multiphase llc series resonant converter for microprocessor voltage regulation. In *IEEE Industry Applications Conference (IAS)*, volume 5, pages 2136–2143, October 2006.

[23] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang. Llc resonant converter for front end dc/dc conversion. In *IEEE Seventeenth Annual Applied Power Electronics Conference and Exposition(APEC)*, volume 2, pages 1108–1112, 2002.

[24] E. Orietti, P. Mattavelli, G. Spiazzi, C. Adragna, and G. Gattavari. Analysis of multi-phase llc resonant converters. In *Brazilian Power Electronics Conference (COBEP)*, pages 464–471, September 2009.

[25] H. Aigner, K. Dierberger, and D. Grafham. Improving the full-bridge phase-shift zvt converter for failure-free operation under extreme conditions in welding and similar applications. In *IEEE Industry Applications Conference(IAS)*, volume 2, pages 1341–1348, October 1998.

[26] D. Tollik and A. Pietkiewiez. Operation of from power soft-switched phase-shifted full-bridge dc-dc converter under extreme conditions. In *Sixteenth International Telecommunications Energy Conference(INTELEC)*, pages 142–147, October 1994.

[27] T. H. Kim, S. J. Lee, and W. Choi. Design and control of the phase shift full bridge converter for the on-board battery charger of the electric forklift. In *IEEE Eighth International Conference on Power Electronics (ICPE ECCE)*, pages 2709–2716, May 2011.

[28] R. Petkov, D. Chapman, and D. James. A comparative study of two dc/dc converter topologies for telecommunications. In *Eighteenth International Telecommunications Energy Conference (INTELEC)*, pages 279–288, October 1996.

[29] B. Y. Chen and Y. S. Lai. Switching control technique of phase-shift-controlled full-bridge converter to improve efficiency under light-load and standby conditions

without additional auxiliary components. *IEEE Transactions on Power Electronics*, 25(4):1001–1012, April 2010.

[30] H. E. Jorgensen, F. Bordry, A. Dupaquier, and G. Fernqvist. High current, low voltage power converter [20ka, 6v] : Lhc converter prototype. In *Sixth European Particle Accelerator Conference*, pages 2059–2061, 1998.

[31] B. C. Franca. *Design and optimization of inter-cell transformers.* PhD thesis, Institut National Polytechnique de Toulouse, 2010.

[32] Jieli Li, C.R. Sullivan, and A. Schultz. Coupled-inductor design optimization for fast-response low-voltage dc-dc converters. In *Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, volume 2, pages 817–823, 2002.

[33] Multi-phase power inductors. `http://www.cooperindustries.com`.

[34] C. Liangliang, X. Lan, and Y. Yan. A novel parallel inverter system based on coupled inductors. In *Twentyfifth International Telecommunications Energy Conference (INTELEC)*, pages 46–50, October 2003.

[35] R. Hausmann and I. Barbi. Three-phase multilevel bidirectional dc-ac converter using three-phase coupled inductors. In *IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 2160–2167, September 2009.

[36] F. Forest, E. Laboure, T.A.Meynard, and V. Smet. Design and comparison of inductors and intercell transformers for filtering of pwm inverter output. *IEEE Transactions on Power Electronics*, 24(3):812–821, March 2009.

[37] R. Peron, V. Guennegues, and Pouliquen. Performances analysis of main components used in 60mw pulsed supply for particle accelerator. In *Thirteenth European Conference on Power Electronics and Applications (EPE)*, September 2009.

[38] M. Le Bolloch, M. Cousineau, and T. Meynard. Current-sharing control technique for interleaving vrms using intercell transformers. In *Thirteenth European Conference on Power Electronics and Applications (EPE)*, September 2009.

[39] K.W.E.Cheng. Tapped inductor for switched-mode power converters. In *Second International Conference on Power Electronics Systems and Applications (ICPESA)*, pages 14–20, November 2006.

[40] P. Xu, J. Wei, K. Yao, Y. Meng, and F. Lee. Investigation of candidate topologies for 12 v vrm. In *Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, volume 2, pages 686–692, 2002.

[41] K. Yao, Mao Ye, Ming Xu, and F.C. Lee. Tapped-inductor buck converter for high-step-down dc-dc conversion. *IEEE Transactions on Power Electronics*, 20(4):775–780, July 2005.

[42] J. Kingston, R. Morrison, M. Egan, and G. Hallissey. Application of a passive lossless snubber to a tapped inductor buck dc/dc converter. In *International Conference on Power Electronics, Machines and Drives*, pages 445–450, June 2002.

[43] O. Lee, S. Y. Cho, and G. W. Moon. Interleaved buck converter having low switching losses and improved step-down conversion ratio. *IEEE Transactions on Power Electronics*, 27(8):3664–3675, August 2012.

[44] B. L. Narasimharaju, S. P. Dubey, and S.P. Singh. Coupled inductor bidirectional dc-dc converter for improved performance. In *International Conference on Industrial Electronics, Control Robotics (IECR)*, pages 28–33, December 2010.

[45] J. H. Park and B. H. Cho. The zero voltage switching (zvs) critical conduction mode (crm) buck converter with tapped-inductor. *IEEE Transactions on Power Electronics*, 20(4):762–774, July 2005.

[46] Sheng Ye, W. Eberle, and Yan-Fei Liu. A novel non-isolated full bridge topology for vrm applications. In *Twenty Second Annual IEEE Applied Power Electronics Conference (APEC)*, pages 134–140, February 2007.

[47] Sheng Ye, E. Meyer, Yan-Fei Liu, and Xiaodong Liu. A novel two phase nonisolated full bridge with shared primary switches. *IEEE Transactions on Power Electronics*, 23(5):2363–2376, September 2008.

[48] P. Xu, J. Wei, and F. Lee. Multiphase coupled-buck converter-a novel high efficient 12 v voltage regulator module. *IEEE Transactions on Power Electronics*, 18(1):74–82, January 2003.

[49] Peng Xu, Jia Wei, and F. C. Lee. The active-clamp couple-buck converter-a novel high efficiency voltage regulator modules. In *Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, volume 1, pages 252–257, 2001.

[50] G. R. Kamath. Simulation study of a simple flux saturation controller for high-frequency transformer link full-bridge dc-dc converters. In *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pages 1–5, December 2012.

[51] R. W. Erickson and D. Maksimovic. *Fundamentals of power electronics - Second edition. ISBN: 0-7923-7270-0.* Kluwer Academic Publishers, 2001.

[52] D. Graovac, M. Pürschel, and A. Kiep. Application note, mosfet power losses calculation using the datasheet parameters. Infineon website, July 2006.

[53] A. Khaligh and Zhihao Li. Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: State of the art. *IEEE Transactions on Vehicular Technology*, 59(6):2806–2814, July 2010.

[54] J. Dixon. Energy storage for electric vehicles. In *IEEE International Conference on Industrial Technology*, pages 20–26, March 2010.

[55] G. Bühler. Ultracaps - eigenschaften und einsatzgebiete. Technical report, Institut für Elektrische Maschinen Antriebe und Bahnen (IMAB), Technische Universität Braunschweig, 2000.

[56] David Connolly. A review of energy storage technologies for the integration of fluctuating renewable energy. Technical report, University of Limerick, October 2010.

[57] Kuldeep Sahay and Bharti Dwivedi. Energy storage technology for performance enhancement of power systems. Technical report, Institute of Engineering & Technology Lucknow, March 2009.

[58] Bella Espinar and Didier Mayer. The role of energy storage for mini-grid stabilization. Technical Report IEA-PVPS T11-02, MINES ParisTech/ARMINES, France, July 2011.

[59] John D. Boyes and Nancy H. Clark. Technologies for energy storage. flywheels and super conducting magnetic energy storage. In *IEEE Power Engineering Society Summer Meeting*, volume 3, pages 1548–1550, June 2000.

[60] Nippon Chemi-Con. Judicious use of aluminum electrolytic capacitor. Technical Report CAT. No. E1001L.

[61] Vishay Intertechnology, Inc. *Aluminum Electrolytic Capacitors in Power Applications.*

[62] Eddy C. Aeloíza, Jang-Hwan Kim, Pedro Ruminot, and Prasad N. Enjeti. A real time method to estimate electrolytic capacitor condition in pwm adjustable speed drives and uninterruptible power supplies. In *IEEE Power Electronics Specialists Conference*, pages 2867–2872, June 2005.

[63] CDM Cornell Dubilier. Aluminum electrolytic capacitor application guide.

[64] M. R. Acacio Amaral and A. J. Marques Cardoso. An economic offline technique for estimating the equivalent circuit of aluminum electrolytic capacitors. *IEEE Transactions on Instrumentation and Measurement*, 57(12):2697–2710, December 2008.

[65] F. Perisse, P. Venet, G. Rojat, and J. M. Rétif. Simple model of an electrolytic capacitor taking into account the temperature and aging time. *Springer-Verlag, Electrical Engineering Journal*, 88, Issue 2:89–95, September 2006.

[66] General Atomics Energy Products. Engineering bulletins capacitors.

[67] Nichicon Corporation. Application guidelines for aluminum electolytic capacitors. Technical Report CAT. No. 8101C.

[68] Sam Parler (Jr. Director of R&D). Heating in aluminum electrolytic strobe and photoflash capacitors. Technical report, Cornell Dubilier.

[69] Maxwell Technologies, Inc. *Product Guide – Maxwell technologies BOOSTCAP ultracapacitors*, 2009.

[70] Life expectiancy of supercapacitors. `http://www.wima.cn/EN/supercap_applic.htm`.

[71] R. Martin, J.J. Quintana, A. Ramos, and I. de la Nuez. Modeling electrochemical double layer capacitor, from classical to fractional impedance. In *The 14th IEEE Mediterranean Electrotechnical Conference*, pages 61–66, May 2008.

[72] R.M. Nelms, D.R. Cahela, and Bruce J. Tatarchuk. Modeling double-layer capacitor behavior using ladder circuits. *IEEE Transactions on Aerospace and Electronic Systems*, 39(2):430–438, April 2003.

[73] S. Buller, M.Thele, R.W. De Doncker, and E. Karden. Impedance-based simulation models of supercapacitors and li-ion batteries for power electronic applications. *IEEE Transactions on Industry Applications*, 41(3):742–747, May 2005.

[74] S. Buller, E. Karden, D. Kok, and R.W. De Doncker. Modeling the dynamic behavior of supercapacitors using impedance spectroscopy. *IEEE Transactions on Industry Applications*, 38(6):1622–1626, November 2002.

[75] J. Pyrhönen, T. Jokinen, and V. Hrabovcova. *Design of rotating electrical machines ISBN: 978-0-470-69516-6*. John Wiley and Sons Ltd, 2008.

[76] Maria Ines Lopes Marques. Design and control of an electrical machine for flywheel energy-storage system. Master's thesis, Universidade Técnica de Lisboa, May 2008.

[77] E+A Motors. Sychronous motor type overview. `www.eandaUSA.com`, 2007.

[78] Prof. Dr.-Ing. Joachim Böcker. Lecture notes - controlled three-phase drives. Universität Paderborn, 2012.

[79] D. Gerada and A. Mebarki Etal. High-speed electrical machines: technologies, trends and developments. *IEEE Transactions on Industrial Electronics*, 61(6):2946–2959, June 2014.

[80] J. G. Bitterly. Flywheel technology: past, present and 21st century projections. *IEEE Aerospace and Electronic Systems Magazine*, 13(8):13–16, August 1998.

[81] Werner Leonhard. *Control of electrical drives, third edition. ISBN: 3-540-78115-3.* Springer Berlin Heidelberg, 2001.

[82] Perry I-Pei Tsao. *An integrated flywheel energy storage system with a homopolar inductor motor/generator and high-frequency drive.* PhD thesis, University of California, Berkeley, 2003.

[83] Arnon 5 non grain oriented electrical silicon steel core loss chart. `http://http://www.arnoldmagnetics.com/Precision-Thin-Metals/Materials/Silicon-Steel/Non-Grain-Oriented-Electrical-Steel.aspx`.

[84] N. Urasaki, T. Senjyu, and K. Uezato. Investigation of influences of various losses on electromagnetic torque for surface-mounted permanent magnet synchronous motors. *IEEE Transactions on power electronics*, 18(1):131–139, January 2003.

[85] R. Pena-Alzola and R. Sebastian Etal. Review of flywheel based energy storage systems. In *IEEE International Conference onPower Engineering, Energy and Electrical Drives*, pages 1–6, May 2011.

[86] Juan De Santiago and Janaina Goncalves de Oliveira. *Electric machine topologies in energy storage systems ISBN: 978-953-307-119-0.* InTech, 2010.

[87] T. Finken, M. Felden, and K. Hameyer. Comparison and design of different electrical machine types regarding their applicability in hybrid electrical vehicles. In *18th International Conference on Electrical Machines*, pages 1–5, September 2008.

[88] Prof. Dr.-Ing. Joachim Böcker. Lecture notes - mechatronics and electrical drives. Universität Paderborn, 2014.