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High Power LLC Resonant Converter Optimized for High Efficiency and Industrial Use

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Abstract

Since the development and commercialization of the internet in the 1990s, the market for industrial power supplies of the information and telecommunication infrastructure (IT) has steadily grown. As per today the consumption of electrical energy by IT infrastructure in the United States is above 2% of the overall electricity demand. In order to feed IT infrastructure out of the national power grids, the electricity needs to be converted by power supplies. This conversion process requires invests into the power supplies, their space and location, appropriate climatic environment and cooling, and the higher power demand resulting from the electrical conversion losses. The LLC resonant converter analyzed in this thesis potentially enables a distinct reduction of invest and operational costs based on its superior power density and conversion efficiency.

The main obstacles for the adoption of the LLC resonant converter within industrial power supplies are the more disadvantageous control of the power transfer compared to its pulse-width controlled counterparts and the more complex design. This thesis outlines the modeling methods for resonant converters and proposes the extension of the time domain analysis model by a lumped resistive circuit element. Effects are a more accurate prediction of the converters DC-DC gain and the feasibility of modeling the paralleling of two interleaved operated converters. The dynamic modeling of the LLC resonant converter is performed utilizing the extended describing functions method, thereby showing the large variations of the plant characteristic in the dependence on the control variable switching frequency. The results of the dynamic modeling are compared to measurements on a prototype. Further results are demonstrated by a load step measurement, showing the feasibility of an adaptive compensator approach, which is designed to adapt to the variation of the plant characteristic. Further on the problematic short-circuit behavior of the LLC resonant converter is described and a circuit extension based on the resonant capacitor clamping method is proposed. This extension enables the short-circuit robustness of the converter when it is combined with a sophisticated constant current limit control scheme. The successful implementation of such arrangement is demonstrated on a prototype.

The optimal design of the LLC resonant converter is complicated by the non-linear relationship between four basic design parameters and the constraints given by the operating region boundaries. This thesis states fundamental design trade-offs within the LLC converter design for industrial power supplies and proposes the usage of numerical optimization with respect to an optimal converter design regarding operating region coverage and efficiency. The required component loss models for the numerical optimization are derived from theoretical backgrounds and parameterized by data-sheet values or measurements. The method of parameterization by measurement results is especially developed for the loss models of the magnetic components. The execution of the automated design optimization for a design example shows that the efficiency of the converter is especially affected by a limitation of the allowed switching frequency range. In contrast the absolute switching frequency level has less influence, resulting in that the choice of the converter's resonant frequency has minor sensitivity with respect to the converter's efficiency. Based on the substantial loss contributors and a design of

the magnetic components feasible for industrial use, the numerical optimization yields a peak efficiency of 99.2%.

The synchronized paralleling of two LLC resonant converters is especially beneficial in case of low output voltages and resulting high output currents. This is due to the current ripple cancellation effect, which enables a huge reduction of the capacitive output filter volume. The problematic issue of power imbalance between both converters caused by slightly unequal resonant circuit element values is analyzed in this thesis utilizing the time domain modeling approach. With respect to the revealed problem of imbalance a converter arrangement within an industrial power supply is proposed that enables the usage of the synchronized paralleling of two LLC resonant converters and its merits of current ripple cancellation on the output side. The successful implementation of such arrangement is demonstrated on a prototype.

Zusammenfassung

Der Markt für industrielle Stromversorgungen im Bereich der Informations- und Kommunikationstechnik (IKT) erlebt seit Beginn des Internetbooms in den 90er Jahren ein stetiges Wachstum. Mittlerweile liegt der Stromverbrauch von informationstechnischen Anlagen in den Vereinigten Staaten bei über 2% des Gesamtstromverbrauches. Der aus dem öffentlichen Stromnetz entnommene Strom muss zur Nutzbarkeit in informationstechnischen Anlagen umgeformt und transformiert werden. Dieser von industriellen Stromversorgungen durchgeführte Transformationsprozess erfordert Investitionen in die Stromversorgung selber, in den Installationsort, für Klimatisierung bzw. Kühlung, und die durch eine Verlustbehaftung des Transformationsprozesses bedingte zusätzliche Stromaufnahme. Der in dieser Arbeit betrachtete LLC Resonanzkonverter besitzt das Potential, durch hohe Leistungsdichte und Effizienz die Investitions- und Betriebskosten informationstechnischer Anlagen deutlich zu reduzieren.

Die Schwierigkeiten für den industriellen Einsatz des LLC Resonanzkonverters liegen in der im Vergleich zu pulsbreitenmodulierten Konvertern ungünstigeren Steuerbarkeit des Energieflusses und den komplexeren Zusammenhängen bei der Auslegung des Konverters. In dieser Arbeit werden die Modellierungsmethoden für Resonanzkonverter beschrieben und die Methode der Zeitbereichsmodellierung um einen resistiven Anteil erweitert. Dies führt zu einer exakteren Bestimmung des Gleichspannungsübersetzungsverhältnisses des Konverters und ermöglicht es zudem die Parallelschaltung von mehreren Konvertern sinnvoll zu beschreiben. Die Modellierung der dynamischen Eigenschaften des LLC Resonanzkonverters wird mittels der Methode der erweiterten Beschreibungsfunktionen durchgeführt und die große Variation der Streckencharakteristik in Abhängigkeit der Stellgröße Schaltfrequenz aufgezeigt. Die Modellierungsergebnisse werden mit Messungen an einem Prototyp verglichen und die Ergebnisse der Realisierung eines adaptiven Reglers, welcher die Variation der Streckencharakteristik kompensiert, anhand einer Lastsprungmessung demonstriert. Das problematische Kurzschlussverhalten des LLC Resonanzkonverters wird in einem weiteren Teil der Arbeit adressiert und eine schaltungstechnische Erweiterung basierend auf der Methode der Spannungsklemmung des Resonanzkondensators vorgeschlagen. Die Erweiterung stellt die Kurzschlussfestigkeit des Konverters in Kombination mit einer steuerungstechnischen Implementierung einer Konstantstrombegrenzung des Ausgangsstromes her. Deren erfolgreiche Realisierung wird anhand von Messbeispielen an einem Prototyp beschrieben.

Die optimale Auslegung des LLC Resonanzkonverters wird durch die nichtlinearen Zusammenhänge zwischen 4 grundsätzlichen Designgrößen und den Betriebsbereichsgrenzen als Nebenbedingungen erschwert. Diese Arbeit legt grundsätzliche Zielkonflikte bei der Auslegung des LLC Resonanzkonverters für die Applikation in einer industriellen Stromversorgung dar und schlägt zur Durchführung einer optimalen Auslegung hinsichtlich Effizienz und Betriebsbereichabdeckung den Einsatz eines numerischen Optimierers vor. Die zur Durchführung einer solchen automatischen Optimierung notwendigen Verlustmodelle werden auf Basis theoretischer Zusammenhänge aufgestellt und mittels Datenblattangaben oder messtechnisch gewonnener Werte parametrisiert. Die messtechnische Parametrisierung wurde insbesondere für die magnetischen Komponenten entwickelt und durchgeführt. Die Ausführung der automatisierten optimalen Auslegung anhand eines Designbeispiels zeigt, dass besonders eine

Einengung des zulässigen Schaltfrequenzbereiches die Effizienz des Konverters beeinträchtigt. Das Schaltfrequenzniveau hat hingegen einen geringeren Einfluss auf die Konvertereffizienz, sodass die zu wählende Resonanzfrequenz des Resonanzkreises nur eine geringe Sensitivität für die Konvertereffizienz darstellt. Basierend auf den wesentlichen Verlustanteilen und einer industriell geeigneten Realisierung der magnetischen Bauelemente resultiert aus der automatischen Optimierung ein Spitzenwirkungsgrad von 99,2%.

Die synchron getaktete Parallelschaltung zweier LLC Resonanzkonverter ist durch die gegenseitige Kompensation der Ein- und Ausgangsstromwelligkeiten besonders geeignet für niedrige Ausgangsspannungen und hieraus resultierenden hohen Ausgangsströmen. Durch die Kompensation wird eine massive Verkleinerung des kapazitiven Ausgangsfilters möglich. Die sich bei der Parallelschaltung auftuende Problematik der Leistungsimbalance durch Bauelementtoleranzen wird in dieser Arbeit basierend auf einem Zeitbereichsmodell des Konverters analysiert. Auf Grund der dargelegten Problematik wird eine Konverteranordnung vorgeschlagen, welche die synchron getaktete Parallelschaltung des LLC Resonanzkonverters in einem industriellen Stromversorgungsgerät und die Nutzung der reduzierten Stromwelligkeit auf der Ausgangsseite ermöglicht. Dies wird anhand von Prototypmessungen demonstriert.

Contents

List of Symbols

Name	Description	Unit of measure
A_c	core cross section	m^2
A_e	equivalent core cross section	m^2
A_g	cross section of air gap	m^2
A_i	system matrix of state *i*	---
A_m	Amplitude margin	unitless
A_R	cross section of a resistive element	m^2
A_w	area of winding window	m^2
B_i	input matrix of state *i*	---
B,b	flux density	Vs / m^2
b_w	winding window with	m
C_cl	capacitance of clamping capacitor	As / V
C_DL	DC link capacitance	As / V
C_i	output matrix of state *i*	---
$\boldsymbol{c}(\dots)$	vector of non-linear constraint functions of …	---
C_j	junction capacitance of a semiconductor	As / V
C_oss	drain-to-source output capacitance of a MOSFET semiconductor	As / V
C_s	series resonant capacitance	As / V
C_str	stray capacitance of a magnetic component	As / V
C_DG	drain-to-gate capacitance of a MOSFET semiconductor	As / V
C_DS	drain-to-source capacitance of a MOSFET semiconductor	As / V
C_{GS}	gate-to-source capacitance of a MOSFET semiconductor	As / V
d	damping factor	unitless
d	diameter	m
d_0	diameter of a litz wire	m
D	electrical flux density	As / m^2
D_i	feedthrough matrix of state *i*	---
E	electrical field strength	V / m
$f(\dots)$	function of …	---
f	frequency	s^{-1}
f_s	switching frequency	s^{-1}
f_ss	excitation frequency	s^{-1}
F_burst	switching frequency threshold of burst mode operation	s^{-1}
F_c	cross over frequency	s^{-1}
F_s	skin effect factor	unitless
F_p	proximity effect factor	unitless
f_0	resonant frequency	s^{-1}
$\boldsymbol{F}(\dots)$	vector of non-linear system functions of …	---
$F(\boldsymbol{x})$	objective function of search vector $\boldsymbol{x}$	---
F_n	normalized switching frequency f_s	unitless
F_1	normalized resonance frequency f_1	unitless
G	transfer function	---
$g(\boldsymbol{x})$	constrains function of search vector $\boldsymbol{x}$	unitless
h	inductance ratio of series and parallel resonant inductance	unitless

h	height of winding window	m
h_i	height of winding layer i	m
H	magnetic field strength	A / m
H_{fr}	magnetic field strength of a fringing field	A / m
H_i	external magnetic field strength at position of layer i	A / m
H_{r}	internal, radial oriented magnetic field strength of a litz wire	A / m
i	number of a winding layer	unitless
I	number of intervals within a switching period	unitless
$\boldsymbol{I}$	unity matrix	unitless
I_{Base}	base current for current normalization	A
i_{buck}	modulated output current of a buck-type switching cell	A
I_{cc}	current value of constant current regulation	A
$i_{\mathrm{D}}, i_{\mathrm{chn}}$	drain input and channel current of a MOSFET semiconductor	A
$i_{\mathrm{DG}}, i_{\mathrm{DS}}$	capacitive currents of a MOSFET semiconductor	A
i_{F}	terminal current of a diode	A
i_{g}	source current of the effective voltage source of the LLC ECD	A
i_{i}	inverter bridge input current	A
I_i	current in winding layer i	A
i_{o}	rectifier output current	A
I_{o}	average of i_{o} or DC-DC converter output current	A
i_{r}	series resonant current	A
i_{p}	parallel resonant current	A
i_{m}	magnetizing current	A
I_{r}	resonant current during a switching transition	A
i_{S}	input current of switch S	A
i_{Ss}	input current of switch Ss	A
I_{st}	current in a single strand of a litz wire	A
i_{w}	terminal current of a winding	A
j, J	normalized current i, I	unitless
j	imaginary unit	---
k	Steinmetz parameter for sinusoidal excitation	W
k_{br}	auxiliary factor indicating half- or full-bridge configuration	unitless
k_{c}	Steinmetz parameter for arbitrary excitation	W
k_{Cj}	coefficient of junction capacitance influence	unitless
k_{cl}	factor of input to clamping voltage ratio	unitless
k_{ctr}	initial contraction coefficient	unitless
$k_{\mathrm{Ls}}, k_{\mathrm{Cs}}, k_{\mathrm{Lp}}$	coefficients of value variance of the nominal value of L_s, C_s, L_p	unitless
K_{fr}	fringing field proportionality factor	A / (Vsm)
K_{g1}	factor of adjustable gain in a frequency response measurement	$(\mathrm{Vs})^{-1}$
k_{plt}	coefficient of penalty function of optimization constraints	unitless
k_{rec}	auxiliary factor indicating center-tapped or full-wave rectification	unitless
$K_{\mathrm{s..}}, K_{\mathrm{c..}}$	unknowns of an initial value problem	---
K_{sh}	load sharing factor	unitless
k_{sw}	coefficient of switching loss energy	unitless
k_{tol}	minimal progress of optimization solver bevor termination	---
L	inductance	Vs / A
l_{e}	equivalent magnetic path length	m

L_f	filter inductor of a forward-type converter	Vs / A
l_g	air gap length	m
l_i	length of winding i	m
l_R	length of a resistive element	m
L_s	series resonant inductance	Vs / A
L_p	parallel resonant inductance	Vs / A
L_m	magnetizing or mutual inductance of transformer	Vs / A
L_σ	stray inductance of a current path	Vs / A
L	number of winding layers of a winding	unitless
M	normalized DC-DC gain	unitless
M_oi	DC-DC gain input voltage to output voltage	unitless
m	normalized voltage v	unitless
N_ch	number of turns of a choke	unitless
n_con	number of interleaved operated converters	unitless
N_w	number of turns of a winding	unitless
N_i	number of turns of winding or winding layer i	unitless
n_igp	number of initial grid points	unitless
N_st	number of strands in a litz wire	unitless
n	transformer turns ratio	unitless
N_p, N_s	primary and secondary number of turns of a transformer winding	unitless
N'_bw	equivalent number of strands of winding window width	unitless
N'_hw	equivalent number of strands of winding window height	unitless
p	tolerance	unitless
p_i	input power	W
p_cu	copper packing density of a winding	unitless
$p_{\mathrm{cu},i}$	copper packing density of winding layer i	unitless
p_o	output power	W
p_v	dissipative power loss	W
P_Vs	dissipative power loss related to the skin effect	W
P_Vp	dissipative power loss related to the proximity effect	W
q	control variable of a converter	---
Q	quality factor or normalized load resistance	unitless
Q_ac	quality factor or normalized load resistance of an AC ECD	unitless
Q	electric charge	As
Q_g	gate charge of a MOSFET	As
R	ohmic resistance	V / A
R_ac	load resistance of AC equivalent circuit	V / A
R_AC	AC resistance of a conductor, winding layer or winding	V / A
R_c	equivalent resistance of the output capacitor ECD	V / A
$R_\mathrm{DS(on)}$	on-state resistance of a MOSFET	V / A
R_L	load resistance	V / A
R_s	equivalent series resistance of resonant circuit	V / A
R_DC	DC resistance of a conductor or winding layer	V / A
R_d	equivalent series resistance of secondary side of the LLC ECD	V / A
s	Laplace variable	s^{-1}
$S_\mathrm{v,x}$	sensitivity of conversion losses to a design parameter or value x	W/[x]
t	time	s

T	period	s
t_{ch}	time instant of a switching transition of depleted channel current	s
t_{end}	time instant of a ending switching transition	s
t_k	time instant *k*	s
t_{sw}	time instant of a starting switching transition	s
$T_{k,i}$	time stamp of interval *i* in switching period *k*	s
T_{c}	core temperature	K
T_{clc}	calculation time caused delay of a signal processed in a DSP	s
T_{d}	half-bridge dead time	s
T_{HU}	hold-up time	s
T_{j}	junction temperature of a semiconductor element	K
T_{w}	winding temperature	K
T_0	resonant period	s
T_{s}	switching period	s
T_{sp}	sampling period of a DSP processed signal	s
T_{ZVS}	half-bridge reload time	s
T_β	natural period	s
$\boldsymbol{u}(t)$	time variable input vector of a state-space model	---
$v_{\mathrm{A}}, v_{\mathrm{B}}$	input signals of a FRA	V
v_{AC}	AC grid voltage	V
V_{Base}	voltage base for voltage normalization	V
V_{c}	core volume of a magnetic component	m^3
V_{cl}	clamp voltage	V
V_{Ccl}	voltage of clamping capacitor	V
v_{Cs}	resonant capacitor voltage	V
V_{Cs}	resonant capacitor voltage during a switching transition	V
v_{Co}	voltage of capacitive part of the output capacitor equivalent circuit	V
v_{ctrl}	control voltage representing the input signal of a SISO system	V
v_{D}	terminal voltage of a diode	V
v_{d}	voltage of the rectifier output of LLC equivalent circuit	V
v_{dr}	drive voltage of a semiconductor switch	V
V_{DL}	DC-link voltage	V
v_{DS}	drain-to-source voltage of MOSFET semiconductor	V
v_{err}	control error signal in a voltage control loop	V
v_{f}	forward voltage drop of a diode	V
V_g	resonant circuit effective input voltage	V
v_{gAB}	resonant circuit effective input voltage between nodes A and B	V
v_{i}	input voltage of DC-DC converter	V
v_{Lp}	voltage of parallel resonant inductance L_{p}	V
v_{Ls}	voltage of series resonant inductance L_{s}	V
V_{nCs}	normalized resonant capacitor voltage	unitless
v_{o}	output voltage of DC-DC converter	V
v_{o}^*	setpoint of a voltage control loop	V
v_{Rs}	voltage of resonant circuit equivalent resistance R_{s}	V
v_{S}	main terminal voltage of switch S	V
v_{w}	terminal voltage of a winding	V

V_{ZD}	break down voltage of a Zener diode	V
$w_{\mathrm{Cs}}, w_{\mathrm{Ls}}, w_{\mathrm{Lp}}$	electrical energy stored in circuit elements C_s, L_s, L_p	Ws
W_{v}	loss energy of a defined event	Ws
$\boldsymbol{x}(t)$	time variable state vector of a state-space model	---
$\boldsymbol{x}$	parameter search vector of an optimization problem	---
X_{x}	Reactance of element x	V / A
$\boldsymbol{x}_{\mathrm{hcv}}$	harmonic coefficient vector	---
$\boldsymbol{y}(t)$	time variable output vector of a state-space model	---
Z_{i}	input impedance of AC equivalent circuit	V / A
Z_0	characteristic impedance	V / A
$\alpha, \beta, \gamma, \delta$	substitutions in an initial value problem	---
α, β	Steinmetz coefficients	unitless
α	skin constant	m^{-1}
α_{T}	temperature coefficient	K^{-1}
γ	skin depth factor	unitless
δ	skin depth	m
φ	phase angle or phase shift	deg
φ	phase margin	deg
ε	minimum value of progress in a numerical search algorithm before termination	---
ω_0	resonant angular frequency	s^{-1}
ω_{s}	angular frequency of switching period	s^{-1}
μ	magnetic permeability	Vs / (Am)
μ_0	magnetic permeability in a vacuum	Vs / (Am)
μ_{r}	magnetic permeability constant	unitless
μ_{eq}	equivalent permeability	Vs / (Am)
θ	time correspondent switching period angle	unitless
Θ	magnetomotive force	A
Δ	difference operator	---
ρ	specific electrical resistance	Vm / A
η	electrical conversion efficiency	unitless
ν	number of harmonic component	unitless
κ	specific electrical conductivity	A / (Vm)
π	circle constant	---
Φ	magnetic flux or angular function	Vs or unitless
Φ_{m}	mutual magnetic flux	Vs
∇	Nabla operator	---

General Notations

x	variable or signal x	---
X	average or static value of x (unless otherwise noted)	---
X, X^*	X is complex, X is complex conjugate	---
$\hat{x}$	peak value of x	---
$\dot{x}$	derivative of x	---
$\bar{x}$	average of x	---
$\vec{X}$	X is vector	---
$\boldsymbol{X}$	X is multidimensional	---
$\Re$	real part operator	---

Subscripts

ch	choke related
eq	equivalent
g	gap, related to magnetic components
i	input
j	junction
m	mutual
max	maximal
min	minimal
nl	non linear
nom	nominal
pg	peak gain
o	output
p	related to primary side
s	related to secondary side
xf	transformer related
zg	zero gain
zl	zero load
x,y,z	x,y,z component of a Cartesian system
0	starting value of iterative process
<1>	fundamental component

Abbreviations

AC	Alternating Current
CCMA	Continous Conduction Mode Above Resonance
ECD	Equivalent Circuit Diagram
DCMB	Discontinous Conduction Mode Below Resonance
DC	Direct Current
DDL	Dual DC-Link
DE	Differential Equation
DSP	Digital Signal Processor
EDF	Extended Describing Function
EMI	Electro Magnetic Interference
FHA	Fundamental Harmonic Analysis
FOM	Figure of Merit
FRA	Frequency Response Analyzer
hcv	harmonic coefficient vector
IA	Impedance Analyzer
IT	Information Technology
IVP	Initial Value Problem
MOSFET	Metal-Oxid Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
plt	penalty
PSU	Power Supply Unit
sat	saturation
SISO	Single Input Single Output System

sgn	signum
s/h	sample and hold
XFMR	Transformer

1 Introduction

Since the development and commercialization of the internet in the 1990s a steadily increasing worldwide demand for information and telecommunication infrastructure has started. Today's infrastructure consists of a mix of central and decentral appearances of information technology hardware. The central appearances are counted dedicated buildings occupying huge numbers of computer, server and storage hardware owned by governmental institutions, research networks or private companies. The decentral appearances are counted local installations or outdoor cabinets that serve as internet network hubs or as base stations for cellular radio services.

For the world wide information and communication infrastructure the following superordinate characteristics can be stated:

- The hardware equipment is electrically supplied out of the national AC power grids.
- Every equipment requires a power supply unit that enables the supply out of the national AC power grid by converting the high voltage AC into low voltage DC current.
- The usage and importance of information technology for today's society deserves for an uninterruptable service quality of network and radio services and hence an uninterruptable power supply of the equipment.

Based on these facts it becomes obvious that the market for industrial power supplies has gained the same growth and importance as the information technology and its services. The industry market report [Eykyn] is cited by [Carbone] as follows: "Also driving demand for AC-DC and DC-DC power supplies will be the continued growth of data centers that support cloud computing and the Internet of Things. Revenue for power supplies to the server, storage and networking markets will rise 24 percent from 2014 to 2018, according to the report." Furthermore according to [Delta] the actual market revenue for "Telecom/ Datacom, industrial and medical devices" as part of the "AC-DC Non-commodity market" is projected as follows: "The market was worth USD 8.3 billion in 2013 and is projected to grow to USD 12.4 billion by 2018 at an average of more than 8% a year." The before mentioned market research data demonstrate the actual multibillion US dollar market volume of industrial power supplies and the still on-going substantial growths.

In parallel to the growth of the market the consumption of electrical energy by information technology equipment has also increased and become a distinct part of the world wide power consumption and greenhouse gas emissions. For example the estimated consumption of US data centers in 2013 is $91 \cdot 10^9$ kWh [Benenson], which is a percentage of 2.24% out of the total US electricity consumption of $4066 \cdot 10^9$ kWh in 2013 [EIA]. This evidence has led to the requirement of striving for energy efficiency within the information technology and in particular for efficient power conversion within the power supply units. The voluntary "80plus" certification program (www.plugloadsolutions.com) for power supply units has evolved as an industry standard and defined the conversion efficiency of power supplies as to be better than 80% in the beginning of the program in 2005 and up to efficiency values of higher than 96% for today's highest rated "Titanium" level certificate.

The success of the "80plus" program[1] is supported by two circumstances: Firstly the public promotions of governmental institutions like the United States Environmental Protection Agency (EPA) (www.epa.gov) pushed big equipment manufacturers and internet companies to adapt the energy efficiency certification standards because of public interest. Secondly the steadily increasing amount of electrical energy required to operate modern big data centers as well increases the installation and operational costs of the electricity and cooling infrastructure of those data centers. It should be noted here that the cooling system is an essential installation part of big data centers since the consumed energy, which can be in the range of several 10^{th} of MW for big facilities[2], is completely dissipated as process heat. In consequence the usage of energy efficient power supplies typically redeems quickly. For example: The dissipated energy that is saved for a 3000 W power supply having 96% instead of 90% conversion efficiency and running for 3 years at 80% nominal load is 3780 kWh. Assuming the electricity price of 0.0665 US$/kWh[3], the 96% efficient power supply is profitable if it is less than 252 US$ more expensive than the 90% efficient version. This dollar value is typically above 50% of the total sales price of a 3000 W unit according to the author's experience[4]. Additional savings result from downgrades of the electricity and cooling infrastructure of a data center.

In prospect of the described demand for more efficient power supplies compared to the state of the art, this work proposes the usage of the LLC resonant converter within the power supply as a solution for higher efficiency, reduced electricity and cooling needs. As per today the LLC resonant converter has already commonly been identified within the power electronics community as a candidate for highly efficient power conversion. But a key factor for a broad industrial usage of the LLC resonant converter is given by the optimal design and sophisticated control of the converter, at which the treatment of both aspects requires appropriate modeling of the converter and its function. Modeling and design are thoroughly analyzed in this work and solutions for the industrial usage are presented.

Chapter 2 summarizes the electrical requirements of power supplies for the industrial telecommunication and server sector. Among a description of potential DC-DC power converter topologies the state of the art is presented. The potentials and beneficial characteristics of the LLC resonant converter topology are outlined and the motivation of this work is stated in detail.

In Chapter 3 the existing modeling methods are summarized and the ones applied in this work are presented. A model extension compared to the state of the art is proposed that considers resistive damping within the exact time domain solution. This extension especially facilitates the analysis of load sharing between paralleled LLC resonant converters presented in Chapter 6. In a further part of Chapter 3 the loss modeling of the main loss contributing circuit elements of a LLC resonant converter is presented. Especially for the loss modeling of the inductive components a simplified method derived from relevant methods of existing literature is proposed which is applied further on in this work.

[1] With date 7/17/2015 5256 PSUs of 295 brands have been certified and published on www.plugloadsolutions.com

[2] The case study in [Benenson2] for a typical data center design assumes 252 server racks of 30 kW rated input power each, equaling a total input power of 7.56 MW

[3] US average May 2015 according to [EIA2]

[4] Based on sales prices for industrial customers in 2015 and dependent on the order quantity. The experience of the author is based on his engagement with an important supplier of industrial PSUs.

The controlling needs for the LLC resonant converter used in an industrial power supply are stated in Chapter 4. In a first part of the chapter the derivation of a dynamic model based on the fundamental frequency approach is presented. The results are analyzed and evaluated with respect to a PID-type controller design. Experimental results are shown. In a second part of the chapter the short-circuit robustness of the LLC resonant converter is analyzed and discussed. A new solution based on the resonant capacitor clamping method is described in detail and experimental results demonstrate the feasibility of the analysis and the method.

In Chapter 5 the optimal design of the LLC resonant converter with respect to the application is treated. Design constraints are defined and basic design trade-offs are formulated and analyzed. The numerical optimization method applied on the LLC resonant converter is proposed and demonstrated in this work. Therefore the numerical optimization solver used is described and applied on a simplified design example. Finally the numerical optimization procedure is applied on a concrete industrial design case, at which the considered loss models are parameterized from measurements of proven industrial components. The results of this design case optimization are analyzed and general design facts are concluded.

Chapter 6 addresses the parallel operation of LLC resonant converters. This is of special interest for low output voltages and resulting high output currents. Combined with an interleaved operation of the paralleled LLC converters the current ripple cancellation effect distinctively reduces the required ripple current rating of the output filter. The chapter analyzes the problem of the load sharing mismatch between such interleaved operated LLC converters and proposes a workaround suitable for application in industrial power supplies.

2 DC-DC Converters within Industrial IT Power Supplies

2.1 Requirements

2.1.1 Architecture of IT Power Supply Systems

The services offered by IT systems to institutional, industrial and private customers are generally sensitive to interruptions. One fact is that computers typically use volatile memory, i.e. Random Access Memory (RAM), to store data that is currently processed by algorithms or edited by users. Interruptions in the power supply of the computer would result in loss of this data and further in the need of restarting the algorithms and redoing the latest operations. Further points are the interruption of communication services like a cell phone call or the communication via a social network, and the services offered by upcoming cloud computing possibilities. Therefore the interruption of IT services typically generates additional costs or income reductions for the service provider. In consequence one key factor for the architecture of IT power supply systems is the robustness against voltage dips or outages of the national AC power grid. The maximal allowed occurrences of voltage dips in a national power grid for example is defined in the norm EN-50160 for the European Union. The allowed likelihood generally decreases with the duration and the percentage of the voltage dip.

Depending on the IT service offered several configurations of voltage back-up infrastructure exist. For long-term voltage back-up in the range of multiple minutes and hours fossil fuel powered generators are typically used to protect data centers or central network hubs located in a dedicated facility. For mid-term voltage back-up in the range of multiple milliseconds up to several minutes batteries are commonly used. For data-centers with gasoline back-up generator the batteries need to supply the IT loads until the gasoline generators have been started and taken over the supply. For small data centers, minor important network hubs or radio substations, the batteries need to supply the loads for the entire grid outage duration. The amount of installed battery capacity thereby depends on the service provider and its approximation of severity and likelihood of service interruptions.

The arrangement of the battery back-up within an IT power supply system can be done in different ways. In case the back-up is connected on the AC side of the power supply it is commonly called a UPS (Uninterruptible Power Supply) system. UPS systems are popular for small enterprise installations since they are universal and easy to install. A UPS just needs to be plugged in between the AC supply and the AC inlet of the IT power supply system. In higher scale and higher power installations a UPS system is not cost effective, since the AC voltage back-up by a DC battery voltage requires an additional AC-DC and DC-AC converter stage. A popular more cost effective method exists by connecting the battery directly or via an additional DC-DC converter to an intermediate DC voltage of a power supply system. In general the two possibilities of a DC back-up path designated 1 and 2 in Fig. 2.1 exist. Path 1 connects the battery to the DC-link of the PSU. In such case the PSU output voltage can be regulated independently on the battery voltage by adjusting the DC-DC voltage gain. A direct connection of the PSU output voltage to a 12 V load would also be possible, thereby omitting the intermediate bus converter (IBC). Path 2 connects the battery to the PSU output voltage. Because the battery voltage depends on the state of charge (SOC) of the battery, the connection of a 12 V load with tight input voltage range requirements requires an additional IBC. In

case of mobile base stations the Radio is usually able to work with an input voltage range that fits to the battery voltage range.

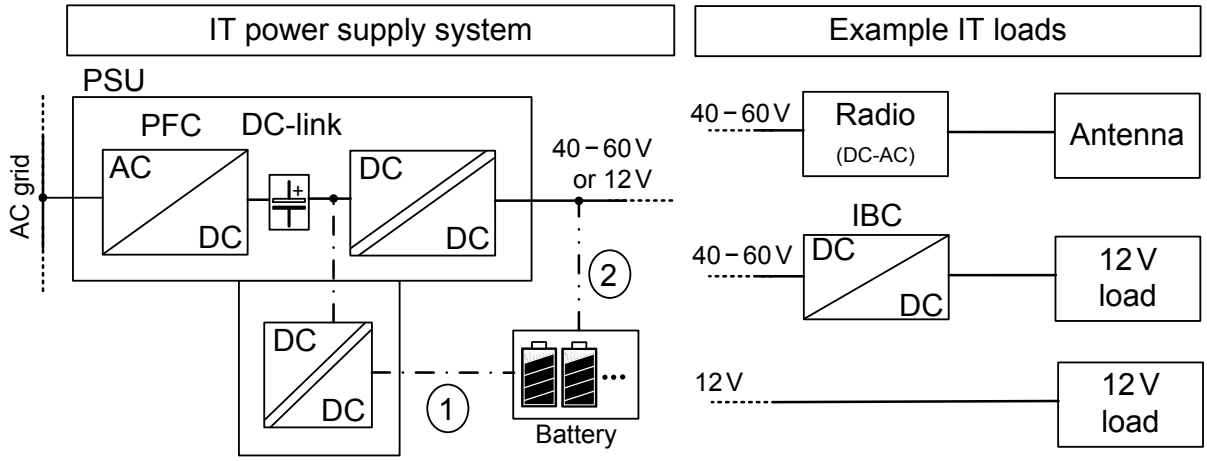

Fig. 2.1: General block diagram of an IT power supply system with two different battery back-up arrangements 1 and 2 (left) and exemplary IT loads (right). The voltage range 40 – 60 V is a typical voltage level that minimizes the distribution conductor cross section requirements at a still nonhazardous voltage level.

A further aspect of a highly reliable IT power supply system is the redundancy with respect to failure of the power electronics hardware. This requirement is met by building clusters of paralleled PSUs like shown in Fig. 2.2 with for example

$$\sum_{n-1} P_{\mathrm{o,PSU}} = \sum_{m} P_{\mathrm{i,load}} \,. \tag{2.1}$$

PSUs for mobile phone Radios may be not necessarily clustered due to installation space restrictions and the fact that mobile phone radio cells have already a certain degree of overlapping, and thus exhibit redundancy by a multiple number of Radios installed in a certain region.

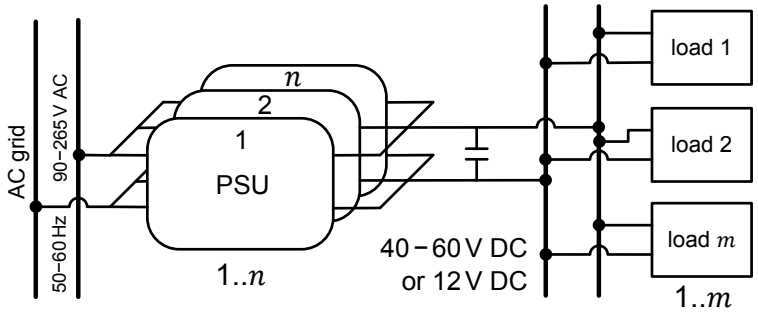

Fig. 2.2: Clustering of PSUs for redundancy with respect to PSU hardware failures

2.1.2 Performance Characteristics of the DC-DC Converter

The DC-DC converter within the PSU needs to establish galvanic isolation according to regulations and standards like the IEC-60664. Hence it needs to be equipped with an isolation transformer. Further requirements are

- Control of a constant output voltage with respect to load variations
- Control of a constant output voltage with respect to input voltage variations
- Short-circuit robustness of the output
- Controlled output current and power limitation
- Maintained voltage regulation at light and zero load
- Low emission of electromagnetic energy for EMC compliance of the PSU
- Highly efficient operation due to typically 24 hours operation per day

The input voltage V_i of the DC-DC converter depends on the charge status of the DC-link capacitor C_DL. The DC-link capacitor has the function of buffering the actual power difference between the power delivered by the PFC stage and the power consumed by the DC-DC converter. The following reasons for an actual power difference can be stated:

- The PFC stage power delivery has the form of a rectified sinusoidal waveform due to its nature of operation, whereas the DC-DC converter draws power according to the load requirements. The DC-link voltage controller of the PFC stage ensures that the average values of both powers are equal by adjusting the average power delivered by the PFC stage. The alternating power delivery of the PFC stage leads to an alternating voltage superimposed on the DC-link voltage and having a fundamental frequency that is twice that of the AC grid voltage.
- In case of an AC voltage outage the PFC stage delivers zero power. This leads to decreasing of the DC-link voltage. The output loads can be supplied from the energy stored in the DC-link capacitor as long as the DC-DC converter tolerates the reduced input voltage by increasing its DC-DC gain $M_\mathrm{oi} = V_\mathrm{o} / V_\mathrm{i}$. The time difference between the AC voltage outage and the minimum DC-link voltage tolerated by the DC-DC converter is defined as and commonly called hold-up time T_HU. The status of AC voltage outage but simultaneous supplied output loads by the energy stored in the DC-link capacitor is called hold-up condition. The hold-up capability of a PSU is typically designed and used to bridge the outage of one half or one entire AC period, since those events have a sensitive likelihood. By utilizing the DC-link capacitance in the described way, the life-time of the back-up batteries can be optimized.
- In case of a lightning surge pulse on the AC power line the excess energy is commonly transferred into the DC-link capacitor which leads to a fast increase of the DC-link voltage. The output voltage can be maintained as long as the DC-DC converter tolerates the increased input voltage V_i by decreasing its DC-DC gain M_oi.
- Since the dynamic load variations are typically much faster than the power control of the PFC stage, huge changes of the output loading lead to over- resp. undershoots of the DC-link voltage.

The aforementioned points lead to the requirement of a valid input voltage range for the DC-DC converter given by the minimum and maximum input voltage $V_\mathrm{i,min}$ and $V_\mathrm{i,max}$. The set-value of the DC-link voltage controller is defined as the nominal input voltage $V_\mathrm{i,nom}$. The DC-DC converter is operated to a major part of its operating time in the vicinity of $V_\mathrm{i,nom}$. In

consequence the optimization of the efficiency of the DC-DC converter should focus on the case $V_i = V_{i,nom}$.

The desired output voltage characteristic of the DC-DC converter in case of a battery backup according to back-up path 2 (c.f. Fig. 2.1) is shown in Fig. 2.3. The nominal voltage $V_{o,nom}$ should be maintained by the converter over the entire load range $I_o = [0.. I_{o,nom}]$. The output power limitation range of $P_o = P_{o,max}$ at $I_o = [I_{o,nom}..I_{o,max}]$ is defined by the battery voltage range given by $V_o = [V_{o,min}..V_{o,nom}]$. By supplying the maximal output power $P_{o,max}$ even at the minimum battery voltage $V_{o,min}$, the power capability of the PSU is utilized to full extend in the following case: If the battery charge power plus the load power demand is higher than $P_{o,max}$, the decrease of V_o limits the battery charge power such that the charge power is the exact difference between $P_{o,max}$ and the load power. This method ensures the fastest recharge time of the batteries and is therefore a typical requirement of industrial power supplies with back-up path 2. The maximum output voltage $V_{o,max}$ is an optional requirement and demanded for higher flexibility with respect to different load or battery configurations.

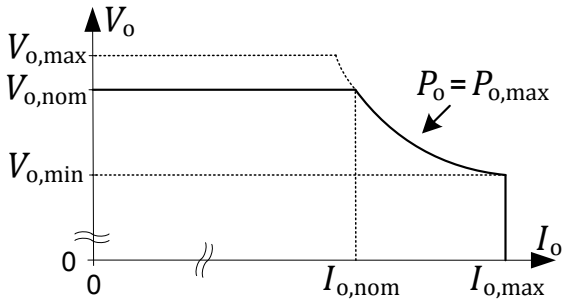

Fig. 2.3: Beneficial output characteristic of a PSU for supplying a DC bus that has a battery back-up connection.

The input and output voltage ranges effectively translate into the normalized DC-DC gain range requirement

$$M_{min} = k_{br}\frac{nV_{o,min}}{V_{i,max}} \quad < \quad M_{nom} = k_{br}\frac{nV_{o,nom}}{V_{i,nom}} \quad < \quad M_{max} = k_{br}\frac{nV_{o,max}}{V_{i,min}}. \qquad (2.2)$$

For IT power supplies comprising back-up path 1, the output voltage range could be very small, whereas the DC-DC gain range requirement decreases accordingly.

Due to million dollar scale investment requirements of large data-center owners for acquiring PSUs, the bill of material of the PSU needs to be as low as possible but the reliability needs to be sufficient. Typical life-times of PSUs in data-centers are 3 – 5 years and of PSUs for telecommunication applications up to 10 years and more. However, the reliability topic is strongly linked to the matter of compromise between component quality respectively rating and costs. It is therefore difficult and not in the scope of this work to rate a certain topology with respect to its reliability.

2.2 State of the Art

2.2.1 Topology and Design

Among a multitude of potential converter topologies for building up a DC-DC converter, the dominant converter topologies used for industrial IT power supplies in the past decade were the 2-transistor forward converter (2-TF) (e.g. [Erickson], [Walker]) and the phase-shifted full-bridge converter (PSFB) (e.g. [Erickson][5], [Badstuebner2]). The 2-TF converter is known for its robustness[6], whereas the PSFB converter can be operated in soft-switching ZVS mode yielding higher conversion efficiency due to lower switching losses. Both converter types operate with constant switching frequency in PWM mode and can be controlled in well-known, robust and industrial proven peak-current mode, also called current programmed control in [Erickson], [Sheehan]. The adoption of the PSFB converter topology in industrial IT PSUs was driven by higher efficiency and power density requirements. Meanwhile the LLC resonant converter is adopted in the industry based on even higher efficiency and power density requirements, which can be verifiably addressed by the LLC converter (c.f. Chapter 2.2.2). An interesting point is that the beneficial characteristics of the LLC resonant converter with respect to its application within an industrial IT PSU has been known since many years [Huang]. The reason for the late adoption of the topology in industry can be at least partwise justified by the relative complex design and variable switching frequency control requirement. Examples for the complexity of the design and control can be found in many publications (e.g. [Beiranvand], [Adragna], [Binder], [Feng], [Fang3], [Feng3], [Fu], [Oeder4], [Wang]). It can be appraised that the overall complexity and unusual variable frequency control has inhibited the easy adoption of the topology in industry.

This work extends the state of the art with respect to the industrial application of the LLC resonant converter on the following fields:

- Converter modeling
  The exact time domain solution method is extended by the normalized factor d to account for resistive losses within the resonant circuit. This improves the comparability between different design variants, the prediction of the DC-DC gain and facilitates the normalized description of the load-sharing characteristic between two paralleled LLC converters in interleaving configuration.
- Loss modeling
  The loss modeling of the inductive components of the LLC converter is realized by an analytical loss model that is parameterized by measurements on components which are constructed similar as the final components. This method circumvents the complicated analytical modeling of side-effects within real-world inductive components but approximates those effects by exemplary measurements.
- Converter design
  The numerical and automated converter design proposed in this work takes the absolute value of the working switching frequency f_s and its influence on the converter performance subject to all relevant constraints of an IT PSU into account.

[5] This book refers to the Full-bridge transformer-isolated buck converter

[6] Robustness reasons for the 2-TF converter: 1. The 2-TF contains no bridge leg that can directly short the input voltage in case of non-optimal or faulty bridge driving signals. 2. The magnetization of the transformer is securely reset in every switching cycle and thus core saturation is inherently prohibited.

- Converter control
  The compensator design takes the different plant characteristics of the LLC converter in dependence on the normalized switching frequency F_n into account, resulting in an adaptive compensator approach. Furthermore a new combined design and control method for realizing short-circuit robustness and output current limitation is proposed.
- Paralleling
  The different influences of operatin region and component value deviations on the load sharing beween interleaved operated LLC converters are revealed. A patented method for industrial application of paralleled LLC converters is demonstrated.

2.2.2 The Potential of the LLC Resonant Converter

The LLC resonant converter was recently adopted by industry for the application in industrial IT PSUs. Thereby it replaces gradually the commonly used PWM buck-type converters like the 2-TF and the PSFB. Therefore it is feasible to compare the performance characteristics of the LLC resonant converter with those of PWM buck-type converters [Zhao2]. A comparison to other variants of resonant converters, e.g. the LCC resonant converter [Pawellek], is not performed in this work and considered as a separate field of discussion.

Fig. 2.4 and Fig. 2.5 show the principal schematic of the LLC resonant converter respectively the PSFB converter. In order to distinguish the left-hand, i.e. the input side of the isolation transformer T_1 from its right-hand, i.e. output side, the common nomenclature of primary, i.e. input, and secondary, i.e. output side, is adopted in this work. On this note the schematics of Fig. 2.4 and Fig. 2.5 are drawn with a full-bridge on the primary side and a full-wave rectifier on the secondary side. Further typical possibilities on the primary side are the half-bridge configuration or the three-level configuration. On the secondary side typical possible variants for the LLC resonant converter are the center-tapped rectifier or the voltage-doubler rectifier. For the PSFB converter they are the center-tapped rectifier or the current-doubler rectifier. All different variants account for different current and voltage levels with respect to the ratings and availability of components and have to be selected in dependence on the concrete converter specification. For comparison between the converter variants the same input and output current and voltage levels have to be assumed, hence the same types of bridge and rectification should be considered.

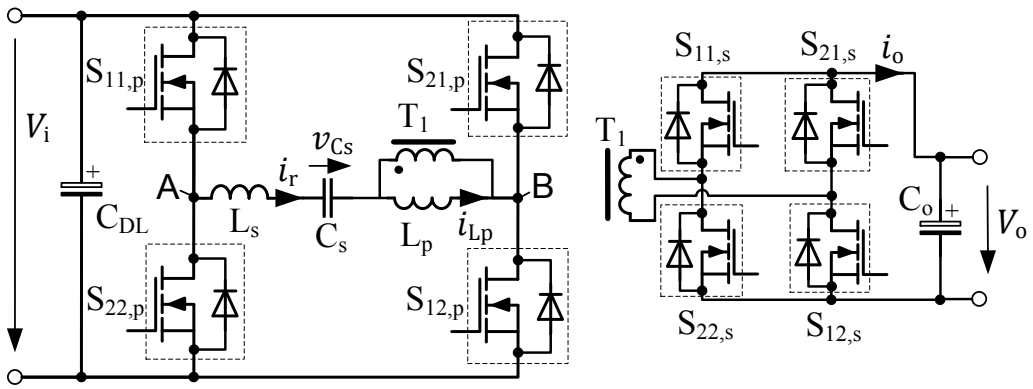

Fig. 2.4: Principal schematic of the LLC resonant converter, here drawn with a full-bridge on the primary side and a full-wave rectifier on the secondary side. Furthermore the rectifier is drawn in a synchronous rectification configuration, hence employing MOSFETs instead of diodes. All diodes drawn are meant as inherent body-diodes of the MOSFETs.

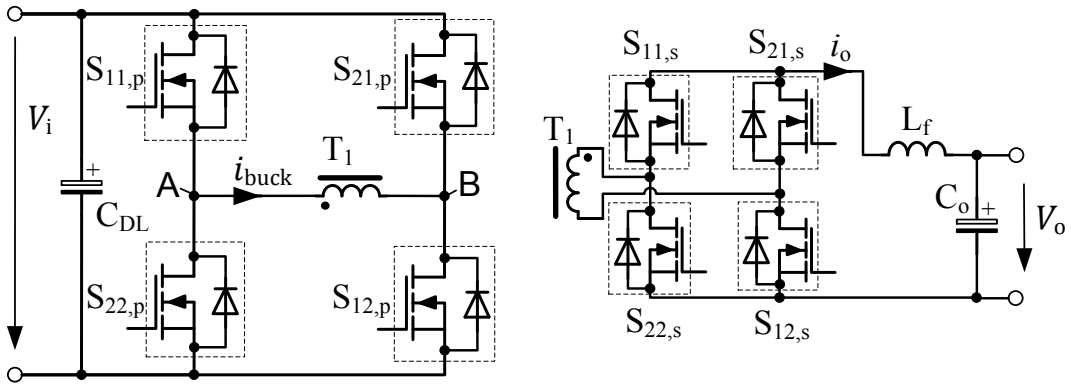

Fig. 2.5: Principal schematic of the PSFB converter, here drawn with a full-bridge on the primary side and a full-wave rectifier on the secondary side. Furthermore the rectifier is drawn in a synchronous rectification configuration, hence employing MOSFETs instead of diodes. All diodes drawn are meant as inherent body-diodes of the MOSFETs.

Besides of several differing details of the converters that result in industrial application with respect to construction and control, a comparison of major stress parameters is given in Table 2.1. The parameters are calculated based on the design example of Table 5.6, which is a typical IT PSU for battery back-up path 2. The parameters are the RMS current values on the primary side of the converters flowing between star points A and B ($I_{\mathrm{buck,RMS}}$ and $I_{\mathrm{r,RMS}}$), the turn-off switching currents of the full-bridge switches ($i_{\mathrm{buck,sw\_off}}$ and $i_{\mathrm{r,sw\_off}}$), the RMS current values on the secondary side that flow out of the rectifier into the output filter ($I_{\mathrm{o,RMS,PSFB}}$ and $I_{\mathrm{o,RMS,LLC}}$), and the blocking voltages of the rectifier switches ($V_{\mathrm{max\_rect,PSFB}}$ and $V_{\mathrm{max\_rect,LLC}}$). The calculation is based on the following assumptions:

- All components are ideal.
- The filter inductor L_f of the PSFB converter is designed such that its peak-to-peak ripple current is 20% of the nominal output current $I_{\mathrm{o,nom}} = 3\ \mathrm{kW} / 54.5\ \mathrm{V} \approx 55\ \mathrm{A}$.
- The RMS value of the resonant current i_r of the LLC converter is described by (5.8) with sufficient accuracy for the purpose of the comparison.
- The RMS value of the rectified current i_o of the LLC converter is described by the crest-factor of a sinusoidal waveform with sufficient accuracy for the purpose of the comparison.

Table 2.1: Comparison of selected electrical stress parameters between buck-type PWM and the LLC resonant converter. Values in brackets result for the special case $M_{\mathrm{nom}} = M_{\mathrm{max}} = 1$.

Output loading	$I_{\mathrm{buck,RMS}}$/A	$I_{\mathrm{r,RMS}}$/A	$i_{\mathrm{buck,sw\_off}}$/A	$i_{\mathrm{r,sw\_off}}$/A
20%	1.9 (1.5)	1.7 (1.7)	3.4 (2.2)	0.38 (0.38)
60%	5.5 (4.4)	5.0 (5.0)	8.0 (5.1)	0.38 (0.38)
100%	9.2 (7.3)	8.3 (8.3)	12.6 (8.1)	0.38 (0.38)

Output loading	$I_{\mathrm{o,RMS,PSFB}}$/A	$I_{\mathrm{o,RMS,LLC}}$/A	$V_{\mathrm{max\_rect,PSFB}}$/V	$V_{\mathrm{max\_rect,LLC}}$/V
20%	11.5 (11.5)	12.2 (12.2)	85.4 (54.5)	54.5 (54.5)
60%	33.2 (33.2)	36.7 (36.7)	85.4 (54.5)	54.5 (54.5)
100%	55.1 (55.1)	61.1 (61.1)	85.4 (54.5)	54.5 (54.5)

The comparison yields the following major points:

- The RMS current values flowing in the primary side of the transformer are comparable, where the exact difference depends on the requirement for $M_{\max}$ as indicated by the bracketed values for $M_{\max} = 1$. The LLC converter has a disadvantage since the same current has to flow through the additional components L_s and C_s compared to the PSFB converter.
- The turn-off switching currents are distinctively, i.e. more than 10 times higher for the PSFB converter as compared to the LLC converter.
- The RMS current value flowing in the output rectifier is slightly higher for the LLC converter as compared to the PSFB converter. Simultaneously the blocking voltage of the output rectifier devices is lower, such that devices with higher current ratings and lower conduction losses can be selected. The PSFB converter has a disadvantage since the rectified current has to flow through additional component L_f compared to the LLC converter.

Further points not represented by the numbers of Table 2.1 are:

- As a matter of fact the resistance especially of the inductive components increases with increasing frequency of the harmonic component of the current (c.f. Chapter 3.2.3.2). Because the resonant and output current waveform of the LLC converter have sinusoidal and those of the PSFB have rectangular shape character, the LLC converter has the advantage of less content of high order harmonic numbers with respect to the currents flowing in the main power path.
- The resonant inductor L_s in the main power path of the LLC converter limits the commutation current slope for the output rectifier. This is an advantage of the LLC converter since the reverse recovery losses of the rectifier devices are lower at reduced current slope during commutation.

The appraisement of afore listed points with respect to the overall performance of the converter within an IT PSU may depend on further construction and device details. But as a most obvious and clear difference the turn-off switching currents for the primary bridge can be pointed out as a key advantage of the LLC converter with respect to the converter efficiency. According to [Semdisc] the ZVS switching losses of a modern super-junction MOSFET with nominal $R_{DS(on)}$ of 70 mΩ increase from 2 µJ at 0.4 A to 116 µJ at 8 A. Hence, the difference in ZVS switching losses between the above treated LLC and the PSFB converter at a moderate switching frequency of e.g. $f_S = 80$ kHz is 9.12 W, which is an additional loss of 0.5% at 60% output loading.

The difference in turn-off switching currents between the PSFB and the LLC resonant converter is explained by the L_s-C_s series resonant circuit of the LLC converter. In this resonant circuit the resonant capacitor C_s acts as an inherent and smooth current commutator[7] (c.f. Fig. 3.3), whereas in the PSFB converter the current needs to be commutated completely by the switching devices. This characteristic enables the LLC resonant converter as well for high switching frequency application with the potential of reaching a very high power density due

[7] At switching frequencies higher than the L_s-C_s resonance frequency the natural commutation by the resonant capacitor C_s is the more earlier interrupted by the switching action of the bridge the higher the switching frequency is (c.f. Fig. 3.3). Since the preferred operating region of the LLC converter is typically close to the resonance frequency, the natural commutation by the resonant capacitor C_s is typically utilized to a high extend in nominal operating conditions.

to less voluminous passive components of the converter and the EMI filters. A further advantage of the LLC converter with respect to high switching frequency application is that the stray inductance of the transformer is utilized as a beneficial element as part of the resonant inductance L_s. In contrast for the PSFB converter the stray inductance increases the voltage stress of the rectifier devices and therefore is not beneficial but leads to the need of additional snubber networks ([Redl1], [Redl2], [Redl3]). However, high switching frequency application in the range of several hundred kHz to 1 MHz typically yields distinctive lower electrical efficiency caused by higher switching and driving losses. The efficiency optimum of typical IT PSUs is found below 100 kHz switching frequency, which is shown by the optimization results presented in Chapter 5. An overall evaluation of the compromise between converter efficiency and power density is subject to a multi-objective optimization ([Kolar2], [Biela3]) and not performed in this work.

3 Analysis and Modeling of the LLC Resonant Converter

3.1 Modeling of the Converter Operation

3.1.1 Modeling Methods

The study of literature related to the modeling of power converters and especially of resonant power converters yields a very broad range of modeling methodologies, at which each methodology having varying degrees of success and ease of implementation. Moreover many of the modeling methodologies are based on relatively minor variations, or adaptations, of previously documented techniques. A document giving a comparison of publicized modeling methodologies is [Foster2]. This document states that "recently, there has been a proliferation in the number of publications addressing the simulation of resonant power converter systems". The methodologies chosen for this work have to be qualified for these tasks:

- To provide a mathematical tool that can predict the steady-state DC-DC gain of a LLC resonant converter and current and voltage waveforms with high precision. Additionally a low computational effort is demanded to limit run times of automated design routines using the tool. Moreover the tool should be applicable to the computer algebra programs Mathcad or Mathematica due to availability to the author.
- To predict the small-signal characteristic of the LLC resonant converter in order to facilitate the controller design.

Qualified modeling methods are:

- Sampled-Data Modeling
- eFHA (Extended Fundamental Harmonic Approach)
- EDF (Extended Describing Function) method
    - EDF with respect to only the fundamental harmonic (analytical solution)
    - EDF with respect to additional higher order harmonics (numerical solution)
- Exact time domain solution by numerical methods

Each method is described in the following:

Sampled-Data modeling

The Sampled-Data modeling technique is based on a discrete-time state-space model representation. It relies on the property of power electronics systems, that they can be described by a succession of different configurations of linear time invariant (LTI) systems. The transitions between the intervals of the LTI configurations are given by the switching actions of the semiconductor devices. Hence, the time domain behavior of a power electronic system can be described by

$$\begin{aligned} \dot{\boldsymbol{x}}(t) &= A_i \boldsymbol{x}(t) + B_i \boldsymbol{u}(t) \\ \boldsymbol{y}(t) &= C_i \boldsymbol{x}(t) + D_i \boldsymbol{u}(t) \end{aligned} \tag{3.1}$$

$$\text{for} \quad t_k + T_{k,(i-1)} < t < t_k + T_{k,i} \quad \text{with} \quad 1 \le i \le I\,.$$

Since a power electronic systems exhibits cyclic behavior it is feasible to set

$$T_{k,0} = 0 \qquad t_{k+1} = t_k + T_{k,I}\,. \tag{3.2}$$

To solve for the successive proceeding of the time intervals, the state vector $\boldsymbol{x}(t_k + T_{k,i})$ at the end of an interval must be solved with the state vector $\boldsymbol{x}(t_k + T_{k,(i-1)})$ from the beginning of the interval. The time domain solution is given by

$$\boldsymbol{x}\big(t_k + T_{k,(i-1)} + t\big) = e^{A_i\left(t-\left(t_k+T_{k,(i-1)}\right)\right)}\boldsymbol{x}\big(t_k + T_{k,(i-1)}\big) + \int_{t_k+T_{k,(i-1)}}^{t_k+T_{k,(i-1)}+t} e^{A_i\tau}B\boldsymbol{u}(\tau)d\tau\,. \tag{3.3}$$

Further unknowns are the transition time stamps $T_{k,i}$. One possible approach to find the transition time stamps is to proceed step-wise with a predefined time step Δt. After each time step the occurrence of a switching transition has to be checked for. In case a switching transition occurred, the time step needs to be decreased until the switching transition is exactly met. Then the process is continued with the new according set of system matrices. This method is described e.g. in [Hsiao]. To calculate the demanded steady-state DC-DC gain by this method further measures are necessary. One possibility, which has been used by [Bucher] to acquire the steady-state operating points of an LLC and LLCC converter, is to detect the steady-state condition during a transient simulation by testing for a continuous fulfilment of the condition

$$\boldsymbol{x}(t_{k+1}) = \boldsymbol{x}(t_k). \tag{3.4}$$

This method would be also possible by means of classical Spice based time domain simulation, but the time duration of the simulation runs would be higher by several orders of magnitude [Hsiao]. Also the sampled-data approach exhibits a certain amount of computational effort, i.e. calculation of the exponential matrix terms and searching for the switching instants, to find the steady-state solution of a given set of input parameters.

The small-signal characteristic could be acquired by the use of the virtual network analyzer (VNA) method based on a time domain simulation set-up. But since this method is extensive in terms of computational effort, alternative methods based on the sampled-data modeling are proposed in literature. Those methods rely on a complete discrete time description of the converter operation,

$$\boldsymbol{x}(t_{k+1}) = \boldsymbol{F}(\boldsymbol{x}(t_k), \boldsymbol{T}_k) \quad \text{s.t.} \quad \boldsymbol{c}(\boldsymbol{x}(t_k), \boldsymbol{T}_k) = 0\,, \tag{3.5}$$

in which $\boldsymbol{c}$ contains an implicit description of the switching instants vector $\boldsymbol{T}_k$ depending on $\boldsymbol{x}$. The small-signal behavior can be determined by the steps well known from the same process applied to the state-space averaging method (SPAM): Perturbation of a steady-state condition, linearization, and evaluation in the frequency domain. The application has been demonstrated by [Elbuluk], [Verghese], [Stahl3] on a series resonant converter and by [Forsyth2] on a LCC resonant converter. [Stahl] stated that the application on the LLC converter is in principal possible but of high effort. Instead he proposed an alternative method that uses a time domain simulator to find the small-signal derivatives of the state-variables. A complete solution of the sampled-data modeling for the LLC converter yet is not known from literature.

eFHA

The eFHA method is reported several times in literature. The method is intended to increase the accuracy of the FHA (c.f. Chapter 3.1.6) approach – which in fact is not sufficient for performing converter designs – for converters exhibiting third order resonant circuits such as the LCC [Forsyth] and LLC [Foster3] resonant converter. The poor accuracy of the FHA approach especially in case of third order resonant converters is due to the interaction of the resonant element connected in parallel to the XFMR (C_p for LCC and L_p for LLC) with the output rectifier. This leads to a difference of the transformer voltage to an ideal square wave voltage or an ideal sinusoidal voltage, respectively, and hence to a distinctive modeling error. The eFHA approach takes the non-ideal transformer voltage into account by extracting the fundamental harmonic of the exact time domain transformer voltage in dependence of the output voltage and current of the rectifier. The value of this fundamental harmonic is then used to calculate an equivalent impedance that can be used to execute the circuit calculations by standard AC circuit theory. Nevertheless, also the eFHA approach typically requires numerical solving of at least one transcendental equation if operating modes exhibiting discontinuous quantities are examined.

A substantial assumption of the eFHA approach is that the resonant current is perfectly sinusoidal. This assumption is qualified in case of the LCC resonant converter, so that the eFHA method yields quite accurate results throughout a wide operating region [Forsyth]. In [Foster3] the eFHA method is applied to the LLC resonant converter. The proposed equations of this paper were examined in [Oeder3] in terms of accuracy. Whereas the error of the DC-DC gain is to a certain extent acceptable, very high errors are found in the predicted peak values of the resonant voltage and current. One reason for the modeling error is the non-sinusoidal resonant current of the LLC converter especially at switching frequencies much lower or higher than the resonant frequency. In consequence the eFHA approach is not suited as a modeling method for the LLC resonant converter if applied like in [Foster3]. Furthermore it is not known how to extend the eFHA model by resistive losses, which is an additional modeling feature increasing the accuracy of a design process.

Generally it is possible to get the small-signal characteristic from the eFHA model, but no reported validation for the LLC converter is known from literature.

EDF

The EDF method combines the state space representation of the converter model with the frequency domain representation of the converter waveforms, thereby using Describing Functions [Gelb] to treat the nonlinearities of the state space model. The primal goal of the EDF method is the calculation of the converters small-signal characteristic, but steady-state DC-DC gain calculations are also conditionally possible. Basically two classes of EDF modeling techniques relevant to the modeling of resonant converters are known:

The first class uses not more than the DC components of the slow varying state variables and the fundamental harmonic of the fast varying state variables to build the converter model. This type of modeling has been demonstrated for the series resonant converter in [Sanders], for the LCC resonant converter in [Maas] and for the LLC resonant converter in [Tian] and [Foster4]. This modeling approach has the following attributes:

- the converter model and the small-signal characteristics can be derived analytically
- the converter model includes the steady-state solution and therefore the DC-DC gain characteristic
- effects of higher order harmonics are not supported, resulting in limited model precision
- discontinuous state variables, like the LLC resonant current in the below resonant region or the LCC transformer voltage at heavy loads, are not supported, resulting in substantial modeling errors within the according operating conditions.

In consequence this modeling class is useful only for approximate but fast calculations of the DC-DC gain and the small-signal characteristic of the LLC converter. Operating points much higher or lower than the resonant frequency, e.g. the DC-DC gain calculations for the hold-up condition, are not modeled with sufficient precision by this technique. The approximate small-signal characteristic can be used for the initial, not yet optimized controller design.

The second class of EDF modeling techniques (EDF-2) uses also higher order harmonics of both the slow and the fast varying state variables in order to predict the small-signal characteristic of the converter as precise as possible. The number of considered harmonics depends on the required modeling precision and can be appropriately chosen. However, the consideration of higher order harmonics usually leads to a highly involved mathematical model including implicit nonlinear equations. Solving the resulting model analytically is impossible in probably all cases.

An enhancement of the EDF-2 method is the method of [Groves]. Here it is found that the prediction of the small-signal characteristic including the effects of higher order harmonics is possible, but the exact steady state solution of the corresponding operating point must be known in advance. This method was adapted by [Yang], thereby introducing simplifications that can be used if accurate prediction of the small-signal characteristic is only required for modulation frequencies up to the Nyquist frequency (i.e. half the switching frequency). Furthermore [Yang] demonstrates a systematic implementation of the proposed EDF modeling technique into a computer program (documented by Matlab m-files). The required inputs of the computer program are the piecewise-linear state equations of the corresponding operating mode, and, as already stated, the steady state solution of the corresponding operating point. The EDF-2 method is applied on the LLC resonant converter in [Yang3].

This modeling approach has the following attributes:

- the steady-state solution must be found in advance by numerical methods
- once the steady-state solution is known the small-signal characteristics can be derived with low computational effort
- effects of higher order harmonics are well supported, resulting in high model precision
- discontinuous state variables, like the LLC resonant current in the below resonant region or the LCC transformer voltage at heavy loads, are well supported, resulting in precise predictions of the small-signal characteristics.

Generally both EDF modeling techniques support the consideration of resistive circuit elements without considerable extra effort. None of both supports the exact calculation of the steady-state DC-DC gain.

Exact time domain solution

The exact time domain steady-state solution of a resonant converter can be achieved by solving the nonlinear system of equations that can be deduced from the mathematical converter model. This method has been demonstrated in [Lazar] for the LLC resonant converter and in [Kunze], [Kirchenberger] for the LCC resonant converter. The solving algorithm can be implemented in Mathematica or even Mathcad because both programs are able to solve a nonlinear system of equations by Newton's method.
A disadvantage of this method is that for every operating mode a separate system of equations exists, and that in some operating areas the according operating mode is not known in advance. A complete steady-state modeling of the LLC converter therefore requires the consideration of every possible operating mode and the boundaries between them. Such a comprehensive analysis can be found in [Yu2]. Generally it is not possible to extract the small-signal characteristic from this modeling method, so that it can only be used for steady-state calculations.
The direct steady-state calculation method described above has not yet been demonstrated for converter models including resistive elements, so that resistive loss effects on the steady-state characteristic are not included in the solution. This will be presented in this work by introducing the damping factor d (c.f. Chapter 3.1.3).

Concluding the presented investigation of LLC design methods, the deductions for modeling the LLC resonant converter in order to facilitate a reliable converter design are:

- Use the exact time domain method to derive the steady-state and DC-DC gain characteristics, thereby expanding the existing model by resistive elements
- For an initial, non-optimized controller design, use the EDF modeling method based on the fundamental frequency, like in [Maas]; The EDF-2 modeling method according to [Yang] was applied on the LLC converter under the author's supervision in [Schmidt], but no reliable results were achieved. For optimized, highly precise controller design, it is therefore suggested to acquire the plant's small-signal characteristic by measurement. The measured result also includes further parasitic effects, which would be difficult to be covered by the circuit model.

3.1.2 Operating Mode Analysis of the Ideal LLC Converter

In case of resonant converters the resonant circuit interacts with the semiconductor bridge on the input side and the rectifier on the output side, where the switching instants of the semiconductors are typically unknown because they are implicit functions of the state variables. This dependency of the switching instants from the state variables leads to the occurrence of several operating modes. In case of the LLC resonant converter 7 operating modes exist, which were investigated in [Lazar] and are summarized in Table 3.1. Additionally the resulting switching condition (ZVS/ZCS, c.f. Chapter 3.1.7) for an ideal bridge is given. At modes exhibiting both switching conditions the valid switching condition depends on the circuit and actual input and output parameters.

Table 3.1: Operating Modes of the LLC resonant converter

Acronym	Operating Mode	Bridge Mode
CCMA	Continuous Conduction Mode Above Resonance	ZVS
DCMA	Discontinuous Conduction Mode Above Resonance	ZVS
CCMB	Continuous Conduction Mode Below Resonance	ZVS or ZCS
DCMB1	Discontinuous Conduction Mode Below Resonance 1	ZVS or ZCS
DCMB2	Discontinuous Conduction Mode Below Resonance 2	ZVS
DCMAB	Discontinuous Conduction Mode Above and Below Resonance	ZVS
Cutoff	Cutoff Mode Above and Below Resonance	ZVS

For calculating the steady state of the LLC converter in every operating mode, each operating mode needs to be treated with a separate model. Moreover adjacent operating modes and the boundaries between them need to be specified. In [Yu2] a comprehensive summary and analysis of all operating modes is given. In this work only the operating modes CCMA and DCMB2 are presented, since these operating modes are active in a major operating range of a typical applied LLC converter. Referring to the interested application of a server or telecom PSU, at least all operating points in the upper half of the output power range can be addressed by these modes. In Fig. 3.1 the sequences of operating modes in dependence on the output loading are illustrated. In the above resonance region $F_\mathrm{n} > 1$ the CCMA mode is the full load mode, and the DCMA and DCMAB modes occur at light output loadings. In the below resonance region $F_\mathrm{n} < 1$ the DCMB2 mode is the desired full load mode and the DCMBAB mode as well the light load mode. The CCMB mode is avoided by proper design of the LLC converter, because the desired ZVS condition cannot be achieved in this mode. The noted ZVS property of the CCMB mode exists only in a very limited operating range and is typically not valid for a real converter exhibiting parasitic elements (c.f. Chapter 3.1.7). The DCMB1 mode is kind of a transition mode between the CCMB and DCMB2 mode. Its ZVS condition is also critical in case of a real converter. The DCMB1 mode therefore gives the bounding area of the desired operating region but has no significant share of it.

The below resonance region $F_\mathrm{n} < 1$ comprises the areas $F_1 < F_\mathrm{n} < 1$ and $F_\mathrm{n} < F_1$, where F_1 is defined by means of the FHA analysis (c.f. Chapter 3.1.6) and therefore approximate with respect to the prediction of the peak gain point. According to the FHA analysis ZVS is not possible in the area $F_\mathrm{n} < F_1$ independent on the load condition. The FHA analysis also reveals that the peak gain $M_\mathrm{pg}(Q)$ occurs at least very close to the ZVS/ZCS boundary according to Fig. 3.8. The translation of these FHA characteristics into the exact time domain behavior is however only approximate and requires additional verification. In [Fang2] it is claimed that the peak gain based on the exact time domain behavior occurs in DCMB1 or CCMB mode, justified by the assumption that the peak gain represents exactly the ideal ZVS/ZCS boundary. Since this claim cannot be mathematically supported this work is based on the following line of reasoning:

- The peak gain is at least close to the ideal ZVS/ZCS boundary.
- The ideal ZVS/ZCS boundary has limited practical evidence, since the ZVS/ZCS boundary of a real converter is influenced by parasitic elements introducing additional transients at the switching instant (c.f. Chapter 3.1.7)
- Simulation reveals that the DC-DC gain $M(F_\mathrm{n})|_Q$ is at least monotonic in the DCMB2 mode. It is therefore feasible to define that the peak gain $M_\mathrm{pg}(Q)$ is given by the DCMB2 to DCMB1 mode boundary.

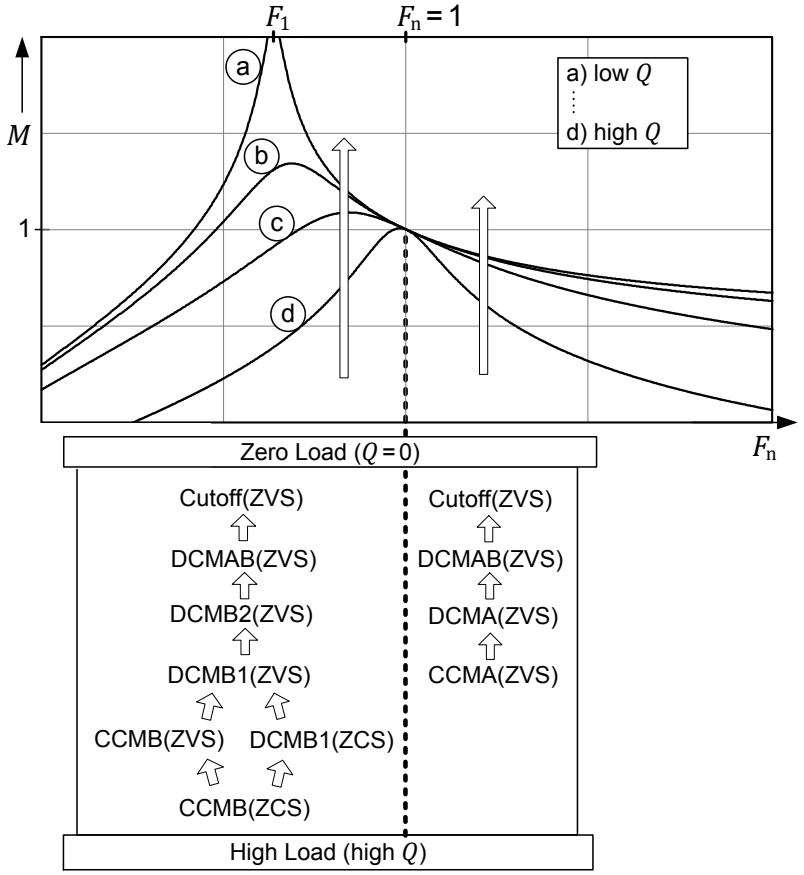

Fig. 3.1: Illustration of the sequencing of operating modes in dependence on the output loading. The sequences are valid for the frequency ranges $F_1 < F_n < 1$ and $F_n > 1$ respectively. The DC-DC gain curves are derived here by means of FHA approximation (c.f. Chapter 3.1.6).

3.1.3 Proposed Model Extension

As a matter of fact the complexity of a converter model depends strongly on the number of parasitic elements included. Hence, it is reasonable to apply a compromise between model complexity and practical usability. The exact time domain modeling method was so far presented in literature only for the ideal LLC converter neglecting any parasitic effects. In [Bucher2] the exact time domain model was extended by loss considerations for the series resonant converter. But resistive voltage drops are considered by the average current flowing in the resistance and incorporated into the model via an equivalent drop of the DC-DC gain. This method yields improved results compared to the ideal model, but still suffers accuracy problems and makes the mathematical model representation more involved.

In this work the extension of the exact time domain solution by a single lumped resistor within the resonant circuit is proposed. Since the model is solved by numerical methods, the additional presence of damping does not affect the solvability of the model. On the one hand the consideration of resistive damping increases the prediction accuracy of the steady state DC-DC gain. On the other hand it is vital for the analysis of the load sharing between two LLC converters operating in parallel connection and with coupled switching frequencies according to Chapter 6.

Fig. 3.2 shows the equivalent circuit model comprising the additional damping represented by the resistor R_s. The voltage source v_{gAB} represents the feeding source voltage to the resonant circuit. Its polarity switches in accordance to the switching states of the semiconductor bridge.

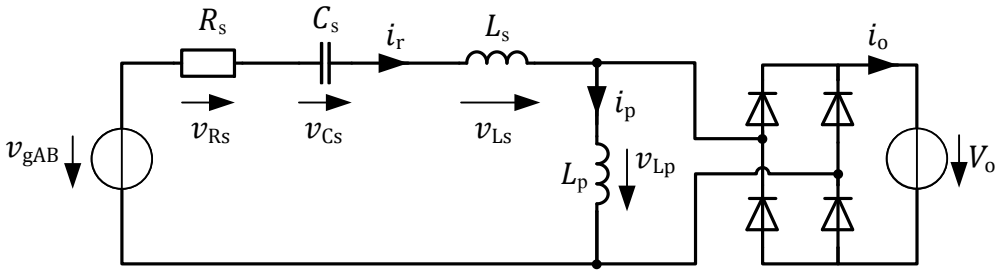

Fig. 3.2: Equivalent circuit model used to derive the steady-state model

In spite of the added damping, the proposed model still lacks properties of a real converter. In the following the most important differences are commented.

1. Core losses
   The core losses associated to the inductances L_s and L_p are expected to give the highest uncertainty to the model since those losses are in the same magnitude as the conduction losses. Modeling of core losses by means of lumped elements is not feasible due to the distinctive nonlinear characteristic of the core material. It is therefore not in the scope of this work to investigate the effect of core losses on the steady-state DC-DC gain characteristic of the LLC converter. As a practical approximation the core losses can be modeled by additional resistive damping, but in which the parametrization is involved and only valid for one single operating point.

2. Semiconductor Drain-Source capacitances
   These capacitances need to be recharged during a switching or voltage transition of the elements. The currents and voltages related to the recharge process are not covered by the model. The hereby introduced error increases with increasing switching frequency. Practical experience shows that the error is small if the LLC converter is operated near to its resonance frequency, i.e. within its preferred operating region.

3. Parts of the resistive damping are located on right hand side of L_p
   The resistances of the XFMR's output winding, the rectifier and the output current path are oriented on the right hand side of L_p, whereas R_s is oriented on the left hand side. By including those secondary sided resistances $R_{s,s}$ into R_s, i.e. $R_s = R_{s,p} + n^2 R_{s,s}$, a power loss error of approximately $n^2 R_{s,s} I_{p,RMS}^2$ results. This error affects the overall model accuracy at light load conditions, characterized in that $I_{r,RMS}$ is similar to $I_{p,RMS}$. At full load conditions, i.e. $I_{r,RMS} \gg I_{p,RMS}$, the modeling error is limited and therefore accepted throughout this work. It should be noted that the exact time domain method is also applicable if a second resistance $R_{s,s}$ is modeled on the right hand side of L_p. However, this leads to very lengthy equations for the nonlinear system of equations and therefore is not presented in this work.

4. Parts of overall resonant inductance L_s are located on the right hand side of L_p
   The current path on the right hand side of L_p exhibits a certain inductivity $L_{s,s}$, in particular the stray inductance of the XFMR and the current loop formed by the rectification arrangement. In case of a high output voltage and a moderate switching frequency, the ratio $L_{s,p} / L_{s,s}$ is typically high enough (~40:1 for the investigated converter of Chapter 5.3.3) to neglect the introduced modeling error by the assumption $L_s = L_{s,p} + n^2 L_{s,s}$. In case of a low output voltage of e.g. $V_o = 12$ V, this assumption must be considered as a source of modeling error.

5. Switching losses
   The switching losses in the LLC resonant converter are very low due to ZVS operation and therefore of negligible influence on the steady-state DC-DC gain.

6. Possible non-linearity of C_s, L_s and L_p
   The grade of non-linearity of capacitors and inductors can be considerably high as well as the resulting modeling error. For the magnetic components used in an LLC converter the non-linearity originating the core material typically is limited by the need for air-gaps to realize the required inductance. For the resonant capacitor, the use of highly linear MLCCs (Multi-Layer Ceramic Capacitors) is assumed, which is supported by nowadays industrial praxis.

3.1.4 Derivation of the Proposed Steady-State Model

The exact time domain solution method is based on the piecewise linear description of the converter operation according to (3.1). Instead of solving (3.1) by means of (3.3), (3.1) is transferred into the single differential equations (DEs) of the state variables, which are then solved for arbitrary initial values:

$$\boldsymbol{x}\left(t - T_{k,i-1}\right) = \boldsymbol{F}_i\left(t - T_{k,i-1}, \boldsymbol{x}\left(T_{k,i-1}\right)\right) \quad \text{with} \quad T_{k,i-1} < t < T_{k,i}\ ,\ t_\mathrm{k} = 0\ . \tag{3.6}$$

Considering the continuity of the state variables

$$\boldsymbol{x}\left(T_{k,i}\right) \equiv \boldsymbol{F_i}\left(T_{k,i} - T_{k,i-1}, \boldsymbol{x}\left(T_{k,i-1}\right)\right), \tag{3.7}$$

the cyclic behavior of the steady-state operation applying (3.2)

$$\boldsymbol{x}\left(T_{k+1,i}\right) \equiv \boldsymbol{x}\left(T_{k,i}\right), \tag{3.8}$$

and the symmetry of operation

$$\boldsymbol{x}\left(T_{k,i+I/2}\right) \equiv -\boldsymbol{x}\left(T_{k,i}\right), \tag{3.9}$$

a non-linear system of equation results given by (index k omitted):

$$\boldsymbol{x}(T_0) = -\boldsymbol{F}_{I/2}\left(T_{I/2} - T_{I/2-1}, \boldsymbol{F}_{I/2-1}\left(T_{I/2-1} - T_{I/2-2}, \ldots \boldsymbol{F}_1\left(T_1 - T_0, \boldsymbol{x}(T_0)\right)\right)\right). \tag{3.10}$$

(3.10) can be solved by numerical approximation methods like Newton's method. The success of the solver depends on the feasibility of the supplied starting values. If the solver does not converge, the starting values were not feasible or a solution does not exist. If the solver converges, the solution must be checked for concordance with the underlying physical model. Especially the periodicity of the trigonometric functions can cause physical incorrect solutions by π-fold phase shifts. The detailed measures of the solution testing are described in Chapter 3.1.5.

As stated in Chapter 3.1.2 only the modes CCMA and DCMB2 are considered in this work. The waveforms of the state variables i_r, i_p and v_Cs are shown in Fig. 3.3. Both modes exhibit two intervals $[t_0..t_1]$ and $[t_1..T_{\mathrm{s}/2}]$ per half of the switching period T_s. The intervals of the second half of the switching period are symmetrical to the first half. The sequences of equivalent circuit configurations according to Fig. 3.4 are:

DCMB2: (a)→(b)→(d)→(e) and CCMA: (a)→(c)→(d)→(f) .

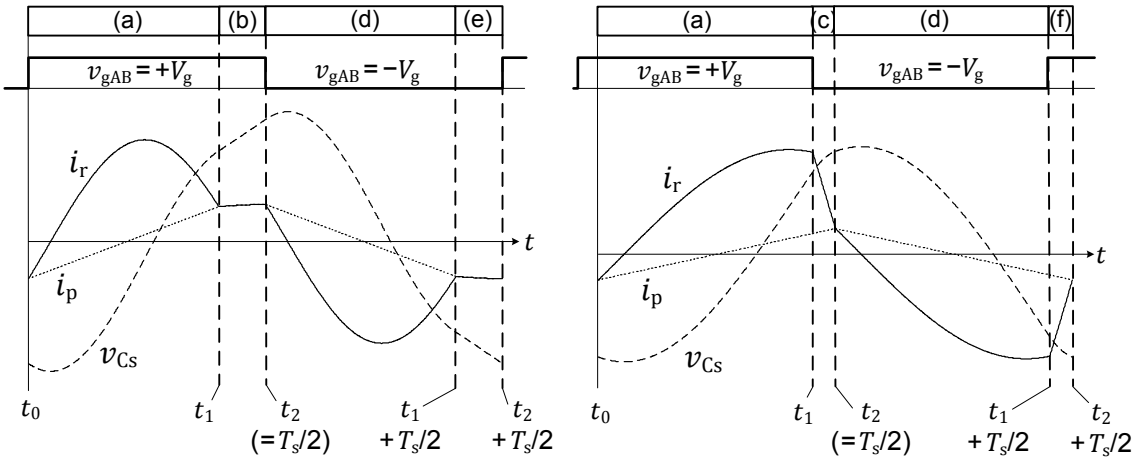

Fig. 3.3: Exemplary waveforms of the LLC's state variables in the operating modes DCMB2 (left) and CCMA (right).

The intervals (a) to (f) have the following description:

- (a), (d): The output rectifier is forward biased. Electrical energy is drawn from source voltage V_g and electrical energy is supplied to sink voltage V_o.
- (b), (d): The output rectifier is not forward biased. Electrical energy is drawn from source voltage V_g.
- (c), (f): The output rectifier is forward biased. Electrical energy is supplied to source voltage V_g and to sink voltage V_o.

Normalization is a common method in switching converter modeling. The normalized model is independent on the voltage, current and power levels of a concrete converter. Using the normalized circuit model, the analysis results, e.g. the DC-DC gain characteristic, can be easily denormalized and applied to any concrete LLC converter design. Common normalizations and characteristic values are summarized in Table 3.2 including the damping factor d, which is introduced to the exact time domain model in this work. The special naming convention regarding the characteristic frequency f_0, which is referred to as resonant frequency in the majority of the literature, is adopted and used throughout this work.

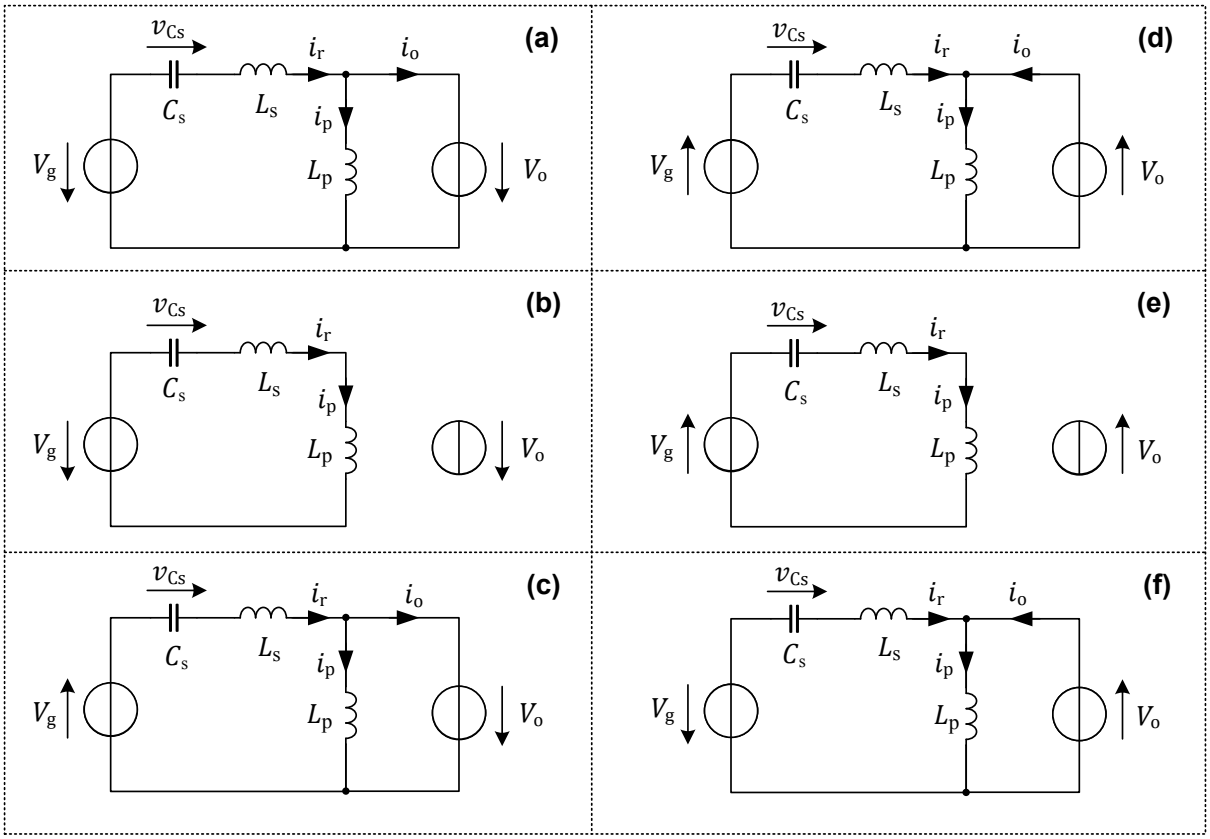

Fig. 3.4: Equivalent circuits of possible circuit configurations during intervals i of the piecewise linear description (3.1)

Table 3.2: Common normalizations and characteristic values of LLC converter parameters

Name	Value	Unit of measure
Inductance ratio	$h = L_p/L_s$	unitless
Characteristic impedance	$Z_0 = \sqrt{L_s/C_s}$	Ω
Characteristic angular frequency (here: resonant angular frequency)	$\omega_0 = 1/\sqrt{L_s C_s}$	s^{-1}
Characteristic frequency (here: resonant frequency)	$f_0 = \omega_0/2\pi$	s^{-1}
Characteristic period (here: resonant period)	$T_0 = 2\pi/\omega_0$	s
Normalized switching frequency	$F_n = f_s/f_0$	unitless
Normalized DC-DC gain	$M = nV_o/V_g$	unitless
Quality factor	$Q = Z_0/(n^2 R_L)$	unitless
AC quality factor	$Q_{ac} = \frac{Z_0}{\frac{8}{\pi^2}n^2 R_L} = \frac{Z_0}{R_{ac}}$	unitless
Time correspondent angle (normalized time)	$\theta = \omega_0 t$	unitless
Damping factor	$d = R_s/Z_0$	unitless

Voltage and current quantities are normalized using

$$m_x = \frac{v_x}{V_{\text{Base}}} \qquad j_x = \frac{i_x}{I_{\text{Base}}} \qquad I_{\text{Base}} = \frac{V_{\text{Base}}}{Z_0} \tag{3.11}$$

The normalization base voltage V_{Base} can be either the input voltage V_g or the reflected output voltage nV_o. This choice determines how to interpret the normalized output current J_o, which is the average value of the normalized output current $j_\text{o}(\theta)$:

$$I_\text{o} = \frac{2}{T_\text{s}} \int_{t_0}^{t_2} i_\text{o}(t)dt \qquad J_\text{o} = \frac{F}{\pi} \int_0^{\frac{\pi}{F}} j_\text{o}(\theta)d\theta \tag{3.12}$$

- $V_{\text{Base}} = nV_\text{o}$: In this case J_o is equal to the quality factor Q and designated as $J_{\text{o(Q)}}$. Assuming the input voltage V_g as a fixed quantity, the curves of constant J_o in the DC-DC gain diagram (c.f. Fig. 3.5) reflect a variable output voltage V_o at constant load resistance $R_\text{L} = V_\text{o} / I_\text{o}$. Another useful interpretation is a variable input voltage V_g assuming a constant output voltage V_o and constant output current I_o. The latter is equal to interpreting $J_{\text{o(Q)}}$ as the normalized output power $p_\text{o} = (V_\text{o} I_\text{o}) / (V_{\text{Base}} I_{\text{Base}})$.

- $V_{\text{Base}} = V_\text{g}$: In this case J_o is not the quality factor Q and designated as $J_{\text{o(I)}}$. Assuming the input voltage V_g as fixed quantity, the curves of constant J_o in the DC-DC gain diagram (c.f. Fig. 3.5) reflect a variable output voltage V_o at constant output current I_o, which originates the "I" in the proposed designation $J_{\text{o(I)}}$.

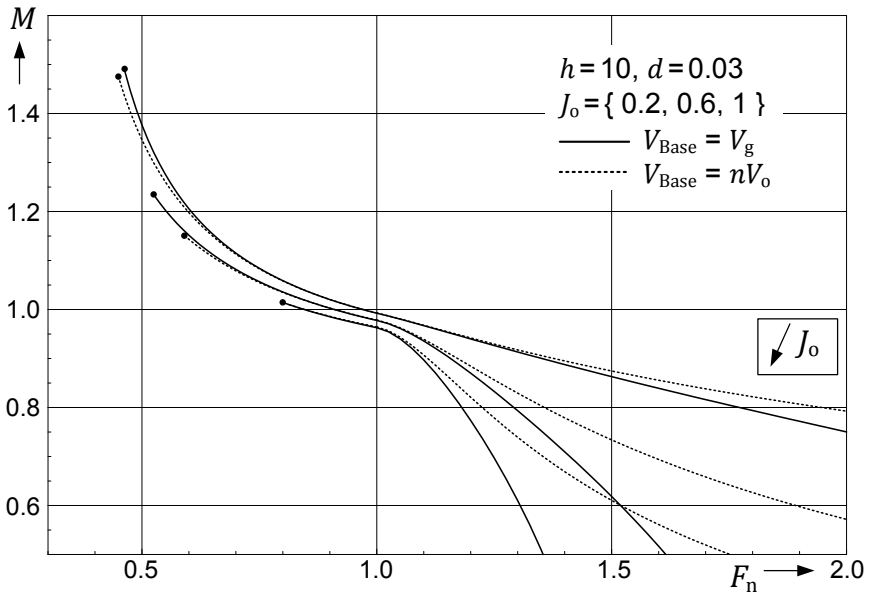

Fig. 3.5: Steady-state DC-DC gain diagram based on normalized parameters; Dots mark operating mode boundaries (here: DCMB2 to DCMB1) except at $F_\text{n} = 1$ (no dot).

In the following the single intervals of the DCMB2 and CCMA mode are described mathematically in the original as well as in the normalized form:

The first interval ($t_0 < t < t_1$) is identical in both modes. The DE describing the resonant current i_r in the first interval is

$$i_\mathrm{r}'' + \frac{R_\mathrm{s}}{L_\mathrm{s}} i_\mathrm{r}' + \frac{1}{L_\mathrm{s} C_\mathrm{s}} i_\mathrm{r} = 0 \qquad j_\mathrm{r}'' + d\omega_0 j_\mathrm{r}' + \omega_0^2 j_\mathrm{r} = 0\,. \tag{3.13}$$

The general solution of (3.13) is given by

$$i_\mathrm{r}(t) = K_{\mathrm{s}01} e^{\alpha t} \sin(\beta t) + K_{\mathrm{c}01} e^{\alpha t} \cos(\beta t)\,. \tag{3.14}$$

The resonant capacitor voltage is derived by

$$v_{\mathrm{Cs}}(t) = \frac{1}{C_\mathrm{s}} \int_{t_0}^{t} i_\mathrm{r}(\tau) d\tau + v_{\mathrm{Cs},0} \qquad m_{\mathrm{Cs}}(\theta) = \int_{\theta_0}^{\theta} j_\mathrm{r}(\vartheta) d\vartheta + m_{\mathrm{Cs},0} \tag{3.15}$$

The current i_p is decoupled from the resonant current dynamics because $\mathrm{L_p}$ is clamped to the output voltage V_o , hence

$$i_\mathrm{p}(t) = \frac{1}{L_\mathrm{p}} n V_\mathrm{o} t + i_{\mathrm{p},0}\,. \tag{3.16}$$

The normalized equation depends on the normalization base:

$$V_\mathrm{Base} = V_\mathrm{g} \;\rightarrow\; j_\mathrm{p}(\theta) = \frac{M}{h}\theta + j_{\mathrm{p},0} \qquad V_\mathrm{Base} = nV_\mathrm{o} \;\rightarrow\; j_\mathrm{p}(\theta) = \frac{1}{h}\theta + j_{\mathrm{p},0}\,. \tag{3.17}$$

The initial values of the state variables are unknowns:

$$\begin{aligned} &i_\mathrm{r}(t = t_0) = i_{\mathrm{r},0} && i_\mathrm{p}(t = t_0) = i_{\mathrm{p},0} && v_{\mathrm{Cs}}(t = t_0) = v_{\mathrm{Cs},0} \\ &j_\mathrm{r}(\theta = \theta_0) = j_{\mathrm{r},0} && j_\mathrm{p}(\theta = \theta_0) = j_{\mathrm{p},0} && m_{\mathrm{Cs}}(\theta = \theta_0) = m_{\mathrm{Cs},0}\,. \end{aligned} \tag{3.18}$$

Since t_0 is defined such that $i_{\mathrm{p},0} = i_{\mathrm{r},0}$, the unknowns reduce to $i_{\mathrm{r},0}$ and $v_{\mathrm{Cs},0}$.

To solve the IVP of (3.13) the initial value of the first derivative of i_r is required:

$$i_\mathrm{r}'(t = t_0) = \frac{1}{L_\mathrm{s}}\left(V_\mathrm{g} - nV_\mathrm{o} - R_\mathrm{s} i_{\mathrm{r},0} - v_{\mathrm{Cs},0}\right),$$

$$\text{case } V_\mathrm{Base} = V_\mathrm{g} \quad \rightarrow \quad j_\mathrm{r}'(\theta = \theta_0) = \omega_0\left(1 - M - d j_{\mathrm{r},0} - m_{\mathrm{Cs},0}\right),$$

$$\text{case } V_\mathrm{Base} = nV_\mathrm{o} \quad \rightarrow \quad j_\mathrm{r}'(\theta = \theta_0) = \omega_0\left(\frac{1}{M} - 1 - d j_{\mathrm{r},0} - m_{\mathrm{Cs},0}\right). \tag{3.19}$$

The second interval ($t_1 < t < t_2$) is different for both modes. For the CCMA mode the DE is the same as in the first interval, (3.13). The general solution is given by

$$i_\mathrm{r}(t) = K_{\mathrm{s}12\mathrm{A}} e^{\alpha t} \sin(\beta t) + K_{\mathrm{c}12\mathrm{A}} e^{\alpha t} \cos(\beta t)\,, \tag{3.20}$$

the capacitor waveform derived by

$$v_{\mathrm{Cs}}(t) = \frac{1}{C_{\mathrm{s}}}\int_{t_1}^{t} i_{\mathrm{r}}(\tau)d\tau + v_{\mathrm{Cs},1} \qquad m_{\mathrm{Cs}}(\theta) = \int_{\theta_1}^{\theta} j_{\mathrm{r}}(\vartheta)d\vartheta + m_{\mathrm{Cs},1} \tag{3.21}$$

and the current i_{p} similar to (3.17) given by

$$i_{\mathrm{p}}(t) = \frac{1}{L_{\mathrm{p}}} nV_{\mathrm{o}}t + i_{\mathrm{p},1} \qquad j_{\mathrm{p}}(\theta) = \frac{M}{h}\theta + j_{\mathrm{p},1} \qquad j_{\mathrm{p}}(\theta) = \frac{1}{h}\theta + j_{\mathrm{p},1}\,. \tag{3.22}$$

The initial values of the second interval are further unknowns

$$\begin{aligned} &i_{\mathrm{r}}(t = t_1) = i_{\mathrm{r},1} && i_{\mathrm{p}}(t = t_1) = i_{\mathrm{p},1} && v_{\mathrm{Cs}}(t = t_1) = v_{\mathrm{Cs},1} \\ &j_{\mathrm{r}}(\theta = \theta_1) = j_{\mathrm{r},1} && j_{\mathrm{p}}(\theta = \theta_1) = j_{\mathrm{p},1} && m_{\mathrm{Cs}}(\theta = \theta_1) = m_{\mathrm{Cs},1} \end{aligned} \tag{3.23}$$

and in the derivative of i_{r} the sign of V_{g} changes compared to (3.19):

$$i_{\mathrm{r}}'(t = t_1) = \frac{1}{L_{\mathrm{s}}}\left(-V_{\mathrm{g}} - nV_{\mathrm{o}} - R_{\mathrm{s}}i_{\mathrm{r},1} - v_{\mathrm{Cs},1}\right),$$

$$\text{case } V_{\mathrm{Base}} = V_{\mathrm{g}} \quad \rightarrow \quad j_{\mathrm{r}}'(\theta = \theta_1) = \omega_0\left(-1 - M - dj_{\mathrm{r},1} - m_{\mathrm{Cs},1}\right),$$

$$\text{case } V_{\mathrm{Base}} = nV_{\mathrm{o}} \quad \rightarrow \quad j_{\mathrm{r}}'(\theta = \theta_1) = \omega_0\left(-\frac{1}{M} - 1 - dj_{\mathrm{r},1} - m_{\mathrm{Cs},1}\right). \tag{3.24}$$

For the DCMB2 mode the DE of the second interval ($t_1 < t < t_2$) is different. The inductance of the second order resonant circuit becomes $L_{\mathrm{s}} + L_{\mathrm{p}}$ instead of L_{s}:

$$i_{\mathrm{r}}'' + \frac{R_{\mathrm{s}}}{L_{\mathrm{s}} + L_{\mathrm{p}}} i_{\mathrm{r}}' + \frac{1}{(L_{\mathrm{s}} + L_{\mathrm{p}})C_{\mathrm{s}}} i_{\mathrm{r}} = 0 \qquad j_{\mathrm{r}}'' + \frac{d\omega_0}{(1+h)} j_{\mathrm{r}}' + \frac{\omega_0^2}{(1+h)} j_{\mathrm{r}} = 0\,. \tag{3.25}$$

The general solution of (3.25) is given by

$$i_{\mathrm{r}}(t) = K_{\mathrm{s12B}}e^{\gamma t}\sin(\delta t) + K_{\mathrm{c12B}}e^{\gamma t}\cos(\delta t)\,, \tag{3.26}$$

and the resonant capacitor voltage same as by (3.21). The equation describing i_{p} is no longer discrete, because

$$i_{\mathrm{p}}(t) = i_{\mathrm{r}}(t)|_{t_1 < t < t_2}\,. \tag{3.27}$$

The initial values are the same as in (3.23), but since t_1 is defined such that $i_{p,1} = i_{r,1}$, the unknowns reduce to $i_{\mathrm{r},1}$ and $v_{\mathrm{Cs},1}$. The initial value of the first derivative of i_{r} is given by

$$i_{\mathrm{r}}'(t=t_1)=\frac{1}{L_{\mathrm{s}}+L_{\mathrm{p}}}\left(V_{\mathrm{g}}-R_{\mathrm{s}}i_{\mathrm{r},1}-v_{\mathrm{Cs},1}\right),$$

$$\text{case } V_{\mathrm{Base}}=V_{\mathrm{g}} \quad \rightarrow \quad j_{\mathrm{r}}'(\theta=\theta_1)=\frac{\omega_0}{1+h}\left(1-dj_{\mathrm{r},1}-m_{\mathrm{Cs},1}\right),$$

$$\text{case } V_{\mathrm{Base}}=nV_{\mathrm{o}} \quad \rightarrow \quad j_{\mathrm{r}}'(\theta=\theta_1)=\frac{\omega_0}{1+h}\left(\frac{1}{M}-dj_{\mathrm{r},1}-m_{\mathrm{Cs},1}\right). \tag{3.28}$$

The solutions of the IVPs (3.19)(3.24)(3.28) are given in appendix 9.1. After solving the IVPs of the single intervals, the system of equations describing the steady-state can be generated according to (3.10). For the CCMA mode the set of equations is given by

$$\begin{aligned}
&i_{\mathrm{r},0}=-i_{\mathrm{r}}(t=t_2=T_{\mathrm{s}}/2) && j_{\mathrm{r},0}=-j_{\mathrm{r}}(\theta=\theta_2=\pi/F)\\
&i_{\mathrm{p},0}=i_{\mathrm{r},0}=-i_{\mathrm{p}}(t=t_2=T_{\mathrm{s}}/2) && j_{\mathrm{p},0}=j_{\mathrm{r},0}=-j_{\mathrm{p}}(\theta=\theta_2=\pi/F)\\
&v_{\mathrm{Cs},0}=-v_{\mathrm{Cs}}(t=t_2=T_{\mathrm{s}}/2) && m_{\mathrm{Cs},0}=-m_{\mathrm{Cs}}(\theta=\theta_2=\pi/F)\\
&i_{\mathrm{r},1}=i_{\mathrm{r}}(t=t_1) && j_{\mathrm{r},1}=j_{\mathrm{r}}(\theta=\theta_1)\\
&i_{\mathrm{p},1}=i_{\mathrm{p}}(t=t_1) && j_{\mathrm{p},1}=j_{\mathrm{p}}(\theta=\theta_1)\\
&v_{\mathrm{Cs},1}=v_{\mathrm{Cs}}(t=t_1) && m_{\mathrm{Cs},1}=m_{\mathrm{Cs}}(\theta=\theta_1).
\end{aligned} \tag{3.29}$$

Because of the ideal voltage sink V_{o} in the equivalent circuit of Fig. 3.2 the output loading is still undefined. Therefore (3.29) is supplemented by the normalized output current equation (3.12):

$$I_{\mathrm{o}}=\frac{2}{T_{\mathrm{s}}}\int_0^{T_{\mathrm{s}}/2} i_{\mathrm{o}}(t)dt \qquad J_{\mathrm{o}}=\frac{F}{\pi}\int_0^{\pi/F} j_{\mathrm{o}}(\theta)d\theta\,.$$

The set of equations (3.29) exhibits seven equations and initially 10 unknowns: $i_{\mathrm{r},0}$, $v_{\mathrm{Cs},0}$, $i_{\mathrm{r},1}$, $i_{\mathrm{p},1}$, $v_{\mathrm{Cs},1}$, t_1, T_{s}, V_{o}, V_{g}, I_{o}. Hence, three of the unknowns must be preset to make the set of equations determinate. It is obvious that these should be three of the subset of T_{s}, V_{o}, V_{g}, I_{o}. For example, if the switching frequency $f_{\mathrm{s}} = 1 / T_{\mathrm{s}}$, the input voltage V_{g} and the average output current I_{o} are preset, the solution of (3.29) reveals the resulting output voltage V_{o} for the target load point defined by I_{o}. But in principal any unknown of (3.29) can be solved for, provided that three of the unknowns are preset and feasible starting values for the numerical solver are provided as input.

For the DCMB2 mode the set of equations is given by

$$\begin{aligned}
&i_{\mathrm{r},0}=-i_{\mathrm{r}}(t=t_2=T_{\mathrm{s}}/2) && j_{\mathrm{r},0}=-j_{\mathrm{r}}(\theta=\theta_2=\pi/F)\\
&v_{\mathrm{Cs},0}=-v_{\mathrm{Cs}}(t=t_2=T_{\mathrm{s}}/2) && m_{\mathrm{Cs},0}=-m_{\mathrm{Cs}}(\theta=\theta_2=\pi/F)\\
&i_{\mathrm{r},1}=i_{\mathrm{r}}(t=t_1) && j_{\mathrm{r},1}=j_{\mathrm{r}}(\theta=\theta_1)\\
&i_{\mathrm{p},1}=i_{\mathrm{p}}(t=t_1) && j_{\mathrm{p},1}=j_{\mathrm{p}}(\theta=\theta_1)\\
&v_{\mathrm{Cs},1}=v_{\mathrm{Cs}}(t=t_1) && m_{\mathrm{Cs},1}=m_{\mathrm{Cs}}(\theta=\theta_1)\\
&I_{\mathrm{o}}=\frac{2}{T_{\mathrm{s}}}\int_0^{T_{\mathrm{s}}/2} i_{\mathrm{o}}(t)dt && J_{\mathrm{o}}=\frac{F}{\pi}\int_0^{\pi/F} j_{\mathrm{o}}(\theta)d\theta\,,
\end{aligned} \tag{3.30}$$

with six equations and initially 9 unknowns: $i_{r,0}$, $v_{Cs,0}$, $i_{r,1}$, $v_{Cs,1}$, t_1, T_s, V_o, V_g, I_o. Like as the CCMA mode three unknowns must be preset to yield a determinate set of equations, preferably three out of the subset T_s, V_o, V_g, I_o.

3.1.5 Boundaries of CCMA and DCMB2 Mode

The numerical solving of (3.29) and (3.30) requires the input of feasible starting values. Since the waveforms of the modes are qualitatively known, it is possible to formulate starting values with a very high convergence probability. According to practical experience the following starting values are unconditionally feasible, if a reasonable solution exists:

$$\begin{aligned} j_{r,0} &= -0.5 & i_{p,1} &= 0.5 \cdot 0.9 \quad \text{(if CCMA)} \\ m_{Cs,0} &= -0.5 & \theta_1 &= \pi \cdot 0.9 \\ j_{r,1} &= 0.5 & \theta_2 &= \pi \quad \text{(if } T_s \text{ is unknown)} \\ v_{Cs,1} &= 0.5 & M &= 1 \quad \text{(if } V_o \text{ or } V_g \text{ is unknown).} \end{aligned} \tag{3.31}$$

Based hereupon the possible outcomes of a solving process are:

The numerical solver does not converge and

1. the solution with respect to the given input and output parameters lies in an adjacent or other operating point.
2. no solution with respect to the given input and output parameters does exist in any operating mode.

The numerical solver converges and

3. the solution is correct. Due to the underlying physical model and analysis it is the only solution.
4. the solution is incorrect but the correct solution with respect to the given input and output parameters lies in an adjacent or other operating mode.
5. no solution with respect to the given input and output parameters does exist in any operating mode.

In order to test a set of input and output parameters for a solution in the operating modes of interest, the solving can just be conducted for the respective operating modes in a successive manner based on outcomes 1) and 4). In order to test the correctness of a converged solution, it must comply with the complete discrete time description (3.5). Since the continuity of the state-variables is proven by convergence of the solving process, the compliance to the implicitly defined switching actions $\boldsymbol{c}(\boldsymbol{x}(t_k), \boldsymbol{T}_k) = 0$ is still unknown. For the respective operating modes this is done by the following procedures.

Switching instant at $t = t_0$ (CCMA and DCMB2 mode):
The voltage across L_p must be at least as high as the output voltage nV_o to forward bias the output rectifier. This condition is given by

$$\left(-v_{\mathrm{Cs},0}+V_{\mathrm{g}}\right)\frac{L_{\mathrm{p}}}{L_{\mathrm{p}}+L_{\mathrm{s}}}>nV_{\mathrm{o}}\,,$$

$$\text{case}\quad V_{\mathrm{Base}}=V_{\mathrm{g}}\quad\rightarrow\quad\left(-m_{\mathrm{Cs},0}-dj_{\mathrm{r},0}+1\right)\frac{1}{M}\frac{1}{1+\frac{1}{h}}>1\,,$$

$$\text{case}\quad V_{\mathrm{Base}}=nV_{\mathrm{o}}\quad\rightarrow\quad\left(-m_{\mathrm{Cs},0}-dj_{\mathrm{r},0}+\frac{1}{M}\right)\frac{1}{1+\frac{1}{h}}>1\,. \tag{3.32}$$

This condition describes the boundaries between CCMA and DCMA as well as between DCMB2 and DCMAB modes.

Interval $[t_1..t_2]$ (DCMB2 mode):
In the interval $[t_1..t_2]$ the absolute voltage across L_p must be lower as the output voltage so that the output rectifier stays reverse biased:

$$\left(v_{\mathrm{Cs}}+R_{\mathrm{s}}i_{\mathrm{r}}-V_{\mathrm{g}}\right)\frac{L_{\mathrm{p}}}{L_{\mathrm{p}}+L_{\mathrm{s}}}<nV_{\mathrm{o}}|_{t_1<t<t_2}\,, \tag{3.33}$$

This condition describes the boundary between DCMB2 and DCMB1 mode. It can be shorted to a time independent inequality if a monotonic rising of v_{Cs} in the interval $[t_1..t_2]$, i.e. $i_{\mathrm{r}}(t)|_{t_1<t<t_2}>0$, is assumed. This is at least true for the operating range of practical interest, since $i_{\mathrm{r}}(t=t_2)$ should have a certain positive value to facilitate ZVS switching of the bridge (c.f. Chapter 3.1.7). If so v_{Cs} is maximal at $t=t_2$ and condition (3.33) is met if it is met at $t=t_2$. In consequence (3.33) is given by

$$\left(v_{\mathrm{Cs},2}+R_{\mathrm{s}}i_{\mathrm{r},2}-V_{\mathrm{g}}\right)\frac{L_{\mathrm{p}}}{L_{\mathrm{p}}+L_{\mathrm{s}}}<nV_{\mathrm{o}}\quad\text{and}\quad i_{\mathrm{r},2}>0\,,$$

$$\text{case}\quad V_{\mathrm{Base}}=V_{\mathrm{g}}\quad\rightarrow\quad\left(m_{\mathrm{Cs},2}+dj_{\mathrm{r},2}-1\right)\frac{1}{M}\frac{1}{1+\frac{1}{h}}<1\quad\text{and}\quad j_{\mathrm{r},2}>0\,,$$

$$\text{case}\quad V_{\mathrm{Base}}=nV_{\mathrm{o}}\quad\rightarrow\quad\left(m_{\mathrm{Cs},2}+dj_{\mathrm{r},2}-\frac{1}{M}\right)\frac{1}{1+\frac{1}{h}}<1\quad\text{and}\quad j_{\mathrm{r},2}>0$$

and considering symmetry by

$$\left(-v_{\mathrm{Cs},0}-R_{\mathrm{s}}i_{\mathrm{r},0}-V_{\mathrm{g}}\right)\frac{L_{\mathrm{p}}}{L_{\mathrm{p}}+L_{\mathrm{s}}}<nV_{\mathrm{o}}\quad\text{and}\quad i_{\mathrm{r},0}<0\,,$$

$$\text{case}\quad V_{\mathrm{Base}}=V_{\mathrm{g}}\quad\rightarrow\quad\left(-m_{\mathrm{Cs},0}-dj_{\mathrm{r},0}-1\right)\frac{1}{M}\frac{1}{1+\frac{1}{h}}<1\quad\text{and}\quad j_{\mathrm{r},0}<0\,,$$

$$\text{case}\quad V_{\mathrm{Base}}=nV_{\mathrm{o}}\quad\rightarrow\quad\left(-m_{\mathrm{Cs},0}-dj_{\mathrm{r},0}-\frac{1}{M}\right)\frac{1}{1+\frac{1}{h}}<1\quad\text{and}\quad j_{\mathrm{r},0}<0\,. \tag{3.34}$$

A complete verification of (3.5) with respect to the steady-state solution outputted by the numerical solver would require to check the implicit switching conditions at each time instant

within the switching period. However, checking for (3.32) and (3.34) experimentally turned out to be sufficient to exclude incorrect solutions in the operating range of practical interest. Only one additional test is introduced to recognize incorrect solutions which are originated in a π-fold phase shift within the trigonometric functions. Such an incorrect solution can result at very low switching frequency, which is shown by Fig. 3.6, and is not recognized by (3.32) and (3.34). It can be observed that the interval $[t_0..t_1]$ is longer than the natural period $T_\beta = t_\beta - t_0$ of the L_s-C_s-R_s series resonant circuit. Thus a feasible condition to exclude such incorrect solution is given by

$$(t_1 - t_0) < T_\beta = \frac{T_0}{\beta} \qquad (\theta_1 - \theta_0) < \frac{2\pi}{\beta} \qquad \text{with} \quad \beta = \sqrt{1 - \left(\frac{d}{2}\right)^2}\,. \tag{3.35}$$

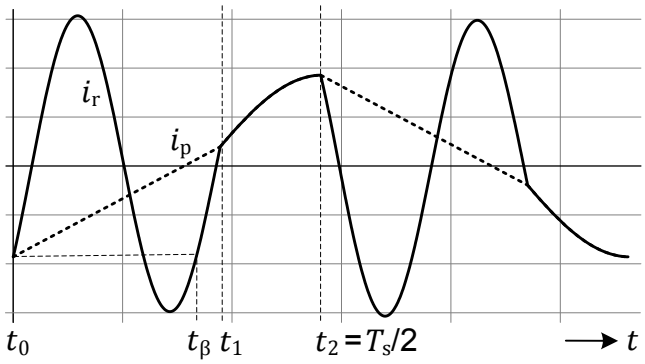

Fig. 3.6: Incorrect solution at very low switching frequency $F_n = 0.3$ not recognized by (3.32) and (3.34)

It should be noted that typically it is not necessary to distinguish between DCMB2 and CCMA mode for (3.34). This is because the CCMA mode complies with (3.34) anyway in operating regions of practical interest (e.g. tested up to 6 times rated load).

3.1.6 Review of the Fundamental Harmonic Analysis (FHA) Approach

The FHA approach has been proposed in literature since the beginnings of the resonant converter discussion ([Steigerwald], [Batarseh]). The FHA considers only the fundamental harmonic of the state variable's waveforms. This is justified by the filtering characteristic of the resonant circuit, by which the harmonic components of the exciting square wave voltage V_{gAB} generated by the bridge are distinctively dampened. But in case of third order resonant circuits like the LLC and LCC series-parallel resonant converter, the FHA additionally suffers from the implicit operation of the output rectifier, which can cause high harmonic content in at least one state variable. This problem is especially addressed by model extensions that are proposed in literature and commonly abbreviated as eFHA (extended FHA), e.g. [Forsyth], [Foster3], [Cao]. Both FHA methods model the converter behavior by means of classic AC circuit theory. Therefore the LLC resonant converter is approximated by the equivalent circuit schematic shown in Fig. 3.7 (assuming $n = 1$). The amplitudes of the fundamental of the exciting voltage $v_{gAB\langle 1\rangle}(t)$ and of the resulting voltage $v_{o\langle 1\rangle}(t)$ are extracted from the fourier series expansion of a square wave voltage and given by

$$\hat{v}_{gAB\langle 1\rangle} = \frac{4}{\pi} V_g \qquad \hat{v}_{o\langle 1\rangle} = \frac{4}{\pi} V_o\,. \tag{3.36}$$

The amplitude of the fundamental of the output current $i_{o\langle 1\rangle}(t)$ is derived from the average output current and used to determine the equivalent load resistor R_{ac}:

$$\hat{\imath}_{o\langle 1\rangle} = \frac{\pi}{2} I_o \qquad R_{ac} = \frac{\hat{v}_{o\langle 1\rangle}}{\hat{\imath}_{o\langle 1\rangle}} = \frac{8}{\pi^2}\frac{V_o}{I_o} = \frac{8}{\pi^2} R_L \tag{3.37}$$

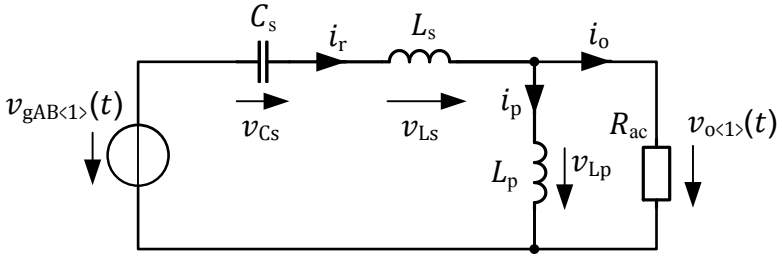

Fig. 3.7: Equivalent circuit schematic of the LLC converter with respect to the FHA method assuming n = 1

Because $\hat{v}_{o\langle 1\rangle} / \hat{v}_{gAB\langle 1\rangle} = V_o / V_g = M$ the DC-DC gain can be calculated by the AC transfer behavior

$$G(j\omega_s) = \frac{\hat{v}_{o\langle 1\rangle}(j\omega_s)}{\hat{v}_{gAB\langle 1\rangle}(j\omega_s)} = \frac{jX_{Lp}||R_{ac}}{-jX_{Cs} + jX_{Ls} + (jX_{Lp}||R_{ac})}. \tag{3.38}$$

With $X_L = \omega_s L$, $X_C = (\omega_s C)^{-1}$ and normalizations of Table 3.2:

$$G(jF_n) = \frac{h(jF_n)^2}{1 + hQ_{ac}(jF_n) + (1+h)(jF_n)^2 + hQ_{ac}(jF_n)^3}. \tag{3.39}$$

The DC-DC gain is finally given by $|G(jF_n)|$:

$$M(F_n) = \frac{hF_n^2}{\sqrt{(1-(1+h)F_n^2)^2 + \left(hQF_n(1-F_n^2)\right)^2}}. \tag{3.40}$$

The input impedance defined by $Z_i(j\omega_s) = \hat{v}_{gAB\langle 1\rangle}(j\omega_s) / \hat{\imath}_{r\langle 1\rangle}(j\omega_s)$ and normalized with respect to Z_0 is given by

$$\frac{Z_i(jF_n)}{Z_0} = \frac{1 + hQ_{ac}(jF_n) + (1+h)(jF_n)^2 + hQ_{ac}(jF_n)^3}{(jF_n)(1 + hQ_{ac}(jF_n))} \tag{3.41}$$

The phase of the input impedance $\varphi = \arg(Z_i(jF_n))$ can be interpreted regarding the switching condition of the bridge. For $\varphi > 0$ the bridge switches before the resonant current has reversed which results in ZVS. For $\varphi < 0$ the bridge switches after the resonant current has reversed which results in ZCS (c.f. Chapter 3.1.7). The curve $\varphi = 0$ in the DC-DC gain and impedance diagrams can be obtained by replacing Q_{ac} in (3.40) resp. (3.41) by

$$Q_{ac}(F_n) = \sqrt{\frac{1 - F_n^2(1+h)}{F_n^2 h^2 (F_n^2 - 1)}}, \tag{3.42}$$

which is derived from the equation $\arg(Z_\mathrm{i}(jF_\mathrm{n})) = 0$. Since Q_ac must be real, the valid parameter range of (3.42) is given by

$$\sqrt{\frac{1}{1+h}} < F_\mathrm{n} < 1\,,$$

at which the lower boundary is the normalized resonant frequency of the C_s-L_s-L_p series resonant circuit:

$$F_1 = \frac{f_1}{f_0} = \sqrt{\frac{1}{1+h}} \quad \text{with} \quad f_1 = \frac{1}{2\pi\sqrt{C_\mathrm{s}(L_\mathrm{s}+L_\mathrm{p})}}. \tag{3.43}$$

The DC-DC gain and input impedance diagrams are shown in Fig. 3.8. From the characteristic of the curve $\varphi = 0$ it can be deduced, that at switching frequencies below F_1 ZCS is the only possible switching condition for the bridge semiconductors. Due to the linearity of the equivalent circuit, no operating modes like for the exact time domain analysis can be distinguished. The only subdivision is possible by the operating regions $\varphi < 0$ (ZCS) and $\varphi > 0$ (ZVS). It can be further deduced that for $F_1 < F_\mathrm{n} < 1$ the switching condition depends on the output loading Q_ac, whereas for $F_\mathrm{n} > 1$ the switching condition is restricted to ZVS.

The FHA approach is an analytical analysis method which is feasible to give a basic understanding of the resonant circuit topology. But especially in case of at least third order resonant circuits the FHA approach exhibits modeling errors that permit the use of the method within a reasonable converter design (c.f. [Oeder2]). The extent of the modeling error is shown in Fig. 3.9 by means of a comparison of the steady-state DC-DC gain predictions between the FHA and the exact solution. The modeling error increases with increasing difference between f_s and f_0. This is in accordance to the fact that the resonant current becomes more and more non-sinusoidal the more detuned the resonant circuit is. At $F_\mathrm{n} = 0.6$ and $Q = 0.4$ the DC-DC gain prediction error of the FHA is around -30%. Since the achievable peak gain of the LLC converter is an important number in the converter design, the FHA method cannot be a reasonable design instrument.

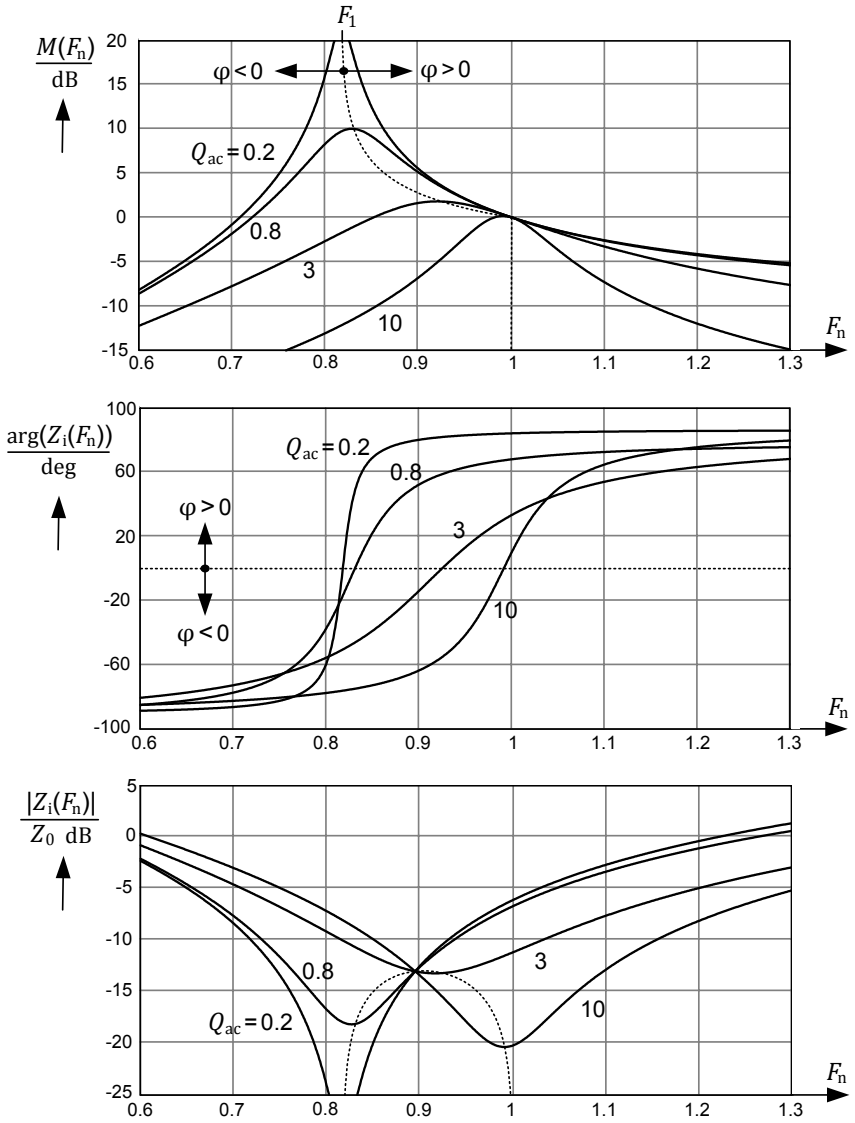

Fig. 3.8: Steady-state characteristics of the LLC resonant converter based on FHA approach

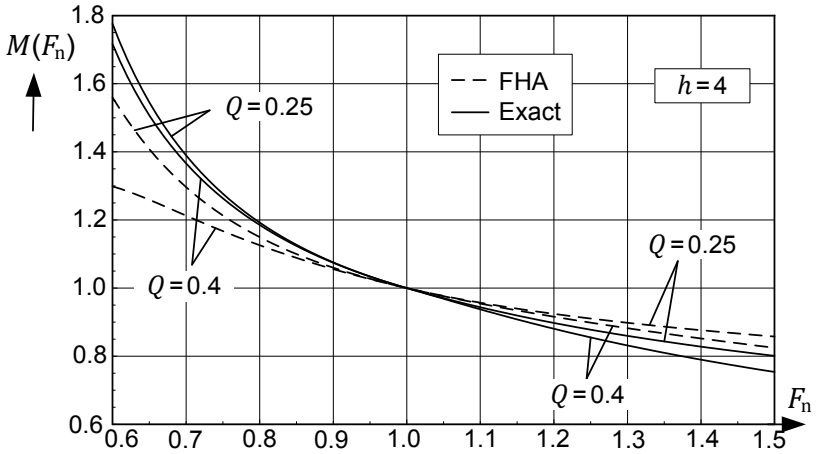

Fig. 3.9: Comparison of the predicted steady-state DC-DC gain between the FHA and the exact time domain approach

3.1.7 ZVS Investigation

An important property of the LLC resonant converter is the ZVS soft switching capability. ZVS omits the occurrence of turn-on losses in the bridge semiconductors. Fig. 3.10 illustrates the basic principle of ZVS under certain assumptions for the components. Lossless turn-on is achieved if $T_\mathrm{d} > T_\mathrm{ZVS}$ is true.

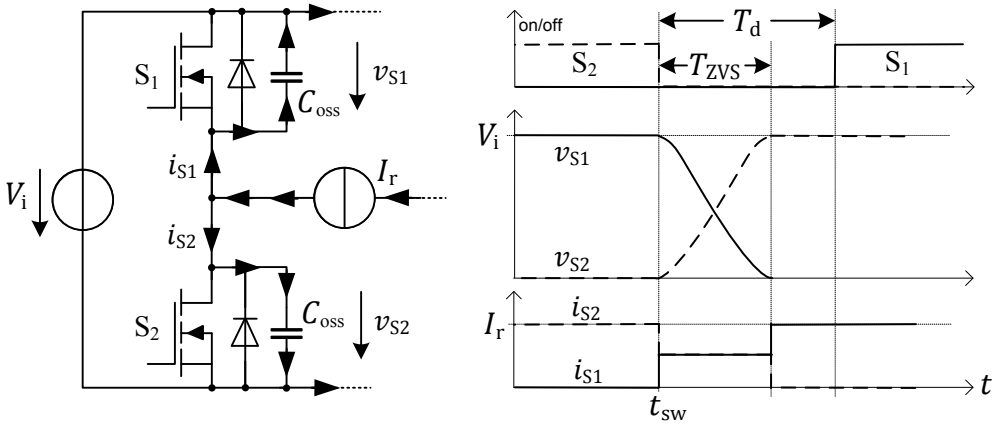

Fig. 3.10: Illustration of a ZVS switching instant of the semiconductor bridge based on idealized component assumptions

The idealized switching transition of Fig. 3.10 assumes that I_r is of constant positive value during the dead time T_d. This assumption is also made by some authors within a design methodology for the LLC converter ([Lu], [Jung]). The assumption originates in the relatively high inductance value of L_p compared to the output capacitances C_oss of the bridge semiconductors with resptect to the stored energy of the elements. In case of a half bridge this approach yields the condition

$$L_\mathrm{p} \leq \frac{T_\mathrm{d}}{16 C_\mathrm{oss} f_\mathrm{s}} \,. \tag{3.44}$$

But as a matter of fact (3.44) neglects the electrical circuit behavior on the secondary side during the switching transition, which will be discussed later. A more precise ZVS investigation is given by [Adragna], [Oeder]. These authors consider a variable current $i_\mathrm{r}(t)$ that recharges the C_oss capacitances. Thereby the behavior of $i_\mathrm{r}(t)$ during the switching transition is derived from an ideal converter operation. However, both latter approaches do not take the detailed circuit behavior into account. In [Lee] the influence of parasitic components on the operation of the LLC converter is studied, but only with respect to the steady-state characteristics. In [Park] the influence of parasitic components on the switching transitions of the rectification stage of a LLC resonant converter is analyzed. The analysis requires also the consideration of the switching transition of the bridge, since both switching transitions occur simultaneously, if at the switching instant of the bridge the resonant current $i_\mathrm{r}(t_\mathrm{sw})$ is not much higher than the current $i_\mathrm{p}(t_\mathrm{sw})$. This is always true in below resonance operation. In above resonance operation it depends on the operating point, given by the switching frequency F_n and the output loading I_o. At fixed F_n the distance between the switching transitions of the bridge and the rectifier decreases with decreasing I_o.

In a similar manner as in [Park] the equivalent circuit of an LLC converter during a switching transition can be constructed like in Fig. 3.11. A necessary condition for such equivalent circuit is that the output voltage can be modeled by an ideal voltage sink. Furthermore the resonant capacitor voltage is assumed to be constant $v_{\mathrm{Cs}}(t)|_{t_{\mathrm{sw}}<t<t_{\mathrm{sw}}+T_{\mathrm{ZVS}}} = V_{\mathrm{Cs}}$ during the duration of the switching transition. The model includes the output capacitances C_{oss} and C_{j} of the bridge semiconductors and of the output rectifiers respectively. It also includes a possible stray capacitance of the XFMR C_{str}. The stray inductances of the rectification circuit are lumped into the inductances L_{σ}. The equivalent circuit is valid for center-tapped as well as full-wave rectification arrangements. In case of full-wave rectification the rectifiers $\mathrm{S_{S<x>}}$ consist of a series connection of two rectification elements.

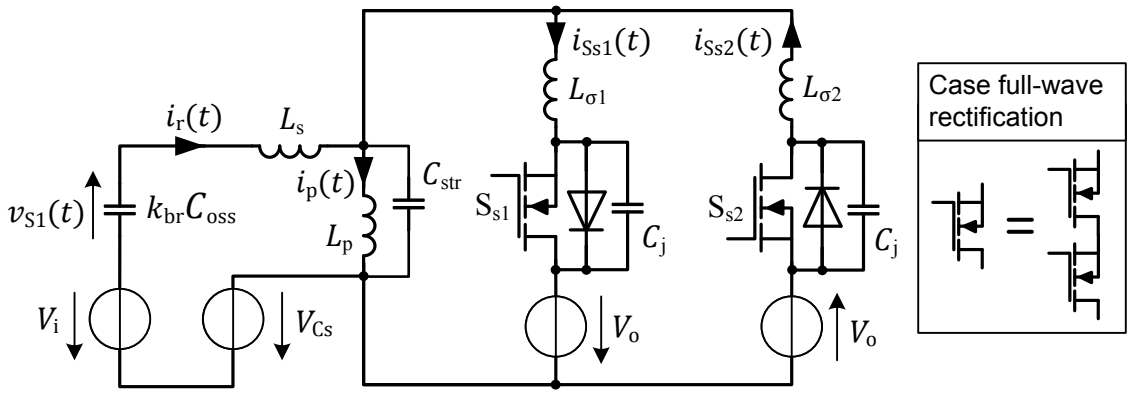

Fig. 3.11: Equivalent circuit diagram during a switching transition of the LLC converter taking major parasitic components into account and assuming $n = 1$; $k_{\mathrm{br}} = 1$: case full-bridge, $k_{\mathrm{br}} = 2$: case half-bridge

The equivalent circuit of Fig. 3.11 reveals the high complexity of the ZVS switching transition within the LLC converter. The exact time domain analysis would yield a DE of eighth order. Besides the high order of the circuit, the linearity especially of $\mathrm{C_{oss}}$ in case of Super-Junction MOSFETs usage is not valid, which introduces a distinct modeling error. It is therefore not possible to construct a simple mathematical ZVS condition that is feasible to be applied within an automatic optimization procedure. Instead the ZVS condition has to be modelled approximately and verified by measurements on the real circuit.

In order to provide an approximate mathematical ZVS condition a worst-case consideration is used. The recharge process of the capacitances in Fig. 3.11 is essential a L-C resonant transition, that exchanges stored energies between inductances and capacitances. Since the inductance ratio h is typically in the range 8 – 12, it is feasible with respect to a worst-case consideration to neglect the energy stored in $\mathrm{L_s}$ for the transition. Furthermore, if the high-frequent Eigenvalues of the equivalent circuit are neglected, which are introduced by the stray inductances L_{σ}, the switching transition can be simplified to a single L-C resonant transition between inductance L_{p} and the overall capacitance $k_{\mathrm{br}}C_{\mathrm{oss}} \| C_{\mathrm{str}} \| k_{\mathrm{rec}}C_{\mathrm{j}}$. The starting angle of the resonant transition depends on the capacitor voltage V_{Cs}. With $V_{\mathrm{Cs}} = V_{\mathrm{i}}$ the transition starts in the zero crossing of the inductor voltage. Since typically the resonant circuit is designed such that $v_{\mathrm{Cs}}(t) < V_{\mathrm{i}}$, the case $V_{\mathrm{Cs}} = V_{\mathrm{i}}$ represents the worst-case for the ZVS condition. Furthermore assuming $M \approx 1$, i.e. close to resonance operation, the voltage swing of all capacitances during the ZVS transition is approximately same and equal to $2V_{\mathrm{i}} / k_{\mathrm{br}}$. The ZVS condition can then be formulated as

$$i_{\mathrm{p}}(t_{\mathrm{sw}}) \geq \frac{2V_{\mathrm{i}}}{k_{\mathrm{br}}} \sqrt{\frac{k_{\mathrm{br}}C_{\mathrm{oss}} + C_{\mathrm{str}} + k_{\mathrm{rec}}C_{\mathrm{j}}}{L_{\mathrm{p}}}}, \tag{3.45}$$

with $k_{\mathrm{rec}} = 1$ for the full-wave and $k_{\mathrm{rec}} = 2$ for the center-tapped rectification case. The condition (3.45) does not incorporate the dead time T_{d}. Instead it is assumed that T_{d} is appropriately adjustable, such that the complete voltage swing of the capacitances can run off if necessary. Furthermore, if $i_{\mathrm{p}}(t_{\mathrm{sw}})$ is derived from $i_{\mathrm{p}}(t_{\mathrm{sw}}) = nV_{\mathrm{o}}/(4f_{\mathrm{s}}L_{\mathrm{p}})$, which is true at resonance and above resonance operation, (3.45) can be refined to

$$L_{\mathrm{p}} \leq \frac{1}{64\left(k_{\mathrm{br}}C_{\mathrm{oss}} + C_{\mathrm{str}} + k_{\mathrm{rec}}C_{\mathrm{j}}\right)f_{\mathrm{s}}^2} \tag{3.46}$$

3.2 Loss Modeling and Efficiency Estimation

One fundamental step in the optimization of a power converter is to model and predict the losses in dependence on important design parameters and the operating condition. On the one hand the losses determine the conversion efficiency. On the other hand they are a side condition for the thermal and mechanic design of the power converter. Hence, loss models are a vital part for optimizing a power converter.
The overall losses of a power converter are made up of different loss types, with some of them being the dominant loss types producing the majority of the overall losses. In order to predict the overall losses accurately, especially each of the dominant loss types need to be modeled reasonably.
Due to the difficulties and extent of the analytical modeling of real world components, this work supports the empirical loss modeling based on measurements, which avoids the need for analytical loss models and their parametrization.
For empirical loss models several points throughout the operating range of a component are measured, at which all other points are predicted from the measured points. To reduce the number of measured points of an empirical loss model, it might be feasible to utilize component characteristics predicted by an analytical model. E.g. the loss modeling of inductive components in paragraph 1.2.3 incorporates such measure to reduce the number of parameter dependencies that have to be evaluated experimentally.

3.2.1 Classification of Loss Types

The major loss types within a power electronics converter can be distinguished by causative components and by loss characteristic. Causative components are

- Semiconductor components: switches and diodes
- Inductive components: chokes and transformers
- Capacitive components: resonant and filter capacitors
- Residual components: conductive paths and connections

Loss characteristics can be classified with respect to the current I flowing in a component according to Fig. 3.12. Losses $P_v \nsim I, f$ are e.g. auxiliary power for controlling the power converter and leakage currents, which might be dependent on input or output voltages. The losses

$P_v \sim I, f$ are forward voltage losses of diodes and switching losses at specified switched currents. The losses $P_v \sim I^x f^x$, $(x \in \mathbb{R}) \wedge (x > 0)$, are hysteresis losses of magnetic components that can be basically modeled by (3.49). The losses $P_v \sim I^2$ are conduction losses, at which especially the conduction losses of magnetic components exhibit a distinct frequency characteristic. All losses are additionally dependent on the temperature.

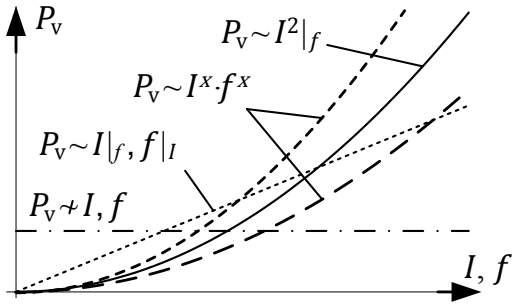

Fig. 3.12: Basic loss characteristics with respect to a component current I and its fundamental excitation frequency f

By means of a normalized notation and assuming that conduction losses can be calculated by the currents RMS value, the efficiency of the LLC converter can be written as

$$\eta = \frac{P_\mathrm{o}}{P_\mathrm{o} + P_\mathrm{v}} = \frac{1}{1 + \sum_i \left[d_i(f_\mathrm{s}) \frac{V_\mathrm{Base}}{V_\mathrm{o}} \left(\frac{J_\mathrm{r,RMS}^2 + J_\mathrm{o,RMS}^2}{J_\mathrm{o}} \right) + \frac{V_{\mathrm{f},i}}{V_\mathrm{o}} + \frac{P_{\mathrm{v},i}(f_\mathrm{s}, J_\mathrm{o})}{P_\mathrm{o}} + \frac{P_{\mathrm{v},i}(V_\mathrm{i}, V_\mathrm{o})}{P_\mathrm{o}} + \frac{P_{\mathrm{v},i}}{P_\mathrm{o}} \right]}, \tag{3.47}$$

with $d_i(f_\mathrm{s})$ – frequency dependent damping; $V_{\mathrm{f},i}$ – forward voltage drop of a diode; $P_{\mathrm{v},i}(f_\mathrm{s}, J_\mathrm{o})$ – switching frequency and current dependent losses excluding conduction losses; $P_{\mathrm{v},i}(V_\mathrm{i}, V_\mathrm{o})$ – input and output voltage dependent losses, $P_{\mathrm{v},i}$ – constant losses.

The semiconductor loss model is presented in Chapter 3.2.2 and the inductive component loss model in Chapter 3.2.3. The capacitive component losses are neglected in this work. For the resonant capacitor C_s this is justified by the availability of highly reliable MLCCs (Multi-Layer Ceramic Capacitors), e.g. [TDK]. The input and output filter capacitors are not part of the design optimization presented in Chapter 5. This is feasible because the overall loss contribution of the filter capacitors is typically not distinct and approximately independent on the design parameters.

3.2.2 Modeling of Semiconductor Losses

Losses of semiconductors split generally into conduction and switching losses. The modeling of the conduction losses is straight forward. From the device datasheet the on-state resistance and/or the forward voltage drop, both in dependence on the temperature is extracted. By knowing the device current the conduction losses can be calculated directly. Of higher effort is the modeling of the switching losses. Several analytical approaches and advancements can

be found in literature (e.g. [Ren], [Xiao], [Yu]) related to Power MOSFET switching modeling. The advancements to classical approximate formulas show that for accurate switching loss modeling a multitude of parameters have to be known for each component to be modeled. Typically those parameters are not available and also switching loss values are not supplied by Power MOSFET and diodes datasheets. The most accurate and practical switching loss modeling method therefore is the measurement of the switching losses on a test platform.

The accuracy of analytical and empirical modeling of switching losses is determined by the reproduction of the real circuit arrangement with respect to stray inductances, stray capacitances, driving circuits and freewheeling devices [Clemente]. The accurate reproduction is difficult unless the measurement is performed on the real circuit arrangement. When using a test platform for the measurements it is therefore necessary to reproduce the parameters of the real arrangement as best as possible.

The switching losses of the bridge MOSFETs must be considered with respect to the ZVS switching condition. The analysis of ZVS switching losses is not yet broadly discussed in literature. In order to model or estimate the ZVS switching losses a more detailed analysis compared to the classical loss estimation formulas is necessary. Due to a lack of feasible publicized references the following explanations and data is based on a brief discussion with experts of a major semiconductor manufacturer [Semdisc]. The important feature of a turn-off procedure of a modern super-junction MOSFET is the very fast turn-off of the channel compared to the duration of the voltage swing. This is illustrated in Fig. 3.13. This results in that the major part of the received energy by the device is stored in the output capacitance $C_{\mathrm{oss}} = C_{\mathrm{DS}} + C_{\mathrm{DG}}$. In consequence only a small amount of energy $\bar{p}_{\mathrm{chn}}(t_{\mathrm{chn}} - t_{\mathrm{sw}})$ is dissipated. The ability of MOSFETs for such kind of loss-less turn-off switching can be characterized according to [Lefebvre]. For this work it is assumed, that in case of the applied modern super-junction MOSFETs the turn-off energy $\bar{p}_{\mathrm{chn}}(t_{\mathrm{chn}} - t_{\mathrm{sw}})$ is already negligible, which is in concordance with [Semdisc]. Since the stored energy in C_{oss} is restored by the ZVS principle, the overall switching losses seem to be negligible. But according to [Semdisc] the charge and discharge process of C_{oss} exhibits a further loss mechanism, which is originated in resistive losses generated by the (dis-)charge current in the MOSFET channel. It is furthermore strongly dependent on the rapidness of the recharge process due to field effects. A typical value of actual super-junction MOSFETs is that 20% of the C_{oss} stored energy is dissipated by this effect at low switching currents. Due to the beneficial characteristic of the LLC converter of exhibiting low switching currents (c.f. Chapter 2.2.2) and because the author had no ability to measure the ZVS losses e.g. by the method used in [Broadmeadow] so far, the applied switching loss model in this work is given in an approximate manner by

$$P_{\mathrm{v,br\_sw}} = 20\% \frac{1}{2} C_{\mathrm{oss}} V_{\mathrm{i}}^2 f_{\mathrm{s}} \tag{3.48}$$

The switching losses of the rectification elements need to be discussed, too. The switching event can always be considered as a diode switching event. In case of synchronous rectification (SR) MOSFETs are used, but the switching of the MOSFETs is done such that at the beginning of the conduction period the MOSFET has not yet turned on, and at the end of the conduction period the MOSFET is turned off prior. This procedure is necessary because the switching instants have to be derived from measured and processed signals, which in practice has only limited accuracy [Figge]. In consequence the turn-on and turn-off event of the SR

MOSFETs are processed by their internal body diode. The turn-on losses of the diode, originating from the commonly known forward recovery effect, are assumed to be negligible because no publication is known stating a noteworthy influence. The turn-off losses of a diode are determined by its reverse recovery behavior (c.f. Fig. 3.14). The height of the turn-off losses depends on the $\mathrm{d}i/\mathrm{d}t$ slope of the forward current $i_\mathrm{F}(t)$, the clamped voltage level V_cl, the inductance of the commutation loop, and on the reverse recovery behavior of the diode itself. The multiple factors make the switching loss modeling of the synchronous rectifiers involved. Since in datasheets the reverse recovery behavior of diodes and MOSFET body diodes is typically only given for a single combination of parameters, accurate loss modeling requires the measurement of the device in dependence on multiple parameters like proposed in [Stahl2].

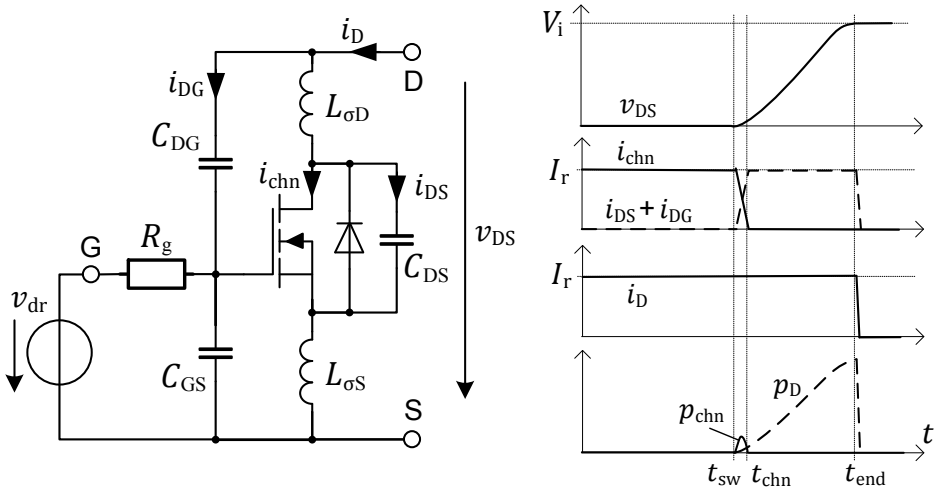

Fig. 3.13: Common equivalent circuit model for MOSFETs and idealized waveforms of an inductive clamped turn-off process

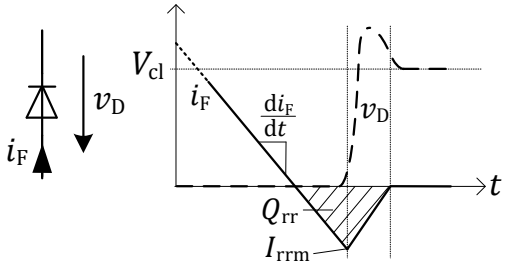

Fig. 3.14: Idealized reverse recovery behavior of a power diode

Such measurement facility was not available to the author. Hence, the switching losses of the output rectifier cannot be considered for the design optimization. But this does not lead to less accuracy of the design optimization, if nominal operating points close to or below resonance result as optimized designs. At such operating points the output rectifier switching is very soft due to a low current slope, and is commonly referred to as ZCS switching. Considerable switching losses occur only in the above resonance region, which results in a slight error of the optimization result, if the optimized result yields nominal operating points in the above resonance region. In such case, the resonant frequency f_0 of the optimized result will be slightly too high compared to the real optimum.

3.2.3 Modeling of Inductive Component Losses

Inductive component losses split into core losses and copper losses. Core losses are hysteresis losses and conduction losses of eddy currents flowing in the core. In this work only ferrite core material with low conductivity is considered, so that Eddy Currents flowing in the core play no significant role for the loss modeling. Copper losses are conduction losses in the copper material. The currents in the copper material can be described as an average net current of the component superimposed by different types of eddy currents.

Modeling of hysteresis losses in literature and practice is to the most performed empirically. This is due to the complicated physical process of hysteresis losses and its analytical description. It is furthermore supported by the possibility to model the core losses by quite simple approximation formulas, which are based on the empirical law of hysteresis first stated by Steinmetz [Steinmetz].

In contrast the conduction losses of the coil are much more suited to be modeled by analytical methods, what is expressed by a multitude of publications that are dedicated to analytical conduction loss modeling in inductive components (e.g. [Dowell], [Ferreira], [Nan], [Severns]). In many cases the reported model accuracy of the presented analytical modeling approaches is acceptable and would be feasible to support accurate loss modeling and optimization routines. However, the accuracies of the analytical models especially depend on the feasibility of boundary conditions and constraints that must be chosen to enable the analytical approach. Typical assumptions are a regular and equal winding distribution, a complete covering of the winding window by the winding, and an infinite permeability of the core material. Furthermore assumptions for simplified magnetic field distribution inside the winding window have to be made. All these assumptions will add modeling errors when applied to real world inductive components, where the modeling error itself is unknown and would have to be verified elaborately for every new magnetic component that is designed.
As to omit the difficulties and uncertainties of the analytical modeling of real world inductive components, this work supports the empirical modeling of the copper losses based on measurement results. Unfortunately, the measurement of copper losses of inductive components is a very time consuming task. In order to speed up the process, an analytical approximate copper loss model was chosen from literature and will be presented. From the model certain interdependencies between winding copper loss and design parameters are adopted. In this way the number of measurements that are necessary to empirically model the winding copper losses in dependence on design parameters is reduced.

3.2.3.1 Core Loss Model

Core material applied in modern server and telecom power supplies is typically made of soft ferrite based on MnZn (Manganese-Zinc) material. The law of hysteresis first stated by Steinmetz [Steinmetz] describes the core losses for sinusoidal magnetization curves in dependence on the peak magnetization. Later extended by the signal frequency the formula exhibits three coefficients k, α, β :

$$P_{\mathrm{v,core}} = k \cdot (f/\mathrm{Hz})^{\alpha} \cdot (\hat{B}/\mathrm{T})^{\beta} . \tag{3.49}$$

The accuracy of the Steinmetz equation depends on the core material, core temperature, signal characteristics and core shape. Hence, certain extensions are presented in literatures which add more parameters to the law. Especially for the popular MnZn material several works found in literature propose feasible extensions. The work of [Li] extends the Steinmetz equation for arbitrary, i.e. non sinusoidal signals, by appropriately recognizing the rate of change of the magnetization throughout the hysteresis curve instead of just relying on the peak magnetization. The new law is designated GSE (General Steinmetz Equation). The work of [Venkatachalam] rewrites the GSE to make it applicable to the concept of major and minor loops prior introduced by [Albach]. This law is designated iGSE (improved GSE). For applying the iGSE law, the signal has to be broken into major and minor hysteresis loops, at which the losses of each loop are finally added to get the overall hysteresis losses. A further improvement to the iGSE is proposed by [Muehlethaler2] and designated i^2GSE. This method increases the model accuracy in case of trapezoidal and non-symmetric triangle signals. By introducing an additional loss term, relaxation effects within the core material are accounted for. A detailed study of the core losses in case of non-symmetric triangle signals is also found in [Mu]. One example for describing core losses in dependence on a DC pre-magnetization is given in [Muehlethaler3]. A detailed study on influences on the measuring accuracy of core losses is given by [Stadler].
In this work the core losses are modeled via the iGSE. The iGSE is defined by

$$P_{\mathrm{v,core}} = \frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} k_\mathrm{c} \left| \frac{dB(t)}{dt} \right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{3.50}$$

with

$$k_\mathrm{c} = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos(\theta)|^{\alpha} 2^{\beta-\alpha} d\theta},$$

where k is the Steinmetz parameter for sinusoidal excitation and ΔB the peak-to-peak flux density of the respective magnetization loop (units omitted in (3.50)). The i^2GSE and the sub-loop concept are not applied in this work because the benefits on the loss modeling do not justify the higher modeling effort. This can be explained by observing the current waveforms of the LLC converter. The resonant current, which is flowing in the resonant choke L_s, is almost sinusoidal, and the magnetizing waveform of the transformer is almost triangular. Significant deviations from the ideal waveforms occur in strong below resp. strong above resonant operation. But since the optimal operating region of the LLC converter is close to resonance, the loss modeling for the design optimization can concentrate on the resonance region.

The core loss data given in manufacturer datasheets is acquired on a small toroid core sample. The core loss as such is an average core loss throughout the cross section of the toroid core. The adoption of the loss data on core shapes used in real converters, which are e.g. U-, E- or PQ-cores, has implications. In a rectangular core the core cross section changes in the corner segments and often also by different linear segments of the core. Therefore it would be necessary to calculate the core losses separately for each segment of the core. Also the magnetic flux constriction in the core corners can only approximately be treated. In consequence a certain modeling error must be considered if datasheet supplied loss characteristics are used for core loss calculations of applied core shapes.

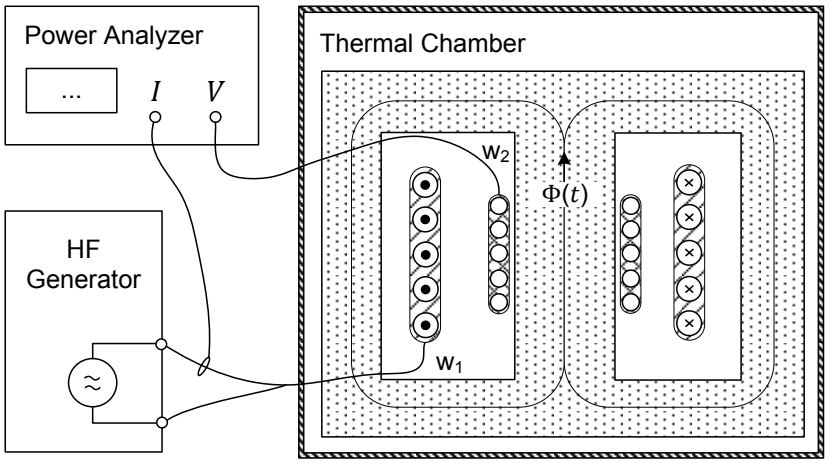

Fig. 3.15: Core loss measurement principle arrangement

A more accurate approach relies on the measurement of the core losses of the applied core shape which is illustrated in Fig. 3.15. By sensing the voltage with a separate winding, the resistive losses of the exciting winding, including its own skin-effect losses and possible proximity-effect losses in the sense winding, are excluded from the measurement. The relation between the measured values and the field quantities in the core can be described by

$$P_{\mathrm{v,core}} = f\int_0^T i_{\mathrm{w1}}(t)\,u_{\mathrm{w2}}(t)dt = f\int_0^T \frac{H(t)l_{\mathrm{e}}}{N_{\mathrm{w1}}}\frac{dB(t)}{dt}A_{\mathrm{e}}N_{\mathrm{w2}}dt = f\frac{N_{\mathrm{w2}}}{N_{\mathrm{w1}}}\left(\oint HdB\right)V\,, \tag{3.51}$$

where l_{e} and A_{e} are equivalent magnetic path length and core cross section, that account for the different core segments. Since this relationship is not precise due to the averaged equivalent values, another justification for the measurement method is possible by balancing the loss contributors: Assuming impressed sinusoidal excitation current $i_{\mathrm{w1}}(t)$, the voltage of the excitation winding $u_{\mathrm{w1}}(t)$ can be divided into a voltage originating from the core flux $u_{w2}(t) = N_{w2}d\Phi/dt$ plus a voltage originating from the stray flux and copper losses $u_{\mathrm{w1}}(t) - u_{\mathrm{w2}}(t)$. The loss balance can then be written as

$$\begin{aligned} P_{\mathrm{v,core}} = P_{\mathrm{v}} - P_{\mathrm{v,copper}} &= f\left[\int_0^T i_{\mathrm{w1}}(t)\,u_{\mathrm{w1}}(t)dt - \int_0^T i_{\mathrm{w1}}(t)\,(u_{\mathrm{w1}}(t) - u_{\mathrm{w2}}(t))dt\right] \\ &= f\int_0^T i_{\mathrm{w1}}(t)\,u_{\mathrm{w2}}(t)dt\,. \end{aligned} \tag{3.52}$$

This type of core loss measurement can only be conducted at ungapped cores. In case of gapped cores the stray fields inside the winding window would significantly increase and disturb the core flux sensing as well as a uniform magnetization of the core.

3.2.3.2 Approximate Copper Loss Model for Inductive Components

The dissipative energy loss of a current carrying conductor based on Ohms law and according to Parseval's theorem is given by

$$P_\nu = \Re\left(\sum_{\nu=0}^{\infty} U_\nu I_\nu^*\right) = R\sum_{\nu=0}^{\infty} |I_\nu|^2 = R I_{\mathrm{RMS}}^2 \tag{3.53}$$

$$\text{with} \quad X_\nu = \frac{\sqrt{2}}{T}\int_0^T x(t)e^{-j\nu\omega t}dt\,, \quad X_0 = \frac{1}{T}\int_0^T x(t)dt\,, \quad R = \rho \cdot l_\mathrm{R} \,/\, A_\mathrm{R}\,.$$

This calculation assumes an equal distribution of the current among the cross section of the wire. But in case of harmonic currents $I_\nu \neq 0$ the homogenous current density is disturbed by the appearance of well-known eddy currents [Lammeraner]. The unequal distribution of the current leads to an increase of the overall resistance of the conductor, since its cross section A effectively reduces.

Eddy currents are induced currents which can be described by Maxwells equations. The curl of current within conductive material with permeability $\mu = \mu_0$ is given by the derivation of the magnetic field H:

$$\mathrm{rot}\,\vec{E} = \frac{1}{\kappa}\mathrm{rot}\,\vec{J} = -\frac{\partial \vec{B}}{\partial t} = -\mu_0 \frac{\partial \vec{H}}{\partial t}\,.$$

The inducing magnetic field H is given by overall current densities $\vec{J}$, which includes the induced and impressed current densities of the problem, whereas displacement currents $\vec{D}$ are neglected due to their low effect in the relevant frequency range:

$$\mathrm{rot}\,\vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \approx \vec{J}\,.$$

The phenomena caused by eddy currents in inductive components are distinguished by the source of the inducing magnetic field H: For the skin effect the field is generated by the current flowing in the conductor itself, and for the proximity effect the field is generated by currents flowing in adjacent conductors.

In most cases the exact calculation of eddy currents in inductive components is not possible by analytical methods, or at least very complicated. Therefore many authors make assumptions to get an approximate but clear analytical solution for the problem. A popular method is the reduction of the problem to a one-dimensional (1-D) one, so that quite simple analytical solutions can be found ([Dowell], [Ferreira2]). The 1-D approximation was successfully utilized e.g. by [Wallmeier] to model typical inductive components used in modern power electronic converters. The 1-D approximation of inductors and transformers is based on the arrangement of Fig. 3.16. The basic assumptions for the model are:

1. The curvature of the winding layers with respect to the y-axis is neglected.
2. Unregular zones of the winding, e.g. inlet and outlet wire, are neglected.
3. Displacement currents are neglected, i.e. the magnetic field is only determined by conductor currents.
4. The core has infinite permeability $\mu \to \infty$ and zero conductivity $\kappa \to 0$. Hence the core properties are no part of the solution and the magnetic field has perpendicular orientation on the core surface.
5. The winding width is equal to the winding window width b_w.

6. The y-component H_y of the magnetic field is dominant so that the x-component H_x can be neglected.

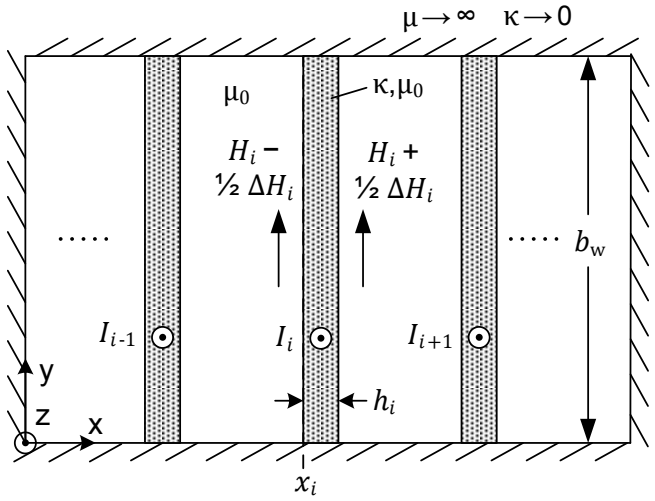

Fig. 3.16: Basic 1-dimensional approximation of an inductive component with multiple winding layers

Because of assumption 4) the strip conductor at position x_i can be governed as to have infinite width. The field solution of such a conductor is e.g. given in [Ferreira2]. Starting point is a differential equation derived from Maxwell's equations assuming $\vec{B} = \mu_0 \vec{H}$,

$$\nabla^2 \vec{H} = \alpha^2 \vec{H}, \quad \alpha = \frac{1+j}{\delta}, \quad \delta = \frac{1}{\sqrt{\pi f \kappa \mu_0}} \text{ (δ: skin depth)}, \tag{3.54}$$

at which the time dependence of the quantities has been substituted by a complex Fourier expansion with $x(t) = \sqrt{2} X e^{j\omega t}$. To solve the equation appropriate boundary values must be chosen. Here two basic cases can be distinguished: If the magnetic field is generated by the own current of the inductor, the boundary values become

$$H_y(x_i + h_i) = -H_y(x_i) = \Delta H_i/2 = I_i/(2b_w)$$

and the magnetic field and current density solution is

$$H_{y,i}(x) = I_i \frac{\sinh(\alpha(x - h_i/2))}{2b_w \sinh(\alpha h_i/2)} \qquad J_{z,i} = I_i \frac{\alpha \cosh(\alpha(x - h_i/2))}{2b_w \sinh(\alpha h_i/2)}. \tag{3.55}$$

If the magnetic field is generated by other than the own current of the inductor, the boundary values become $H_y(x_i + h_i) = H_y(x_i) = H_i$ and the solution is

$$H_{y,i}(x) = H_i \frac{\cosh\big(\alpha(x - h_i/2)\big)}{\cosh(\alpha h_i/2)} \qquad J_{z,i}(x) = H_i \frac{\alpha \sinh \alpha \left(x - \frac{h_i}{2}\right)}{\cosh\left(\frac{\alpha h_i}{2}\right)}. \tag{3.56}$$

Hence two basic solutions arise, at which the current density of (3.55) is related to the inner skin effect of the conductor, and the current density of (3.56) to the proximity effect between multiple adjacent conductors. An important fact pointed out by [Ferreira2] is, that the resulting current densities of skin and proximity effect are orthogonal to each other in this case. The advantage is that the power loss generated by each effect can be calculated separately due to the orthogonality. The power loss per unit length of conductor related to the skin effect becomes

$$P'_{\mathrm{Vs},i} = \frac{b_\mathrm{w}}{\kappa}\int_{x_i}^{x_i+h_i} \Re\{J_{\mathrm{z},i}(x)J^*_{\mathrm{z},i}(x)\}dx$$
$$= \frac{b_\mathrm{w}}{\kappa}\int_{x_i}^{x_i+h_i} \left|J_{\mathrm{z},i}(x)\right|^2 dx = I_i^2\,\frac{\gamma_i}{4b_\mathrm{w}\kappa h}\,\frac{\sinh(\gamma_i)+\sin(\gamma_i)}{\cosh(\gamma_i)-\cos(\gamma_i)}, \tag{3.57}$$

$$\gamma_i = h_i/\delta.$$

The same quantity related to the proximity effect becomes

$$P'_{\mathrm{Vp},i} = \frac{b_\mathrm{w}}{\kappa}\int_{x_i}^{x_i+h_i} \left|J_{\mathrm{z},i}(x)\right|^2 dx = H^2_{\mathrm{y},i}\,\frac{b_\mathrm{w}\gamma_i}{\kappa h}\,\frac{\sinh(\gamma_i)-\sin(\gamma_i)}{\cosh(\gamma_i)+\cos(\gamma_i)}. \tag{3.58}$$

Considering the orthogonality of skin and proximity current densities the overall power loss per unit length of a single layer becomes

$$P'_{\mathrm{V},i} = P'_{\mathrm{Vs},i} + P'_{\mathrm{Vp},i}\,. \tag{3.59}$$

By isolating the DC resistance $R_{\mathrm{DC},i}$ of the conductor and defining l_i as the length of winding i, (3.59) can be rewritten as

$$P_{\mathrm{V},i} = R_{\mathrm{DC},i}(F_\mathrm{s}(\gamma_i)\,I_i^2 + F_\mathrm{p}(\gamma_i)\,b_\mathrm{w}^2\,H^2_{\mathrm{y},i})\,, \tag{3.60}$$

$$R_{\mathrm{DC},i} = \frac{l_i}{\kappa b_\mathrm{w} h_i},\quad F_\mathrm{s}(\gamma_i) = \frac{\gamma_i}{2}\,\frac{\sinh(\gamma_i)+\sin(\gamma_i)}{\cosh(\gamma_i)-\cos(\gamma_i)},\quad F_\mathrm{p}(\gamma_i) = 2\gamma_i\,\frac{\sinh(\gamma_i)-\sin(\gamma_i)}{\cosh(\gamma_i)+\cos(\gamma_i)}.$$

This solution is an exact solution for the arrangement of Fig. 6, which in any case differs from the real component that is to be modeled. Hence, the modeling error depends on the winding material used in the layers. Practical winding materials are foil (thin strip conductor), round wire and litz (stranded round wire). In case of foil the modeling error especially arises from gaps between the winding layer and the core when the width of the foil is smaller than b_w. By this gap the assumption of no radial component in the magnetic field $H_\mathrm{x} = 0$ is violated. The H_x component leads to additional eddy currents in the foil conductor which are not included in the model. In [Wallmeier] studies on the extent of the modeling error by means of FEM simulations are presented and empirical adjusting factors are proposed.

A very familiar case in modern power electronics converters, and especially for the LLC resonant converter, is the use of litz wire for the magnetic component windings. Litz consists of many enameled and bundled wire strands aiming to reduce the ratio between the individual

wire radius and the skin depth. The individual wire radius must be appropriately chosen so that the advantage of a reduced skin effect factor F_s is higher than the disadvantage of an increased DC resistance R_{DC} due to lower copper density in the winding window and the disadvantage of increased proximity losses due to a higher number of individual conductors.

[Ferreira2] demonstrates the consideration of litz for the 1-D modeling approach. Here the conductor area $h \cdot b_w$ of Fig. 3.16 is considered to be covered with litz wire, where N_i is the number of turns of the litz wire in layer i and N_{st} the number of strands in the litz bundle. The packing factor $p_{cu,i}$, which is the ratio between the overall copper cross sectional area and the outer dimensions product $h_i \cdot b_w$ of the layer, is less than one. Typical values for litz wire are between 0.5 and 0.6 [Pack].

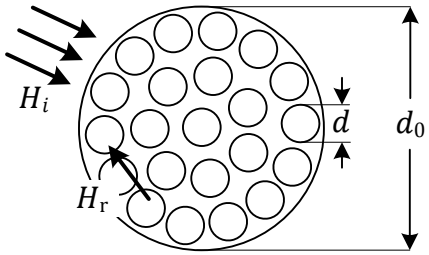

Fig. 3.17: Litz wire cross sectional view and magnetic field components

The basic idea of the approach is as follows: Every litz strand has its own skin effect losses plus proximity effect losses that can be calculated by assuming a round conductor that is exposed to an external uniform magnetic field. Clearly, uniformity of the external magnetic field is an approximation, but since the individual wire strands are very small compared to the overall dimensions of the bundle resp. layer, the resulting modeling error is assumed to be not significant. The external magnetic field is a superposition of the radial oriented field H_r generated by the litz bundle itself and the field H_i generated by the other layers of the winding (c.v. Fig. 3.17). By calculating the resulting losses of a litz wire which is conducting the current I_i and exposed to the uniform external magnetic field H_i , (3.60) can be rewritten (c.f. [Muehletaler], [Wallmeier]) as

$$P_{V\_litz,i} = R_{DC\_litz,i}\left(F_{s\_round}(\gamma_i)\, I_i^2 + N_{st} F_{p\_round}(\gamma_i)(\pi d)^2 \left(H_{y,i}^2 + \frac{I_i^2}{2(\pi d_0)^2}\right)\right), \quad (3.61)$$

$$F_{s\_round}(\gamma_i) = \frac{\gamma_i}{2\sqrt{2}} \frac{ber_0(\gamma_i)(bei_1(\gamma_i) - ber_1(\gamma_i)) - bei_0(\gamma_i)(bei_1(\gamma_i) + ber_1(\gamma_i))}{ber_1^2(\gamma_i) + bei_1^2(\gamma_i)},$$

$$F_{p\_round}(\gamma_i) = \frac{\gamma_i}{\sqrt{2}} \frac{ber_1(\gamma_i)(bei_2(\gamma_i) - ber_2(\gamma_i)) - bei_1(\gamma_i)(bei_2(\gamma_i) + ber_2(\gamma_i))}{ber_0^2(\gamma_i) + bei_0^2(\gamma_i)},$$

$$\gamma = \frac{d}{\sqrt{2}\delta}, \qquad R_{DC,i} = \frac{4\, l_i}{\pi d^2 \kappa} \frac{1}{N_{st}} .$$

Since one layer usually consists of multiple litz wire turns N_i , the overall loss of one layer is

$$P_{V,i} = N_i P_{V\_litz,i} . \quad (3.62)$$

The main feature of the 1-D approximation with respect to the modeling of inductors and transformers is the possibility to separate the layer currents in the solution of the field-problem. In [Wallmeier] this feature was used to enable the impedance calculation of an arbitrary connection of single layers, even though the layers may be of different construction type. The design optimization presented in Chapter 5 requires the calculation of losses in dependence on design parameters. An important design parameter of inductive components is the number of turns N_w. Since the 1-D approximation enables the separation of the layer currents in the field solution, it also enables the separation of the number of turns in the field solution. Hence, the variation of losses in dependence on the number of turns N_w can be calculated from the 1-D approximation, if certain further assumptions are made. Those will be explained in the according paragraphs.

3.2.3.3 Copper Loss Modeling of LLC Resonant Choke

The optimization procedure presented in Chapter 5 requires knowledge of the losses of the choke in dependence on design parameters. Design parameters are core shape, overall component volume, air gap, number of turns and winding type. Automatic optimization considering all design parameters of the choke is not in the scope of this work. Models with an extended number of parameters used in automatic optimization are e.g. used in [Biela2].
The main points that support the use of a small order model approach in this work are:

- When designing an AC-DC power supply with today's high power density requirements ($50 - 100\ \mathrm{W/in^3}$), the mounting space of the magnetic components is already predefined by the form factor of the specified power supply housing and the surrounding components. In such a case asking for the optimal magnetic component volume is less feasible than asking for the optimal magnetic component that fits into the available space.
- In many practical design cases the core geometry cannot be arbitrarily chosen due to costs. Hence, readily available and cost efficient core shapes e.g. in the company or division have to be used.
- The same applies for the winding material. Commonly a limited range of winding materials is available. In case of litz there is a high probability that available types have already proven good results in the relevant frequency range.
- The computation time for optimal results considering a high number of design parameters increases at least by 2 power the number of design parameters. It is an aim that computation time should not become unpractical regarding industrial design processes.

Considering the above criteria only the design parameters air gap length l_g and number of turns N_w are chosen. This selection is based on the following further assumptions:

1. The user has chosen the best fitting core geometry for the actual design problem.
2. Only litz wire is considered as winding material. As so the user has chosen the best available type of litz wire considering skin depth.
3. The winding window is always filled up completely by the winding.

Assumption 2) is justified by the pure and high frequent AC current that is flowing in a resonant power choke. It is further more supported by practical experience. Assumption 1) yields a constant winding window size A_w. Assumption 3) has certain consequences regarding that

the number of turns N_w is a varying parameter. When using litz wire according to assumption 2) the diameter of the litz strands is considered as fixed for the design optimization. Hence, the variation of the number of turns N_w in practice is only possible by using litz wire with different number of strands N_st. If (3.61) is used for loss modeling, the single loss contributions would change by different factors and it would be difficult to isolate the factor N_w from the equation. An alternative model is proposed here. Since the litz wires typically are closely wound so that no geometrical separation of layers of litz wire can be justified, the cross section of the litz covered winding windows is assumed just as one single cluster of round conductors. Fig. 3.18 shows the proposed approximations. The single strands are assumed to be in equal vertical alignment, hence forming a cluster of layers of round conductors with the same number of conductors in every layer. By applying the 1-D approximation every layer of this cluster is regarded as a single layer. Moreover the radial magnetic field component H_x can be neglected because the single strand is small compared to the overall arrangement.
In order to calculate the power loss in dependence on the number of turns N_w the additional approximation of a uniform distribution of the strands over the whole winding windows is necessary. Since in most cases the overall number of strands is high, the error introduced by this approximation is negligible. The equal distribution allows defining an equivalent packing density. The packing density is given by

$$p_\mathrm{w} = \frac{N_\mathrm{w} N_\mathrm{st} \pi d^2}{4 A_\mathrm{w}}, \tag{3.63}$$

with $N_\mathrm{w} N_\mathrm{st}$ being the overall number of strands in the winding window. According to the packing density approximation illustrated in Fig. 3.18, the equivalent number of strands along the x- resp. y-axis is given by

$$N'_\mathrm{bw} = \frac{b_\mathrm{w} 2\sqrt{p_\mathrm{w}}}{d\sqrt{\pi}} \quad N'_\mathrm{hw} = \frac{h_\mathrm{w} 2\sqrt{p_\mathrm{w}}}{d\sqrt{\pi}} \tag{3.64}$$

with

$$N_\mathrm{w} N_\mathrm{st} = N'_\mathrm{hw} N'_\mathrm{bw} \quad \text{and} \quad \frac{N'_\mathrm{bw}}{N'_\mathrm{hw}} = \frac{b_\mathrm{w}}{h_\mathrm{w}} .$$

Taking I_w as the whole litz current, the current in every strand $I_{\mathrm{st},i}$ can be expressed by

$$I_{\mathrm{st},i} = I_\mathrm{w} \frac{N_\mathrm{w}}{N'_\mathrm{hw} N'_\mathrm{bw}}. \tag{3.65}$$

The power loss in every strand then becomes

$$P_{\mathrm{v\_strand},i} = R_{\mathrm{DC\_strand},i} \left(F_{\mathrm{s\_round}}(\gamma)\, I^2_{\mathrm{st},i} + F_{\mathrm{p\_round}}(\gamma) (\pi d)^2 H^2_{\mathrm{y},i} \right), \tag{3.66}$$

$$\gamma = \frac{d}{\sqrt{2}\delta}, \qquad R_{\mathrm{DC},i} = \frac{4\, l_i}{\pi d^2 \kappa}.$$

The overall power loss is found by summing up every strands loss to

$$P_{\mathrm{v}} = \sum_{i=1}^{N'_{\mathrm{hw}}} N'_{\mathrm{bw}} P_{\mathrm{v\_strand},i} \,. \tag{3.67}$$

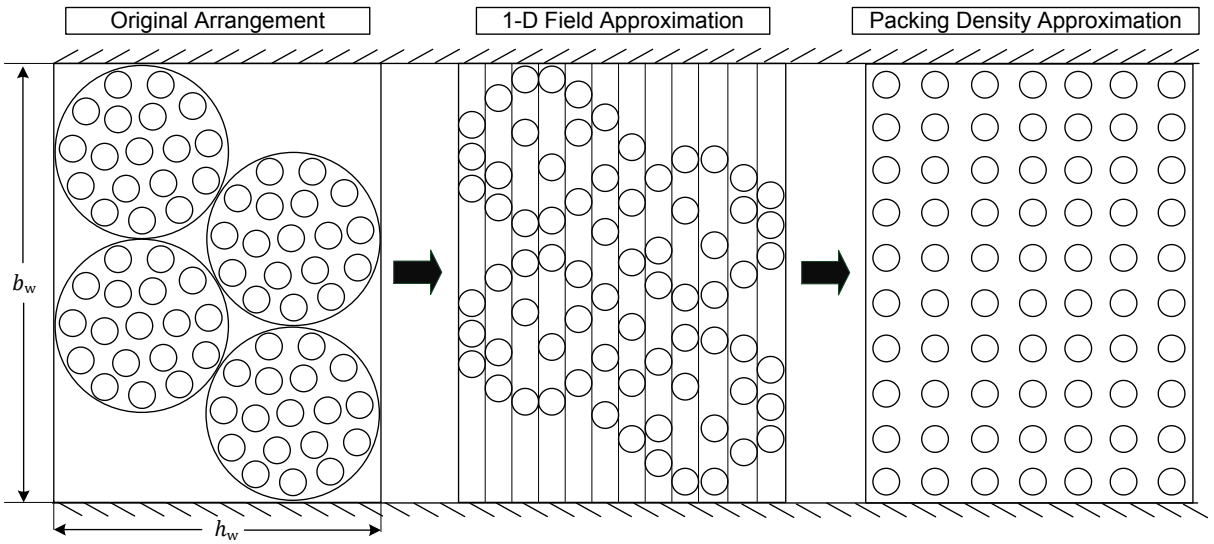

Fig. 3.18: Illustration of approximation methods for litz windings

To complete the power loss model the magnetic field H_i in every layer must be calculated. Therefore it is assumed that the LLC resonant choke is realized by a center-legged core geometry and that the air gap is localized in the cores center leg. The air gap produces a fringing field which yields a considerable radial magnetic field component H_{x} in the vicinity of the air gap ([Roshen], [Wallmeier]). In consequence the fringing field effect cannot be modeled by the 1-D approach and must be separately considered. In a first step the magnetic field of the winding window is calculated by assuming that the air gap is distributed along the whole winding width b_{w} as illustrated in Fig. 3.19. An equivalent permeability is derived such that the air gap reluctance stays equal:

$$\mu_{\mathrm{eq}} = \mu_0 \frac{b_{\mathrm{w}}}{l_{\mathrm{g}}} \,. \tag{3.68}$$

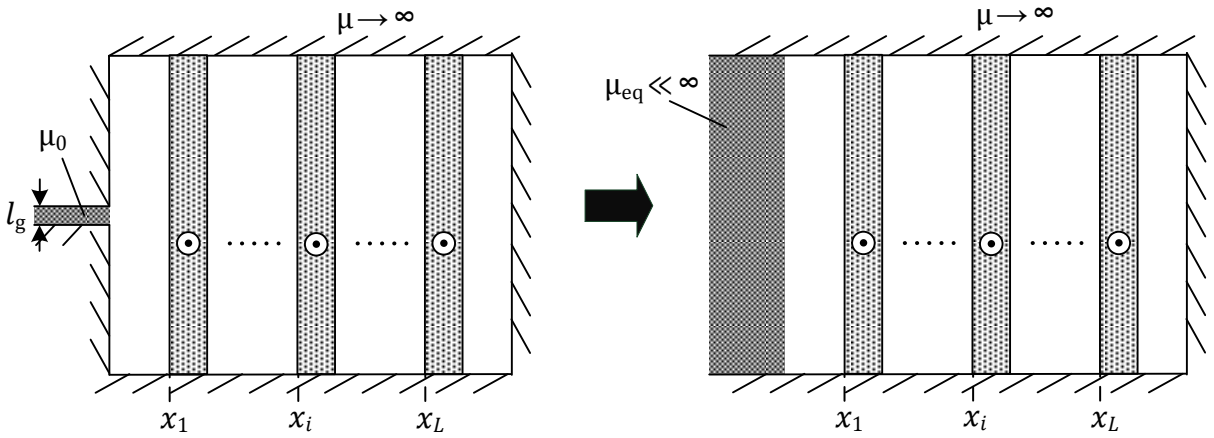

Fig. 3.19: 1-D approximation of a choke with center-legged air gap

In this model the magnetic field H_i of the single layers is calculated by Amperes law. The current flowing in every layer according to (3.65) is given by

$$I_i' = I_\mathrm{w} \frac{N_\mathrm{w}}{N_\mathrm{hw}'} \,. \tag{3.69}$$

Starting point is the magnetic field in layer L which is a superposition of the magnetic field of the own current

$$H_\mathrm{y}(x_L + h_L) = -H_\mathrm{y}(x_L) = I_i'/(2b_\mathrm{w})$$

and the external magnetic field

$$H_\mathrm{y}(x_L + h_L) = H_\mathrm{y}(x_L) = H_L \,.$$

Since the magnetic field in the core material with $\mu \to \infty$ must be zero such that

$$H_\mathrm{y}(x_L + h_L) = H_L + I_i'/(2b_\mathrm{w}) \equiv 0 \,,$$

the external magnetic field H_i at layer L is given by

$$H_L = -I_i'/(2b_\mathrm{w}) \,. \tag{3.70}$$

Hence the magnetic field in the layer at position x_i is given by

$$H_{\mathrm{y},i} = \sum\nolimits_{j=i}^{L-1} \frac{-I_i'}{b_\mathrm{w}} + (-I_i')/(2b_\mathrm{w}) = \frac{(L - i + 0.5)}{b_\mathrm{w}} (-I_i') \,. \tag{3.71}$$

By combining (3.67) with (3.65) and (3.71) the power loss of the whole winding is

$$P_\mathrm{v} = \sum_{i=1}^{N_\mathrm{hw}'} N_\mathrm{bw}' R_{\mathrm{DC\_strand},i} \left[F_\mathrm{s\_round}(\gamma) \left(\frac{N_\mathrm{w} I_\mathrm{w}}{N_\mathrm{hw}' N_\mathrm{bw}'} \right)^2 + F_\mathrm{p\_round}(\gamma) (\pi d)^2 \left(\frac{(L - i + 0.5) N_\mathrm{w} I_\mathrm{w}}{N_\mathrm{hw}' b_\mathrm{w}} \right)^2 \right]. \tag{3.72}$$

Assuming that the packing density p_w is independent of N_w, (3.72) can be rewritten as

$$P_\mathrm{v} = R_\mathrm{AC} I_\mathrm{w}^2 \quad \text{with} \quad R_\mathrm{AC} \sim N_\mathrm{w}^2 \,. \tag{3.73}$$

Now considering the fringing field, its coordinate dependent intensity is unknown. But since the core material is assumed to be linear, the intensity of the fringing field $\vec{H}_\mathrm{fr}$ will be proportional to the core flux and a factor K_fr can be assumed such that

$$\left| \vec{H}_\mathrm{fr}(x, y) \right| = K_\mathrm{fr}\, \Phi = K_\mathrm{fr} N_\mathrm{w} I_\mathrm{w} \mu_\mathrm{eq} \frac{A_\mathrm{g}}{b_\mathrm{w}} \,. \tag{3.74}$$

Because the size of every strand compared to the overall arrangement is small, it is feasible to assume a uniform external magnetic field $\vec{H}_{\mathrm{fr}}(x_{\mathrm{strand}}, y_{\mathrm{strand}})$ throughout the strands cross-sectional area. By superimposing the fringing field intensity, (3.66) becomes

$$\begin{aligned} P_{\mathrm{v\_strand},i} &= R_{\mathrm{DC\_strand},i}(F_{\mathrm{s\_round}}(\gamma)\, I_{\mathrm{st},i}^2 + F_{\mathrm{p\_round}}(\gamma)(\pi d)^2\left(H_{\mathrm{y},i} + \left|\vec{H}_{\mathrm{fr}}(x_{\mathrm{strand}}, y_{\mathrm{strand}})\right|\right)^2 \\ &= R_{\mathrm{DC\_strand},i}(F_{\mathrm{s\_round}}(\gamma) I_{\mathrm{st},i}^2 + F_{\mathrm{p\_round}}(\gamma)(\pi d)^2\left(H_{\mathrm{y},i} + K_{\mathrm{fr}} N_{\mathrm{w}} I_{\mathrm{w}} \mu_{\mathrm{eq}} \frac{A_{\mathrm{g}}}{b_{\mathrm{w}}}\right)^2). \end{aligned} \tag{3.75}$$

Combining (3.75) and (3.65) and (3.71), again the term $(N_{\mathrm{w}} I_{\mathrm{w}})^2$ can be isolated, such that the proportionality $R_{\mathrm{AC}} \sim N_{\mathrm{w}}^2$ remains valid. Additionally it needs to be considered that the optimization procedure presented in Chapter 5 also varies the air gap length l_{g} of the choke and that the factor K_{fr} in (3.75) is non-lineary dependent on l_{g}. An analytical approach to calculate the fringing field intensity in dependence on l_{g}, $\vec{H}_{\mathrm{fr}}(x, y, l_{\mathrm{g}})$, is given in [Wallmeier]. However, the analytical approach is not adopted in this work for its higher computational effort. Instead, it is assumed in a first step that the optimization procedure yields results that are close to the original measured component, i.e. $l_{\mathrm{g}} \approx l_{\mathrm{g0}}$, and in consequence also the variation of the losses due to a modified fringing field distribution is small and negligible. If the latter assumption cannot be confirmed after the first optimization run, a choke exhibiting an air gap length value l_{g} closer to the value directed by the first optimization run needs to be build up and remeasured in order to increase the accuracy of the optimization result. The empirical loss modeling then reduces to the steps:

1. Build up a sample component with best estimated values for l_{g0} and N_0.
2. Measure the loss characteristic $R_{\mathrm{AC}}(f, l_{\mathrm{g0}}, N_{\mathrm{w0}}, T_{\mathrm{w0}})$.
3. Perform the design optimization with the loss calculation according to
   $$R_{\mathrm{AC}}(f, N_{\mathrm{w}}, T_{\mathrm{w}}) = R_{\mathrm{AC}}\left(f, l_{\mathrm{g0}}, N_{\mathrm{w0}}, T_{\mathrm{w0}}\right)(N_{\mathrm{w}} - N_{\mathrm{w0}})^2\left(1 + \alpha_{\mathrm{T}}(T_{\mathrm{w}} - T_{\mathrm{w0}})\right).$$ [8]
5. If the optimized result yields air gaps significantly different to l_{g0} , build another sample component with a more appropriate air gap and measure $R_{\mathrm{AC}}(f, l_{\mathrm{g0}}, N_{\mathrm{w0}}, T_{\mathrm{w0}})$ again.
6. Repeat steps 3) and 4) as necessary.

3.2.3.4 Copper Loss Modeling of the LLC Transformer

For the copper loss modeling of the LLC transformer two cases are distinguished. The primary winding of the transformer is always considered as a litz winding. The secondary winding is considered as a litz winding for high voltage outputs like battery chargers, and as a foil winding for low voltage outputs like server and telecom power supplies. In case of foil windings the approximation presented for litz windings is not valid, because the number of layers changes if the number of turns changes for the foil winding. The consideration of a loss model

[8] The consideration of temperature dependence in this equation is based on the temperature dependence of the DC resistance of the wire. Strictly also the skin depth is dependent on the temperature due to its dependency on the material conductivity (c.f. (3.54)). Since the temperature dependency of R_{AC} is not processed in this work for a thermal model and the temperature dependency of the DC resistance is considered as the major influence path, the temperature dependency of the skin depth is neglected in the following.

for foil windings with varying number of turns would lead to a more involved computation compared to (3.73), but which is not covered in this work. However, in case of low voltage outputs the number of turns of the transformer and the transformer turns ratio in reality have a relative coarse quantization. Typically only few variants are feasible, which alternatively should be addressed by comparative measurements.

For the loss modeling of the LLC transformer the impact of an integration of the choke L_p of the LLC resonant circuit into the transformer has to be studied. For this work and its applications L_p is considered to be integrated into the transformer, since this is an effective measure in terms of costs and power density aspects. The integration of L_p leads to a formal superposition of two classes of current densities (c.f. Fig. (3.53)). First class is the current density J_{z_xf} associated with the transformer operation. This current density is characterized in that the overall magnetomotive force $\Theta_{xf}(t)$ in the winding window is zero because $i_o(t) = n i_r(t)$. The second class is the current density J_{z_m} associated with the inductance L_p and is linked to a mutual core flux $\Phi_m(t)$ such that

$$\Theta_{Lp}(t) = \Phi_m(t)\frac{l_g}{\mu_0 A_g} = N_p\left(i_r(t) - \frac{i_o(t)}{n}\right) = N_p i_p(t)\,. \tag{3.76}$$

Hence the current $i_p(t)$ is the magnetizing current of the transformer.

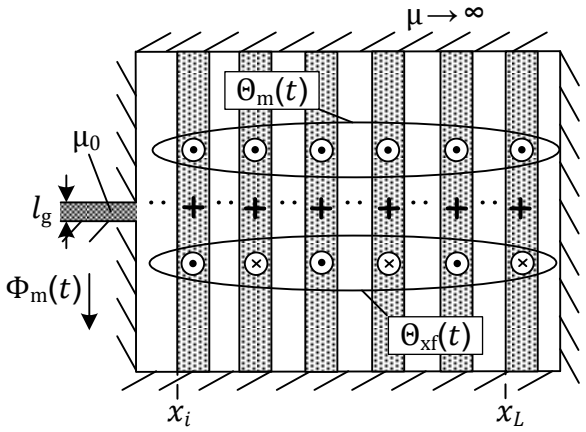

Fig. 3.20: 1-D approximation of an L_p-integrated transformer

For an exact solution both current density classes could not be separated and must be treated comprehensively by choosing appropriate boundary values when solving (3.54), at which in that more general case the phasors $H_y(x_i + h_i)$ and $H_y(x_i)$ are no more of equal phase [Brockmeyer]. Although this would be analytically solvable, it would not be possible to model the losses associated with the mutual flux current by a single R_{AC} characteristic that moreover could be acquired by measurement.
Hence, a practical workaround to the exact solution is proposed here. Fig. 3.21 shows the harmonic content of the transformer currents $i_o(t)$ and $i_p(t)$ of a LLC converter operating at different switching frequencies. The chosen design parameters are typical values of an LLC converter applied in a power supply and operating in a high load range. It can be observed that the fundamental components of $i_o(t)$ and $i_p(t)$ are nearly orthogonal to each other for the below resonance region $F_n < 1$. Close to resonance at $F_n = 0.997$ the third and fifth harmonics of $i_o(t)$ and $i_p(t)$ are not orthogonal to each other, but $i_o(t)$ comprises just a negligible amount of them. Below resonance at $F_n = 0.758$ the amount of the third and fifth harmonics is

higher, but the third harmonic is close to orthogonal between $i_o(t)$ and $i_p(t)$. In consequence for the below resonance region it is feasible to assume orthogonality between $i_o(t)$ and $i_p(t)$ without introducing relevant errors.

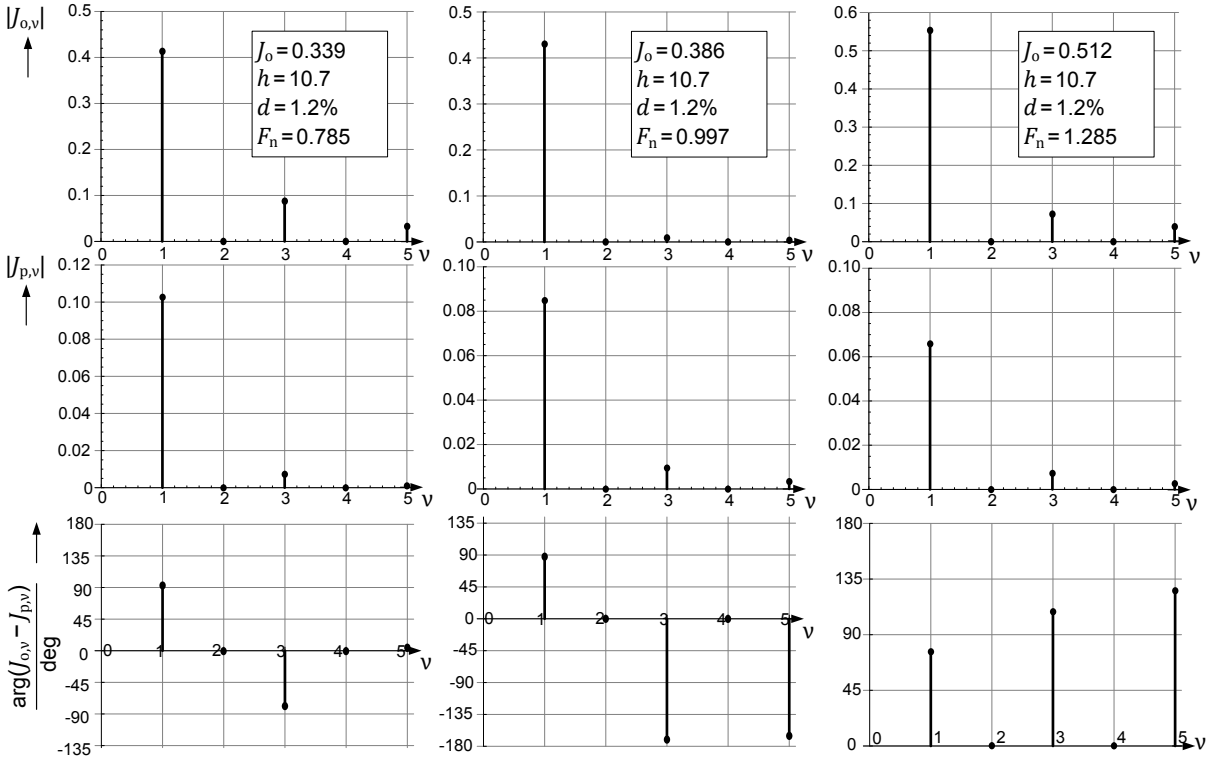

Fig. 3.21: Harmonic analysis ($\nu \leq 5$) of current waveforms of a LLC converter operating with typical design parameters

The assumption of orthogonality between $i_o(t)$ and $i_p(t)$ is problematic in the above resonance region. At $F_n = 1.285$ the fundamental harmonic has a phase difference of appr. 76°, which no longer justifies the assumption of orthogonality. Also a considerable amount of the third harmonic is present in $i_o(t)$ and $i_p(t)$ with phase difference of appr. 108°. For the scope of this work, the error produced by the orthogonality assumption in the above resonance region will be accepted. This is a necessary step for minimizing the computation times of the optimization solver presented in Chapter 5. The error produced in the optimization result is limited due to the fact, that for every design variant that is processed by the optimization solver a similar error in the transformer copper losses results. Another point is, that the efficiency optimization aimed by the optimization solver typically yields operating points close to resonance, if the LLC converter is applied in server and telecom power supplies. And close to resonance, the error introduced by the orthogonality assumption is assumed to be negligible based on the above analysis.

Assuming orthogonality between $i_o(t)$ and $i_p(t)$, the losses generated by each current density class can be calculated separately as it is justified for orthogonal harmonics. The separate current densities can be calculated by the same methods presented in paragraph 3.2.3.3. For the current density class J_{z_xf} , which is linked to $i_o(t)$, the magnetic field $H_{y,i}$ must be calculated according to the sign of the magneto motive force of each layer, because layers associated with the primary winding have different sign than those of the secondary winding. The R_{AC}

characteristic according to the current densities $J_{\mathrm{z\_xf}}$ can be measured by shorting out one winding of the L_p-integrated transformer while measuring at the other winding. It is designated $R_{\mathrm{AC\_xf\_p}}(f)$ if measured at the primary winding and $R_{\mathrm{AC\_xf\_s}}(f)$ if measured at the secondary winding, where $R_{\mathrm{AC\_xf\_p}}(f) = n^2 R_{\mathrm{AC\_xf\_s}}(f)$ can be used to verify the correctness of the measurement.

For the current density class $J_{\mathrm{z\_m}}$, which is linked to $i_{\mathrm{p}}(t)$, first the current distribution between the windings must be determined. Since

$$i_{\mathrm{r}}(t) = i_{\mathrm{o}}(t) + i_{\mathrm{p}}(t) \quad \text{and} \quad I_{\mathrm{r}}^2 \approx I_{\mathrm{o}}^2 + I_{\mathrm{p}}^2 \,, \tag{3.77}$$

the magnetizing current must be treated as flowing in the primary winding of the transformer. Hence the magnetic field $H_{\mathrm{y},i}$ must be calculated by considering $i_{\mathrm{p}}(t)$ in the primary winding and neglecting the secondary winding. The R_{AC} characteristic can be measured at the primary winding while the secondary winding being open circuited. It is designated $R_{\mathrm{AC\_m\_p}}(f)$. The overall copper losses are finally given by

$$P_{\mathrm{v}} = R_{\mathrm{AC\_xf\_p}} I_{\mathrm{o}}^2 + R_{\mathrm{AC\_m\_p}} I_{\mathrm{p}}^2 \,. \tag{3.78}$$

In the optimization example presented in Chapter 5.4 the width of the winding window b_{w} is used additionally as a free design parameter. Therefore the proportionality $R_{\mathrm{AC}} \sim 1/b_{\mathrm{w}}$ is incorporated. This proportionality can be deduced from (3.72) for litz windings and from (3.60) for foil windings considering that $H_{\mathrm{y},i} \sim 1/b_{\mathrm{w}}$ according to Ampere's law.

3.2.3.5 Copper Loss Measuring Principal

An important point of the presented copper loss model is the conduction of the measurements of the R_{AC} characteristic. Commonly the measurement of passive two-port components is performed by an impedance analyzer (IA), e.g. the 4294a from Keysight Technologies [Keysight]. The IA is able to measure the complex small-signal impedance of the two-port element at a certain frequency and to sweep the measurement frequency over a desired range. The measured impedance can be interpreted according to an equivalent circuit of the two-port element. For magnetic components the equivalent circuit of a L_{eq}-R_{eq} series connection can be used. Under the assumption of the loss model of Chapter 3.2.3.2, namely the linearity of the material and the DEs, the measured small-signal characteristic is identical to the large-signal characteristic. It therefore can be stated that the characteristic of the equivalent resistance R_{eq} is equal to the R_{AC} characteristic for the copper loss calculation (3.73) under the following assumption:
The core losses are small compared to the copper losses at the applied excitation amplitude of the IA. This assumption is valid for short-circuit measurements at transformers, e.g. the measurement of $R_{\mathrm{AC\_xf\_p}}(f)$. It is not valid for chokes with un-gapped cores. The validity for chokes with gapped cores depends on the concrete component. In case of the resonant choke L_s the assumption is typically valid, because the component is built as an energy storage element, and therefore is constructed with a distinctive air gap (e.g. > 1.5 mm, c.f. Chapter 5.4). Due to the air gap the magnetic resistance of the core is high and the resulting flux low compared to the current linkage. In case of the parallel choke L_p the assumption is critical, be-

cause of the typically small air gap of L_p (e.g. < 1 mm, c.f. Chapter 5). Hence in this work the measured R_{AC} characteristic $R_{AC\_m\_p}(f)$ of L_p is verified respectively corrected by a comprehensive large-signal loss measurement. The copper losses are calculated by the difference between the overall-losses of the component and the core losses. Both losses are measured according to Chapter 3.2.3.1. For the overall losses just the original component is used, at which the original winding is used as the excitation and sense winding simultaneously. The results of the small-signal measurements and the compensation function resulting from the large signal measurements are presented in appendix 9.2.2 for the application example of Chapter 5.4. Because the compensation function could not be determined on the original core during this work, it needs to be considered as approximative (c.f. appendix 9.2.2). But since the loss component linked to $R_{AC\_m\_p}(f)$ is small (c.f. Fig. 5.16), the accuracy of the design optimization and its analysis results are considered to be feasible despite possible errors in the prediction of the R_{AC} characteristic of L_p.

4 Controlling of the LLC Converter

4.1 Controlling Needs and Concepts

For the controlling of a DC-DC power converter generally two aspects can be distinguished:

- For all operating points within the desired operating range of input voltages, output voltages and output loads an equilibrium operation must be supported by the converter.
- Besides the equilibrium operation the feedback-loop(s) closed by the controlling measures must be stable at every operating condition and the dynamic response has to be sufficient.

According to the steady-state characteristic of the LLC converter (c.f. Fig. 4.1) an equilibrium operation is achieved if the switching frequency F_n is set in accordance to the output loading J_o and input to output voltage ratio M. An important point is that the slope of the DC-DC gain in dependence on F_n is monotonic at every load condition, provided that the lower switching frequency limit is higher than the peak gain point at maximum output loading:

$$F_{\mathrm{n,min}} \geq F_{\mathrm{n,pg}} \quad \text{with} \quad M\left(J_{\mathrm{o,max}}, F_{\mathrm{n,pg}}\right) = M_{\mathrm{pg}}\left(J_{\mathrm{o,max}}\right) \;\&\; M\left(F_{\mathrm{n,min}}\right) \geq \mathrm{M_{max}}\,. \qquad (4.1)$$

Condition (4.1) has to be achieved by design; otherwise the slope reverse of the DC-DC gain results in a positive feedback of the control loop, which will trap the controller.

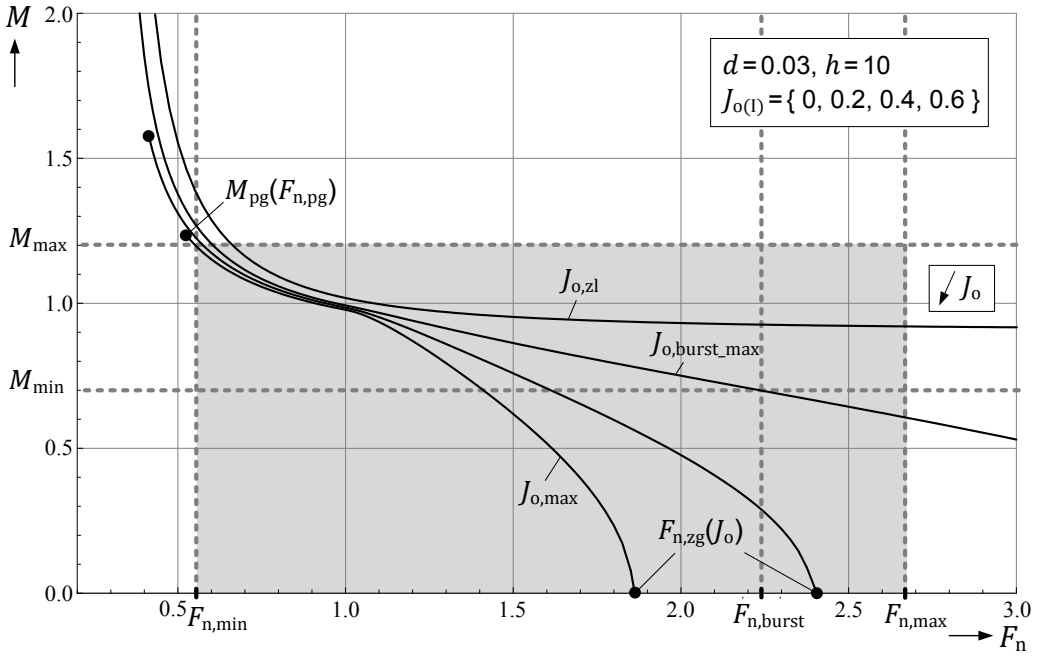

Fig. 4.1: DC-DC gain diagram of the LLC converter illustrating the operating range and its boundaries.

An intricate point, which is generally critical to resonant converters, is the ability to support an equilibrium operation at light and zero output loads. In case of the LLC converter F_n is in-

creased at decreasing output load. The ability of the LLC converter to supply light loads is expressed at least by the condition $J_{\mathrm{o,min}} \leq M_{\mathrm{min}}$, and more stringent by the condition

$$M\left(J_{\mathrm{o,min}}, F_{\mathrm{n,max}}\right) \leq M_{\mathrm{min}} . \tag{4.2}$$

The abidance of (4.2) has to be verified by calculating the DC-DC gain $M(J_{\mathrm{o,min}}, F_{\mathrm{n,max}})$. Since this operating point most probably is served by the DCMAB mode, (4.2) cannot be analytically treated but must be verified by numerically solving the DCMAB mode. The ability of the LLC converter to maintain a certain output voltage at zero load $J_{\mathrm{o,zl}}$ can be tested by calculating the zero load output voltage of the LLC converter $V_{\mathrm{o,zl}}(F_{\mathrm{n}})$. This voltage is given by the maximum voltage at $\mathrm{L_p}$ during one switching period in the Cutoff mode, because as such the output rectifier is at the boundary of getting forward biased [Lazar]. It can be analytically determined resulting in the zero load gain

$$M_{\mathrm{zl}}(F_{\mathrm{n}}) = \frac{h}{1+h} \frac{1/n}{\cos\left[\frac{\pi}{2} \frac{1}{F_{\mathrm{n}}\sqrt{1+h}}\right]} . \tag{4.3}$$

If

$$M_{\mathrm{zl}}\left(F_{\mathrm{n,max}}\right) \leq M_{\mathrm{min}} , \tag{4.4}$$

the LLC converter can regulate at zero load and (4.2) is met as well. Often (4.2) resp. (4.4) cannot be met in practical design cases or F_{n} has to be increased to high values resulting in a very inefficient operation due to switching related losses, which are proportional to f_{s}. A common method here to enable zero load equilibrium operation or to increase the efficiency of this operation point is burst mode operation. In this mode the energy transfer is limited by introducing blanking times to the bridge driving signals. The burst mode operation effectively limits the light load switching frequency range by defining a maximum frequency F_{burst} that represents the boundary between normal and burst mode operation. This boundary is reached below a certain output loading $J_{\mathrm{o,burst\_max}}$. The output loading in burst mode is limited due to the increased output voltage ripple that is generated by the burst pulses. By defining F_{burst} and $J_{\mathrm{o,burst\_max}}$ the light load condition (4.2) changes to

$$M\left(J_{\mathrm{o,burst\_max}}, F_{\mathrm{n,burst}}\right) \leq M_{\mathrm{min}} . \tag{4.5}$$

Another critical point within the steady-state operating range is the short-circuit state of the output defined by $M(J_{\mathrm{o,max}}) = 0$. The ability of the LLC converter to limit the short-circuit output current is expressed by the condition

$$F_{\mathrm{n,zg}}\left(J_{\mathrm{o,max}}\right) \leq F_{\mathrm{n,max}} . \tag{4.6}$$

The compliance of the LLC converter to the steady-state operating range described by (4.1) - (4.6) is a matter of the optimal converter design, which is addressed by Chapter 5.

The dynamic control of the LLC converter in a server or telecom PSU has the function to regulate a constant output voltage V_{o}. Disturbing quantities are the output load and the DC-link voltage. The output voltage control loop of resonant converters distinguish from that of PWM type converters: Most PWM type converters exhibit the two state variables inductor current

and output capacitor voltage. By applying a cascaded control structure by an underlying current control loop and an outer voltage control loop all major state variables of the converter are under direct control, which typically results in very acceptable control behavior and bandwidth. In contrast the LLC converter exhibits as well the state variable output capacitor voltage, but also further three state variables resulting from the three resonant circuit elements.

Generally two control methods for the LLC converter are known:

1. The most common and simple control method is to treat the LLC converter as a SISO (Single Input Single Output System) and use a single feedback control loop realized by classical PID compensator design. Hereby the output capacitor voltage is the controlled variable and the switching frequency the manipulated variable.
2. Further more sophisticated control methods incorporate some or all fast varying state variables of the LLC resonant circuit. Those methods are commonly referred to as trajectory control or optimal trajectory control (OTC) ([Chen], [Feng], [Feng2]). But the implication of trajectory control is an accurate and fast measurement of the state variables. Optimally all waveforms $i_{\mathrm{r}}(t)$, $v_{\mathrm{Cs}}(t)$ and $i_{\mathrm{p}}(t)$ needs to be sampled at least once per switching period at a defined time instant. The sampled values then need to be processed very fast to decide about the next switching actions. However, such signal processing is not realizable with actual budgetary DSP controllers that are available for mass produced PSUs. Therefore, e.g. in [Feng2], a simplified control measure based on the OTC analysis of the LLC converter is added to a classical SISO control loop to improve the step load response. This measure can be implemented on budgetary DSP controllers and achieves beneficial results.

With respect to a budgetary implementation of the control method the classical SISO principal is examined in this work. Hereby the quality of the output voltage control depends on the transfer characteristic of the LLC converter and an appropriate PID compensator design.

A further aspect of controlling a LLC resonant converter is the implementation of the Synchronous Rectification functionality (SR). The application of SR distinctively increases the efficiency of low output voltage LLC converters. The prototypes used for evaluation in this chapter and in Chapter 6 include SR. Also the design optimization method presented in Chapter 5 assumes the application of SR. However, the SR implementation for the LLC converter has additional implications compared to the SR implementation for PWM type converters. Numerous publications, mainly publicized throughout the last years, deal with the SR for LLC topic (e.g. [Fu], [Wang], [Feng4], [Ho], [Wang2], [Wang3], [Liu], [Figge]). [Figge] includes the concept of SR implementation that is applied on the prototypes investigated in this chapter and Chapter 6.

4.2 Small-Signal Modeling and Compensator Design

4.2.1 Small-Signal Modeling

In order to stabilize a SISO feedback loop the small-signal transfer behavior of the plant has to be known. In the industrial PSU design praxis the experimental measurement of the feedback loop characteristic is common. On the one hand this is due to the enhanced theoretical background necessary to analytically derive the transfer behavior of a power conversion cir-

cuit. On the other hand it is often difficult to include parasitic effects and non-idealities of components in a theoretical model, which degrades the model accuracy to certain degrees. It is therefore compulsory to verify an analytical derived transfer behavior and the compensator designs based here upon by final measurements. With this background the theoretical EDF-1 method is recapitulated here to study the principal transfer-behavior of the LLC converter. The EDF-1 method considers only the DC and fundamental harmonic components of the waveforms and therefore is of approximate nature. It is proposed as a basis for initial compensator design and parameter studies.

The EDF designation is derived from the describing function (DF) concept of [Gelb]. The DF concept is related to the frequency response of nonlinear transfer blocks with input to output functionality $y(t) = f_{\mathrm{nl}}(x(t))$. It assumes that for a nonlinear block located within a bandwidth limited environment, the frequency response of f_{nl} can be approximated by neglecting the side-band components generated by the nonlinear behavior such that

$$f_{\mathrm{nl}}(\Re\{Xe^{j\omega t}\}) \approx \Re\{F_{\mathrm{EDF}}(X)e^{j\omega t}\}\,. \tag{4.7}$$

The EDF method extends the DF idea to a multi variable system $f_{\mathrm{nl}}(\boldsymbol{x},\boldsymbol{u},s(t)) \rightarrow F_{\mathrm{DF}}(\boldsymbol{X},\boldsymbol{u},q)$ with harmonic vector $\boldsymbol{X}$, input vector $\boldsymbol{u}$ and $s(t)$ control variable q. Provided that

$$x(t) = \sum_{\nu=-\infty}^{\nu=+\infty} X_\nu e^{j\nu\omega t} \tag{4.8}$$

the harmonic vector $\boldsymbol{X}$ contains a limited number of Fourier coefficients of the signals of all state variables of the system. The requisite of calculating the transfer behavior additionally requires the generalization of time dependence of the Fourier coefficients $\boldsymbol{X} \rightarrow \boldsymbol{X}(t)$. Therefore the calculation of the Fourier coefficients is defined by a sliding integration window with length $2\pi/\omega$ according to

$$X_\nu(t) = \frac{\omega}{2\pi}\int_{t-\frac{2\pi}{\omega}}^{t} x(\tau)e^{-j\nu\omega\tau}d\tau \tag{4.9}$$

$$x(t+\tau-2\pi/\omega) = \sum_{\nu=-\infty}^{\nu=+\infty} X_\nu(t)e^{j\nu\omega(t+\tau-2\pi/\omega)}\,, \quad \tau \in [0..2\pi/\omega]\,. \tag{4.10}$$

The DF idea seems to be well applicable to resonant converters due to the filtering characteristic of the resonant circuit.

Starting point of the EDF-1 model is a state-space description of the converter operation for the desired operating mode. Based on the equivalent circuit of Fig. 4.2 the CCMA mode is represented by the state space model (4.11) and output equations (4.12). The underlined terms are nonlinear functions that must be treated specially in the harmonic approximation. The simple representation (4.11) is not possible for the DCMB2 mode due to the discontinuous conduction of the output rectifier. In order to not complicate the model the effect of discontinuous conduction is neglected here like it is done by the FHA. In consequence (4.11) is as well

used to model the DCMB2 mode and the modeling error is tolerated and must be kept in mind.

$$\begin{aligned}
\frac{d}{dt}i_\mathrm{r} &= \frac{1}{L_\mathrm{s}}[\underline{v_\mathrm{gAB}} - i_\mathrm{r}R_\mathrm{s} - v_\mathrm{cs} - ((R_\mathrm{d}+R')\underline{|i_\mathrm{r}-i_\mathrm{p}|} + R'i_\mathrm{o} + R'/R_\mathrm{c}v_\mathrm{Co})\underline{sgn(i_\mathrm{r}-i_\mathrm{p})}]\\
\frac{d}{dt}v_\mathrm{Cs} &= \frac{1}{C_\mathrm{s}}i_\mathrm{r}\\
\frac{d}{dt}i_\mathrm{p} &= \frac{1}{L_\mathrm{p}}[((R_\mathrm{d}+R')\underline{|i_\mathrm{r}-i_\mathrm{p}|} + R'i_\mathrm{o} + R'/R_\mathrm{c}v_\mathrm{Co})\underline{sgn(i_\mathrm{r}-i_\mathrm{p})}]\\
\frac{d}{dt}v_\mathrm{Co} &= \frac{1}{C_\mathrm{o}}\frac{R'}{R_\mathrm{c}}[\underline{|i_\mathrm{r}-i_\mathrm{p}|} + i_\mathrm{o} - \frac{1}{R}v_\mathrm{Co}]
\end{aligned} \tag{4.11}$$

$$\begin{aligned}
i_\mathrm{gAV} &= \overline{i_\mathrm{r}\underline{sgn(v_\mathrm{gAB})}} = \frac{1}{T_\mathrm{s}}\int_0^{T_\mathrm{s}} i_\mathrm{r}\frac{v_\mathrm{gAB}}{V_\mathrm{g}}dt\\
v_\mathrm{o} &= R'\underline{|i_\mathrm{r}-i_\mathrm{p}|} + R'I_\mathrm{o} + \frac{R'}{R_\mathrm{c}v_\mathrm{Co}} \qquad \text{with} \quad R' = \frac{R_\mathrm{L}R_\mathrm{c}}{R_\mathrm{L}+R_\mathrm{c}}
\end{aligned} \tag{4.12}$$

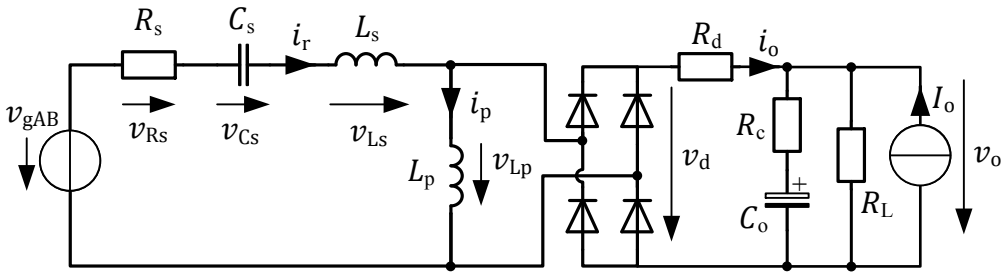

Fig. 4.2: Extended equivalent circuit for EDF modeling of the LLC converter

The key step of the EDF-1 method is the approximation of the state-space model (4.11) by the DC and fundamental harmonic components of the state variables and the manifestation of the harmonic balance. The harmonic balance equates the amplitude and phase information of the state variables between the left and right side of (4.11) according to

$$\begin{aligned}
\frac{d}{dt}\begin{bmatrix} X_{\nu,0}(t)e^{j\nu\omega_\mathrm{s}t} \\ \vdots \\ X_{\nu,n}(t)e^{j\nu\omega_\mathrm{s}t} \end{bmatrix} &= \begin{bmatrix} \left(\frac{d}{dt}X_{\nu,0}(t) + j\nu\omega_\mathrm{s}X_{\nu,0}(t)\right)e^{j\nu\omega_\mathrm{s}t} \\ \vdots \\ \left(\frac{d}{dt}X_{\nu,n}(t) + j\nu\omega_\mathrm{s}X_{\nu,n}(t)\right)e^{j\nu\omega_\mathrm{s}t} \end{bmatrix}\\
&\equiv \begin{bmatrix} F_{\mathrm{EDF},0}\big(\boldsymbol{X}(t),\boldsymbol{u}(t),q(t)\big)e^{j\nu\omega_\mathrm{s}t} \\ \vdots \\ F_{\mathrm{EDF,n}}\big(\boldsymbol{X}(t),\boldsymbol{u}(t),q(t)\big)e^{j\nu\omega_\mathrm{s}t} \end{bmatrix}\\
\text{with} \quad \boldsymbol{X}(t) &= \begin{bmatrix} X_{\nu,0}(t) \\ \vdots \\ X_{\nu,n}(t) \end{bmatrix}, \quad n\text{: length of } \boldsymbol{X}(t)\,.
\end{aligned} \tag{4.13}$$

In case of resonant converters the expressions (4.9), (4.10), (4.13) are not exact because the switching frequency is a control variable and therefore time dependent: $\omega_s \rightarrow \omega_s(t)$. Accounting for this the Fourier coefficients need to be defined along an angle φ which is linked to time by the angle function $\Phi(t)$. As such the signal function $x(t)$ and its Fourier coefficients have the expression

$$X_\nu(t) = \frac{1}{2\pi}\int_{\Phi(t)-2\pi}^{\Phi(t)} x\left(\Phi^{-1}(\varphi)\right)e^{-j\nu\varphi}d\varphi \quad \text{with} \quad \frac{d\Phi(t)}{dt} = \omega_s(t) \tag{4.14}$$

$$x(t+\tau-T(t)) = \sum_{\nu=-\infty}^{\nu=+\infty} X_\nu(t)e^{j\nu\Phi(t+\tau-T(t))}\,, \quad \tau \in [0..T(t)]\,, \tag{4.15}$$

in which $T(t)$ now is defined as the time period in which the phase function $\Phi(t)$ varies exactly by 2π in the interval $[t-T(t), t]$. $T(t)$ can be calculated by solving the equation

$$\int_{t-T(t)}^{t} \omega(\tau)d\tau \equiv 2\pi \tag{4.16}$$

The harmonic balance equation (4.13) is generalized such that (4.17) results.

$$\begin{aligned}\frac{d}{dt}\begin{bmatrix} X_{\nu,0}(t)e^{j\nu\Phi(t)} \\ \vdots \\ X_{\nu,n}(t)e^{j\nu\Phi(t)}\end{bmatrix} &= \begin{bmatrix}\left(\frac{d}{dt}X_{\nu,0}(t) + j\nu\omega_s(t)X_{\nu,0}(t)\right)e^{j\nu\Phi(t)} \\ \vdots \\ \left(\frac{d}{dt}X_{\nu,n}(t) + j\nu\omega_s(t)X_{\nu,n}(t)\right)e^{j\nu\Phi(t)}\end{bmatrix} \\ &\equiv \begin{bmatrix} F_{\mathrm{EDF},0}\left(\boldsymbol{X}(t), \boldsymbol{u}(t), q(t)\right)e^{j\nu\Phi(t)} \\ \vdots \\ F_{\mathrm{EDF,n}}\left(\boldsymbol{X}(t), \boldsymbol{u}(t), q(t)\right)e^{j\nu\Phi(t)}\end{bmatrix}\end{aligned} \tag{4.17}$$

In [Sanders] the implication of time dependent switching frequency is analyzed by derivating the Fourier coefficient (4.14) with respect to time. The calculation yields additional terms in the harmonic balance equation, but which are shown to approach zero as a limiting value for $\dot{\omega_s} \rightarrow 0$. He concludes that therefore the neglection of the time varying frequency in the model is a good approximation. In the following, the application of the EDF-1 method on the LLC resonant converter is conducted with neglection of the time varying frequency for calculating the Fourier coefficients. Instead the circuit is assumed to be in a steady state during the integration period of the Fourier coefficients, at which (4.9) is written as

$$X_\nu(t) = \frac{\omega_s(t)}{2\pi}\int_{t-\frac{2\pi}{\omega_s(t)}}^{t} x(\tau)e^{-j\nu\omega_s(t)\tau}d\tau\,. \tag{4.18}$$

This simplification can be described as a quasi-stationary approach. It is conceivable that the impact of the quasi-stationary approach on the accuracy of the EDF-1 method increases the closer the excitation frequency is to the switching frequency of the converter.

The fundamental harmonic approximation of (4.11) is done for the real representation of a Fourier series expansion due to convenient notation:

$$x(t) = x_0(t) + x_c(t)\cos\big(\Phi(t)\big) + x_s(t)\sin\big(\Phi(t)\big) \tag{4.19}$$

As such the state variables are approximated by

$$\begin{aligned} i_r(t) &\approx i_{r,c}(t)\cos\big(\Phi(t)\big) + i_{r,s}\sin\big(\Phi(t)\big) \\ v_{Cs}(t) &\approx v_{Cs,c}(t)\cos\big(\Phi(t)\big) + v_{Cs,s}(t)\sin\big(\Phi(t)\big) \\ i_p(t) &\approx i_{p,c}(t)\cos\big(\Phi(t)\big) + i_{p,s}(t)\sin\big(\Phi(t)\big) \\ v_{Co}(t) &\approx V_{Co}(t)\,, \end{aligned} \tag{4.20}$$

and the derivatives of the harmonic state variables can be written as

$$\begin{aligned} \frac{d}{dt}i_r(t) &\approx \Big(\frac{d}{dt}i_{r,c}(t) + \omega_s(t)i_{r,s}(t)\Big)\cos\big(\Phi(t)\big) \\ &+ \Big(\frac{d}{dt}i_{r,s}(t) - \omega_s(t)i_{r,c}(t)\Big)\sin\big(\Phi(t)\big) \\ \frac{d}{dt}v_{Cs}(t) &\approx \Big(\frac{d}{dt}v_{Cs,c}(t) + \omega_s(t)v_{Cs,s}(t)\Big)\cos\big(\Phi(t)\big) \\ &+ \Big(\frac{d}{dt}v_{Cs,s}(t) - \omega_s(t)v_{Cs,c}(t)\Big)\sin\big(\Phi(t)\big) \\ \frac{d}{dt}i_p(t) &\approx \Big(\frac{d}{dt}i_{p,c}(t) + \omega_s(t)i_{p,s}(t)\Big)\cos\big(\Phi(t)\big) \\ &+ \Big(\frac{d}{dt}i_{p,s}(t) - \omega_s(t)i_{p,c}(t)\Big)\sin\big(\Phi(t)\big)\,. \end{aligned} \tag{4.21}$$

The harmonic coefficient vector (hcv) becomes

$$\boldsymbol{x}_{hcv} = \big(i_{r,s}\,,\, i_{r,c}\,,\, v_{Cs,s}\,,\, v_{Cs,c}\,,\, i_{p,s}\,,\, i_{p,c}\,,\, V_{Co}\big)^T\,. \tag{4.22}$$

To complete the model the fundamental harmonic components of the nonlinear functions of (4.11) and (4.12) must also be extracted. The function $\underline{v_{gAB}}$ is a square wave with amplitude V_g and by defining the square wave of $\underline{v_{gAB}}$ as odd function its fundamental component is

$$\underline{v_{gAB}}(t)_{<1>} = \frac{4}{\pi}V_g\sin\big(\Phi(t)\big). \tag{4.23}$$

For calculating the average of the source current $\bar{\imath}_g$, $\underline{v_{gAB}}$ is substituted by (4.23):

$$\frac{1}{T_s(t)}\int_{-T_s(t)}^{0} i_r(\tau)\frac{\underline{v_{gAB}(\tau)}}{V_g}\,d\tau = \frac{1}{T_s(t)}\int_{-T_s(t)}^{0} i_r(\tau)\frac{4}{\pi}\sin(\omega_s(t)\tau)\,d\tau = \cdots = \frac{2}{\pi}i_{r,s}(t)\,. \quad (4.24)$$

The absolute function $\underline{|i_r - i_p|}$ has no fundamental component ω_s but the DC component

$$\underline{|i_r - i_p|}_{DC} = \frac{2}{\pi}\underline{|i_r - i_p|}_{peak} \quad (4.25)$$

Considering the harmonic approximation of $i_r(t)$ and $i_p(t)$ by

$$i_r(t) - i_p(t) = (i_{r,s} - i_{p,s})\sin(\Phi(t)) + (i_{r,c} - i_{p,c})\cos(\Phi(t))\,, \quad (4.26)$$

(4.25) becomes

$$\underline{|i_r - i_p|}_{DC} = \frac{2}{\pi}\sqrt{(i_{r,s} - i_{p,s})^2 + (i_{r,c} - i_{p,c})^2} \quad (4.27)$$

The signum function $\underline{sgn(i_r - i_p)}$ is a unity square wave with the phase given by the argument (4.26) . Its fundamental component therefore is

$$\underline{sgn(i_r - i_p)}(t)_{<1>} = \frac{4}{\pi}\frac{(i_{r,s} - i_{p,s})\sin(\Phi(t)) + (i_{r,c} - i_{p,c})\cos(\Phi(t))}{\sqrt{(i_{r,s} - i_{p,s})^2 + (i_{r,c} - i_{p,c})^2}}. \quad (4.28)$$

With the substitution of (4.20) to (4.28) into (4.11) and (4.12) the large signal EDF-1 model of the LLC converter is complete. By setting $\dot{x}_{hcv} \equiv 0$ the model can be analytically solved for $M = v_o/V_g$. By numerical comparison the EDF-1 steady-state solution yields exactly the same result as the FHA solution (3.40). But with the EDF-1 model additionally the influence of R_s, R_d and R_c can be considered as shown in Fig. 4.3 for $R_s = d \cdot Z_0$.

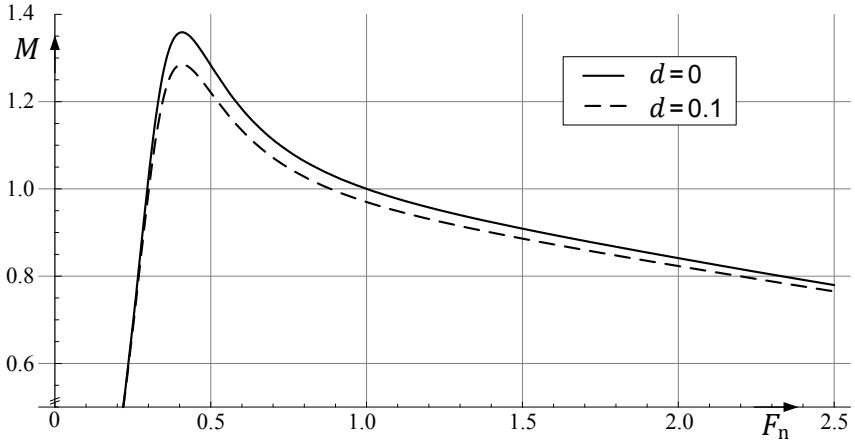

Fig. 4.3: Steady-state DC-DC gain calculated by the EDF-1 model; h = 8, Q = 0.251, $R_d = R_c = 0$

In order to extract the small-signal characteristic the EDF-1 large-signal model needs to be linearized at a certain operating point. Therefore all time-variable values have to be substitut-

ed by its small-signal representation $\bar{x} + \Delta x$, in which $\bar{x}$ represents the steady-state solution and Δx the small-signal excitation at excitation frequency f_{ss} [Erickson]. The linearization procedure is an approximate method because its neglects the influence of non-linear terms which are given by a mutual multiplication between small-signal excitations, i.e.

$$\Delta x^2 \approx 0 \quad \text{and} \quad \Delta x \Delta y \approx 0\,. \tag{4.29}$$

The intention of (4.29) is that whenever the small-signal excitations are small enough, the linear terms have much higher gain such that $k_1 \Delta x \gg k_2 \Delta x^2$ ($k_{<x>}$: respective factor within a factorized form of the large signal model). The validity of this assumption also depends on the dimensional relationship between the factors $k_{<x>}$. It is required that $k_2 \gg k_1$ is not true. Since neglecting non-linear terms is a quite convenient method to build a small-signal model, the condition $k_2 \gg k_1$ is typically not analyzed in detail for a given problem, but instead the small-signal model of a given problem is verified by a comparison to measurements. This approach is also adapted in this work and the resulting small-signal model is compared to measurement results. However, neglecting non-linear terms is furthermore supported by the fact that for a given excitation frequency f_{ss} the non-linear terms yield frequencies that are different to the excitation frequency due to modulation effects. As a consequence the transfer behavior, which essentially is the frequency response at the excitation frequency f_{ss}, is only indirectly influenced by the non-linear terms, which can be interpreted as a further increase of the validity of the assumption (4.29).

The large-signal EDF-1 model of the LLC converter comprises non-linear relations: In (4.27) the term $\sqrt{\left(i_{r,s} - i_{p,s}\right)^2 + \left(i_{r,c} - i_{p,c}\right)^2}$ occurs in the numerator and in (4.28) in the denominator. The linearization is a two-step procedure. Firstly the perturbation and application of (4.29) yields

$$\sqrt{\left(i_{r,s} - i_{p,s}\right)^2 + \left(i_{r,c} - i_{p,c}\right)^2} \approx \bar{i}_{rp}\sqrt{(1 + \Delta i_{rp})} \tag{4.30}$$

with

$$\bar{i}_{rp} = \sqrt{\bar{i}_{r,s} + \bar{i}_{r,c} + \bar{i}_{p,s} + \bar{i}_{p,c} - 2\,\bar{i}_{r,s}\bar{i}_{p,s} - 2\,\bar{i}_{r,c}\bar{i}_{p,c}}$$

and

$$\Delta i_{rp} = \frac{1}{\bar{i}_{rp}^2}\big(2\,\bar{i}_{r,c}\Delta i_{r,c} - 2\,\bar{i}_{p,c}\Delta i_{r,c} - 2\,\bar{i}_{r,c}\Delta i_{p,c} + 2\,\bar{i}_{p,c}\Delta i_{p,c} + 2\,\bar{i}_{p,s}\Delta i_{p,s} - 2\,\bar{i}_{r,s}\Delta i_{p,s} - 2\,\bar{i}_{p,s}\Delta i_{r,s} + 2\,\bar{i}_{r,s}\Delta i_{r,s}\big).$$

Secondly (4.29) is applied to the binomial series expansion of (4.30) according to

$$(1 \pm \Delta x)^m = 1 \pm m\Delta x + \frac{m(m-1)}{2!}\Delta x \pm \cdots \approx 1 \pm m\Delta x\,, \tag{4.31}$$

which yields

$$\bar{i}_{rp}\sqrt{(1 + \Delta i_{rp})} \approx \bar{i}_{rp}\left(1 + \frac{1}{2}\Delta i_{rp}\right) \text{ resp. } \frac{1}{\bar{i}_{rp}\sqrt{\left(1 + \Delta i_{rp}\right)}} \approx \frac{1}{\bar{i}_{rp}}\left(1 - \frac{1}{2}\Delta i_{rp}\right). \tag{4.32}$$

Considering that per definition $0 = \boldsymbol{A}\overline{\boldsymbol{x}}_{\mathrm{hcv}} + \boldsymbol{B}\overline{\boldsymbol{u}}$ is true, the linearization procedure results in the small-signal system model

$$\begin{aligned} \Delta\dot{\boldsymbol{x}}_{\mathrm{hcv}} &= \boldsymbol{A}\Delta\boldsymbol{x}_{\mathrm{hcv}} + \boldsymbol{B}\Delta\boldsymbol{u} \\ \Delta\boldsymbol{y} &= \boldsymbol{C}\Delta\boldsymbol{x}_{\mathrm{hcv}} + \boldsymbol{D}\Delta\boldsymbol{u} \end{aligned} \tag{4.33}$$

The small-signal transfer functions of (4.33) are given according to e.g. [Föllinger] by

$$\boldsymbol{G}(s) = \boldsymbol{C}(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B} + \boldsymbol{D} \tag{4.34}$$

such that

$$\begin{pmatrix} \Delta v_{\mathrm{o}} \\ \Delta i_{\mathrm{gAV}} \end{pmatrix} = \boldsymbol{G}(s) \begin{pmatrix} \Delta V_{\mathrm{g}} \\ \Delta\omega_{\mathrm{s}} \\ \Delta i_{\mathrm{o}} \end{pmatrix}. \tag{4.35}$$

4.2.2 Evaluation of the Small-Signal Model

The EDF-1 small-signal model (4.35) offers two possible use cases. Firstly it can be used for analytical studies on the dynamic behavior of the LLC converter in dependence on interesting parameters. Secondly it has to be evaluated if the accuracy of the model is sufficient for being utilized in the compensator design. In order to answer the latter question the EDF-1 model is compared to measurement results. The measurements are conducted on a LLC converter prototype exhibiting the parameters given in Table 4.1. The values for the parasitic resistances R_{s}, R_{d} and R_{c} (c.f. Fig. 4.2) are estimated. It is therefore assumed that these values have no significant effect on the small-signal characteristic. Further model approximations that are possibly relevant are the negligence of the core losses of the magnetic components and the parasitic junction capacitances of the semiconductor switches. The prototype exhibits a synchronous rectification.

Table 4.1: Parameters of the LLC converter prototype used for the frequency response measurement

L_{s}	36.4 µH
C_{s}	58 nF
L_{p}	188 µH
R_{s}	0.3 Ω
R_{d}	12 mΩ
R_{c}	2.5 mΩ

C_{o}	4.42 mF
n	7.28
$V_{\mathrm{i,nom}}$	400 V
$I_{\mathrm{o,nom}}$	50 A
$V_{\mathrm{o,nom}}$	54 V
f_0	110 kHz

Fig. 4.4 shows the principal measurement setup. The LLC converter prototype is controlled digitally by a DSP and has a readily programmed SISO control loop with v_{o}: controlled variable and f_{s}: manipulated variable. The control loop comprises the sampling of the output voltage v_{o}, the calculation of the T_{s} value by the compensator algorithm and the modulator unit, which generates the switching commands for the LLC converter power circuit according $f_{\mathrm{s}} = 1 / T_{\mathrm{s}}$. In order to measure the frequency response the control loop is opened by inserting a frequency response analyzer (FRA). At the same time within the DSP the sampled voltage v_{ctrl} is bypassed directly to the signal output by calculating $T_{\mathrm{s}} = 1/\left(K_{\mathrm{g1}} v_{\mathrm{ctrl}}\right)$ with known factor K_{g1}. The measured frequency response in consequence is described by

$$G_{v_A - v_B}(f_{ss}) = \left.\frac{\hat{v}_B}{\hat{v}_A}\right|_{f_{ss}} = \frac{\hat{T}_s}{\hat{v}_{ctrl}} \cdot \frac{\hat{f}_s}{\hat{T}_s} \cdot \frac{\hat{v}_o}{\hat{f}_s} = \frac{\hat{T}_s}{\hat{v}_{ctrl}} \cdot \frac{\hat{f}_s}{\hat{T}_s} G_{f_s - v_o}(f_{ss}) \tag{4.36}$$

with $G_{f_s - v_o}(f_{ss}) = 2\pi\, G_{\omega_s - v_o}(f_{ss})$ and $\hat{x}/\hat{y} \equiv \Delta x/\Delta y$: small-signal transfer behavior.

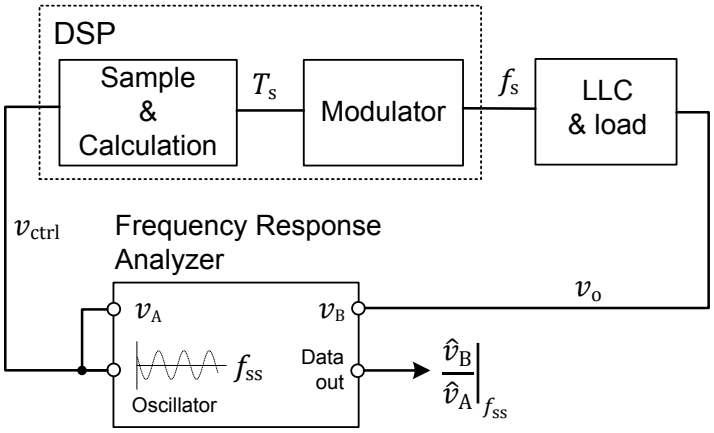

Fig. 4.4: Principle measurement setup for measuring the control to output frequency response of a LLC converter with partwise digital signal processing (DSP)

The comparison between the measured frequency response $G_{v_A - v_B}(f_{ss})$ and the calculated one $G_{f_s - v_o}(f_{ss}) = \hat{v}_o/\hat{f}_s$ has the limitation, that the control loop signal is partwise processed digitally by the DSP. This comprises the sampling of v_{ctrl} with sampling rate T_{sp} = 10 µs, the calculation of T_s with calculation delay $T_{clc} = 0.6\, T_{sp}$ and the output of the switching command waveform with frequency f_s. These signal processing steps generate additional amplitude and phase components, which need to be considered for the comparison. However, in case the compensator is designed based on the measured transfer characteristic, the effects are automatically considered since they are included in the measured plant characteristic.

The effects caused by the partwise digital signal processing are treated as follows:
The digital sampling of the analog signal v_{ctrl} generates a train of impulses with the Laplace-Transform

$$V^*_{ctrl}(s) = \sum_{k=0}^{\infty} v_{ctrl}(kT_{sp})\, e^{-kT_{sp}} \tag{4.37}$$

The frequency spectrum of (4.37) and the one of the original signal have the relationship

$$V^*_{ctrl}(s) = \frac{1}{T_{sp}} \sum_{n=-\infty}^{n=+\infty} V_{ctrl}(s - jn\frac{2\pi}{T_{sp}}) \tag{4.38}$$

The signal (4.37) is further processed with calculation delay T_{clc} and supplied to the Modulator. The provision of T_s to the Modulator has the characteristic of a zero-order hold (ZOH) block. The transfer function of a ZOH, e.g. [Lutz], is given by

$$G_{ZOH}(s) = (1 - e^{-sT_{sp}})/s \tag{4.39}$$

The transfer characteristic $\hat{T}_s/\hat{v}_{ctrl}$ therefore is described by

$$T_{\mathrm{Ts}}(s) = \left[\sum_{n=-\infty}^{n=+\infty} V_{\mathrm{ctrl}}\left(s - jn\frac{2\pi}{T_{\mathrm{sp}}}\right)\frac{K_{\mathrm{g1}}}{T_{\mathrm{sp}}}\frac{1 - e^{-sT_{\mathrm{sp}}}}{s}\, e^{-sT_{\mathrm{clc}}}\right]^{-1}. \tag{4.40}$$

Because the FRA uses a strong band-pass filter when measuring the frequency response, (4.40) can be reduced to

$$T'_{\mathrm{Ts}}(s) = \left[V_{\mathrm{ctrl}}(s)\frac{K_{\mathrm{g1}}}{T_{\mathrm{sp}}}\frac{1 - e^{-sT_{\mathrm{sp}}}}{s}\, e^{-sT_{\mathrm{clc}}}\right]^{-1}. \tag{4.41}$$

Hereby it is assumed that the side-band frequency components do not influence the measured frequency component, which is true for a LTI system and for the LLC converter if the small-signal excitation amplitude is infinite small.

The transfer characteristic $\hat{f}_{\mathrm{s}}/\hat{T}_{\mathrm{s}}$ describes essentially the frequency behavior of the Modulator. This depends on the exact realization of the modulator. In the treated case the dead time depends e.g. on the continuously moving phase relationship between $T_{\mathrm{s}}(kT)$ and the modulator state, since in general $T_{\mathrm{s}} \neq T_{\mathrm{sp}}$. This dead time has to be modeled by statistical means. However, the modeling of $\hat{f}_{\mathrm{s}}/\hat{T}_{\mathrm{s}}$ is not performed in this work. The comparison between measured and calculated frequency response therefore naturally exhibits a phase error in the upper frequency range. Unless other possible unknown influences this error is rooted in the modulator characteristic. In case the measured transfer characteristic (4.36) is used for the compensator design, all sampling and modulator related amplitude and phase components are automatically considered. In case the compensator design is based on the EDF-1 small-signal model the transfer characteristic $\hat{f}_{\mathrm{s}}/\hat{T}_{\mathrm{s}}$ needs to be appropriately modeled if the desired control loop bandwidth is higher than the switching frequency divided by a certain factor. This factor is extracted from the measurement results in the following.

Fig. 4.5 shows a comparison between the measured and calculated small-signal transfer characteristic at depicted switching frequencies F_{n} . The visualized functions are given by

$$G_{f_{\mathrm{s}}-v_{\mathrm{o}}}(f_{\mathrm{ss}}) = 2\pi \boldsymbol{G}(s)_{1,2}\big|_{s=j2\pi f_{\mathrm{ss}}}$$

and

$$G'_{f_{\mathrm{s}}-v_{\mathrm{o}}}(f_{\mathrm{ss}}) = G_{v_{\mathrm{A}}-v_{\mathrm{B}}}(f_{\mathrm{ss}})\left(\frac{K_{\mathrm{g1}}}{T_{\mathrm{sp}}}\frac{1 - e^{-sT_{\mathrm{sp}}}}{s}\, e^{-sT_{\mathrm{clc}}}\right)^{-1}\Bigg|_{s=j2\pi f_{\mathrm{ss}}}.$$

Hereby the measured transfer characteristic is plotted in a corrected version $G'_{f_{\mathrm{s}}-v_{\mathrm{o}}}(f_{\mathrm{ss}})$ to account for the s/h behavior and calculation delays according to (4.40). The comparison yields the following observations:

- In all cases an increasing phase error at high excitation frequencies f_{ss} can be observed. As already stated this error can be interpreted as the phase delay introduced by the modulator and its specific realization. Moreover the starting point of increasing phase error depends on the switching frequency F_{n}. At $F_{\mathrm{n}} = 0.84$ a major deviation can be stated for $f_{\mathrm{ss}} \gtrsim 2$ kHz, at $F_{\mathrm{n}} = 1$ for $f_{\mathrm{ss}} \gtrsim 3$ kHz, at $F_{\mathrm{n}} = 1.2$ and $F_{\mathrm{n}} = 1.8$ for $f_{\mathrm{ss}} \gtrsim 3.5$ kHz. This coincides with the fact that the modulator delay is reduced with increasing switching frequency f_{s}.

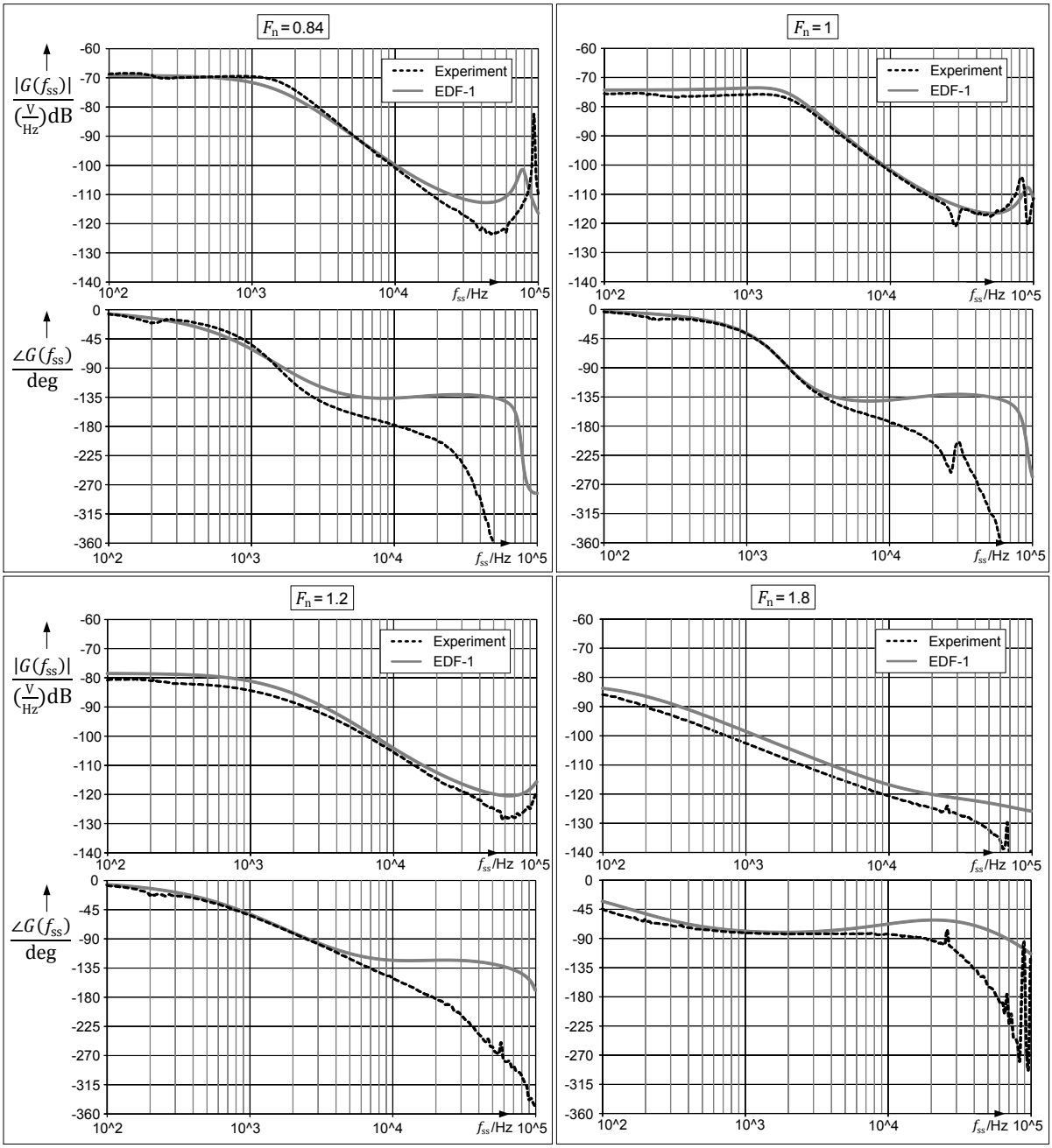

Fig. 4.5: Comparison between calculated control to output transfer characteristic $G_{f_s - v_o}(f_{ss})$ *and corrected measured transfer characteristic* $G'_{f_s - v_o}(f_{ss})$ *of the LLC converter at* $V_i = 400\ V$ *and* $I_o = 25\ A$.

- At $F_n = 0.84$ the double pole at $f_{ss} \approx 1.5$ kHz of the transfer behavior is less damped in the measured results. This is supposed to be an implication of the DCMB2 mode regarding the negligence of the discontinuous output current in the EDF-1 model. However, an answer with exact physical background to this question is not given here.
- For the treated set-up the phase is accurately predicted by the EDF-1 model if $f_{ss} \leq 50\ f_s$ at $F_n \geq 1$. At $F_n \leq 1$ the phase is predicted higher for the f_{ss} area below the double pole frequency.

- With regard to a compensator design utilizing the EDF-1 model, a major source of error is given by deviations of the plant gain. Esp. at $F_n = 1.8$ the gain error is up to 6 dB, which is not feasible for a reliable compensator design. It can be stated that the EDF-1 model supports dynamic analysis and initial compensator design, but that a final compensator design should be verified and optimized by transfer characteristic measurements of the real converter. This is at least true for the converter set-up used here for performing the measurements.
- At $f_{ss} \approx 200$ Hz small disturbances to a smooth frequency curve can be examined in most cases. It is assumed that these are not part of the control to output transfer characteristic since unfortunately the Power Supply feeding the input voltage of the LLC converter during the measurements produced a ripple voltage in the respective frequency range.

4.2.3 Aspects on the Compensator Design

The SISO control loop approach for controlling the output voltage of the LLC converter requires the design of a compensator in dependence on the plant characteristic $G_{f_s - v_o}(f_{ss})$. As shown by Fig. 4.5 the plant characteristic varies distinctively with the switching frequency f_s. Especially IT PSUs comprising battery back-up path 2 (c.f. Chapter 2.1.1) need to serve high DC-DC gain ranges and therefore also high switching frequency ranges. The switching frequency range investigated in Fig. 4.5 is at least utilized in a typical IT PSU with back-up path 2. In consequence the compensator needs to be stable and optimized for every plant characteristic that occurs in the utilized switching frequency range. Taking the plant characteristics of Fig. 4.5 as an example, the plant gain $\left| G_{f_s - v_o}(f_{ss}) \right| / (\mathrm{V/Hz})$ at $f_{ss} = 1$ kHz varies between -69.5 dB at $F_n = 0.84$ and -103 dB at $F_n = 1.8$, which gives a variation of 33.3 dB. This variation is caused on the one hand by different steady-state gains and on the other hand by different pole characteristics. The double pole occurring in the below resonance frequency range splits into two separate poles in the above resonance region, and the two poles separating more and more the higher the switching frequency is [Yang3]. The phase characteristic varies accordingly. Assuming $f_{ss} \approx 1$ kHz as a feasible cross-over frequency for a potential PID compensator design, the compensator needs to be adapted to the switching frequency if an overall optimized control loop behavior with mentioned cross-over frequency is desired. A possible adaptive compensator approach is illustrated in Fig. 4.6. Within this approach an additional feedback loop according to $f_s = F(v_{err}, f_s)$ is established, that generally has to be analyzed for stability issues. However, this analysis is not conducted in this work; instead an experimentally achieved indication on the stability of the adaptive compensator approach is presented. Therefore an adaptive PID compensator according to Fig. 4.6 was realized such that the control loop cross over frequency F_c , the phase margin φ_m and the amplitude margin A_m are in the range

$$(1\ \mathrm{kHz} < F_c < 2\ \mathrm{kHz})\ \&\ (\varphi_m > 45)\ \&\ (A_m > 12\ dB)\big|_{(I_o = 25\ \mathrm{A})\ \&\ (0.84 < F_n < 1.8)}. \quad (4.42)$$

With the realized adaptive PID compensator no instabilities are observed in the experimental evaluation and the exemplary step-load performance shown in Fig. 4.7 is achieved. The 55% load step causes less than 600 mV peak-to-peak or 1.1% V_o peak-to-peak output voltage disturbance. It must be pointed out that no general stability assumption of the adaptive compensator approach can be derived from the experimental evaluation.

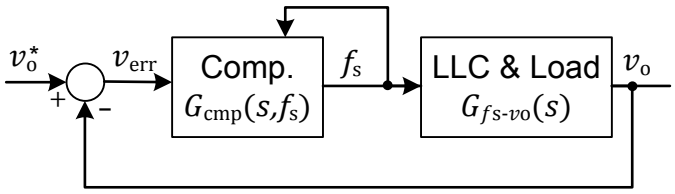

Fig. 4.6: Principal structure of an adaptive compensator control loop for the LLC converter

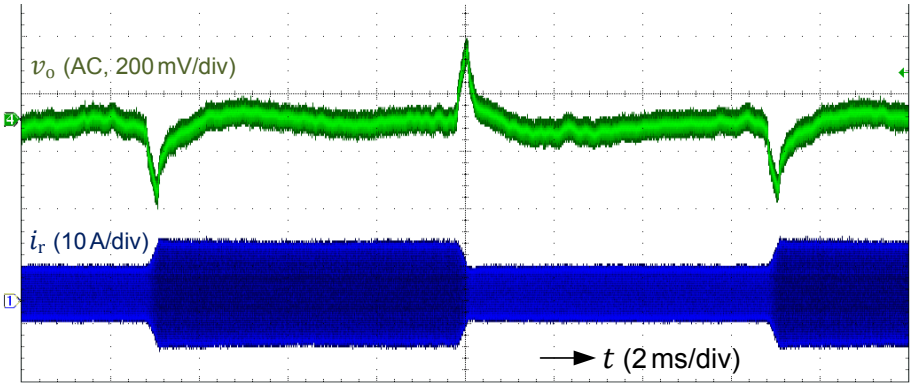

Fig. 4.7: Step load performance of the adaptive PID compensator approach (4.42) at V_i = 400 V, V_o = 54.5 V, I_o = 14 A (30% $I_{o,nom}$) and 39 A (85% $I_{o,nom}$); Ch 1 (10 A/div): resonant current i_r (due to the time scaling only the envelope can be seen) , Ch 4 (200 mV/div): AC part of output voltage v_o.

A further aspect on the compensator design is given by the load dependence of the plant characteristic. In order to analyze this aspect Fig. 4.8 depicts the measured control to output transfer characteristics $G_{v_A-v_B}(f_{ss})/K_{g1}$ at different output loadings and at different switching frequencies. The comparison allows the following deductions:

- At $F_n = 0.84$ the plant characteristic changes only slightly in dependence on the output loading. The gain decreases slightly with increasing loading and the phase deviates only at higher excitation frequencies $f_{ss} > 5$ kHz. The gain change coincides qualitatively with the steady-state DC-DC gain characteristic considering $(\partial/\partial F_n)\, M(F_n)$ (c.f. Fig. 4.1). It is feasible to design a robust compensator applicable to the complete given load range at $F_n \approx 0.84$.
- At $F_n = 1$ the gain and phase are slightly changing in the upper load range, i.e. $I_o = 25$ A to 50 A. This range can be served by one robust compensator design. In the lower load range the plant characteristic changes distinctively in the way that the double pole at $f_{ss} \approx 2$ kHz splits into two single poles. In consequence the compensator design needs to be evaluated at high and low output loadings at $F_n \approx 1$.
- At $F_n = 1.2$ and $F_n = 1.8$ the behavior of the pole movement is contrary to the case at $F_n = 1$: At low output loading a double pole characteristic can qualitatively be stated, at which the poles split into two single poles for the upper load range. Within the upper load range the gain change is very distinctive, which again coincides with the steady-state DC-DC gain characteristic considering $(\partial/\partial F_n)\, M(F_n)$ (c.f. Fig. 4.1). Due to this characteristic a robust compensator must be designed for the highest possible output loading, where the compensator performance will not be optimized at lower output loadings. Alternatively the compensator can be adapted to the output loading, but this implies proofing of the stability of the adaptive approach.

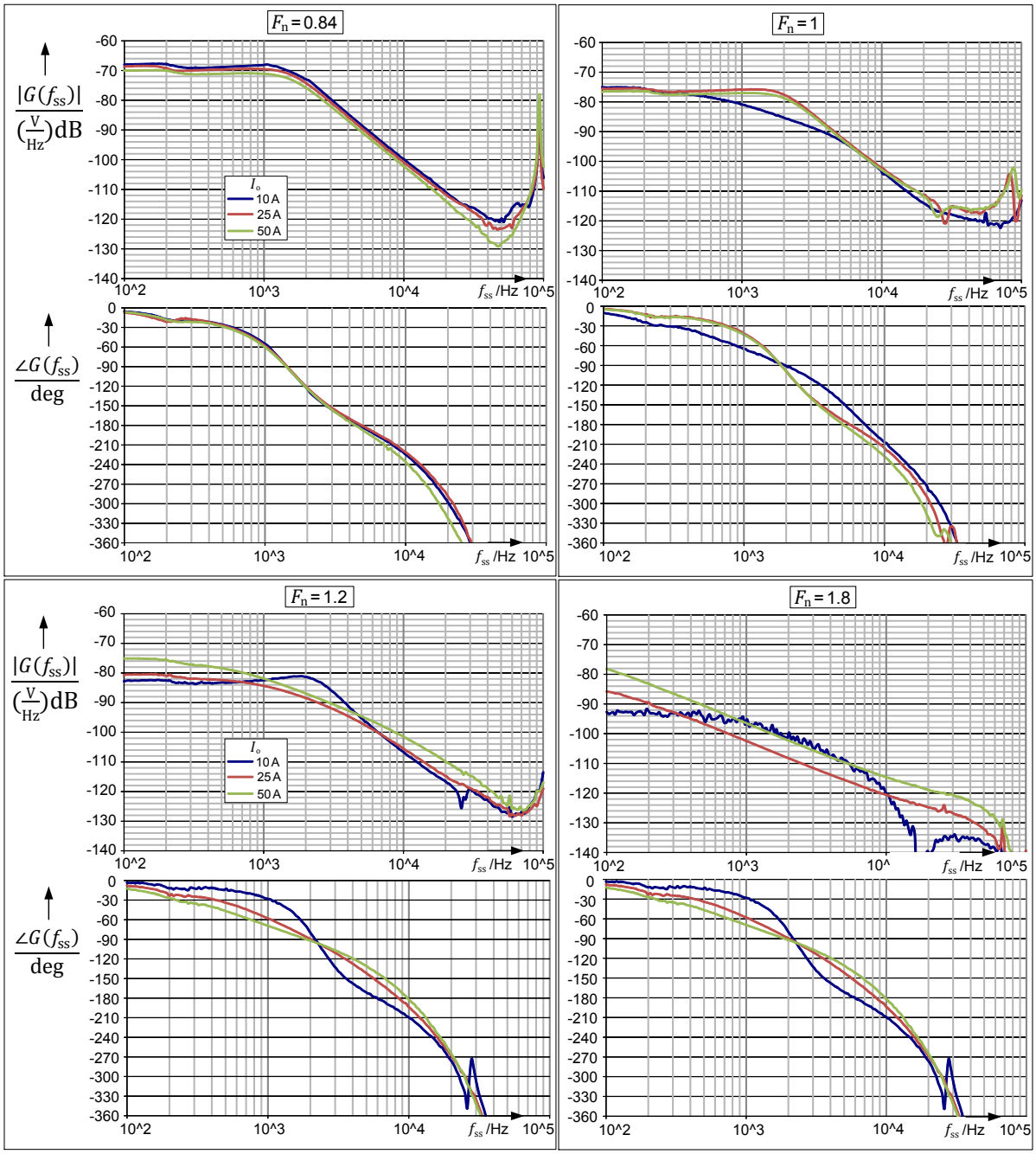

Fig. 4.8: Comparison between control to output transfer characteristics $G_{v_A - v_B}(f_{ss})/K_{g1}$ at different output loadings I_o and at V_i = 400 V.

An important aspect on the SISO control approach for the LLC converter is the Audio Susceptibility, which is given by

$$G_{v_g - v_o}(f_{ss}) = \boldsymbol{G}(s)_{1,1}\big|_{s=j2\pi f_{ss}} .$$

Practical experience shows that the DC-link voltage ripple v_{g_ripp} of a PSU, which results from the pulsating power input of the PFC stage according to $p_{PFC}(t) \sim (v_{grid}(t))^2$, is not reasonable damped by a SISO control approach regulating the output voltage v_o. The theoretical background of this phenomenon can be qualitatively analyzed by means of the EDF-1 small-

signal model. Fig. 4.9 shows a comparison between $G_{v_g-v_o}(f_{ss})$ and $G_{f_s-v_o}(f_{ss})$ based on the EDF-1 model. The Audio Susceptibility problem arises as follows: Due to the strong phase decline in $G_{f_s-v_o}(f_{ss})$ starting at $f_{ss} \approx 1$ kHz (c.f. also Fig. 4.5 for the measured values), the compensator design is challenging if a control loop bandwidth for v_o much higher than 1 kHz is desired. This is also supported by the limited compensator calculation speed in case digital control is employed[9].Based on this it can be stated that the gain characteristics of $G_{v_g-v_o}(f_{ss})$ and $G_{f_s-v_o}(f_{ss})$ are similar up to the potential control loop bandwidth. In consequence the DC-link voltage ripple, which has a frequency of 100 Hz in a 50 Hz public grid, is damped only by the open loop gain of the v_o control loop at $f_{ss} = 100$ Hz. Since the control loop gain is limited by the stability boundary, also the damping of the DC-link voltage ripple is limited.

As an example the compensator implementation of (4.42) has an open loop gain of $G_{op\_lp}(100\text{ Hz})\big|_{F_n=1} = 22.8$ dB. Considering the DC-link voltage ripple as a disturbance on v_o, the damping of the ripple is given by the disturbance transfer characteristic [Föllinger]

$$G_z(f_{ss}) = \frac{1}{1 + G_{op\_lp}(f_{ss})}. \tag{4.43}$$

As such the disturbance v_{o_ripp} superimposed on v_o is given by

$$v_{o\_ripp}(s) = G_z(f_{ss})\, G_{v_g-v_o}(f_{ss}) V_{g\_ripp}(s). \tag{4.44}$$

The gain of (4.44) for the given example is calculated to

$$\left| G_z(f_{ss})\, G_{v_g-v_o}(f_{ss}) \right|_{f_{ss} = 100\text{ Hz}} \approx 9.46 \cdot 10^{-3},$$

hence a DC-link voltage ripple of e.g. 30 V peak-to-peak would result in 284 mV peak-to-peak voltage ripple superimposed on v_o. Because this 100 Hz voltage ripple might be out of the customer requirements, a workaround successfully used in the industry is the feed-forward of the DC-link voltage ripple into the control loop, but in case of a galvanically isolated DC-DC converter with the drawback of additional communication measures crossing the isolation barrier. Control method solutions to the Audio Susceptibility problem avoiding such additional hardware effort have not yet successfully evolved in literature and industry.

[9] In case of digital control the poles and zeroes of the compensator are limited to the two-fold value of the sampling period in order to avoid aliasing. The used LLC converter prototype uses the TMS28027 DSP and a sampling rate of $T_{sp} = 10$ µs.

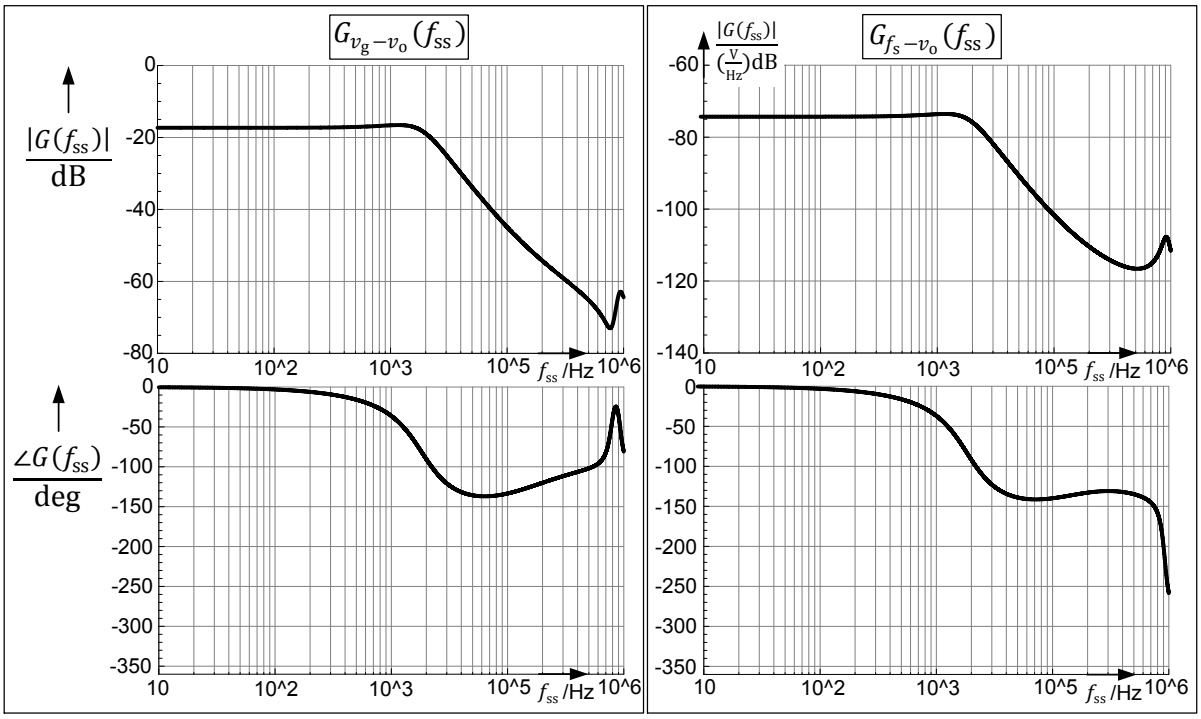

Fig. 4.9: Comparison between the transfer characteristics $G_{v_g-v_o}(f_{ss})$ (Audio Susceptibility) and $G_{f_s-v_o}(f_{ss})$ at F_n = 1, V_i = 400 V and I_o = 25 A and based on the EDF-1 model.

4.3 Overload Protection and Control

In general the highest aim of an overload protection of DC-DC converters is to omit non-reversible damage of components of the converter by excessive currents or voltages appearing at the components. Without detailed analysis it is stated that for DC-DC converters this aim can be reached by limiting the output current and the output power of the converter. With respect to a reliable converter design and operation the following strategy for overload protection and control is a straight-forward approach:

1. The converter comprises a shut-down mechanism in dependence on measured quantities and appropriate shut-down thresholds. This ensures that components cannot be destroyed by unforeseen load or converter control incidents.
2. The shut-down of the converter may not be the deserved output characteristic of the converter in case of overloads. Instead a controlled limitation of output power and current is of interest to ensure a maximal up-time and supply of the connected loads. Such limitations can be realized by additional control measures or feedback control loops.

The implementation of the described protection strategy results in different methodologies for PWM-type and resonant converters. Besides the often referred beneficial characteristics of the LLC resonant converter compared to PWM-type converters regarding efficiency and EMI, the described overload protection strategy is more complex to achieve. This circumstance results from the fact, that PWM-type converters can be cycle-by-cycle current limited by well proven peak-current control measures. But peak-current control is typically not applicable in general to resonant converters and in more specific to the LLC resonant converter since those are con-

trolled by switching frequency and not by duty cycle control. Despite duty cycle control is proposed by some authors for the LLC converter ([Raju], [McDonald]), it has the disadvantages of a non-linear control law and typically the loss of ZVS operation. Since the loss of ZVS is not acceptable for high efficient PSUs, the overload and short-circuit protection of the LLC resonant converter by control means would have at least the implication of a mix of different control laws and methods. Furthermore it would require a very fast signal processing and a sophisticated implementation if a defined over current characteristic should be achieved (c.f. also [Yang4]). Due to the noted reasons a popular method proposed in literature is the resonant capacitor diode clamp approach that adds short-circuit and overload robustness to the LLC converter inherently (e.g. [Yang3], [Yang4], [Zhao]). This method could be beneficially combined with the control approach presented in Fig. 4.10 and employing the above mentioned protection strategy. Here the output current control loop is the outer loop of a cascaded SISO structure and hence can serve as a long-term output current limitation but not as a protection for fast transient overloads. It is therefore feasible to have an inherent short-circuit robustness of the LLC converter such that the converter can survive transient overloads and the control structure and output characteristic shown in Fig. 4.10 can be employed.

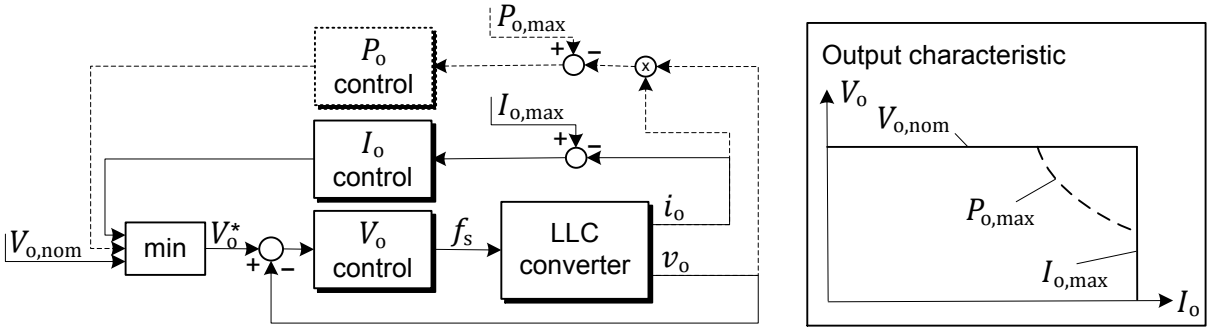

Fig. 4.10: Cascaded control structure for the LLC resonant converter employing outer output current and output power limiting control loops

The clamping diodes approach proposed in [Yang3] can serve as an inherent overload protection of the converter. The principal of this method is to clamp the resonant capacitor voltage v_{Cs} to the input voltage V_i in overload operation. The clamping action leads to a circulation of energy between the resonant circuit and the input power source, whereby the energy transfer to the output is reduced. In case of a full-bridge configuration of the converter's inverter stage, a bridge rectifier can be used to clamp the bipolar resonant capacitor voltage to the input voltage. In case of a half-bridge configuration, the split capacitor configuration of the resonant capacitor C_s must be used, whereby the clamping diodes D_1 and D_2 can be added in parallel to the resonant capacitors $C_s/2$ (c.f. Fig. 4.11).

The clamping diodes approach on the one hand limits the voltage appearing at the resonant capacitor to a maximum given by the actual input voltage. On the other hand the overall short-circuit current is limited, too. But especially for front-end power supplies one major disadvantage arises: During a line drop the DC-link capacitor is discharged to hold-up the output voltage and consequently the DC-link voltage, which is the input voltage V_i to the DC-DC converter, decreases. This leads to a decreasing switching frequency and therefore to an increasing resonant capacitor voltage and potentially to an unintended clamping of the resonant capacitor voltage. The unintended clamping alters the DC-DC gain characteristic of the LLC

converter and causes reduced output power and hold-up time. These implications of the clamping diodes approach will be analyzed in the following.

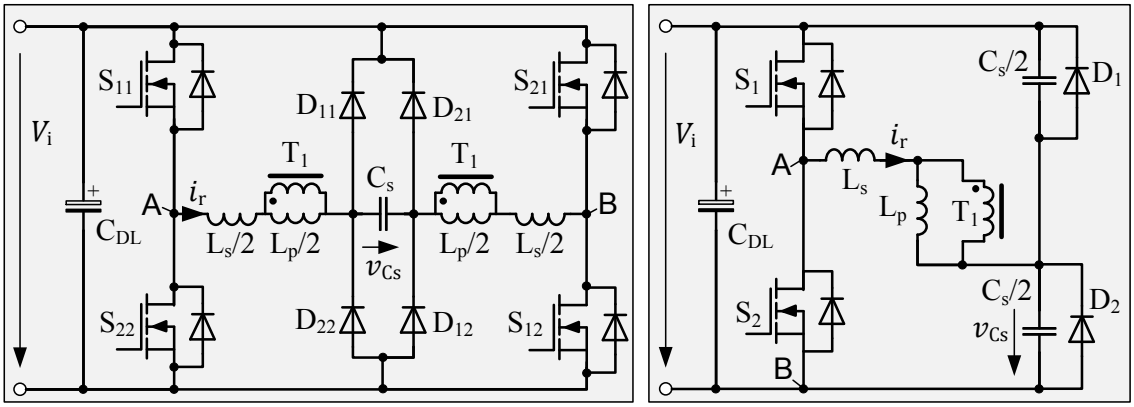

Fig. 4.11:LLC converter primary sides employing resonant capacitor clamping for inherent overload protection; Left: Full-bridge, Right: Half-bridge

4.3.1 Implications of the Resonant Capacitor Clamping Approach

The implications of the resonant capacitor clamping approach on the converter design and operation can be qualitatively analyzed by means of a FHA, respecting that the accuracy of the FHA approach is not sufficient to perform a detailed circuit design. By employing the FHA the resonant capacitor voltage v_{Cs} normalized to the exciting bridge voltage v_{gAB} and denoted as V_{nCs} is expressed by

$$V_{\mathrm{nCs}}(h, Q_{\mathrm{ac}}, F_{\mathrm{n}}) = \frac{V_{\mathrm{Cs\langle 1\rangle}}}{V_{\mathrm{gAB\langle 1\rangle}}} = \frac{1 + \frac{1}{F_{\mathrm{n}}}\frac{1}{hQ_{\mathrm{ac}}}}{1 + \frac{1}{F_{\mathrm{n}}}\frac{1}{hQ_{\mathrm{ac}}} + \frac{F_{\mathrm{n}}}{Q_{\mathrm{ac}}}\left(1 + \frac{1}{h}\right) + F_{\mathrm{n}}^2}, \tag{4.45}$$

where $V_{\mathrm{Cs<1>}}$ and $V_{\mathrm{gAB<1>}}$ are the fundamental components of the corresponding waveforms. The clamping diodes (e.g. D_1, D_2 in case of a half-bridge, c.f. Fig. 4.11) become forward biased if $v_{\mathrm{Cs}} > V_{\mathrm{i}}$. By FHA means this threshold is expressed by $V_{\mathrm{nCs}} > \pi/4$. Fig. 4.12 visualizes (4.45) and the clamping threshold. It can be observed that in general the clamping threshold $v_{\mathrm{Cs}} = V_{\mathrm{i}}$ is reached within the ZVS operating area $\varphi > 0$ of the LLC converter. This entails that the preferred operating region of the LLC converter is diminished by the presence of the clamping diodes. Unfortunately the operating region that is affected by the clamping diodes is demanded in case of front-end power supplies with hold-up requirements. The ability of the DC-DC converter of a front-end power supply to hold-up the output power in case of a line drop-out and therefore shrinking DC-link voltage has a direct influence on the performance parameters cost and power density: the higher the maximal DC-DC gain capability of the DC-DC converter the less DC-link capacitance needs to be installed in order to meet a certain hold-up time requirement (typical values: 10 to 20 ms) because the hold-up energy is given by $E_{\mathrm{hold\_up}} = 1/2\ C_{\mathrm{DL}}\left(V_{\mathrm{i,nom}} - V_{\mathrm{i,min}}\right)^2$.

Furthermore Fig. 4.12 shows that the hold-up performance of the LLC converter employing the clamping approach can be optimized by minimizing the characteristic impedance Z_0 which is proportional to Q. But the minimization of Z_0 at the same time reduces the inherent

short-circuit current limitation of the clamping approach (c.f. (5.5)) and increases the switching frequency range (c.f. Fig. 5.7).

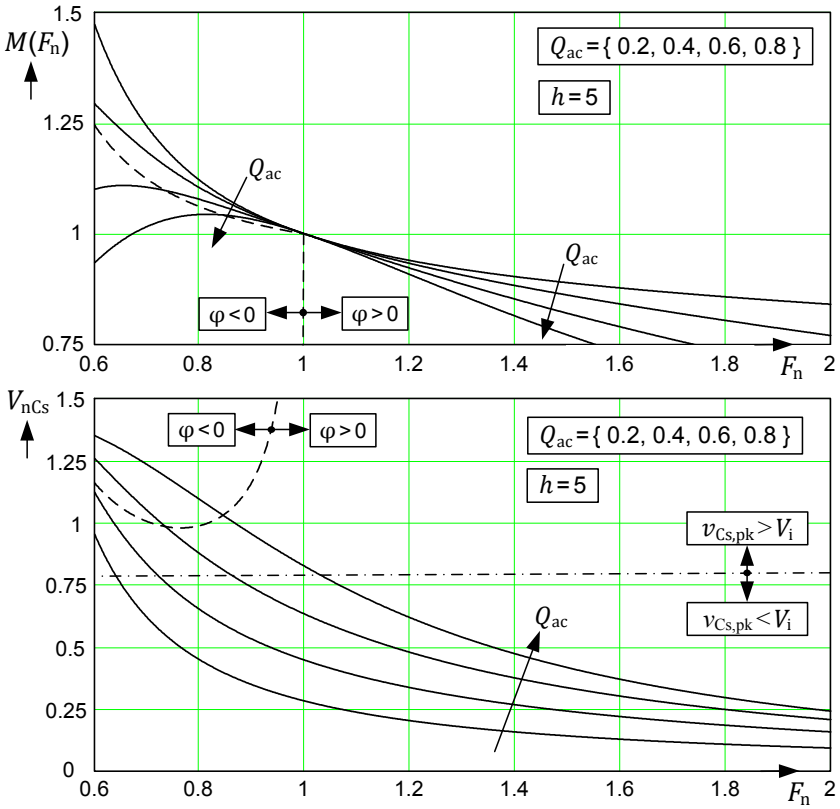

Fig. 4.12: Normalized DC-DC gain curves (top) and corresponding normalized resonant capacitor voltage (bottom) in dependence on F_n and design parameter Q_{ac}; φ: phase angle of the FHA input impedance Z_i of the resonant circuit, $\varphi > 0 \rightarrow$ ZVS, $\varphi < 0 \rightarrow$ ZCS (c.f. Chapter 3.1.6)

Based on the above analysis the clamping diode approach, though enabling feasible overload and short-circuit protection of the LLC resonant converter, diminishes the performance of the DC-DC converter at least in the case of a front-end power supply with hold-up requirement. In order to circumvent the performance implications of the clamping diode approach the author has proposed an extended clamping scheme in [Figge6], [Figge4] which is described and analyzed in the following.

4.3.2 Extended Resonant Capacitor Clamping Scheme

A feasible extension of the resonant capacitor clamping scheme is possible by introducing an additional energy storage element that absorbs the excessive energy of the resonant circuit in case of overload or short-circuit. Proposed circuit elements for this purpose are a voltage suppressor diode or a capacitor with sufficient capacitance, i.e. energy absorption capability. In the following the usage of a capacitor C_{cl} is assumed.

The extension of the resonant capacitor clamping scheme by C_{cl} is shown in Fig. 4.13 for both the full-bridge and the half-bridge variants. In both variants diodes D_3 and D_4 needs to be added. In case of the full-bridge variant these diodes guarantee a minimal charge of C_{cl} with

the nominal input voltage V_i. In case of the half-bridge variant they additionally serve as a flow path for the clamping current. By employing C_cl a decreasing clamping threshold of v_Cs in case of a line drop-out and subsequent temporary decreasing DC-link voltage V_i is omitted. Instead the voltage of C_cl remains at the previous nominal value and the operating region of the LLC converter is no longer limited by the presence of the clamping circuitry.
During an overload or short-circuit situation, C_cl absorbs energy and therefore is charged effecting a steady increase of voltage V_Ccl. Thus the capacitance of C_cl must be chosen according to expected numbers and intensities of overload events and C_cl needs to be equipped with an over voltage detection and a discharge circuitry (c.f. Fig. 4.13). The discharge circuitry may be a passive resistive network in its simplest implementation.

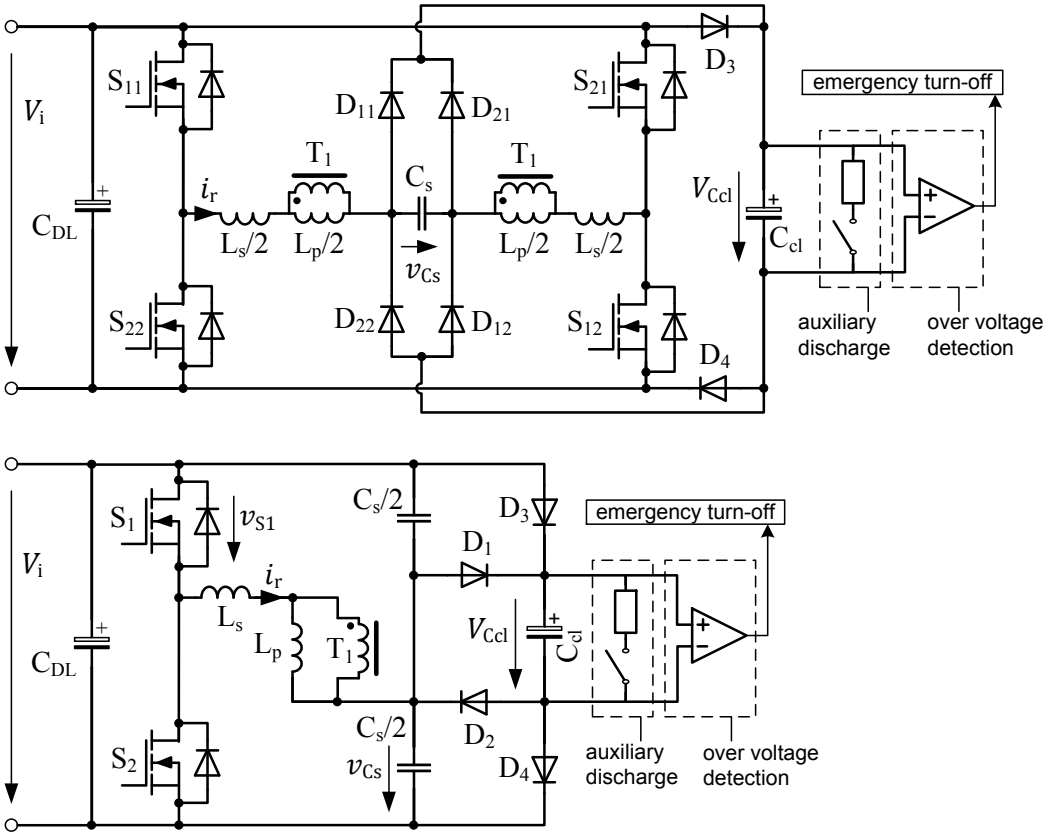

Fig. 4.13: Circuit diagrams of the extended resonant capacitor clamping scheme. Top: Full-bridge variant, Bottom: Half-bridge variant

For the both variants full-bridge and half-bridge different clamping thresholds result if the factor $k_\mathrm{cl} = V_\mathrm{i}/V_\mathrm{cl}$, which is defined as the ratio between the actual input voltage and the clamping voltage (here $V_\mathrm{cl} = V_\mathrm{Ccl}$), is unequal one. The clamping thresholds at which the amplitude of the resonant capacitor voltage equals the clamping voltage ($v_\mathrm{Cs,pk} = V_\mathrm{cl}$) is calculated according to (4.45) to

$$V_\mathrm{nCs,FB} = \frac{\pi}{4}\frac{1}{k_\mathrm{cl}}\bigg|_{0<k_\mathrm{cl}} \tag{4.46}$$

in case of a full-bridge configuration and to

$$V_{\mathrm{nCs,HB}} = \frac{\pi}{4}\frac{1}{k_{\mathrm{cl}}}(2 - k_{\mathrm{cl}})\Big|_{0<k_{\mathrm{cl}}<2} \tag{4.47}$$

in case of a half-bridge configuration. (4.46) and (4.47) are different because in case of the half-bridge a DC component $V_{\mathrm{i}}/2$ is superimposed on v_{Cs} as opposed to the full-bridge case. In the following the case of a half-bridge configuration will be followed.

The principle waveforms during a hold-up condition of both the extended and the basic clamping scheme are illustrated in Fig. 4.14 (left) for a half bridge configuration of the LLC converter. At t_0, V_{i} starts to decrease. At t_1, the actual value of V_{i} equals the peak voltage amplitude $v_{\mathrm{Cs,pk}}$ of the resonant capacitor. In case of the basic clamping scheme (dashed lines), the resonant capacitor voltage is clamped to the DC-link voltage for $t > t_1$ and the output power is accordingly reduced, resulting in less hold-up time. In case of the extended clamping scheme (solid lines), the clamping of the resonant capacitor voltage is delayed, until the peak voltage amplitude $v_{\mathrm{Cs,pk}}$ of the resonant capacitor equals the actual clamping capacitor voltage V_{Ccl} at $t = t_2$. Due to the diodes D_3 and D_4, at $t = t_2$, V_{Ccl} is still at the nominal value of V_{i} prior to the hold-up incidence.

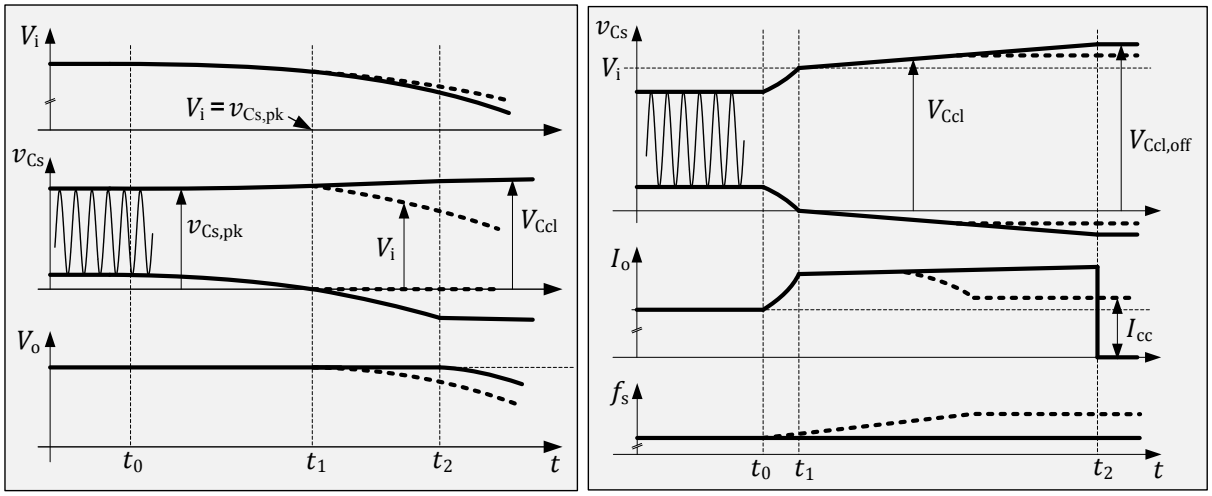

Fig. 4.14: Qualitative illustration of the behavior of several voltage and current quantities during a hold-up (left) and a short-circuit incidence (right). Left: Dashed lines represent the behavior in case of application of the basic resonant capacitor clamping approach (c.f. Fig. 4.11) and solid lines in case of the extended clamping approach (c.f. Fig. 4.13. Right: Dashed lines represent the behavior in case of the controller raising the switching frequency to regulate the output current to the limit value I_{cc}. Solid lines represent the behavior in case no controller action is initiated.

The principle waveforms during a short-circuit condition are illustrated in Fig. 4.14 (right).
At t_0 the output is assumed to be short-circuited, leading to a sharp increase in the output current I_{o}, resonant current i_{r} and resonant capacitor voltage v_{Cs}. For $t > t_1$ the resonant capacitor voltage is clamped to the increasing clamping capacitor voltage V_{Ccl}. If no controller action is applied or the controller fails and therefore the switching frequency remains constant (solid lines), the clamping capacitor voltage rises until a shut-off level $V_{\mathrm{Ccl,off}}$ is reached at $t = t_2$. If e.g. constant current (cc) control of the output is implemented, the controller increases the switching frequency to control the output current to the desired constant output current level I_{cc}. If the capacitance of the clamping capacitor is appropriately chosen considering the dy-

namic of the current controller, the clamping voltage does not reach the shut-off level and the converter remains working, with the ability to resume normal operation when the short-circuit is removed from the output.

4.3.3 Time Domain Analysis of the Resonant Capacitor Clamping Scheme

The circuit analysis is performed for the load case shorted output, which represents the worst case condition in respect to circuit element stresses. This load case simplifies the analysis largely, since the number of operating modes is reduced and the inductance L_p of the resonant circuit can be ignored. In the following analysis all components are assumed to be ideal. Furthermore it is assumed that the voltage of the clamping capacitor V_{Ccl} is constant within the clamping interval of each half period $T_s/2$.

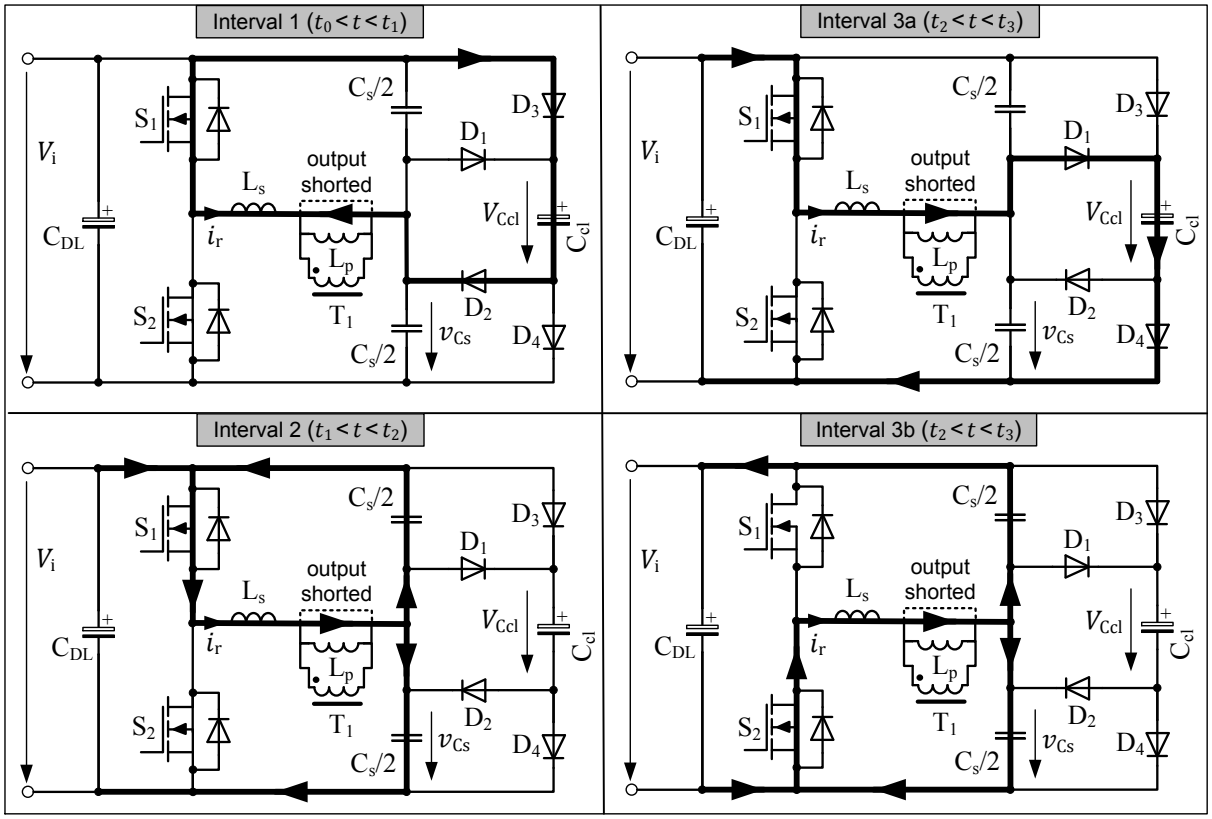

Fig. 4.15: Illustration of current flow paths of the short-circuit operation of a half-bridge LLC converter employing the extended resonant capacitor clamping scheme during intervals with piece-wise linear behavior of circuit quantities

The analysis reveals three possible operating modes A, B, C and four possible network states in a half period. Table 4.2 gives the assignment between network states and operating modes.

Table 4.2: Assignment of network states to the operating modes

Operating mode	Network state / Interval			
	1	*2*	*3a*	*3b*
A	x	x	x	
B	x	x		x
C		x		x

With given circuit element values L_s and C_s, the actual operating mode depends on the actual clamping voltage V_{Ccl} and the switching frequency f_s. Operation in Mode A can change to Mode B, if the switching frequency and/or the clamping voltage are increased. The same applies to the transition from Mode B to Mode C.

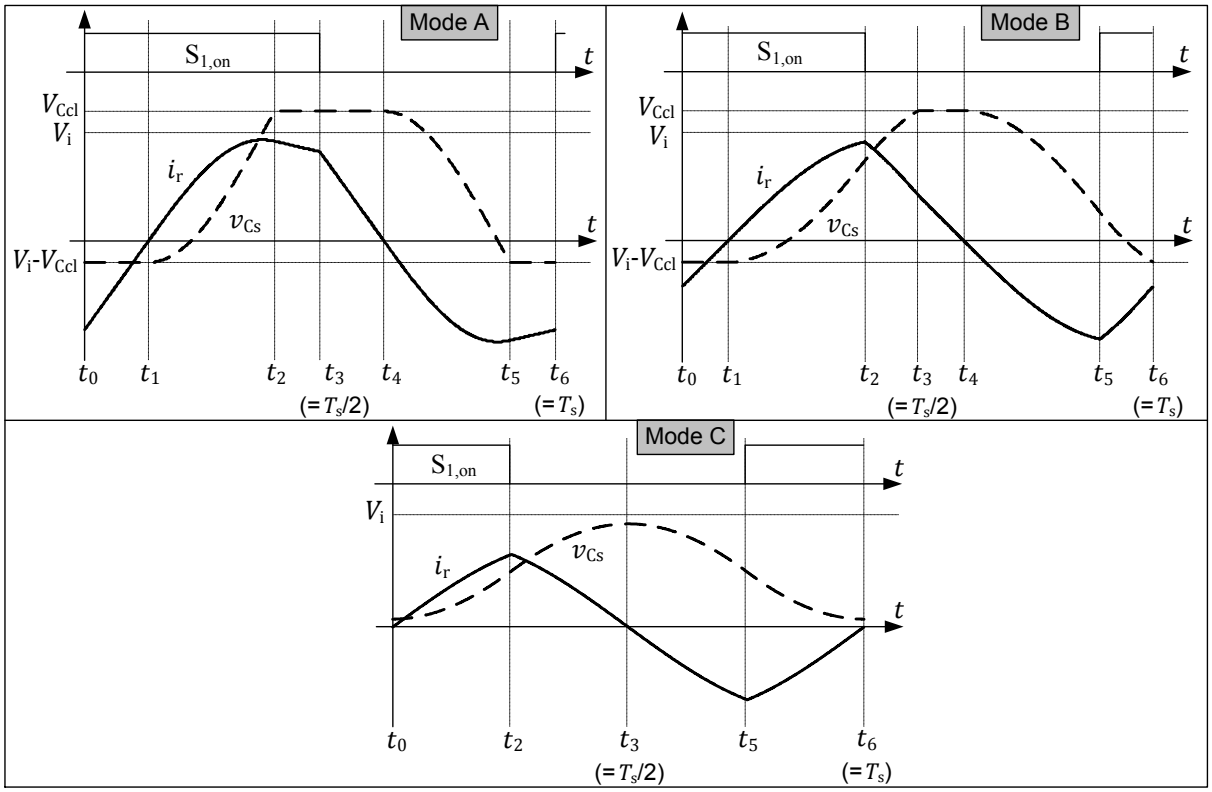

Fig. 4.16: Characteristic steady-state waveforms of operating modes A, B and C of a LLC converter operating at shorted output.

The time domain equations describing the states in case of a half-bridge configuration of the LLC converter are (c.f. Fig. 4.15 and Fig. 4.16):

- Interval 1 ($t_0 < t < t_1$)

$$i_r(t) = i_r(t_0) + \frac{1}{L_s} V_{Ccl}\, t \tag{4.48}$$

$$v_{Cs}(t) = V_i - V_{Ccl} \tag{4.49}$$

- Interval 2 ($t_1 < t < t_2$)

$$i_r(t) = \frac{V_{Ccl}}{Z_0} \sin\big(\omega_0 (t - t_1)\big) \tag{4.50}$$

$$v_{Cs}(t) = V_i - V_{Ccl} \cos(\omega_0 (t - t_1)) \tag{4.51}$$

- Interval 3a ($t_2 < t < t_3$)

$$i_r(t) = i_r(t_2) - \frac{1}{L_s} (V_{Ccl} - V_i)(t - t_2) \tag{4.52}$$

$$v_{Cs}(t) = V_{Ccl} \tag{4.53}$$

- Interval 3b ($t_2 < t < t_3$) (here: solution for Mode B)

$$i_\mathrm{r}(t) = \frac{V_\mathrm{Ccl}}{Z_0}\left[\sin\big(\omega_0(t-t_1)\big) - \sin\big(\omega_0(t-t_2)\big)\right] \tag{4.54}$$

$$v_\mathrm{Cs}(t) = V_\mathrm{i} - V_\mathrm{Ccl} - V_\mathrm{Ccl}\left[\cos\big(\omega_0(t-t_1)\big) - \cos\big(\omega_0(t-t_2)\big)\right]. \tag{4.55}$$

In Mode A the analysis reveals a closed-form solution: Applying the boundary conditions $i_\mathrm{r}(t_1) = 0$, $v_\mathrm{Cs}(t_2) = V_\mathrm{Ccl}$ and by symmetry $i_\mathrm{r}(t_0) = -i_\mathrm{r}(t_3) = -i_\mathrm{r}(T_\mathrm{s}/2)$, the unknowns are solved depending only on the input voltage V_i, clamping voltage V_Ccl and switching frequency $f_\mathrm{s} = 1/T_\mathrm{s}$:

$$-i_\mathrm{r}(t_0) = \frac{\frac{V_\mathrm{Ccl}}{Z_0}\sin(\omega_0 t_{12}) - \frac{1}{L_\mathrm{s}}(V_\mathrm{Ccl} - V_\mathrm{i})\left(\frac{T_\mathrm{s}}{2} - t_{12}\right)}{1 - \frac{V_\mathrm{Ccl} - V_\mathrm{i}}{V_\mathrm{Ccl}}}$$

$$t_{01} = -i_\mathrm{r}(t_0)L_\mathrm{s}/V_\mathrm{Ccl}$$

$$t_{12} = (1/\omega_0)\arccos(V_\mathrm{i}/V_\mathrm{Ccl} - 1)$$

$$t_{23} = T_\mathrm{s}/2 - t_{01} - t_{12} \tag{4.56}$$

with $t_{<xy>} = t_{<y>} - t_{<x>}$.

The boundary between Mode A and Mode B is given by condition $t_{23} = 0$ in Mode A.

For Mode B no closed-form solution could be found. Applying the boundary conditions $i_\mathrm{r}(t_1) = 0$, $v_\mathrm{Cs}(t_3) = V_\mathrm{Ccl}$, and by symmetry $i_\mathrm{r}(t_0) = -i_\mathrm{r}(t_3) = -i_\mathrm{r}(T_\mathrm{s}/2)$, the unknowns are solved to:

$$t_{01} = -i_\mathrm{r}(t_0)L_\mathrm{s}/V_\mathrm{Ccl}$$

$$t_{12} = T_\mathrm{s}/2 - t_{01} - t_{23}$$

$$t_{23} = (1/\omega_0)\arccos[2 - V_\mathrm{i}/V_\mathrm{Ccl} + \cos(\alpha)] \tag{4.57}$$

$$\text{with} \quad \alpha = \omega_0\left(\frac{T_\mathrm{s}}{2} + i_\mathrm{r}(t_0)\frac{L_\mathrm{s}}{V_\mathrm{Ccl}}\right),$$

where a recursive equation for $i_\mathrm{r}(t_0)$ results, which is only solvable by numerical methods:

$$-i_\mathrm{r}(t_0) = \frac{V_\mathrm{Ccl}}{Z_0}\left[\sin(\alpha) - \sin\arccos\left(2 - \frac{V_\mathrm{i}}{V_\mathrm{Ccl}} + \cos(\alpha)\right)\right]. \tag{4.58}$$

The boundary between Mode B and Mode A is given by condition $t_{23} = 0$ in Mode B. At this boundary the resonant current at instant t_3 is given by

$$-i_\mathrm{r}(t_0)|_{t23=0} = i_\mathrm{r}(t_3)|_{t23=0} = \frac{V_\mathrm{Ccl}}{L_\mathrm{s}}\left(\frac{T_\mathrm{s}}{2} - \frac{1}{\omega_0}\arccos\left(-1 - \frac{V_\mathrm{i}}{V_\mathrm{Ccl}}\right)\right). \tag{4.59}$$

The boundary between Mode B and Mode C is given by condition $-i_r(t_0) = i_r(t_3) = 0$. At this boundary the clamping action of the resonant capacitor disappears. Thus the range $0 < -i_r(t_0) < -i_r(t_0)|_{t23=0}$ is the search region for numerical solving of (4.58).

In Mode C the time domain equations describing Interval 3b are different to (4.54) and (4.55). Since no clamping appears in Mode C the voltage V_{Ccl} is substituted by the free variable $v_{\mathrm{Cs,pk}}$. Solving the differential equations results in:

Interval 3b ($t_2 < t < t_3$) (here: solution for Mode C)

$$i_{\mathrm{r}}(t) = -\frac{v_{\mathrm{Cs,pk}}}{Z_0}\sin(\omega_0(t-t_3)) \tag{4.60}$$

$$v_{\mathrm{Cs}}(t) = v_{\mathrm{Cs,pk}}\cos(\omega_0(t-t_3))\,. \tag{4.61}$$

Taking symmetry into account the unknowns are solved into a closed-form solution:

$$t_{02} = t_{23} = T_{\mathrm{s}}/4$$

$$v_{\mathrm{Cs,pk}} = \frac{V_{\mathrm{i}}/2}{\cos(\omega_0\, T_{\mathrm{s}}/4\,)}\,. \tag{4.62}$$

By (4.48) to (4.62) the exact time domain equations for the converter operating at shorted output and under the assumption that V_{Ccl} is constant are given. In order to calculate the voltage increase of C_{cl} over successive switching intervals the charge Q that is transferred into C_{cl} during the clamping action has to be accumulated. The electrical charge that is transferred to the clamping capacitor in each half period $T_{\mathrm{s}}/2$ is given by

$$Q_{\mathrm{A}} = \frac{1}{2}\big(-i_{\mathrm{r}}(t_0)\big)t_{01} + \frac{1}{2}\left(\frac{V_{\mathrm{Ccl}}}{Z_0}\sin(\omega_0 t_{12}) - i_{\mathrm{r}}(t_0)\right)t_{23}$$

$$Q_{\mathrm{B}} = \frac{1}{2}\big(-i_{\mathrm{r}}(t_0)\big)t_{01} \tag{4.63}$$

with $Q_{<x>}$: Charge at Mode <x>. The incremental voltage increase ΔV_{Ccl} of the clamping capacitor within each half period $T_{\mathrm{s}}/2$ therefore is determined by $\Delta V_{\mathrm{Ccl}} = Q_{<x>}/C_{\mathrm{cl}}$. The calculated voltage increase based on the assumption of ideal circuit elements represents a worst case scenario for the rapidness of increase of V_{Ccl}. In reality the circuit losses effect a reduction of the transferred charge $Q_{<x>}$ and the required capacitance value of C_{cl}.

The operation of the extended clamping scheme in case of an overload or hold-up condition, i.e. non zero output voltage, requires a more involved analysis, because L_{p} cannot be neglected. Hence one more state variable and additional operating modes arise. The theoretical analysis of this more general case is not performed within this work. Analysis and calculations have to be performed by time domain simulation methods for such cases if required.

4.3.4 Experimental Results Related to the Resonant Capacitor Clamping Scheme

In order to verify the theoretical analysis and to demonstrate the benefits of the extended clamping scheme, measurements on a prototype are presented. The prototype comprises a DC-DC LLC resonant converter in accordance to the schematic of Fig. 4.11 right and Fig. 4.13 bottom resp. The converter is intended for use in a telecom rectifier and thereby complying with the specification given in Table 4.3. The design of the prototype converter was not performed by the design optimization procedures presented in Chapter 5. Nevertheless it is a valid design for a real industrial converter and therefore suitable for the investigation of the clamping schemes.

Table 4.3: Rough specification of a LLC resonant converter

$V_{\mathrm{i,nom}}$	400 V
$V_{\mathrm{o,nom}}$	53.5 V
$V_{\mathrm{o,min}}$	41 V
$I_{\mathrm{o,max}}$	42 A
$P_{\mathrm{o,nom}}$	1800 W

f_0	118 kHz
$f_{\mathrm{s,min}}$	90 kHz
h	5.8
$J_{\mathrm{o(Q)}}$	0.536

The measurements are carried out with a DC supply for ease of demonstration. A superimposed voltage ripple with twice the grid frequency has to be considered additionally in case the DC link is fed by a PFC rectifier.

4.3.4.1 Experimental Results in Hold-Up Condition

The characteristic steady state waveforms of the prototype converter are shown in Fig. 4.17 for the case that no clamping circuitry is applied. The top of Fig. 4.17 represents the nominal operating point. The bottom represents the maximum DC-DC gain of the converter with the switching frequency set to a minimum of 90 kHz ($F_{\mathrm{n}} = 90\,\mathrm{kHz} / 118\,\mathrm{kHz} \approx 0.76$). Further decrease of the minimum switching frequency would affect the Zero Voltage Switching performance of the half-bridge MOSFETs S_1/S_2 and therefore is not permitted by design constraint.

From the bottom of Fig. 4.17 it can be observed that the application of the basic clamping scheme (Fig. 4.11) would disturb the converter operation at high DC-DC gain due to the negative voltage difference $V_{\mathrm{i}} - v_{\mathrm{Cs,pk}}$ and the resulting forward bias of diodes D_1 resp. D_2. The negative voltage difference is caused by the low input voltage V_{i} at this hold-up condition point and is expressed by

$$V_{\mathrm{i}} - v_{\mathrm{Cs,pk}} = 276\,\mathrm{V} - 382\,\mathrm{V} = -106\,\mathrm{V} < 0\,V\,. \tag{4.64}$$

The application of the extended clamping scheme (Fig. 4.13) avoids the disturbed operation because the clamping voltage is not the input voltage V_{i} but the actual voltage of the clamping capacitor V_{Ccl} and therefore

$$V_{Ccl} - v_{Cs\_pk} = 398\mathrm{V} - 382\mathrm{V} = 16\,\mathrm{V} > 0\,V. \tag{4.65}$$

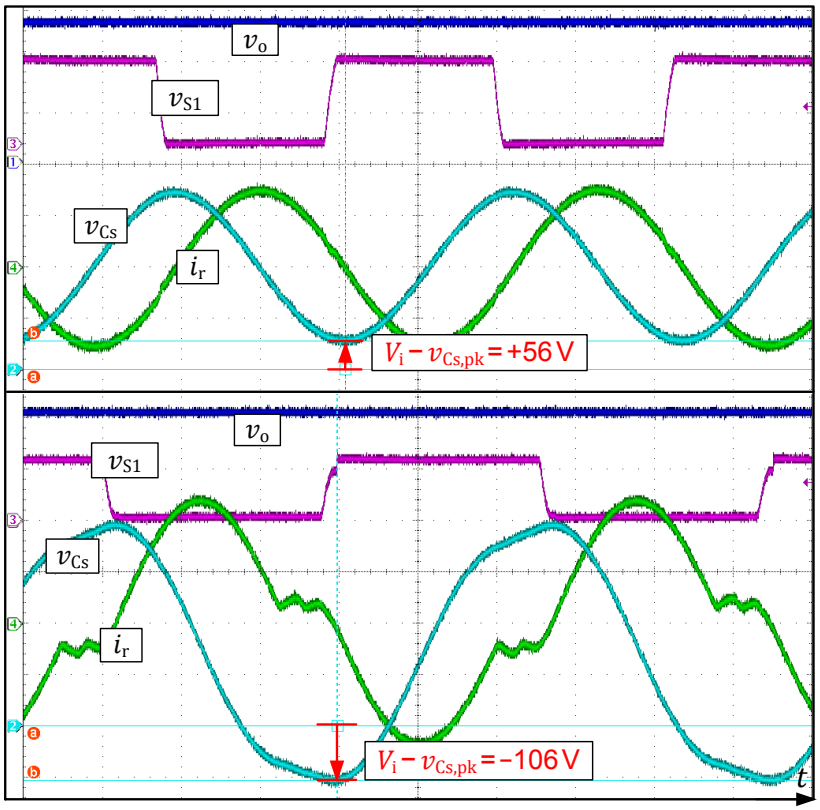

Fig. 4.17: Steady state prototype waveforms without clamping circuits applied; Top: Nominal operating point (V_i = 398 V, V_o = 53.5 V, I_o = 34 A, $f_s = f_0$ = 118 kHz); Bottom: Operating point at minimum output voltage, minimum switching frequency, and maximum DC-DC gain (V_i = 276 V, V_o = 41 V, I_o = 41.5 A, $f_s = f_{s,min}$ = 90 kHz; Scalings: Ch 1 (v_o) 20 V/div, Ch 2 (v_{Cs}) 100 V/div, Ch 3 (v_{S1}) 250 V/div, Ch 4 (i_r) 10 A/div, time (t) 2 µs/div

The different characteristic of the clamping schemes at high DC-DC gain results in different hold-up times. Fig. 4.18 shows measurements of a hold-up condition at 90% of rated output power and compares the characteristic waveforms of both the basic and the extended clamping scheme. It can be observed that the hold-up time of both the nominal output voltage (V_o = 53.5 V) as well as the hold-up time of the minimum output voltage ($V_{o,min}$ = 41 V) is increased by the application of the extended clamping scheme.

The comparison shown by Fig. 4.18 was performed for different output power levels and is summarized in Fig. 4.19. The benefit of the extended clamping scheme is increasing with output power. At 100% the hold- of rated output power up time of V_o = 53.5 V is increased by 65% and the hold-up time of $V_{o,min}$ = 41 V is increased by 83%. The benefits decrease with decreasing output power. Below 80% load the hold-up time of V_o = 53.5 V is similar to both clamping schemes. The reason for this is that the minimum switching frequency of 90 kHz is reached before any clamping action takes place for both clamping schemes below 80% load.

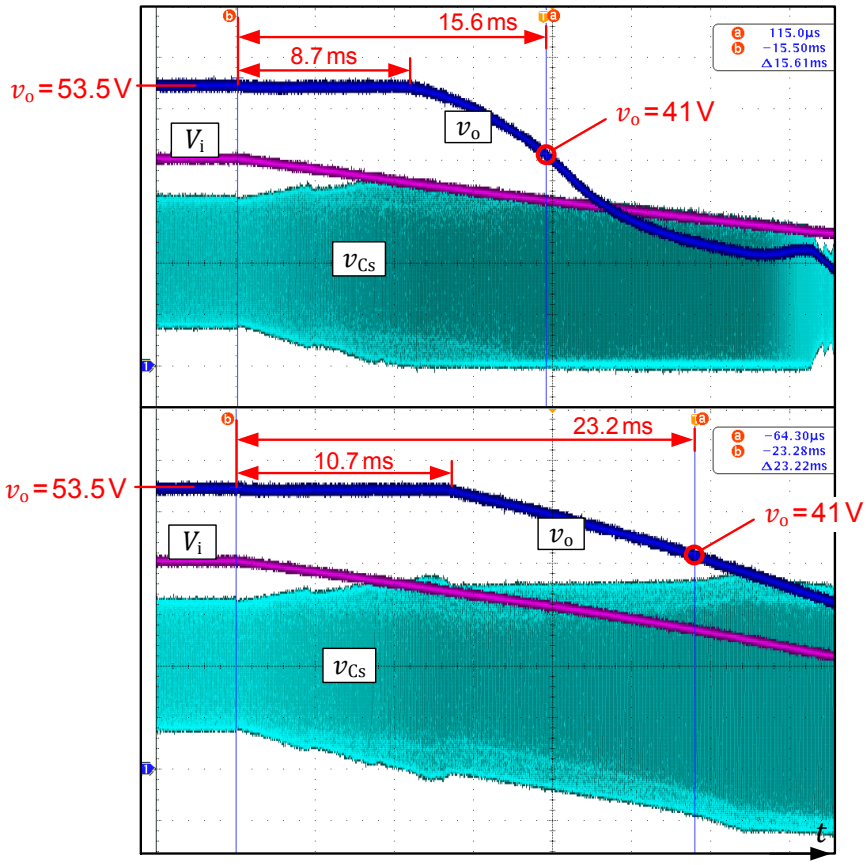

Fig. 4.18: Prototype waveforms of a hold-up condition at 90% of rated output power (P_o = 1620 W), initial values are V_i = 400 V, V_o = 53.5 V; Top: Basic clamping scheme applied, Bottom: Extended clamping scheme applied; Scalings: Ch 1 (v_o) 10 V/div, Ch 2 (v_{Cs}) 100 V/div, Ch 3 (v_i) 100 V/div, time (t) 4 ms/div

The bottom of Fig. 4.19 compares both clamping schemes taking the additional volume of the capacitor C_{cl} into account. Therefore the capacitance of C_{cl} (here: 82 µF) was added to the DC link capacitance when measuring the performance of the basic clamping scheme. In this comparison the hold-up time of V_o = 53.5 V is increased by 48% and V_o = 41 V by 73% at 100% output load. The value of C_{cl} was determined by the investigations of the short-circuit behavior and requirements on C_{cl} which is discussed in the next chapter.

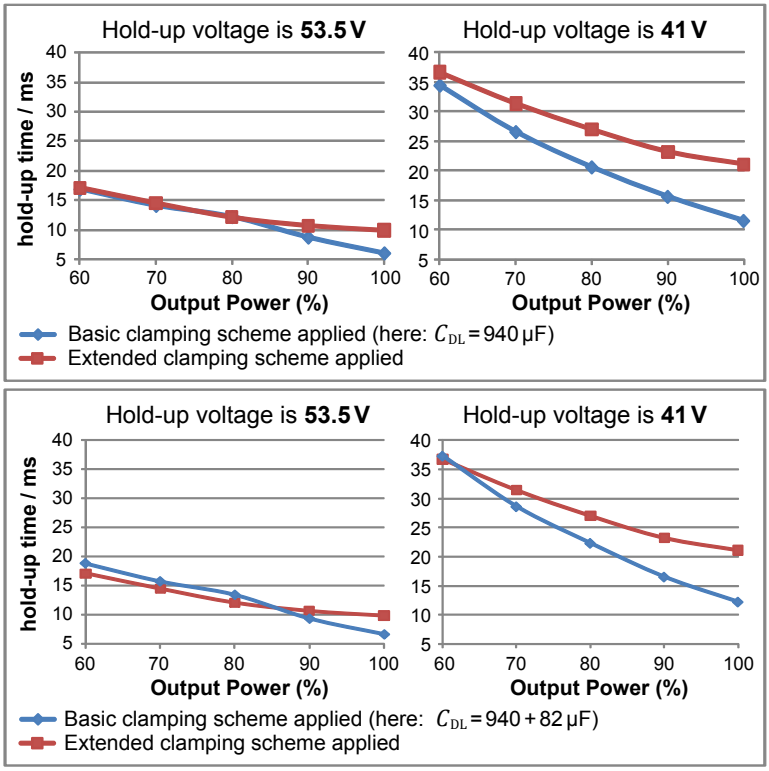

Fig. 4.19: Measured hold-up times versus output power; Top: Both clamping schemes use the same value of DC link capacitance, Bottom: The basic clamping scheme uses a higher value of DC link capacitance in order to compare assemblies with equal volume of the capacitances.

4.3.4.2 Experimental Results in Short-Circuit Condition

When applying the extended clamping scheme the capacitance value of C_{cl} has to be appropriately chosen. The required energy buffering capability of C_{cl} depends on the specified overload characteristic of the converter. If an overload shut-off is desired, the value of C_{cl} can be small, just serving for some time delay to be charged to a shut-off voltage level and trigger the shut-off (c.f. Fig. 4.14 right). If constant current regulation of the output is desired, worst case to the energy buffering capability of C_{cl} obviously is an instantaneous short-circuit condition of the output. In this case C_{cl} is getting charged until the switching frequency is sufficiently increased by the current controller. Fig. 4.20 shows characteristic waveforms of an instantaneous short-circuit event into 0.01 Ω measured on the prototype with C_{cl} = 82 µF. With the slope of the switching frequency limited to 230 Hz/µs the time duration of the clamping action is measured to 290 µs, giving a voltage increase to the clamping capacitor from 400 V to 423 V. The clamping energy of the instantaneous short-circuit event of Fig. 4.20 is 776 mJ and the average power of the clamping action is 776 mJ / 290 µs = 2676 W. Assuming the mentioned parameters and setting an emergency shut-off level of 430 V, the converter will not shut-off in case of an instantaneous short-circuit but run over into constant current regulation (c.f. Fig. 4.14 right). The shut-off level of 430 V enables the use of a 450 V rated capacitor. Those are the most common and therefore the most cost effective types. In succession to a short-circuit event the voltage of C_{cl} must be reset to the steady state DC link voltage by means of an auxiliary discharge circuitry (c.f. Fig. 4.13). The latter depends upon the real shorting conditions and is not analyzed in this work.

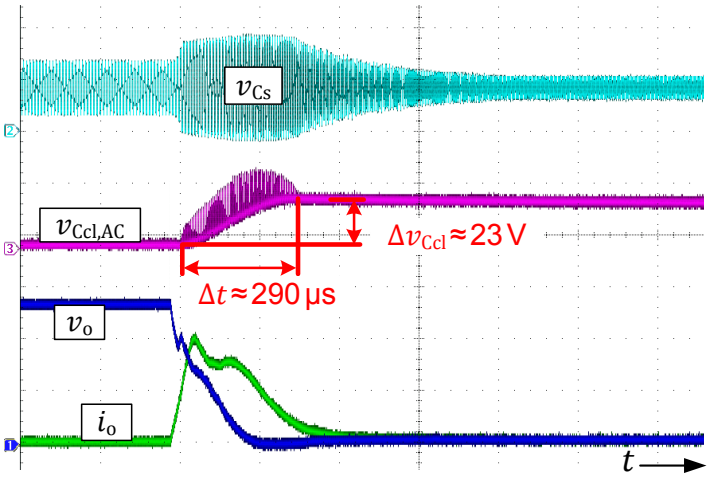

Fig. 4.20: Prototype waveforms of a short-circuit event, initial values are V_i = 400 V, V_o = 53.5 V, I_o = 30 A, short-circuit resistance is 0.01 Ω, C_{cl} is 82 µF; Scalings: Ch 1 (v_o) 20 V/div, Ch 2 (v_{Cs}) 250 V/div, Ch 3 ($v_{Ccl,AC}$) 25 V/div, Ch 4 (i_o) 500 A/div, time (t) 200 µs/div

The capacitance value of C_{cl} can be further reduced, if the limit of the switching frequency slope is increased or if the abruptness of the short-circuit event, i.e. the short-circuit resistance and slope, is specified less hard. The final tuning of the short-circuit behavior has to be performed based on a concrete specification of the unit of application.

The prototype measurement of the instantaneous short-circuit event also demonstrates validity of the circuit analysis of Chapter 4.3.3. All operating modes A, B and C can be extracted from the measurement of the short-circuit event as done in Fig. 4.21. The slope of the clamped resonant capacitor voltage v_{Cs} is caused by non-ideal impedance of the clamping capacitor C_{cl}.

4.3.5 Summary of Resonant Capacitor Clamping Approach

In a typical LLC converter design the hold-up time suffers from the application of the basic clamping diode approach for short-circuit protection. This can be largely reduced by using the extended clamping scheme comprising a separate clamping capacitor C_{cl} and additional charging diodes. The extension of the clamping scheme is applicable to the full-bridge as well as to the half-bridge configuration of the LLC converter. However, the benefit is higher in case of a half-bridge configuration.

As the most relevant result of the investigation the measurements show increased hold-up time by application of the extended clamping scheme compared to the basic clamping diode approach. The hold-up time of $V_{o,min}$ = 41 V increases in the range of 6% at 60% load up to 83% at 100% load. An important design step is the selection of the capacitance value of C_{cl}, if uninterrupted converter operation in case of an instantaneous short-circuit event is desired. Measurements show that the capacitance of C_{cl} being in the range of 10% of the bulk capacitance results in an acceptable peak voltage of 423 V at C_{cl}. The final capacitance value of C_{cl} must be selected based on a concrete specification of the unit of application.

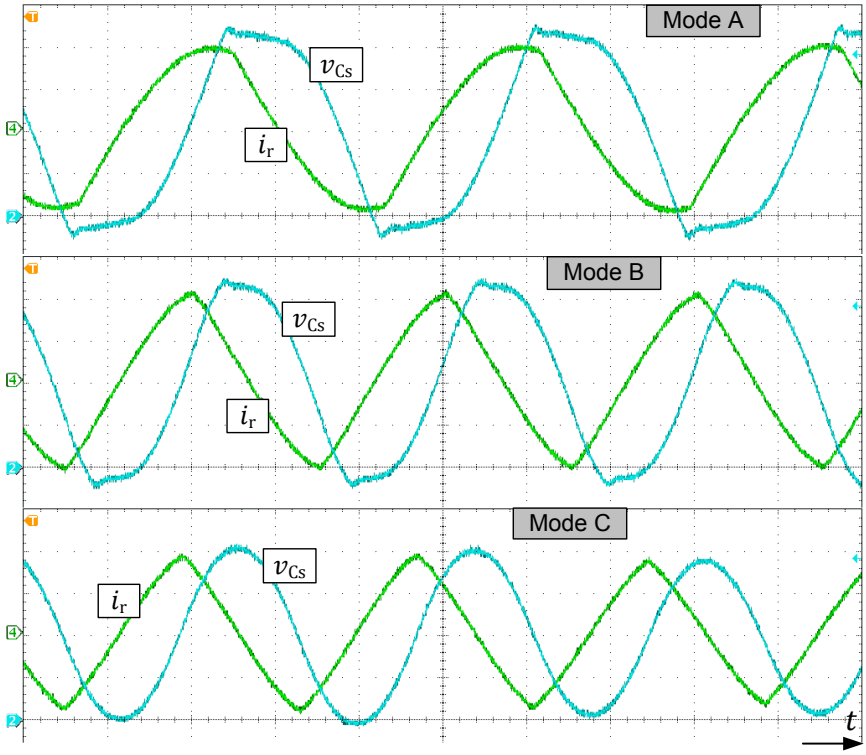

Fig. 4.21: On the prototype measured waveforms of a short-circuit event: Extraction of the operating modes revealed by the circuit analysis of Chapter 4.3.3; Scalings: Ch 2 (v_{Cs}) 100 V/div, Ch 4 (i_r) 20 A/div, time (t) 2 µs/div

5 Numerical Design Optimization

In general the complexity of an optimal converter design depends on the degree of freedom of the design variables with respect to specific design goals and design constraints. At least three optimization levels with typically increasing number of variables can be distinguished: At first the optimization on system level. This level comprises the least number of variables, like e.g. the number of converters in parallel for a given system power. Secondly the optimization on circuit level: On this level the design variables are mainly the lumped values of circuit elements like inductances, capacitances and XFMR turns ratios. Those variables describe the converter behavior, i.e. the functional waveforms, steady state operating points and dynamic characteristics. Thirdly the optimization on component level: On this level basically every physical quantity of a component can be treated as a design variable. However, since the analytical and computational effort of an optimal design procedure should be obviously minimized, a reasonable selection of design variables is compulsory. Design variables on this level are e.g. number of turns, air gap length and physical dimensions of magnetic components. In case the component is not build by the designer but has to be selected out of a given supply, the degree of freedom reduces to the choice of type and number of components in parallel resp. series.

When looking at the optimal design process of the LLC resonant converter compared to PWM-type converters a clear difference can be stated: For PWM type converters the number of components in the idealized equivalent circuit is small and the basic converter operation is simple and can be analytically described, at least for the basic PWM type topologies. For the LLC resonant converter, in more general for all resonant converters, the number of components in the equivalent circuit is increased and the basic converter operation is more complex. Also the degree of freedom in choosing the values of the lumped circuit elements is increased. For this reason the optimal design of the LLC resonant converter is not just subject to the optimization of the components, but also to the optimization of the converter operation, i.e. the choice of lumped element values.

A main step in the optimal converter design is the choice of the objective variable, the parameter search vector $\boldsymbol{x}$ and the formulation of the objective function $F(\boldsymbol{x})$ subject to the design constraints $g(\boldsymbol{x}) < 0$. Nowadays the most desired objective variable is the conversion efficiency η. Other interesting variables are the power density and costs. All those objective variables imply the calculation of the power losses within the objective function. Depending on the desired accuracy of the loss models the objective function becomes typically non analytic or at least difficult to differentiate, even for PWM-type converters. For this reason the design optimization is usually done by means of numerical computing. A lot of examples for PWM-type converters and resonant converters are given in literature, e.g. [Badstuebner], [Badstuebner2], [Biela], [Kolar], [Waffler2], [Foster], [Mirjafari], [Yu2], [Du], at which this work extends the examples from literature by a complete consideration of constraints and their influences for an application of the LLC resonant converter within industrial PSUs with high output power. The non-linear loss models presented in Chapter 3 and the nonlinear steady-state behavior of the LLC converter implies the numerical optimization method for the LLC converter. The optimization is performed for the objective variable η in this work, since this is the most interesting quantity for current industrial requirements.

5.1 Constraints in the LLC Converter Design

The optimization of real world problems typically requires considering constraints besides the optimization of the objective function. For technical systems those constraints are in general given by physical limits of components or signals and by specified boundaries of the operating region. For power electronic systems constraints are for example the saturation flux density of a magnetic component or the maximal allowed voltage of a capacitor or semiconductor component.

The consideration of constraints usually complicates the evaluation of the optimization problem. Additional measures have to be implemented into the optimization solver and problems in convergence may occur. But nowadays common numerical computing tools are capable of solving also black-box problems within acceptable time frames. Black-box models have the advantage that the constraints can be easily added to the optimization task by additional procedural inspection inside the black-box. Thus black-box methods combined with today's computing capabilities are well suited for treating optimization problems of real world technical systems like power electronic converters and are applied in this work. They give great flexibility in formulating the design problem and enable reusability of objective function code.

Possible constraints for the LLC resonant converter design are given in the following:

Complete coverage of the specified operating region:
The LLC DC-DC converter should cover a certain input-/output voltage range preferably throughout the complete load range $J_{\mathrm{o,min}} < J_{\mathrm{o}} < J_{\mathrm{o,max}}$. The operating region constraints of the LLC converter are described by (4.1) to (4.6).

Physical limits:
The peak flux density within the magnetic components shall not saturate the core in any operating condition. Therefore the combination of values for core cross section A_{c}, number of turns N_{w} and air gap l_{g} is limited which is expressed by

$$\hat{b} < B_{\mathrm{L,sat}}|_{T_{\mathrm{c}}=T_{\mathrm{c,max}}} \tag{5.1}$$

Another critical component of a series resonant type converter is the series resonant capacitor C_{s}. The resulting peak voltage has to be checked for not violating the maximal allowed voltage of the component in any operating condition.

$$v_{\mathrm{Cs,pk}} < V_{\mathrm{Cs,max}} \tag{5.2}$$

Other constraints:
When calculating the overall power loss P_{v} of the LLC converter at a given operating point, it is assumed that the bridge is operating under ZVS. ZVS operation should be achieved at least at nominal operating conditions, i.e. for nominal output voltage and output current range. Therefore it depends on the converter specification. For the sake of a reduced number of calculations within one objective function call, the ZVS condition is represented by (3.46) for the design example of Chapter 5.4. If the results of the optimization run indicate that the ZVS condition is limiting the optimized result, a more detailed inspection of the ZVS condition is

necessary, including a sensitivity analysis on the optimized result. Furthermore condition (3.46) neglects the hold-up, i.e. deep below resonance operation at $V_p = V_{p,min}$. But since this is only a special operating condition that has no efficiency impact, violation of the ZVS condition at this operating point is accepted.
Another critical point is the consideration of element value deviations from the intended value. Because in mass production the reproduction accuracy is limited to a certain tolerance class and especially capacitors might be prone to aging, a slight deviation of element values must not prevent the converter from operating in accordance to the specifications. This can be checked in an approximate or in an exact manner. For exact checking every constraint would have to be checked with all possible combinations of worst case deviations of all resonant circuit elements. Since for the LLC converter there are three elements L_s, C_s, L_p, and each of them can be deviated in positive or negative direction, this results in eight combinations of worst case deviations. Checking for eight more constraints would add considerate computation time to the optimization procedure. To omit the additional evaluations an iterative method can be used yielding approximate but feasible results: After the first optimization run the violation of constraints under element value deviations have to be checked. If constraints are violated, a certain amount of clearance needs to be subtracted from the constraints prior to a second optimization run. A feasible design is found by repeating this procedure as required. In [Binder] the influence of component tolerances on an optimal converter design is analyzed by gradually evaluating the correlation between each design parameter deviation and the design constraints. This analysis determines the worst-case deviations and its analytically expressed influence on the optimal converter design parameters. However, since the method is based on FHA modeling, it cannot be applied for the design methodology followed in this work.

5.2 The Optimization Solver

Because the LLC steady-state model is implemented in MATHEMATICA, an optimization solver was chosen that could be also used in MATHEMATICA. The Global Optimization package (Version 8.0) [Loehle] provides different global optimization methods for MATHEMATICA. It was easily available to the author and therefore used throughout this work.

The objective function $F(\boldsymbol{x})$ that is build for optimizing the LLC resonant converter is nonlinear and non-analytic. It is essentially built as a black-box function, which includes also the design constraints treated by a penalty system. The objective function therefore can exhibit also discontinuities of the function value at the borders of the feasible region. Furthermore the existence of local optima cannot be precluded. The optimization solver should be able to treat such discontinuities and should be robust to local optima. Within the Global Optimization package the optimization solver GlobalMinima (GM) is suitable for such kind of optimization problems, because it does not calculate any derivatives but instead relies on an evolutional method. Fig. 5.1 shows a flow-chart of the GM algorithm.

The parameters to be initially supplied to the GM algorithm are

- n_{igp}: number of initial grid points
- k_{ctr}: initial contraction coefficient
- k_{tol}: absolute value of minimal progress in the objective function to proceed the algorithm

- $\boldsymbol{x}_{\text{low}}$, $\boldsymbol{x}_{\text{high}}$: boundaries of initial search region for the search vector; the global minimum should be located within these boundaries to ensure maximal success of the algorithm

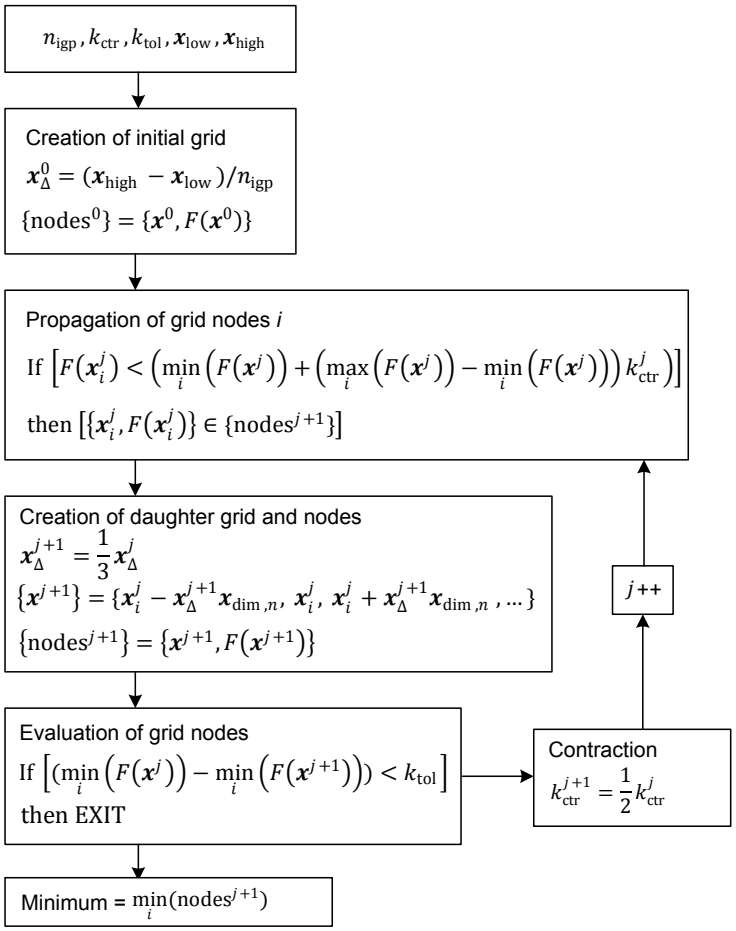

Fig. 5.1: Flow-chart of the GM algorithm; $\boldsymbol{x}_i^j$: search vector i at generation j and $\boldsymbol{x}_{\Delta}^j$: distance between grid points for generation j and $\boldsymbol{x}_{\text{dim,n}}$: zero vector except a one at row n

The GM algorithm initially evaluates the objective function $F(\boldsymbol{x})$ at points of a Cartesian grid located in between the given boundaries $\boldsymbol{x}_{\text{low}}$ and $\boldsymbol{x}_{\text{high}}$ and with a grid spacing of $\boldsymbol{x}_{\Delta}^{0} = (\boldsymbol{x}_{\text{high}} - \boldsymbol{x}_{\text{low}})/n_{\text{igp}}$. The resulting initial grid nodes $\{nodes^0\} = \{\boldsymbol{x}^0, F(\boldsymbol{x}_0)\}$ are then entered into an iterative evaluation loop with daughter nodes generated at each iteration step. The algorithm stops if within one iteration the progress in the objective function is lower than the predefined tolerance k_{tol}.

In each iteration the grid spacing $\boldsymbol{x}_{\Delta}$ used to generate the daughter nodes $\boldsymbol{x}^{j+1}$ is reduced by factor 1/3. This specific factor exactly ensures that on the one hand every point in between the search region $\boldsymbol{x}_{\text{low}}$ to $\boldsymbol{x}_{\text{high}}$ can be reached by the algorithm and on the other hand no points will be evaluated twice. This can be shown by means of the geometric series. Assuming one initial grid point continuously moving in one direction by the actual grid spacing $\boldsymbol{x}_{\Delta}^{j}$, the overall movement of the point after endless iterations will be

$$\boldsymbol{x}_{\Delta}^{0} \sum_{n=1}^{\infty} \left(\frac{1}{3}\right)^{n} = 0.5\, \boldsymbol{x}_{\Delta}^{0}\,,$$

i.e. every initial grid point can move in maximum one half of the initial grid spacing to its sides, which proves the proposition.

Furthermore the contraction coefficient k_{ctr} is halved at each iteration of the algorithm. This behavior is a build-in of the GM algorithm and cannot be modified. It is assumed that other rates of decreasing k_{ctr} would also enable the convergence of the algorithm, but that halving gives an overall good behavior of the algorithm in terms of computational efficiency and robustness to local optima. Instead of controlling the progress in k_{ctr} the user can control the initial value of k_{ctr}. A high value (must be less than one) will generate more grid points in the early stage of the algorithm and hence will be beneficial in case of noisy functions, i.e. in case of many small local minima with respect to the initial grid density. A low value will guide the algorithm with less computational effort to more general minima, and hence will be beneficial in case of few and broader minima with respect to the initial grid density.

The success of the GM algorithm and the quality of the detected minimum especially depend on the choice of the parameters n_{igp} and k_{ctr} in relation to the characteristic of the objective function. Hence, the results of the GM algorithm have to be checked for reproducibility by varying the boundaries or density of the initial grid to find optimal parameter values n_{igp} and k_{ctr} for the actual problem.

5.3 Manifestation of Design Problems

5.3.1 Design Parameters and Interdependencies

In general every physical quantity of the converter setup can be an optimization parameter. But it is of course reasonable to choose only those parameters that are evident to the subject of the optimization. Since a converter can usually be described by an equivalent circuit that comprises lumped circuit elements, it is furthermore feasible to consider the lumped circuit element values as basic optimization parameters. Additional optimization parameters can be added for the physical components that represent the lumped circuit elements. The additional parameters can be processed in two ways. Many publications use an optimization sub-loop for the physical component, thereby providing a decoupling between the lumped circuit elements and the physical quantities of the components. Such a decoupling is likely to ease the optimization procedure and makes it more flexible. However, in a system of multiple circuit elements the optimization sub-loops yield the disadvantage that not every possible combination of physical quantities of the whole converter arrangement is tested by the optimization solver. Especially if the circuit elements are interdependent subject to the design constraints, the global optimum of the whole circuit arrangement might not be found. In such case it is appropriate to add the additional parameters of the physical component to the global search vector $\boldsymbol{x}$.

The DC-DC gain diagram can be considered as a map of steady-state operating conditions and therefore as map of the whole operating area (c.f. Fig. 4.1). The curves in the normalized DC-DC gain diagram are subject to the parameters inductance ratio h and normalized output cur-

rent J_o. Furthermore the x-axis of the diagram is normalized to the resonant frequency f_0 and the y-axis normalization includes the XFMR turns ratio n. The parameters h, J_o, f_0 and n are therefore the basic degrees of freedom of the design problem. The three parameters h, J_o and f_0 are bijectively coupled to the resonant circuit element values L_s, C_s and L_p. The XFMR turns ratio n just scales the input-to-output voltage ratio by a rational number.

Since PWM-type converters have been state-of-the-art for power supply designs up to now, it is appropriate to compare the degrees of freedom between PWM-type and the LLC resonant converter. PWM-type converters basically have the degrees of freedom inductance value L_f, switching frequency f_s and XFMR turns ratio n. They therefore exhibit one parameter less on circuit level. Additionally the interdependence of design parameters has to be considered in order to compare the design complexities. For the PWM-type converters it can be stated that the three design parameters are less interdependent: In the continuous conduction mode there is only one DC-DC gain curve which is controlled by the applied duty cycle and independent on the inductance value or the output loading. Hence, for meeting the design constraints regarding full load and short-circuit operations no dependence between the design parameters needs to be considered. In the discontinuous conduction mode the DC-DC gain curves become as well dependent on the inductance value and the output loading. But typically no constraints or at most soft constraints are interrelated to this mode of operation. For the LLC converter the interdependence between the four design parameters is much more distinct: The design constraints (4.1) to (4.6) limit the feasible range of the design parameters. From the DC-DC gain diagram Fig. 4.1 it can be observed that the constraints cannot be met if any of the design parameters is out of a feasible range. It therefore can be stated that the four circuit level design parameters of the LLC resonant converter are completely interdependent as illustrated in Fig. 5.2.

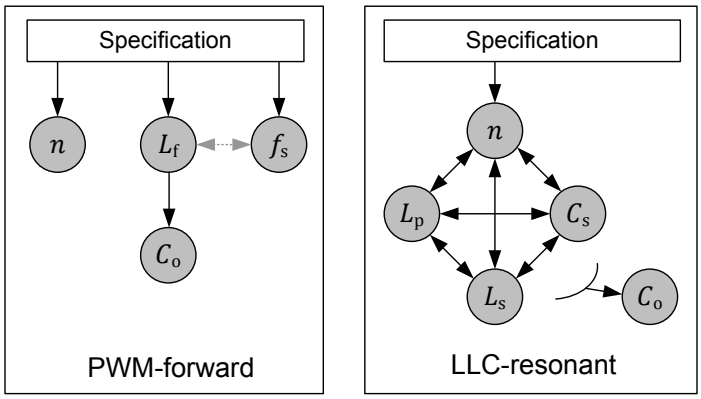

Fig. 5.2: Comparison of basic design parameter interdependencies

Due to the complete interdependence of the circuit level design parameters of the LLC converter, it is feasible to formulate basic design problems of the LLC converter. The solutions to the basic design problems give additional insight and can support the treatment of similar or more specific design problems.

The design optimization in this work is focused on steady-state operating conditions within the specified operating range. The dynamic behavior related to the regulation of output voltage and output current is not part of the optimization considerations. It is therefore assumed that the regulatory functions are capable of dealing with every variant of converter designs.

Even though this assumption should be further investigated in future work, it is supported by practical experience and for now adopted throughout this work.

5.3.2 The LLC Converter Common Design Problem

A main property of the DC-DC gain characteristic of the LLC converter is the load independent DC-DC gain point that occurs when the switching frequency of an ideal LLC converter is tuned to its resonant frequency f_0, i.e. $F_\mathrm{n} = 1$, c.f. Fig. 5.3. At this point the output characteristic is independent on the resonant circuit elements values L_s, C_s and L_p and the behavior of the current and voltage waveforms can be analytically expressed if resistive damping is neglected. The normalized expression are identical for both normalization bases $\{I,Q\}$ since for $F_\mathrm{n} = 1$ the relation $V_\mathrm{g} = nV_\mathrm{o}$ must be true in case of steady-state operation.

$$i_\mathrm{r}(t) = i_\mathrm{r,pk}\sin(\omega_0 t + \varphi) \qquad j_\mathrm{r}(t) = j_\mathrm{r,pk}\sin(\theta + \varphi) \tag{5.3}$$

$$v_\mathrm{Cs}(t) = -v_\mathrm{Cs,pk}\cos(\omega_0 t + \varphi) \qquad m_\mathrm{Cs}(t) = m_\mathrm{Cs,pk}\cos(\theta + \varphi) \tag{5.4}$$

$$v_\mathrm{Cs,pk} = Z_0\, i_\mathrm{r,pk} \qquad m_\mathrm{Cs,pk} = j_\mathrm{r,pk} \tag{5.5}$$

$$i_\mathrm{p}(t) = \frac{nV_\mathrm{o}}{L_\mathrm{p}}\left(t - \frac{T_0}{4}\right) = \frac{nV_\mathrm{o}}{L_\mathrm{p}}t - i_\mathrm{p,pk} \qquad j_\mathrm{p}(\theta) = \frac{1}{h}\left(\theta - \frac{\pi}{2}\right) = \frac{1}{h}\theta - j_\mathrm{p,pk} \tag{5.6}$$

The phase angle φ can be derived by integrating the output current and solving for φ:

$$\frac{I_\mathrm{o}}{n} = \int_0^{\frac{T_\mathrm{s}}{2}} (i_\mathrm{r}(t) - i_\mathrm{p}(t))dt \quad \rightarrow \quad \varphi = \arctan\left[\frac{1}{\omega_0}\frac{nV_\mathrm{o}}{L_\mathrm{p}}\frac{n}{I_\mathrm{o}}\right] \tag{5.7}$$

By utilizing the relationship $\sin(\varphi) = i_\mathrm{p,pk}/i_\mathrm{r,pk}$ the RMS value of the resonant current can be derived to

$$I_\mathrm{r,RMS} = \frac{1}{\sqrt{2}}\sqrt{\left(\frac{\pi}{2}\frac{I_\mathrm{o}}{n}\right)^2 + {i_\mathrm{p,pk}}^2}\,, \tag{5.8}$$

and in the normalized form to

$$J_\mathrm{r,RMS} = \frac{1}{\sqrt{2}}\sqrt{\left(\frac{\pi}{2}J_\mathrm{o}\right)^2 + {j_\mathrm{p,pk}}^2} = \frac{1}{\sqrt{2}}\sqrt{\left(\frac{\pi}{2}J_\mathrm{o}\right)^2 + \left(\frac{\pi}{2}\frac{1}{h}\right)^2} = \frac{\pi}{2\sqrt{2}}\sqrt{J_\mathrm{o}^2 + \left(\frac{1}{h}\right)^2}\,. \tag{5.9}$$

At $F_\mathrm{n} = 1$ the constraints (5.2) and (3.46) can be treated analytically and independent of the DC-DC gain M. The resonant capacitor voltage maximum $\hat{v}_\mathrm{Cs}$ is adjusted by Z_0 and the resonant current at switching instant $i_\mathrm{r,0}$ by L_p. The choice of Z_0 determines the amount of energy that is stored in the resonant circuit because $\hat{\imath}_\mathrm{r}$ is independent of Z_0 and

$$\hat{w}_\mathrm{Ls} = \hat{w}_\mathrm{Cs} = \frac{1}{2}L_\mathrm{s}\hat{\imath}_\mathrm{r}^2 = \frac{Z_0}{4\pi f_0}\hat{\imath}_\mathrm{r}^2\,. \tag{5.10}$$

From an efficiency point of view it would be optimal to choose Z_0 close to zero if just the resonant point $F_n = 1$ would be considered. The choice of L_p influences the reactive power flow, expressed by the RMS value of the resonant current acc. to (5.6) and (5.8) and therefore should be maximized considering efficiency. The maximal value of L_p is constrained by the ZVS condition (3.46) and hence (3.46) yields the optimal L_p value subject to the lowest RMS value of the resonant current.

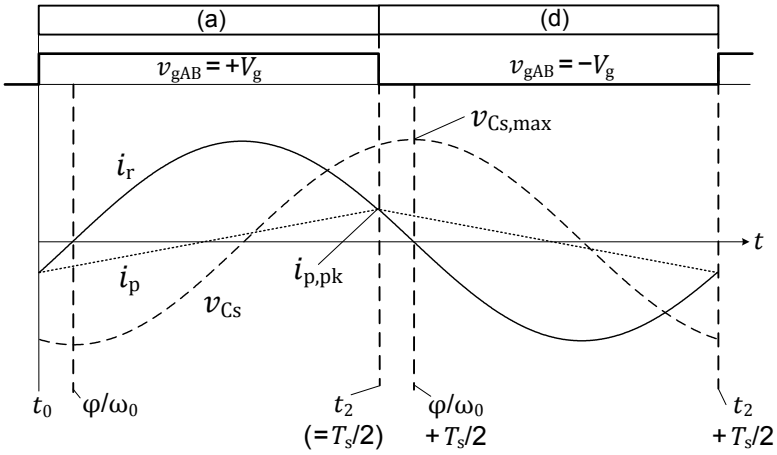

Fig. 5.3: LLC converter waveforms at $F_n = 1$

(5.1) and (5.2) are basic design trade-offs of the LLC converter, that must be minimum fulfilled since the preferred operating range of the LLC converter is the resonant point. Further tightening of these trade-offs and additional trade-offs result from the whole specified operating region. The DC-DC gain behavior of the LLC converter not at the resonant point can be qualitatively described as follows: The higher the difference between the actual switching frequency and the resonant point, i.e. the more detuned the resonant circuit is, the more dependency of the DC-DC gain characteristic on the resonant circuit parameters results (c.f. Fig. 4.1). Because the boundaries of the operating region are typically far below and far above the resonant point, the choice of Z_0 and L_p resp. h is as well limited by the design constraints. Furthermore the basic design trade-offs (5.1) and (5.2) need to be examined at additional operating points. In consequence the multiple factors influencing the choice of Z_0 and h results in a multitude of design trade-offs.

The primary design goal of the LLC converter is to comply with the design constraints, i.e. to enable working properly in the specified operating range. This goal already limits the feasible range of the design parameters. Hence, the final design variant must be chosen from the valid design variants according to the specification. The latter choice in fact is the degree of freedom that allows for a design optimization with respect to an objective variable, which in this work is the conversion efficiency η. The optimization of η implies that the sum of losses is minimized according to (3.47). The single loss contributions thereby exhibit different dependencies, including dependencies on the design parameters. The sum of losses therefore is a mix-up of different dependencies. Hence, a complete analysis of the resulting design trade-offs regarding η is very detailed. By using a numerical optimization solver this detailed analysis can be skipped, what is proposed in this work for the real design optimization and presented in Chapter 5.4. However, some basic insight to the included design trade-offs can be gained by fractional analysis of (3.47). Such analysis is supported by the fact that the model-

ing and parameterization of conversion losses is of high effort. It is therefore helpful to know about the sensitivity of a particular loss mechanism on the optimization result, such that the required model accuracy and parameterizing effort of a loss mechanism can be estimated.

A central loss quantity are the conduction losses on the primary side of the LLC converter. Those have been investigated in [Froehleke], [Froehleke2] for the Series, Parallel and Series-Parallel resonant converter for supporting the rating and selection between the converter types. Assuming that the conduction losses can be calculated by the RMS value of the resonant current, the normalized power loss in case of the LLC resonant converter is given by

$$\frac{P_\mathrm{v}}{P_\mathrm{o}} = \frac{R(f_\mathrm{s})(I_\mathrm{r,RMS}^2 + I_\mathrm{o,RMS}^2)}{P_\mathrm{o}} = d(f_\mathrm{s})\frac{V_\mathrm{Base}}{V_\mathrm{o}}\left(\frac{J_\mathrm{r,RMS}^2 + J_\mathrm{o,RMS}^2}{J_\mathrm{o}}\right). \tag{5.11}$$

The contribution of $J_\mathrm{r,RMS}^2$ in (5.11) can be shown to be distinctively dependent on the design parameter h, which is already indicated by (5.9). The dependency throughout the whole operating range is shown by Fig. 5.4. It becomes clear that the minimization of conduction losses by maximizing h is valid throughout the whole operating range of the LLC converter. But it needs to be pointed out that this evidence assumes that J_o is constant; hence it is only true if maximizing h correlates with maximizing L_p.

Furthermore the conduction losses according to (5.11) are dependent on the operating region. The trend of $J_\mathrm{r,RMS}$ shown in Fig. 5.5 demonstrates that the below resonance region is unfavorable regarding conduction losses. It is furthermore remarkable that in the above resonance region the dependency of $J_\mathrm{r,RMS}$ on F_n is very small compared to the below resonance region. Furthermore shown by Fig. 5.5 is the dependency of $J_\mathrm{r,RMS}$ on the characteristic impedance Z_0. Because of $(J_\mathrm{o} \sim Z_0)|_{I_\mathrm{o}}$, it can be observed that the trend over F_n of $J_\mathrm{r,RMS}$ is little dependent on Z_0.

Many design methodologies in literature rely on minimizing the conduction losses according to (5.11) and the above analysis ([Fang], [Pawellek], [Oeder5], [Fu2], [Ivensky], [Lu], [Jung], [Zhang], [Adragna]). A comprehensive design optimization of course needs to consider all loss contributions. It also needs to consider, what will be shown below, the frequency dependency of the loss contributors.

Although in general the LLC design parameters are interdependent, some single qualitative design trade-offs can be formulated in dependence on the circuit level design parameters Z_0, h and f_0. In the following it is always assumed that $(J_\mathrm{o} \sim Z_0)|_{I_\mathrm{o}}$. The first consideration regards the degree of freedom in choosing the inductance ratio h: Maximizing h on the one hand minimizes $I_\mathrm{r,RMS}$, but on the other hand lowers the peak gain $M_\mathrm{pg} = M\left(F_\mathrm{n,pg}\right)|_{J_\mathrm{o}}$ and increases the minimal gain $M_\mathrm{mg}(F_\mathrm{n}) = M(F_\mathrm{n})|_{1<F_\mathrm{n}<F_\mathrm{n,zg},J_\mathrm{o}}$, which is shown by Fig. 5.6. Hence it can be concluded that $I_\mathrm{r,RMS}$ is minimized subject to the design constraints, if the maximal gain of the design variant exactly fits the maximum required gain $M_\mathrm{pg}|_{J_\mathrm{o}} = M_\mathrm{max}|_{J_\mathrm{o}}$.

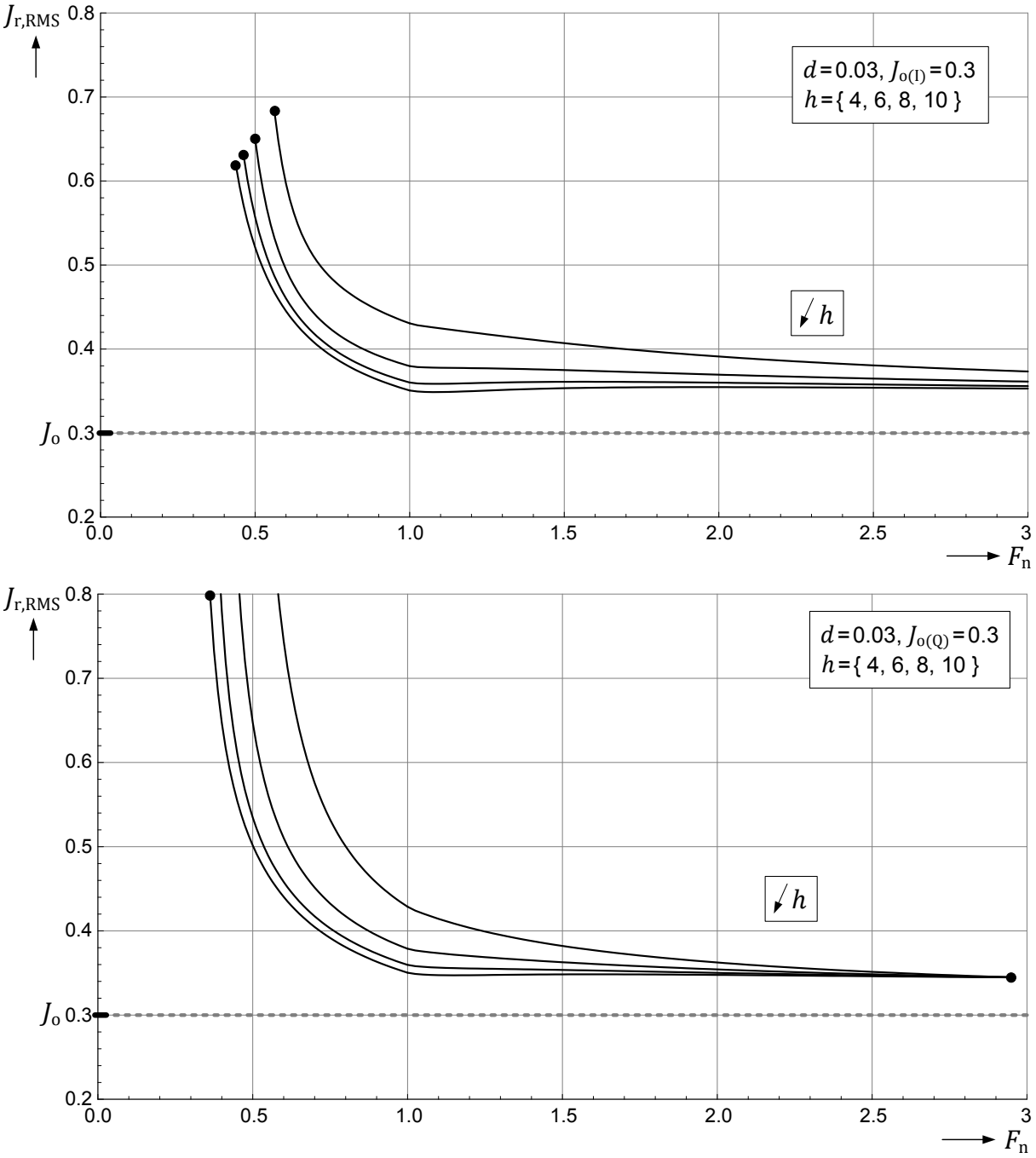

Fig. 5.4: Normalized DC-DC gain diagrams for different normalization bases {I,Q} and in dependence on parameter h; dots mark the boundaries to another operating mode except at $F_n = 1$.

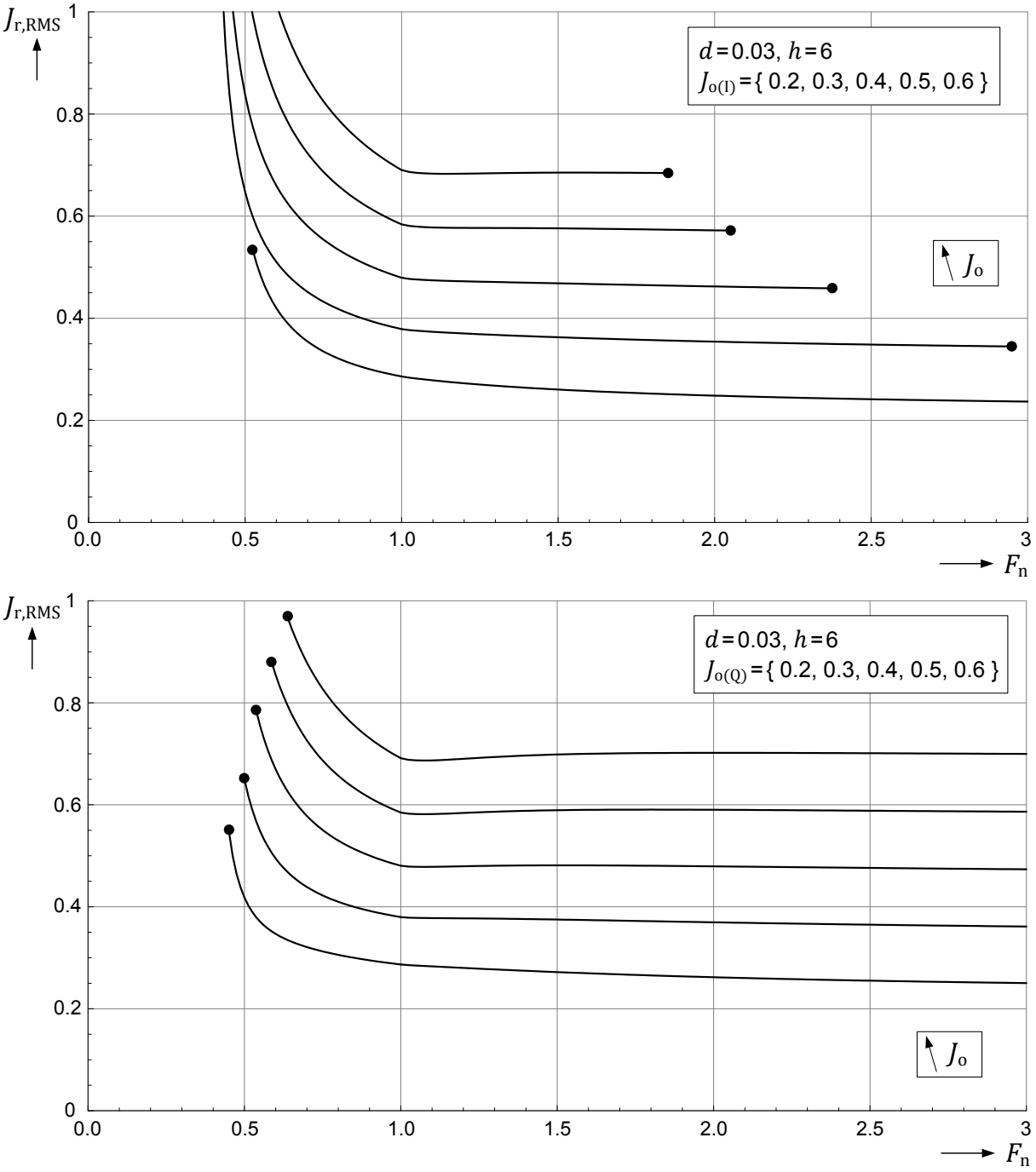

Fig. 5.5: Normalized DC-DC gain diagrams for different normalization bases {I,Q} and in dependence on parameter J_o; dots mark the boundaries to another operating mode except at $F_n = 1$.

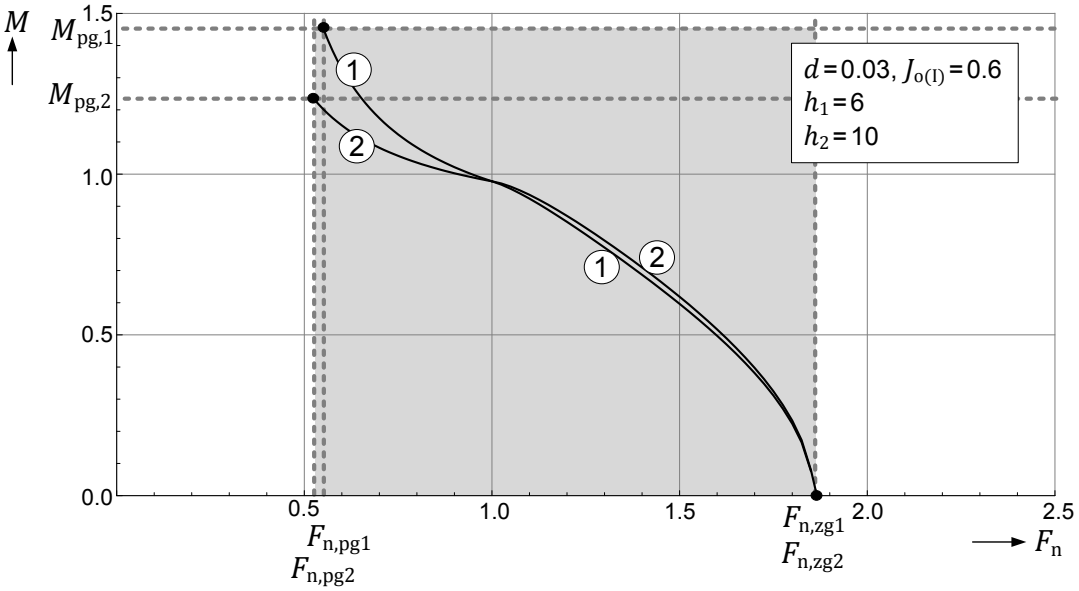

Fig. 5.6: DC-DC gain diagram in dependence on parameter h

The second consideration regards the degree of freedom in choosing the characteristic impedance of the resonant circuit: Reducing the characteristic impedance increases the maximal gain of the design variant, but decreases at the same time the lowest switching frequency $F_{n,pg}$ and increases the highest switching frequency $F_{n,zg}$, which is shown by Fig. 5.7. Furthermore it increases the no load gain M_{zl} and the burst load threshold $J_{o,burst\_max}$. In conclusion Z_0 and the switching frequency range $F_{n,zg} - F_{n,pg}$ are a matter of fundamental design trade-off. Solving the both described design trade-offs is described by [Fang] and called Peak Gain Placement. [Fang] finds that the Peak Gain Placement cannot be solved analytically. He therefore generated an approximate solution of a transcendental equation that shows good accuracy for low values of h but limited accuracy for high values of h. However, by using a numerical optimization solver like proposed in this work, such approximate solutions can be omitted.

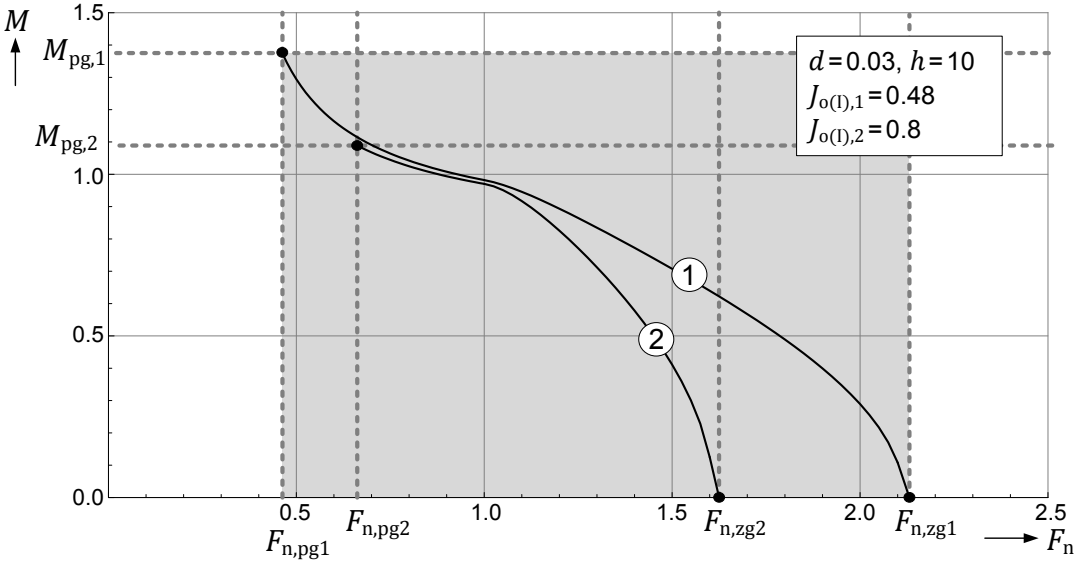

Fig. 5.7: DC-DC gain diagram in dependence on parameter Z_0, which is proportional to $J_{o(I)}$

The Peak Gain Placement method can be generalized regarding the switching frequency level. This is implied by the fact that it can be illustrated in a DC-DC gain diagram with the *x*-axis normalized to the resonance frequency f_0 (c.f. Fig. 5.6 and Fig. 5.7). But for a concrete converter design also the overall switching frequency level, closely related to the value of f_0, has to be chosen. Provided that the switching frequency limits are given as normalized quantities $F_{\mathrm{n,pg}}$ and $F_{\mathrm{n,zg}}$, the design steps Peak Gain Placement and choice of f_0 could be independently performed. In such case the Peak Gain Placement yields an optimal design regarding the minimization of $I_{\mathrm{r,RMS}}$, Z_0 and $\hat{\imath}_{\mathrm{p}}$ and because of (5.10) and $\widehat{w}_{\mathrm{Lp}} = 0.5\, L_{\mathrm{p}} \hat{\imath}_{\mathrm{p}}^2$ also the minimization of the stored energy in the magnetic components. It is therefore close to an optimal design regarding efficiency and power density.

An additional aspect that should be pointed out in this work is the design case, in which the switching frequency limits might be given as absolute quantities $f_{\mathrm{s,min}}$ and $f_{\mathrm{s,max}}$, especially with the lower switching frequency limit set by the audible noise boundary, or set by an output ripple requirement. In such case, the Peak Gain Placement and the choice of switching frequency level become coupled to each other. This circumstance is illustrated in Fig. 5.8. The x-axis is shown denormalized, and the switching frequency limits are given as absolute quantities. It can be seen that for the same peak gain and the same minimum switching frequency, now the Peak Gain Placement generates results with different resonance frequencies, in this example $f_{0,1}$ and $f_{0,2}$. And since the vicinity of the resonance frequency is the preferred operating region of the converter, the different design variants result in different operating frequencies.

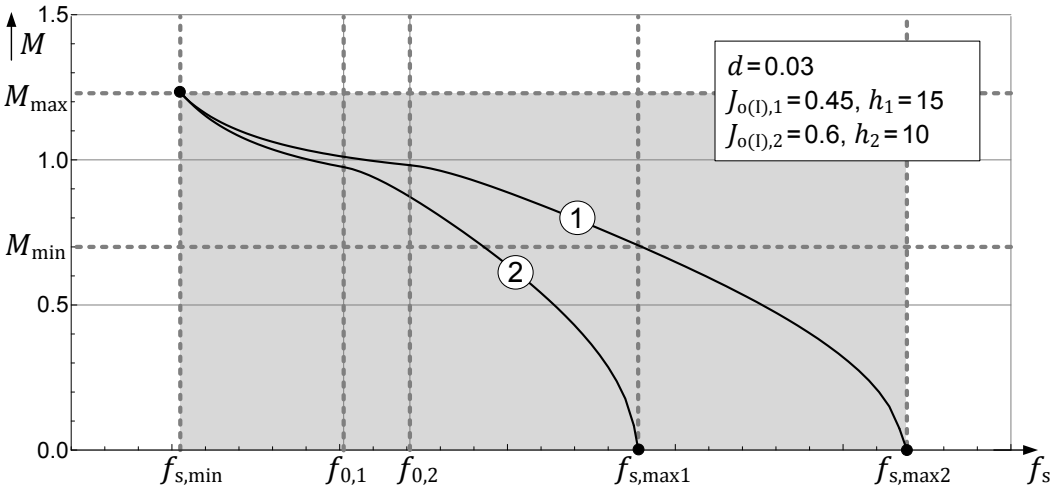

Fig. 5.8: Two different design variants with identical peak gain but different resonant frequencies $f_{0,1}$ and $f_{0,2}$

The choice of the optimal design variant (here: $f_{0,1}$ or $f_{0,2}$) now additionally depends on the frequency characteristic of the losses (c.f. (3.47)). A sensitivity of the losses with respect to the switching frequency and current can be defined by

$$S_{\mathrm{v},f_{\mathrm{s}}} = \frac{\partial P_{\mathrm{v}}}{\partial f_{\mathrm{s}}} \qquad \text{and} \qquad S_{\mathrm{v,iRMS}} = \frac{\partial P_{\mathrm{v}}}{\partial I_{\mathrm{RMS}}}$$

The optimal design variant depends on the share between all losses with $S_{\mathrm{v},f_{\mathrm{s}}} \neq 0$ and all losses with $S_{\mathrm{v,iRMS}} \neq 0$, as well as on the sensitivities $S_{\mathrm{v},f_{\mathrm{s}}}$ and $S_{\mathrm{v,iRMS}}$ themselves. The importance of a loss type within the optimization process can be described by the product $P_{\mathrm{v}} \cdot S_{\mathrm{v}}$. Table

5.1 summarizes qualitatively the normalized sensitivities S_v/P_v for several loss types on an estimation basis. The numerical optimization solver proposed in this work is able to find the optimal design variant subject to the described complex of problems without the need of a detailed analysis of the loss types and their characteristics.

Table 5.1: Qualitative sensitivities of single loss mechanisms

Component	*Loss mechanism*	*Switching frequency related normalized sensitivity* $S_{v,f_s}/P_v$	*Current related normalized sensitivity* $S_{v,iRMS}/P_v$
Bridge MOSFETs	Conduction losses	Low	High ($P_v \sim I_{RMS}^2$)
	C_{oss} energy dissipation	Low (ZVS)	n/a
	C_{oss} recharge losses	High ($P_v \sim f_s$)	Medium (Function of speed of recharge)
	Gate charge losses	High ($P_v \sim f_s$)	n/a
	Transconductance modulation	High ($P_v \sim f_s$)	Medium (Soft turn-off due to C_{oss})
Resonant choke (L_s)	Resistive losses	High (Skin/Proximity effect)	High ($P_v \sim I_{RMS}^2$)
	Hysteresis losses	High ($P_v \sim f_s^{\alpha}$)	High ($P_v \sim I_{RMS}^{\beta}\big\vert_{waveform}$)
Resonant capacitor (C_s)	Resistive/Dielectric losses	Medium (Skin effect)	High ($P_v \sim I_{RMS}^2$ for resistive losses)
XFMR (T_1)	Resistive losses	High (Skin/Proximity effect)	High ($P_v \sim I_{RMS}^2$)
	Hysteresis losses	High ($P_v \sim f_s^{\alpha}$)	High ($P_v \sim I_{RMS}^{\beta}\big\vert_{waveform}$)
Rectifier MOSFETs	Conduction losses	Low	High ($P_v \sim I_{RMS}^2$)
	C_{oss} energy dissipation	Low(ZVS)	n/a
	C_{oss} recharge	High ($P_v \sim f_s$)	Medium (Function of speed of recharge)
	Gate charge	High ($P_v \sim f_s$)	n/a
	Transconductance modulation	Low (ZCS)	Low (ZCS)
PCB	Resistive losses	Medium (Skin effect)	High ($P_v \sim I_{RMS}^2$)

5.3.3 Exemplary Optimization Process

As described in Chapter 5.3.2 the numerical converter design optimization is especially feasible if the resonance frequency f_0 is an additional design parameter besides h and Z_0 and at the same time the minimum switching frequency is given as an absolute value. In this case, the peak gain placement design becomes a trade-off between losses that are sensitive to current and losses that are sensitive to switching frequency. A prominent example for a single trade-off is the losses of the magnetic components. Provided that the core volumes and cross sec-

tions are constant, a higher switching frequency reduces the core losses according to (3.49) but increases the conduction losses according to (3.60).

In order to demonstrate the characteristics of those trade-offs with respect to the conversion efficiency of the LLC converter, the numerical design optimization of an exemplary and simplified design case is performed. The simplified design case includes the following assumptions:

- All components are ideal
- All losses are represented by a single lumped resistance $R_{\mathrm{s,p}}$ of the resonant circuit and by an overall sum of switching loss energy $W_{\mathrm{v,sw}}$
- $R_{\mathrm{s,p}}$ and $W_{\mathrm{v,sw}}$ are constant throughout design variants and operating conditions

The design optimization is repeated for different switching loss energies $W_{\mathrm{v,sw}}$. This is controlled by the factor k_{sw} , so that overall losses are given by

$$P_{\mathrm{v}}(f_{\mathrm{s}}, k_{\mathrm{sw}}) = R_{\mathrm{s,p}} \cdot I_{\mathrm{r,RMS}}^2 + W_{\mathrm{v,sw}} \cdot f_{\mathrm{s}} \cdot k_{\mathrm{sw}} \tag{5.12}$$

By varying k_{sw} , now the influence of a different mix-up of loss types on the optimal converter design can be studied. For a real converter the mix-up of loss types depend on the used circuit components and hence for different components different optimal design variants might result.

For programming the optimization solver the treatment of constraints is an important aspect. Fig. 5.9 shows a flow chart of the implemented optimization algorithm. The algorithm comprises a system of penalties added to the objective function result in case of dissatisfying constraints. The penalty system needs to distinguish two cases:

1. The numerical steady-state solver does not converge, which indicates that the LLC converter exhibits no steady-state solution for the actual parameter set. In this case the actual run is aborted and a low η is reported. The optimization solver proceeds with the next run.
2. A user given constraint is violated. In this case a penalty is calculated that is proportional to the extent of constraint violation. The penalties of one run are summed up and applied to the final result of the objective variable η.

The penalty gain k_{plt} is selected carefully: On the one hand it needs to be high enough to safely exclude non feasible solutions. On the other hand the penalized output should be in a similar scale as the feasible solution area, since badly scaled objective function values reduce the computational efficiency of the GM algorithm by generating a higher number of daughter nodes.

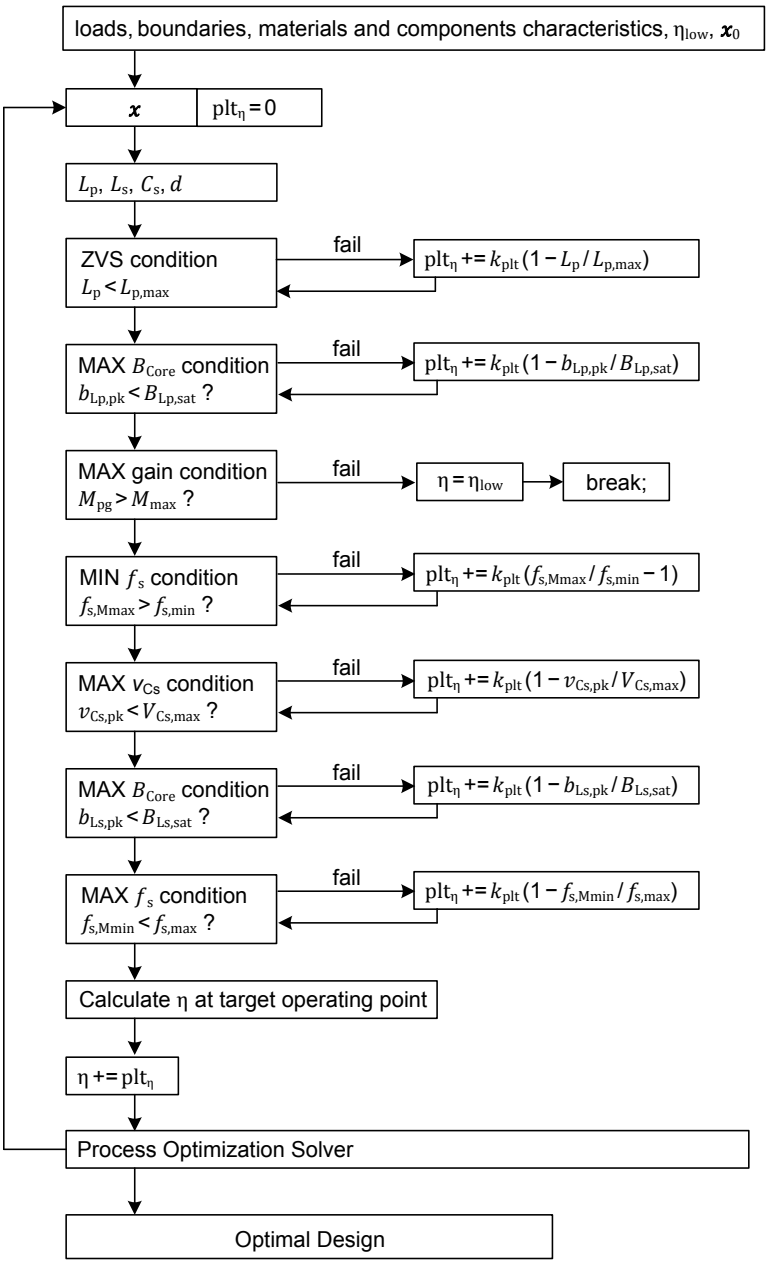

Fig. 5.9: Structure of the optimization process including the system of penalties

For the simplified design case the design parameters and constraints are chosen to be in a typical order of a 3 kW, 54.5 V output power supply and summarized in Table 5.2. The constraint of maximum flux density is skipped in this example since the magnetic components are assumed to be ideal in this simplified design case. The ZVS condition (3.46) is substituted by the simplified condition

$$i_{r,ZVS\_min} \leq nV_o/(4f_sL_p) \approx i_r(t_{sw})|_{(V_o=V_{o,nom})\ \&\ (0.2\ I_{o,nom}<I_o<I_{o,nom})} \tag{5.13}$$

The elements in the parameter search vector $\boldsymbol{x}$ are $\{h, Z_0, f_0\}$.

Table 5.2: Design specification used for the exemplary design optimization

$V_{\mathrm{i,nom}}$	410 V
$V_{\mathrm{i,min}}$	300 V
$V_{\mathrm{o,nom}}$	54.5 V
$P_{\mathrm{o,nom}}$	3000 W
$P_{\mathrm{o,opt}}$	60% $P_{\mathrm{o,nom}}$

$v_{\mathrm{Cs,max}}$	500 V
$f_{\mathrm{s,min}}$	40 kHz
$f_{\mathrm{s,max}}$	300 kHz
$i_{\mathrm{r,ZVS\_min}}$	2 A
$R_{\mathrm{s,p}}$	0.3 Ω
$W_{\mathrm{v,sw}}$	200 µJ

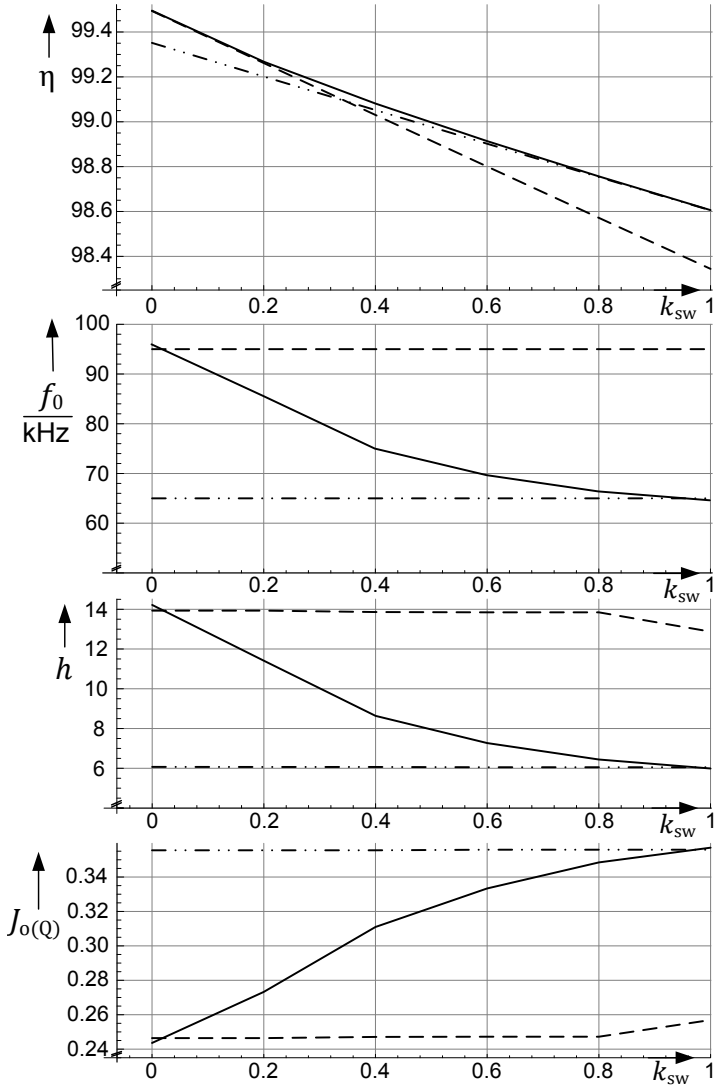

Fig. 5.10: Optimized efficiency η and concordant design parameters f_0, h and nominal load $J_{\mathrm{o(Q)}}$ for different values of k_{sw}; Dashed lines: Results for predefined f_0 value; Graphs are interpolated from k_{sw} = {0, 0.2, 0.4, 0.6, 0.8, 1}.

The result of the optimization process with k_{sw} sweeping from 0 to 1 is shown in Fig. 5.10. The solid line represents the optimization in dependence on the design parameters h, Z_0 (resp. J_{o}) and f_0. For the dashed lines the dependency is reduced on h and Z_0, whereas f_0 is fixed to a certain value. The characteristic of the solid curve is in accordance to the theory: The higher

the portion of losses that are sensitive to switching frequency, the lower the optimal resonant frequency f_0 and vice versa. In case of a fixed resonant frequency f_0, the difference between the dashed lines and the solid line gives the potential efficiency increase by optimal selection of f_0. The maximal potential efficiency increase in the shown design case is appr. 0.4% at $\{f_0 = 95\ \text{kHz}, k_{\text{sw}} = 1\}$. For a real converter the sensitivity of the efficiency on the selection of the resonant frequency f_0 depends on the loss characteristic of the real components and hence on the selection of the components itself. It is therefore feasible to apply the optimization procedure on every new converter design in order to guarantee the best possible efficiency with the selected components. A design optimization example of a real converter design is demonstrated in Chapter 5.4.

5.4 Design Optimization Example Based on Measurements

In this chapter the numerical optimization solver is tested with the parameters of a real converter circuit as an example. The principal schematic of the demonstrator circuit is shown in Fig. 5.11. For over-load protection of the resonant circuit, C_s is clamped by z-diodes ZD_1 and ZD_2 to the DC-link voltage V_i (c.f. Chapter 4.3). The z-diode voltage dictates the value for $v_{\text{Cs,max}}$ according to

$$V_{\text{Cs,max}} < V_{\text{i,min}} + 2V_{\text{ZD}} \tag{5.14}$$

Equation (5.14) typically needs to be evaluated in the hold-up condition, because V_i is minimal and v_{Cs} maximal due to the lower switching frequency. This is as well true for the contemplated optimization case.

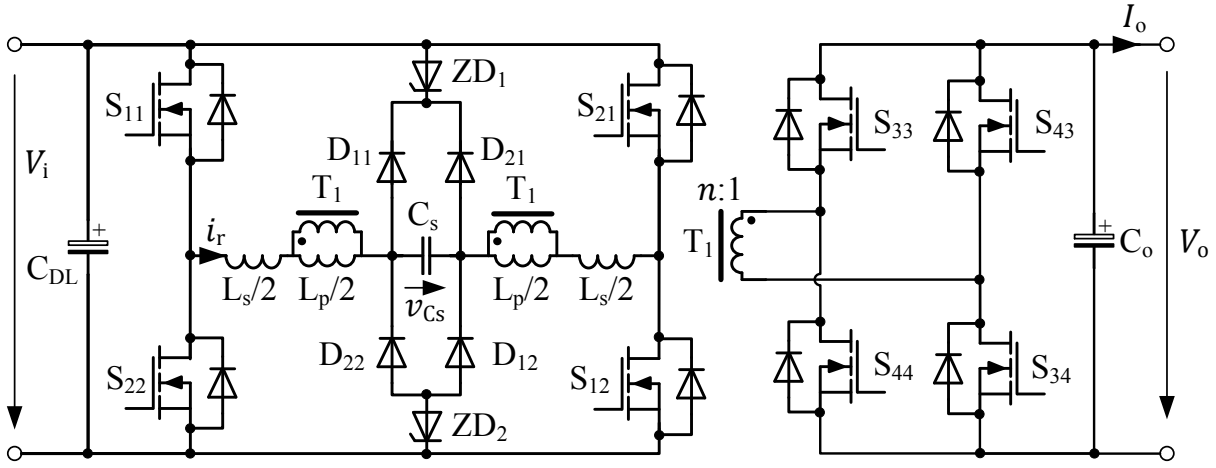

Fig. 5.11: Principal schematic of the example converter used for demonstrating the design optimization methodology

A very critical point when comparing a theoretical loss model with the measured losses of a real converter is the influence of the component temperatures. Unless the temperatures of every single component are determined during the efficiency measurements, the comparison has limited accuracy just by uncertain temperatures. Also the results of the design optimization may vary in dependence on the assumed cooling conditions and heat distribution. Because the author had no ability to monitor the single component temperatures and no thermal model is applied, the component temperatures are assumed for the sake of simplification of the design optimization. The assumed component temperatures are derived by experience and given in

Table 5.3 together with a description of all converter components and their relevant parasitic parameters. The non-linear output capacitances of the bridge MOSFETs are simplified according to their datasheet to $C_{\mathrm{oss(er)}}$: energy related equivalent capacitance and: time related equivalent capacitance. The core saturation limits $B_{\mathrm{L,sat}}$ are derived from worst-case temperature considerations, since the saturation boundary of the used core material decreases with increasing temperature.

Table 5.3: Circuit element data of the example converter

Component	Type	Characteristic values
Bridge-MOSFETs S_{11}, S_{22}, S_{21}, S_{12}	IPW60R070C6	$C_{\mathrm{oss(er)}} = 140$ pF $C_{\mathrm{oss(tr)}} = 710$ pF $Q_{\mathrm{g}} = 170$ nC $T_{\mathrm{j}} = 70$ °C → $R_{\mathrm{DS(on),Tj}} = 100$ mΩ
Rectifier-MOSFETs S_{33}, S_{44}, S_{43}, S_{34} (6x in parallel)	BSC036NE7	$C_{\mathrm{oss}} = 990$ pF $Q_{\mathrm{g}} = 65$ nC $T_{\mathrm{j}} = 80$ °C → $R_{\mathrm{DS(on),Tj}} = 3.7$ mΩ
Z-diodes ZD_1, ZD_2	2x 5.0SMDJ24A	$V_{\mathrm{ZD}} \approx 80$ V
Resonant choke L_s	PQ 45/30, core material: DMR95, winding: litz	$T_{\mathrm{w}} = 50$ °C, $T_{\mathrm{c}} = 60$ °C, $B_{\mathrm{Ls,sat}} = 320$ mT, $N_{\mathrm{ch,0}} = 15$, $l_{\mathrm{g,0}} = 2.1$ mm
XFMR T_1	UU <*xx*>/32/24, core material: DMR95, windings: litz and foil, <*xx*> = $b_{\mathrm{w}} + 20$ mm	$T_{\mathrm{w}} = 60$ °C, $T_{\mathrm{c}} = 70$ °C, $n = 7.4$, $B_{\mathrm{Lp,sat}} = 350$ mT, $N_{\mathrm{p,0}} = 37$, $l_{\mathrm{g,0}} = 0.65$ mm
Resonant Capacitor	C0G-type MLCCs	$V_{\mathrm{max}} = 630$ V

According to the loss modeling approach of the magnetic components (c.f. Chapter 3.2.3) the core geometries are considered to be defined prior to the optimization run and hence fixed parameters. A special case is given by the used double U-core XFMR that is shown in Fig. 5.12. For this XFMR all core geometry parameters are fixed except the winding window with b_{w}. As derived in Chapter 3.2.3.4 the variation of b_{w} can be feasibly considered in the copper loss model by the proportionality $R_{\mathrm{AC}} \sim 1/b_{\mathrm{w}}$. This degree of freedom in the core geometry allows for an additional and obvious trade-off between the core losses and the copper losses of the transformer.

As stated in Chapter 3.2.3.4 the proposed loss modeling approach of the magnetic components is not valid if the number of turns is varied in case of foil windings. Furthermore in the contemplated example the number of turns of the secondary foil windings $N_{\mathrm{s}} = N_{\mathrm{p,0}}/n = 5$ could be varied at the real component by only discrete numbers, which results in a variation of ±20% for the next possible number of secondary turns. In consequence the validity of the loss modeling approach is only fulfilled if the number of secondary turns is constant. However, for the following design optimization example the number of turns of the primary winding as well as of the secondary winding is considered as a free varying rational number, where the above mentioned limitations are neglected. Also this practice yields results which are not in precise concordance with the underlying physical models, this was chosen in order to be able to monitor the principal course of direction of the optimization solver for the number of turns

values. The hereby observed reduced evidence in form of the direction information is still correct despite the model simplifications, since the monotonic dependence between number of turns and the resulting R_{AC} resistance is still valid. The predictions of the optimization solver for the number of turns of the foil winding are to be considered as more qualitatively, the more the predicted number deviates from the original value. A further constraint given by the proposed loss modeling approach is that the turns ratio n cannot be varied, because the dependency on n is not supported by the modeling approach and its related measurement technique (c.f. Chapter 3.2.3.4).

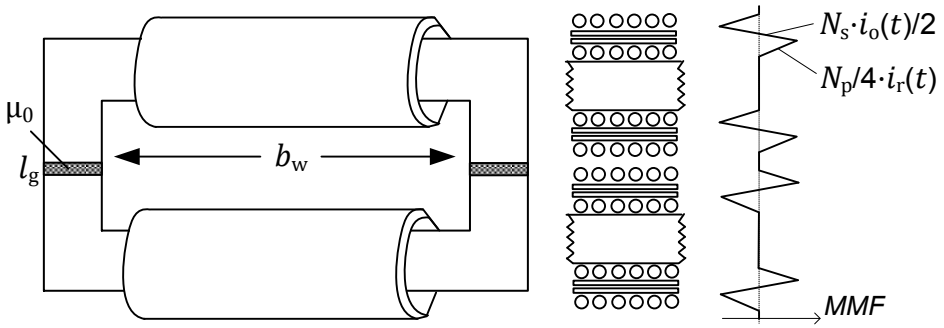

Fig. 5.12: Layout and winding layer construction of the XFMR used in the example converter. The winding width b_w is considered as a free varying design parameter. MMF: Magneto Motive Force

The parametrization of the copper loss model of the magnetic components acc. to Chapter 3.2.3 is done by measuring the frequency dependent resistances at room temperature. The measured R_{AC} characteristics $R_{AC\_ch}(f)$, $R_{AC\_xf\_p}(f)$, $R_{AC\_m\_p}(f)$ and the applied polynomial fittings are given in appendix 9.2.2. The Steinmetz parameters acc. to (3.49) for calculating the core losses are extracted from the core material datasheet [DMEGC], at which a curve fitting procedure is applied on the given loss characteristic graph in order to generate a functional description between the core power loss density, excitation frequency, core temperature and core peak flux density. The result of the curve fitting is given in appdendix 9.2.1 and the according Steinmetz parameters are shown in Table 5.4.

Table 5.4: Steinmetz parameters of DMR95 core material originating its datasheet; $k_T(\hat{B})$: temperature fitting function (c.f. appdendix 9.2.1)

Component	V_c / cm^3	k/V_c / (mW/cm^3)	α	β
Resonant choke L_s	26.59	$60.31 \cdot 10^{-6} \cdot k_T(\hat{B})$	1.7	2.54
XFMR T_1	71.74	$60.31 \cdot 10^{-6} \cdot k_T(\hat{B})$	1.7	2.54

The complete list of the considered loss contributions within the optimization process is given in Table 5.5. Not included are losses occurring in the input and output filters as well as losses occurring on the PCB copper tracks and in the resonant capacitor C_s (c.f. Chapter 3.2.1).

The design optimization example is subject to input and output parameters and constraints which are given in Table 5.6. The example converter is considered to be a server or telecom PSU with a certain input and output voltage range according to the descriptions of Chapter 2.1.2. The main operation of the converter is at its nominal output voltage $V_{o,nom}$ and hence used for the efficiency calculation. The output power for the efficiency calculation is chosen

to be 60% of the nominal load. This is based on the assumption of a 2+1 redundant overlaying system approach and some additional overhead (c.f. Chapter 2.1.1).

Table 5.5: Considered loss types and respective loss formulas within the optimization process

Loss type	Nomenclature	Formula
Bridge conduction losses	$P_{\mathrm{v,br\_cond}}$	$4(\,R_{\mathrm{DS(on)},T_\mathrm{j}}\,I^2_{\mathrm{r,RMS}}/2)$
Bridge switching losses	$P_{\mathrm{v,br\_sw}}$	$4(\,20\%\frac{1}{2}C_{\mathrm{oss}}V_\mathrm{i}{}^2 f_\mathrm{s})$
Bridge driving losses	$P_{\mathrm{v,br\_dr}}$	$4(Q_\mathrm{g}\,(10\,\mathrm{V})f_\mathrm{s})$
Rectifier conduction losses	$P_{\mathrm{v,rec\_cond}}$	$4\,(\frac{R_{\mathrm{DS(on)},T_\mathrm{j}}}{6}I^2_{\mathrm{o,RMS}}/2)$
Rectifier switching losses	$P_{\mathrm{v,rec\_sw}}$	neglected
Rectifier driving losses	$P_{\mathrm{v,rec\_}dr}$	$4(6\,Q_\mathrm{g}\,(10\,\mathrm{V})f_\mathrm{s})$
Choke copper losses	$P_{\mathrm{v,ch\_cu}}$	$R_{\mathrm{AC\_ch}}(f_\mathrm{s},N_\mathrm{ch},T_\mathrm{w})I^2_\mathrm{r}$
Choke core losses	$P_{\mathrm{v,ch\_core}}$	acc. (3.50) & Table 5.4
Xfmr copper loss by output current	$P_{\mathrm{v,xf\_cu}}$	$R_{\mathrm{AC\_xf\_p}}(f_\mathrm{s},N_\mathrm{p},T_\mathrm{w})I^2_\mathrm{o}$
Xfmr copper loss by magnetizing current	$P_{\mathrm{v,xf\_m\_cu}}$	$R_{\mathrm{AC\_m\_p}}(f_\mathrm{s},N_\mathrm{p},T_\mathrm{w})I^2_\mathrm{p}$
Xfmr core loss	$P_{\mathrm{v,xf\_core}}$	acc. (3.50) & Table 5.4

The resonant frequency f_0 is a free varying design parameter. It will be evaluated in the given range. The switching frequency boundaries are treated with special attention, since they constitute an important parameter for the feasibility of the presented optimization approach. The upper boundary is defined relative to the resonant frequency f_0. This effects that the short-circuit and over-load behavior of different design variants is comparable in terms of dynamic controllability, because the relative switching frequency increase that is performed by the output controller in case of a short-circuit or over-load is equal (c.f. Chapter 4.3). The lower switching frequency boundary is defined by absolute values, at which different cases can be constructed: $f_{\mathrm{s,min}} = 0\,\mathrm{kHz}$ effects no lower switching frequency boundary. This case is for theoretical evaluation, since commonly the threshold of audibility needs to be topped. Hence, the second case, $f_{\mathrm{s,min}} = 20\,\mathrm{kHz}$, represents the lowest practical boundary. A third case $f_{\mathrm{s,min}} = 40\,\mathrm{kHz}$ is taken as a reference scenario. This is established because a higher $f_{\mathrm{s,min}}$ value also determines a higher optimal operating frequency of the converter and generally limits the input and output filter requirements. These are also important if the overall volume of the power supply shall be small, which is commonly deserved in industry.

The damping resistance $R_{\mathrm{s,p}}$ is approximately chosen and constant for all design variants. A variable part of $R_{\mathrm{s,p}}$ results in fact by the frequency dependent resistance of the magnetic components. But this variation and its influence on the optimization results is assumed to be negligible. The maximal inductance $L_{\mathrm{p,max}}$ and the switching loss energy $W_{\mathrm{v,sw}}$ are given according to Chapter 3.2.

Table 5.6: Parameters and constraints used for the design optimization of the example converter

$V_{\mathrm{i,nom}}$	410 V
$V_{\mathrm{i,min}}$	280 V
$V_{\mathrm{o,nom}}$	54.5 V
$V_{\mathrm{o,min}}$	43 V
$V_{\mathrm{o,max}}$	58 V
$P_{\mathrm{o,nom}}$	3000 W
$P_{\mathrm{o,opt}}$	60% $P_{\mathrm{o,nom}}$

$v_{\mathrm{Cs,max}}$	440 V (c.f. (5.14))
f_0	50 – 120 kHz
$f_{\mathrm{s,min}}$	40 kHz
$f_{\mathrm{s,max}}$	3.5 f_0
$L_{\mathrm{p,max}}$	acc. (3.46)
R_{sp}	0.35 Ω
$W_{\mathrm{v,sw}}$	acc. (3.48)

The optimization solver is configured as shown by Fig. 5.9. The degrees of freedom, i.e. the elements in the parameter search vector $\boldsymbol{x}$, are $\{h,\ Z_0,\ l_{\mathrm{g,ch}},\ l_{\mathrm{g,xf}},\ b_{\mathrm{w}}\}$. f_0 is chosen to have a predefined value which is swept over a certain range to demonstrate the dependence of the optimization result on f_0. Compared to the simplified design case (c.f. Table 5.2), now the air gap values of the resonant choke $l_{\mathrm{g,ch}}$ and the transformer $l_{\mathrm{g,xf}}$ as well as the transformer winding window width b_{w} are additionally considered as searched parameters. The number of turns of both the resonant choke and the transformer result out of $N_{\mathrm{w}} = \sqrt{L/A_{\mathrm{l}}(l_{\mathrm{g}})}$ with A_{l}: air-gap reluctance calculated according to [Undeland]:

$$A_{\mathrm{l}} = \frac{\mu_0}{l_{\mathrm{g}}} \begin{cases} (b_{\mathrm{s}} + l_{\mathrm{g}})(t_{\mathrm{s}} + l_{\mathrm{g}}) & \text{for rectangular core cross section}^{10} \\ \frac{\pi}{4}(b_{\mathrm{s}} + l_{\mathrm{g}})^2 & \text{for round core cross section}^{11} \end{cases} .$$

In order to analyze the optimization process of the LLC converter several optimization runs with different parameter sets (= scenarios) are performed. The list of parameter sets is given in Table 5.7. Scenario (1) is the reference scenario according to Table 5.6. Based on the reference scenario the additional scenarios (2) – (7) differ from the reference scenario by the written values. By this the influence of one particular design constraint can be analyzed. The results of the optimization runs are illustrated in Fig. 5.13 to Fig. 5.17. The parametrization of the optimization solver for the shown results is $n_{\mathrm{igp}} = 8,\ k_{\mathrm{tol}} = 0.01,\ k_{\mathrm{ctr}} = 0.01$. These values have been evaluated by test runs to give a feasible compromise between accuracy, reproducibility and computation time. The computation time of one optimization run is approximately 45 minutes on an intel CORE™i5 CPU with 8 Gb of working memory.
The initial upper and lower boundaries of the search vector are

$$\begin{aligned} \boldsymbol{x} &= \{h,\ Z_0,\ l_{\mathrm{g,ch}},\ l_{\mathrm{g,xf}},\ b_{\mathrm{w}}\} \\ \boldsymbol{x}_{\mathrm{low}} &= \{2.5,\ 3,\ 0.4 \cdot 10^{-3},\ 0.2 \cdot 10^{-3},\ 20 \cdot 10^{-3}\} \\ \boldsymbol{x}_{\mathrm{high}} &= \{25,\ 30,\ 4 \cdot 10^{-3},\ 2 \cdot 10^{-3},\ 200 \cdot 10^{-3}\}. \end{aligned} \tag{5.15}$$

These boundaries define the search region of the optimization solver. Due to the contraction of the step width (c.f. Chapter 5.2) the solver cannot evaluate to points outside the search region. Hence the initial search vector boundaries are at the same time the solution boundaries.

[10] b_{s}: width of core cross sectional area and t_{s}: height of core cross sectional area
[11] d_{s}: diameter of core cross sectional area

Table 5.7: Different parameter sets used for the optimization runs

	$V_{\mathrm{i,min}}$	$f_{\mathrm{s,min}}$	$F_{\mathrm{n,max}}$	$v_{\mathrm{Cs,max}}$	$P_{\mathrm{o,opt\_nom}}$	$b_{\mathrm{w,max}}$
(1)	280 V	40 kHz	3.5	440 V	0.6	20 cm
(2)		20 kHz				
(3)		0 kHz	10			
(4)					1	
(5)				1000 V		
(6)	315 V					
(7)						5.5 cm

The diagrams of Fig. 5.13 and Fig. 5.14 show the key parameter values evaluated by the optimization solver in dependence on the resonant frequency f_0. Relating to the reference scenario (1) an efficiency optimum results at $f_0 = 85$ kHz with $\eta = 99.09\%$. The developed implementation of the optimization solver allows analyzing if and what constraint is impeding a higher efficiency optimization result. Generally zones of constraints impeding the optimization results can be stated. These zones are most clearly expressed by the inductance ratio h due to the following evidence: On the one hand h is a normalized parameter and independent on the concrete switching frequency level. On the other hand the maximization of h results in the lowest RMS current values in the resonant circuit acc. to (5.11) and Fig. 5.4 and hence the maximization of h is one strong force within the optimization evaluation. In Fig. 5.13 all scenarios exhibit a zone $f_0 > 90$ kHz with constant values of h and Z_0. In this zone the optimization result is bordered by the $v_{\mathrm{Cs,max}}$ constraint. The $v_{\mathrm{Cs,max}}$ constraint limits the characteristic impedance Z_0 (c.f. (5.5)) and via h also the value of L_{p}. A second zone $50\,\mathrm{kHz} < f_0 < 90\,\mathrm{kHz}$ exists for scenario (1) with steadily increasing value of h. In this zone the optimization result is bordered by the $f_{\mathrm{s,min}}$ constraint. Obviously h needs to be as low as necessary here in order to fulfill the maximum gain requirement (4.1). This is additionally supported by comparing scenario (1) with (2). Scenario (2) has a lower value for $f_{\mathrm{s,min}}$ defined and results in higher values of h. Also the $v_{\mathrm{Cs,max}}$ zone is extended to the range $f_0 > 65\,\mathrm{kHz}$. The zone $50\,\mathrm{kHz} < f_0 < 65\,\mathrm{kHz}$ of scenario (2) has no constraint bordered optimization result and hence results from a pure loss trade-off. The same applies to scenario (3) for the zone $50\,\mathrm{kHz} < f_0 < 75\,\mathrm{kHz}$. But here it has to be considered that the optimization solver could not reach solutions at $h > 25$ due to (5.15).
Looking at the efficiency η it can be observed that the difference between scenarios (2) and (3) on the one hand and scenario (1) on the other hand clearly correlates with the value of h. This result shows that the maximization of h is crucial for an efficiency optimized design not only for the simplified design case (5.12) but as well for the real design case examined here.

It is interesting that scenario (4) yields nearly the same component values as the reference scenario. Just the efficiency is lower due to the higher output load, and the b_{w} value is higher due to a changed compromise between core and conduction losses of the transformer. The similarity of (1) and (4) can be explained by the evidence that the results of (1) and (4) are completely determined by constraining borders and hence not a pure component loss trade-off is determinative for the result.

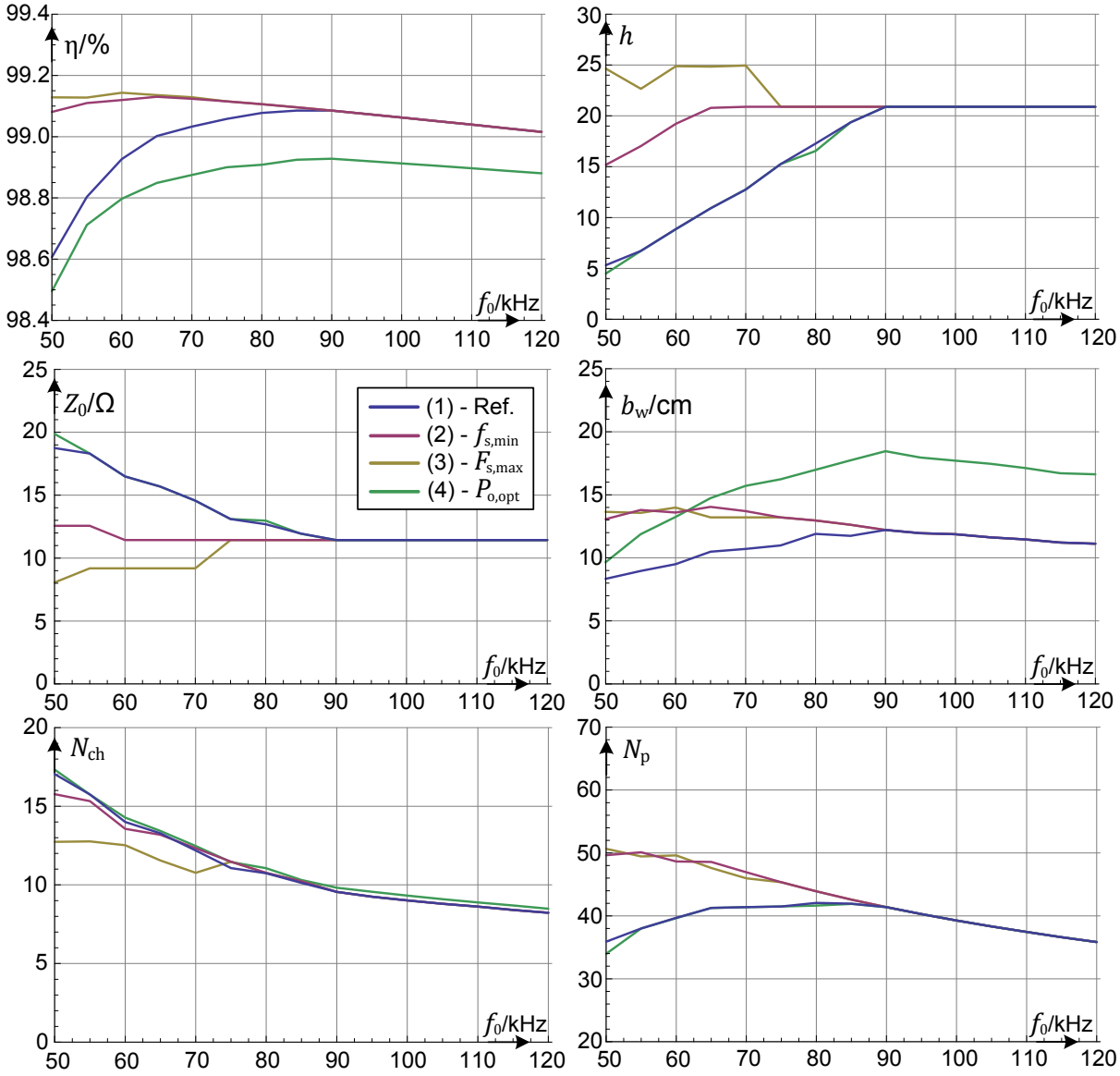

Fig. 5.13: Result of the optimization runs in dependence on the resonant frequency f_0. The curves are linearly interpolated from an evaluation grid with $\Delta f_0 = 5$ kHz. Drawn are the reference scenario (1) and scenarios (2) to (4).

Scenario (5) shows the dependence of the optimization result on the $v_{Cs,max}$ constraint. From Fig. 5.14 it can be observed that the efficiency is slightly higher compared to (1) throughout the whole f_0 range. With respect to parameter h the two zones $50\,\text{kHz} < f_0 < 95\,\text{kHz}$ with $f_{s,min}$ bordered results and $f_0 > 95\,\text{kHz}$ with pure loss trade-off results exist. It is remarkable that even though the efficiency of (5) is higher, the h values are nearly equal for (1) and (5) in the first zone. The difference is given by a higher value of Z_0 for (5) enabled by the released $v_{Cs,max}$ constraint. The higher value of Z_0 effects a higher value of L_p, which is the reason for the higher efficiency result even though the number of turns N_{ch} and N_p of the magnetic components are higher. Knowing this result it must be added that for scenario (1) the zone $50\,\text{kHz} < f_0 < 90\,\text{kHz}$ is not only constrained by $f_{s,min}$, but also by $v_{Cs,max}$. For scenario (1) this has not been explicitly detected. The probable reason for this is that the objective function may exhibit some roughness in this solution region which is higher than the detection accura-

cy of the optimization solver. Unfortunately this cannot be visualized, since the search vector dimension is higher than two. In Fig. 5.15 the $h - Z_0$ design plane is visualized for the point $f_0 = 70\,\text{kHz}$ of scenario (1). Even though l_g, l_xf and b_w are constant in this graphic, it can be already stated that no definite region most probably exhibiting the optimum can be announced.

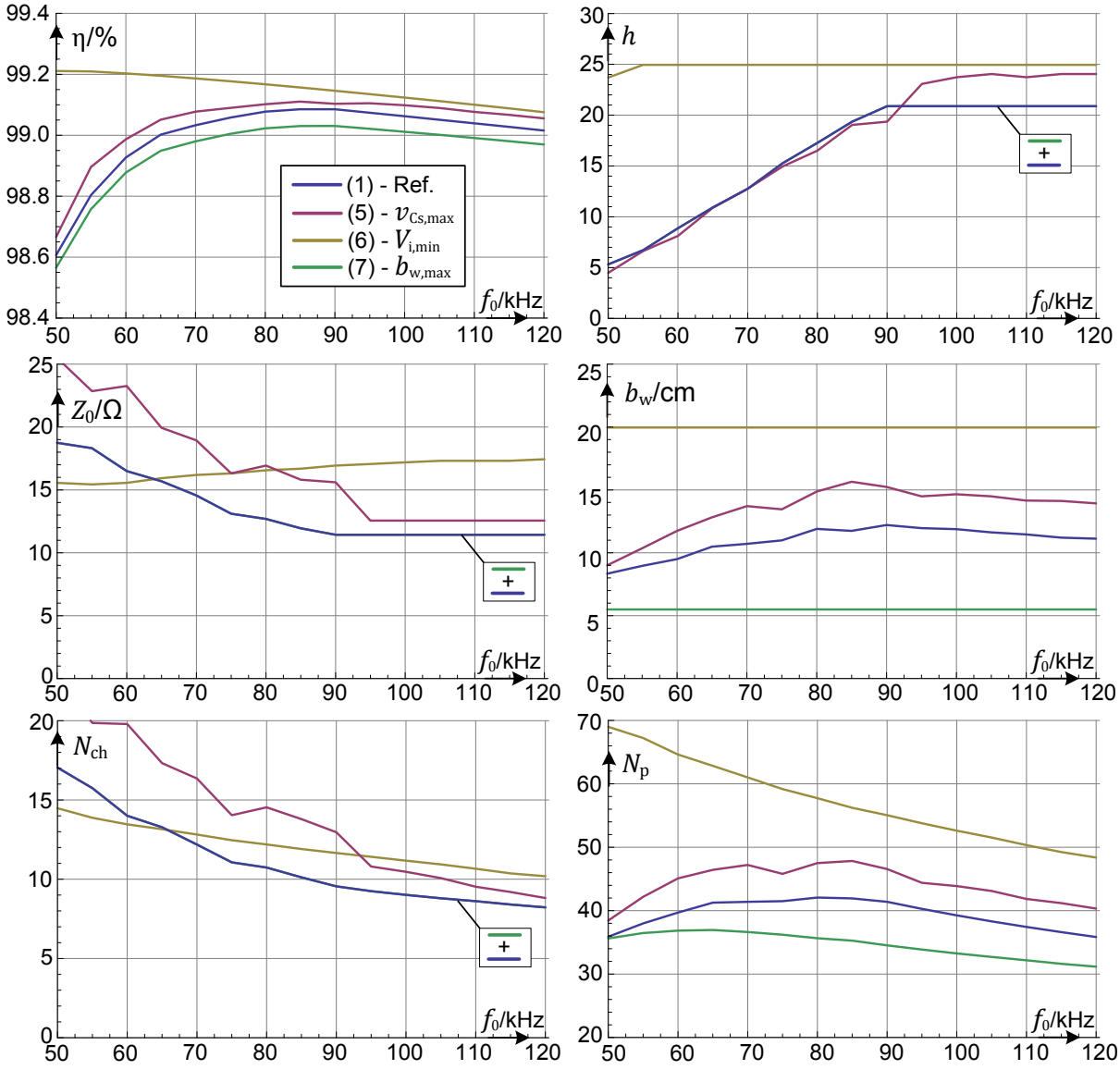

Fig. 5.14: Result of the optimization runs in dependence on the resonant frequency f_0. The curves are linearly interpolated from an evaluation grid with $\Delta f_0 = 5$ kHz. Drawn are the reference scenario (1) and scenarios (5) to (7).

Scenario (6) demonstrates the influence of the peak gain requirement by having a distinctive lowered one. It can be observed that h is at its maximum throughout nearly the whole f_0 range as well as the b_w parameter. Also no constraint impedes the optimization result except the search region boundaries (5.15). It can be stated that with only a low peak gain requirement the efficiency optimum is not located within the investigated f_0 range but at $f_0 < 50\,\text{kHz}$. A further remarkable observation is the characteristic of the parameters b_w and N_p. At scenario

(1) the volume of the transformer, though a free parameter via b_w, does not tend to increase infinitely but results in an optimal volume. But in scenario (6) the volume is unconditionally at its maximal allowed volume. In consequence a general proposition on the volume of the transformer, e.g. that a higher volume yields a higher efficiency cannot be stated. Instead the optimal volume always depends on the concrete design parameters.

Scenario (7) fixes the parameter b_w at 5.5 cm. But for the design parameters h and Z_0 no difference compared to the reference scenario results. The explanation for that is similar as for scenario (4): the optimized parameters are completely determined by constraining borders instead of loss trade-offs. Under such condition it would be possible to decouple the magnetic component optimization into a separate inner optimization loop and reduce the main search vector by the respective dimensions. In case the optimized parameters are determined by loss trade-offs, this statement cannot be generally made.

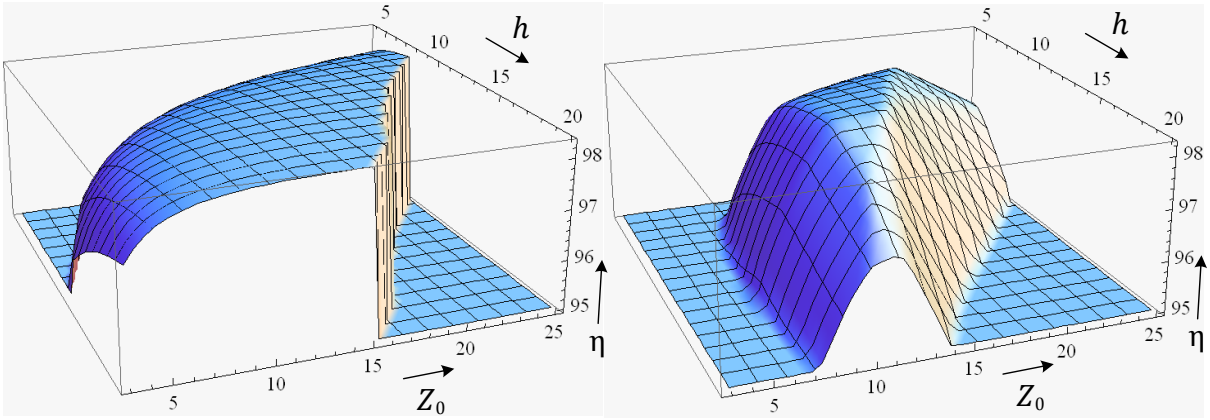

Fig. 5.15: $h - Z_0$ design plane at f_0 = 70 kHz and corresponding optimized parameters according to scenario (1): l_{ch} = 1.93 mm, l_{xf} = 2.00 mm, b_w = 10.7 cm; Left: w/o design penalties applied (k_{plt} = 0); Right: w/ design penalties applied (k_{plt} = 5)

The detailed loss distribution at the efficiency optimal point of the reference scenario is illustrated in Fig. 5.16. The highest losses occur in the bridge MOSFETs, second the transformer, third the rectifier and fourth the choke. The highest single loss part is clearly the conduction loss in the bridge MOSFETs. Using MOSFETs with lower on-state resistance but equal switching performance would be the most valuable point to further increase the efficiency of the example converter. Also due to the typical high temperature dependency of the $R_{DS(on)}$ of today's super junction MOSFETs good cooling of the bridge MOSFETs would benefit the conversion efficiency. For further efficiency optimization the transformer should be considered for optimization, e.g. by using better core material or more optimized litz wire. One residual point that is not covered by the optimization is the number of MOSFETs in parallel of the rectifier. The chosen number of 6 (c.f. Table 5.3) is subject to a preceded estimation for an optimal number. Based on the reference scenario result this number is verified:

No. in parallel	4	5	**6**	7	8	9
$P_{v,rec}$ / W	3.36	3.12	**3.04**	3.05	3.12	3.23

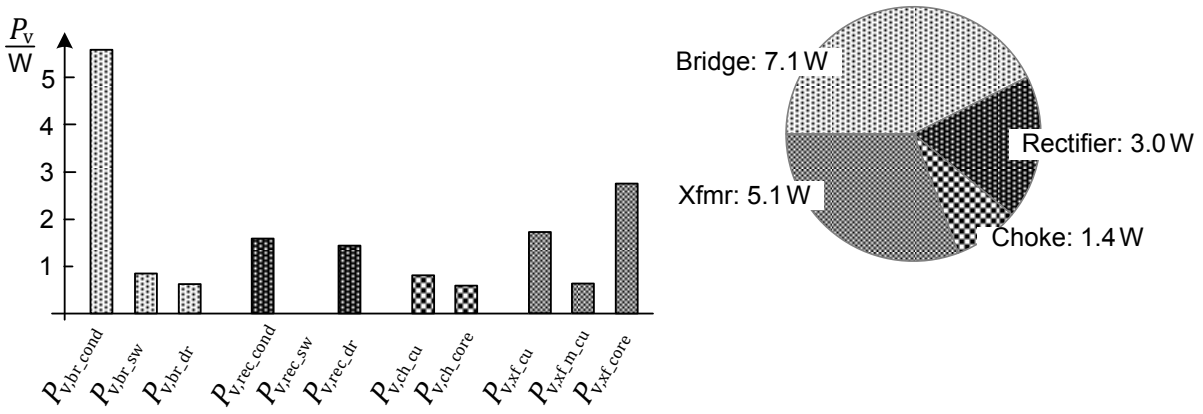

Fig. 5.16: Detailed loss distribution at the efficiency optimum f_0 = 85 kHz of scenario (1) and according to the loss listing of Table 5.5

Fig. 5.17 shows a loss breakdown of depicted scenarios in dependence on f_0. For the reference scenario it can be clearly observed that the losses on the primary side ($P_{\mathrm{v,br}}$, $P_{\mathrm{v,ch}}$, $P_{\mathrm{v,xf}}$) of the converter increase with increasing peak gain requirement as opposed to the losses on the secondary side ($P_{\mathrm{v,rec}}$) of the converter. Peak gain requirement here needs to be understood as a combination of the value of M_{pg} itself and the value of

$$f_0 - f_{\mathrm{s,min}}\big|_{M_{\mathrm{pg}}}. \tag{5.16}$$

Lower values of (5.16) require the LLC converter to yield a higher DC-DC gain with less change in the control variable f_{s}, which is considered as a higher peak gain requirement. For scenario (3) and (6) the peak gain requirement is reduced, i.e. for (3) the value of (5.16) is reduced and for (6) the value of M_{pg}. The reduced peak gain requirement leads to distinctively lower primary sided losses at low f_0 values. This coincides with the understanding that a high peak gain requirement requires a higher amount of reactive current in the resonant circuit, principally realized by reduced values of L_{p}, leading to higher losses in the primary side components.

At high f_0 values the losses of (1) and (3) are identical, which is in concordance to the equality of the h and Z_0 values (c.f. Fig. 5.13). Obviously the design is no longer determined by the peak gain requirement (5.16) in this zone. But scenario (6) exhibits some differences in the losses compared to (1): The lower losses in the bridge and in the transformer coincide with higher values of h, and the higher losses in the choke with higher values of Z_0 (c.f. Fig. 5.14). On component level referring to (6) compared to (1), L_{s} and L_{p} are increased and L_{p} is more increased than L_{s}. In the loss figure the sum of the losses of (6) is lower than of (1). As already analyzed before this is a result of the $v_{\mathrm{Cs,max}}$ constraint in combination with the peak gain requirement M_{pg}, which effects a limitation of the value of L_{s} and via h also a limitation of the value of L_{p} for scenario (1).

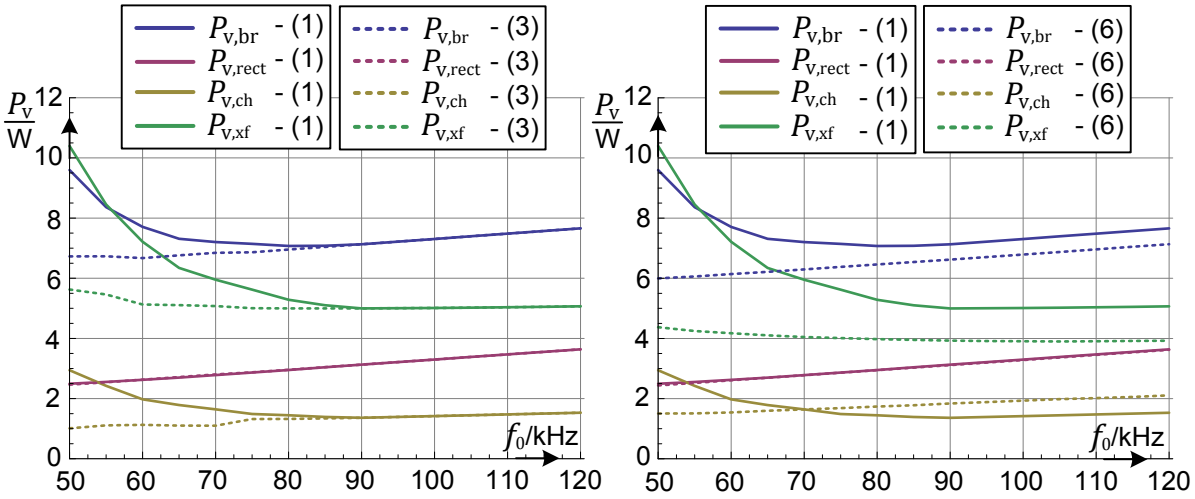

Fig. 5.17: Loss characteristics in dependence on f_0 for scenarios (1), (3) and (6). Losses are partially summarized according to the indices of the variables of Table 5.5.

6 Parallel Operation of LLC Converters

6.1 Basic Problems and Concepts

The parallel operation of power converters in general is driven by two factors. On the one hand it allows for a simple upscaling of the processed power. The advantages are less bulky components and more design flexibility. On the other hand the paralleled converters can be operated in the so called interleaving configuration. The interleaving configuration is successfully applied to PWM-type converters since many years, especially within PFC (Power Factor Correction) stages. Necessary condition for the interleaving configuration is that the paralleled converters are operated with the same switching frequency f_s. By appropriate phase-shift between the switching commands of the single converters, the input and output current ripples superimpose and cancel out each other to a certain degree. If n_{con} is the number of converters in parallel, a trivial phase-shift of $\varphi = 2\pi/n_{con}$ results in a major reduction of the ratio between the AC and the DC component of the overall output current. A more detailed analysis of the cancellation effect is presented in e.g. [Klaassens], and in case of PFC circuits in e.g. [Grote]. The reduced current ripple can be utilized to reduce the required volume of the filter components and/or to reduce the power losses in the filter components.

The interleaved paralleling of LLC resonant converters is considered especially in case of a low output voltage, at which the current ripple cancellation is highly demanded due to high output currents. The FOM of the current ripple cancellation effect is given by the ratio between the RMS value of the AC component of the converters superimposed output currents I_{o,RMS_AC} and the overall DC output current I_o: $\mathrm{FOM}_{int} = I_{o,RMS\_AC}/I_o$. The output current of a LLC converter operating close to its resonance frequency can be approximated by a rectified sinus waveform $i_o(t) = |\sin(2\pi f_s t)|$. Then the FOMs of a single LLC converter and two resp. three interleaved converters are given by

$$\mathrm{FOM}_{int,1} = \sqrt{\frac{1}{2} - \frac{4}{\pi^2}\frac{\pi}{2}}\,, \quad \mathrm{FOM}_{int,2} = \sqrt{1 + \frac{2}{\pi} - \frac{16}{\pi^2}\frac{\pi}{4}}\,, \quad \mathrm{FOM}_{int,3} = \sqrt{2 + \frac{3\sqrt{3}}{\pi} - \frac{36}{\pi^2}\frac{\pi}{6}}\,. \tag{6.1}$$

The ratios between the FOM factors yield the reduction of ripple current for a given output power:

$$\frac{\mathrm{FOM}_{int,2}}{\mathrm{FOM}_{int,1}} \approx 0.202\,, \qquad \frac{\mathrm{FOM}_{int,3}}{\mathrm{FOM}_{int,2}} \approx 0.429\,, \qquad \frac{\mathrm{FOM}_{int,3}}{\mathrm{FOM}_{int,1}} \approx 0.087\,. \tag{6.2}$$

(6.2) shows that the RMS ripple current is reduced approximately 5 times if a certain output power is realized by two interleaved operating LLC converters instead of one single converter. Furthermore it is reduced more than 10 times for three interleaved converters. The reduction has a great relevance considering the absolute value of $\mathrm{FOM}_{int,1} \approx 0.48$, which means that the RMS ripple current flowing in the output filter capacitors is roughly one half of the overall output current I_o. For the case of a 12 V and 3 kW output the resulting ripple currents are summarized in Table 6.1. In case of a single LLC converter the output filter capacitors need to

conduct a RMS current of more than 120 A, which would require a very costly output filter in terms of volume, efficiency and thermal limits. In consequence the interleaved operation of at least two LLC converters for high power and low voltage outputs is highly demanded.

Table 6.1: Approximate output capacitor ripple current in dependence of the number of interleaved converters

	Single	2-interleaved	3-interleaved
I_{o}	250 A	250 A	250 A
$I_{\mathrm{o,RMS\_AC}}$	120.9 A	24.43 A	10.49 A

Unfortunately a serious issue arises when operating two or more LLC resonant converters in an interleaving configuration, namely the unbalanced power distribution among the paralleled converters resulting from value mismatches of the passive resonant circuit elements. At this point the LLC resonant converter distinguishes from PWM-type converters: To enable the current ripple cancellation effect the paralleled converters have to be operated at the same switching frequencies. Since for PWM-type converters the control quantity is duty-cycle, each converter can be controlled independently regardless of the equality of the switching frequencies. On the contrary the control quantity of the LLC converter is the switching frequency, where the duty-cycle is constantly 50% to achieve and retain soft switching. Hence, LLC converters in an interleaved configuration cannot be controlled independently and power sharing among the converters becomes an issue.

According to the analytical results within this work the load sharing among interleaved LLC converters is quite sensitive to value mismatches of the passive resonant circuit components and sufficient reliability in mass production is critical. Since the LLC resonant circuit exhibits the three passive components L_s, L_p and C_s, a plurality of possible load sharing characteristics results, which have to be investigated thoroughly. The following analysis is based on the steady-state load sharing characteristics. It is expected that the dynamic load sharing characteristic is close to the steady-state one, since no noticeable load sharing dynamic effects could be observed during prototype measurements. However, the dynamic load sharing characteristic among interleaved LLC converters and stability considerations could be a topic for further investigations.

6.2 Analysis of Current Share Behavior

In this work the analysis of the load sharing error among interleaved operated LLC converters is limited to $n_{\mathrm{con}} = 2$. In this case the LLC converters are designated LLC_1 and LLC_2. The resonant circuit element values of each converter are given by

$$\begin{bmatrix} L_{\mathrm{s},1} \\ C_{\mathrm{s},1} \\ L_{\mathrm{p},1} \end{bmatrix} = \left(1 + \begin{pmatrix} k_{\mathrm{Ls},1} \\ k_{\mathrm{Cs},1} \\ k_{\mathrm{Lp},1} \end{pmatrix} \right) \begin{bmatrix} L_{\mathrm{s}} \\ C_{\mathrm{s}} \\ L_{\mathrm{p}} \end{bmatrix} \qquad \begin{bmatrix} L_{\mathrm{s},2} \\ C_{\mathrm{s},2} \\ L_{\mathrm{p},2} \end{bmatrix} = \left(1 + \begin{pmatrix} k_{\mathrm{Ls},2} \\ k_{\mathrm{Cs},2} \\ k_{\mathrm{Lp},2} \end{pmatrix} \right) \begin{bmatrix} L_{\mathrm{s}} \\ C_{\mathrm{s}} \\ L_{\mathrm{p}} \end{bmatrix}. \tag{6.3}$$

In the context of a reasonable converter design the worst-case load sharing error is of highest interest. Assuming that $\pm p$ is the tolerance band of each resonant circuit element, the maxi-

mum value mismatch of each element between the paralleled converters is $2p$ of the nominal value. In the following always the maximum value mismatch of $2p$ is assumed so that

$$\begin{pmatrix} k_{\mathrm{Ls},1} \\ k_{\mathrm{Cs},1} \\ k_{\mathrm{Lp},1} \end{pmatrix} = -\begin{pmatrix} k_{\mathrm{Ls},2} \\ k_{\mathrm{Cs},2} \\ k_{\mathrm{Lp},2} \end{pmatrix} = \begin{pmatrix} sgn_{\mathrm{Ls1}} \\ sgn_{\mathrm{Cs1}} \\ sgn_{\mathrm{Lp1}} \end{pmatrix} \begin{pmatrix} p_{\mathrm{Ls}} \\ p_{\mathrm{Cs}} \\ p_{\mathrm{Lp}} \end{pmatrix}. \tag{6.4}$$

The *sgn* vector in (6.4) contains the elements +1 and -1 and defines the direction of the value deviations. For the *sgn* vector eight variants exist

$$\begin{pmatrix} sgn_{\mathrm{Ls1}} \\ sgn_{\mathrm{Cs1}} \\ sgn_{\mathrm{Lp1}} \end{pmatrix} = \begin{pmatrix} + & + & - & - & , & - & - & + & + \\ + & + & + & + & & - & - & - & - \\ + & - & - & + & & - & + & + & - \end{pmatrix}, \tag{6.5}$$

in which one half of the variants is symmetric to the other half. In consequence only 4 worst-case variants have to be evaluated in the analysis.

In order to deduce more general conclusions the *sgn* vector can be translated into the parameters f_0, h, Z_0 by stating the value relations "<", "=" and ">" between LLC_1 and LLC_2:

$$\begin{pmatrix} + \\ + \\ + \end{pmatrix} \rightarrow \begin{pmatrix} f_{0,1} < f_{0,2} \\ Z_{0,1} = Z_{0,2} \\ h_1 = h_2 \end{pmatrix} \qquad \begin{pmatrix} + \\ + \\ - \end{pmatrix} \rightarrow \begin{pmatrix} f_{0,1} < f_{0,2} \\ Z_{0,1} = Z_{0,2} \\ h_1 < h_2 \end{pmatrix} \tag{6.6}$$

$$\begin{pmatrix} - \\ + \\ - \end{pmatrix} \rightarrow \begin{pmatrix} f_{0,1} = f_{0,2} \\ Z_{0,1} < Z_{0,2} \\ h_1 = h_2 \end{pmatrix} \qquad \begin{pmatrix} - \\ + \\ + \end{pmatrix} \rightarrow \begin{pmatrix} f_{0,1} = f_{0,2} \\ Z_{0,1} < Z_{0,2} \\ h_1 > h_2 \end{pmatrix}. \tag{6.7}$$

The load sharing error is characterized in an unsymmetrical splitting of the overall output current $I_\mathrm{o} = I_{\mathrm{o},1} + I_{\mathrm{o},2}$ on the single LLC converters. Hence a factor K_sh can be defined such that

$$I_{\mathrm{o},1} = K_\mathrm{sh}\left(I_{\mathrm{o},1} + I_{\mathrm{o},2}\right) \qquad I_{\mathrm{o},2} = (1 - K_\mathrm{sh})\left(I_{\mathrm{o},1} + I_{\mathrm{o},2}\right) \quad \text{with} \quad K_\mathrm{sh} = 0..1. \tag{6.8}$$

K_sh is a function of the value mismatches of the resonant circuit elements: $K_\mathrm{sh} = F(k_\mathrm{Cs},k_\mathrm{Ls},k_\mathrm{Lp})$. In order to determine the value of K_sh at a certain component mismatch, the steady-state solution of parallel operating LLC converters needs to be found. Advantageously, the exact time domain modeling approach derived in Chapter 3.1.4 has to be used, if long running times of SPICE-like time domain simulations shall be avoided. Therefore an iterative procedure in form of a bisection algorithm was developed and is shown in Fig. 6.1. The algorithm finds the K_sh value in less than one second on a standard office PC. The key step in the algorithm is the calculation of the DC-DC gains M_1 and M_2 in dependence on K_sh. Therefore the steady-state solver based on the exact time domain modeling is called twice with the different parameter sets (6.9) and (6.10).

$$d_1 = \frac{d}{\sqrt{(1+p_{\mathrm{Cs}}\%)(1+p_{\mathrm{Ls}}\%)}} \qquad h_1 = h\frac{1+p_{\mathrm{Lp}}\%}{1+p_{\mathrm{Ls}}\%}$$
$$J_{\mathrm{o},1} = J_{\mathrm{o}}K_{\mathrm{sh}}2\sqrt{(1+p_{\mathrm{Cs}}\%)(1+p_{\mathrm{Ls}}\%)} \qquad \theta_{2,1} = \frac{\pi}{F_{\mathrm{n}}}\frac{1}{\sqrt{(1+p_{\mathrm{Cs}}\%)(1+p_{\mathrm{Ls}}\%)}}\,, \tag{6.9}$$

$$d_2 = \frac{d}{\sqrt{(1-p_{\mathrm{Cs}}\%)(1-p_{\mathrm{Ls}}\%)}} \qquad h_2 = h\frac{1-p_{\mathrm{Lp}}\%}{1-p_{\mathrm{Ls}}\%}$$
$$J_{\mathrm{o},2} = J_{\mathrm{o}}(1-K_{\mathrm{sh}})2\sqrt{(1-p_{\mathrm{Cs}}\%)(1-p_{\mathrm{Ls}}\%)} \qquad \theta_{2,2} = \frac{\pi}{F_{\mathrm{n}}}\frac{1}{\sqrt{(1-p_{\mathrm{Cs}}\%)(1-p_{\mathrm{Ls}}\%)}}\,. \tag{6.10}$$

The purpose of the bisection method is to find the K_{sh} value that satisfies the condition $M_1 = M_2$, which represents the steady-state solution of the paralleled LLC converters. Therefore the algorithm step-wise changes the K_{sh} value starting at the initial value 0.5, which represents the steady-state solution with no element mismatch $p = 0$. The algorithm proceeds in one direction until a zero crossing is detected. After each zero crossing the step-width is halved and the search direction reversed. Finally the algorithm stops if the actual evaluation is lower than the predefined value ε.

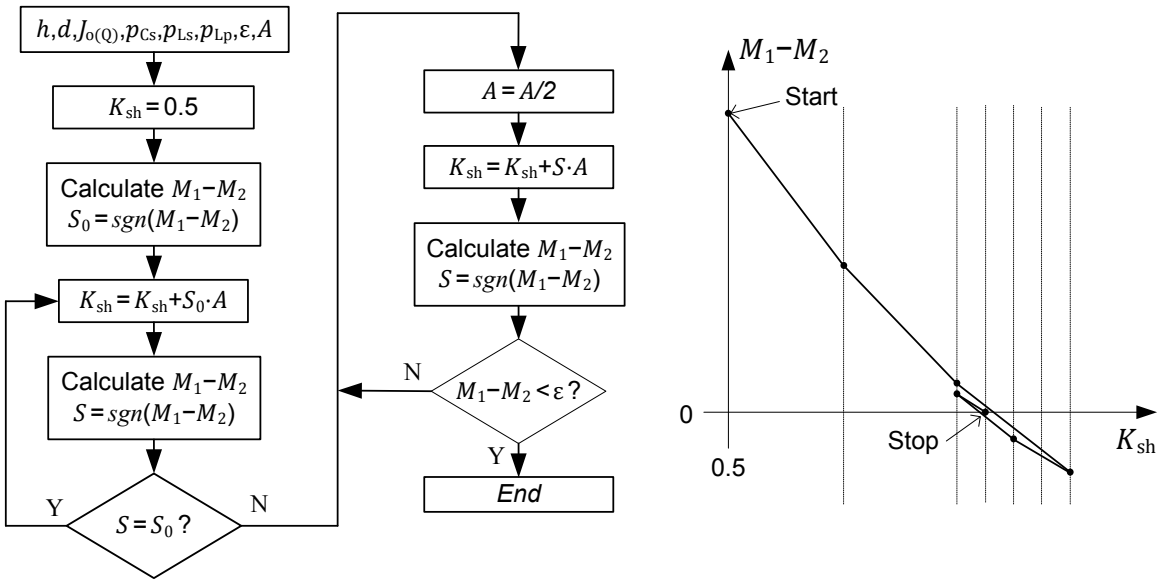

Fig. 6.1: Applied bisection algorithm for finding the steady-state solution of paralleled LLC converters with mismatched circuit components; symbol A: step width, symbol S: search direction

The evaluation of K_{sh} in dependence on the normalized switching frequency F_{n} for the cases given by (6.6) and (6.7) and at $p = 2.5\%$ is shown in Fig. 6.2. The following observations can be made:

- The load sharing error grows worse at lower output loads in every case. One root cause of this behavior is the resistive damping, which has less influence at lower current levels

- The influence of h mismatch, which is proportional to L_p at constant f_0 and Z_0, is small in the above resonance region and moderate in the below resonance region by comparing diagrams A to B and C to D.
- The influence of a mismatch in Z_0 is very small, which can be seen in diagram D.

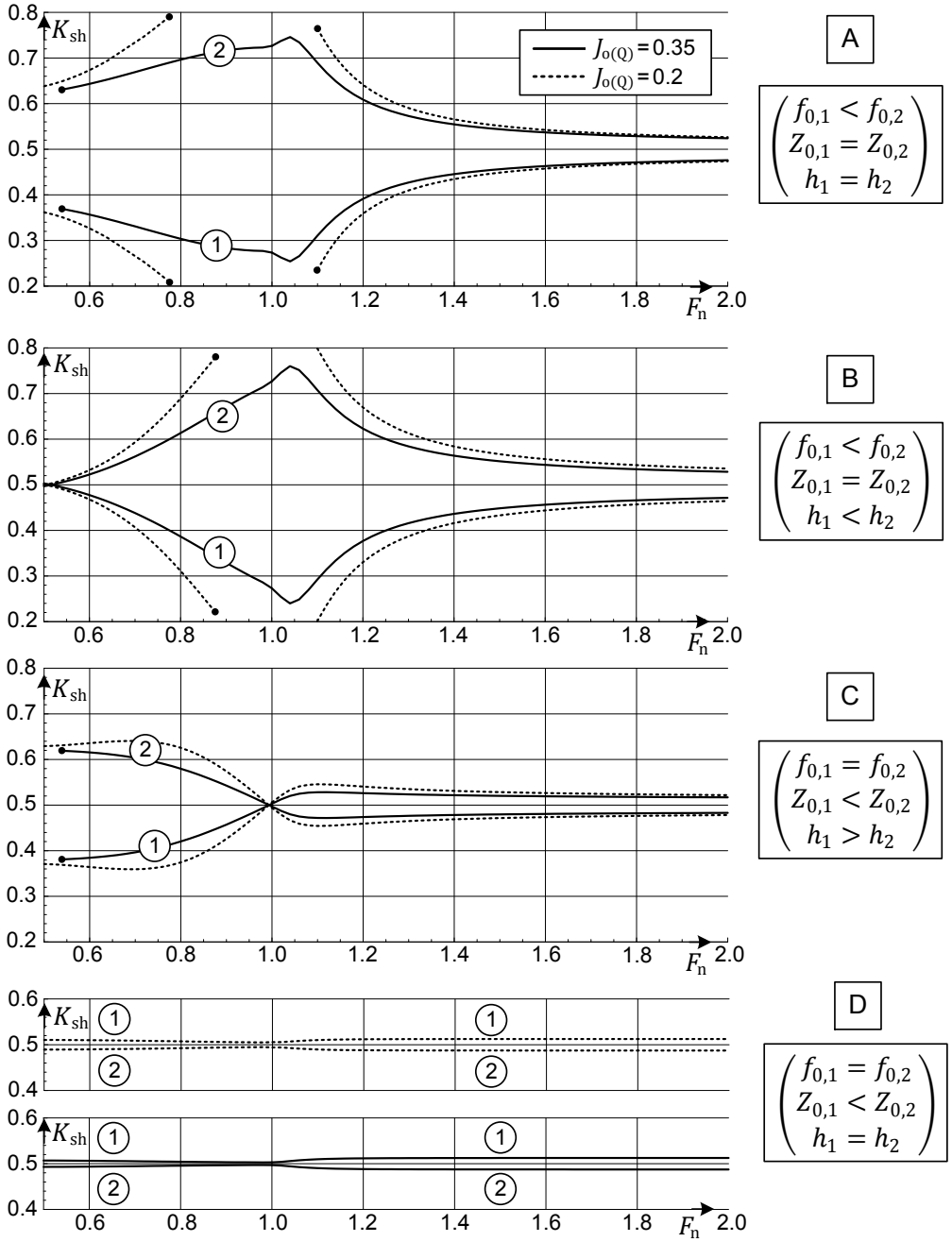

Fig. 6.2: Evaluation of K_sh in dependence on the worst-case value mismatches A to D and at $p = 2.5\%$, $h = 10$, $d = 0.03$; dots mark operating mode boundaries except at $F_\mathrm{n} = 1$; Curves are interpolated from a sampling rate of $\Delta F_\mathrm{n} = 0.02$.

- The influence of a mismatch in f_0 is very distinct, which can be seen in diagram A. The root cause of this behavior is the low output impedance, i.e. load independent DC-DC gain of the LLC converter in the vicinity of the resonance point. The ideal LLC

converter exhibits load independent DC-DC gain at $F_n = 1$ which would result in $K_{sh} = 0$ or $K_{sh} = 1$ respectively at that point. The reason of a K_{sh} value above 0.2 in diagram A is the resistive damping described by the factor d (c.f. Fig. 3.5). The influence of d on the load sharing behavior is demonstrated by Fig. 6.3. Beneath the resonance region the load sharing becomes very unbalanced especially in the below resonance region. This coincides with the fact, that especially in the below resonance region the DC-DC gain curves can be described as stiff with respect to the output loading (c.f. Fig. 3.5), i.e. the LLC converter exhibits a low steady-state output impedance in this region. The stiffness is softened by the presence of damping.

According to the above analysis consequences on a practical usage of the interleaved paralleling of LLC converters arise. Even though the tolerance class of $p = \pm 2.5\%$, which was used for the analysis, is already challenging to guarantee in mass production, a worst case load sharing error of more than ±20% at full load condition results in the vicinity of the resonance point. Also the assumed damping of $d = 3\%$ is a realistic value derived from experimental loss measurements. Since the preferred operating area of the LLC converter employed in highly efficient PSUs is the resonance frequency vicinity, the high sensitivity of the load sharing to component value mismatches impedes the use of the LLC interleaving configuration without additional measures.

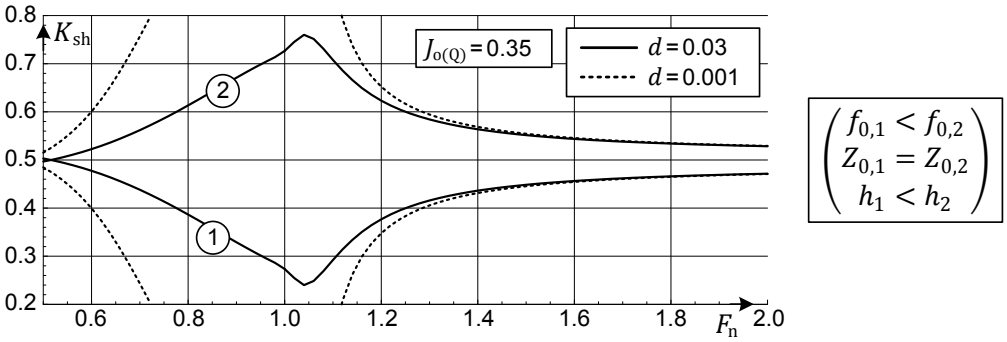

Fig. 6.3: Evaluation of K_{sh} for a certain worst-case value mismatch and in dependence on the resistive damping d at $p = 2.5\%$, $h = 10$; Curves are interpolated from a sampling rate of $\Delta F_s = 0.02$.

6.3 Industrial Solutions

The load sharing analysis of Chapter 6.2 revealed that additional measures are compulsory if an interleaved operation of paralleled LLC converters is desired. In literature only few propositions exist how to practically deal with the load sharing issue ([Figge2], [Figge3], [Orietti], [Kim], [Yang2]).

For the method presented in [Orietti] the resonant current return paths of three half-bridge LLC converters are star connected forming a three phase system. The measurement results show that the balancing issue can be addressed by this method. But a lot of question arise in terms of practical issues like no-load, burst-mode, short-circuit and start-up behavior. Up to now no report about the practical feasibility of the concept for industry is known.

A theoretically straight forward approach is to feed each LLC converter with different input voltages, thereby maintaining the current ripple cancellation effect only on the output side of the converters. This would be still desirable in case of e.g. sever PSUs, because their DC-link voltage is high and the current ripple cancellation effect is especially demanded on the low voltage high current output side. One practical solution on how to supply each of two LLC converter rails with different input voltages is a series connection of the input voltages ([Figge2], [Kim], [Yang2]). In such a configuration an inherent input current balance is achieved because the input capacitor of the converter that draws more input current will discharge and the other input capacitor will charge accordingly until a balanced steady-state is reached. Even though this solution will probably perform well in practice, the disadvantage is that at a given DC- link voltage the resulting input voltages of both LLC converter rails are halved and the input currents are doubled, leading to higher resistive losses on the primary side of the converters and hence to lower conversion efficiency.

Due to the efficiency drawback of an input-series connection of interleaved LLC converters another method is proposed in this work [Figge5], which is especially applicable to high power PSUs. It relies on the fact that in high power PSUs also the PFC stage is often built in an interleaved configuration and hence can be utilized to provide two independently adjustable DC-link voltages. Fig. 6.4 shows the evolution of the circuit concept. The solution is designated as “Dual DC-Link” (DDL) concept.

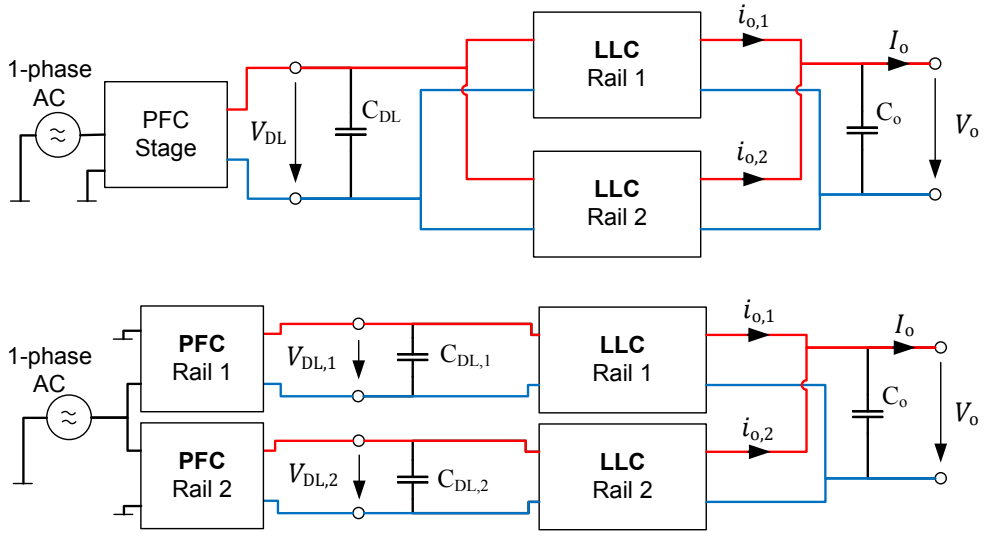

Fig. 6.4: Two possible circuit concepts of a high power server PSU incorporating two paralleled LLC converters. Top: Simple drop-in variant; Bottom: Variant employing the “Dual DC-Link” (DDL) configuration

By supplying each LLC converter with a separate input voltage, the load sharing among the converter rails can be actively balanced. Since both rails are fed from the same AC-grid phase, the low frequency DC-link voltage ripple will be similar on both links, resulting in a constant voltage difference $\Delta V_{DL} = V_{DL,1} - V_{DL,2}$ throughout the entire AC period.

An important point of the DDL concept is the knowledge of the worst-case value of ΔV_{DL} since the DC-link voltage exhibits upper and lower limits. The lower limit is given by the maximum AC grid peak-voltage V_{AC,pk_max} . In order to maintain regulation of the PFC’s boost

converter, the DC-link voltage needs to be higher than $V_{\mathrm{AC,pk\_max}}$. The upper limit $V_{\mathrm{DL,max}}$ is given by the voltage rating of the DC-Link capacitor and the primary sided switches of the DC-DC converter. Since the PSU has 1-phase input a low frequency voltage ripple $V_{\mathrm{DL,pk\text{-}pk}}$ is superimposed on the DC-Link voltage. Furthermore considering a voltage buffer $V_{\mathrm{DL,buf}}$ for transients, the DC-link voltage difference is limited to

$$\Delta V_{\mathrm{DL}} < V_{\mathrm{DL,max}} - V_{\mathrm{AC,pk\_max}} - V_{\mathrm{DL,pk\text{-}pk}} - V_{\mathrm{DL,buf}} \tag{6.11}$$

A typical value for (6.11) is 450 V − 375 V − 30 V − 30 V = 15 V. In order to determine ΔV_{DL} in dependence on the worst-case element value mismatches at $\pm p$ deviations, the steady-state inverse DC-DC gains $1/M_1$ and $1/M_2$ at balanced output currents $I_{\mathrm{o},1} = I_{\mathrm{o},2}$ must be calculated. Denormalization of $1/M$ for a given output voltage V_{o} and transformer turns ratio n yields the corresponding input voltage V_{DL} of the LLC converter. The calculated inverse DC-DC gains and respective input voltages in dependence on the normalized switching frequency F_{n} for the cases given by (6.6) and (6.7) and at $p = 2.5\%$ are shown in Fig. 6.5. For the resulting characteristic of the DC-link voltage difference ΔV_{DL} the following observations are made:

- Similar to the outcomes of the load sharing analysis of Chapter 6.2 the highest impact on ΔV_{DL} is given by a mismatch of the resonant frequencies f_0, which can be seen in diagram A. ΔV_{DL} is approximately constant in the below resonance region and doubles throughout the F_{n} transition $1 \rightarrow 1.2$, i.e. between resonance and above resonance operation.
- From diagrams A to D it is observed that the impact of the output loading, represented by J_{o}, on ΔV_{DL} is roughly negligible in the below resonance region. In the above resonance region ΔV_{DL} slightly increases with increasing output loading.
- The impact of h mismatch, which is proportional to L_{p} at constant f_0 and Z_0, is observed to be small in total by comparing diagrams A to B and C to D.
- The impact of a mismatch in Z_0 is generally very small, which can be seen in diagram D.
- The impact of the damping factor d on ΔV_{DL} is additionally highlighted in Fig. 6.6. Whereas the absolute values of $1/M_1$ and $1/M_2$ are clearly shifted by the damping effect, it is observed that, in contrast to the respective situation in Fig. 6.3, here the impact of d is more or less negligible in the whole depicted parameter range.

In the shown case of an exemplary assumed tolerance class of $p = 2.5\%$ for all the three resonant circuit elements, obviously (6.11) is easily met throughout the depicted F_{n} range. However, a more feasible tolerance class for mass production is $p = 5\%$ for all the three resonant circuit elements, which is stated from the industrial experience of the author. In such case, which is shown by Fig. 6.7 for mismatches A and B, the constraint (6.11) becomes violated in above resonance operation. But in the vicinity of the resonance, which is the preferred nominal operating condition of the LLC converter, as well as in below resonance, (6.11) still is met. In consequence (6.11) becomes a further design constraint and must be included into an optimal design process of the interleaved operated LLC converters.

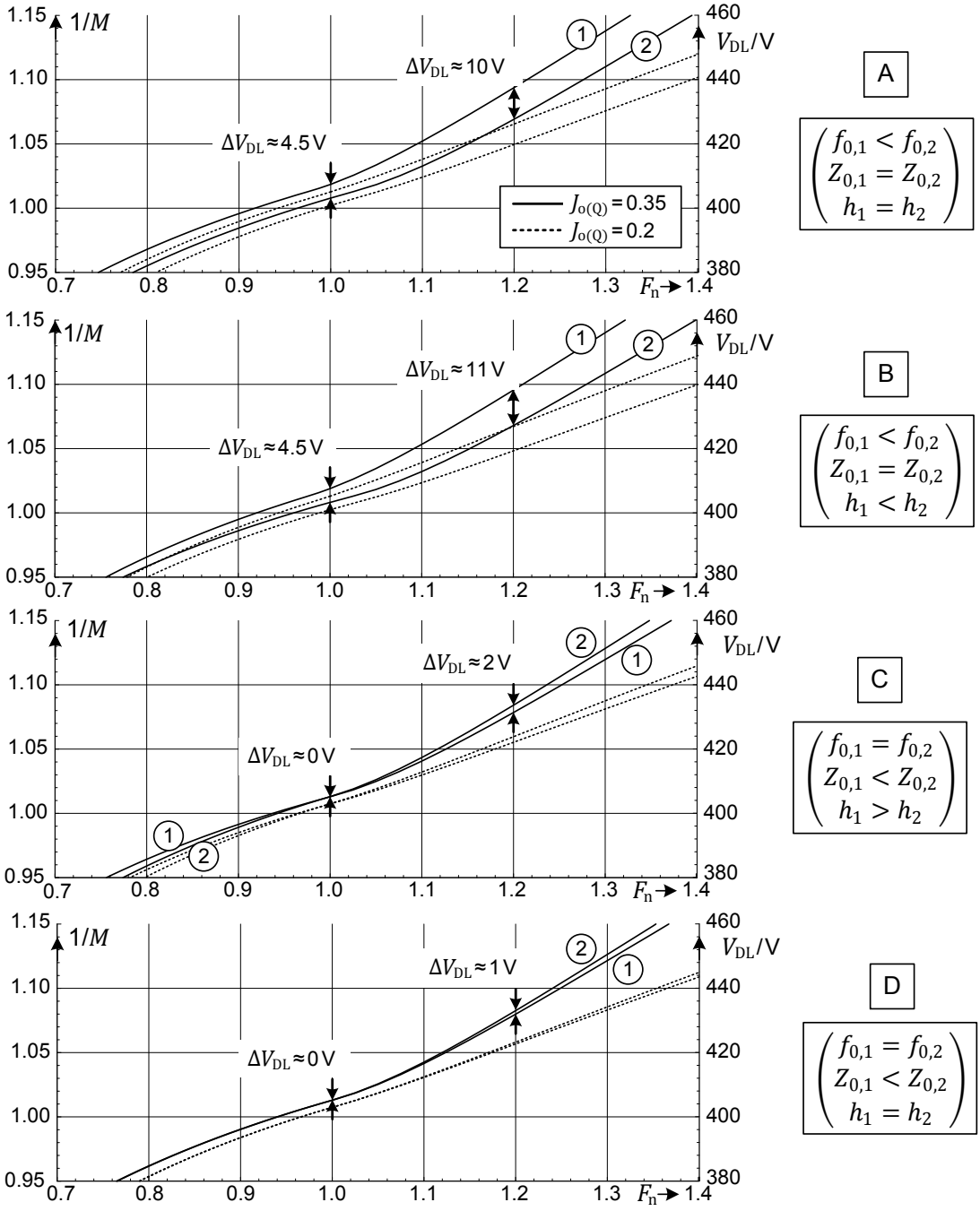

Fig. 6.5: Diagrams of the normalized DC-link voltages 1/M at balanced output currents $I_{o,1} = I_{o,2}$ in dependence on the worst-case value mismatches A to D and at $p = 2.5\%$, $h = 11.5$, $d = 0.03$. The right y-axis represents the denormalized DC-link voltage for $n = 16$ (case half-bridge) and $V_o = 12.5$ V; Curves are interpolated from a sampling rate of at least $\Delta F_n = 0.025$.

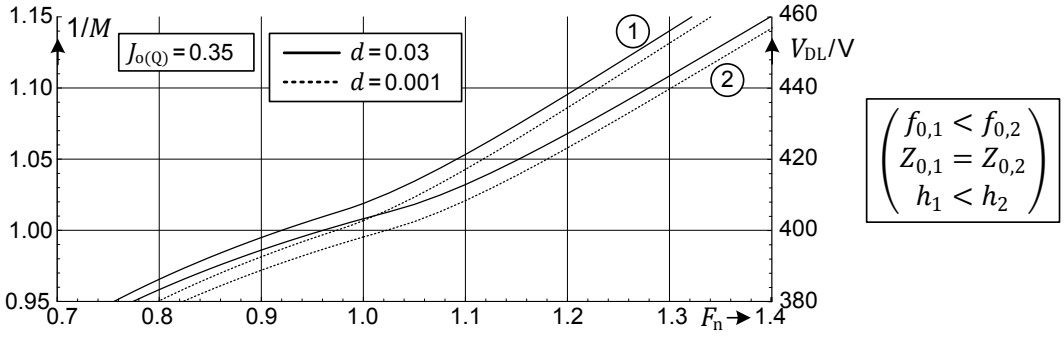

Fig. 6.6: Diagram of the normalized DC-link voltages 1/M at balanced output currents $I_{o,1} = I_{o,2}$ for a certain worst-case value mismatch and two different damping factors d at $p = 2.5\%$, $h = 11.5$. The right y-axis represents the denormalized DC-link voltage for $n = 16$ (case half-bridge) and $V_o = 12.5$ V; Curves are interpolated from a sampling rate of at least $\Delta F_n = 0.025$.

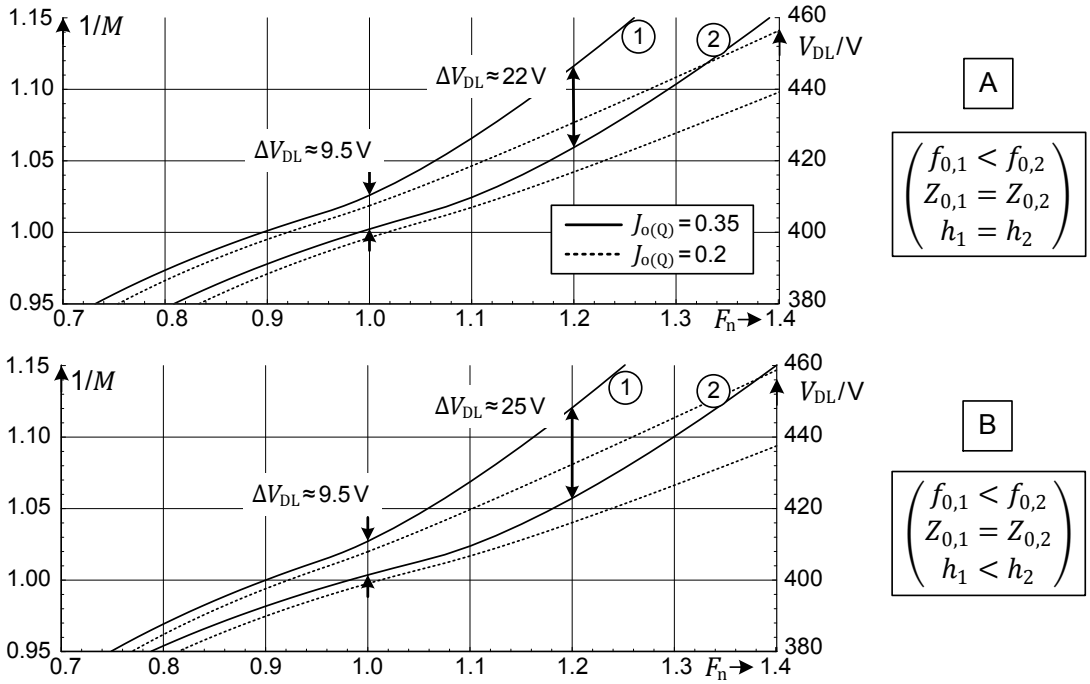

Fig. 6.7: Diagrams of the normalized DC-link voltages 1/M at balanced output currents $I_{o,1} = I_{o,2}$ for certain worst-case value mismatches A and B and at $p = 5\%$, $h = 11.5$, $d = 0.03$. The right y-axis represents the denormalized DC-link voltage for $n = 16$ (case half-bridge) and $V_o = 12.5$ V; Curves are interpolated from a sampling rate of at least $\Delta F_n = 0.025$.

6.4 Experimental Results

As already stated the interleaved paralleling of LLC converters is especially demanded in case of low voltage high current outputs. Therefore the experimental results are obtained on a PSU prototype unit providing a nominal 3 kW of output power at 12.2 V output voltage, resulting in a 246 A of total output current. The prototype unit is constructed similar to Fig. 6.4, bottom. It consists of a single phase AC grid input fed to two interleaved operated PFC circuits. The

PFC circuits generate two DC-link voltages of approximately 400 V, acting as inputs of two LLC converters that are connected in parallel at their outputs and interleaved operated. For test purposes the both DC-link voltages can be connected to each other in order to disable the DDL functionality. The LLC converters comprise a Synchronous Rectification (SR). The SR is necessary to limit the power losses generated by the high output current flowing in the rectification semiconductors (c.f. Fig. 2.4). As a matter of the SR control implementation used in this prototype, the SR device is not turned on throughout its whole conduction period, which leads to partial body diode conduction intervals at the borders of the conduction period (c.f. [Figge]). Those body diode conduction intervals generate a certain modeling error, because they are not covered by the model used in this work. The used model assumes that the SR devices are ideally turned-on and therefore are modeled by the single on-state resistance of the SR MOSFET. Furthermore the length of these intervals varies in dependence on the load condition and the operating frequency. Whereas at operating frequencies $F_n < 1$ the relative length of the body diode conduction time is small and roughly constant throughout the operating range, it increases with increasing operating frequency at $F_n > 1$. The SR modeling error needs to be considered for the following comparisons between calculated and measured values.

The general compliance of the steady-state model with the LLC converters of the prototype was tested by means of the steady-state DC-DC gain. A comparison between modelled and measured DC-DC gain is shown in Fig. 6.8. It is observed that the accuracy is acceptable especially at resonance and below resonance operation. In the above resonance region a clear modeling error arises. The error increases with increasing switching frequency. The source of the error is supposed to be a superposition of two effects: Firstly the body conduction time of the SR devices increases with increasing switching frequency in the above resonance region and thus the DC-DC gain drops accordingly. The body diode conduction time as well increases with increasing output loading. Hence, the DC-DC gain drop related to the body diode effect should be stronger at higher output loadings, which is confirmed by the measurement results. The higher measured DC-DC gain at the lower output loading $J_{o(l)} = 0.195$ is caused by a second effect, namely an additional resonance between inductance L_s and the junction capacitances C_j of the SR MOSFETs. This effect is qualitatively demonstrated by considering C_j capacitance for the FHA DC-DC gain approximation of the LLC converter, which is shown in Fig. 6.9.

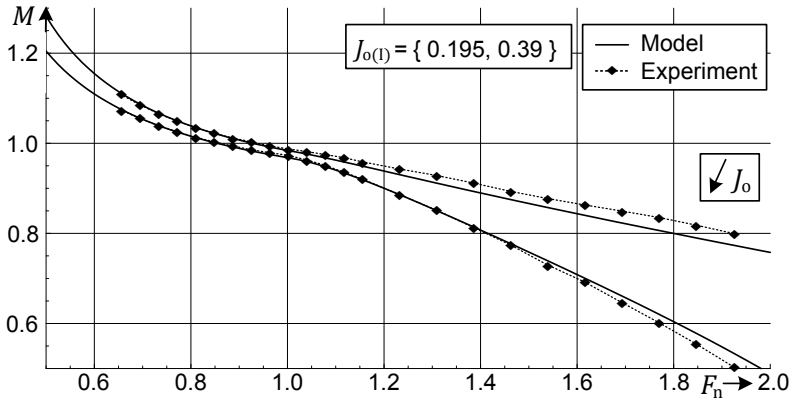

Fig. 6.8: Calculated and measured steady-state DC-DC gain at h = 11.5 and d = 6.6%

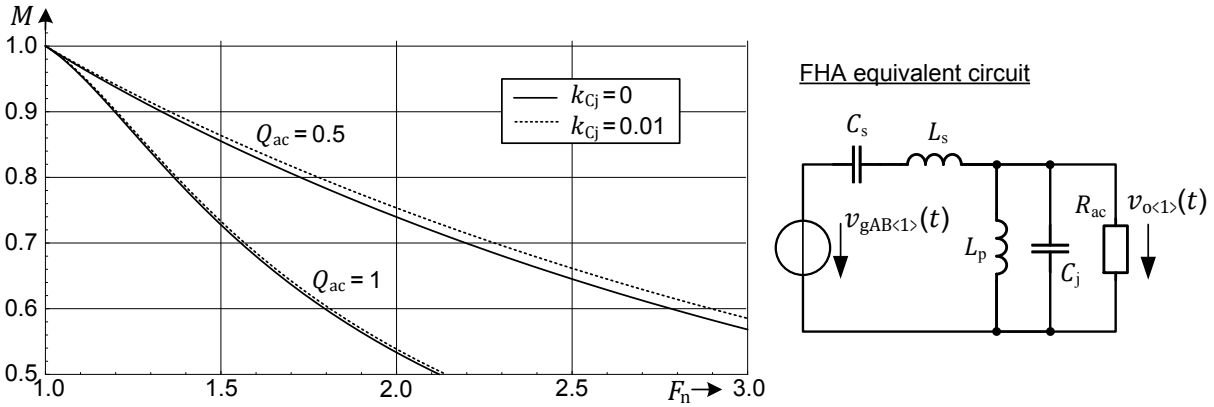

Fig. 6.9: Steady-state DC-DC gain including the capacitance C_j and calculated by FHA means; The value of C_j is given by $C_j = k_{Cj} \cdot C_s$; $h = 6$.

In order to verify the theoretical load sharing analysis the prototype was configured with disabled DDL functionality, i.e. with both DC-link voltages connected to each other, thus feeding only one single voltage to the inputs of both LLC converters. Furthermore the resonant inductor of converter LLC_1 was increased, representing the worst-case deviation of a tolerance class of $p_{Ls} = 7.2\%$. The measurement of the inductances $L_{p,1}$ and $L_{p,2}$ revealed $p_{Ls} = 1\%$ and the measurement of the capacitances $p_{Cs} \approx 0\%$. With these values the mismatch cases given by (6.12) can be realized. Since the load sharing analysis in Chapter 6.2 revealed that the dependence of the load sharing on a mismatch in Z_0 is very small, (6.12) approximately represents also the mismatch case (6.13) with $p_{Ls} = p_{Cs} \approx 0.5 \cdot 7.2\% = 3.6\%$.

$$\begin{pmatrix} + \\ 0 \\ + \end{pmatrix} \rightarrow \begin{pmatrix} f_{0,1} < f_{0,2} \\ Z_{0,1} > Z_{0,2} \\ h_1 < h_2 \end{pmatrix} \qquad \begin{pmatrix} + \\ 0 \\ - \end{pmatrix} \rightarrow \begin{pmatrix} f_{0,1} < f_{0,2} \\ Z_{0,1} > Z_{0,2} \\ h_1 < h_2 \end{pmatrix} \tag{6.12}$$

$$\begin{pmatrix} + \\ + \\ + \end{pmatrix} \rightarrow \begin{pmatrix} f_{0,1} < f_{0,2} \\ Z_{0,1} = Z_{0,2} \\ h_1 < h_2 \end{pmatrix} \qquad \begin{pmatrix} + \\ + \\ - \end{pmatrix} \rightarrow \begin{pmatrix} f_{0,1} < f_{0,2} \\ Z_{0,1} = Z_{0,2} \\ h_1 < h_2 \end{pmatrix}. \tag{6.13}$$

The comparison between measured and calculated load sharing factor K_{sh} is shown in Fig. 6.10. It can be observed that the overall characteristic of the load sharing is quite well represented by the mathematical model. But it must be stated that the load sharing imbalance is over-estimated by the model especially in the range $1 < F_n < 1.4$. This modeling error cannot be completely assigned to a single root cause, since several known effects that are not covered by the model may superimpose. For accurate model verification at least the SR operation has to be taken into account, e.g. by not using SR but pure diode rectification. However, for the used prototype this was not possible due to thermal limits of the assembly. Nevertheless the conclusion of the load sharing analysis stays valid. The load sharing between interleaved operated paralleled LLC converters is generally too sensitive to component value mismatches to be applied in a reliable way.

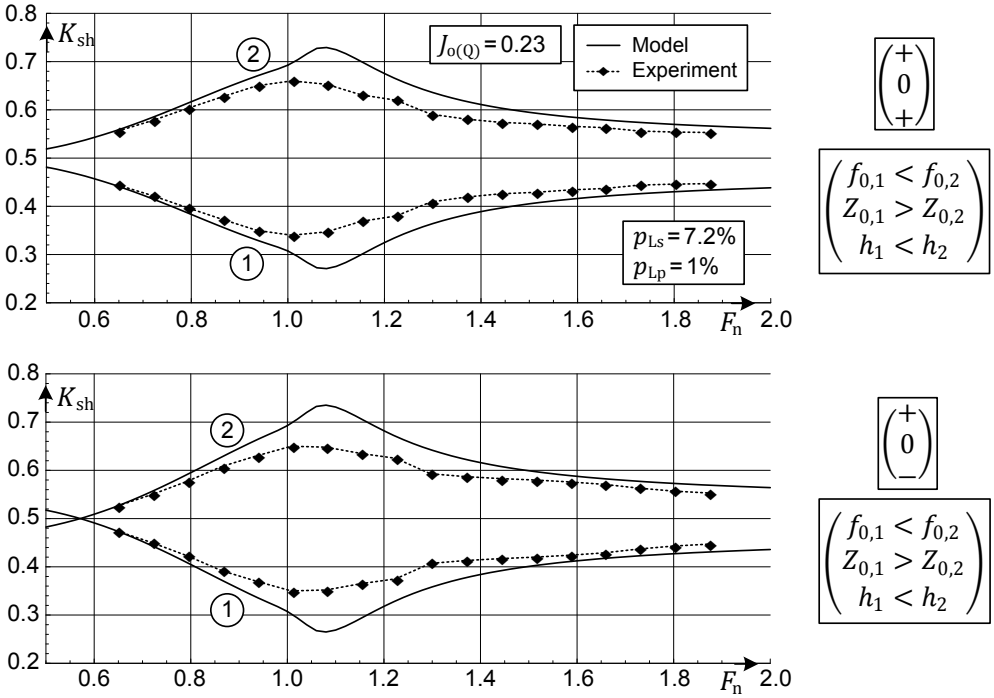

Fig. 6.10: Comparison between calculated and measured load sharing factor K_{sh} for the exemplary value mismatches (6.12) resp. (6.13) at $h = 11.5$, $d = 6.6\%$; the output loading accords to roughly 60% of the prototype's nominal output power.

Also the exemplary value mismatch given by part one of (6.12) was used to verify the mathematical model for the DDL functionality. A comparison between calculated and measured DC-link voltages $V_{DL,1}$ and $V_{DL,2}$ is shown by Fig. 6.11. It is observed that the DC-link voltage difference is predicted with feasible accuracy. The error in the prediction of the absolute DC-link voltage is below 1%. The slightly higher DC-link voltage compared to the prediction can be explained by the additional voltage drop generated by the non-ideal SR operation.

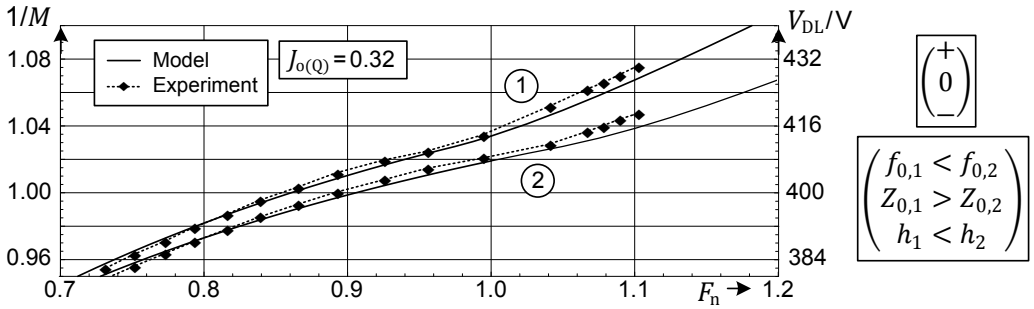

Fig. 6.11: Comparison between calculated and measured normalized DC-link voltages $1/M_1$ and $1/M_2$ and DC-link voltages $V_{DL,1}$ and $V_{DL,2}$ at balanced output currents $I_{o,1} = I_{o,2}$ for the exemplary value mismatch part one of (6.12) at $h = 11.5$, $d = 6.6\%$.

The mathematical modeling of the steady-state DC-DC gain according to Fig. 6.11 is sufficient for a converter design employing the DDL concept. The circuit designer can easily estimate the required tolerance class for the resonant circuit components. Another topic is the dynamic behavior of the interleaved operated LLC converter. But a mathematical description of this is not in the scope of this work. Instead it is noted, that the prototype tests did not yield

any intrinsic instabilities of the parallel structure of two LLC converters throughout every operating condition. Hence without mathematical proof the stability of the structure is assumed, provided that the specific ratio between the DC-link capacitance and the nominal output power is in the same range as in the prototype. Hereby the proportionality between the nominal output power and the characteristic impedance Z_0 for a specified design method is considered, too. For the prototype the ratio is 560 µF / 1500 W ≈ 370 nF/W. The dynamic stability of the DDL in a certain operating range is shown in Fig. 6.12, at which the control concept of [Figge5] is applied. In this control concept the paralleled LLC converters are treated as a single LLC converter, hence no structural changes to the typical single output voltage control loop of a not paralleled LLC converter are made. In Fig. 6.12 the common output of the LLC converters is step-load excited by 50% of the nominal output power, which leads to low frequent settling oscillations of the DC-link voltage. By the movement of the DC-link voltages a certain operating frequency range of the LLC converters is passed through. Thereby no instabilities, e.g. oscillations between the paralleled LLC converters, can be observed. Instead the resonant current envelopes and DC-link voltages track in close agreement between the both converters.

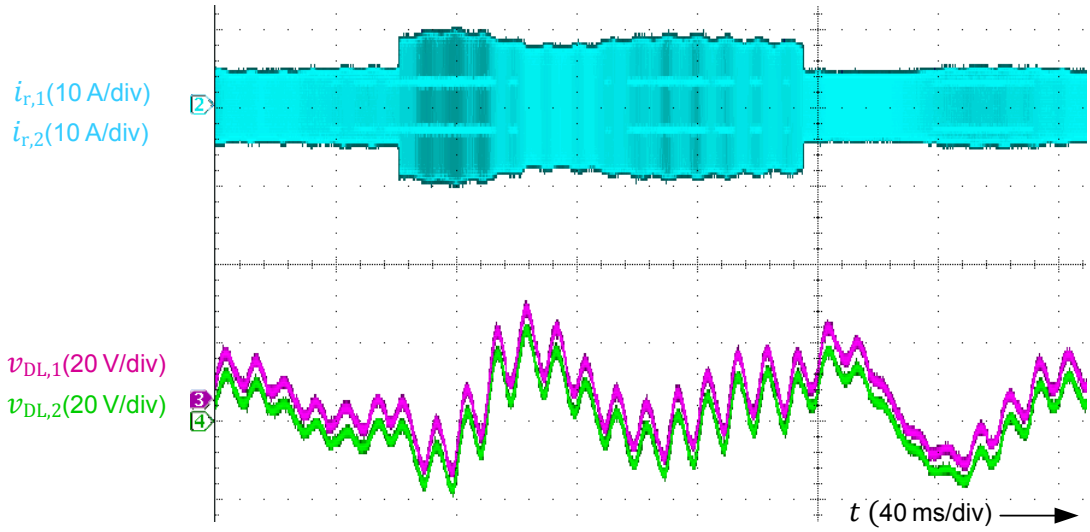

Fig. 6.12: Measured waveforms within the prototype's LLC converters with the DDL concept applied. Ch 1 ($i_{r,1}$) 10 A/div, Ch 2 ($i_{r,2}$) 10 A/div, Ch 3 (AC part of $V_{DL,1}$) 20 V/div, Ch 4 (AC part of $V_{DL,2}$) 20 V/div. Channels 1 and 2 have the same y-position.

7 Conclusion

The industrial adoption of the LLC resonant converter and its usage in power supplies for information and communication technology installations is already on the way. State-of the art solutions for modeling, design, control, short-circuit robustness and interleaved operation for high output currents exist, but are neither satisfactory nor optimized in detail, and hence laid the foundation of this work. The following achievements and results are claimed in this thesis:

- Design
  The complete interdependence of the four basic design variables of the LLC resonant converter (n: transformer turns ratio, $L_\mathrm{s}, L_\mathrm{p}$: resonant inductances, C_s: resonant capacitance) yields a multi-dimensional design space which is non-linearly constrained by the requirements of the converter application. The design optimization with respect to efficiency and volume of the circuit components is complex but can basically be addressed by Peak Gain placement, which is based on the minimization of the reactive power within the resonant circuit. The Peak Gain placement itself is inherently independent of the absolute switching frequency level, i.e. it can be performed with normalized switching frequency representation. Moreover it does not cover the consideration of the design constraints, which has to be performed additionally.
  The design optimization utilizing a numerical optimization solver as proposed in this thesis takes the absolute switching frequency level and all design constraints in a universal manner into account. This facilitates the analysis of design constraint influences and the absolute switching frequency level on the optimal design result. The analysis of the LLC converter for application in an exemplary IT PSU shows that the peak gain requirement has by far the biggest influence on the converter efficiency if the allowed switching frequency range is limited. But if the resonance frequency is a free design parameter, the optimal efficiency result has a quite low dependence on the design constraints and the switching frequency level. All partial load efficiency optima are located within the range of 99.0% to 99.2% on the basis of the considered loss models.

- Modeling
  The inclusion of resistive damping into the exact time domain model on the one hand facilitates more precise prediction of the DC-DC gain and on the other hand enables the normalized representation of the power balance between two interleaved operated LLC resonant converters. The inclusion of resistive damping is necessary due to the high sensitivity of the resistive damping to the power balance.

- Control
  The LLC converter exhibits a strong variation of its control-to-output transfer function in dependence on the operating region. Based on a detailed analysis of the dynamic behavior an adaptive compensator approach is successfully employed and tested. The adaptive compensator approach for the output voltage regulation enables a cross-over frequency higher than 1 kHz within the relevant switching frequency range and at output loads higher than 50% of the nominal load. Especially in the above resonance region the plant characteristic has a disadvantageous dependence on the output loading. Thus an optimal compensator would require adapting its parameters with the output loading in addition to the switching

frequency. Further improvements to the output voltage control quality of the LLC resonant converter are expected by the employment of current mode control. But even though some publications exist on this topic ([Jang], [Jang2]), no implementation method suitable for industrial adoption is known due to insufficient bandwidth and accuracy.

In consequence of a lack of suitable current mode control methods for the LLC resonant converter, the overload-protection and output current limitation of the LLC converter requires additional measures. It is demonstrated that a novel method based on the resonant capacitor clamping approach is able to realize constant output current limitation for the LLC converter.

- Interleaved operation for high output currents
  The popular interleaving configuration of converters can be also applied for the LLC resonant converter if provisions for the power balance are implemented. The power balance is especially affected by differing resonance frequencies and has unfeasible imbalance even if tight circuit element tolerances of ±2.5% are presumed. As a work-around the power balancing by means of separated input voltages can be used in IT PSUs, which enables a reliable industrial adoption of the LLC resonant converter even at high output power at low output voltage levels.

Concluding the described results, the author believes that his investigations will support a better and broader industrial application of the LLC resonant converter and a shortened development time. This is considered not only for existing but also for future requirements to the electrical performance figures, which includes the upcoming evolution of the applied switching frequencies into the MHz range.

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9 Appendix

9.1 Solutions of IVPs of LLC Resonant Converter Time Domain Analysis

First interval ($t_0 < t < t_1$) of CCMA and DCMB2 mode:

DE:

$$i_\mathrm{r}'' + \frac{R_\mathrm{s}}{L_\mathrm{s}} i_\mathrm{r}' + \frac{1}{L_\mathrm{s} C_\mathrm{s}} i_\mathrm{r} = 0 \qquad j_\mathrm{r}'' + d\omega_0 j_\mathrm{r}' + \omega_0^2 j_\mathrm{r} = 0$$

General solution:

$$i_\mathrm{r}(t) = K_{\mathrm{s}01} e^{\alpha t} \sin(\beta t) + K_{\mathrm{c}01} e^{\alpha t} \cos(\beta t)$$

$$j_\mathrm{r}(\theta) = K_{\mathrm{s}01\mathrm{n}} e^{\alpha\,\theta/\omega_0} \sin(\beta\,\theta/\omega_0) + K_{\mathrm{c}01\mathrm{n}} e^{\alpha\,\theta/\omega_0} \cos(\beta\,\theta/\omega_0)$$

with

$$\alpha = -\frac{d}{2}\omega_0, \;\; \beta = \sqrt{1 - \left(\frac{d}{2}\right)^2}\,\omega_0, \text{ provided } d < 2$$

Solving the IVP by applying (3.19) the time domain waveforms are derived as

case $V_\mathrm{base} = V_\mathrm{g}$:

$$j_\mathrm{r}(\theta) = e^{-\frac{d}{2}\theta} \left[j_{\mathrm{r},0} \cos(\beta\,\theta/\omega_0) - \frac{\left(-1 + d/2\, j_{\mathrm{r},0} + M + m_{\mathrm{Cs},0}\right) \sin(\beta\,\theta/\omega_0)}{\beta/\omega_0} \right],$$

$$v_\mathrm{Cs}(\theta) = 1 - M + e^{-\frac{d}{2}\theta} \left[\left(-1 + M + m_{\mathrm{Cs},0}\right) \cos(\beta\,\theta/\omega_0) + \frac{\left(j_{\mathrm{r},0} + d/2\left(-1 + M + m_{\mathrm{Cs},0}\right)\right) \sin(\beta\,\theta/\omega_0)}{\beta/\omega_0} \right],$$

case $V_\mathrm{base} = nV_\mathrm{o}$:

$$j_\mathrm{r}(\theta) = e^{-\frac{d}{2}\theta} \left[j_{\mathrm{r},0} \cos(\beta\,\theta/\omega_0) - \frac{\left(-1/M + \left(1 + d/2\, j_{\mathrm{r},0} + m_{\mathrm{Cs},0}\right)\right) \sin(\beta\,\theta/\omega_0)}{\beta/\omega_0} \right],$$

$$v_\mathrm{Cs}(\theta) = \frac{1}{M} - 1 + e^{-\frac{d}{2}\theta} \left[\left(-1/M + 1 + m_{\mathrm{Cs},0}\right) \cos(\beta\,\theta/\omega_0) + \frac{\left(j_{\mathrm{r},0} + d/2\left(-1/M + 1 + m_{\mathrm{Cs},0}\right)\right) \sin(\beta\,\theta/\omega_0)}{\beta/\omega_0} \right].$$

Second interval ($t_1 < t < t_2$) of CCMA mode:

DE:

$$i_\mathrm{r}'' + \frac{R_\mathrm{s}}{L_\mathrm{s}} i_\mathrm{r}' + \frac{1}{L_\mathrm{s} C_\mathrm{s}} i_\mathrm{r} = 0 \qquad j_\mathrm{r}'' + d\omega_0 j_\mathrm{r}' + \omega_0^2 j_\mathrm{r} = 0$$

General solution:

$$i_\mathrm{r}(t) = K_\mathrm{s12A} e^{\alpha t} \sin(\beta t) + K_\mathrm{c12A} e^{\alpha t} \cos(\beta t)$$

$$j_\mathrm{r}(\theta) = K_\mathrm{s12An} e^{\alpha\,\theta/\omega_0} \sin(\beta\,\theta/\omega_0) + K_\mathrm{c12An} e^{\alpha\,\theta/\omega_0} \cos(\beta\,\theta/\omega_0)$$

with

$$\alpha = -\frac{d}{2}\omega_0, \;\; \beta = \sqrt{1 - \left(\frac{d}{2}\right)^2}\,\omega_0, \text{ provided } d < 2$$

Solving the IVP by applying (3.24) the time domain waveforms are derived as

case $V_\mathrm{base} = V_\mathrm{g}$:

$$j_\mathrm{r}(\theta) = e^{-\frac{d}{2}\theta} \left[j_{\mathrm{r},1} \cos(\beta\,\theta/\omega_0) - \frac{\left(1 + d/2\, j_{\mathrm{r},1} + M + m_{\mathrm{Cs},1}\right) \sin(\beta\,\theta/\omega_0)}{\beta/\omega_0} \right]$$

$$v_\mathrm{Cs}(\theta) = -1 - M + e^{-\frac{d}{2}\theta} \left[\left(1 + M + m_{\mathrm{Cs},1}\right) \cos(\beta\,\theta/\omega_0) + \frac{\left(j_{\mathrm{r},1} + d/2\left(1 + M + m_{\mathrm{Cs},1}\right)\right) \sin(\beta\,\theta/\omega_0)}{\beta/\omega_0} \right],$$

case $V_\mathrm{base} = nV_\mathrm{o}$:

$$j_\mathrm{r}(\theta) = e^{-\frac{d}{2}\theta} \left[j_{\mathrm{r},1} \cos(\beta\,\theta/\omega_0) - \frac{\left(1/M + \left(1 + d/2\, j_{\mathrm{r},1} + m_{\mathrm{Cs},1}\right)\right) \sin(\beta\,\theta/\omega_0)}{\beta/\omega_0} \right],$$

$$v_\mathrm{Cs}(\theta) = -\frac{1}{M} - 1 + e^{-\frac{d}{2}\theta} \left[\left(1/M + 1 + m_{\mathrm{Cs},1}\right) \cos(\beta\,\theta/\omega_0) + \frac{\left(j_{\mathrm{r},1} + d/2\left(1/M + 1 + m_{\mathrm{Cs},1}\right)\right) \sin(\beta\,\theta/\omega_0)}{\beta/\omega_0} \right].$$

Second interval ($t_1 < t < t_2$) of DCMB2 mode:

DE:

$$i_\mathrm{r}'' + \frac{R_\mathrm{s}}{L_\mathrm{s}+L_\mathrm{p}} i_\mathrm{r}' + \frac{1}{(L_\mathrm{s}+L_\mathrm{p})C_\mathrm{s}} i_\mathrm{r} = 0 \qquad j_\mathrm{r}'' + \frac{d\omega_0}{(1+h)} j_\mathrm{r}' + \frac{\omega_0^2}{(1+h)} j_\mathrm{r} = 0$$

General solution:

$$i_\mathrm{r}(t) = K_{\mathrm{s12B}} e^{\gamma t} \sin(\delta t) + K_{\mathrm{c12B}} e^{\gamma t} \cos(\delta t)$$

$$j_\mathrm{r}(\theta) = K_{\mathrm{s12Bn}} e^{\gamma\, \theta/\omega_0} \sin(\delta\, \theta/\omega_0) + K_{\mathrm{c12Bn}} e^{\gamma\, \theta/\omega_0} \cos(\delta\, \theta/\omega_0)$$

with

$$\gamma = -\frac{d}{2(1+h)}\omega_0, \quad \delta = \sqrt{\frac{1}{1+h} - \left(\frac{d}{2(1+h)}\right)^2}\,\omega_0, \text{ provided } d < 2\sqrt{1+h}$$

Solving the IVP by applying (3.28) the time domain waveforms are derived as

case $V_{\mathrm{base}} = V_\mathrm{g}$:

$$j_\mathrm{r}(\theta) = e^{-\frac{d}{2(1+h)}\theta} \left[j_{\mathrm{r},1} \cos(\delta\, \theta/\omega_0) - \frac{\left(-1 + d/2\, j_{\mathrm{r},1} + m_{\mathrm{Cs},1}\right) \sin(\delta\, \theta/\omega_0)}{\delta/\omega_0 (1+h)} \right]$$

$$v_{\mathrm{Cs}}(\theta) = 1 + e^{-\frac{d}{2(1+h)}\theta} \left[\left(-1 + m_{\mathrm{Cs},1}\right) \cos(\delta\, \theta/\omega_0) + \frac{\left((1+h) j_{\mathrm{r},1} + d/2\left(-1 + m_{\mathrm{Cs},1}\right)\right) \sin(\delta\, \theta/\omega_0)}{\delta/\omega_0 (1+h)} \right],$$

case $V_{\mathrm{base}} = nV_\mathrm{o}$:

$$j_\mathrm{r}(\theta) = e^{-\frac{d}{2(1+h)}\theta} \left[j_{\mathrm{r},1} \cos(\delta\, \theta/\omega_0) - \frac{\left(-1/M + d/2\, j_{\mathrm{r},1} + m_{\mathrm{Cs},1}\right) \sin(\delta\, \theta/\omega_0)}{\delta/\omega_0 (1+h)} \right],$$

$$v_{\mathrm{Cs}}(\theta) = \frac{1}{M} + e^{-\frac{d}{2(1+h)}\theta} \left[\left(-1/M + m_{\mathrm{Cs},1}\right) \cos(\delta\, \theta/\omega_0) + \frac{\left((1+h) j_{\mathrm{r},1} + d/2\left(-1/M + m_{\mathrm{Cs},1}\right)\right) \sin(\delta\, \theta/\omega_0)}{\delta/\omega_0 (1+h)} \right].$$

9.2 Empirical Modeling Results of Magnetic Components Based on Measurements and Datasheet Values

9.2.1 Core Losses

Fig. 9.1 shows the datasheet supplied core loss density characteristic of DMR95 MnZn ferrite material for $T_c = 25°C$ and $T_c = 100°C$. Based on this graph a curve fitting functional description is derived given by

$$P_{v,core}(f, \hat{B}, T_c) = k \cdot f^{\alpha} \cdot \hat{B}^{\beta} \cdot \left(1 + ct1 \cdot (T_c - 25°C) \cdot k_T(\hat{B}) + ct2 \cdot (T_c - 25°C)^2\right).$$

Because also the shape of the curves is temperature dependend especially for $f < 200$ kHz, the temperature compensation term is equipped with the flux dependend factor $k_T(\hat{B})$ according to

$$k_T(\hat{B}) = \begin{cases} 1.3 & \text{if} \quad \hat{B} < 70 \cdot 10^{-3}\text{H} \\ 1.3 + 3\text{H}^{-1} \cdot \left(70 \cdot 10^{-3}\text{H} - \hat{B}\right) & \text{otherwise} \end{cases}.$$

The resulting graph is shown in the diagram for $T_c = 65°C$. The accuracy of the curve fitting is optimized for frequencies $f < 100$ kHz, since this is the most probable switching frequency range resulting from the optimal design procedure applied in this work.

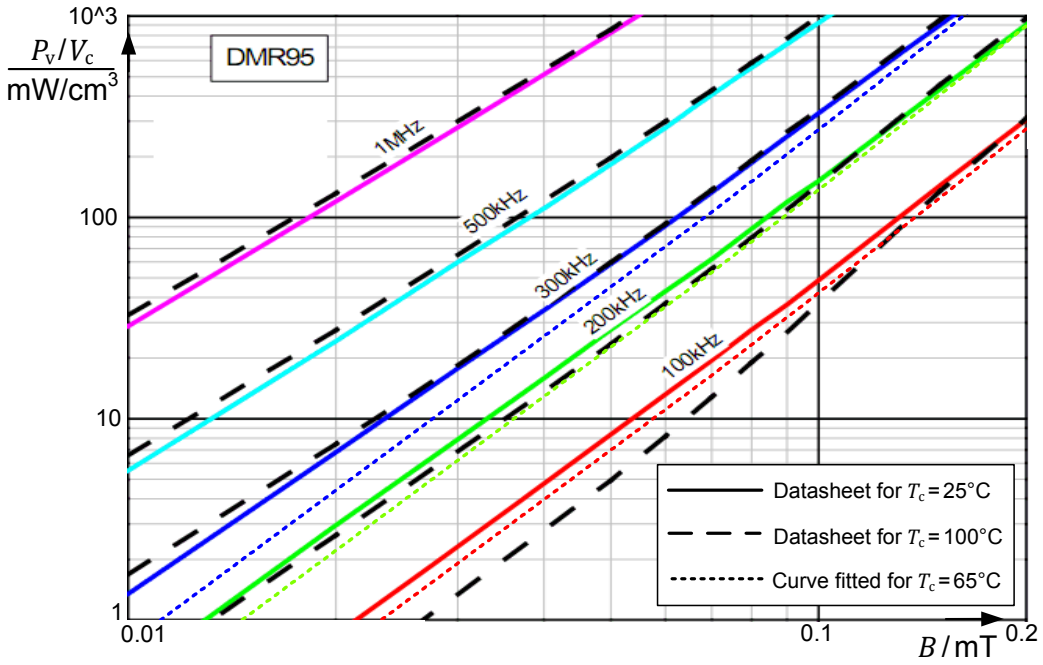

Fig. 9.1: Power loss density of DMR95 core material: Comparison between datasheet supplied graphs [DMEGC] and curve fitted values.

9.2.2 Copper Losses

The copper losses are measured according to the descriptions in Chapter 3.2.3 and in particular Chapter 3.2.3.5. Fig. 9.2 shows the measurement results for the resonant choke and the determined polynomial fitting curve. The fitting curve is given by

$$R_{\mathrm{AC\_ch}}(f, N_{\mathrm{ch}}, T_{\mathrm{w}}) = (3.411 \cdot 10^{-12} \cdot (f/\mathrm{Hz})^2 + 1.602 \cdot 10^{-7} \cdot (f/\mathrm{Hz}) + 0.01394) \\ (N_{\mathrm{ch}}/15)^2 \left(1 + 0.004\ \mathrm{K}^{-1}(T_{\mathrm{w}} - 25°\mathrm{C})\right) \Omega\,.$$

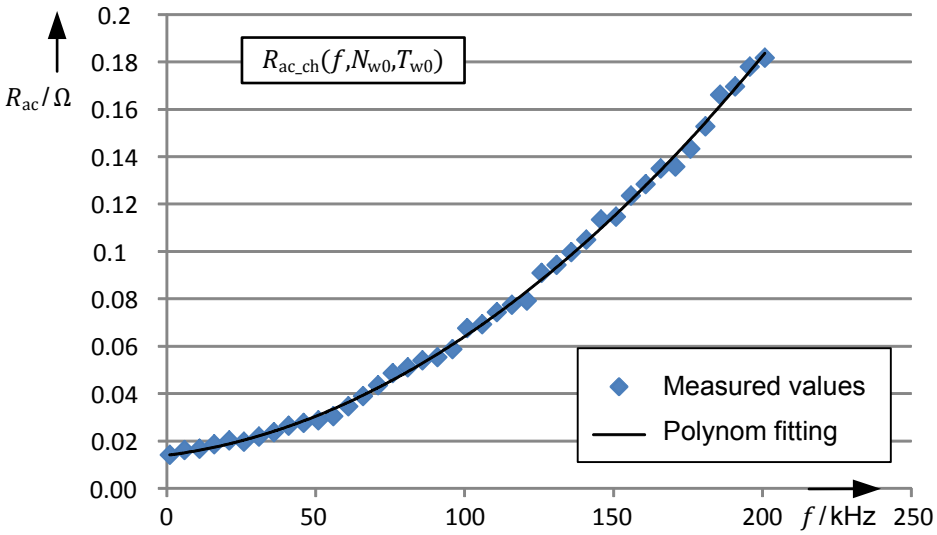

Fig. 9.2: Small-signal measurement of the R_{AC} characteristic of the resonant choke

Fig. 9.3 shows the measurement results for the short-circuit resistance of the transformer and according polynomial fitting. The fitting curve is given by

$$R_{\mathrm{AC\_xf\_p}}(f, N_{\mathrm{p}}, T_{\mathrm{w}}, b_{\mathrm{w}}) = (1.514 \cdot 10^{-12} \cdot (f/\mathrm{Hz})^2 + 3.197 \cdot 10^{-7} \cdot (f/\mathrm{Hz}) + 0.06346) \\ (N_{\mathrm{p}}/37)^2 \left(1 + 0.004\ \mathrm{K}^{-1}(T_{\mathrm{w}} - 25°\mathrm{C})\right) (b_{\mathrm{w}}/(0.055\ \mathrm{m}))\ \Omega\,.$$

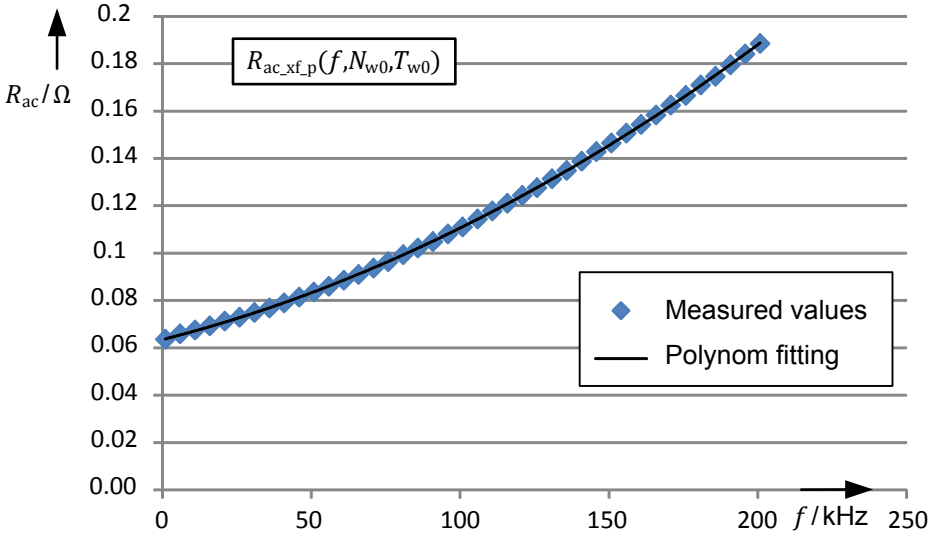

Fig. 9.3: Small-signal measurement of the R_{AC} characteristic of the the transformer with shorted secondary winding

Fig. 9.4 shows the measurement results for the primary winding of the transformer and the according polynomial fitting given by

$$R_{\mathrm{AC\_m\_p}}(f, N_\mathrm{p}, T_\mathrm{w}, b_\mathrm{w}) = (9.972 \cdot 10^{-11} \cdot (f/\mathrm{Hz})^2 + 2.504 \cdot 10^{-7} \cdot (f/\mathrm{Hz}) + 0.2057) \\ (N_\mathrm{p}/37)^2 \left(1 + 0.004\ \mathrm{K}^{-1}(T_\mathrm{w} - 25°\mathrm{C})\right) (b_\mathrm{w}/(0.055\ \mathrm{m}))\ \Omega\,.$$

Furthermore it shows the polynomial fitting curve including a compensation for the core losses of the transformer that are superimposed during the small-signal measurement due to the small air-gap of the transformer. The compensation function is given by the factor

$$K_{\mathrm{cr\_cmp}}(f) = \begin{cases} 1 & \text{for} \quad f < 25\ \mathrm{kHz} \\ \dfrac{1}{((2 + (f/(25\ \mathrm{kHz}))^{1.3})/3)} & \text{for} \quad f \geq 25\ \mathrm{kHz} \end{cases}\,.$$

The compensation function is derived from large-signal measurement results on a PQ5050 core with $l_\mathrm{g} = 0.6$ mm and $N_\mathrm{p} = 22$. It is therefore not an exactly determined function for the investigated transformer but needs to be considered as an approximation.

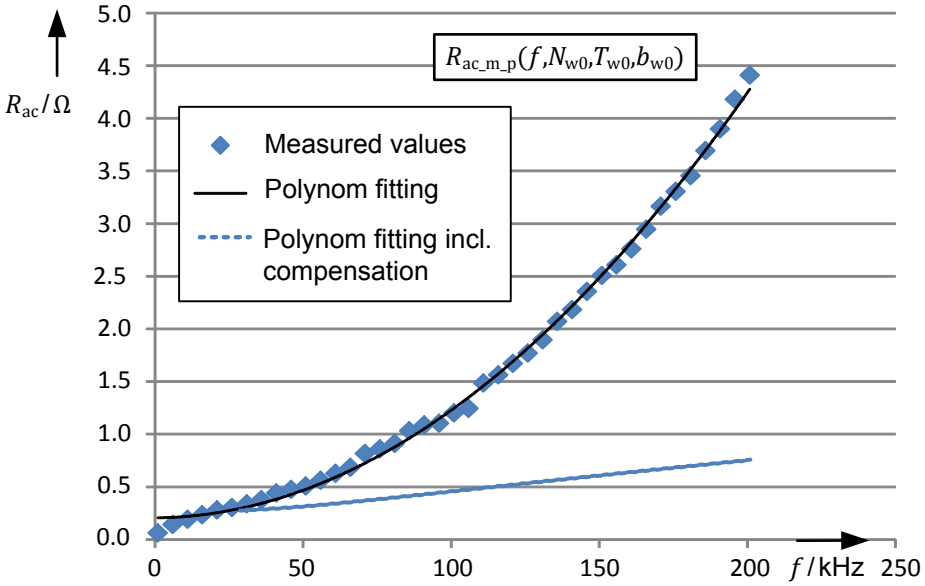

Fig. 9.4: Small-signal measurement of the R_{AC} characteristic of the the transformer's primary winding and the applied R_{AC} characteristic including compensation for core losses.

List of Publications

H. Figge, T. Grote, N. Fröhleke et al., "Paralleling of LLC resonant converters using frequency controlled current balancing," IEEE Power Electronics Specialists Conference (PESC), 2008

H. Figge, T. Grote, N. Fröhleke et al., "Overcurrent protection for the LLC resonant converter with improved hold-up time," Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2011

H. Figge, N. Fröhleke, J. Böcker et al., "Cost-Effective Implementation of a Digitally Controlled LLC Resonant Converter for Application in Server- and Telecom-PSUs," International Exhibition and Conference for Power Electronics, Intelligent Motion and Power Quality (PCIM) Europe, 2012

H. Figge, T. Grote, F. Schafmeister et al., "Two-phase interleaving configuration of the LLC resonant converter - Analysis and experimental evaluation," 39th Annual Conference of the IEEE Industrial Electronics Society (IECON), 2013

Patents

H. Figge and F. Schafmeister, "Resonant capacitor clamping circuit in resonant converter," United States Patent 8,611,115, 2013

H. Figge, F. Schafmeister and T. Grote, "LLC BALANCING," United States Patent Application 20140009985, 2014

Co-Author

T. Grote, H. Figge, N. Fröhleke et al., "Semi-Digital Interleaved PFC Control with Optimized Light Load Efficiency," Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2009

T. Grote, F. Schafmeister, H. Figge et al., "Adaptive digital slope compensation for peak current mode control," IEEE Energy Conversion Congress and Exposition (ECCE), 2009

T. Grote, H. Figge, N. Fröhleke et al., "Digital control strategy for multi-phase interleaved boundary mode and DCM boost PFC converters," IEEE Energy Conversion Congress and Exposition (ECCE), 2011

T. Grote, H. Figge and F. Schafmeister, "Today's Relevance of Digital Control in Server- and Telecom Power Supplies," International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), 2015

C. Henkenius, N. Fröhleke, J. Böcker et al., "DCM detection for on-line adaption of control parameters for totem-pole PFC rectifier," IEEE International Conference on Industrial Technology (ICIT), 2015